

APPLICATION NOTE

ANP083 | Adapter PCB for filtering electromagnetic interference on an RS-485 interface



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01. INTRODUCTION

As a result of the constantly growing number of applications based on networked communication via data lines, it is becoming increasingly important to ensure trouble-free operation as well as the safety of electrical systems and devices. By filtering directly at the interface, interference emissions, electrostatic discharges (ESD) and fast transients (burst) are prevented from entering the system and thus negatively influencing the operating performance. To verify the EMC properties of electrical systems, special tests are carried out in accredited EMC test laboratories. If these tests are not passed, the application has to be revised. In order to simplify this process, an adapter stick was designed which contains a complete filter circuit for the selected application and can be plugged into the appropriate interface. The simple plug-in allows a quick check of the filter effect on the system to be tested. Once the tests are passed with the filter stick inserted, the circuit can be implemented in the system.

This application note describes the design of such a filter stick for the RS-485 transmission standard. Since no connector is defined for RS-485 applications, 9-pin D-SUB connectors and the pin assignment defined by PROFIBUS, shown in Table 1, have been selected. This ensures the widest possible range of applications.

Pin-Number	Purpose
3	Dataline B
5	Ground
6	Supply voltage line
8	Dataline A

Table 1: Pin assignment

Before the selection of the components for the filter circuit is made, the required effect is defined. The selected RS-485 interface requires a high level of protection against common mode interference over the entire frequency range. In addition, all signals with frequencies that do not correspond to the transmission standard should be attenuated. There must also be protection against overvoltages on the data lines. The supply voltage line should provide a uniform and interference-free voltage.

02. SELECTION OF COMPONENTS

In this section, the components necessary to achieve the desired filter effects are selected and dimensioned. Typical procedures are calculations by transfer functions and simulations. There are helpful online tools, such as **REDEXPERT** from Würth Elektronik, to compare characteristic data and real measured values of individual components with each other and thus select the suitable component for the circuit. It is classified into filters for the data line and the supply voltage line, since different requirements are placed on the filters.

2.1 Filter Circuit of the data lines

First a common mode choke is selected. Here it is necessary to determine the frequency at which the line could act as an antenna and thus cause common-mode interference. This limit is reached when the line length is equal to a quarter of the wavelength λ . Beyond this length, the line can no longer be considered a lossless short-circuit, since the parasitic effects reach dimensions that cannot be neglected. Relevant for this calculation is the maximum possible cable length for RS-485 applications, which is specified at 1.2 km. From equation (1) follows a value of 4.8 km for the wavelength λ . With this, the cut-off frequency $f_{\lambda/4}$ with eq.(2) can then be calculated as follows. It is done for the first assumption of light in vacuum. This may vary depending on the transmission path used.

$$1.2 \text{ km} = \frac{\lambda}{4} \tag{1}$$

$$f_{\lambda/4} = \frac{c}{\lambda} = \frac{300,000 \frac{\text{km}}{\text{s}}}{4.8 \text{ km}} = 62.5 \text{ kHz} \tag{2}$$

Since the frequency increases with a decreasing cable length, it is necessary that the common mode choke already has a high attenuation at 62.5 kHz and increases for larger frequencies. Therefore, the component WE-SL2 [744222](#) is selected, which is shown in Figure 1.

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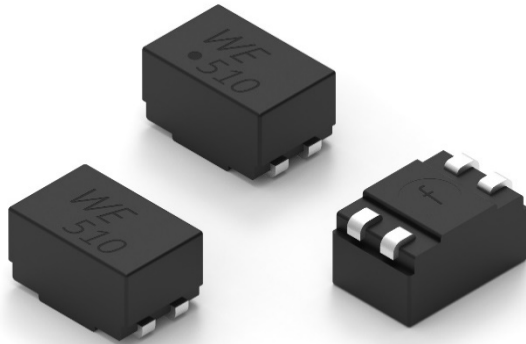


Figure 1: WE SL2 744222

Figure 2 shows the common mode insertion loss of the component. It can be seen that the component already has a high attenuation of approx. 16.5 dB at the frequency $f_{\lambda/4} = 62.5$ kHz.

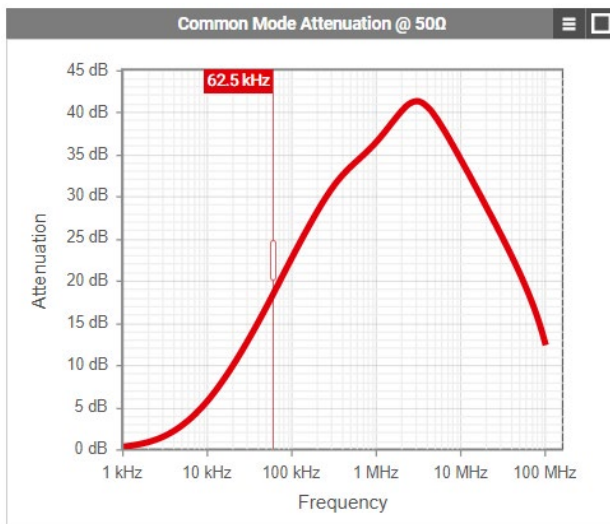


Figure 2: Common mode insertion loss WE-SL2 744222

The ESD suppressors for overvoltage protection are then selected. An important parameter here is the value of the applied voltage. As the data lines need to be protected in this case, an ESD suppressor with a voltage specification of 5 V is selected. There are ESD suppressors specially specified for RS-485 applications with the article designation WE-VE [823 570 505 60](#) in the Würth Elektronik catalog. Another value relevant for the filter circuit is the capacitance, which is included in the total capacitance of the circuit. The capacitance of this component is 56 pF.

Now the filter is already prepared for common mode noise and overvoltages. It still needs sufficient protection against differential mode interferences.

The last components used to protect the data lines are capacitors. Since all other components have already been selected, the required total capacitance, which should lead to

the desired attenuation against differential mode interferences can be calculated using a transfer function. In order to set this up, the overall equivalent circuit for differential mode must be considered. This consists of the termination resistors at the beginning and end of the line, an inductance and a capacitance. Figure 3 illustrates this structure.

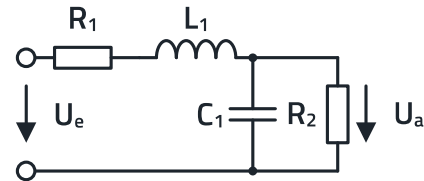


Figure 3: Structure of the complete system

From this setup the following equation (3) is derived for the transfer function.

$$\frac{U_a}{U_e} = \frac{(X_{C1} \parallel R_2)}{R_1 + X_{L1} + (X_{C1} \parallel R_2)} \quad (3)$$

$$\frac{U_a}{U_e} = \frac{\frac{X_{C1} \cdot R_2}{X_{C1} + R_2}}{R_1 + X_{L1} + \frac{X_{C1} \cdot R_2}{X_{C1} + R_2}}$$

X_L is the reactance of the inductor L_1 and X_C the reactance of the capacitor C_1 . According to the standard, the maximum transmission rate of the RS-485 standard is 12 Mbps. Since RS-485 transmission uses NRZ (Non Return to Zero) encoding, the transmission frequency f_{\max} can be calculated as follows.

$$f_{\max} = \frac{\text{maximum transfer rate}}{2} \quad (4)$$

$$f_{\max} = \frac{12 \text{ Mbps}}{2} = 6 \text{ MHz}$$

Since all signals up to this frequency are to be transmitted unhindered, a desired attenuation of 3 dB at a cut-off frequency $f_{\text{cut-off}} = 15$ MHz is specified to ensure a certain buffer. Due to the design of the circuit as a voltage divider, a basic attenuation of 6 dB must also be included in this value. The total attenuation is calculated to be 9 dB, which in turn corresponds to a total voltage ratio of approx. 0.35. In this case, the voltage ratio of approx. 0.35 is the amount of a previously unknown, complex number ($\rightarrow \frac{U_a}{U_e} = Z$). Due to the termination of RS-485 applications, the resistance value for R_1 and R_2 is 120 Ω each. For the value of the differential mode inductance L , the value for the leakage inductance of the

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common mode choke $L_S = 90 \text{ nH}$ is used from the data sheet, since the common-mode inductance is cancelled due to the opposite currents of the signal. By using the cut-off frequency and the leakage inductance, eq. (5) for the reactance X_L of the inductance follows.

$$X_{L1} = j\omega L = j \cdot 2 \pi \cdot 15 \text{ MHz} \cdot 90 \text{ nH} = j \cdot 8.48 \quad (5)$$

The last unknown parameter in the transfer function is the reactance X_C of the capacitance. By changing eq.(3), the following eq.(6) results for X_C .

$$X_{C1} = \frac{Z \cdot R_2 \cdot (X_{L1} + R_1)}{R_2 - Z \cdot (R_1 + R_2 + X_{L1})} \quad (6)$$

Since the reactance of a capacitor does not contain a real part, it can be set to zero. Therefore the formula must be divided into a real part and an imaginary part. By inserting eq.(7) and transforming eq.(6) ,eq.(8) is obtained.

$$Z = a + jb \quad (7)$$

$$X_{C1} = \frac{(a \cdot R_1 \cdot R_2 - j b \cdot X_{L1} \cdot R_2) + j (a \cdot R_2 \cdot X_{L1} + b \cdot R_1 \cdot R_2)}{R_2 - ((a \cdot (R_1 + R_2) - j b \cdot X_{L1}) + j (a \cdot X_{L1} + b \cdot (R_1 + R_2)))} \quad (8)$$

This eq.(8) can be complexly conjugated, so that there is no imaginary part in the denominator, while a complex number remains in the numerator. The real part of this complex number is set to zero and converted to one of the parameters a or b. The real part of this complex number is set to zero. With this equation and equation (9) now two equations for two unknown variables are available. Thus the system of equations can be solved.

$$|Z| \approx 0,35 = \sqrt{a^2 + b^2} \quad (9)$$

The following values result from the calculation with the help of Matlab Simulink:

<u>Real part:</u>	$a \approx 0.23$
<u>Imaginary part:</u>	$b \approx -0.27$
<u>Complex number:</u>	$Z \approx 0.23 - j \cdot 0.27$

The imaginary part then forms the formula (eq.(10)) for X_{C1} .

$$X_{C1} = \frac{R_2 \cdot (a \cdot X_{L1} + a \cdot R_1 + j b \cdot X_{L1} + j b \cdot R_1)}{R_2 - (a + j b) \cdot (X_{L1} + R_1 + R_2)} \quad (10)$$

This results in the following value:

Impedance of the capacitor: $X_{C1} = -j \cdot 58.49 \Omega$

Using the values for X_C and $f_{\text{cut-off}}$ results in eq.(11) for the total capacity of the system.

$$C = \frac{1}{j\omega X_{C1}} \quad (11)$$

$$C = \frac{1}{j \cdot 2 \pi \cdot 15 \text{ MHz} \cdot (-j \cdot 58.49 \Omega)} = 181.38 \text{ pF}$$

To achieve the desired attenuation of 3 dB at 15 MHz, the filter structure must therefore contain a total capacitance of $C = 181.38 \text{ pF}$. The first contribution to this total capacity is made by the ESD suppressors with a capacity of 56 pF each. Since these are parallel to the circuit and connected to ground, only half the capacitance of one component is included, as shown in eq.12.

$$C_{\text{ESD}} = \frac{56 \text{ pF} \cdot 56 \text{ pF}}{56 \text{ pF} + 56 \text{ pF}} = 28 \text{ pF} \quad (12)$$

As a result the two ESD suppressors influence the circuit with a total capacitance of 28 pF.

According to the same principle, two capacitors are built into the circuit. These are used to divert high-frequency interference. Combined with the common-mode choke, this design offers very high protection against common-mode interference over a wide frequency range. A small capacitance is sufficient to achieve the desired effect. Two capacitors with a capacitance of 100 pF are selected. The effect of the capacitors is calculated as with the ESD suppressors. Thus, the two capacitors act with a total of 50 pF on the circuit.

In addition to the common-mode choke and the two capacitors which are connected to ground, a capacitor is inserted between the data lines A and B to counteract to symmetrical interference. Since a capacitance of 78 pF is already present in the system due to the ESD suppressors and the two other capacitors, a capacitance of 100 pF is selected for this capacitor.

By selecting the components, a total capacitance of 178 pF is achieved, which deviates only 3.38 pF from the calculated total capacitance. The deviation is unavoidable due to the fixed capacitance values of the capacitors available in the range of products and has been kept as small as possible with this selection. Since the circuit is to be kept small, only MLCCs are used.

The component selection for the filter circuit is now complete. Figure 4 shows the selected design of the filter circuit for data lines A and B.

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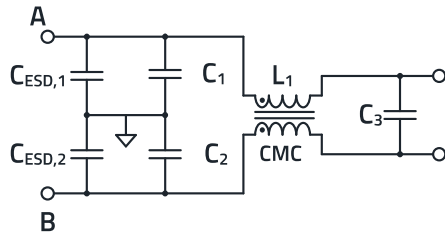


Figure 4: Filter circuit of the data lines

To check if the selected components achieve the desired effect, the circuit in Figure 4 can be simulated using LTspice. The VDE standard EN 55017 specifies that the differential mode test circuit must be simulated via isolators with a winding ratio of 1:1, since the simulation only considers two ports. In addition to the selected filter elements serial resistors at the beginning and the end of the circuit are inserted to take the influence of the impedance matched microstrips on the PCB into account. The datalines of the filter stick where designed with a differential impedance of 120 Ω (=60 Ω per microstrip) to avoid reflections at the ends of the RS-485 bus which are terminated with 120 Ω. Figure 5 shows the standard-compliant symmetrical design of the circuit for testing the attenuation behavior for differential mode signals.

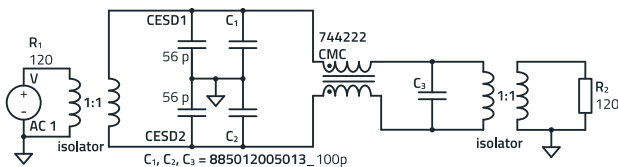


Figure 5: Design of the differential mode test circuit

Figure 6 shows the simulation result for load by differential mode currents as they exist in normal operation. The signal transmission of the entire circuit is displayed, with the Y axis showing the level of differential mode load in dB and the X axis showing the corresponding frequency range from 10 kHz to 1 GHz. Measurement takes place at the output of the circuit.

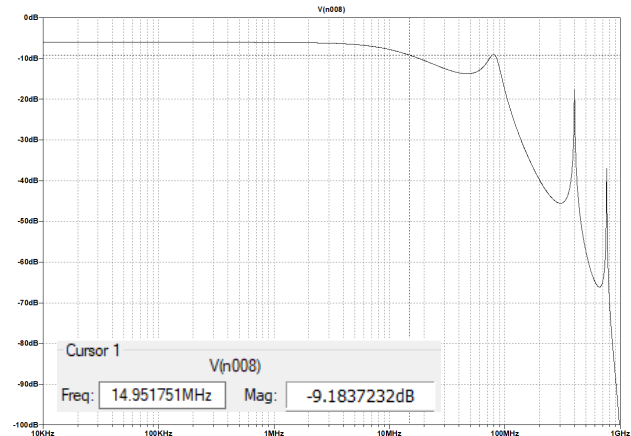


Figure 6: Simulation of the differential mode load (SDD21) on the dataline

The 6 dB basic attenuation is caused, as described above, due to the simulated circuit being designed as a voltage divider. As it can be seen, the signal is not damped in the transmission range of the RS-485 standards (< 6 MHz). The marker point is at approx. 15 MHz and shows an attenuation of about 9.18 dB. This shows that the design with the help of **REDEXPERT** and the calculation by the transfer function leads almost exactly to the desired result. The deviation of 0.18 dB can be explained by the small difference of the used and calculated total capacitance and the fact that models of real components are used for the simulation, while ideal values were assumed for the calculation.

For the simulation of common mode loads, the VDE standard EN 55017 states that the filter circuit must be inserted between the signal generator and the receiver and that the input and output conductors must be connected in parallel. Because of the use of a parallel circuit a serial resistance of 30 Ω was added into the circuit to simulate the 60 Ω per microstrip. Eq.(13) shows the calculation which leads to this value.

$$R_{\text{total}} = \frac{60 \Omega \cdot 60 \Omega}{60 \Omega + 60 \Omega} = 30 \Omega \quad (13)$$

The standard-compliant asymmetrical common mode test circuit is simulated, as shown in Figure 7, with the following circuit.

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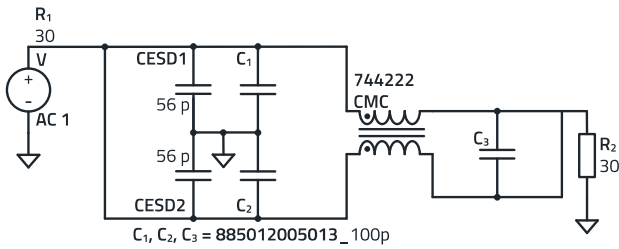


Figure 7: Circuit for simulation of common mode load

Figure 8 shows the simulated result. The 6 dB basic attenuation is also present here. It can be seen that the attenuation already begins to increase from 10 kHz. At the calculated frequency $f_{1/4} = 62.5$ kHz, an attenuation of approx. 23.82 dB is shown. The common-mode choke alone achieved an attenuation of 16.5 dB at this frequency, as shown in Figure 2. The remaining 7.32 dB are due to the additional capacitors. The circuit offers high attenuation to common-mode interference over the entire simulated frequency range.

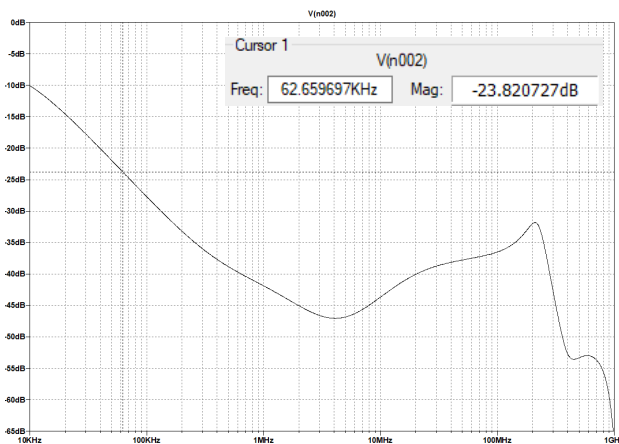


Figure 8: Simulation of the common mode load (SCC21) on the data line

Overall, the simulation shows a good result, both for the damping of unwanted differential mode signals as well as common-mode interference of all kinds, which is why the circuit can be transferred into the design of the filter stick.

2.2 Filter circuit of the supply voltage line

According to the RS-485 transmission standard, a pure DC voltage of 5 V with a current of 200 mA should be applied to the supply voltage line. To obtain such a clean DC voltage, all frequency components must be filtered out, that means a low pass filter is required. Due to the characteristic that the attenuation increases per frequency decade with each pole of the filter, a third order low pass is selected for the filter circuit. The attenuation is therefore 60 dB per frequency decade. A low-pass, as shown in Figure 9, consists of two capacitors and an inductor.

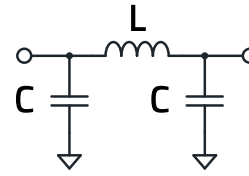


Figure 9: 3rd order low pass filter

As a result of its design, which is looking like a π , it is often referred to as a Pi filter. In order to select suitable components that meet the requirements of the filter, the online tool REDEXPERT is used.

The first step is to select the right inductance. It should be noted that a current of 200 mA flows on the supply voltage line. This is important because an inductor designed for lower currents would be strongly heated. To prevent this, a PCB ferrite with a rated current of $I_R = 500$ mA is selected. This means that the ferrite heats up only 40 K at a current of 500 mA. In addition, the inductance should counteract currents and voltages with frequency components with a certain impedance. The following Figure 10 shows the impedance curve of the selected PCB ferrite, which increases with frequency. Furthermore REDEXPERT makes it possible to display impedance curves at different currents. Here 200 mA was selected based on the application.

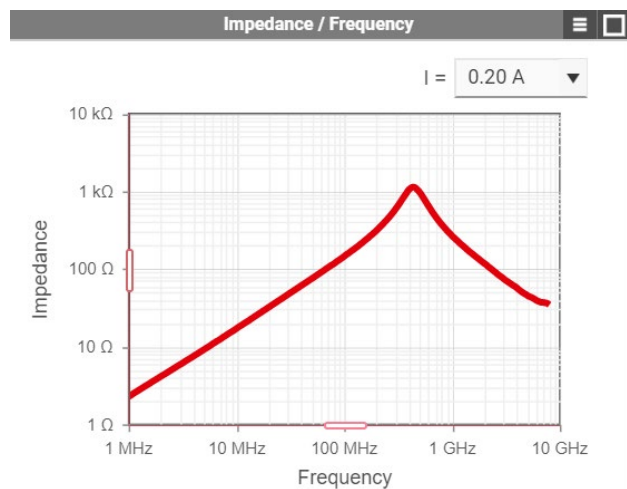


Figure 10: Impedance curve of WE-TMSB 7426924 1152

The capacitors for the Pi filter are selected so that the attenuation range is as large and steep as possible and all currents and voltages with frequency components are well conducted to ground. For reasons of size, MLCCs are used for the data lines. The article WE-CSGP [885 012 105 006](#) with a capacitance of 1 μ F is selected.

The capacitors selected are made of X5R ceramic, which enables a high capacitance. However, due to its internal structure, the material is also very voltage-dependent. An

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applied voltage leads to a drop in capacity, this effect is called DC bias. How exactly this effect affects the selected capacitors can be seen in REDEXPERT. The following Figure 11 shows the voltage dependence of the article WE-CSGP 885 012 105 006.

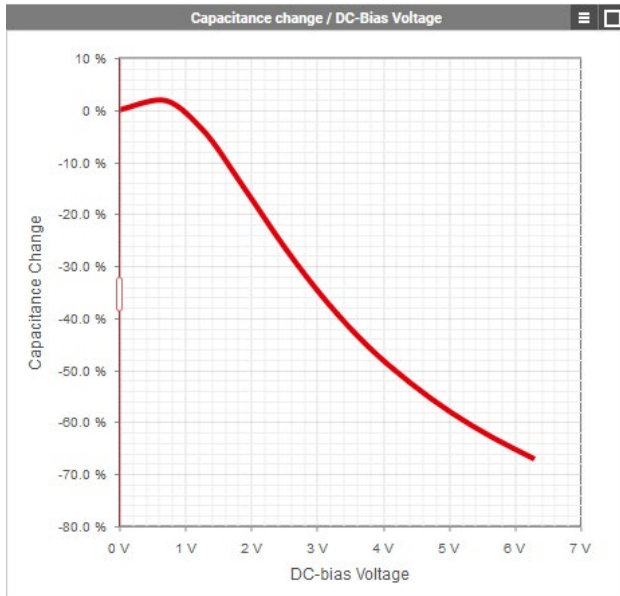


Figure 11: Capacitance change vs. DC-bias voltage

It is shown that the capacitors at 5 V affect the circuit with about 42% of their original capacity.

Because of the current dependence of the ferrite and the voltage dependence of the capacitors, it is important to test the circuit under the conditions of the application.

First the effect of the selected Pi filter is simulated in LTspice with the circuit shown in Figure 12.

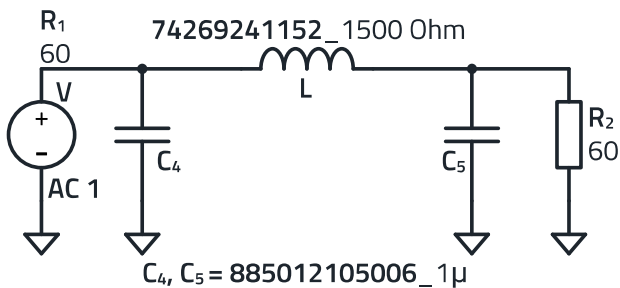


Figure 12: LTspice Layout of the Pi Filter.

The components of Würth Elektronik eiSos are available as models in LTspice, which allows simulation to be as accurate as possible. An ac voltage source with an amplitude of 1 V is used. Figure 13 shows the simulation result of this setup.

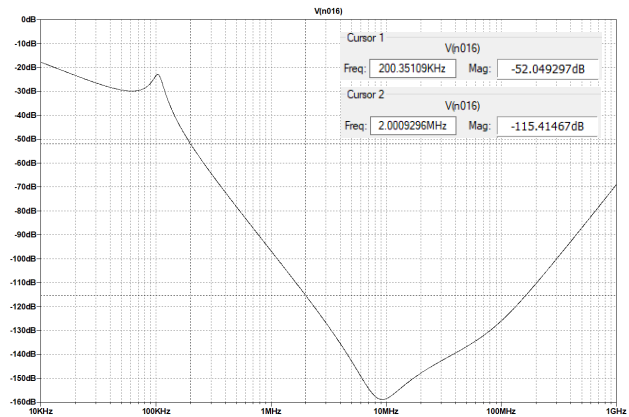


Figure 13: Simulation of the Pi filter

Due to the construction of the simulated circuit as voltage divider, there is again a basic attenuation of 6 dB. The markers show that, as expected, the attenuation per frequency decade is 60 dB. It can also be seen that the entire frequency range shows good attenuation. However, the high maximum attenuation value of approx. 158 dB is conspicuous. It is questionable whether such a high attenuation can be achieved with real components. Also the most network analysers reach their limit at 100 dB.

Now all required filter elements are selected. Since the simulations show good results, the circuit designs are built with the selected components. However, the simulations do not relate to all the factors present in circuits, such as material influences and line losses into account. Therefore, measurements are required to show whether the structure meets the requirements for high safety against interference signals and transients under real conditions.

03. PCB DESIGN

In order to prevent reflections, the traces on the circuit board of the filter stick, called microstrips, should have the same impedance as the application, in this case 120 Ω in total. Since this is a differential data line, the impedances are summed during symmetrical transmission. Therefore, the lines must be designed for an impedance of 60 Ω each. In order to achieve a certain line impedance, the following parameters shown in Figure 14 must be matched to each other. Figure 14 shows the basic structure of a printed circuit board.

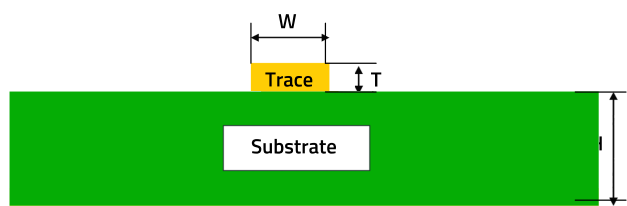


Figure 14: Layout of a printed circuit board

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By varying the parameters shown in Figure 14, it is possible to adjust the impedance of the PCB. Parameter W represents the width of the trace, parameter T the height of the trace and parameter H the thickness of the substrate material between the trace and ground plane, which is mostly FR4. FR4 is a flame retardant, non-conductive composite material made of epoxy resin and glass fiber fabric and is the most used material for printed circuit board production as a result of its good adhesion, water resistance and tracking resistance.

With the help of a microstrip calculator, the impedance of a printed circuit board can be calculated by entering the parameters just described. The height of the end copper is given as $35\ \mu\text{m}$ as standard and at the lowest cost. The width of the traces can be freely selected. The wider the trace, the lower the impedance. Since the small size of the components and connectors restricts the width of the tracks and an impedance of $60\ \Omega$ is to be achieved, the parameter H , i.e. the distance to the ground plane, must be adjusted. In order to allow a small distance, a PCB with four layers is used. Here it is possible to use the second layer as ground potential and thus to keep the distance to the surface very small. The following Figure 15 shows a standard PCB structure with four layers and a copper height of $35\ \mu\text{m}$.

Note: The $18\ \mu\text{m}$ copper in the chart will be plated up to $35\ \mu\text{m}$ in the finished board.

Figure 15 shows that the distance between the first and second layers is $0.288\ \text{mm}$, and by using the distance of $0.288\ \text{mm}$, the height of the end copper of $35\ \mu\text{m}$, and the dielectric constant of the FR-4 material of 4, it is possible to adjust the width of the trace to achieve an impedance of $60\ \Omega$. The following parameters are selected to achieve an impedance of about $60\ \Omega$.

Material Text	Mat.-Nr.	μm	Stackup
A-RS Copper foil-018my 330x490mm	50200238	18	VS
A-RS-FR4-Prepreg-2116-TG135	50200534	288	
A-RS-FR4-Prepreg-7628-TG135	50200465	0	
		35	L2
A-RS-FR4-ML-0.71mm-035+035-TG135	50200375	710	
		35	L3
A-RS-FR4-Prepreg-7628-TG135	50200465	288	
A-RS-FR4-Prepreg-2116-TG135	50200534	0	
A-RS Copper foil-018my 330x490mm	50200238	18	RS

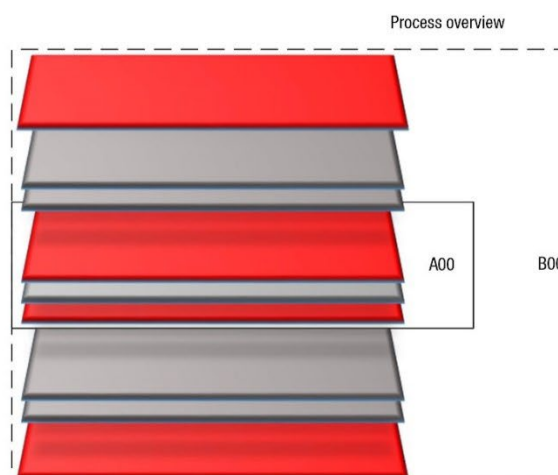
Figure 15: Layout of a PCB with four layers

Parameter	Symbol	Value
Trace Thickness	T	$35\ \mu\text{m}$
Substrate Height	H	$0.288\ \text{mm}$
Trace Width	W	$0.4\ \text{mm}$
Substrate Dielectric	E	4

Table 2: PCB parameters

In general it is important to keep the filter stick as compact as possible. The components are all placed on the top side of the board. Only the connectors have to be soldered on the underside due to their THT construction. In order to avoid reflections, care must be taken that the tracks are not at right angles. Rounded paths and 45° angles ensure a better signal flow. In addition, it is also important to place the components directly on the tracks to keep the paths short.

Figure 16 shows the complete board design. In the layout of the data lines, the ESD suppressors are placed near the input connector to divert ESD pulses as quickly as possible. All other components follow at short intervals. However, the components should not be placed directly next to each other, otherwise undesired capacitive coupling could occur. Both data lines should have the same length due to the symmetrical signal transmission. Plated, through-hole vias are used for connection to ground. They are placed next to the pads and form a conductive connection to the underside of the board, which represents the ground potential. In the layout of the supply voltage line, the two pin 6s are connected with a straight line. In the same principle as explained above, the components are placed directly on the line. Due to the available space, several vias are attached to the capacitors in order to make the connection to the ground potential as low-impedance as possible.



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Both pin 5s and the housing surface are connected to ground. The black edges represent the space required by the protruding D-SUB connector.

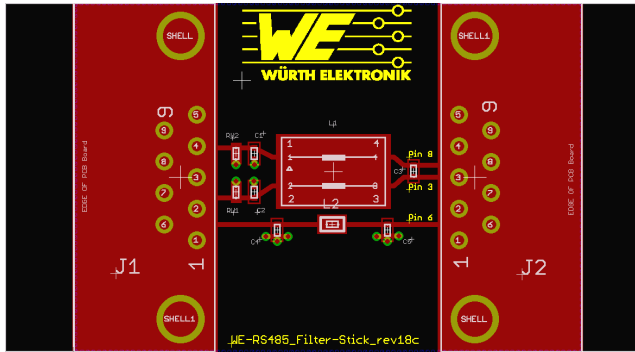


Figure 16: Complete filter stick design.

04. MEASUREMENT OF THE S-PARAMETERS

First, the transmission characteristics of the data lines A and B are measured for differential and common mode transmission. The aim of the measurement is to prove that the filter stick allows unattenuated transmission of all signals in the frequency range up to 6 MHz according to RS-485 standards during differential signal transmission and filters out unwanted signals with higher frequencies. Common mode signals should be attenuated over the entire frequency range without exceptions. Based on the calculations and the simulation, the signal up to 6 MHz should be able to pass almost undamped. The attenuation should then begin and reach an attenuation of 3 dB at 15 MHz. Figure 17 shows the measurement result of the mixed-mode S parameter S_{DD21} .

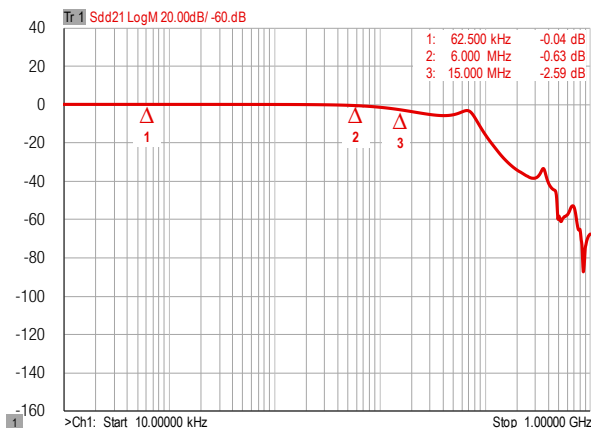


Figure 17: Transmission behavior of data lines with push-pull signals

Marker point 2 at 6 MHz shows an attenuation value of 0.63 dB, indicating that at the highest possible transmission frequency, approx. 93% of the signal is transmitted undamped. Typically, the attenuation for successful transmission should be lower than the cutoff frequency,

which is generally defined as 3 dB. Marker point 3 at 15 MHz shows an attenuation value of 2.59 dB, which corresponds to a transmission ratio of 74.2%. As the frequency increases, the attenuation also increases continuously, with the exception of some resonances, up to a value over 80 dB.

In addition to investigating the attenuation behavior during push-pull transmission, the behavior towards common mode signals must also be investigated. For this purpose, the mixed-mode S-parameter S_{CC21} , shown in Figure 18, is investigated.

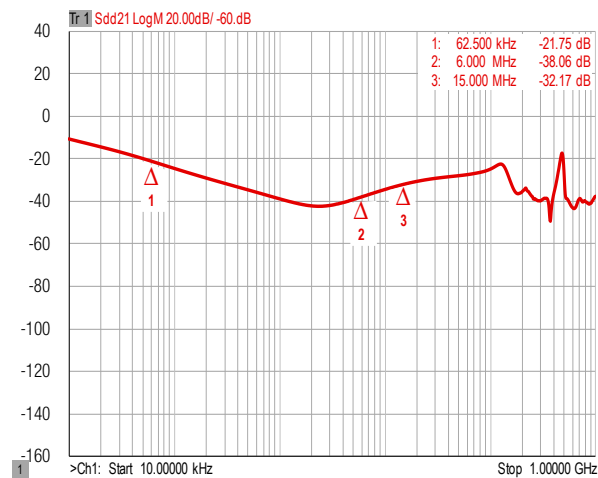


Figure 18: Transmission behavior of data lines with common mode signals

It can be seen that the signal is attenuated from the beginning of the frequency range represented. According to marker point 1, the attenuation at the calculated cut-off frequency $f_{\lambda/4}$ is approx. 21.8 dB. From 50 kHz the attenuation is always over 20 dB, which corresponds to a transmission ratio of less than 10%.

In the next step, the transmission properties of the supply voltage line are presented. To measure these, a two port measurement is necessary. The S-parameter S_{21} describes the signal transmission of the filter. Since a Pi filter (a third order low-pass) was used here, it is to be expected that a high attenuation is present in the entire frequency range. Figure 19 shows the measurement result of the supply voltage line.

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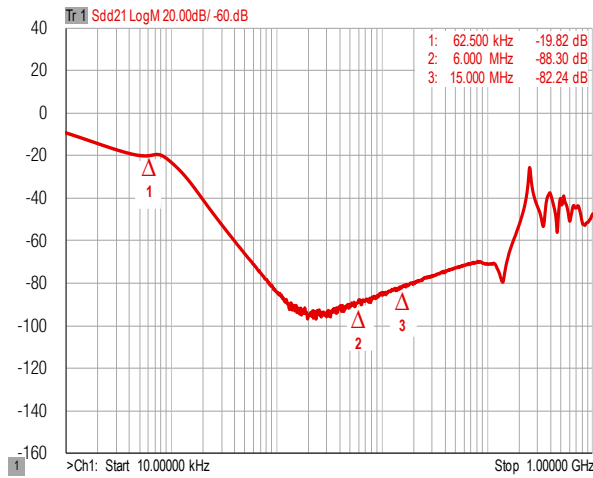


Figure 19: Transmission behavior of the supply voltage cable

As can be seen in Figure 19, the attenuation at the beginning of the frequency range is approx. 10 dB. At marker point 1, which is 62.5 kHz, the attenuation is already 19.82 dB. The attenuation reaches a maximum value at near 2 MHz with a value of about 95 dB.

05. EVALUATION AND CONCLUSION

First, the behavior of the differential mode transmission is analysed. Figure 20 shows the simulated and the measured mixed-mode S-parameter S_{DD21} of the data lines A and B. The red line is the simulated and the black line the measured graph. The horizontal axis represents the frequency in Hz, while the vertical axis indicates the attenuation in dB.

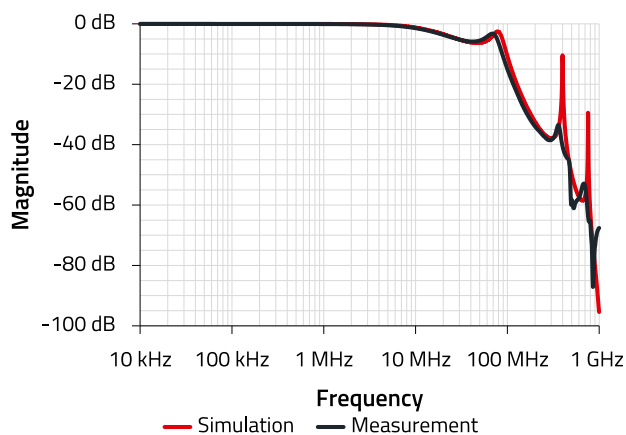


Figure 20: Comparison of S_{DD21} of data lines A and B

Before insertion in Figure 20, the 6 dB basic attenuation due to construction as a voltage divider in LTspice was taken out in order to obtain a better comparison between the simulated and the measured graph. It can be seen that the attenuation of both graphs begin at about the same moment. The goal of not attenuating signals up to 6 MHz was successfully

achieved. Thus, all signals that comply with the RS-485 standard can be transmitted without interference. Overall, it can be seen that the simulated course is almost identical to the measured course. The only recognizable differences are the different resonances and the minimal deviations of the attenuation values. In general, the quality Q of the components determines the height of the resonances. The higher the Q-factor, the greater the amplitudes of the resonances, due to the lower losses caused by the reactance. The resonances of the measured graph are significantly smaller, since parasitic effects are present which are not considered by the simulation and which have a negative influence on the quality of the system. The small deviations of the damping values can be explained by component tolerances.

Since the two graphs are almost identical, the real structure of the filter circuit achieves the desired property of allowing signals relevant for data transmission of the RS-485 standard to pass undamped. Signals with higher frequencies are attenuated to prevent interference in data transmission.

Next, the simulated and measured behavior of common mode signals is compared using the same principle. Figure 21 shows the simulated and measured curve of the mixed-mode S-parameter S_{CC11} of the data lines A and B. The color division is the same as in Figure 20.

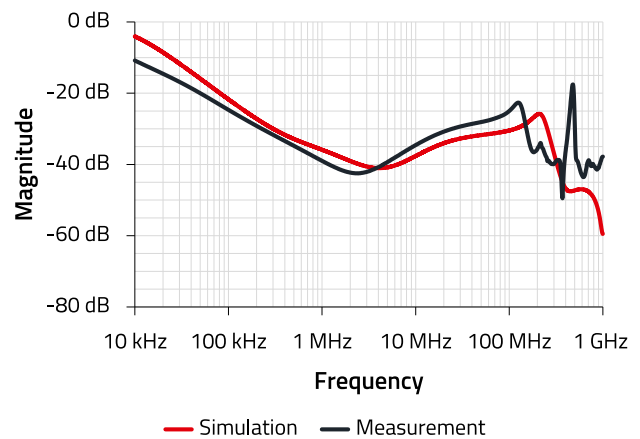


Figure 21: Comparison of S_{CC21} of data line A and B

Here it can be seen that the curves of both graphs are also very similar up to approx. 300 MHz. The resonance points are located at nearly the same places, but are differently pronounced. As described earlier, this can be explained by influences on the quality of the system. Furthermore, the LTspice models used are only simplified replicas of the real components and may show deviations from the real behavior. The deviations of the damping values and resonances in the action range of the common mode choke can be explained by

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inductance tolerances of the component. In the frequency range above 300 MHz, increased resonances occur due to coupling of the parasitic capacitances of the circuit board and the components.

Overall, the measurement confirms that the circuit offers sufficiently high attenuation over the entire relevant frequency range compared to common mode signals. The calculated frequency $f_{\lambda/4} = 62.5$ kHz also achieves an attenuation of 21.8 dB. However, the fact that this is below the expected value of 23.8 dB can be explained by the tolerances of the inductance value of the common-mode choke. Already from a frequency of 50 kHz, only attenuation values over 20 dB are achieved.

The comparison shows that the real structure of the filter circuit comes very close to that of the simulation and exhibits extremely satisfactory attenuation compared to common-mode interference. The circuit shows the desired result for both common mode and differential signals and is thus verified for use in filtering the data lines of the RS-485 standard.

The simulation and measurement results of the supply voltage line are also compared. Figure 22 shows both graphs of the transmission S_{21} .

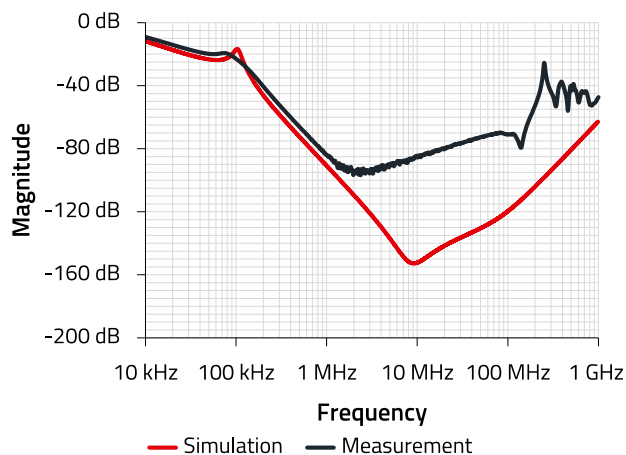


Figure 22: Comparison of S_{21} of the supply voltage line

Here, the 6 dB basic attenuation of the simulation model was also taken out to provide a better comparison.

It can be seen that both graphs have an almost identical curve at the beginning. Only a few dB difference in the attenuation values separate the two graphs. A clear difference can be seen at a frequency of 2 MHz. The simulation graph decreases to a value near 150 dB, while the measured graph reaches a maximum attenuation value of 95 dB. Attenuation values of 95 to 150 dB are very high, i.e. the very small voltages measured by the network analyzer are in the range

of the analyzer's inherent noise; the measuring instrument reaches its technical limits in this range. The high filter attenuation of more than 85 dB in the frequency range above approx. 1 MHz means, on the one hand, high decoupling between the filter input and the filter output. On the other hand, however, even the slightest parasitic capacitive coupling of conductor tracks, component connections (front sides of the connection pads) and connector connections is noticeable, which leads to "overcoupling" of the filter and to resonances.

Despite the deviations from the simulation result, the measurement shows a good filter behavior because there is a sufficiently high attenuation over the entire frequency range. This ensures that all AC voltages are filtered out of the supply voltage and that only one DC voltage is transmitted.

As described above, the applied DC voltage reduces the capacity of the capacitors. The current flowing through the filter reduces the inductance and shifts the resonant frequency of the choke. This effect can be measured. The following Figure 23 shows the comparison between the measurement with and without applied DC voltage (DC bias).

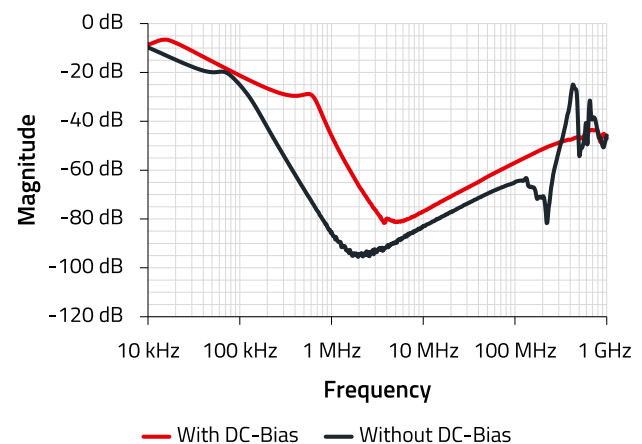


Figure 23: Comparison of measurements with and without DC bias

The black curve shows the measurement without DC bias and the red curve shows the measurement with a DC bias of 5 V and 200 mA. It can be seen, that the first resonance shifts to a higher frequency. This is because the resonant frequency of the SMD ferrite increases with increasing current and the inductance decreases. The reduced capacity of the two capacitors due to the applied voltage of 5 V leads to a slightly lower filter attenuation, which is still very high despite the DC bias influence.

The measurement thus shows that even under practical conditions with DC bias effects, a satisfactory attenuation result can be expected over the measured frequency range.

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The goal of achieving high attenuation values over a wide frequency spectrum has thus been achieved.

Since the measurements of the supply voltage line have also shown satisfactory results, it is confirmed that the designed filter circuit reliably attenuates undesired signals, interference and ESD influences without affecting the RS-485 transmission standards.

Thus all initial targets have been successfully achieved. In order to optimize the EMC behavior of an application, it is possible to check whether the circuit leads to the desired results by simply plugging it in. If this is the case, the complete design can be implemented in the application.

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A Appendix

A.1 Circuit diagram and final product

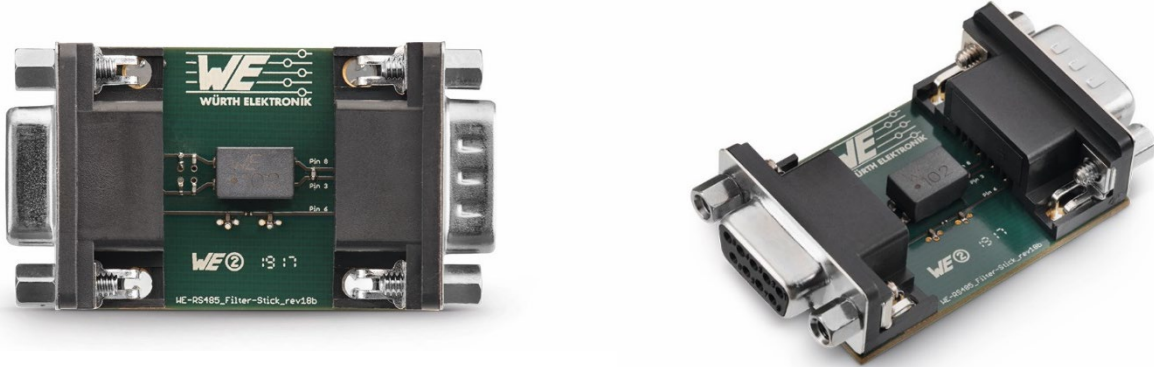
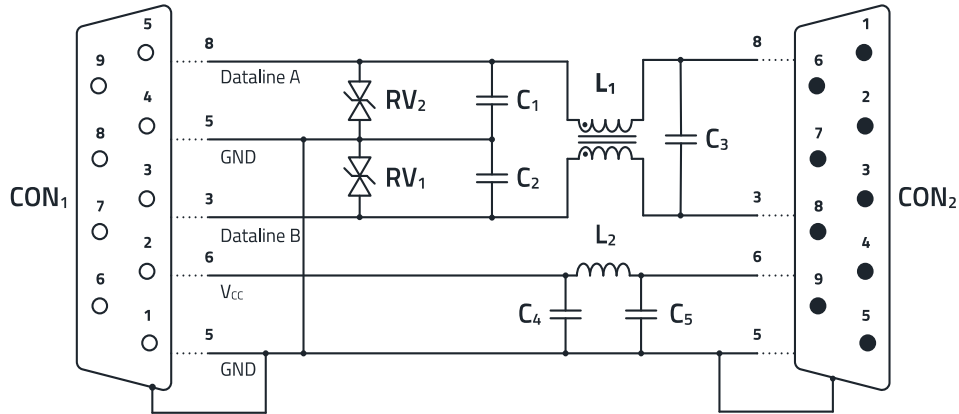


Figure 24: Complete circuit diagram and photos of the filter stick

A.2 Bill of Materials

Index	Properties	Series	Datasheet	Amount
L ₁	Common Mode Line Filter $Z_{MAX} = 6000 \Omega$; $V_{R(AC)} = 50 \text{ V}$	WE-SL2	744222	1
RV ₁ ; RV ₂	ESD Suppressor $V_{DC} = 5 \text{ V}$; $I_{LEAK} = 1 \mu\text{A}$; $V_{CLAMP,typ} = 55 \text{ V}$	WE-VE	823 570 505 60	2
C ₁ ; C ₂ ; C ₃	Multilayer Ceramic Chip Capacitor $C = 100 \text{ pF}$; $V_{R(DC)} = 10 \text{ V}$; NPO	WCAP-CSGP	885 012 005 013	3
CON ₁	D-SUB Female PCB Connector 8.08 mm	WR-DSUB	618 009 231 121	1
CON ₂	D-SUB Male PCB Connector 8.08 mm	WR-DSUB	618 009 231 221	1
C ₄ ; C ₅	Multilayer Ceramic Chip Capacitor $C = 1 \mu\text{F}$; $V_{R(DC)} = 6.3 \text{ V}$; X5R	WCAP-CSGP	885 012 105 006	2
L ₂	SMD-Ferrit $Z @ 100 \text{ MHz} = 1500 \Omega$; $I_R = 500 \text{ mA}$	WE-TMSB	742 692 41152	1

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