

APPLICATION NOTE

The USB Interface from EMC Point of View



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1. Technologies and key figures

The USB [Universal Serial Bus] specification defines the mechanical and electrical characteristics, as well as the protocol layer of the interface. The cable and connector are precisely defined. USB defines two types of hardware, hubs and functions, as well as terminal devices. In theory, up to 127 devices can be linked together in a star bus topology in which the only limitation is the 7-bit address. Connections are possible between the hub and function or terminal device or between hub and hub, whereby direct connections between terminal devices are not possible.

USB is a differential, bidirectional, serial cable bus. The differential NRZI (Non-Return-to-Zero-Invert) signal is transmitted asynchronously between the ports. The maximum cable length is 4 meters, the cable contains four wires, two for the twisted data pair and two for the supply voltage of the terminal devices and ground.

The data rate is between 10 kB/s and 480 MB/s in one of the three possible modes.

- 10-100 kbps for slow data transmission (mouse, keyboard). The signal voltage is between 0 V and 0.3 V.
- 0.5 - 10 Mbps for medium data transmission rates. The signal voltage here is 0.3 V (low) up to 2.8 V (high).
- 25 - 480 Mbps for high data transmission rates, defined as USB 2.0 with a maximum possible rate of 480 Mbps. The signal voltage here is 0 V ±10 mV (low) up to 400 mV ±10% (high).

At high data transmission rates it is necessary to terminate each of the symmetrical conductor pairs to ground with a 45 Ω terminal resistor. Here the cable impedance must be 90 Ω +/- 15% (symmetrical / differential).

Originally, USB was intended to supersede the serial and parallel interfaces in IT, meanwhile USB has become established not only in the IT domain, but has become indispensable in many other fields of application, e.g.

- home audio, video – for digital photos and music
- automotive – for MP3 music
- mobile IT, such as hand scanners – uploading data to a PC
- industry controllers – software upgrade, data download and upload
- medical devices – software upgrade, data download and upload

USB is a network with a star-shaped topology. All other USB terminal devices branch out from the host controller. A USB terminal device represents the bus connection, whereas a USB hub can branch to another hub or to terminal devices. Every other USB hub can represent a branching point until the maximum number of addressable devices is attained.

This illustrates what a complex network structure can be built up with a USB and this also clearly shows that this structure has to be paid special attention with regard to EMC. It is now apparent that even USB devices as standalone devices, i.e. without hub, without further branches, can display EMC weaknesses and "only just" meet the demands placed on them, and in a more complex structure can no longer meet their requirements. This then manifests itself in write/read errors with drives, dropouts with cameras, writing delays with keyboards, etc. But more on that later.

2. Hardware and components

Receptacles and plugs can have different sizes with USB, depending on their use in cameras, video devices or IT. The USB hub and terminal device connector can also differ in their form. The pin assignment is always the same, as shown in Fig. 1 and Table 1.



Fig. 1: Pin assignment of the USB interface, type A receptacle and plug

| USB 2.0 pin assignment and cable assembly | | |
|---|-------------|--------|
| Pin | Signal name | Color |
| 1 | VBUS | red |
| 2 | D- | white |
| 3 | D+ | green |
| 4 | GND | black |
| Package | Shielding | Ground |

Table 1: Pin assignment and cable assembly for USB

The USB cable should be structured as shown in Fig. 2.

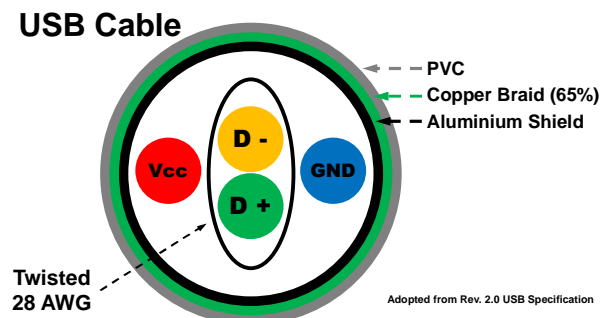


Fig. 2 USB cable layout

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The cable has four wires, which are precisely defined - the data wires are 28 AWG (American Wire Gauge) and the supply wires are 20 to 28 AWG. This defines the diameter and copper resistance, the HF conductor parameters result from the further structure. The two supply wires are untwisted, the data wires are twisted around one another, this results in the differential mode impedance of 45 Ω or 90 Ω (+/- 15%) against ground. The cable shielding should have a shielding braid with an area coverage of at least 65% and also an aluminum shield, i.e. double shielding is intended to guarantee high shield attenuation and consistent wave impedance for the cable. I can confirm from practice that there are many "black sheep" on the market, some of which only have an aluminum shield and even this consists of a foil that is only metalized on one side. Structured like this, the "shield" leaves a gap over the entire length of the cable and so the shield attenuation hardly attains values over 15 dB rather than the common >50 dB - but it is cheap!

The cable length must not exceed 5 meters. If longer lengths are needed, hubs have to be connected in-between.

Due to the high flexibility in the application and the high data transmission rate, special requirements arise for the circuit design and the interface construction - also depending on the application area.

Chip manufacturers know the problem of high data rates and the EMC requirements that still apply in terms of interference emission and immunity, and develop their USB controllers to be as good as possible in this regard. Nonetheless, not only the chip design, but also the complete circuitry concept has to be developed with a view to EMC. For this reason, the

- circuit concept
- layout
- filter concept
- construction (housing, connectors)

have to be coordinated. This certainly takes more effort in the development phase, but pays off in higher quality and also in lower production costs (!). Good engineering does not make products more expensive, but, given the same quality, makes them cheaper!

3. EMC criteria

So what does EMC have to do with the USB interface? Before taking a closer look at this, I would like to define an equation:

EMC = assured functionality

EMC is not "nice to have" to meet legal requirements for the declaration of conformity! EMC in our example of the USB means:

- **Low interference radiation:** A well matched symmetrical interface with optimized filters does not radiate. Through matching, the useful signal has the required quality factor

Q, so we also achieve the required signal-to-noise ratio and high interference immunity.

- **High interference immunity:** By symmetrizing the useful signal and using additional filters with overvoltage protection as well as interface jacks offering high levels of shielding attenuation with the relevant high design quality (not expensive) housing design, the interference immunity is considerably increased against transients and other inductively and capacitively coupled interference signals and therefore the functionality is ensured.

Before we examine the circuitry and design measures, here is a brief excursion into EMC basics. What is EMC? Electromagnetic Compatibility is the capability of an electrical system or device to work properly in its electromagnetic environment without being disturbed in its proper operation by neighboring systems or devices and without disturbing other systems or devices in their proper operation. This is a long and complicated sentence, but contains just what we previously described somewhat more technically with the question "What does EMC mean in case of the USB interface".

What EMC phenomena do we have to consider in the development of a product with USB and what are the most critical phenomena? These are:

- interference emission (interference field strength)
- interference immunity against electrostatic discharge (ESD)
- interference immunity against fast transients (burst)

As mentioned, there are now numerous application areas for USB. Every application area has other standard EMC requirements, but let us consider our equation:

EMC = assured functionality

Functionality must always be ensured and experience shows: If functionality works, then EMC also works, regardless of the application area. In the following we will examine USB circuit design step-by-step and present the design points to be considered.



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4. EMC circuitry concepts

The USB interface is a bidirectional, symmetric interface, as presented in Fig. 3.

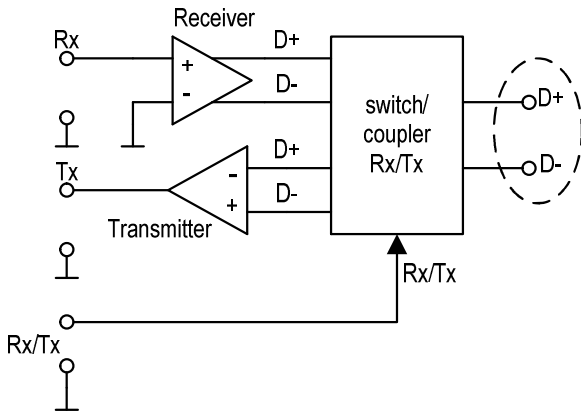


Fig. 3: The USB interface is symmetrical and bidirectional

Symmetrical transmission techniques have numerous advantages in terms of signal integrity, which are apparent in lower interference emission and higher interference immunity. Fig. 4 provides a more detailed explanation.

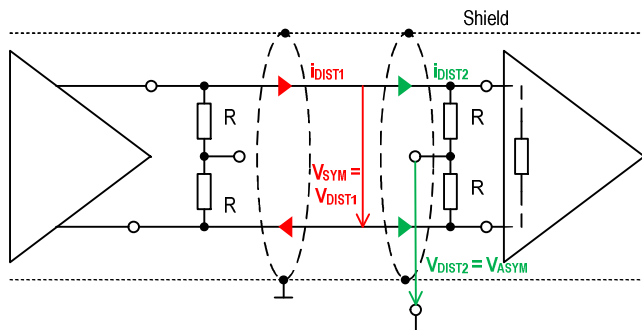


Fig. 4: The symmetrical interface with its measurable interference voltages

The following are measurable:

- a) \underline{U}_{sym} : interference voltage between the signal wires
- b) \underline{U}_{Asym} : interference voltage between the voltage midpoint and the reference voltage (ground) and the cable shielding.

This means that the USB transmission path can be affected by both differential mode, as well as common mode interference voltages. This can be both interference voltages from the interface itself, in this case described as interference radiation or interference emission or an electromagnetic effect from the outside in the form of inductive, capacitive or wave coupling - in this case described as interference coupling, which assumes a certain interference immunity of the interface in order to maintain continued function.

4.1. Interference emission

In the case of USB transmission, differential mode interference is mainly generated by non-linear signal harmonics due to mismatching and inadequate circuit design. Given asymmetry of the transmission path, i.e. transmitter, circuit board and conductor tracks, possibly filters, cables through to the receiver, this interference can lead to interference radiation and impairment of signal quality.

Common mode interference arises from parasitic coupling in the circuit environment of the USB controller, which can usually be found from capacitive coupling on the USB signal with rising interference frequency and increasingly in amplitude. However, these interference types are found on both USB wires in phase and at the same amplitude and therefore do not impair the useful signal. Asymmetries in the cable or at the receiver often convert the originally common mode into a differential mode interference signal, however, which can then contribute to signal impairment. High quality circuit design is called for here too. Fig. 5 illustrates the case.

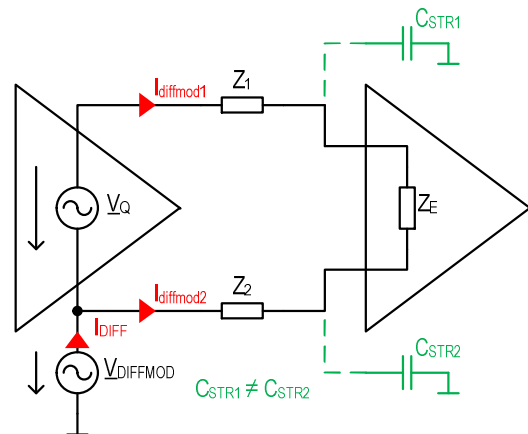


Fig. 5: Conversion of differential mode to common mode interference due to parasitic coupling capacities.

4.2. Interference immunity

Differential mode data transmission offers a significant advantage over the simple coaxial cable when it comes to the effect of interference on the USB. Fig. 6 presents the effect of interference on a coaxial cable. Depending on the shielding effectiveness of the coaxial cable, a burst (electric field), for example radiated from a mains cable in parallel with the USB cable, couples into the data line and interferes with the data signal. This leads to data or communication errors, which depend on the interference signal length and amplitude.

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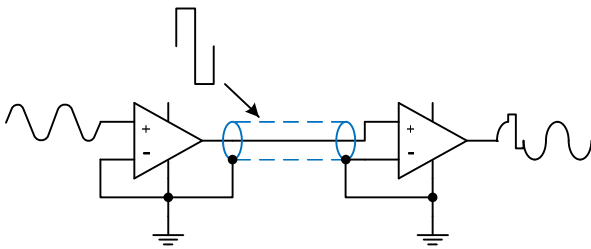


Fig. 6: Effect of interference on a coaxial data transmission path

Fig. 7 represents the case of differential mode data transmission, in this case with only a twisted pair of wires. The polarity of the useful signal is shifted from one wire to the other by 180°, the signal difference is evaluated at the input of the receiver. But the interference signal affects both wires in the same phase, so this cannot have an effect as an interference signal at the receiver.

Furthermore, in the case of the inductive interference effect (magnetic field), the twisting of the wires achieves compensation of the interference effect. As a result of the symmetrization of the partial inductances of the respective twisted wire, the interference influences compensate each other.

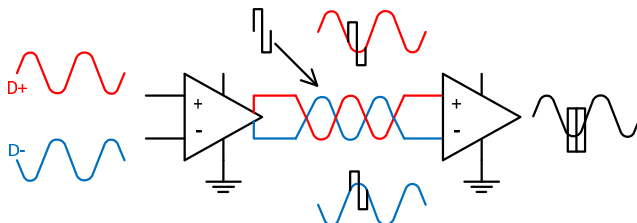


Fig. 7: Compensation of electrical interference coupling of the differential mode signal input and twisted wire pairs

4.3. Possibilities of reducing emission and increasing interference immunity

It is apparent in practice that interference emissions cannot be prevented and also interference immunity also has its - sometimes stringent requirements. The reason lies in many details, of which these are the most important:

- The inputs/outputs of the USB controller are insufficiently symmetrical, the USB signal displays common mode interference.
- The layout is not HF/EMC compatible, parasitic capacitances and the lack of wave impedance matching generates common mode interference.
- The circuit design (USB filter) is inadequate, the filters affect the signal quality and/or the insertion loss is too low.

- The interface design (receptacle, housing) is inadequate, poor ground reduces the shield attenuation of the cable, filters have poor ground reference.
- The USB cable is asymmetrical, poorly shielded, has inadequate ground connection. The cable deteriorates the signal quality, radiates signal harmonics and has insufficient shield attenuation towards external interference sources.

Some points cannot be influenced, these include the technical realization of the USB controller and the use of "cheap" USB cable. This demonstrates that preventive measures have to be met. Measures to

- protect the interface from the effects of external interference, which can lead to the destruction of the USB controller.
- limit interference radiation of signals via the cable.

5. Realization of the USB filter

5.1. Circuit technology

Both points can be fulfilled using additional filters and the USB interfaces. Fig. 8 shows the basic circuit of a symmetrical USB signal filter.

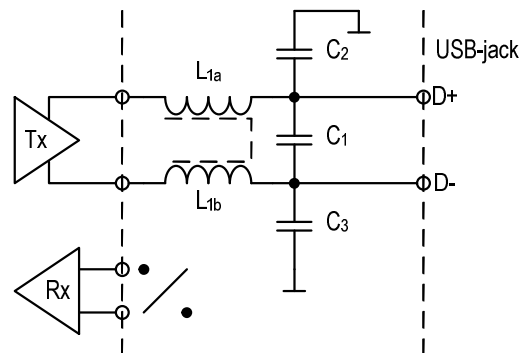


Fig. 8: Basic circuit of a symmetrical signal filter

Capacitances of up to approx. 3 pF between the data line and ground are tolerable with USB 2.0, beyond this the signal is impaired too much so that non-linear distortions occur that cause phase shift and attenuation in the harmonic component of the useful signal. The capacitors C2 and C3, together with the current-compensated choke, reduce the symmetrical interference components. The capacitances C2/2 and C3/2 affect the signal. It goes without saying that - C2 = C3. C1 reduces the symmetrical interference components and thus also affects the useful signal, its capacitance should be less than 4 pF. The values depend strongly on the properties of the current-compensated choke. The choke must have a high degree of symmetry and low stray capacitance between L1a and L1b. Furthermore, the real component of the ferrite permeability - that is the inductive component (!) - must be low and within the useful frequency range. In contrast, the

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resistive component of the permeability - that is the complex component (!) - must be high and within the frequency range to be filtered. Fig. 9 illustrates the relationships. The ferrite material has its transition range at around 200 MHz.

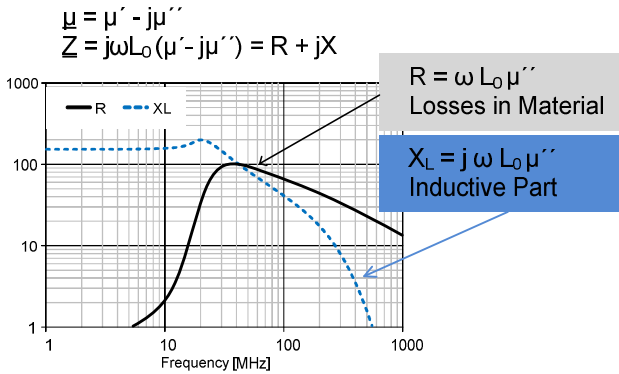


Fig. 9: Example for the curves for the complex and real permeability components of a HF ferrite material

Transient interference signals, such as ESD and bursts, can generally be limited with varistors. Especially SMD multilayer varistors which are particularly fast and withstand a high level of energy. What they all have in common is their high capacity, which is why they are not suitable for limiting transients at the USB. Transient limitation with diodes is shown in Fig. 10. Transients are limited against ground, both on D+ as well as on D- up to the forward voltage VF of the diodes. This voltage is around 0.7 V for silicon diodes. A problem appears very quickly here, which is why the diode pair on the right has two red flashes: The signal voltage of the "mid-speed" signal is up to 2.8V (D+ to D-), i.e. 1.4 V to ground. The positive branch must therefore be provided with an "offset" in order to avoid impairing higher signal voltages.

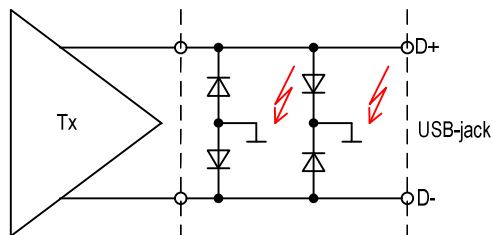


Fig. 10: Diode limiter to reduce coupled transients (burst, ESD) on the USB interface

Fig. 11. shows the solution. An additional TVS diode with a limitation voltage of 6 V sets the threshold value to approx. 6.7 V. That is sufficient for protection; TVS diodes with lower limitation voltages are too slow to limit ESD. The voltage levels are illustrated in Fig. 12.

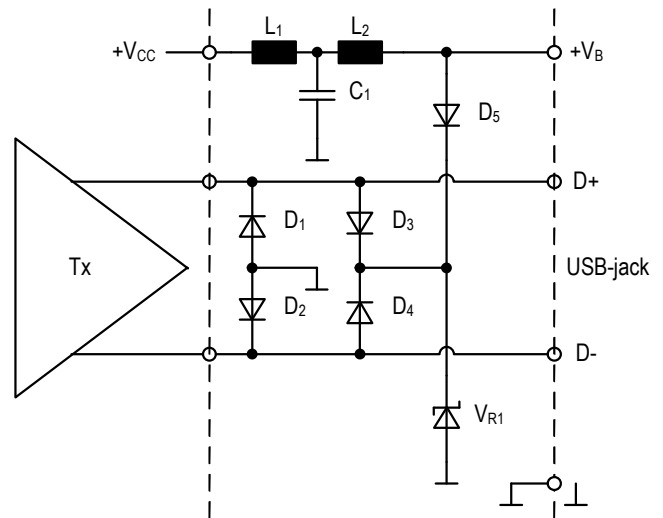


Fig. 11: Diode limiter to reduce coupled transients (burst, ESD) on the USB interface with "offset" for higher signal levels

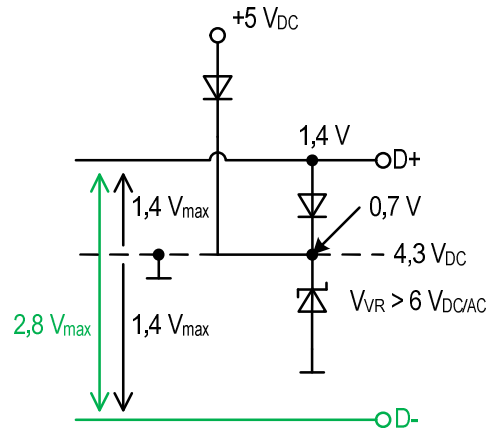


Fig. 12: Voltage level of the positive diode path

Transient limitation at the connection of the supply voltage can be achieved at the same time using the additional diode D5 in Fig. 10. Although the capacitance of the TVS diode is low at 5 pF, it would be too high for USB. As VR1 is in series with D3 and D4, however, the capacitance of VR1 reduces the overall capacitance that affects the signal here - so it is uncritical, as D3 and D4 have capacitances of approx. 2 pF. As in Fig. 8, the capacitors are in series with D3 and D4 with reference to the signal, there is an overall signal-to-signal capacitive load of 2 pF and signal against ground of around 3 pF.

In the supply voltage branch there is a T-filter with two SMD ferrites and a ceramic capacitor. The lossy component of the permeability should rise sharply at around 30 MHz, the inductive component is uncritical, as no signals are affected. The current carrying capacity is an important parameter, which is specified in the datasheets at 20°C. It should, of



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course, be selected to be adequate for the respective application.

5.2. Practical example

Fig. 13 shows the complete circuit diagram. The associated technical data of the components are specified as follows.

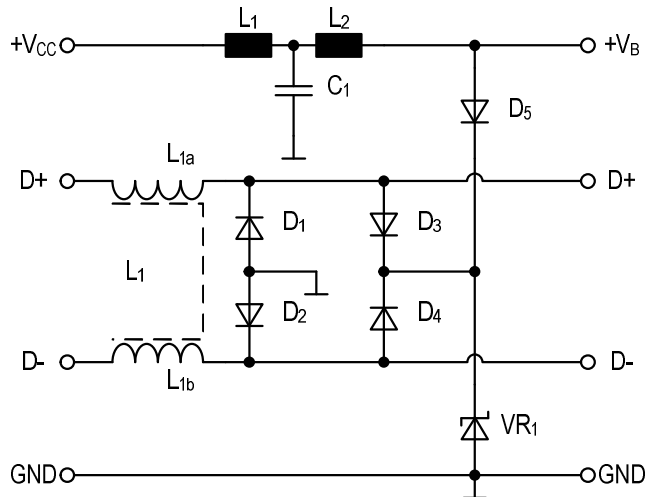


Fig. 13: Complete circuit diagram of the USB 2.0 filter

5.2.1. Filter for DC supply

The SMD ferrite already has an impedance of 300 Ω at 30 MHz, of which 200 Ω is resistive – i.e. the "ohmic" component. The ferrite has its maximum impedance in the range from approx. 80 MHz to 500 MHz in which the highest level of interference is to be anticipated in USB data transmission, above 200 MHz it is practically only lossy. Above 200 MHz the ferrite acts like an ohmic resistance without reactive components. Table 2 shows an overview of the most important parameters, the impedance curve is presented in Fig. 14.

| Properties | Test conditions | | Value | Unit | Tol. |
|---------------------|-----------------|----------|-------|------|-------|
| Impedance @ 100 MHz | 100 MHz | Z | 600 | Ω | ±25 % |
| Maximum impedance | 200 MHz | Z | 800 | Ω | typ. |
| Rated current | ΔT = 40 K | I_R | 1000 | mA | max. |
| DC resistance | | R_{DC} | 0.20 | Ω | max. |

Table 2: Electrical characteristics of SMD ferrite 742792651

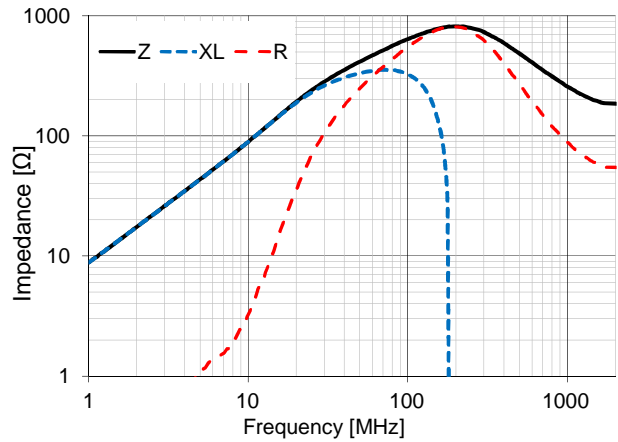


Fig. 14: Impedance curve of the SMD ferrite 742792651

The capacitor WCAP-CSGP X7R0603684K016DFCT10000 used here (Part. No 885012206051) has the following characteristics:

- Max. voltage 16 V
- Capacity: 680 nF
- Tolerance: 10%
- Ceramic: X7R

The capacitor should have its series resonant frequency above 500 MHz, which depends on the dielectric and the package. Small packages like 0603 or smaller with lossy dielectric such as X5R or Y5V are well suited. Lossy dielectrics exhibit less pronounced resonances, which is desirable for filters in the supply area. The resonance is a series resonance, which, as a result of the parasitic components above the resonance frequency of the filter, make the capacitor unfit for use, i.e. in advance: The ground connection of the capacitor also has to be low-inductance (layout!) in order to keep the total impedance as low as possible. Fig. 15 illustrates the relationship.

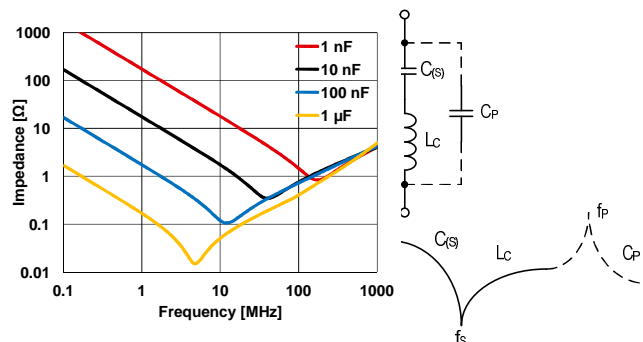


Fig. 15: The capacitor with its parasitic properties (simplified)

Depending on the package and dielectric, the capacitor has a series resonance that can already occur at a few MHz. Furthermore, the capacitor has a second resonance, whose frequency is significantly higher, however. Typical SMD 0805



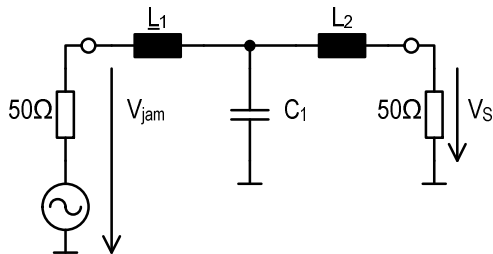
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package capacitors with X5R ceramic of 100 nF have their series resonance at approx. 500 MHz and their parallel resonance at 1.5 GHz.

The T-filter constructed this way for the supply voltage has a high insertion loss. The T-circuit was therefore chosen, because it has to be assumed that both the source, as well as the sink, in the power supply area are of low impedance. This gives rise to an optimal mismatch and therefore maximum suppression.

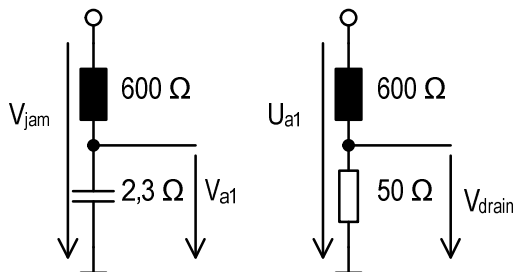
In Fig. 16 the theoretically possible insertion loss is calculated for the example of a 50 Ω system. There is a maximum attenuation of 70 dB at 100 MHz. This should be sufficient even for the toughest of situations!



assumption: source, drain = 50 Ω

$L_1, L_2: 600 \Omega @ 100 \text{ MHz}$

$$C_1: 680 \text{ nF} = \frac{1}{2\pi f * 680 * 10^{-12}} \Omega @ 100 \text{ MHz} \rightarrow 2,3 \Omega$$



$$a_1 = 20 * \log\left(\frac{2,3}{600 + 2,3}\right) = 48 \text{ dB}$$

$$a_2 = 20 * \log\left(\frac{50}{600 + 50}\right) = 22 \text{ dB}$$

$$a_{ges} = 48 \text{ dB} + 22 \text{ dB} = 70 \text{ dB}$$

Fig. 16: Calculation of the insertion loss of the T-filter in the supply voltage

5.2.2. Data line filter

The current-compensated choke 744232090 is the heart of the data line filter. On account of its winding technology and the few windings, the choke has a high degree of symmetry and low parasitic capacitances. A high insertion loss can be attained as a result of the high permeability of the ferrite material. The structure is shown in Fig. 17, the most important parameters are given in Table 3.

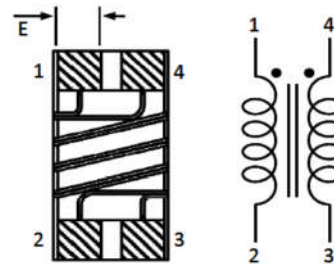


Fig. 17: Current-compensated choke 744232090 for the data line filter

| Properties | Test cond. | | Value | Unit | Tol. |
|---------------|---------------------------|----------|-------|------|------|
| Impedance | 100 MHz | Z | 90 | Ω | ±25% |
| Rated voltage | | U_R | 50 | v | max. |
| Rated current | $\Delta T = 40 \text{ K}$ | I_R | 370 | mA | max. |
| RDC | @ 20°C | R_{DC} | 0.30 | Ω | max. |

Table 3: Electrical characteristics of current-compensated choke 744232090

The impedance curve of the choke in common and differential mode is presented in Fig. 18. It is its common mode or asymmetrical suppression that takes effect if the same interference components are on D+ and D- with respect to ground. This is always the case for capacitive or inductive coupling on the circuit or its conductor tracks. So this impedance component must be as high as possible. At 100 MHz the choke has around 90 Ω. The differential mode impedance is the impedance compensated by the winding structure. "In one branch the current goes in - in the other out again", which is how current compensation should arise and the useful signal sees this impedance. This impedance must be as small as possible. All components of this impedance arise from asymmetries in the set-up and due to losses in the material from eddy currents and the skin effect. At 100 MHz this choke has a differential mode impedance of 6 Ω (both windings together).



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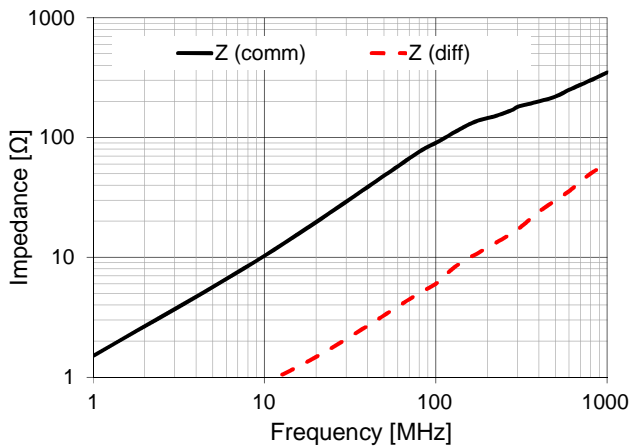


Fig. 18: Impedance curve of current-compensated choke 744232090

Now to the filter capacitors that form a low-pass 2nd order filter in the output of the filter. A diode array is used here instead of capacitors. The integrated diodes also have a capacitance, a parasitic capacitance, which we make use of here. In addition, the parasitic inductance of the TVS diodes in the array is very low. This has to be the case, as otherwise a short response time to the overvoltage transients cannot be attained. So we combine an almost ideal capacitor with effective transient protection. The most important electrical characteristics and the structure of the array are presented in Fig. 19.

| Properties | Test conditions | Value typ. | Value max. | Unit |
|------------|---|------------|------------|------|
| C_{IO} | $V_{Pin5}=5V, V_{Pin2}=0V, V_{IO}=2.5V, f=100MHz, I/O \text{ to GND}$ | 2.0 | 2.5 | pF |
| C_x | $V_{Pin5}=5V, V_{Pin2}=0V, V_{IO}=2.5V, f=100MHz, I/O \text{ to GND}$ | 0.4 | 0.6 | pF |

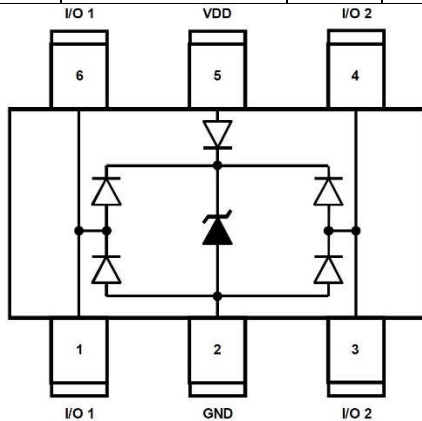
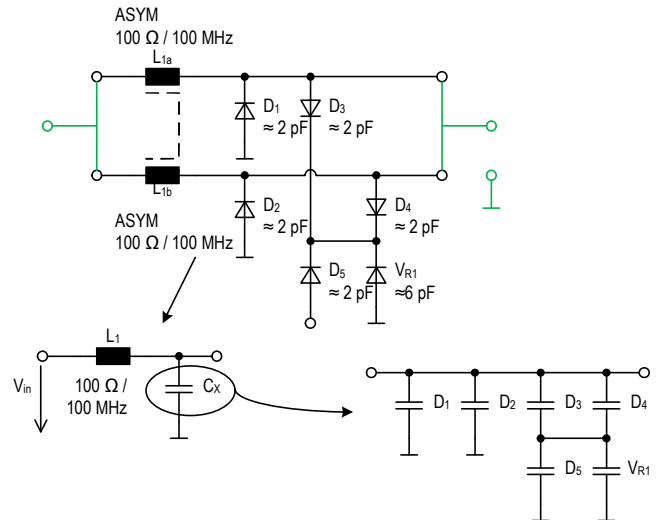


Fig. 19: Electrical characteristics and structure of the diode array WE-TVS 82400102

The interference signal attenuation can also be calculated for this filter; assuming that the interference occurs at both signal wires in the same amplitude and phase angle, the calculation in Fig. 20 applies.



$$C_x = 6,6 \text{ pF}$$

$$X_C = \frac{1}{j\omega C} = 240 \Omega @ 100 \text{ MHz}$$

$$a = 20 \cdot \log\left(\frac{100}{240 + 100}\right) = 10,6 \text{ dB}$$

Fig. 20: Calculation of the insertion loss of the USB data line filter

Here the attenuation is 10 dB at 100 MHz. Even this is sufficient, as the interference components can be assumed to be lower than on the power supply connection and the useful signal should not be affected. Every capacitance to ground acts as a signal load of half capacitance.

5.2.3 Layout

The circuit board with its conductor tracks is an arrangement of components with capacitances and inductances. The layout therefore has to be developed according to the circuit requirements. A simple LC low-pass filter can be significantly impaired in its effectiveness by an unfavorable layout. Fig. 21:



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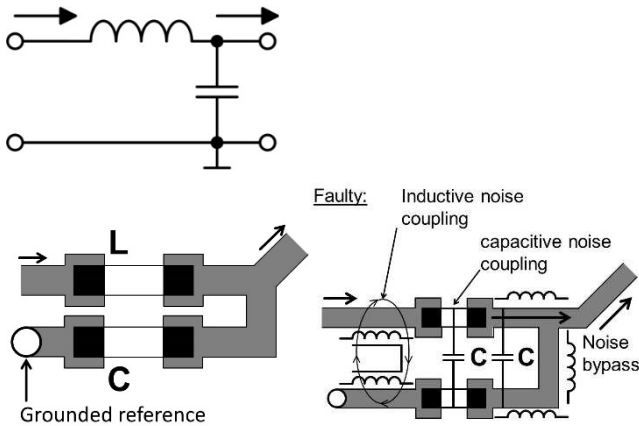


Fig. 21: Example of a low-pass filter for high frequencies with an unfavorable layout

What is wrong with the layout in Fig. 20?

- The ground connection to the capacitor is too long. 1 cm of track corresponds to 6-10 nH.
- The ground connection should pass directly to the housing, as the ground reference of the cable shielding and the ground reference of the filter must lie on the same HF potential.
- A stub line to the capacitor passes between the inductor and capacitor. This stub line is an additional inductance in series with the capacitor and, as a result of the higher reactance of the inductance with increasing frequency, renders the capacitor ineffective.
- The filter input and filter output couple inductively with each other. The filter is short-circuited with increasing frequencies.
- The components couple capacitively as they are located parallel to one other. Here too, the coupling is greater with increasing frequency.
- The corrected layout with the associated HF-compatible arrangement is shown in Fig. 22.

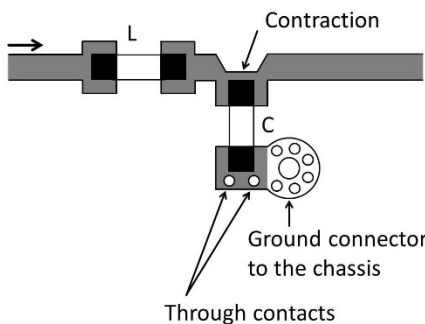


Fig. 22: HF-optimized layout of an LC filter

What is right with the layout in Fig. 22?

- The contraction prevents that interference current is bypassed at the capacitor. The capacitor "lies" in the signal path.

- The rectangular arrangement of the components prevents mutual coupling.
- The short ground connection at the capacitor, which is of low impedance as a result of two through-contacts, offers an ideally HF-passivated reference point for the capacitor.

5.3. The Würth Elektronik eiSos USB 2.0 EMC Application Board

All the points discussed so far have been considered in the USB Application Board.

The data lines are routed symmetrically, all ground connections have the shortest connection to the chassis and the circuit board also has a ground plane. The empty space, also around the components, has been filled with compound in order to reduce coupling between the tracks and between the components. All ground connections are provided with at least two through-contacts. The layout and both sides of the circuit board are presented in Fig. 23. Fig. 24 shows the resulting USB dongle; the circuit diagram corresponds to that in Fig. 13, the layout to that in Fig. 23. The optimal connection of the reference and chassis ground is clearly identifiable from the USB receptacles of the device (PC) are of low impedance, connected directly to the chassis and the USB cable is also shielded, as described previously.

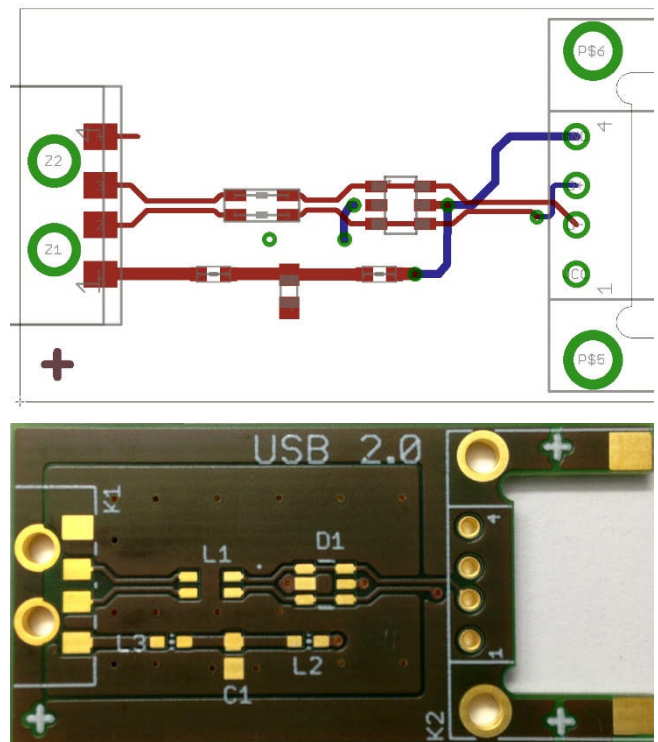


Fig. 23: Layout and component side of the EMC Application Board for USB



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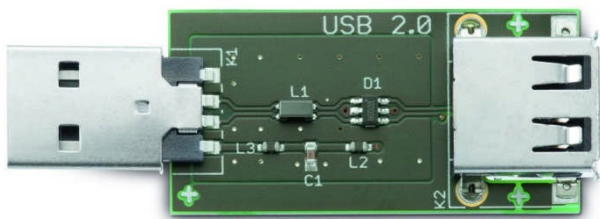


Fig. 24: USB Dongle, closed and opened, layout according to Fig. 23, circuit diagram according to Fig. 13

The following curves in Fig. 25 a-c show (from top to bottom) the insertion loss of the power supply filter, the common mode and differential mode impedance of the data line filter and the transient limitation of the data line filter.

VCC Line Noise Suppression

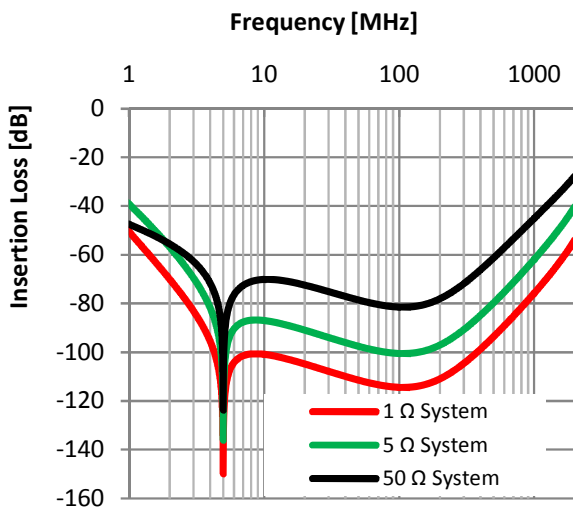


Fig. 25a: Insertion loss of the power supply filter

Data Line Impedance

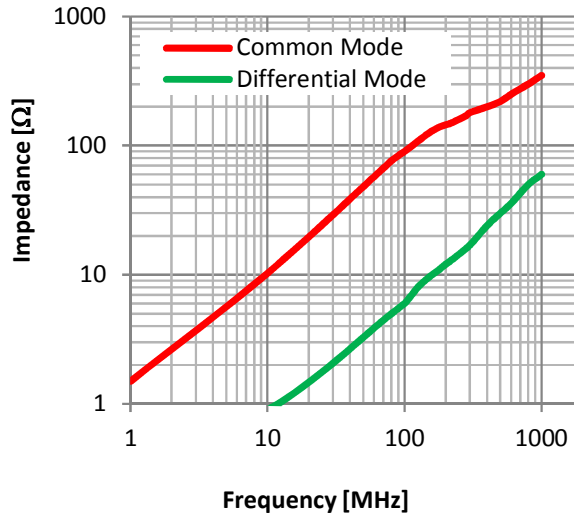


Fig. 25b: Impedance of the data line filter, common and differential mode

ESD Suppression

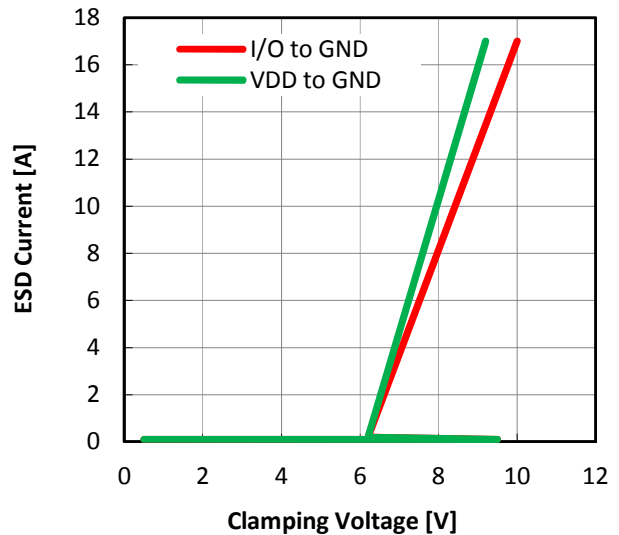


Fig. 25 c: Voltage limitation of the data line filter against transient interference, such as bursts and ESD

The filter is usually integrated on the controller board within the device. Würth developed the EMC Application Dongle in order to facilitate the engineer's circuit development and to be in a position to evaluate effectiveness. Despite an optimal layout and ground connection to the USB receptacles, the dongle requires an HF-compatible ground connection from the USB receptacles to the PC on the one hand, and to the cable on the other. The reason is that the Vcc filter capacitor (Fig. 13) and the overvoltage diodes have to dissipate their

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HF interference currents and possibly transient interference currents; this only works against ground or the chassis. Fig. 26 shows the set-up.

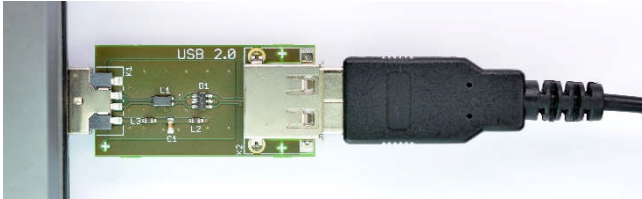


Fig. 26: Use of the EMC USB dongle

Used in this way, as a signal source for a PC and as a peripheral device, a USB hard drive emits an interference emission spectrum as in Fig. 27. The yellow curve shows the interference spectrum on D+ in front of the filter, the blue curve behind it. The interference is reduced by up to 35 dB. The magnitude of suppression is strongly dependent on the impedance of the interference source, which depends of the type of coupling, i.e. capacitive, inductive or radiated. The higher the impedance of the interference source, the more effectively the filter works. Interference sources that are on the ground system of the device cannot be reduced by a filter, of course, as there is no corresponding reference or grounding point.

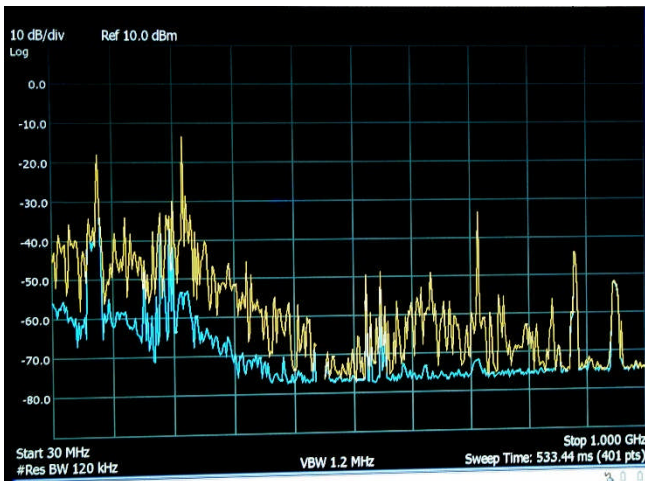


Fig. 27: Interference emission spectrum on D+ before and after the data line filter

Fig. 28 shows the interference spectrum before and after the power supply filter. A reduction in interference of around 20 dB is apparent here too.

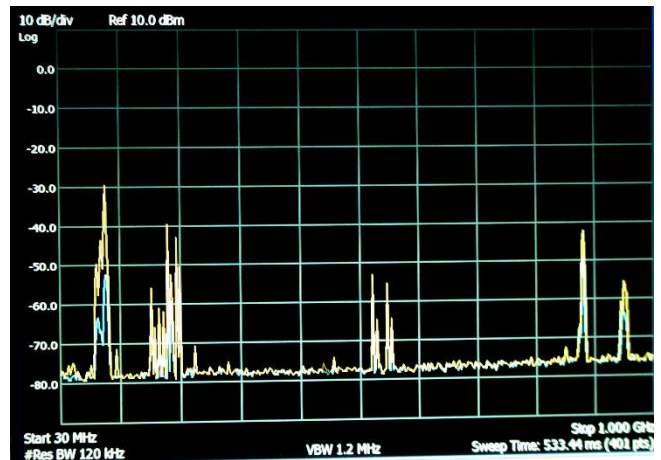


Fig. 28: Interference emission spectrum on the power supply line before and after the data line filter

5.4. The USB 2.0 EPLE jack with integrated filter

Filter design has its pitfalls, as shown from numerous practical examples. All these pitfalls are controllable, but framework conditions, such as space requirements, the mechanical concept and many others, often do not permit "good" filter design. Retrofitting a filter, e.g. following EMC approval measurements, also frequently turns out to be costly and time-consuming.

That is why Würth Elektronik offers a USB jack with integrated (!) USB filter.

The most important technical data:

- ESD and overvoltage protection to < 10 V for 15 kV discharge voltage
- Common mode data line attenuation to 90 Ω at 100 MHz of > 10 dB (dependent on the source and sink impedance)
- Attenuation at the voltage supply at 100 MHz: > 40 dB (dependent on the source and sink impedance), the filter attenuates reliably up to over 1 GHz

The filter is therefore outstandingly shielded and has an optimal ground reference. In addition, the extremely small package strongly reduces coupling between the components and conductor tracks in the useful frequency range up to 1 GHz. By simply replacing existing unfiltered receptacles with these makes the application extremely convenient and shows

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immediate

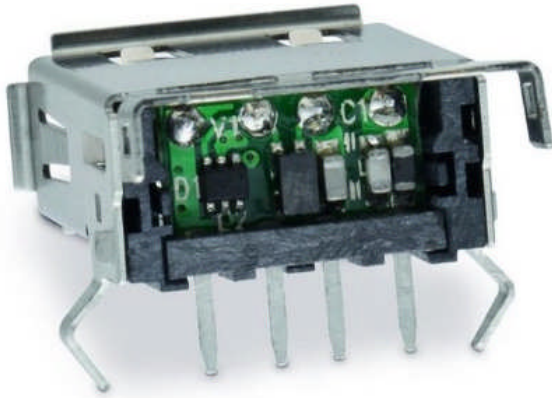


Fig. 29: USB receptacle with integrated EMC filter

effect.

balancing act between performance and time. Würth Elektronik would like to present you with the necessary components, as well as the necessary expertise to support you in optimally designing the USB interface. We hope to have done this with the products introduced and this brief technical article and wish you every success with your next design.

6. Summary

EMC without filters is no longer possible in today's circuit technology. Electronics in tight spaces, useful frequencies up into the GHz range and also consideration of the EMC standards necessitate their use. EMC is not "nice to have" or to satisfy the regulations and standards, but is a quality feature for which the user of the product has a right. Nevertheless, EMC is often an engineering challenge and a

7. Bill of Materials

| Description | Package | Electrical specification | Order code |
|-------------------------|----------|--|---------------------------------|
| WE-CBF EMI ferrite bead | EIA 0603 | $Z = 600 \Omega$; $I_R = 1A$; $R_{DC} = 0.2 \Omega$ | 742 792 651 |
| WE-CNSW CM choke | 1206 | $Z = 90 \Omega$; $I_R = 370 \text{ mA}$; $R_{DC} = 0.3 \Omega$ | 744 232 090 |
| WE-TVS High Speed | SOT23-6L | $V_{RWM} = 5 \text{ V}$; 4+1 channel; $C_{Ch} = 2 \text{ pF}$ | 824 001 02 |
| WCAP-CSGP | 0603 | X7R; $680 \text{ nF} \pm 10\%$; 16 V) | 885 0122 060 51 |
| EMC USB adapter | USB A-A | USB 2.0, $90 \Omega_{\text{Diff}}$; 1 A; ESD+EMI protected | 829 999 STICK |
| WE-USBH EPLE connector | USB A | USB 2.0, $90 \Omega_{\text{Diff}}$; 1 A; ESD+EMI protected | 849 21 21 |

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The technical specifications are stated in the current data sheet of the products. Therefore the customers shall use the data sheets and are cautioned to verify that data sheets are current. The current data sheets can be downloaded at www.we-online.com. Customers shall strictly observe any product-specific notes, cautions and warnings. WE reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services.

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USEFUL LINKS

Application Notes:

<http://www.we-online.com/app-notes>

REDEXPERT:

<http://www.we-online.com/component-selector>

Toolbox:

<http://www.we-online.com/toolbox>

Product Catalog:

<http://katalog.we-online.de/en/>

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