WHITE PAPER

Whisker Growth and Mitigation

WÜRTH ELEKTRONIK

WPP001, BY ALFONS HARPAINTNER

1. Introduction

Several customers ask about whisker formation in our products. Below are some facts about understanding and mitigation strategies of whiskers in Würth Elektronik eiSos Group.

2. Whisker – the hidden Challenge

Whisker formation on tin-surfaces is a well known phenomenon since the early 50-ies. Although it was not well understood because when whiskers occurred the parameters as well as the test instruments were not well documented or still insufficient, this problem seemed to be solved by the use of lead additions to tin-surfaces.

With new legislative actions in the European Community to avoid lead in electronic parts effective in 7/2006 (directive 2002/95/EC) the whisker problem came back. Suppliers of electronic materials (e.g. wires, lead frames) as well as the manufacturers of electronic parts had to face this challenge.

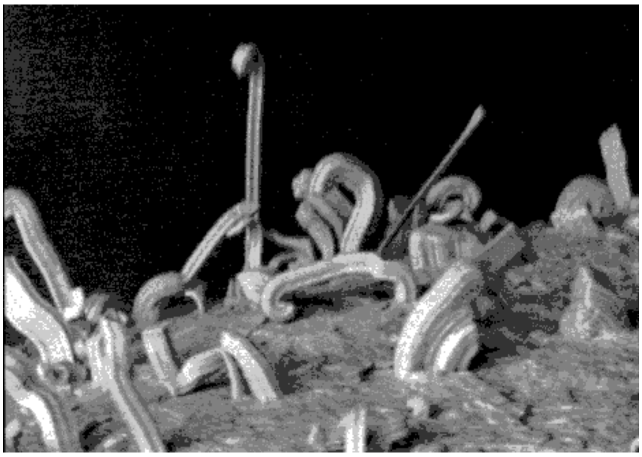

Figure 1: Whisker formation on Tin surface (reprinted with permission of NASA Electronic Parts & Packaging (NEPP) Program

2.1. Definition: What is a whisker?

It is a crystalline structure of material (hair like) with diameters of 1-10 µm (typically 1 µm) and a length of 10 µm to some mm.

Whiskers can be straight, kinked or even curved. Whiskers appear on tin surfaces and may reduce the isolation resistance and/or the distance to adjacent parts. Additional problems arise when the whiskers break and short the printed circuit board or some fine pitch components. One of the most critical failures is a metal vapor arc at high currents and voltage.

Whisker induced failures are reported in commercial satellites, medical devices, power plants and consumer products.

Whiskers grow at different environmental conditions (temperature / moisture / pressure). They grow from the base, not from the top that means they grow out of the substrate.

2.2. Appearance: Where is the risk high?

The risk of Whisker growth is high where a copper-surface is covered with pure tin. But it is not only restricted to this combination.

Theory of Whisker Growth

The fundamental research about whisker growth is still incomplete. The common and widely accepted understanding is that whisker growth is induced by compressive forces in the tin layers.

At the interface between copper and tin even at room temperature an intermetallic layer of Cu_6Sn_5 will form, which is shown in figure 2.

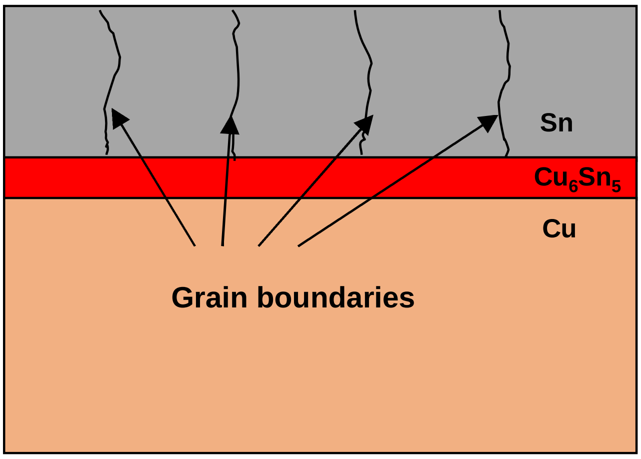

Figure 2: Start conditions for whisker growth

At temperatures below 60 °C the bulk diffusion of this CuSn phase is much lower than the intergranular diffusion. So the intermetallic phase more and more fills the grain boundaries which leads to an increasing stress in the Sn grains.

The Cu_6Sn_5 phase needs more space than the original material and is expanding the lattice spacing (see figure 3. The change in lattice spacing is inducing compressive stress to the tin plating.

The stress is finally released when whiskers grow (starting at small defects) and a mass transport is initiated out of the tin layer.

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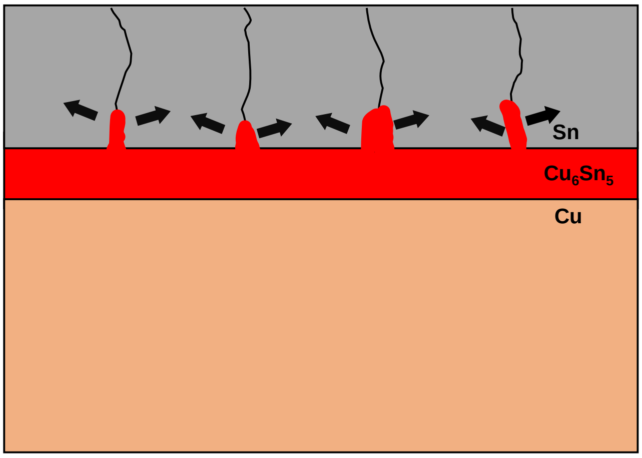

Figure 3: Stress induced by grain boundary diffusion

The tin oxide, shown in figure 4, has a similar effect on top of the tin. SnO_2 as well as SnO need more space than tin alone, so the humidity or corrosion taking the way down on the grain boundaries will lead to compressive stress, too.

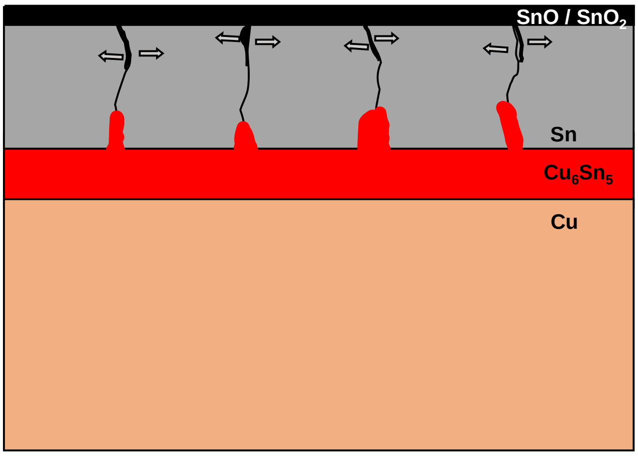

Figure 4: Stress induced by oxygen growth

Impurities contribute to further stress as they easily can be oxidized. So the tin plating chemistry and process will directly influence the tendency of whisker growth.

Electroplated finishes (especially "bright" finishes) therefore appear to be most susceptible to whisker formation because this process is introducing more impurities into the grains and as there are smaller grains it has also more grain boundaries.

Last but not least the influence of externally applied compressive stress has to be considered. Bending or forming tin coated wires or lead frames (lead forming prior to mounting of an electronic component) as well as scratches or torqueing against the coated surface introduce regions of potential whisker growth.

2.3. Mitigating whisker growth

From the theories above, one can easily conclude:

To avoid whisker growth it is necessary to avoid any stress on a tin plated material. The stress can be reduced by taking in account one or more of the following guidelines.

- Avoid a big difference of the CTE (Coefficient of Thermal Expansion) between plating material and substrate.
- If possible, use matte tin platings to reduce impurities and have bigger grains. For instance the carbon content of matte tin is much lower than for bright tin platings.
- Make thick electroplated Sn coatings (empirical value >10 µm) when plating directly on copper, as the induced stress will be reduced by thicker films. The bigger grains act as a damping for the forces in deeper layers. Anyway, with the formation of horizontal grain boundaries the migration of Cu to the surface areas is stopped, where the whisker are very sensitive to compressive forces.
- Avoid mechanical treatment without any further annealing. Especially compressed areas (inner side of bending) are sensitive to a whisker formation.
- Make a heat treatment, within 24 h after plating, at higher temperatures >60 °C (preferred 1 h at 150 °C). A Cu_3Sn layer is formed out of and below Cu_6Sn_5 phase acting as a barrier layer for further migration of Cu_6Sn_5 (see figure 5). The Cu_3Sn has lower molecular volume and will not add to stress in the tin layer. As the bulk diffusion is predominant in higher temperatures, a regular double layer is formed. The tendency to move into the grain boundaries is lower, as with the thickness of the barrier layers copper movement is reduced.
- Usage of a barrier layer between the copper (base material) and the tin-layer. In normal cases an electroplated nickel-layer (Würth Elektronik specification: average thickness 2 µm), which also prevents growth of Cu_6Sn_5 layer, is used. The hereby formed Ni_3Sn has a lower molecular volume than the Cu_6Sn_5 leading to tensile stress which can partly compensate the compressive stress of the surrounding. The migration of copper through the blocking layer is stopped and there will be only small coper parts from the original Cu_6Sn_5 layer going into the grain boundaries.
- Use hot dipping of tin, which gives homogeneous layers and bigger grains. It has low level impurities and is forming stress free buildups due to the hot process. Impurities are always a center of oxidations. The lattice is disturbed in the surroundings and oxygen in combination with hydrogen can move easy along this paths inducing stress. For THT components where a solder dipping process can easily be done, this method is mostly chosen.

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- Silver as barrier layer between copper base material and tin top layer is also a common used method to prevent tin whisker.

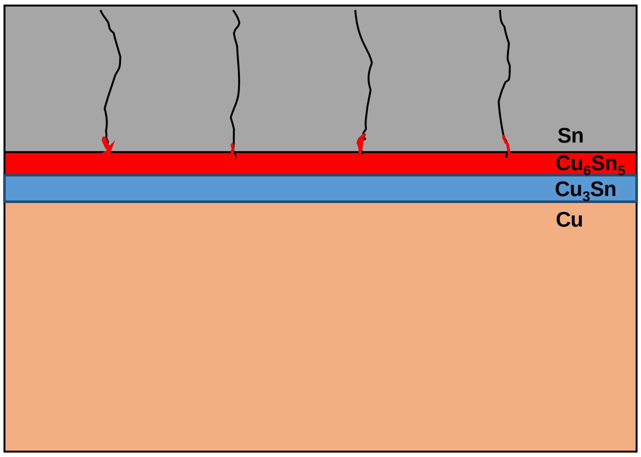

Figure 5: Formation of Cu_3Sn by annealing

2.4. Test conditions to prove low whisker risk

There will be always small regions of stress in a layer and thus the risk for whiskers will always be there. However it is commonly agreed, that whisker growth that will saturate at a length of <50 µm within several hundreds of hours (mostly 2000 h) can be tolerated (JESD 22A121A).

In the JESD 201 recommended tests for different layers used in electronics industry can be found.

In general there are three tests that have to be done. Many companies follow these recommendations; however have modified the tests due to their components.

These 3 tests are:

a. Temperature Cycling

(-40 °C to 85 °C / 1000 cycles)

A temperature cycling is a common agreement to prove whisker “free” parts. This test accelerates the stress by thermal mismatches of the layers. For different parts and companies the lower temperatures range from -55 °C to -25 °C and cycles vary from 3 times/h to a dwell time of 30 min for each step.

b. Ambient Temperature and Humidity Storage

(30°C and RH 60% till 4000 h)

Due to the preferred grain boundary diffusion of Cu_6Sn_5 at lower temperatures, storage and humidity at room temperature are increasing whisker formation. This test is often cancelled, but it is representing the actual conditions in the applications.

High Humidity and Temperature Storage

(60 °C and RH 90 % till 4000 h)

This is to increase the oxidation at higher temperatures. It is still in the region where whisker typically occur (-55 °C < T < 85 °C). The temperature is relative low, as higher temperatures would lead to the contradictory effect of recrystallization and stress release. However, some companies prefer to make 85 / 85 tests.

3. Whisker mitigation at WE eiSos

Würth Elektronik eiSos consequently follows the theories and recommendations above to reduce the risk of whisker formation. In addition to that, WE eiSos also does whisker tests to prove the quality for selected platings.

As an example, the following pictures show an electroplated tin surface of a SMD lead with 2 µm (average) nickel underplating before and after a whisker growth test which was carried out by an external accredited lab.

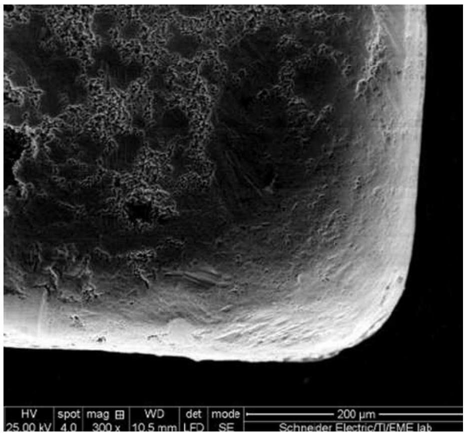

Figure 6: SEM image of tin surface before test

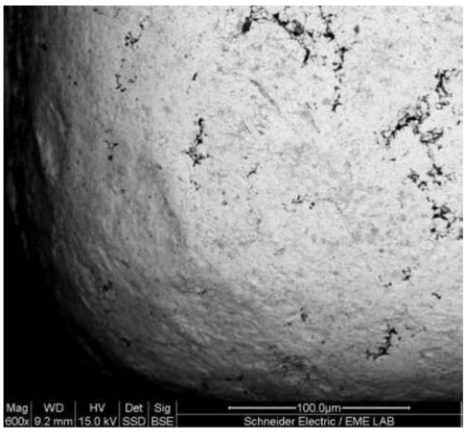

Figure 7: SEM image of tin surface after 1500 h, RH 93 %, 55 °C

As can be seen in Figure 6 and Figure 7, there was no whisker growth detected. These tests are carried out, to verify the effectiveness of the whisker mitigation strategies of Würth Elektronik eiSos.

4. Summary

Würth Elektronik eiSos has many years' experience in passive components. The surface finishes used on the electronic components have low risk of whisker growth.

5. Literature

1) Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on Waste Electrical and Electronic Equipment (WEEE)

2) Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS)

3) C. Xu, Y. Zhang, C. Fan, and J. Abys: “Understanding Whisker Phenomenon: The Driving Force for Whisker Formation”, CircuiTree, pp. 94-105, 2002.

4) J. Smetana: ”Theory of Tin Whisker Growth “The End Game””, iNEMI Tin Whisker Workshop at ECTC, 2005, updated 2007

5) L. Panashchenko: “The Art of Metal Whisker Appreciation: A Practical Guide for Electronics Professionals”, IPC Tin Whisker Conference, 2012

6) JESD22-A121: Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes, July 2004

7) JESD201: Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finishes, 2006

8) JEDEC/IPC: JOINT PUBLICATION No. 2,”Current Tin Whiskers Theory and Mitigation Practices”, 2006

9) NASA Electronic Parts & Packaging (NEPP) Program, http://nepp.nasa.gov/whisker

APPLICATION NOTE

Whisker

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CONTACT INFORMATION

Würth Elektronik eiSos GmbH & Co. KG
Max-Eyth-Str. 1, 74638 Waldenburg, Germany
Tel.: +49 (0) 7942 / 945 – 0
Email: appnotes@we-online.de
Web: http://www.we-online.com