Webinar

Via Filling – Applications in Practice
Agenda

- Via Filling
  - Through Hole Vias - IPC-4761
    - Plugging
    - Filling
    - Filled & Capped
  - Microvia Filling and Stacked Vias

Stefan Keller
Product Manager
Via Filling

Overview Through Hole Vias

Wording: **IPC-4761**
Design Guide for Protection of Printed Board Via Structures
Type 1 to 7

*Tenting:* not relevant any more

**Plugging + Filling**

*Important: precise definition / specification*
Via Filling – Through Hole Vias

Plugging

Plugging (IPC-4761 Type 3)

Sealing of vias from one side (screen printing process)
Very cost-effective

Applications:
- Prevention of solder fill on solder wave
- Vacuum handling during further processing
- Coating after assembly – prevent flow off

- Not suitable for vias in solder areas

Sealing from both sides is problematic
- Air entrapment > cracking
- Chemical entrapment > corrosion
Via Filling – Through Hole Vias

Plugging

**Plugging**  (IPC-4761 Type 3)

Design Rules (WE):
- Final diameter 0.15 – 0.50 mm
- Vias open
- Sufficient distance hole to solder area
  at least 0.25 mm at 0.20 mm final Ø,
  greater distance with greater via diameters

Printing process after final surface process in order to protect the via hole walls from corrosion
Uncritical with ENIG (Ni/Au)
(immersion Sn: pure tin thickness is reduced by the curing process)

Please note:
Bumps (up to 50 µm / max. 70 µm) –
critical close to solder areas especially BGAs
Via Filling – Through Hole Vias

Filled Via (IPC-4761 Type 6) covered with solder resist

Normally filled / sealed with solder resist after etching process
> before surface finish

Cheaper than filling with epoxy resin

Concerns:
- Potential of voids and cracks caused by shrinkage of the resist
- Long time reliability possibly reduced (risk of corrosion in the barrels)

WE: not used in the German plants
Filled Via (IPC-4761 Type 5)

= Filling with epoxy resin - without coverage

Application:
HDI build-ups - buried vias on inner layers to prevent voids and dents on the copper foil above
(WE: applied with core thickness about 1.10 mm or greater)

Outer layers:
Copper cap automatically (= Type 7 filled & capped) by plating process of component holes
Via Filling – Through Hole Vias
Filled & Capped

IPC-4761 Type 7

- Filling completely with epoxy resin + covering metallization
- Several additional process steps / additional costs up to + 20%
- Possibly limitations for design and manufacturability

Aim:
Prevention solder drainage / Vias in solder areas
High solder process reliability
Optimal via protection

Main application:

Thermal vias
  Short heat paths
  Low thermal resistance

Mandatory with glued heatsinks
  (to prevent breakdowns on the hole edges)
Via Filling – Through Hole Vias

Filled & Capped

IPC-4761 Type 5 / 7

**Manufacturing Process**

- Copper
- FR4
- Copper

- Drilling

- Plating process

- Vacuum – Filling - Process

- Curing

- Brushing / Planarizing

- optional: Cap plating (Type 7)

- Drilling + Plating THT holes

Source: WE
Via Filling – Through Hole Vias
Filled & Capped

Examples for Vertical Vacuum Filling Machines
Via Filling – Through Hole Vias
Filled & Capped

IPC-4761 Type 7

Application example:
Compact engine control unit
High power density (max. 60W)
Maintenance-free
Without active cooling

Heat dissipation of the components via Thermal Vias / Alu-Heatsink / Housing
Via Filling

**Thermal Simulation and Measurement**

Further optimizations necessary?

Thermal Simulation - Würth Elektronik CBT Product Management
Via Filling – Through Hole Vias

Filled & Capped

Alternatives:

Partial solder area instead of entire area
(multiple design possibilities)
Via filling not needed

HDI build-up
Buried via + microvia instead of filled PTH via

Improved heat dissipation
with additional microvias in the soldering area
and buried vias on inner layers

Additional costs possibly low
Via Filling – Through Hole Vias

Filled & Capped

IPC-4761 Type 7

Further applications:

- Via in pad (soldering pad / BGA pad)
  components put directly onto vias
  (e.g. short distance to the BGA on other side)

- Via too close to soldering pad
  („design mistake“)

Cost consideration / Relationships
Design ↔ PCB costs and processes

Alternatives:

- Dogbone
- HDI
  especially BGAs
Quality Requirements (IPC-6012)

- Plating thickness
- Cap Plating
- Voids ....

*partial differences between class 2 and 3*
Via Filling – Though Hole Vias

Filled & Capped

Design-Parameters

Recommendations:

- Drill diameter 0.25 - 0.50 mm
  - Thermal vias 0.30 / 0.35 mm End Ø
- Pitch min. 0.80 mm
- PCB thickness 0.65 – 2.50 mm
- All vias filled

Copper plating thickness
on outer layers often thicker
Relationship design parameter – final copper thickness

> Recommendation:
  spacing 125 µm (instead 100 µm), especially
  IPC Class 3 requirements
Via Filling

Microvia Filling

IPC-7095C: „max. 22% of the image diameter“

The appearance of voids depends on:
- Flux, solder paste
- Temperature profile
- ...

Outer layers
- Solder process reliability
- Reliability solder joint

•μViP technology is being used by WABCO in HDI products for over 10 years with 0 ppm
Via Filling

Microvia Filling

IPC-7095C: “max. 22% of the image diameter”

The appearance of voids depends on:

- Flux, solder paste
- Temperature profile
- ...

1. Copper - Filling
   Common technology for microvias
   Very special plating process
   Degree of filling > 80% usually enough

2. Filled & Capped
   Additional process steps
   Plating thickness on surface!

Outer layers
- Solder process reliability
- Reliability solder joint
Via Filling

Microvia Filling

Inner layers

Stacked Microvias

Applications:

- 0.40 mm Pitch BGA
- Miniaturization
  - Please note: costs
- AnyLayer / ELIC – build-ups (Mobiles)
Via Filling

Stacked Vias

IPC-2262A
Design Standard for HDI Printed Boards

WE - Recommendation

+ ZVEI - AK
Quality
German Electronic Manufacturers' Association

≥ 0.40 mm

Existing Designs should be changed asap!

We would support you!

Figure 5-4  Type III HDI Construction with Stacked Microvias
(Caution: Unbalanced constructions as shown above may result in excessive bow and twist.)
Note 1: Stacking not recommended for resin or conductive/non-conductive filled microvias.
Note 2: Stacking not recommended over resin or conductive/non-conductive filled vias due to potential for reduced reliability. The use of staggered structures instead is recommended.

Caution: HDI design with microvias stacked or buried vias is not recommended.
Via Filling

Stacked Vias

Differences in long-term reliability stacked versus staggered Vias

Staggered Vias withstand usually more thermal cycles!

Basis: fast temperature cycle tests / Interconnect Stress Test by WE (and international published investigations)

Recommendation: existing Designs should be changed as soon as possible
- Reduction of risk of damage
- Usually cost reduction potential
- Better delivery performance
Knowing the relationships - is a secret of success!

We are looking forward to good cooperation!

Stefan Keller
Product Manager
stefan.keller@we-online.de