customer	
pcb name	
WE article number	
engineer	
date	

WÜRTH ELEKTRONIK

Multilayer 10 Layers

PCB Thickness : 1,70 mm +/- 10%

Rigid area Structure	Rigid area Thickness	Material description		Viatypes	Layer usage	Impedance Er	Impedance Z[Ohm] Line / Space	
Soldermask	**15**					3,5		
L1	**45**	* Incl. Plating	Top-Layer					
	140	FR4 TG 150				3,7		
L2	**35**							
	150	FR4 TG 150				4,3		
L3	**35**							
	140	FR4 TG 150				3,7		
L4	**35**							
	150	FR4 TG 150				4,3		
L5	**35**							
	140	FR4 TG 150				3,7		
L6	**35**							
	150	FR4 TG 150				4,3		
L7	**35**							
	140	FR4 TG 150				3,7		
L8	**35**							
	150	FR4 TG 150				4,3		
L9	**35**							
	140	FR4 TG 150				3,7		
L10	**45**	* Incl. Plating	Bottom-Layer					
Soldermask	**15**					3,5		

Notes:

50 % copper occupancy IL

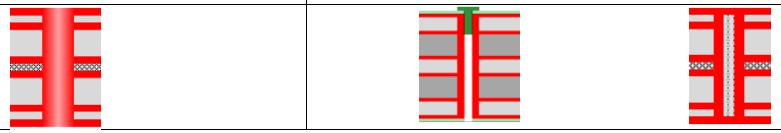
final copper thickness according to IPC 6012

Dielectric material according IPC-4101 E / 128 (127)

For Microvia technology please use our HDI stackups

Revision: Created: W. Brylka / Scrutinised: A. Schilpp / Approved: A.Schilpp

Template Revision: 06/2018 by Andreas Schilpp

Via types - Standard and options

Standard Via	*Plugged Via (Type III-a)*	*Filled & Capped Via (IPC Type VII)*