Embedding Technology Design Guide

INDICATORS FOR TECHNOLOGY USE

ET Solder

- Active components that are not available as a bare die
- Active and passive components
- Range of the solid SMD components can be used (with restrictions)

ET Microvia

- Combination of active and passive components
- Highly reliable assembly and packaging technology
- Copper or nickel-palladium pad metallisation on the components

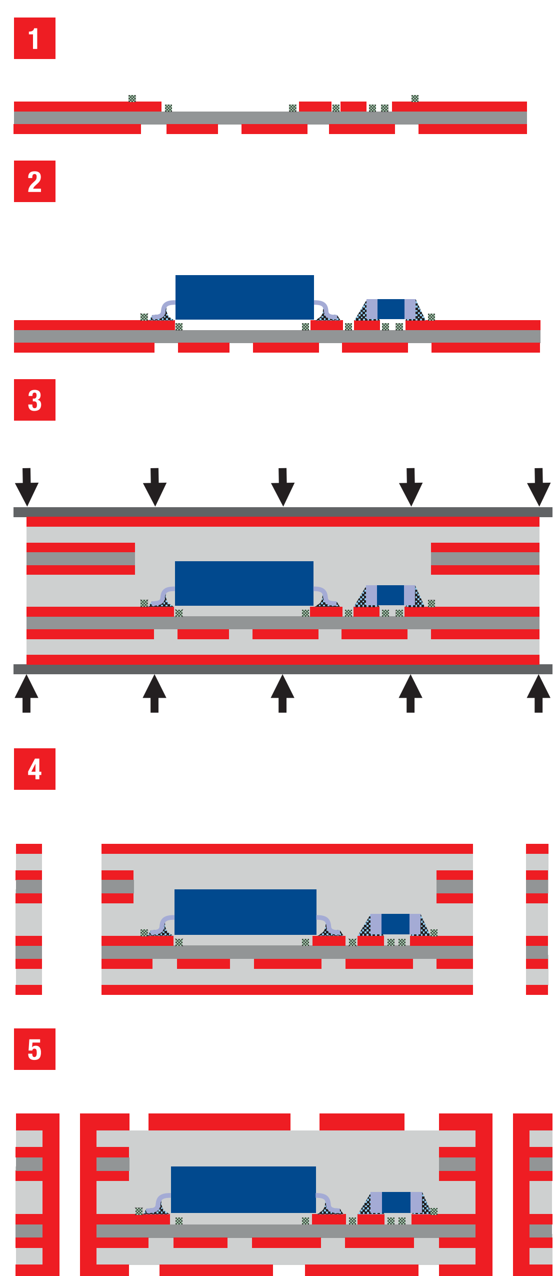
ET Flip-Chip

- Active components, which were previously wire-bonded
- No passive components possible
- Active components with pitch < 250 µm

PROCESS FLOWS

The process flows shown here only serve as a description of the process. The actual stack-up and the number of layers will be adapted to the customer's requirement.

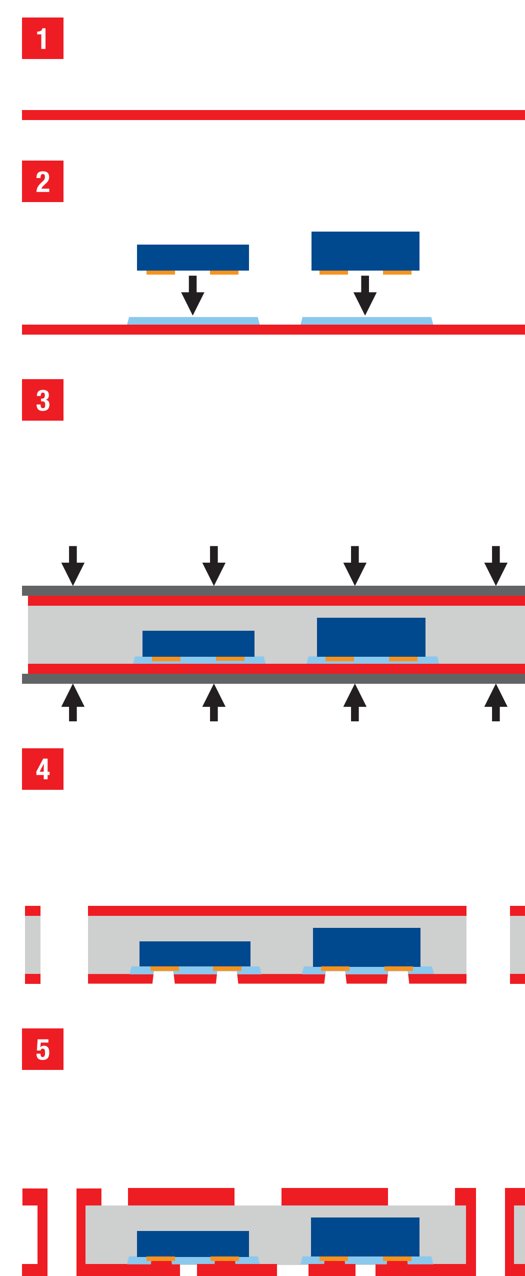
ET Solder



1. Structured inner layer core with footprint for SMD components
2. SMD assembly (lead free reflow)
3. Multilayer lamination

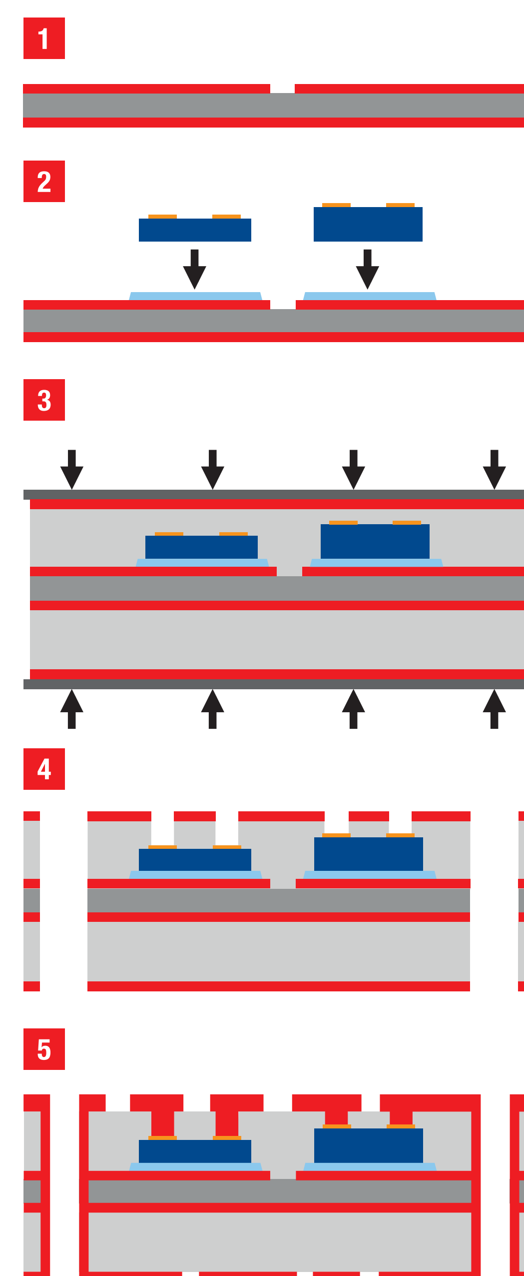
4+5 Depending on customer request, additional circuit board processes

ET Microvia Version 1



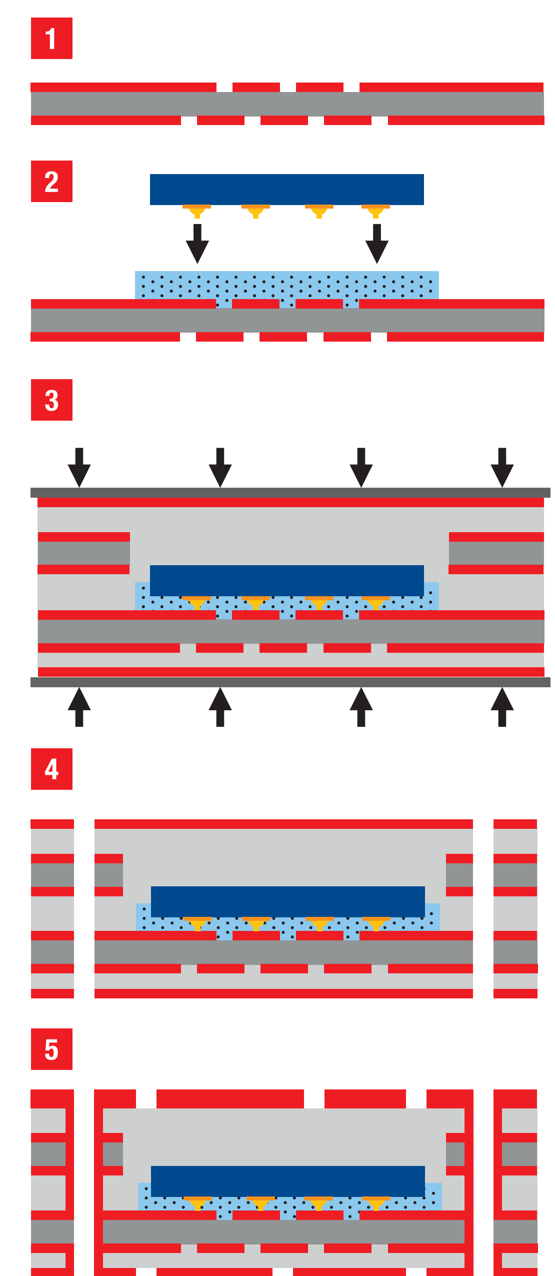
1. Cu foil as starting substrate
2. Assembly (face-down) on Cu foil with non-conductive adhesive (NCA)
3. Multilayer lamination
4. Laser drilling in Cu and adhesive
5. Electrical connection between chip and PCB via Cu metallisation and structuring

ET Microvia Version 2



1. Structured inner layer core
2. Assembly (face-up) on core with conductive (ICA – isotropic conductive adhesive) or non-conductive adhesive (NCA)
3. Multilayer lamination
4. Laser drilling in Cu and resin
5. Electrical connection between chip and PCB via Cu metallisation and structuring

ET Flip-Chip



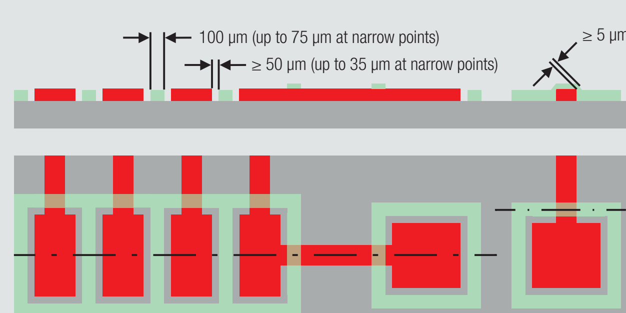
1. Structured inner layer core with footprint for Flip-Chip
2. Flip-Chip assembly using ACA adhesive (anisotropic conductive adhesive)
3. Multilayer lamination

4+5 Depending on customer request, additional circuit board processes

DESIGN RULES

Depending on the final buildup and design of the circuit board with embedded components, all circuit board designs with embedded components are subject to the Design Rules/Design Guides "Basic Design Guide", "Flex-Rigid Design Guide", "Thermal Management Design Guide" and "HDI Design Guide" that are currently applicable at Würth Elektronik. The additional specific design rules are as follows:

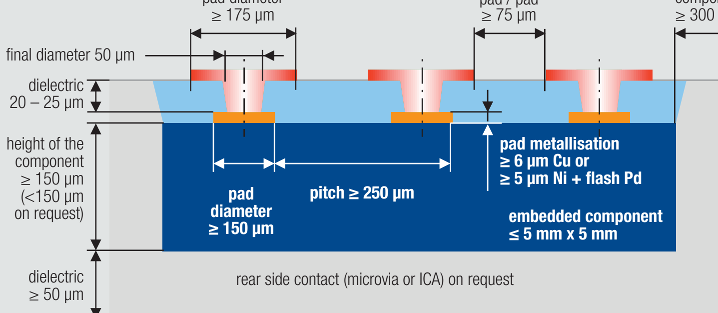
ET Solder



Regarding ET Solder, the design rules are only extended to include the rules for the inner solder mask which may NOT be designed across the entire area. The solder resist function is defined by frames surrounding the solder pads.

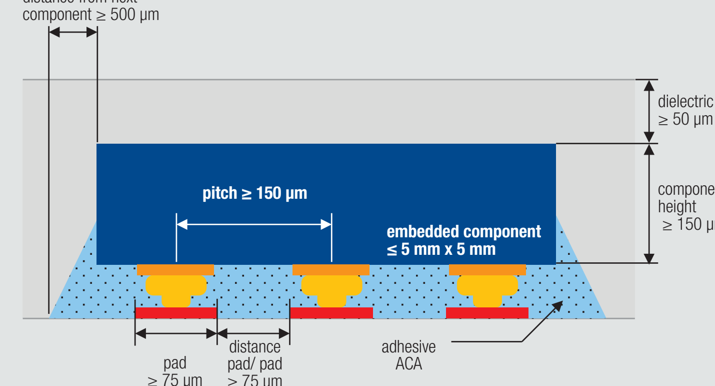
This rule for the solder mask applies to Cu thicknesses of 18 µm and 35 µm on the inner layer to be assembled. Please contact us for other Cu thicknesses.

ET Microvia



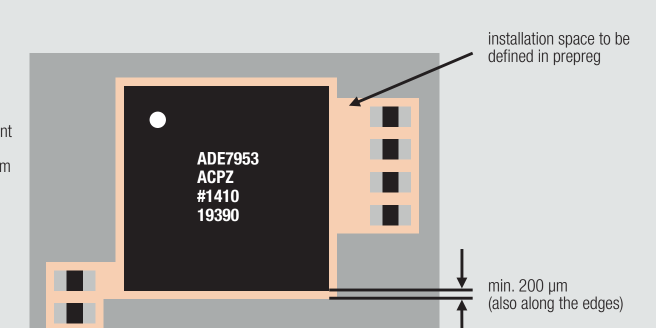
These minimum dimensions shown for Cu tracks, microvias and pads for the microvia only apply to the layer to be assembled. The maximum Cu thickness of this layer is 25 µm. Please contact us for other Cu thicknesses.

ET Flip-Chip



The dimensions for the Cu tracks for the ET Flip-Chip are based on Cu thicknesses ≤ 18 µm. Please contact us for Cu thicknesses > 18 µm.

Component positioning – resin flow



The following applies to the cut-outs milled in prepreg: All points within the cut-out must be accessible at a distance of ≤ 5.0 mm from the boundary of the cut-out.