# Gleanergy Multi-Source Energy Harvesting Demo Board with Battery Chargers and Life-Extenders for Use with DC2321A Dust Demo Board

## DESCRIPTION

Demonstration circuit 2344A development platform is a versatile Energy Harvesting Demo Board that is capable of accepting solar, thermal, and piezoelectric energy sources or any high impedance AC or DC source. The board contains four independent power circuits consisting of the following EH ICs:

- LTC3106 – 300mA, Low Voltage Buck-Boost Converter with PowerPath™ and 1.5µA Quiescent Current

- LTC3107 – Ultralow Voltage Energy Harvester and Primary Battery Life Extender

- LTC3330 – Nanopower Buck-Boost DC/DC with Energy Harvesting Battery Life Extender

- LTC3331 – Nanopower Buck-Boost DC/DC with Energy Harvesting Battery Charger

- LTC2935-2 – Ultralow Power Supervisor with Power-Fail Output Selectable Thresholds

The DC2344A demo board is designed to connect to a DC2321A, a Dust mote wireless sensor node demo board which monitors the batteries and the status signals of each IC.

The DC2344A hosts two types of energy harvesting transducers (thermoelectric generator and solar cells). A terminal block is used for connecting an external piezo-electric transducer or any other high impedance AC source to this board. In addition to the provided sources, input turrets allow the user to connect external transducers to the board.

As a backup power supply, the board holds a primary battery and a secondary battery which can be easily routed to any of the applicable ICs.

The board hosts groups of switches, jumpers, and resistors which allow its operation be configured in various ways. As a result, the system is very customizable and can be modified to meet the user's needs. This compatibility makes it a perfect evaluation tool for any low power energy harvesting system.

Please refer to the individual IC data sheets for the operation of each power management circuit. The application section of this demo manual describes the system level functionality of this board and the various ways it can be used in early design prototyping.

**Design files for this circuit board are available at http://www.linear.com/demo/DC2344A**
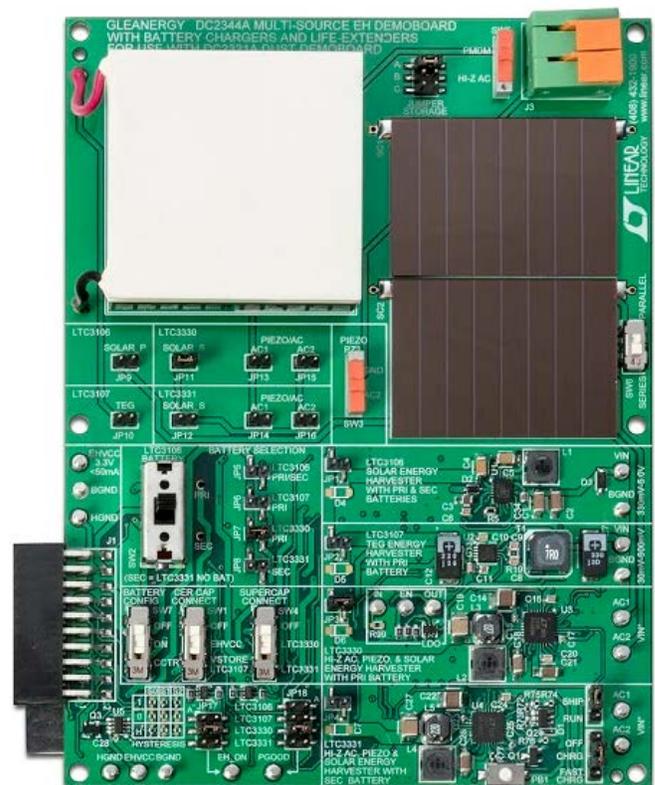
## BOARD PHOTO



**Figure 1. DC2344A in the Gleanergy Energy Harvesting Demonstration Kit for EH Wireless Sensor Nodes**

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# BOARD LAYOUT ORGANIZATION DIAGRAM

GLEANERGY™ DC2344A MULTI-SOURCE EH DEMOBOARD
WITH BATTERY CHARGERS AND LIFE-EXTENDERS
FOR USE WITH DC2321A DUST DEMOBOARD

PIEZO INPUT

(408) 432-1900
www.linear.com

LINEAR TECHNOLOGY

THERMOELECTRIC GENERATOR

SOLAR CELL 1

PARALLEL

SOLAR CELL 2

SERIES

TRANSDUCER SELECTION

BATTERY ROUTING

LTC3106

LTC3107

ENERGY MANAGEMENT

LTC3330

LTC2935-2

STATUS SIGNALS

LTC3331

EH_ON          PGOOD

**Figure 2. Board Layout Organization Diagram**

LINEAR TECHNOLOGY

# SPECIFICATIONS

| TYPE | PART | PARAMETER | CONDITIONS | MIN | TYPICAL/ DEFAULT | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|
| IC | LTC3106 | $V_{IN}$ | Backup Power Source Available | 0.33 | | 6 | V | |
| | | | Backup Power Source Unavailable | 0.85 | | | | |
| | | $V_{OUT}$ | | 1.8 | 3.3 | 5 | V | Set Using R6-R9, See Table 10 |
| | | $V_{STORE}$ | | 2.07 | 4 | 4 | V | Set Using R10-R13, See Table 11 |
| | LTC3107 | $V_{IN}$ | | 30 | | 500 | mV | Input to Transformer |
| | | $V_{OUT}$ | | $V_{BAT} - 0.23$ | | $V_{BAT} - 0.03$ | V | Min = Battery Powering Load Max = EH Powering Load |
| | LTC3330 | $V_{AC1}$&$V_{AC2}$ | | 4 | | 19 | V | |
| | | $I_{AC1}$&$I_{AC2}$ | | −50 | | 50 | mA | |
| | | $V_{OUT}$ | | 1.8 | 3.3 | 5 | V | Set Using R20-R25, See Table 14 |
| | | UVLO | Rising Falling | 4 3 | 7 6 | 18 17 | V | Set Using R38-R45, See Table 16 |
| | | LDO_OUT | | 1.2 | 3.3 | 3.3 | V | Set Using R26-R31, See Table 12 |
| | LTC3331 | $V_{AC1}$&$V_{AC2}$ | | 4 | | 19 | V | |
| | | $I_{AC1}$&$I_{AC2}$ | | −50 | | 50 | mA | |
| | | $V_{OUT}$ | | 1.8 | 3.3 | 5 | V | Set Using R46-R51, See Table 14 |
| | | UVLO | Default Rising Default Falling | 4 3 | 7 6 | 18 17 | V | |
| | | $V_{FLOAT}$ | | 3.45 | 4.0 | 4.2 | V | Set Using R52-R57, See Table 13 |
| | | $V_{LBD}$ | | 2.04 | 2.70 | 3.20 | V | See LTC3331 Data Sheet for More Information About These Levels |
| | | $V_{LBC\_BAT\_IN}$ | | 2.35 | 3.03 | 3.53 | V | |
| | | $V_{LBC\_BAT\_OUT}$ | | 3.02 | 3.70 | 4.20 | V | |
| Transducer | Solar Cell | Maximum Power | 200 Lux 400 Lux 600 Lux 1000 Lux | | 32 66 93 144 | | µW | For Single Solar Cell |
| | TEG | Power Output | $\Delta T = 3k$ $\Delta T = 5k$ $\Delta T = 10k$ $\Delta T = 15k$ | | 0.23 0.39 1.38 3.20 | | mW | At Max Power Point |
| Battery | Primary | Voltage | (Note 1) | 3.08 | 3 | 3.8 | V | Replace Battery Below Min Level or Modify Circuit Configuration |
| | Secondary | Voltage | (Note 2) | 3.03 | 3.6 | 4.2 | V | |
| Storage | Ceramic Capacitors | Energy Capacity | EHVCC = 3.3V | | 2.3 | | mJ | Between 3.3V and the Default 2.25V LTC2935-2 Falling Threshold |
| | Supercap | Energy Capacity | | | 37.9 | | mJ | |

The "Typical/Default" column shows data corresponding to the factory configuration of the board where all 0Ω resistors are in their default positions. The min/max columns show the minimum or maximum allowable levels.

**Note 1:** Because the output voltage of the LTC3107 is dependent on the battery voltage, $V_{OUT\_LTC3107}$ will be too low to reach the default 2.85V ground-switching threshold if the primary battery is below 3.08V. Refer to the LTC2935-2 Power Switch Circuit section to modify this threshold, or replace the battery.

**Note 2:** If the secondary battery voltage is below the default 3.03V BAT_IN connect threshold of the LTC3331, it cannot be connected internally to the IC to be used as a backsup source. The battery can still be charged in this state if EH power is available. Alternatively, the connect threshold ($V_{LBC\_BAT\_IN}$) can be changed according to Table 13 or the battery can be replaced.

# ASSEMBLY DRAWING



**Figure 3. DC2344A Top Assembly Drawing**

# ASSEMBLY DRAWING

REV A — LTC CONFIDENTIAL - FOR CUSTOMER USE ONLY

C29

**LTC3330 LDO VOLTAGE SELECTION**

| LDO2 | LDO1 | LDO0 | LDO_OUT |
|------|------|------|---------|
| 0 | 0 | 0 | 1.2V |
| 0 | 0 | 1 | 1.5V |
| 0 | 1 | 0 | 1.8V |
| 0 | 1 | 1 | 2.0V |
| 1 | 0 | 0 | 2.5V |
| 1 | 0 | 1 | 3.0V |
| D  1 | 1 | 0 | 3.3V |
| 1 | 1 | 1 | =LDO_IN |

**OUTPUT VOLTAGE SELECT**

| OUT2 | OUT1 | OUT0 | VOUT |
|------|------|------|------|
| 0 | 0 | 0 | 1.8V |
| 0 | 0 | 1 | 2.5V |
| 0 | 1 | 0 | 2.8V |
| 0 | 1 | 1 | 3.0V |
| D  1 | 0 | 0 | 3.3V |
| 1 | 0 | 1 | 3.6V |
| 1 | 1 | 0 | 4.5V |
| 1 | 1 | 1 | 5.0V |

**LTC3330 AND LTC3331 UVLO SELECTION**

| UV3 | UV2 | UV1 | UV0 | UVLO RISE | UVLO FALLING |
|-----|-----|-----|-----|-----------|--------------|
| 0 | 0 | 0 | 0 | 4V | 3V |
| 0 | 0 | 0 | 1 | 5V | 4V |
| 0 | 0 | 1 | 0 | 6V | 5V |
| D  0 | 0 | 1 | 1 | 7V | 6V |
| 0 | 1 | 0 | 0 | 8V | 7V |
| 0 | 1 | 0 | 1 | 8V | 5V |
| 0 | 1 | 1 | 0 | 10V | 9V |
| 0 | 1 | 1 | 1 | 10V | 5V |
| 1 | 0 | 0 | 0 | 12V | 11V |
| 1 | 0 | 0 | 1 | 12V | 5V |
| 1 | 0 | 1 | 0 | 14V | 13V |
| 1 | 0 | 1 | 1 | 14V | 5V |
| 1 | 1 | 0 | 0 | 16V | 15V |
| 1 | 1 | 0 | 1 | 16V | 5V |
| 1 | 1 | 1 | 0 | 18V | 17V |
| 1 | 1 | 1 | 1 | 18V | 5V |

**LTC3106 VOUT JUMPER CONFIGURATION**

| OS1 | OS2 | VOUT |
|-----|-----|------|
| 0 | 0 | 1.8V |
| 0 | 1 | 3.0V |
| D  1 | 0 | 3.3V |
| 1 | 1 | 5.0V |

**LTC3106 VSTORE JUMPER CONFIGURATION**

| SS1 | SS2 | VSTORE |
|-----|-----|--------|
| 0 | 1 | 2.07V |
| 0 | 1 | 2.9V |
| 1 | 0 | 3.015V |
| D  1 | 1 | 4.0V |

**ILIM SELECTION INSTALL**

| IPK2 | IPK1 | IPK0 | ILIM |
|------|------|------|------|
| 0 | 0 | 0 | 5mA |
| 0 | 0 | 1 | 10mA |
| 0 | 1 | 0 | 15mA |
| 0 | 1 | 1 | 25mA |
| D  1 | 0 | 0 | 50mA |
| 1 | 0 | 1 | 100mA |
| 1 | 1 | 0 | 150mA |
| 1 | 1 | 1 | 250mA |

**LTC2935-2 THRESHOLD SELECTION**

| S0 | S1 | S2 | RESET THRESH | POWER-FAIL THRESH |
|----|----|----|--------------|-------------------|
| 0 | 0 | 0 | 3.30V | 3.45V |
| 1 | 0 | 0 | 3.15V | 3.30V |
| 1 | 1 | 0 | 3.00V | 3.15V |
| 0 | 1 | 0 | 2.85V | 3.00V |
| D↑ 0 | 1 | 1 | 2.70V | 2.85V |
| 0 | 0 | 1 | 2.55V | 2.70V |
| 1 | 0 | 1 | 2.40V | 2.55V |
| D↓ 1 | 1 | 1 | 2.25V | 2.40V |

D = DEFAULT SETTINGS
D↑ = DEFAULT RISING
D↓ = DEFAULT FALLING

**FLOAT SELECT AND BATTERY CONNECTION THRESHOLDS**

| LBSEL | FLOAT1 | FLOAT0 | FLOAT | CONNECT EH | CONNECT PB1 | DISCONNECT |
|-------|--------|--------|-------|------------|-------------|------------|
| 0 | 0 | 0 | 3.45V | 2.35V | 3.02V | 2.04V |
| D  0 | 0 | 1 | 4.0V | 3.03V | 3.70V | 2.70V |
| 0 | 1 | 0 | 4.1V | 3.03V | 3.70V | 2.70V |
| 0 | 1 | 1 | 4.2V | 3.03V | 3.70V | 2.70V |
| 1 | 0 | 0 | 3.45V | 2.85V | N/A | 2.51V |
| 1 | 0 | 1 | 4.0V | 3.53V | N/A | 3.20V |
| 1 | 1 | 0 | 4.1V | 3.53V | N/A | 3.20V |
| 1 | 1 | 1 | 4.2V | 3.53V | N/A | 3.20V |

**LTC3331 BATTERY CHARGE CURRENT**

| R72 | I_CHRG |
|-----|--------|
| 113 | 5mA |
| 75.0 | 7.5mA |
| 56.2 | 10mA D |

LTC3106 — TP1, OS, SS, BAL OFF, R93 R94 R95, ON R96 R97 R98

OFF ON — HIGH CAPCY / RUN / MPPC — Q4 R100 R101 R1 R2 R18

ILIMSEL — LO HI

LTC3107 Q5 Q6 — OUT S0 S1 S2 U6 C35 R105 R103 R104 R102 — UV 3 2 1 0 — TP2 TP5

LTC3330 — LDO R109 Q8 TP6 TP3 R108 — IPK 2 1 0 — R107 Q7 R106

LTC3331 — OUT — VIN* / IIN: 4V≤Vpk≤19V ≤50mA, Vpk>19V ≤25mA — UV 3 2 1 0

NOTE: DISCONNECT BATTERIES BEFORE MOVING RESISTORS

FLOAT TP7 — LBSEL 1 0 — TP4 R113 R111 Q9 Q10 R112 R110 — IPK 2 1 0

C31 / C30 / C32 C33 R88 R87 — NOTE: BEFORE POPULATING C31, PLACE INSULATING TAPE OVER THESE CONTACTS

R127 Q14 R126 — SEC BAT2 / PRI BAT1

CAUTION: DO NOT PLACE PRI BAT INTO SEC BAT HOLDER
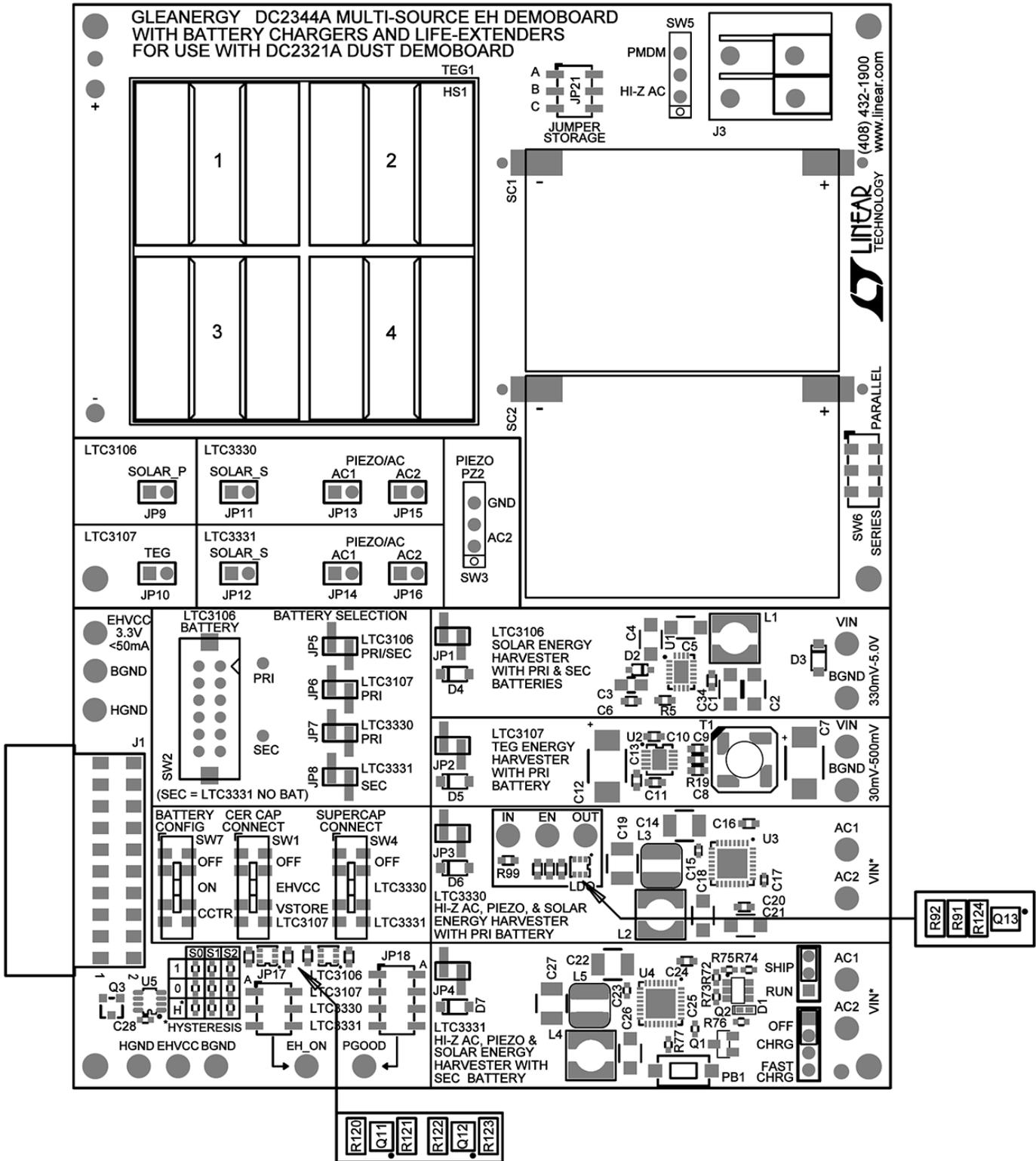
CERAMIC CAP STORAGE CO1-10

R125 R128 — J2

**Figure 4. DC2344A Bottom Assembly Drawing**

# QUICK START PROCEDURE

Reference designators for jumpers and default positions for 0Ω resistors are listed on the assembly drawing. Reference designators for 0Ω resistors are listed in Figure 20.

1. Remove the DC2344A from its box and set it on a table where it has access to a reasonable amount of light.

**Table 1. Available Light vs LTC3330 Startup Time**

| ILLUMINANCE (LUX) | STARTUP TIME (SEC) |
|---|---|
| 400 | 75 |
| 600 | 43 |
| 800 | 30 |
| 1000 | 24 |

Note: startup time is defined as the time taken for a completely discharged circuit to reach the default output switching threshold of 2.85V with the bank of ceramic caps connected to EHVCC.

2. All 0Ω resistors should be in their default position (see Figure 4, default resistors have dots). Verify that the jumpers and switches are also in their default setting as follows:

**Table 2. Default Jumper/Switch Configuration**

| TYPE | REFERENCE DESIGNATOR | POSITION |
|---|---|---|
| JUMPER | JP1 – JP4 | Shunt on JP3 |
| | JP5 – JP8 | (Not Installed) |
| | JP9 – JP16 | Shunt on JP11 |
| | JP17 | Shunt on JP17B |
| | JP18 | Shunt on JP18C |
| | JP19 | SHIP |
| | JP20 | OFF |
| SWITCH | SW1 | EHVCC |
| | SW2 | PRI |
| | SW3 | GND |
| | SW4 | OFF |
| | SW5 | PMDM |
| | SW6 | SERIES |
| | SW7 | OFF |

3. This configuration ensures that solar power is routed to the LTC3330 and that the output of the LTC3330 is routed to EHVCC. Connect VM1 as shown in Figure 5 and observe that the voltage is rising to, or regulated at, 3.3V.

4. Cover the solar cells with your hand and observe the voltage start to drop. Uncover the solar cells and let VM1 regulate to 3.3V.

5. Connect VM2 and LOAD1 as shown in Figure 5. Cover the solar cells again and observe the voltage on VM2 quickly fall to 0V once VM1 drops past 2.25V. Remove your hand and observe the voltage on VM2 quickly rise to the voltage on VM1 as VM1 rises past 2.85V.

6. While covering the solar cells, set SW7 = "ON" and install JP7 to connect the primary battery to the LTC3330. Observe as the voltage on both meters quickly rises to 3.3V and regulates.

7. Uncover the solar cells and observe that there is no change in output voltage as the IC switches from using battery power to harvested solar power.
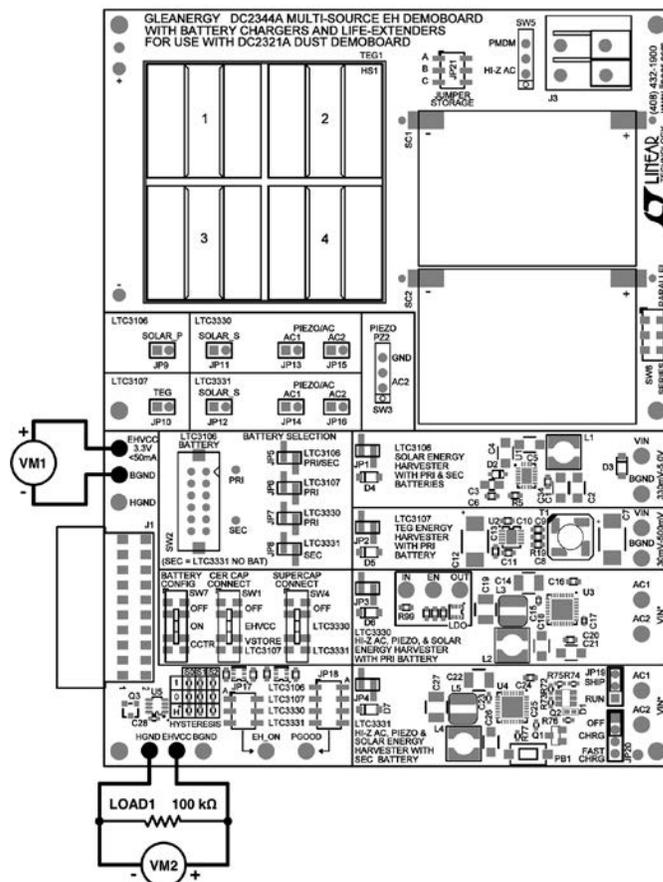


**Figure 5. Setup for General DC2344A Test Procedure**

# QUICK START PROCEDURE

8. Reconfigure the board according to Figure 6:

   a) Move the shunt from JP3 to JP2 in order to route the LTC3107's output to the load. Move the shunt from JP7 to JP6 in order to power the LTC3107 from the primary battery. Move the shunt from JP11 to JP10 in order to route the TEG to the LTC3107's input transformer.

   b) Move the positive lead of VM2 to the shunt on JP6 in order to measure the voltage of the primary battery. Move the negative lead to BGND.
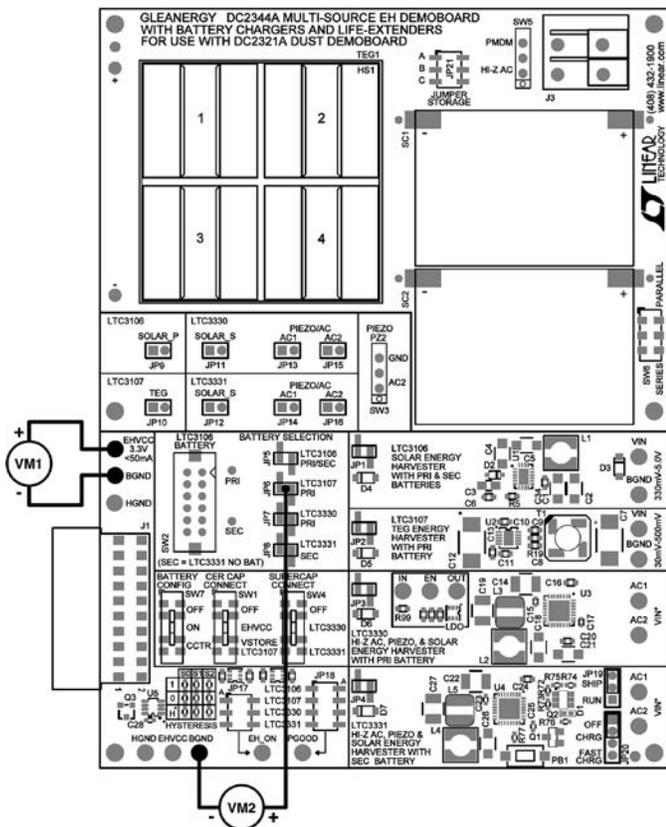


**Figure 6. Setup for DC2344A Test Procedure with LTC3107**

9. Observe the voltage on VM1 and VM2. The voltage on VM1 should be approximately 230mV below the voltage of VM2.

10. Place a warm object, such as your hand, onto the TEG such that good contact is made across the entire surface. Observe the voltage on VM1 rise to 30mV below the voltage on VM2 as the LTC3107 powers the load using harvested thermal energy. NOTE: if the TEG is already at a temperature near the temperature of the warm object, this step may not work. Either wait for the TEG to cool or use a cold object (such as cold spray) to cool the side of the TEG attached to the heat sink.

11. Remove the warm object and observe the voltage on VM1 fall to approximately 230mV below the voltage of VM2 as the LTC3107 powers the load from its backup battery.

**Optional Continuation with Any Transducer**

The source routing flowcharts (Figures 9-11) show how to configure the board for use with any energy harvesting transducer. A user can follow these routing guides to evaluate ICs with the on-board sources or any transducer connected to the board using the input turrets (on the right side of the board) or the terminal block, J3. Additional information on custom configurations using the terminal block can be found in the Custom Transducer Configurations section.

NOTE: IC configurations such as the UVLO windows of the LTC3330 and LTC3331 may need to be changed for use with custom transducers. Refer to Tables 9-16.

1. Reconfigure the board according to Figure 5.

2. Decide which transducer type to use and find the appropriate flowchart. Start at the left of the flowchart and choose settings until a box in the "Configure Demo Board" section is reached.

3. Configure all jumpers and switches listed in the appropriate box. Any jumpers or switches that are not listed in the box are irrelevant for the chosen configuration.

4. Power the energy harvesting transducer and observe the voltage on VM1 and VM2 which should be near 3.3V by default (less for LTC3107).

# OPERATION OVERVIEW

The function of the DC2344A is to provide a low-power wireless application, such as a wireless sensor node, with an uninterrupted power supply which uses as much harvested energy as is available to extend the life of a primary or secondary battery.

The on-board transducers provide energy harvested from the environment, and the batteries serve as a backup supply which can be charged or unused if energy from the transducers is sufficient to power the load.

The four energy-harvesting ICs switch between these sources, using all available harvested energy and as much backup energy as is needed to keep a regulated output.

A supercapacitor and a bank of ceramic capacitors are able to be connected to the board's output in order to store energy, smooth the output, and provide large pulses of current to the load. This helps to ensure that power remains uninterrupted for pulsed loads such as data transmission events on a wireless sensor node.

An LTC2935-2 low-power manager IC monitors the output voltage and switches the ground on the header (HGND) so that it is connected to the ground reference for the rest of the DC2344A (BGND). This completes the circuit and ensures that the load receives a quickly-rising power supply and also that energy storage is able to gather sufficient energy for the required application before the load begins taking power.

For use with the DC2321A demo application, DC2344A additionally passes buffered IC status signals through the output header. Both batteries can also be routed through coulomb counters on DC2321A and back to DC2344A to power the ICs; this allows the voltage, current, and charge of the batteries to be monitored.
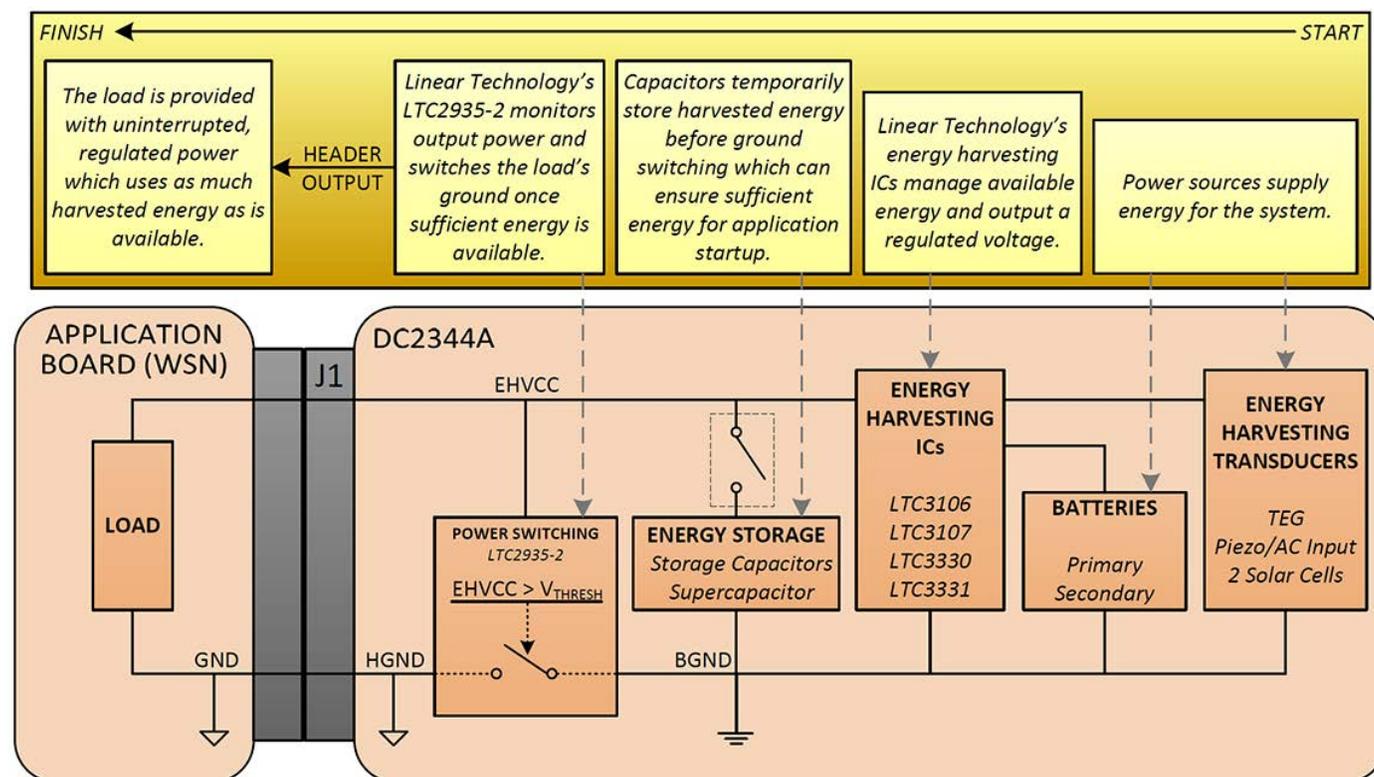
# BLOCK DIAGRAMS



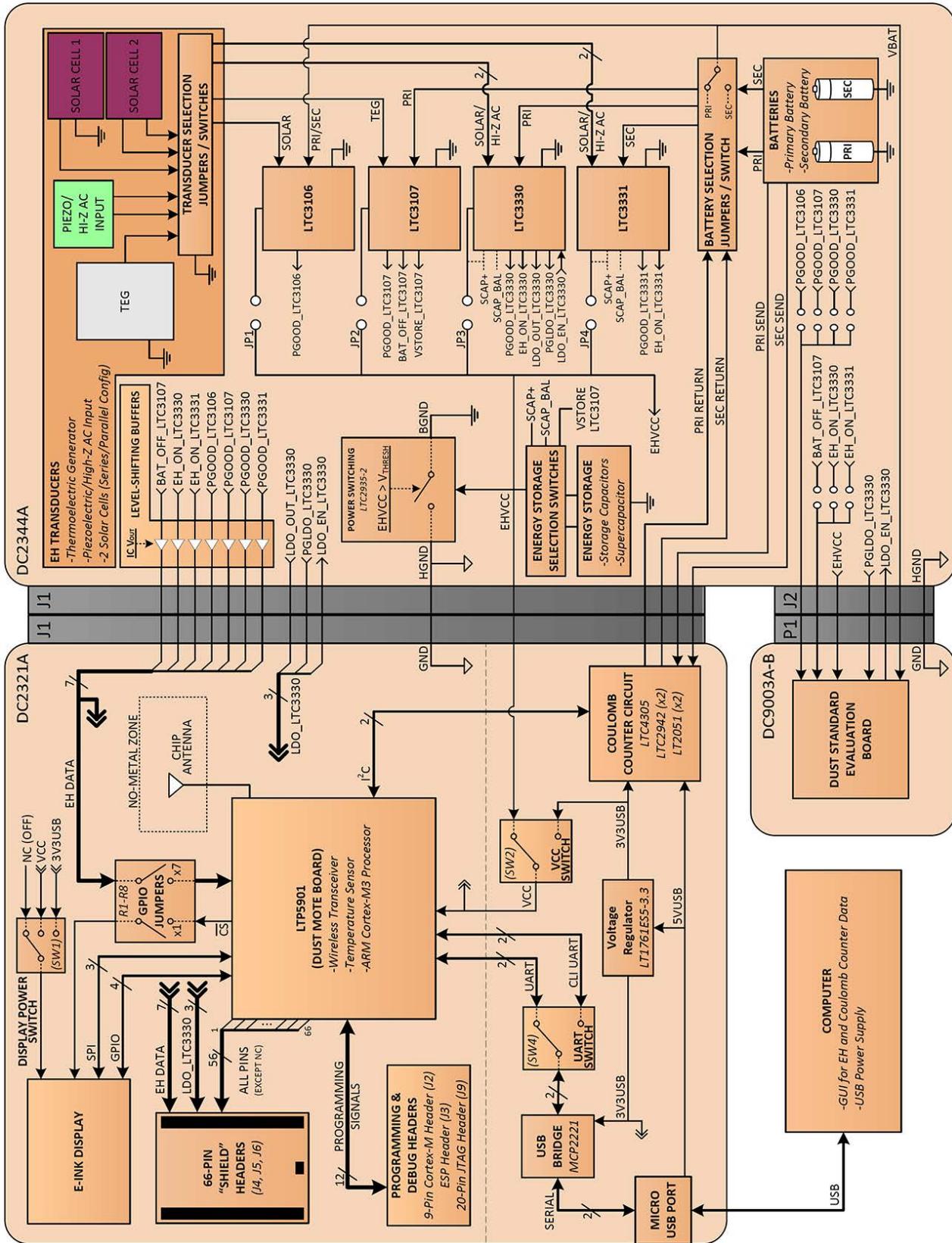Figure 7. DC2344A Simplified Block Diagram

# BLOCK DIAGRAMS



**Figure 8. DC2344A Block Diagram**

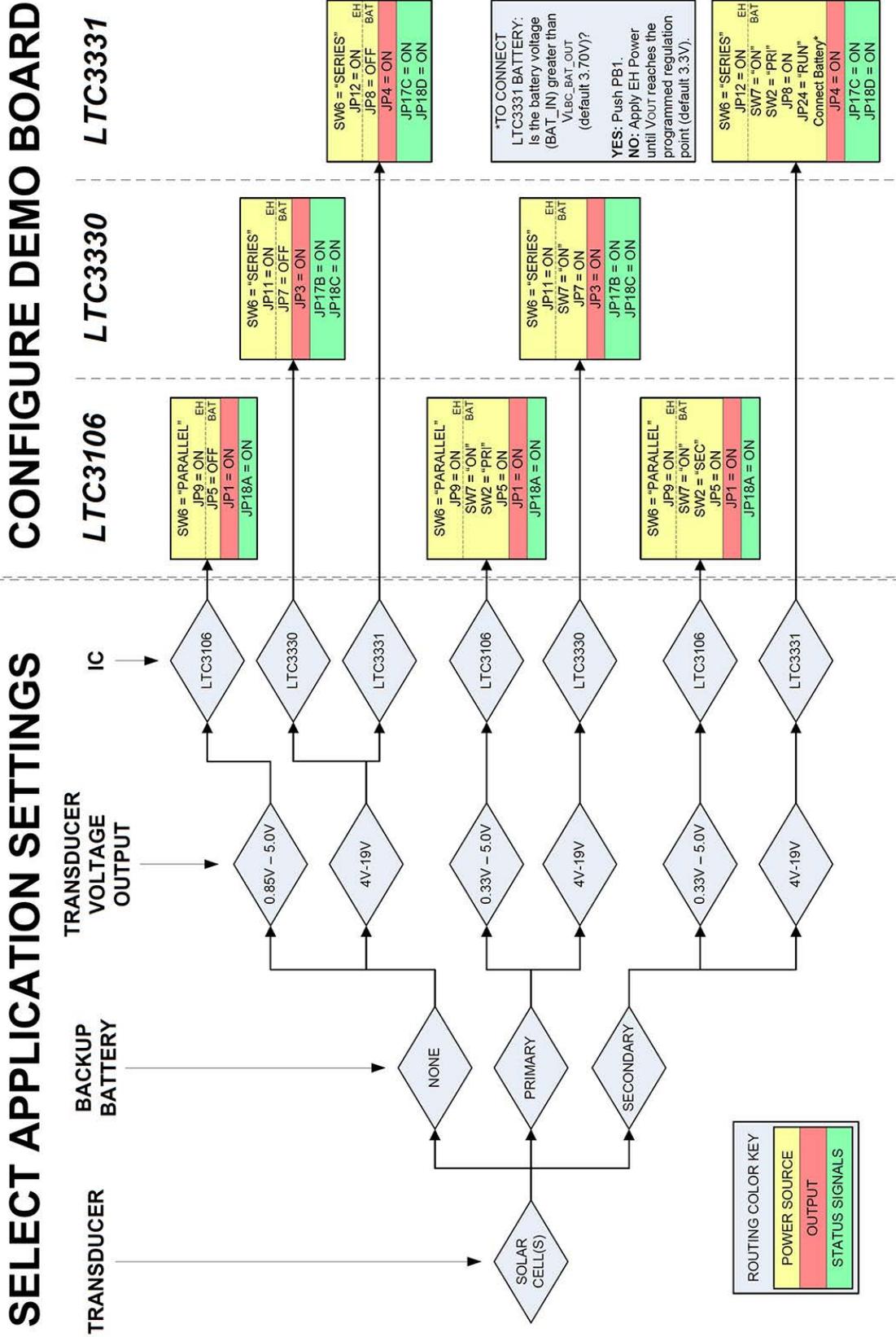dc2344afa

# SOURCE ROUTING FLOWCHARTS



Figure 9. Solar Energy Harvesting Selection and Routing Flowchart

# SOURCE ROUTING FLOWCHARTS

## THERMAL ENERGY HARVESTING

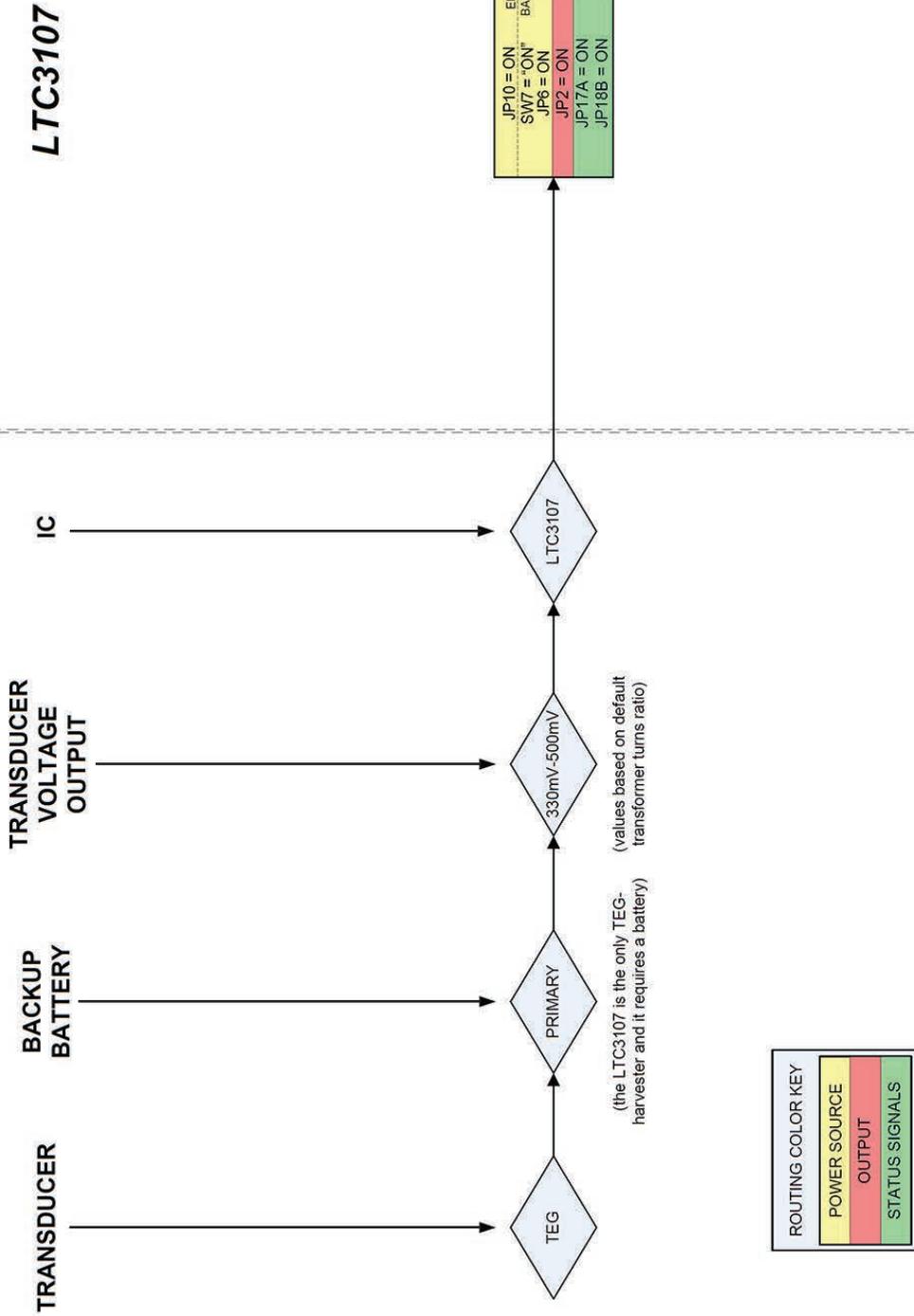### SELECT APPLICATION SETTINGS

### CONFIGURE DEMO BOARD

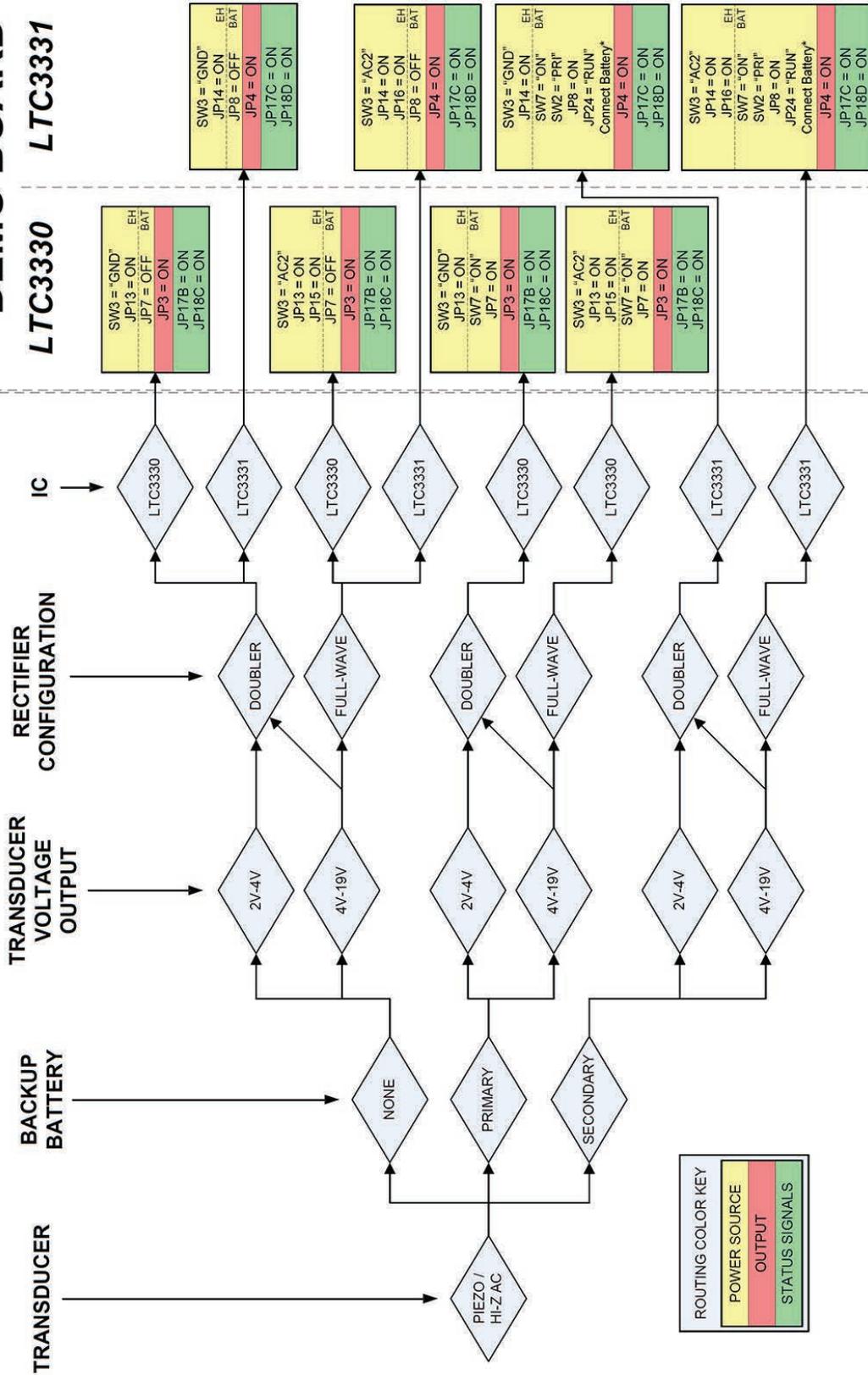LTC3107

TRANSDUCER

BACKUP BATTERY

TRANSDUCER VOLTAGE OUTPUT

IC

TEG

PRIMARY

(the LTC3107 is the only TEG-harvester and it requires a battery)

330mV-500mV

(values based on default transformer turns ratio)

LTC3107

| JP10 = ON SW7 = "ON" JP6 = ON | EH BAT |
| JP2 = ON | |
| JP17A = ON JP18B = ON | |

ROUTING COLOR KEY
POWER SOURCE
OUTPUT
STATUS SIGNALS

**Figure 10. Thermal Energy Harvesting Selection and Routing Flowchart**

dc2344afa

# SOURCE ROUTING FLOWCHARTS



Figure 11. Piezoelectric/High-Impedance AC Energy Harvesting Selection and Routing Flowchart

# POWER SOURCE ROUTING GUIDE

Table 3 shows how to route any given power source to all applicable ICs. Applying the correct configuration for each case will ensure that the output of the source is routed to the input of the IC but, in order to route the output of the IC to the board output (EHVCC), a shunt must still be installed on the appropriate output-selection jumper (JP1-JP4). In order to monitor the status outputs of the IC using the EH_ON and PGOOD turrets, the shunts on JP17 and JP18 must also be installed accordingly.

**Table 3. Power Source Routing Guide**

| POWER SOURCE TYPE | POWER SOURCE | DESTINATION | CONFIGURATION | NOTES |
|---|---|---|---|---|
| Energy-Harvesting Transducer | Solar Panel | LTC3106 | SW6 = "PARALLEL" JP9 = ON | – |
| | | LTC3330 | SW6 = "SERIES" JP11 = ON | – |
| | | LTC3331 | SW6 = "SERIES" JP12 = ON | – |
| | Piezo/AC (Voltage Doubler) | LTC3330 | SW3 = "GND" JP13 = ON | If SW3 = GND, Then One Side of the AC Source Is Grounded and Energy Is Harvested in Voltage-Doubler Configuration |
| | | LTC3331 | SW3 = "GND" JP14 = ON | |
| | Piezo/AC (Full-Wave Rectifier) | LTC3330 | SW3 = "AC2" JP13 = ON JP15 = ON | If SW3 = "AC2", Then AC2 Serves as a Second Rectified Input and Energy Is Harvested in Full-Wave Rectifier Configuration |
| | | LTC3331 | SW3 = "AC2" JP14 = ON JP16 = ON | |
| | TEG | LTC3107 | JP10 = ON | – |
| Battery | Primary Battery | LTC3106 | SW7 = "ON" SW2 = "PRI" JP5 = ON | The Primary Battery Can Power Multiple ICs Simultaneously |
| | | LTC3107 | SW7 = "ON" JP6 = ON | |
| | | LTC3330 | SW7 = "ON" JP7 = ON | |
| | Secondary Battery | LTC3106 | SW7 = "ON" SW2 = "SEC" JP5 = ON | The Secondary Battery Can Only Power One IC at a Time. Using SW2, It Can Be Connected to Either the LTC3106 or the LTC3331 |
| | | LTC3331 | SW7 = "ON" SW2 = "PRI" JP8 = ON JP19 = "RUN" Push PB1 or Apply EH* | *To Connect Using PB1 or EH, the Battery Voltage Must Be Above the PB1 or EH Threshold, Respectively (Listed in Table 13). The Default Thresholds Are 3.7V for PB1 and 3.03V for EH |

# APPLICATION

**Jumper Functions**

**JP1:** Power selection jumper used to route the LTC3106 output to the load.

**JP2:** Power selection jumper used to route the LTC3107 output to the load.

**JP3:** Power selection jumper used to route the LTC3330 output to the load.

**JP4:** Power selection jumper used to route the LTC3331 output to the load.

**JP5:** Battery selection jumper used to route the selected battery to $V_{STORE}$ on the LTC3106. The LTC3106 is compatible with both primary and secondary batteries. SW2 is used to choose which battery is active. If the secondary battery is chosen to power the LTC3106, the LTC3331 cannot be powered by any battery. However, if the primary battery is chosen to power the LTC3106, the LTC3331 can be powered by the secondary battery.

**JP6:** Battery selection jumper used to route the primary battery to $V_{BAT}$ on the LTC3107.

**JP7:** Battery selection jumper used to route the primary battery to BAT on the LTC3330.

**JP8:** Battery selection jumper used to route the secondary battery to BAT_IN on the LTC3331. Note that if SW2 is set to connect the secondary battery to the LTC3106, the secondary battery cannot be connected to the LTC3331.

**JP9:** Transducer selection jumper used to route the solar cells (in parallel) to $V_{IN}$ on the LTC3106. SW6 should be set to "PARALLEL" when JP9 is installed.

**JP10:** Transducer selection jumper used to route the TEG's harvested energy to the transformer's input for the LTC3107.

**JP11:** Transducer selection jumper used to route harvested energy from the solar cells (in series) to AC2 on the LTC3330. SW6 must be set to "SERIES" when JP11 is installed.

**JP12:** Transducer selection jumper used to route harvested energy from the solar cells (in series) to AC2 on the LTC3331. SW6 must be set to "SERIES" when JP12 is installed.

**JP13:** Transducer selection jumper used to route from the PMDM device or alternate high-impedance AC source to AC1 on the LTC3330. With SW3 in the "GND" position, the rectification will be in doubler mode.

**JP14:** Transducer selection jumper used to route from the PMDM device or alternate high-impedance AC source to AC1 on the LTC3331. With SW3 in the "GND" position, the rectification will be in doubler mode.

**JP15:** Transducer selection jumper used to route the PMDM device or alternate high-impedance AC source to AC2 on the LTC3330. SW3 must be in the "AC2" position in order to use JP15 & JP16. This enables a full-wave rectifier configuration between the LTC3330's AC1 and AC2 inputs.

**JP16:** Transducer selection jumper used to route the PMDM device or alternate high-impedance AC source to AC2 on the LTC3331. SW3 must be in the "AC2" position in order to use JP15 & JP16. This enables a full-wave rectifier configuration between the LTC3331's AC1 and AC2 inputs.

**JP17A:** Routes the LTC3107 BAT_OFF signal to the EH_ON turret and the Dust Header EH_ON output.

**JP17B:** Routes the LTC3330 EH_ON signal to the EH_ON turret and the Dust Header EH_ON output.

**JP17C:** Routes the LTC3331 EH_ON signal to the EH_ON turret and the Dust Header EH_ON output.

**JP18A:** Routes the LTC3106 PGOOD signal to the PGOOD turret and the dust header.

**JP18B:** Routes the LTC2935-2 PGOOD signal to the PGOOD turret and the dust header. The LTC3017 does not inherently generate its own PGOOD signal, so an LTC2935-2 monitors its output to create a PGOOD signal.

# APPLICATION

**JP18C:** Routes the LTC3330 PGOOD signal to the PGOOD turret and the dust header.

**JP18D:** Routes the LTC3331 PGOOD signal to the PGOOD turret and the dust header.

**JP19:** Selects the battery storage mode for the secondary battery connected to the LTC3331. In SHIP mode, the battery disconnect switch is forced off to ensure there is no drain on the battery. For operation with the secondary battery, RUN mode must be enabled.

**JP20:** Selects the charging mode for the secondary battery connected to the LTC3331. The charger can be set to OFF (battery life-extension only), CHRG for a slow charge, or FAST CHRG for a faster charge using the LTC3331's external charging circuitry.

**JP21A-JP21C:** Storage for unused jumpers.

**Table 4. Jumper Functions**

| GROUP | | INDIVIDUAL | | |
|---|---|---|---|---|
| REFERENCE | FUNCTION | REFERENCE | FUNCTION | CONDITIONS/NOTES |
| JP1-JP4 | Route IC Output to Board Output (EHVCC) and Header | JP1 | Send $V_{OUT}$ from LTC3106 to Output and Header. | – |
| | | JP2 | Send $V_{OUT}$ from LTC3107 to Output and Header. | |
| | | JP3 | Send $V_{OUT}$ from LTC3330 to Output and Header. | |
| | | JP4 | Send $V_{OUT}$ from LTC3331 to Output and Header. | |
| JP5-JP8 | Connect ICs to Their Respective Batteries | JP5 | Power LTC3106 from Currently Selected Battery | SW2 Selects Battery |
| | | JP6 | Power LTC3107 from Primary Battery | – |
| | | JP7 | Power LTC3330 from Primary Battery | |
| | | JP8 | Power LTC3331 from Secondary Battery | SW2 Must Be Set to "PRI" |
| JP9-JP16 | Connect Transducers to Desired Energy-Harvesting ICs | JP9 | Connect Solar Power Source to LTC3106 | SW6 Must Be Set to "PARALLEL" |
| | | JP10 | Connect TEG Power Source to LTC3107 | – |
| | | JP11 | Connect Solar Power Source to AC2 on LTC3330 | SW6 Must Be Set to "SERIES" |
| | | JP12 | Connect Solar Power Source to AC2 on LTC3331 | |
| | | JP13 | Connect Piezoelectric/AC Source to AC1 on LTC3330 | – |
| | | JP14 | Connect Piezoelectric/AC Source to AC1 on LTC3331 | |
| | | JP15 | Connect Piezoelectric/AC Source to AC2 on LTC3330 | SW3 Must Be Set to "AC2" to Route Power to AC2 |
| | | JP16 | Connect Piezoelectric/AC Source to AC2 on LTC3331 | |
| JP17 | Route EH_ON Signal to Turret and Dust Header | JP17A | Connect LTC3107 BAT_OFF Signal to EH_ON Turret and dust header | – |
| | | JP17B | Connect LTC3330 EH_ON Signal to EH_ON Turret and Dust Header | |
| | | JP17C | Connect LTC3331 EH_ON Signal to EH_ON Turret and Dust Header | |
| JP18 | Route PGOOD Signal to Turret and Dust Header | JP18A | Connect LTC3106 PGOOD Signal to PGOOD Turret and Dust Header | – |
| | | JP18B | Connect LTC2935-2 PGOOD Signal to PGOOD Turret and Dust Header | |
| | | JP18C | Connect LTC3330 PGOOD Signal to PGOOD Turret and Dust Header | |
| | | JP18D | Connect LTC3331 PGOOD Signal to PGOOD Turret and Dust Header | |
| JP19-JP20 | LTC3331 Operation | JP19 | Toggle "Ship" Mode to Avoid Draining Battery When Not in Use | – |
| | | JP20 | Enable Charging or Fast Charging of the Secondary Battery | |
| JP21 | Jumper Storage | – | Store Unused Jumpers | – |

# APPLICATION

### Switch Functions

**SW1:** Connects the ten optional energy storage ceramic capacitors directly to EHVCC or $V_{STORE}$ on the LTC3107. These capacitors can provide short-term power to the system in the event the load has intermittent energy requirements. These capacitors can also be disconnected entirely.

**SW2:** Selects between the primary and secondary batteries for the LTC3106 and connects the same battery to $V_{BAT}$ on the Dust header (J2). Due to charging capabilities, only one IC can use the secondary battery at any time. Therefore, while the LTC3106 is connected to the secondary battery, the LTC3331 cannot receive battery power. With the switch in its default position, all of the energy-harvesting ICs have the potential to be powered by a battery.

**SW3:** Selects the input mode for the piezoelectric or high-impedance AC energy harvesting source. In the "GND" position, one side of the source is grounded which creates a voltage-doubler configuration for the AC1 inputs of the LTC3330 and LTC3331. When SW3 is in the "AC2" position

and the appropriate jumper is installed (JP15 or JP16), the piezoelectric/AC source will be full-wave rectified across inputs AC1 and AC2.

**SW4:** Connects the supercapacitor storage to either the LTC3330 or the LTC3331.

**SW5:** Configures the terminal block input for use with either a capacitive or non-capacitive high-impedance AC or DC source. In PMDM mode, a capacitor is placed in series with the energy harvesting source for maximum peak-to-peak input with certain AC devices.

**SW6:** Configures the solar cells as either series or parallel. For use with the LTC3106, the solar cells should be in parallel; for the LTC3330 and LTC3331 the solar cells should be in series.

**SW7:** Connects/disconnects both the primary and secondary batteries from the board. In the "CCTR" position, batteries are routed through the coulomb counters on DC2321A for monitoring. Connected batteries must be routed to ICs using JP5-JP8.

**Table 4. Jumper Functions**

| REFERENCE | NAME | FUNCTION | POSITION | | RESULT | NOTES |
|---|---|---|---|---|---|---|
| SW1 | ENERGY STORAGE | Select Mode for Optional Energy Storage | 0 | OFF | Optional Energy Storage Disabled | – |
| | | | 1 | EHVCC | Any $V_{OUT}$ Routed to the Header Uses Optional Energy Storage | |
| | | | 2 | VSTORE_LTC3107 | LTC3107's $V_{STORE}$ Function Uses Optional Energy Storage | |
| SW2 | LTC3106 BATTERY | Select Between Batteries for LTC3106 | 0 | PRI | LTC3106 Uses Primary Battery, LTC3331 Uses Secondary | Battery Must Still Be Routed with Jumper |
| | | | 1 | SEC | LTC3106 Uses Secondary Battery, LTC3331 Uses No Battery | |
| SW3 | PIEZO PZ2 | Select Input Configuration for Piezo/AC Sources | 0 | GND | Piezoelectric/AC Sources Have Their PZ2 Input Grounded for Voltage Doubler Configuration | JP15 & JP16 Route the Enabled Signal to AC2 on LTC3330 & LTC3331 |
| | | | 1 | AC2 | Piezoelectric/AC Sources Can Be Routed to AC2 for Full Wave Rectification Configuration Across AC1 and AC2 | |
| SW4 | SUPERCAP BALANCER | Connect the Supercapacitor to the Output of an IC | 0 | OFF | Supercapacitor Balancer and Storage Disabled | R96-R98 Must Be Populated for Active Balancing |
| | | | 1 | LTC3330 | LTC3330's Supercapacitor Storage Enabled | |
| | | | 2 | LTC3331 | LTC3331's Supercapacitor Storage Enabled | |
| SW5 | AC SOURCE | Select Between PMDM Input and General AC Input | 0 | PMDM | PMDM Configuration Is Selected by Placing a Capacitor in Series with the Transducer's Output to AC1 | – |
| | | | 1 | HI-Z AC | Alternate High-Impedance AC Sources Can Be Routed to ICs | – |
| SW6 | SOLAR CELL CONFIG | Select Between Series/Parallel Solar Cell Orientations | 0 | PARALLEL | The Solar Cells Are Configured in Parallel | Use with LTC3106 |
| | | | 1 | SERIES | The Solar Cells Are Configured in Series | Use with LTC3330 & LTC3331 |
| SW7 | BATTERIES | Connect/ Disconnect Batteries | 0 | OFF | Both Batteries Are Disconnected from the Board | JP5-JP8 Route Batteries to ICs |
| | | | 1 | ON | Both Batteries Are Connected to the Board | |
| | | | 2 | CCTR | Both Batteries Are Routed Through Coulomb Counters on DC2321A | |

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# APPLICATION

### Turret Functions

**EHVCC (E1, E2):** Regulated output of all the active energy harvester power management circuits, referenced to BGND. When EHVCC is referenced to HGND it is a switched output that is passed through header J1 to power the load.

**BGND (E3, E4, E10, E12):** This is the board ground: the ground reference for the DC2344A. BGND is the reference for all of the parts on the board except the headers. BGND and HGND (the header ground) are connected through Q3 when the EHVCC voltage with respect to BGND reaches the rising reset threshold of the LTC2935-2 and disconnected when EHVCC falls to the falling reset threshold.

**HGND (E5, E6):** This is the header ground: the ground reference for any load that is connected to the DC2344A through one of its output headers. HGND is the switched ground that ensures the load is presented with a quickly rising voltage. BGND and HGND are connected through Q3 when the EHVCC voltage with respect to BGND reaches the rising reset threshold of the LTC2935-2 and disconnected when EHVCC falls to the falling reset threshold (thresholds configurable with R78-R86). The board is configured from the factory to connect BGND and HGND when EHVCC reaches a rising threshold of 2.85V and disconnect them when EHVCC drops below 2.25V.

**EH_ON (E7):** Energy harvesting on output signal of the IC selected using JP17. A high EH_ON signal is generally an indication that the IC is relying on harvested energy rather than battery energy. The LTC3107's equivalent signal (BAT_OFF) goes high when the battery is not in use. For the LTC3330 and LTC3331, EH_ON is high when the buck switching regulator is in use (EH input) and it is low when the buck-boost switching regulator is in use (battery input). The LTC3106 does not output an EH_ON signal.

**PGOOD (E8):** Power good output of the IC selected using jP18. PGOOD transitioning high indicates that regulation has been reached on $V_{OUT}$. Specific operation depends on which IC is generating the signal. For the universal PGOOD signal that is generated by the LTC2935-2, the rising threshold is 2.85V and the falling threshold is 2.25V. The universal PGOOD signal will switch for any of the EH ICs and can be routed to the turret by installing JP18B.

**VIN_LTC3106 [330mV-5.0V] (E9):** External energy harvester input to the LTC3106.

**VIN_LTC3107 [30mV-500mV] (E11):** External energy harvester input to the LTC3107.

**AC1_LTC3330 [4V – 19V] (E13):** External energy harvester input to AC1 on the LTC3330.

**AC2_LTC3330 [4V – 19V] (E14):** External energy harvester input to AC2 on the LTC3330.

**AC1_LTC3331 [4V – 19V] (E15):** External energy harvester input to AC1 on the LTC3331.

**AC2_LTC3331 [4V – 19V] (E16):** External energy harvester input to AC2 on the LTC3331.

**LDO_IN (E17):** Input voltage for the LDO regulator of the LTC3330. Populating R99 will connect LDO_IN to VOUT_LTC3330.

**LDO_EN (E18):** Active-high LDO enable input. The high logic level for this input is referenced to LDO_IN.

**LDO_OUT (E19):** Regulated LDO output for the LTC3330. The output voltage can be configured using R26-R31.

# APPLICATION

## LTC3106: Solar Energy Harvester with Primary or Secondary Batteries

The LTC3106 solar powered energy harvester's output (VOUT_LTC3106) can be routed to EHVCC by installing the power selection jumper JP1. The PGOOD_LTC3106 signal can be routed to the PGOOD turret by installing JP18A. The LTC3106 does not output an EH_ON indication.

SW2 toggles between the primary or secondary batteries as the backup power source for the LTC3106, and JP5 connects the selected battery to the IC's $V_{STORE}$ input. Because the LTC3106 requires a logic signal to its PRI pin in order to determine which battery is attached and enable/disable charging, SW2 also routes the appropriate signal to the IC.

Solar power will be sent to $V_{IN}$ if JP9 is installed. Solar cells should be in a parallel configuration for use with the LTC3106. This function is controlled by SW6.

The operation of the LTC3106 is configurable using 0Ω resistors as jumpers. These resistors are located in tables on the back of the board. Table 17 is a guide for these resistors and describes each of their functions.

The LTC3106 has the option to enable an undervoltage threshold for LDO regulation. This threshold can be set using the voltage divider formed by R1 and R2 on the bottom of the board. In order to optimize the power drawn from a solar cell, this voltage divider should be configured so that the voltage on the RUN pin is near the maximum power point of the cell. Because the voltage feeding the resistor divider, $V_{IN}$, is subject to fluctuate with light levels, the voltage on the RUN pin will not be the same for all intensities of light. This feature can be enabled/disabled by installing R3 or R4 respectively.

As another option to optimize the LTC3106's operation with a specific solar cell, the board allows programming of the MPPC comparator's activation point using R18. This feature can be disabled/enabled by installing R16 or R17 respectively; when MPPC is enabled, the RUN pin's UVLO function should be disabled using R3/R4 (see Table 17). The MPP pin sources a nominal current of 1.5µA, so the resistor value can be calculated for a specific solar cell's VMP using:

$$R18 = \frac{V_{MP}}{1.5\mu A}$$



**Figure 12. Schematic of LTC3106 Solar Energy Harvesting Power Supply**

# APPLICATION

**LTC3107: TEG Energy Harvester with Primary Battery**

The LTC3107 TEG powered energy harvester's output (VOUT_LTC3107) can be routed to EHVCC by installing the power selection jumper JP2. Because the LTC3107 does not output its own PGOOD signal, an additional LTC2935-2 generates a PGOOD signal based on the output voltage of the IC. This PGOOD_LTC3107 signal can be routed to the PGOOD turret by installing Jumper JP18B. The LTC3107's BAT_OFF signal can be routed to the EH_ON turret by installing JP17A.

Unlike the other ICs, the LTC3107 requires a battery to start up and adapts its output to match the voltage of its battery. With no harvested energy available, $V_{OUT}$ will be regulated to a voltage about 230mV below the battery. While harvesting energy, the LTC3107 preserves the life of its battery and regulates its output to about 30mV below the battery voltage.

Power harvested from the thermoelectric generator will be sent to $V_{IN}$ (the input of the transformer) if JP10 is installed.

When SW1 is in the "VSTORE_LTC3107" position, the optional energy storage capacitors (CO1-CO10) are connected to the LTC3107's $V_{STORE}$ input to store excess harvested energy and further extend the primary battery's life.

When SW7 is "ON" and JP6 is installed, the primary battery is routed to the LTC3107's $V_{BAT}$ input. As a result of the output's dependence on the battery voltage, the primary battery needs to operate at a minimum voltage in order for HGND switching to occur. For correct operation, the primary battery must have a voltage of at least:

$$VPRI > VRISING + 230mV$$

For the LTC2935-2's default rising threshold of 2.85V,

$$VPRI > 2.85V + 230mV = 3.08V$$

If the primary battery's voltage drops below 3.08V, it should be replaced or used exclusively with other ICs. Alternatively, a backup source with a higher voltage can be used or the rising threshold of the LTC2935-2 can be lowered to accommodate the LTC3107's battery-dependent output voltage level (the resistor configuration for this lower threshold is given in Table 6). The default rising threshold is configured to allow the LTC3107's output to switch HGND but, if the LTC3107 is not being evaluated, a higher rising threshold can be used and will result in a wider hysteresis window for the other EH ICs.
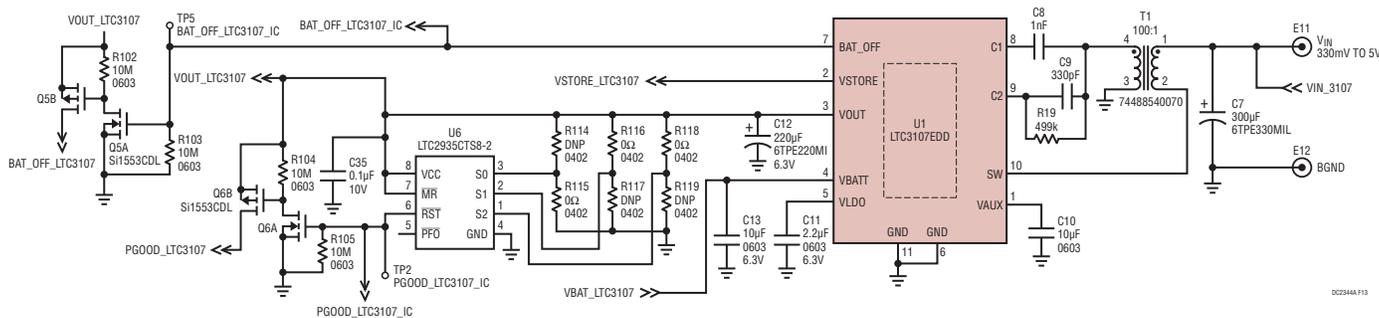


**Figure 13. Schematic of LTC3107 TEG Energy Harvesting Power Supply**

# APPLICATION

## LTC3330: High-Z AC, Piezoelectric, & Solar Energy Harvester with Primary Battery

The LTC3330 Hi-Z AC/piezoelectric/solar powered energy harvester's output (VOUT_LTC3330) can be routed to EHVCC by installing the power selection jumper JP3. The PGOOD_LTC3330 signal can be routed to the PGOOD turret by installing JP18C. EH_ON_LTC3330 can be routed to the EH_ON turret by installing JP17B.

Power harvested from the solar cells can be routed to the LTC3330's AC2 input by installing JP11. In order for this voltage to be within the default UVLO window, the solar cells must be configured in series by SW6.

An external piezoelectric or other high-impedence AC source can be routed to the LTC3330's AC1 input through J3 if JP13 is installed. If SW3 is in the "GND" position, one side of the source is grounded which creates a voltage-doubler configuration. If SW3 is in the "AC2" position

and JP15 is installed, the piezoelectric/AC source can be full-wave rectified across inputs AC1 and AC2. See Figure 22 for a visual of this configuration.

When SW7 is "ON" and JP7 is installed, the primary battery is routed to the LTC3330.

The LTC3330 has a configurable LDO regulator which can be set to different output voltages by moving R26-R31. Three turrets (LDO_IN, LDO_EN, and LDO_OUT) are available to access the inputs and outputs of the LDO. LDO_IN can be pulled to the LTC3330's output, VOUT_LTC3330, by installing R99. The regulator is enabled by pulling LDO_EN high with reference to LDO_IN.

If the application would benefit from a wider PGOOD hysteresis window than the LTC3330 provides, the PGOOD_LTC2935-2 signal can be used in place of any of the PGOOD signals generated by the harvester circuits.
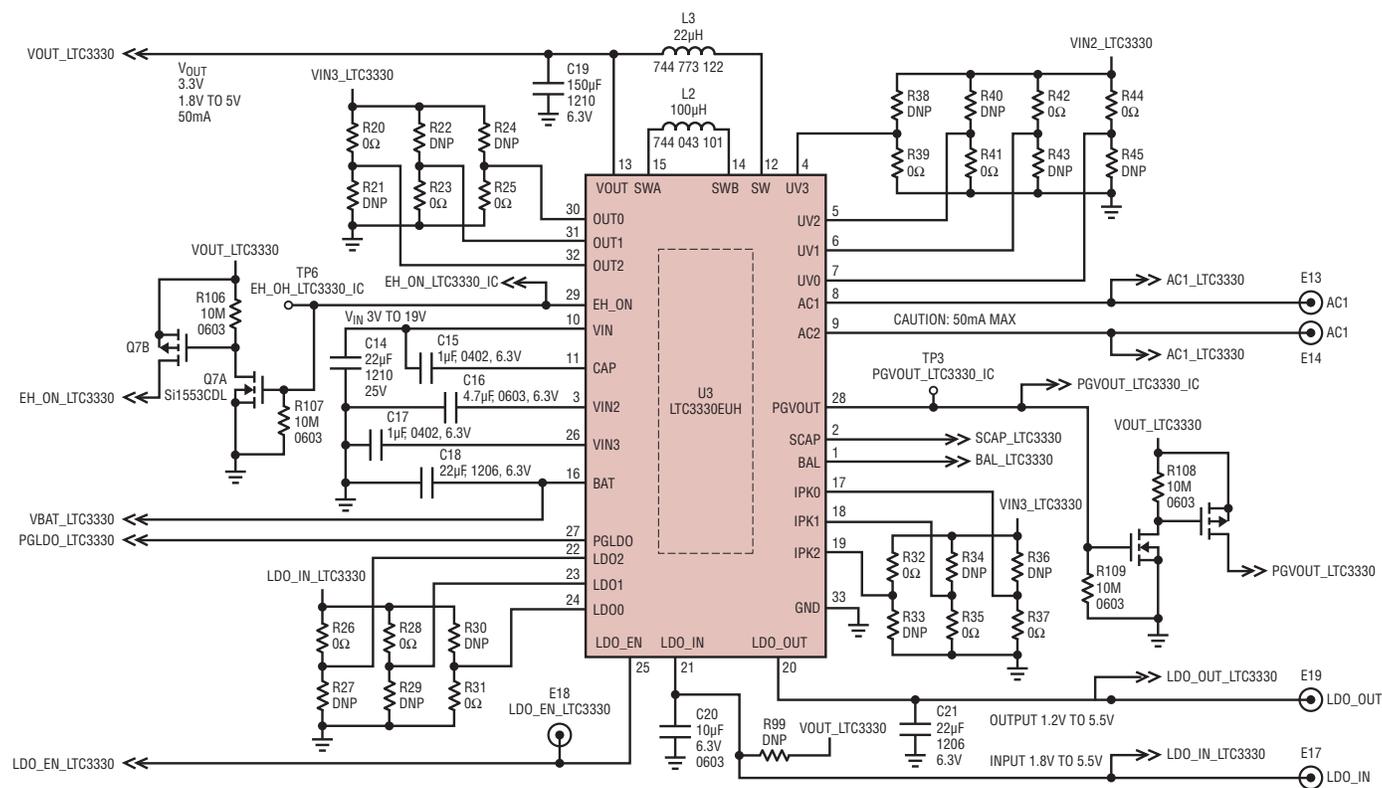


**Figure 14. Schematic of LTC3330 Hi-Z AC, Piezoelectric, & Solar Energy Harvesting Power Supply**

# APPLICATION

**LTC3331: Hi-Z AC, Piezoelectric, & Solar Energy Harvester with Secondary Battery**

The LTC3331 Hi-Z AC/piezoelectric/solar powered energy harvester's output (VOUT_LTC3331) can be routed to EHVCC by installing the power selection jumper JP4. The PGOOD_LTC3331 signal can be routed to the PGOOD turret by installing Jumper JP18D. EH_ON_LTC3331 can be routed to the EH_ON turret by installing JP17C.

Power harvested from the solar cells can be routed to the LTC3331's AC2 input by installing JP12. In order for this voltage to be within the default UVLO window, the solar cells must be configured in series by SW6.

An external piezoelectric (or other high-impedence AC) source can be routed to the LTC3331's AC1 input through J3 if JP14 is installed. If SW3 is in the "GND" position, one side of the source is grounded which creates a voltage-doubler configuration. If SW3 is in the "AC2" position

and JP16 is installed, the piezoelectric/AC source will be full-wave rectified across inputs AC1 and AC2. See Figure 22 for a visual of this configuration.

The operation of the LTC3331 is configurable using JP19 & JP20. Charging of the secondary battery is configurable using JP20. In its "OFF" position, there will be no current sourced to the battery. In the "CHARGE" position, the battery is charged through resistor R76. For higher charging currents up to 10 mA, JP20 should be placed in the "FAST CHG" position. In this mode, the battery is charged using external circuitry connected to the LTC3331 and the battery charge current can be set based on the value of R72.

A "SHIP" mode is provided which manually disconnects the battery. This may be helpful for preventing discharge of the battery when no harvestable energy is available for long periods of time such as during shipping. To disengage "SHIP" mode, JP19 should be installed in the "RUN" position.
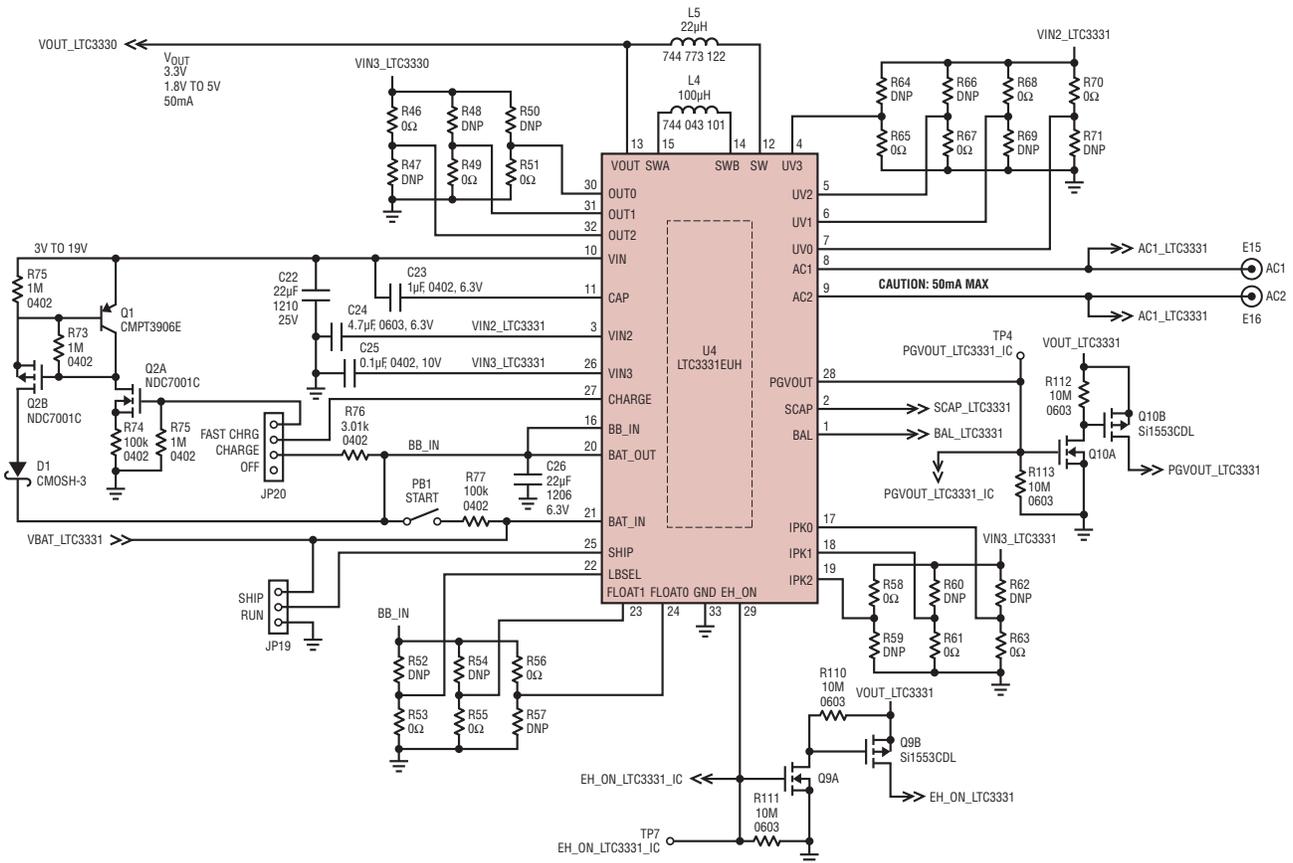


**Figure 15. Schematic of LTC3331 Hi-Z AC, Piezoelectric, & Solar Energy Harvesting Power Supply**

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# APPLICATION

When SW7 is "ON" and JP8 is installed, the secondary battery is routed to the LTC3331's BAT_IN pin. To connect the battery internally, JP19 must be set to "RUN" and the BB_IN pin needs to be brought above the BAT_OUT connect threshold. There are two ways this can be achieved:

1. The IC has reached regulation using EH power and the battery voltage is greater than the BAT_IN connect threshold voltage ("EH" column in Table 13).

2. The battery voltage is greater than the BAT_OUT connect threshold voltage ("PB1" column in Table 13) and tactile switch PB1 is pressed momentarily.

By default, the BAT_IN connect threshold is set to 3.03V and the BAT_OUT connect threshold is set to 3.70V. These thresholds (along with the battery disconnect and float voltages) can be adjusted using R52-R57. Note that the PB1 function does not work for settings where the BAT_OUT threshold is greater than the float voltage.

If the application would benefit from a wider PGOOD hysteresis window than the LTC3331 provides, the PGOOD_LTC2935-2 signal can be used in place of any of the PGOOD signals generated by the harvester circuits.

## LTC2935-2 Power Switch Circuit

If the application requires a wide hysteresis window for the PGOOD signal, the board has the ability to use an independent PGOOD signal which is generated by the LTC2935-2 and available on JP18B. This signal acts as the PGOOD signal for the LTC3107 circuit because the LTC3107 does not have its own PGOOD output, but the PGOOD_LTC2935-2 signal can be used in place of any of the PGOOD signals generated by the harvester circuits.

Some loads do not like to see a slowly rising input voltage. Switch Q3 ensures that EHVCC on the header is off until the energy harvested output voltage is high enough to power the load. By default, the LTC2935-2 is configured to turn on Q3 at 2.85V and turn off Q3 at 2.25V. With this switching, the load will see a fast voltage rise at startup and be able to utilize all of the energy stored in the output capacitors between the 2.85V and 2.25V levels.

The DNP and 0Ω resistors (R78-R86) near the LTC2935-2 allow for customization of the PGOOD thresholds and hysteresis window. By modifying R84-R86, the digital inputs (S0, S1, S2) can be toggled when the rising or falling threshold is reached.
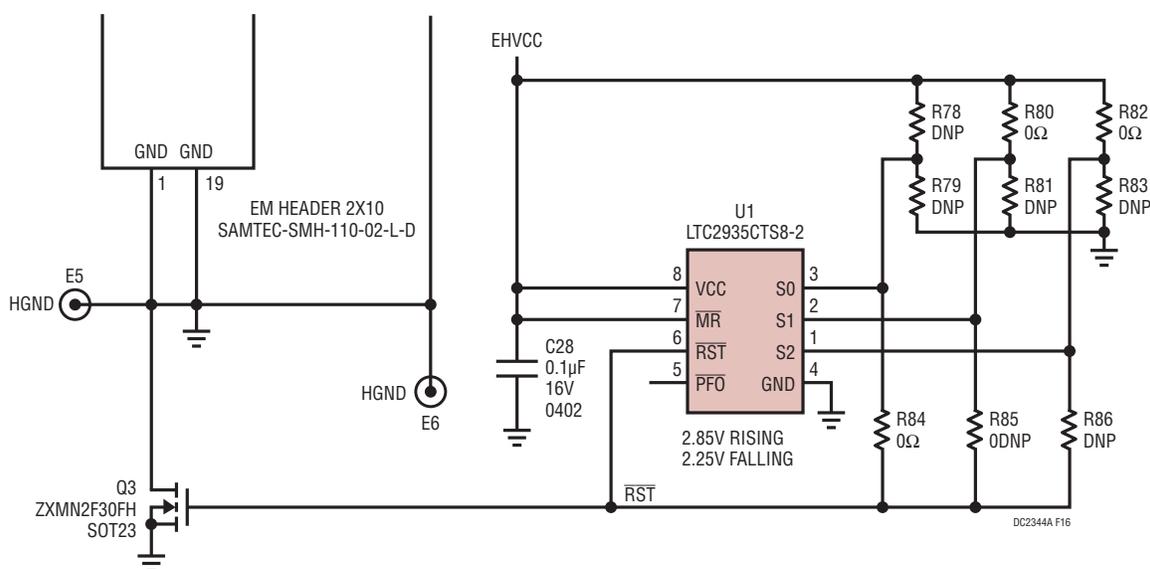


Figure 16. Schematic of LTC2935-2 Low-Power Supervisor and HGND Switching Circuit

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A hysteresis ('H') resistor acts as a '0' until the rising threshold is met, then becomes a '1'. Once the voltage drops below the falling threshold again, it becomes a '0'. In this way, the inputs of the LTC2935-2 can be reconfigured during operation to create a wider hysteresis window.

Table 6 shows a few recommended 0Ω resistor configurations that will result in the widest possible hysteresis windows for different rising threshold voltages. The best value for this threshold depends on which IC is being evaluated. The default setting allows the output voltage of any IC to switch the header ground, but the hysteresis window can be optimized to suit a particular IC output or application.

**Table 6. Possible Settings for Widest Hysteresis Windows**

| ENERGY HARVESTER BEING EVALUATED | S0 | S1 | S2 | FALLING THRESH | RISING THRESH |
|---|---|---|---|---|---|
| All | H | 1 | 1 | 2.25V | 2.85V |
| All Except LTC3107 | 1 | 1 | H | 2.25V | 3.15V |
| Only LTC3107 | H | H | 1 | 2.25V | 2.70V |

The recommendations in this table are based on the default output voltage configuration where EHVCC = 3.3V.

## Signal Buffering

Because DC2344A switches the ground on the output header once a target voltage threshold is reached, it is necessary to buffer any output signal that will come directly in contact with a processor. Without buffering, a signal that is outputting a logic low will give the load an unintended ground reference, causing it to draw power before the ground switching occurs. This happens as the result of a sneak path within the processor.

To prevent this, a simple FET buffer circuit is employed on all IC status signals which cross the output header, J1. With a high input signal, the N-channel FET is enhanced and pulls the P-channel gate low to connect the output to $V_{REF}$. With a low input signal, the N-channel FET is off and the gate of the P-channel FET is pulled high through a resistor to keep the FET off; in this state, the output is not connected to ground, but is instead a high-impedance node.
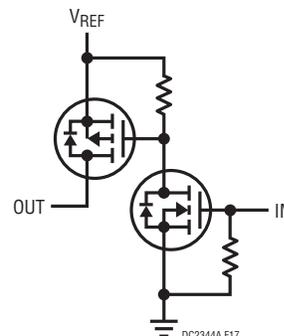


**Figure 17. Simple Signal Buffer/Level Translator Circuit**

On DC2321A, a pull-down resistor on the output of each buffer ensures that the signal is read as a logic low when the node is high-impedance. These resistors are pulled down to GND on DC2321A which is equivalent to HGND on DC2344A.

In addition to preventing sneak paths, the buffers also provide a voltage translation to $V_{REF}$. Because the LTC3330 and LTC3331 status signals output voltages referenced to internal rails rather than the regulation voltage, this voltage translation may be necessary to prevent damage to the load.

## Status Signal Selection

The LTC3107, LTC3330, and LTC3331 ICs each output a logic signal indicating when they are powering the load using harvested energy rather than a backup source. Using JP17, one of these signals can be routed to the EH_ON turret.

**Table 7. Presence of PGOOD / EH_ON Signals for Each IC**

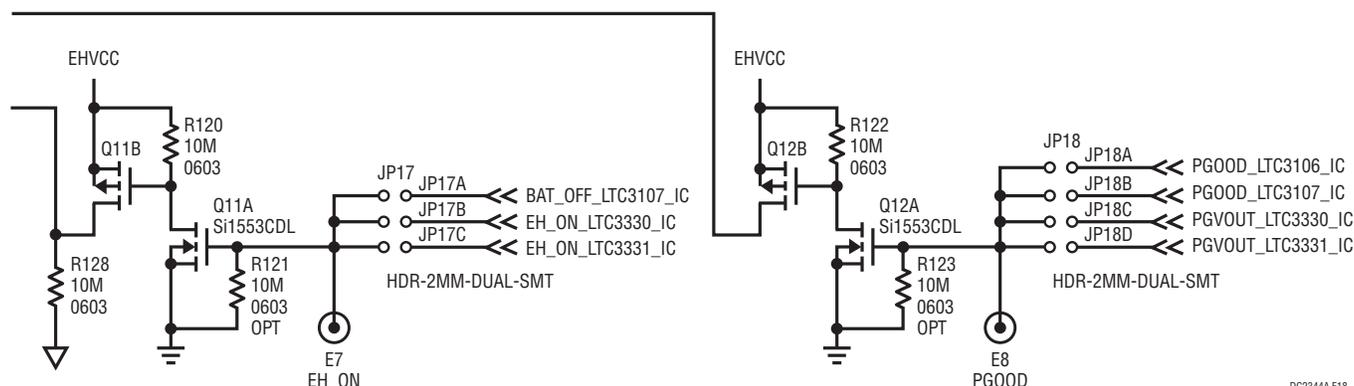| IC | EH_ON | PGOOD |
|---|---|---|
| LTC3106 | – | Yes |
| LTC3107 | Yes | Generated by LTC2935-2 |
| LTC3330 | Yes | Yes |
| LTC3331 | Yes | Yes |

# APPLICATION



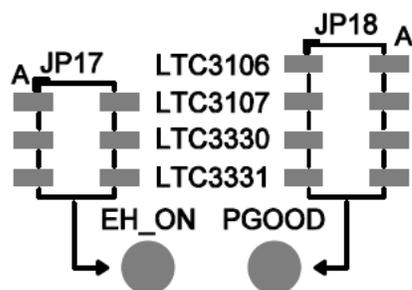**Figure 18. EH_ON and PGOOD Selection Jumpers and Turrets**



**Figure 19. Signal Selection Layout**

Similarly, the LTC3106, LTC3330, and LTC3331 ICs each output a logic signal indicating when the output ($V_{OUT}$) has reached regulation. Because the LTC3107 does not inherently generate this signal, an additional LTC2935-2 monitors its output to create its PGOOD signal. Using JP18, one of these signals can be routed to the PGOOD turret.

The name of each relevant IC is located between its appropriate EH_ON jumper and PGOOD jumper (see Figure 19). Jumper reference designators are listed on the assembly drawing.

## DC9003A Integration

Header J2 is intended for use with the DC9003A Dust manager/mote evaluation board. The EH_ON and PGOOD signals selected by JP17 and JP18 are routed through buffers to the applicable inputs on the Dust board. When the selected PGOOD signal is low, the Dust board will use power from its own on-board battery. When PGOOD is high, power is drawn from EHVCC on DC2344A.

In order to properly interface with DC2344A, R3 on DC9003A must be changed to 750Ω.

## Ceramic Capacitor Storage

The DC2344A hosts a bank of ten optional energy storage capacitors which can be configured using SW1. In the "OFF" position, the capacitors are disconnected from the rest of the circuit. If SW1 is set to "EHVCC", the capacitors are connected to the output voltage, EHVCC. If SW1 is set to "VSTORE_LTC3107", the capacitors are connected to $V_{STORE}$ on the LTC3107 and are used in the IC's own storage function.

At the default EHVCC voltage of 3.3V, the actual capacitance of each capacitor is about 80µF. This gives the storage bank a combined capacitance of about 800µF. Therefore, with the default voltage and switching threshold configurations, the ceramic capacitor bank is able to store about:

$$\text{Stored Energy}|_{V_1 - V_2} = \tfrac{1}{2} C\, V_1^2 - \tfrac{1}{2} C\, V_2^2$$

$$= \tfrac{1}{2} C\, (V_1^2 - V_2^2)$$

$$= \tfrac{1}{2} (0.0008)\, (3.3^2 - 2.25^2)$$

$$= 2.33\ \text{mJ}$$

between 3.3V and the 2.25V LTC2935-2 falling threshold.

# APPLICATION

## Supercap Storage and Active Balancer

The supercapacitor supplied with the board allows the storage of much more energy than can be stored by the bank of ceramic capacitors. At the default EHVCC voltage of 3.3V, the actual capacitance of the supercapacitor is about 13mF. Based on the above calculations, the supercapacitor is able to store 37.88 mJ between 3.3V and the 2.25V default LTC2935-2 falling threshold.

SW4 allows the supercapacitor to be disconnected or tied to the output of either the LTC3330 or the LTC3331. The supercapacitor that is populated by default does not have a balance pin and therefore does not need the active balancing feature of the LTC3330 or the LTC3331.

However, the board does allow the use of active balancing with alternate supercapacitors. In the case that the user wishes to use a supercapacitor with active balancing, C31 can be populated. This footprint is designed to fit CAP-XX supercapacitors in A-Type packages. See Table 8 for recommended parts that will fit the pads on the board.

**Table 8. Recommended Supercapacitors**

| TYPE | CAPACITANCE | PART NUMBER | MANUFACTURER |
|---|---|---|---|
| WITH BALANCE PIN | 85mF | GA209F | CAP-XX |
| | 120mF | HA202F | CAP-XX |
| | 400mF | HA230F | CAP-XX |
| WITHOUT BALANCE PIN | 4.7mF | BZ05KB472ZSB | AVX |
| | 15mF | BZ055B153ZSB | AVX |
| | 33mF | BZ055B333ZSB | AVX |

Before installing C31, be sure to place insulating tape over the specified contacts of C30; the note for doing so can be seen on the bottom assembly drawing as well as underneath C30 on the back of the board.

The active balancing feature is disabled/enabled through the installation of the 0Ω resistors R93-R98. By default, balancing is disabled and R93-R95 are installed. To enable balancing, these three resistors should be moved to R96-R98. Only one group of three resistors should be populated at a time.

## Power Selection Diodes

Diodes D4-D7 are optional components used to "Diode-OR" multiple energy harvesting sources together. When the or-ing diodes are installed, all of the power routing jumpers (JP1-JP4) should be off. The diode drop will be subtracted from the output voltage setpoint, so it is recommended to select a higher output voltage to compensate for the diode drop. When more than one of these diodes is installed and the associated energy harvester inputs are powered, the board will switch between energy harvester power circuits as needed to maintain the output voltage.

At some level of current dependent on the components used, an ideal diode IC becomes more efficient than regular diodes. At low load currents, regular diodes are more efficient because their power consumption is dependent upon the current being passed through. At higher currents, and ideal diode IC becomes more efficient because it requires only a quiescent current and power dissipation is not directly dependent on the current.

# CONFIGURATION TABLES

The following tables show how to configure some settings for the LTC2935-2, LTC3106, LTC3330, and LTC3331. Moving the supplied 0Ω jumper resistor into the appropriate '1' or '0' row will pull the appropriate pin high or low and change some functionality according to the relevant table.

All of the necessary jumper resistors for these functions are supplied with the board, so no additional parts should be needed. Do not populate both the '1' and '0' resistor in the same column for any table as this will result in a short-circuit.



*HYSTERESIS

dc2344a F20a

**Figure 20a. Front 0Ω Resistor Jumpers for Table 9**
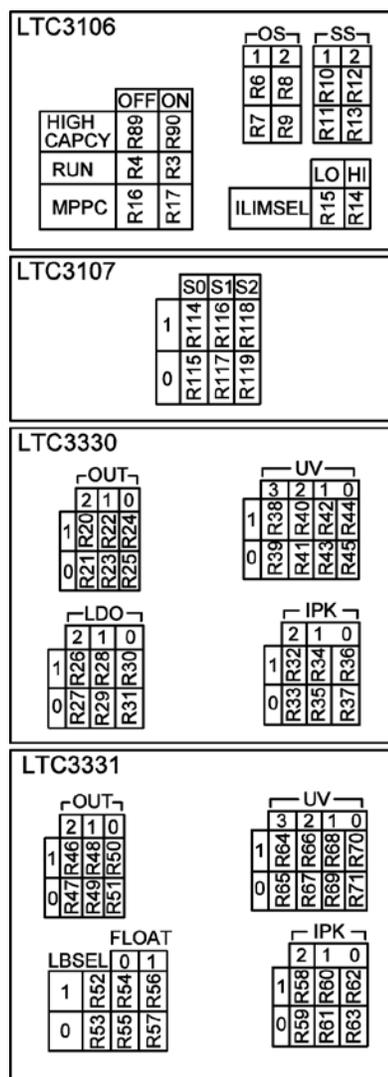


**Figure 20b. Back 0Ω Resistor Jumpers for Tables 10-16**

**LTC2935-2**

**Table 9. PGOOD Threshold Selection**

| S0 | S1 | S2 | RESET THRESH | POWER-FAIL THRESH | |
|----|----|----|--------------|-------------------|---|
| 0 | 0 | 0 | 3.30V | 3.45V | |
| 1 | 0 | 0 | 3.15V | 3.30V | |
| 1 | 1 | 0 | 3.00V | 3.15V | |
| 0 | 1 | 0 | 2.85V | 3.00V | |
| 0 | 1 | 1 | 2.70V | 2.85V | Default Rising |
| 0 | 0 | 1 | 2.55V | 2.70V | |
| 1 | 0 | 1 | 2.40V | 2.55V | |
| 1 | 1 | 1 | 2.25V | 2.40V | Default Falling |

NOTE: Shaded Rows Represent Default Configuration Settings

dc2344afa

# CONFIGURATION TABLES

**LTC3106**

**Table 10. V$_{OUT}$ Selection**

| OS1 | OS2 | V$_{OUT}$ |
|-----|-----|-----------|
| 0 | 0 | 1.8V |
| 0 | 1 | 3.0V |
| 1 | 0 | 3.3V |
| 1 | 1 | 5.0V |

**Table 11. V$_{STORE}$ Selection**

| SS1 | SS2 | V$_{STORE}$ |
|-----|-----|-------------|
| 0 | 0 | 2.07V |
| 0 | 1 | 2.9V |
| 1 | 0 | 3.015V |
| 1 | 1 | 4.0V |

**LTC3330**

**Table 12. LDO Voltage Selection**

| LDO2 | LDO1 | LDO0 | LDO_OUT |
|------|------|------|---------|
| 0 | 0 | 0 | 1.2V |
| 0 | 0 | 1 | 1.5V |
| 0 | 1 | 0 | 1.8V |
| 0 | 1 | 1 | 2.0V |
| 1 | 0 | 0 | 2.5V |
| 1 | 0 | 1 | 3.0V |
| 1 | 1 | 0 | 3.3V |
| 1 | 1 | 1 | = LDO_IN |

**LTC3331**

**Table 13. Float Selection**

| LBSEL | FLOAT1 | FLOAT0 | FLOAT | CONNECT EH | CONNECT PB1 | DISCONNECT |
|-------|--------|--------|-------|------------|-------------|------------|
| 0 | 0 | 0 | 3.45V | 2.35V | 3.02V | 2.04V |
| 0 | 0 | 1 | 4.0V | 3.03V | 3.70V | 2.70V |
| 0 | 1 | 0 | 4.1V | 3.03V | 3.70V | 2.70V |
| 0 | 1 | 1 | 4.2V | 3.03V | 3.70V | 2.70V |
| 1 | 0 | 0 | 3.45V | 2.85V | N/A | 2.51V |
| 1 | 0 | 1 | 4.0V | 3.53V | N/A | 3.20V |
| 1 | 1 | 0 | 4.1V | 3.53V | N/A | 3.20V |
| 1 | 1 | 1 | 4.2V | 3.53V | N/A | 3.20V |

**LTC3330 & LTC3331**

**Table 14. Output Voltage Selection**

| OUT2 | OUT1 | OUT0 | V$_{OUT}$ |
|------|------|------|-----------|
| 0 | 0 | 0 | 1.8V |
| 0 | 0 | 1 | 2.5V |
| 0 | 1 | 0 | 2.8V |
| 0 | 1 | 1 | 3.0V |
| 1 | 0 | 0 | 3.3V |
| 1 | 0 | 1 | 3.6V |
| 1 | 1 | 0 | 4.5V |
| 1 | 1 | 1 | 5.0V |

**Table 15. I$_{PEAK\_BB}$ Selection**

| IPK2 | IPK1 | IPK0 | I$_{LIN}$ | L$_{MIN}$ |
|------|------|------|-----------|-----------|
| 0 | 0 | 0 | 5mA | 1000µH |
| 0 | 0 | 1 | 10mA | 470µH |
| 0 | 1 | 0 | 15mA | 330µH |
| 0 | 1 | 1 | 25mA | 220µH |
| 1 | 0 | 0 | 50mA | 100µH |
| 1 | 0 | 1 | 100mA | 47µH |
| 1 | 1 | 0 | 150mA | 33µH |
| 1 | 1 | 1 | 250mA | 22µH |

**Table 16. V$_{IN}$ UVLO Threshold Selection**

| UV3 | UV2 | UV1 | UV0 | UVLO RISING | UVLO FALLING |
|-----|-----|-----|-----|-------------|--------------|
| 0 | 0 | 0 | 0 | 4V | 3V |
| 0 | 0 | 0 | 1 | 5V | 4V |
| 0 | 0 | 1 | 0 | 6V | 5V |
| 0 | 0 | 1 | 1 | 7V | 6V |
| 0 | 1 | 0 | 0 | 8V | 7V |
| 0 | 1 | 0 | 1 | 8V | 5V |
| 0 | 1 | 1 | 0 | 10V | 9V |
| 0 | 1 | 1 | 1 | 10V | 5V |
| 1 | 0 | 0 | 0 | 12V | 11V |
| 1 | 0 | 0 | 1 | 12V | 5V |
| 1 | 0 | 1 | 0 | 14V | 13V |
| 1 | 0 | 1 | 1 | 14V | 5V |
| 1 | 1 | 0 | 0 | 16V | 15V |
| 1 | 1 | 0 | 1 | 16V | 5V |
| 1 | 1 | 1 | 0 | 18V | 17V |
| 1 | 1 | 1 | 1 | 18V | 5V |

# CONFIGURATION TABLES

## 0Ω Resistor Jumper Functions

**Table 17. 0Ω Resistor Jumper Functions**

| RELEVANT PART | RESISTORS | FUNCTION | DEFAULT POSITION | DEFAULT MODE | DESCRIPTION |
|---|---|---|---|---|---|
| LTC3106 | R3, R4 | RUN Threshold ON/OFF | R3 | RUN Threshold | Enable/Disable Undervoltage Threshold Mode for $V_{IN}$ on the LTC3106. The Undervoltage Threshold Is Configurable by Changing the Values of the Resistors in the External Voltage Divider (R1 & R2) |
| | R6-R9 | Set $V_{OUT}$ | R6, R9 | $V_{OUT}$ = 3.3V | Sets Output Regulation Voltage Output. See Table 10 |
| | R10-R13 | Set $V_{STORE}$ | R10, R12 | $V_{STORE}$ = 4.0V | Sets $V_{STORE}$ Operating Voltage. See Table 11 |
| | R14, R15 | Set Peak Current Limit | R15 | Low Current Limit | Selects the Peak Current Limit for the LTC3106 by Enabling/Disabling the Automatic Power Adjust Feature. In LOW Mode, the LTC3106 Will Operate at the Lowest Peak Current and in HIGH Mode it Will Operate at Higher Peak Currents |
| | R16, R17 | MPPC OFF/ON | R16 | MPPC Disabled | Disables/Enables Maximum Power Point Control for Efficient Energy-Harvesting. The Activation Point for the MPP Comparator is Programmable Using R18. The Nominal MPPC Current is 1.2µA, so the Nominal Set Point is $V_{MPPC}$ = 1.2µA • R18 |
| | R89, R90 | Set Battery Capacity | R89 | Low Capacity Battery | Selects High/Low Battery Capacity Mode for the LTC3106. The Batteries Supplied with the Board are Considered Low-Capacity |
| LTC3330 | R20-R25 | Set $V_{OUT}$ | R20, R23, R25 | $V_{OUT}$ = 3.3V | Sets Output Regulation Voltage Output. See Table 14 |
| | R26-R31 | Set LDO Voltage | R26, R28, R31 | LDO_OUT = 3.3V | Sets Low-Dropout Regulated Voltage Output. See Table 12 |
| | R32-R37 | Set $I_{PEAK\_BB}$ | R32, R35, R37 | $I_{LIN}$ = 50mA | Sets Current Limit for the LTC3330's Buck-Boost Switching Regulator. See Table 15 |
| | R38-R45 | Set UVLO | R39, R41, R42, R44 | RISING = 7V FALLING = 6V | Sets Undervoltage Lockout Thresholds for the LTC3330's Buck Switching Regulator. See Table 16 |
| | R99 | Set LDO_IN | DNP | LDO_IN Floating (LDO Disabled) | Ties LDO_IN to VOUT_LTC3330 |
| LTC3331 | R46-R51 | Set $V_{OUT}$ | R46, R49, R51 | $V_{OUT}$ = 3.3V | Sets Output Regulation Voltage Output. See Table 14 |
| | R52-R57 | Set Float, Connect, & Disconnect | R53, R55, R56 | FLOAT = 4.0V CONNECT = 3.03V DISCONNECT = 2.70V | Selects Battery Float Voltage and Connect/Disconnect Voltage Levels. See Table 13 |
| | R58-R63 | Set $I_{PEAK\_BB}$ | R58, R61, R63 | $I_{LIN}$ = 50mA | Sets Current Limit for the LTC3331's Buck-Boost Switching Regulator. See Table 15 |
| | R64-R71 | Set UVLO | R65, R67, R68, R70 | RISING = 7V FALLING = 6V | Sets Undervoltage Lockout Thresholds for the LTC3331's Buck Switching Regulator. See Table 16 |
| LTC2935-2 | R78-R86 | Set PGOOD Thresholds | R80, R82, R84 | RISING = 2.85V FALLING = 2.25V | Sets Rising/Falling Thresholds for the LTC2935-2's Generated PGOOD Signal Which Switches HGND = BGND. NOTE: Only One "Hysteresis" Jumper (R84, R85, R86) Should be Installed at a Time. See Table 9 |
| Supercap | R93-R98 | Balance OFF/ON | R93-R95 | Active Balancing Disabled | Disables/Enables Active Balancing Using the BAL Pin of a Supercapacitor. Install R93-R95 to Disable Balancing or Install R96-R98 to Enable Balancing. Only One Group Can be Populated at Once. The Default Capacitor Does Not Allow Balancing |

# TRANSDUCERS

### Solar Cells

The DC2344A is equipped with two SC3726I-8-1 solar cells which can be configured in parallel or in series using SW6. The maximum power point of a single cell is roughly 3.3V.

The parallel configuration should be used with the LTC3106 due to its maximum voltage input rating. If SW6 is in the 'SERIES' position, the LTC3106 is still safe from overvoltage but can only be powered by a single cell. The LTC3106 operates near the maximum power point of the cells in parallel using the undervoltage threshold function on its RUN pin. This function is enabled/disabled using R3/R4 and configured using R1/R2. See Table 17 for details.

The series configuration should be used with the LTC3330 and LTC3331 due to their default UVLO settings which operate around the maximum power point of two cells stacked in series. If SW6 is in the 'PARALLEL' position, these ICs will be connected to both cells in parallel but cannot be powered in their default configuration because the input voltage will be below their default UVLO rising threshold.

DC2344A allows other solar cells to be connected using the terminal block or turrets. Table 18 lists some options for solar cells with dimensions similar to the two on-board solar cells.

**Table 18. Recommended Solar Cells**

| MPP OUTPUT(600 LUX) | | | | |
|---|---|---|---|---|
| $V_{MPP}$ (V) | $I_{MPP}$ (µA) | $P_{MPP}$ (µW) | MANUFACTURER/PART# | SUGGESTED IC |
| 3.28 | 27 | 89 | China Solar LTD, KS-3726-8 | LTC3106 (Single/Parallel) LTC3330/LTC3331 (Series) |
| 0.49 | 457 | 224 | Fujikura, FDSC-FTC6 | LTC3106 (MPP Function) |
| 1.64 | 122 | 200 | Panasonic, AM-5412CAR | LTC3106 (RUN Function) |

**KS-3726-8 Characteristics (Single Cell)**
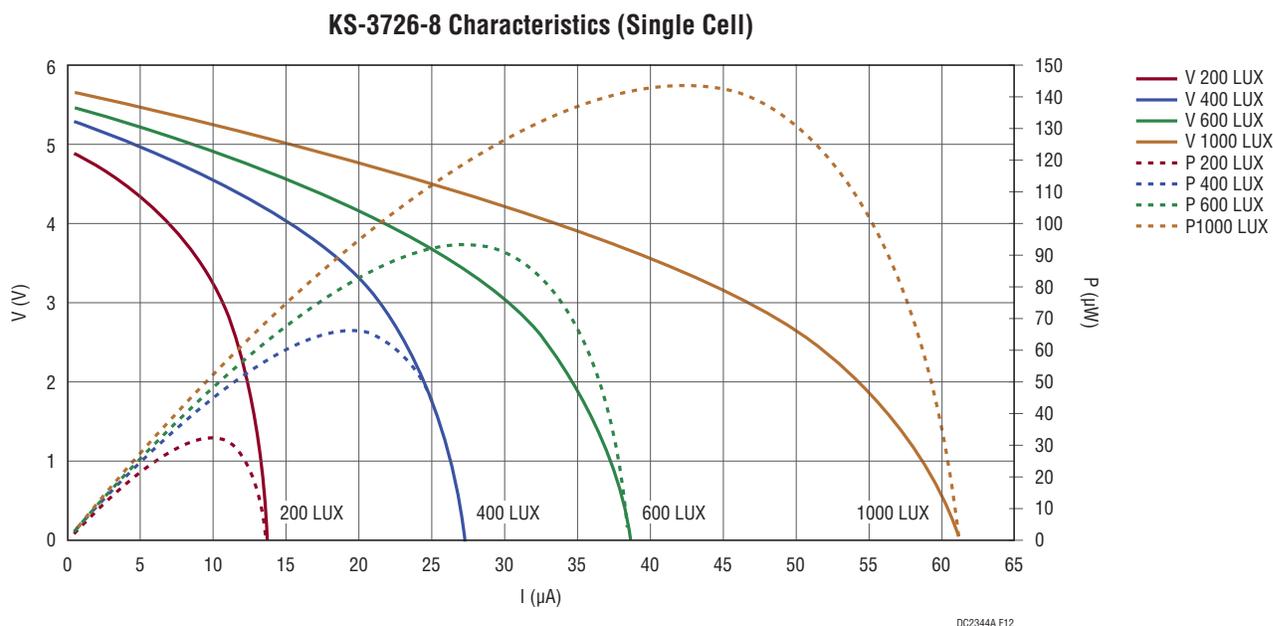


Figure 21. Characteristics of a Single SC3726I-8-1 Solar Cell

# TRANSDUCERS

### TEG

The TEG is used exclusively with the LTC3107. It supplies voltage in the millivolt range and current in the milliamp range, so a transformer is necessary to step up the voltage for use with the IC.

A heat sink is required in this application to create a usable temperature gradient across the surfaces of the TEG. The result is that the bottom of the TEG is kept near room temperature so that only the temperature on the top needs to be altered in order to create a temperature differential.

Due to the small size of the device and its heat sink, the temperature across its junction will even out fairly quickly. As a result, the supplied power is only usable for a short time in this setup.

### Piezo/High-Z AC or DC External Source Input

The terminal block (J3) allows users to connect a piezo-electric, or any other high-impedence AC or DC energy-harvesting device, to the rectified AC1 & AC2 inputs of the LTC3330 & LTC3331. Sources routed through J3 have the option to be configured in voltage doubler or full-wave rectifier mode. This functionality is controlled by JP13-JP16 and SW3.

For voltage doubler configuration, one side of the device is grounded while the other is routed to an IC's AC1 input. In this mode, SW3 should be in the "GND" position in order to ground the switched side of the source (PZ2 on schematic). The appropriate IC is selected by installing JP13 or JP14. This general configuration is shown in Figure 22a. In voltage doubler mode, the UVLO window should be set to the open circuit voltage of the piezo device.

For full-wave rectifier configuration, the device is routed across an IC's AC1 and AC2 inputs. In this mode, SW3 should be in the "AC2" position in order to route the switched side of the source (PZ2) to the AC2 transducer selection jumpers. The appropriate IC is selected by installing JP13 & JP15 or JP14 & JP16. This general configuration is shown in Figure 22c. In full-wave rectifier mode, the UVLO window should be set to approximately half the open circuit voltage of the piezo device.

Figure 22b shows the internal rectifier circuit that is common to both the LTC3330 and the LTC3331. This input is capable of accepting power from a wide range of AC or DC sources.
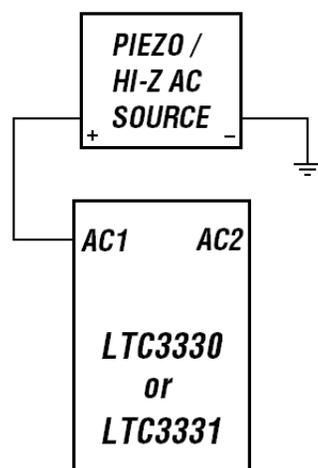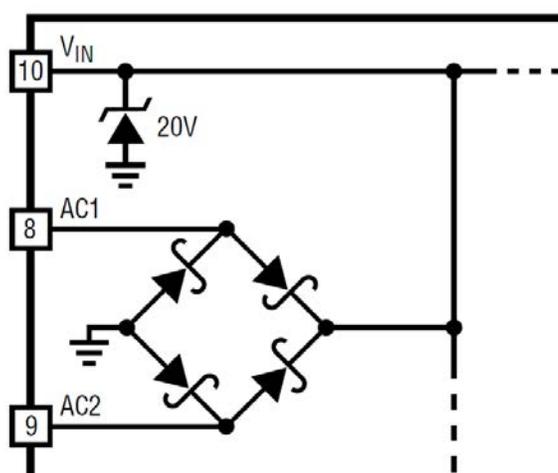
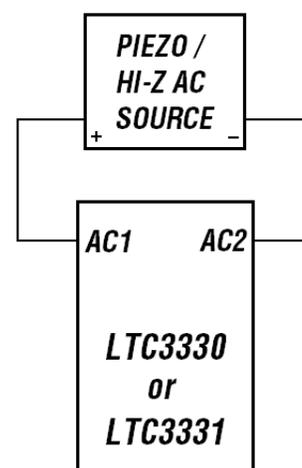**Figure 22a. Voltage Doubler Mode** **Figure 22b. LTC3330 & LTC3331 Internal Rectifier** **Figure 22c. Full-Wave Rectifier Mode**

# TRANSDUCERS

## Custom Transducer Configurations

Various custom energy harvesting sources can be connected to the power management circuits using either the terminal block (J3) or the power input turrets to each IC.

NOTE: Ensure that any power supply fed into the LTC3330 or LTC3331 is current-limited to 50mA using either a resistor or configurable test equipment settings.
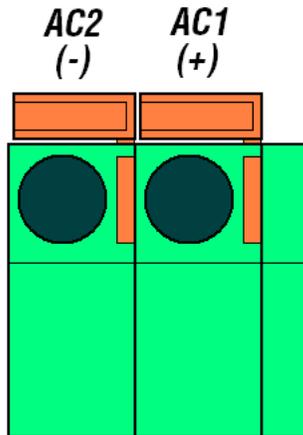


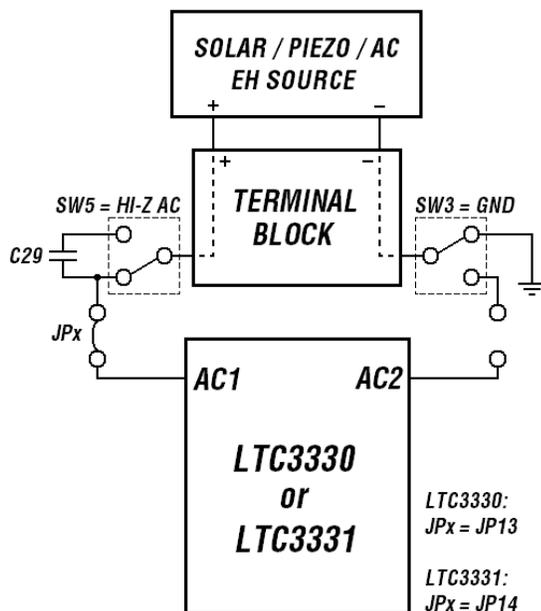**Figure 23. Terminal Block Drawing with ±Terminals Shown**



**Figure 24. Solar Cell/AC Voltage Doubler Configuration Routing**

## Solar Cell/AC Voltage Doubler Configuration

In this configuration, the positive terminal of J3 is routed to the transducer selection jumpers while the negative terminal is connected to ground (BGND). Power can be routed to the AC1 input of either the LTC3330 or LTC3331 if JP13 or JP14 are installed respectively.

This setup is recommended for solar cells and places a piezoelectric or other AC source into voltage doubler configuration. For non-capacitive AC sources, SW5 can be set in the "PMDM" position to connect a series capacitor between the energy harvesting source and the IC input.

With the negative terminal connected to GND, the AC2 input of the selected IC is left open. There are a few routing choices for this pin:

1. Leave AC2 floating.

2. Route on-board solar cells to AC2 on the LTC3330 or LTC3331 by installing JP11 or JP12 respectively. Ensure SW6 = "SERIES".

3. Route an external source to AC2 using the appropriate power input turret on the right side of the board.
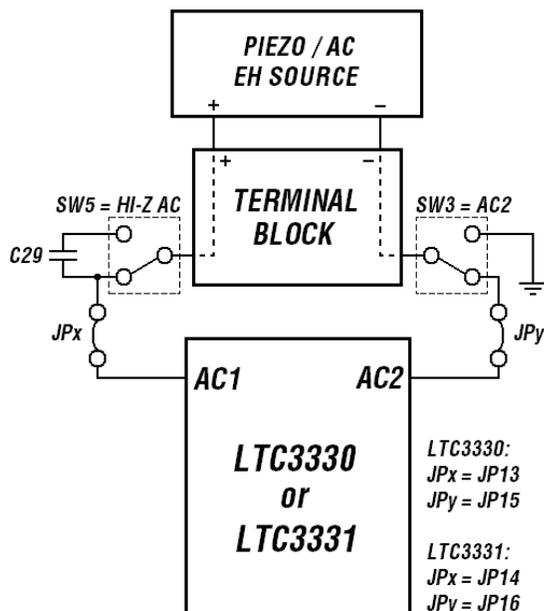
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# TRANSDUCERS



**Figure 25. Full-Wave Rectifier Configuration Routing**

## Full-Wave Rectifier Configuration

In this configuration, both the positive and negative terminals of J3 are routed to the transducer selection jumpers. Power can be routed to the AC1 and AC2 inputs of either the LTC3330 if JP13 and JP15 are installed, or the LTC3331 if JP14 and JP16 are installed.

While this configuration occupies both inputs, it can be useful for AC energy harvesting devices with output voltages that are too high to be used with the LTC3330 or LTC3331 in voltage doubler configuration.
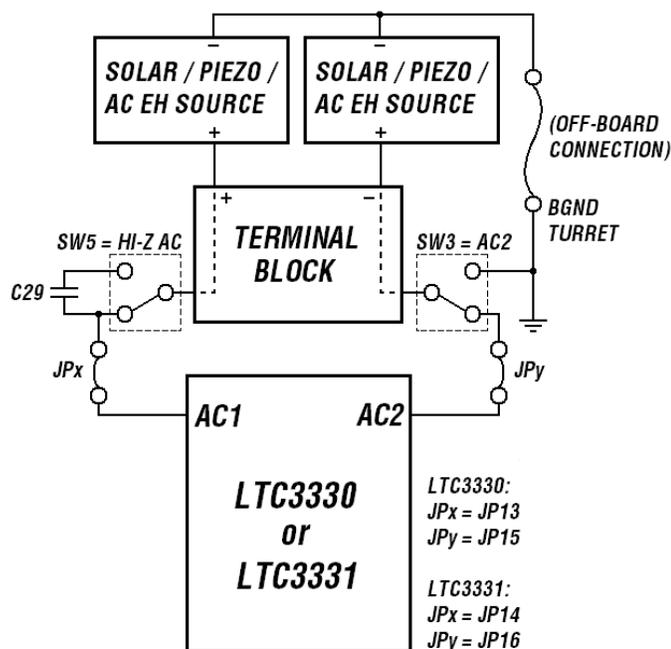


**Figure 26. Dual-Source Configuration Routing**

## Dual-Source Configuration

In this configuration, the positive terminals of two energy harvesting sources are fed into each input of the terminal block. The negative terminals of each energy harvesting source must be externally connected to BGND. Power can be routed to the AC1 and AC2 inputs of either the LTC3330 if JP13 and JP15 are installed, or the LTC3331 if JP14 and JP16 are installed.

Using multiple sources allows the IC to take power from the highest-voltage transducer depending on what energy is available in the environment. For example, two solar cells can be set at different angles so that each one becomes the stronger supply depending on the position of a light source such as the sun. Also, two differently-tuned piezoelectric transducers can be used to capture energy from multiple resonant frequencies on a vibrating body.

# PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
|------|-----|-----------|------------------|--------------------------|
| **LTC3106 Circuit Components** | | | | |
| 1 | 2 | C1, C2 | CAP, CHIP, 100µF, 10V, 20%, X5R, 1206 | TDK, C3216X5R1A107M160AC |
| 2 | 1 | C3 | CAP, CHIP, 4.7µF, 10V, 10%, X7R, 0805 | WÜRTH, 885 012 207 025 |
| 3 | 2 | C4, C5 | CAP, CHIP, 47µF, 10V, 20%, X5R, 1206 | WÜRTH, 885 012 108 012 |
| 4 | 1 | C6 | CAP, CHIP, 0.1µF, 10V, 10%, X7R, 0603 | WÜRTH, 885 012 206 020 |
| 5 | 1 | C34 | CAP, CHIP, X7R, 2.2µF, 10%, 10V, 0603 | WÜRTH, 885012206027 |
| 6 | 1 | D2 | DIODE SCHOTTKY 20V, 1A, SOD-323 | NXP, PMEG2010EA |
| 7 | 1 | D3 | DIODE ZENER (5.1V, 55mA, REVERSE) | CENTRAL, CMHZ4689 |
| 8 | 1 | L1 | INDUCTOR, SHIELDED 15µH, 1.03A, 0.22Ω, 4.8mm × 4.8mm | WÜRTH, 744042150 |
| 9 | 2 | R1, R18 | RES, CHIP, 2.37MΩ, 1%, 1/10W, 0603 | VISHAY, CRCW06032M37FKEA |
| 10 | 1 | R2 | RES, CHIP, 453kΩ, 1%, 1/10W, 0603 | VISHAY, CRCW0603453KFKEA |
| 11 | 1 | R5 | RES, CHIP, 1MΩ, 1/10W, 1%, 0603 | PANASONIC, ERJ-3EKF1004V |
| 12 | 1 | U1 | LOW QUIESCENT CURRENT, BUCK-BOOST POWER MANAGER WITH MPPC | LINEAR TECH, LTC3106EUDC |
| **LTC3107 Circuit Components** | | | | |
| 13 | 1 | C7 | CAP, TANTALUM-POLYMER, 330µF, 6.3V, 20% | PANASONIC, 6TPE330MIL |
| 14 | 1 | C8 | CAP, CHIP, 1000pF, 50V, 10%, X7R, 0603 | WÜRTH, 885 012 206 083 |
| 15 | 1 | C9 | CAP, CHIP, 330pF, 50V, 10%, X7R, 0603 | WÜRTH, 885 012 206 080 |
| 16 | 2 | C10, C13 | CAP, CHIP, 10µF, 6.3V, 20%, X5R, 0603 | WÜRTH, 885 012 106 006 |
| 17 | 1 | C11 | CAP, CHIP, X5R, 2.2µF, 6.3V, 20%, 0603 | WÜRTH, 885 012 106 004 |
| 18 | 1 | C12 | CAP, TANTALUM-POLYMER, 220µF, 6.3V, 20% | PANASONIC, 6TPE220MI |
| 19 | 1 | C35 | CAP, CHIP, X5R, 0.1µF, 20%, 10V, 0402 | WÜRTH, 885 012 105 010 |
| 20 | 1 | R19 | RES, CHIP, 499kΩ, 1/10W, 0603 | PANASONIC, ERJ-3EKF4993V |
| 21 | 1 | T1 | TRANSFORMER, 100:1 TURNS RATIO, 6.0mm × 6.0mm | WÜRTH, 74488540070 |
| 22 | 1 | U2 | ULTRA-LOW VOLTAGE ENERGY HARVESTER/PRIMARY BATTERY LIFE EXTENDER | LINEAR TECH, LTC3107EDD |
| 23 | 1 | U6 | IC, ULTRA-LOW POWER SUPERVISOR WITH POWER-FAIL OUTPUT, TSOT-23 | LINEAR TECH, LTC2935CTS8-2 |
| **LTC3330 Circuit Components** | | | | |
| 24 | 1 | C14 | CAP, CHIP, X5R, 22µF, 20%, 25V, 1210 | WÜRTH, 885 012 109 014 |
| 25 | 2 | C15, C17 | CAP, CHIP, X5R, 1µF, 20%, 6.3V, 0402 | WÜRTH, 885 012 105 006 |
| 26 | 1 | C16 | CAP, CHIP, X5R, 4.7µF, 20%, 6.3V, 0603 | WÜRTH, 885 012 106 005 |
| 27 | 2 | C18, C21 | CAP, CHIP, X5R, 22µF, 20%, 6.3V, 1206 | WÜRTH, 885 012 108 003 |
| 28 | 1 | C19 | CAP, CHIP, X5R, 150µF, 20%, 6.3V, 1210 | SAMSUNG, CL32A157MQVNNNE |
| 29 | 1 | C20 | CAP, CHIP, 10µF, 6.3V, 20%, X5R, 0603 | WÜRTH, 885 012 106 006 |
| 30 | 1 | L2 | INDUCTOR, 100µH , 0.51A, 0.60Ω, 4.8mm × 4.8mm | WÜRTH, 744043101 |
| 31 | 1 | L3 | INDUCTOR, 22µH, 1.00A, 0.37Ω, 4mm × 4.5mm | WÜRTH, 744773122 |
| 32 | 1 | U3 | ENERGY HARVESTING DC/DC WITH BATTERY BACKUP | LINEAR TECH,  LTC3330EUH |

# PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
|------|-----|-----------|------------------|--------------------------|
| **LTC3331 Circuit Components** | | | | |
| 33 | 1 | C22 | CAP, CHIP, X5R, 22µF, 20%, 25V, 1210 | WÜRTH, 885 012 109 014 |
| 34 | 1 | C23 | CAP, CHIP, X5R, 1µF, 20%, 6.3V, 0402 | WÜRTH, 885 012 105 006 |
| 35 | 1 | C24 | CAP, CHIP, X5R, 4.7µF, 20%, 6.3V, 0603 | WÜRTH, 885 012 106 005 |
| 36 | 1 | C26 | CAP, CHIP, X5R, 22µF, 20%, 6.3V, 1206 | WÜRTH, 885 012 108 003 |
| 37 | 1 | C27 | CAP, CHIP, X5R, 150µF, 20%, 6.3V, 1210 | SAMSUNG, CL32A157MQVNNNE |
| 38 | 1 | C25 | CAP, CHIP, X5R, 0.1µF, 20%, 10V, 0402 | WÜRTH, 885 012 105 010 |
| 39 | 1 | D1 | DIODE, SCHOTTKY, 30V, 0.1A, SOD-523 | CENTRAL, CMOSH-3 |
| 40 | 1 | L4 | INDUCTOR, 100µH , 0.51A, 0.60Ω, 4.8mm × 4.8mm | WÜRTH, 744043101 |
| 41 | 1 | L5 | INDUCTOR, 22µH, 1.00A, 0.37Ω, 4mm × 4.5mm | WÜRTH, 744773122 |
| 42 | 1 | Q1 | SMT, BIPOLAR, PNP, 40V, SOT-23 | CENTRAL, CMPT3906E |
| 43 | 1 | Q2 | SMT, DUAL MOSFET, NCHANNEL/PCHANNEL, 60V, SuperSOT-6 | FAIRCHILD, NDC7001C |
| 44 | 1 | R72 | RES, CHIP, 113Ω, 1/16W,1%, 0402 | VISHAY, CRCW0402113RFKED |
| 45 | 2 | R73, R75 | RES, CHIP, 1MΩ, 1/16W,1%, 0402 | VISHAY, CRCW04021M00FKED |
| 46 | 1 | R74 | RES, CHIP, 100kΩ, 1/16W,1%, 0402 | VISHAY, CRCW0402100KFKED |
| 47 | 1 | R76 | RES, CHIP, 3.01kΩ, 1/16W,1%, 0402 | VISHAY, CRCW04023K01FKED |
| 48 | 1 | R77 | RES, CHIP, 100Ω, 1/16W,1%, 0402 | VISHAY, CRCW0402100RFKED |
| 49 | 1 | U4 | NANOPOWER BUCK-BOOST DC/DC WITH EH BATTERY CHARGER | LINEAR TECH,  LTC3331EUH |
| **Switched Output and Signal Buffering Components** | | | | |
| 50 | 1 | C28 | CAP, CHIP, X5R, 0.1µF, 20%, 10V, 0402 | WÜRTH, 885 012 105 010 |
| 51 | 1 | Q3 | N-CHANNEL MOSFET, 30V, SOT23 | ZETEX, ZXMN2F30FH |
| 52 | 11 | Q4-Q14 | DUAL MOSFET 20V N-TYPE/P-TYPE | VISHAY, SI1553CDL-T1-GE3 |
| 53 | 1 | R91 | RES, CHIP, 3MΩ, 1%, 1/10W, 0603 | VISHAY, CRCW06033M00FKEA |
| 54 | 24 | R92, R100-R113, R120-R128 | RES, CHIP, 10MΩ, 1%, 1/10W, 0603 | VISHAY, CRCW060310M0FKEA |
| 55 | 1 | U5 | IC, ULTRA-LOW POWER SUPERVISOR WITH POWER-FAIL OUTPUT, TSOT-23 | LINEAR TECH, LTC2935CTS8-2 |
| **Power Sources and Energy Storage Components** | | | | |
| 56 | 1 | BAT1 | CR2032 COIN LI-ION BATTERY | ENERGIZER , CR2032VP |
| 57 | 1 | BAT2 | COIN LI-ION BATTERY Lir2032 | POWERSTREAM, Lir2032 |
| 58 | 2 | BTH1, BTH2 | BATTERY HOLDER COIN CELL 2032 SMD | WÜRTH, 79527141 |
| 59 | 1 | C29 | CAP, CHIP X5R, 10µF, 20%, 25V,1210 | WÜRTH, 885 012 109 013 |
| 60 | 1 | C30 | SUPERCAP, 15mF, -20%, +80%, 5.5V, SMD | AVX, BZ055B153ZSB |
| 61 | 10 | CO1-CO10 | CAP, CHIP, X5R, 150µF, 20%, 6.3V, 1210 | SAMSUNG, CL32A157MQVNNNE |
| 62 | 2 | SC1, SC2 | AMORPHOUS INDOOR SOLAR CELL, 37mm × 26mm | CHINA SOLAR LTD, KS-3726-8 |
| 63 | 1 | TEG1 | PELTIER MODULE CP85438 | CUI INC., CP85438 |

# PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
|------|-----|-----------|------------------|--------------------------|
| **Additional Demo Board Circuit Components** | | | | |
| 64 | 0 | C31 (OPT) | SUPERCAP, 85mF, 5.0V, 20mm × 18mm | CAP-XX, GA209F |
| 65 | 0 | C32, C33 (OPT) | CAP, CHIP, X5R, 0.1µF, 20%, 10V, 0402 | WÜRTH, 885 012 105 010 |
| 66 | 0 | D4-D7 (OPT) | DIODE, SCHOTTKY, 40V, 1A, SOD-123 | DIODES INC, 1N5819HW-7-F |
| 67 | 0 | R87, R88 (OPT) | RES, CHIP, 7.5kΩ, 1/16W, 1%, 0402 | VISHAY, CRCW04027K50FKED |
| **Hardware For Demo Board Only** | | | | |
| 68 | 19 | E1-E19 | TURRET, 0.061 DIA | MILL-MAX, 2308-2 |
| 69 | 1 | HS1 | HEATSINK, 40mm × 40mm | ATS, ATS-54400D-C2-R0 |
| 70 | 1 | J1 | 2×10, 20-PIN, SMT RIGHT ANGLE SOCKET w/KEY (PIN 14), 0.100 | SAMTEC, SMH-110-02-L-D-14 |
| 71 | 1 | J2 | 2X6, 12-PIN, SMT RIGHT ANGLE SOCKET w/KEY (PIN 5), 0.100 | SAMTEC, SMH-106-02-L-D-05 |
| 72 | 1 | J3 | HORIZONTAL SCREWLESS TERMINAL BLOCK, 2-PIN, 10A 300VAC | WÜRTH, 691 401 710 002B |
| 73 | 8 | JP1-JP4, JP5-JP8 | SMT HEADER, 2 PINS, 2mm | SAMTEC, TMM-102-01-F-S-SM |
| 74 | 8 | JP9-JP16 | HEADER, 2 PINS, 2mm | WÜRTH, 620 002 111 21 |
| 75 | 2 | JP17, JP21 | SMT HEADER, 6 TOTAL PINS, 2 ROWS, 2mm | WÜRTH, 621 006 219 21 |
| 76 | 1 | JP18 | SMT HEADER, 8 TOTAL PINS, 2 ROWS, 2mm | WÜRTH, 621 008 219 21 |
| 77 | 1 | JP19 | HEADER, 3 PINS, 2mm | WÜRTH, 620 003 111 21 |
| 78 | 1 | JP20 | HEADER, 4 PINS, 2mm | WÜRTH, 620 004 111 21 |
| 79 | 8 | JP3, JP7, JP11, JP17B, JP18C, JP19, JP20, JP21A | SHUNT 2mm | WÜRTH, 608 002 134 21 |
| 80 | 1 | PB1 | SWITCH TACTILE, SPST-NO, 0.05A 12V | WÜRTH, 434111025826 |
| 81 | 34 | R3, R6, R9, R10, R12, R15, R16, R20, R23, R25, R26, R28, R31, R32, R35, R37, R39, R41, R42, R44, R46, R49, R51, R53, R55, R56, R58, R61, R63, R65, R67, R68, R70, R89 | RES, CHIP, 0Ω, 0603 | VISHAY, CRCW06030000Z0EA |
| 82 | 0 | R4, R7, R8, R11, R13, R14, R17, R21, R22, R24, R27, R29, R30, R33, R34, R36, R38, R40, R43, R45, R47, R48, R50, R52, R54, R57, R59, R60, R62, R64, R66, R69, R71, R90, R99 (OPT) | RES, CHIP, 0Ω, 0603 | VISHAY, CRCW06030000Z0EA |

# PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
|---|---|---|---|---|
| 83 | 0 | R78, R79, R81, R83, R85, R86, R96, R97, R98, R114, R117, R119 (OPT) | RES, CHIP, 0Ω, 0402 | VISHAY, CRCW04020000Z0ED |
| 84 | 9 | R80, R82, R84, R93, R94, R95, R115, R116, R118 | RES, CHIP, 0Ω, 0402 | VISHAY, CRCW04020000Z0ED |
| 85 | 3 | SW1, SW4, SW7 | DP3T SLIDE SWITCH, 12mm × 3.5mm, 0.2A 12VDC | COPAL, CL-SB-23A-02T |
| 86 | 1 | SW2 | 4PDT SLIDE SWITCH, 16.5mm × 7mm, 0.1A 30VDC | ALPS, SSSF040800 |
| 87 | 2 | SW3, SW5 | SPDT SLIDE SWITCH, 10mm × 2.5mm, 0.5A 12VDC | WÜRTH, 450301014042 |
| 88 | 1 | SW6 | DPDT SLIDE SWITCH, 8.5mm × 3.5mm, 0.2A 12VDC | COPAL, CL-SB-22A-01T |
| 89 | 4 | --- | ADHESIVE CABLE MOUNT U-STYLE CLIP, | WÜRTH, 523252000 |
| 90 | 0.003 | --- | ELECTROCONDUCTIVE ADHESIVE, TWO 6mL TUBES | MG CHEMICALS, 8331-14G |
| 91 | 0.010 | --- | INSTANT ADHESIVE, 20g BOTTLE | LOCTITE, 40340 |
| 92 | 0.001 | --- | ELECTRICAL TAPE, 3/4" × 1/2" | 3M, 33+ SUPER (3/4" × 66') |
| 93 | 0 | STANDOFF ×6 (OPT) | STANDOFF, HEX .625"L, 4-40, THR NYLON | KEYSTONE, 1902F |
| 94 | 0 | SCREW ×6 (OPT) | SCREW, MACH, PHIL, 4-40, .250 IN, NYLON | B&F FASTENER SUPPLY, NY PMS 440 0025 PH |
| 95 | 1 | --- | FAB, PRINTED CIRCUIT BOARD | DEMO CIRCUIT 2344A |
| 96 | 1 | --- | STENCIL - TOP | STENCIL #2344A-TOP |
| 97 | 1 | --- | STENCIL - BOTTOM | STENCIL #2344A-BOTTOM |

# SCHEMATIC DIAGRAM



dc2344afa
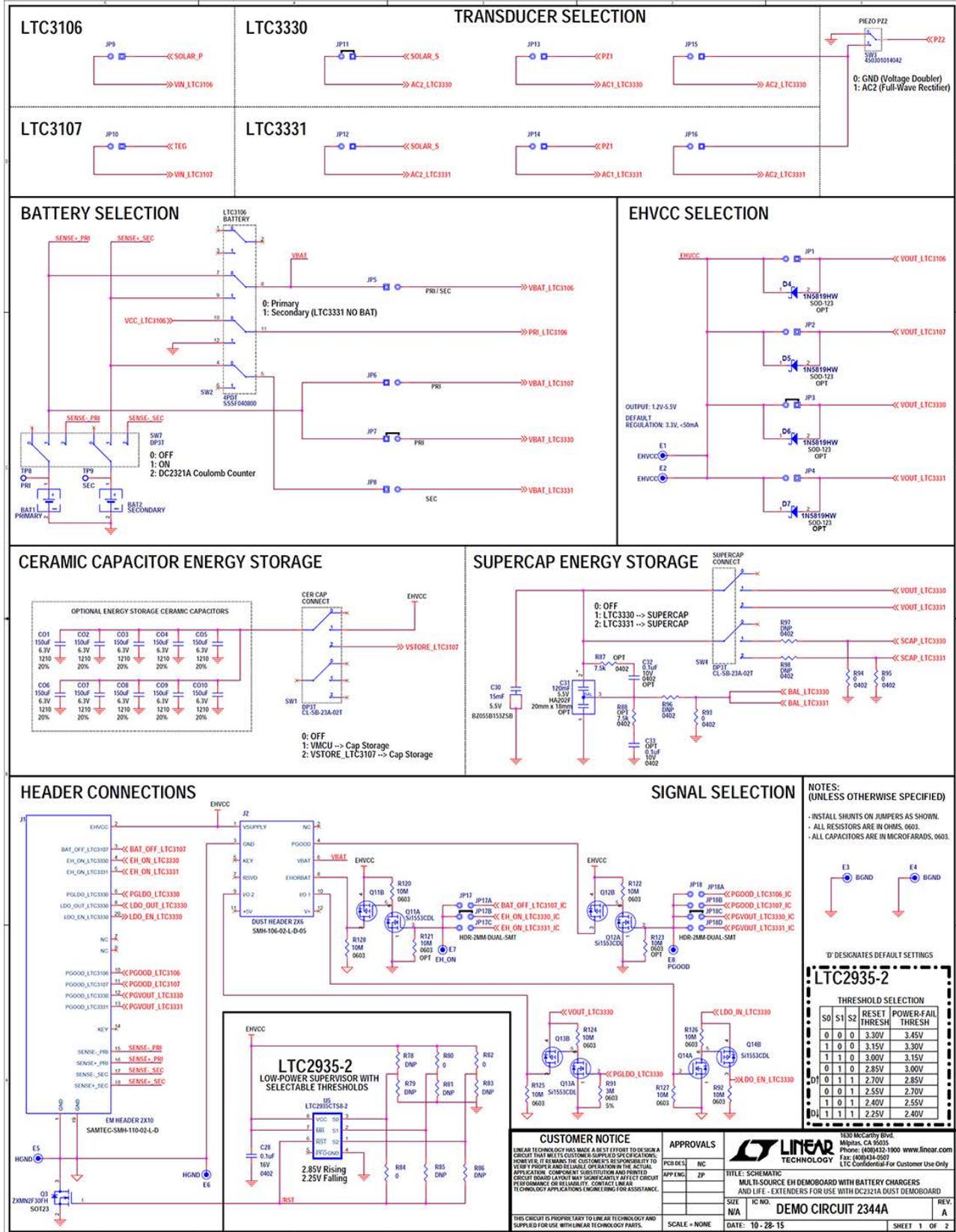
# SCHEMATIC DIAGRAM
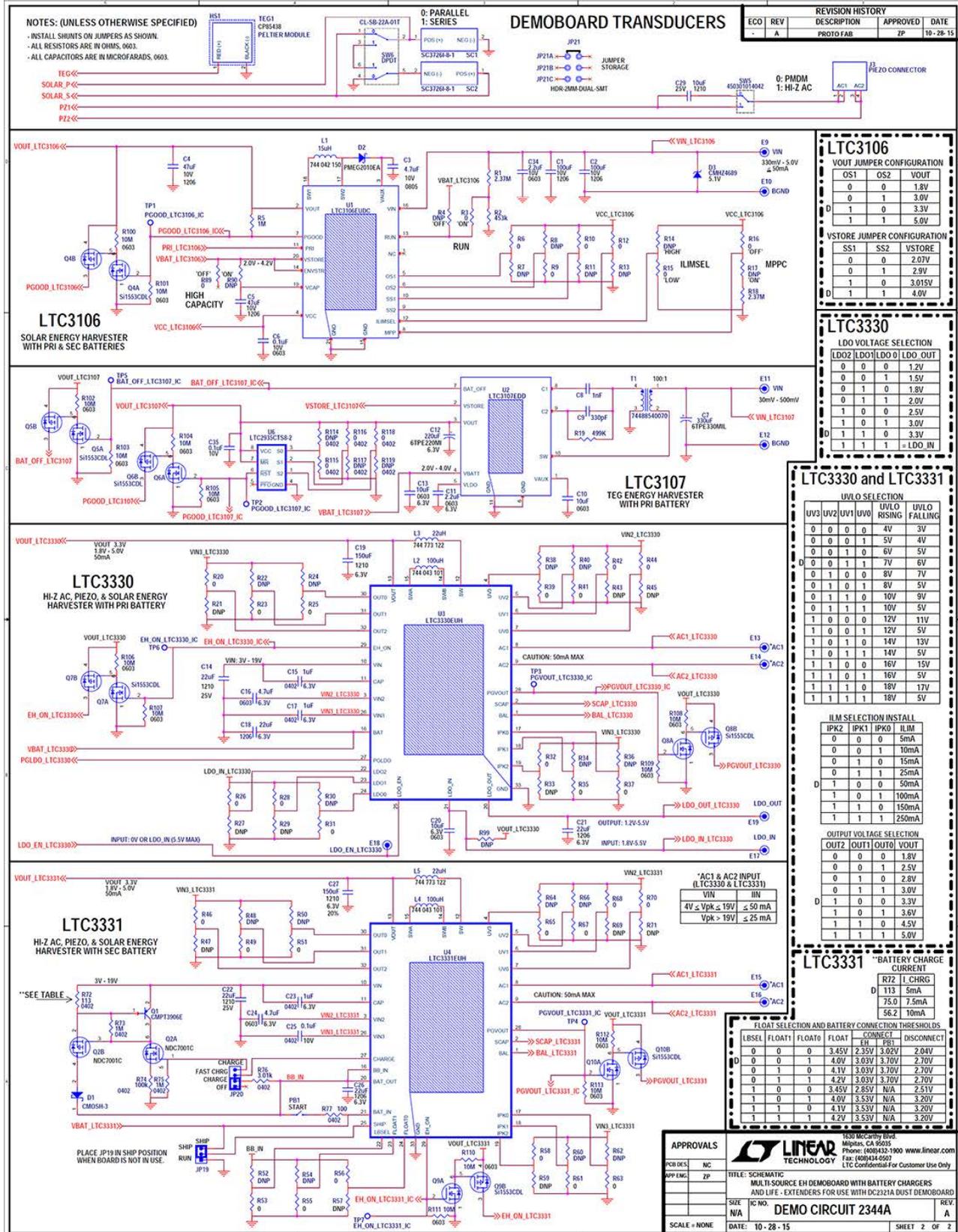
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Mailing Address:


Linear Technology

1630 McCarthy Blvd.

Milpitas, CA 95035

dc2344afa

40 **Linear Technology Corporation**
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LT 0916 REV A • PRINTED IN USA

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