CONDUCTED EMI SIMULATION WITH LTSPICE - FLYBACK DEMO BOARD

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FAE Key Account

WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

Agenda

- Introduction
  - Overview and key points of the board
- Time domain measurements and simulation
  - Background (Calculations)
- EMC measurements from the workbench and EMC simulation
  - Background (Quiz, Calculations, REDEXPERT)

Simulating EMI with LTspice in General

Limits

- Reasonable LTspice EMC simulations:
  - Conducted EMI (content of this presentation)
  - Surge
- For other EMC phenomena, the SPICE simulation is less useful because:
  - The coupling paths are unknown,
  - The phenomena are field-bound,
  - An evaluation criterion is missing. → For an ESD or burst pulse, it is not clear when a real circuit no longer works correctly.

Simulating Conducted EMI with LTspice

Limits

- A simple system is required for the analysis (e.g. a DC/DC converter).
  - A complex system requires too much computing time or LTspice gets stuck with convergence problems.

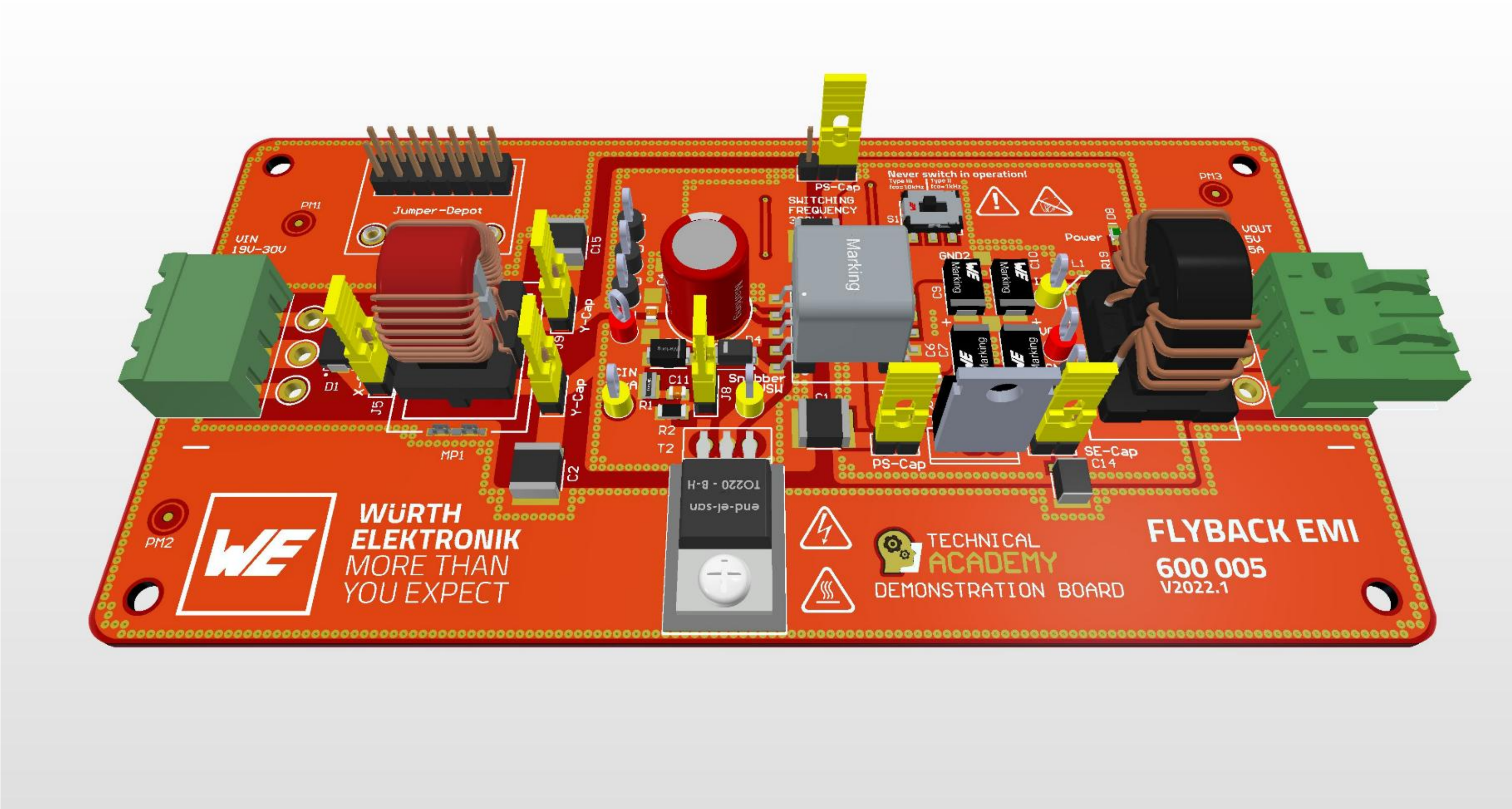
- There are no detectors implemented in LTspice.
  - In a simulation with an AC input voltage you can't capture the difference between Quasi-peak, Peak and Average.
  - As a workaround you can simulate with a DC voltage that corresponds to the AC peak voltage (e.g. 325V).
    - ➢ This is how the peak values can be estimated.

- Coupling paths should be known as far as possible.
  - Conducted coupling can be simulated very well.
  - The problem with capacitive coupling is that the values of the parasitic coupling capacitors are often unknown in reality.
  - Inductive coupling is difficult to analyze and model (refer to Demonstration Board - V2022.1 vs. V2023.1)
    - ➢ A circuit with a bad layout (parasitic loop antennas) cannot be realistically simulated with LTspice.

- The simulation is only as good as the SPICE models used.
  - The relevant component models (e.g. input capacitor) should at least be based on the simplified equivalent circuit diagram (e.g. ESR, ESL included).

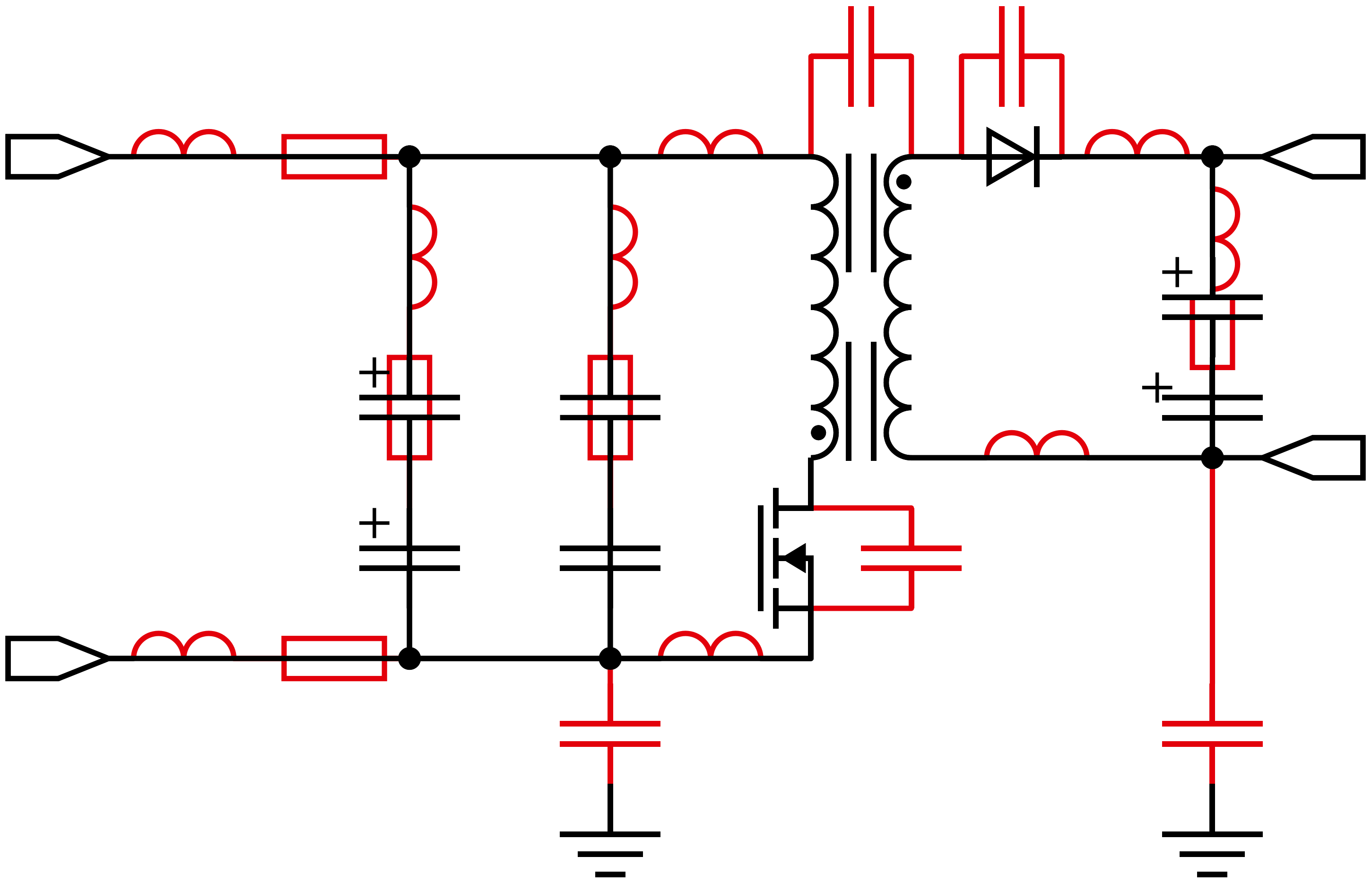
Technical specification – Example application

- DC/DC Flyback-Converter CCM (Forced Continuous Conduction Mode)
  - U_{in} = 24V (19-30V)
  - U_{out} = 5V
  - $I_{out,max}$ = 5A (25W)
  - f_{sw} ≈ 300kHz
  - Efficiency ≈ 90%
- IC: ADP1071-2 (Analog Devices)
  - with synchronous rectifier
- Transformer: WE-PoEH 749119550
- MOSFETs in TO220-package



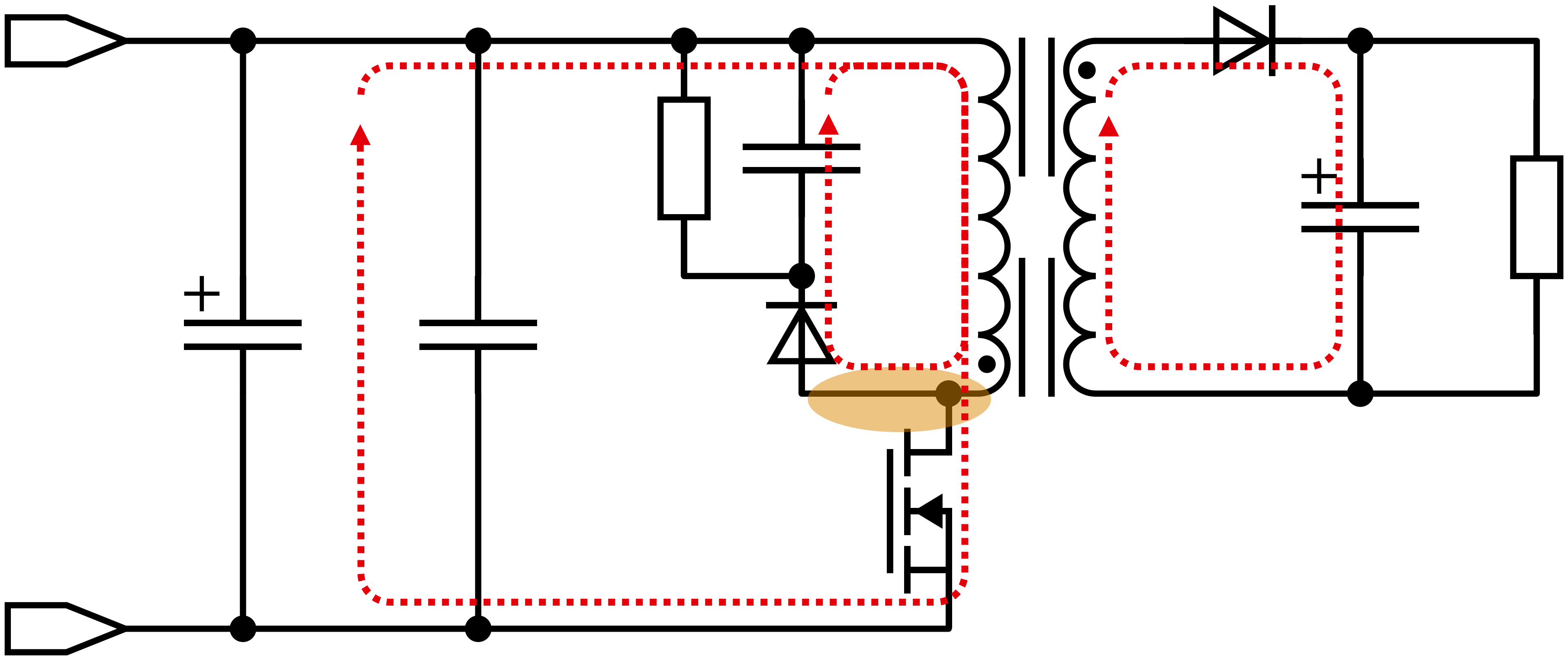
Introduction - Flyback Converter

Parasitic Model



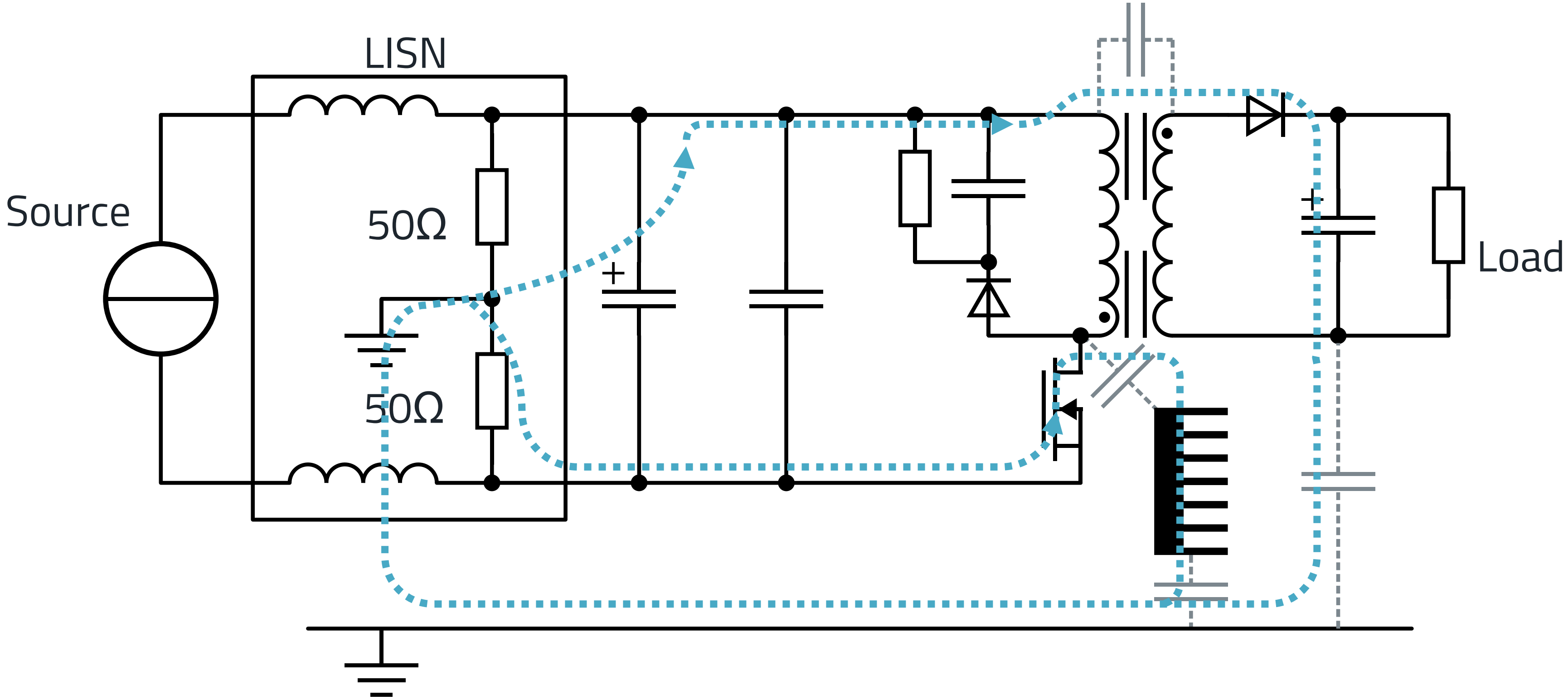
Introduction - Flyback Converter

Hot Node and Critical Loops



Introduction - Capacitive Coupling in a Flyback Converter

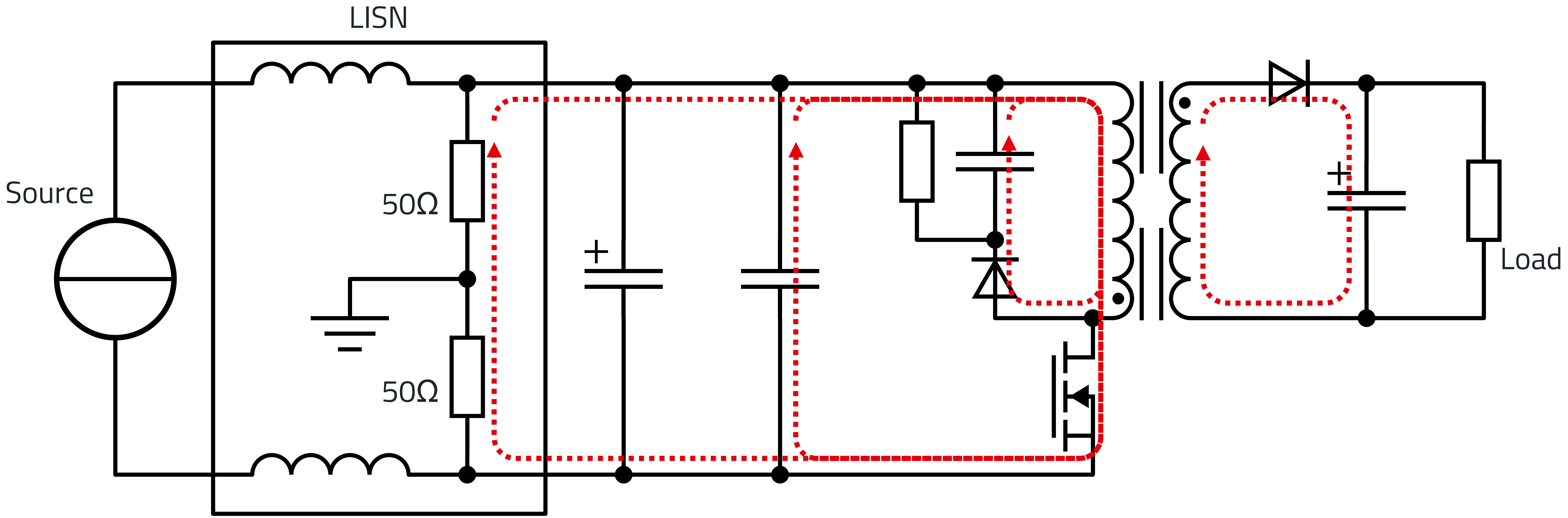
High du/dt Nodes



High common-mode currents through parasitic capacitances
(electric dipole and monopole antennas)

Introduction - Inductive Coupling in a Flyback Converter

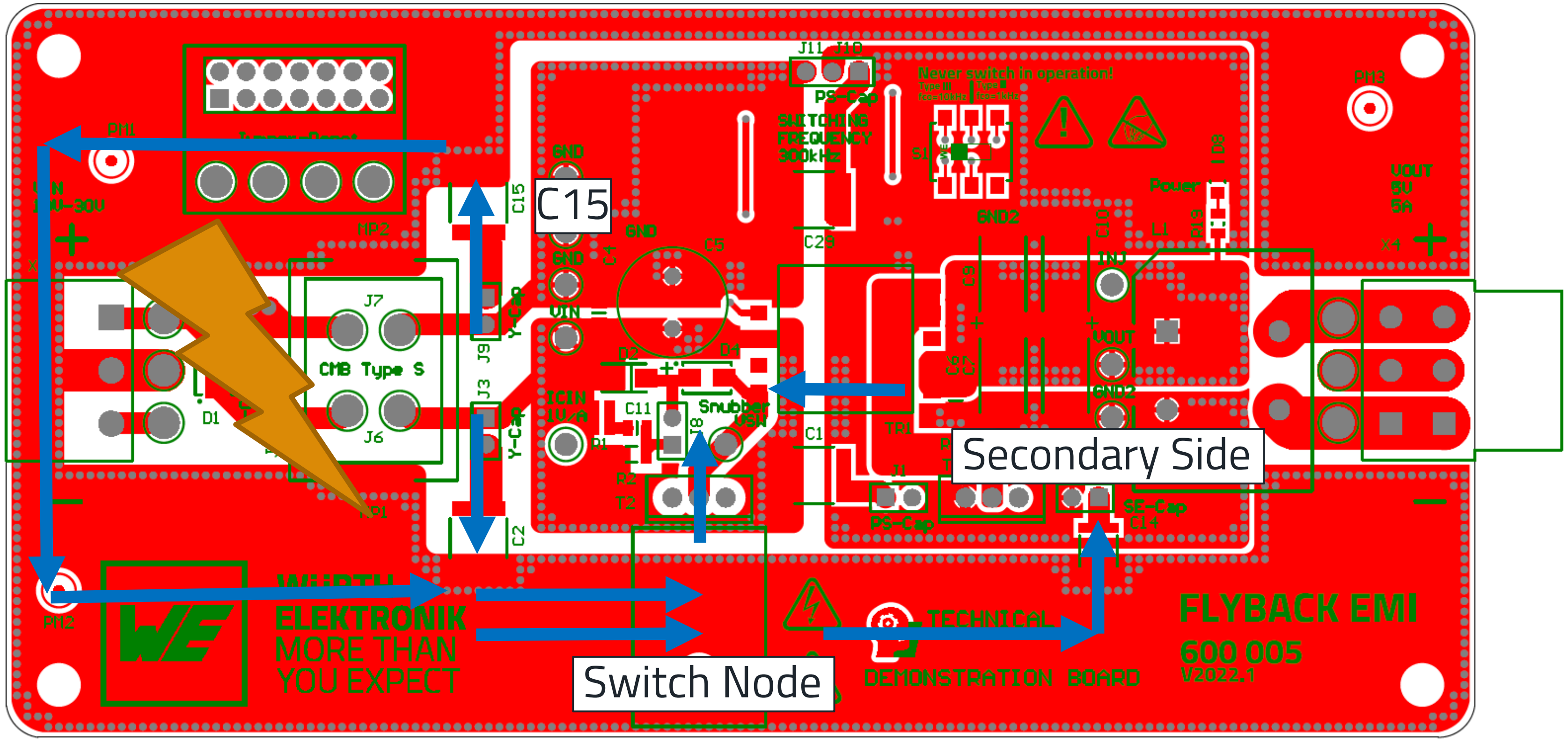
High di/dt Loops



Inductive coupling caused by high di/dt differential-mode currents
(magnetic loop antennas)

Introduction - Inductive coupling

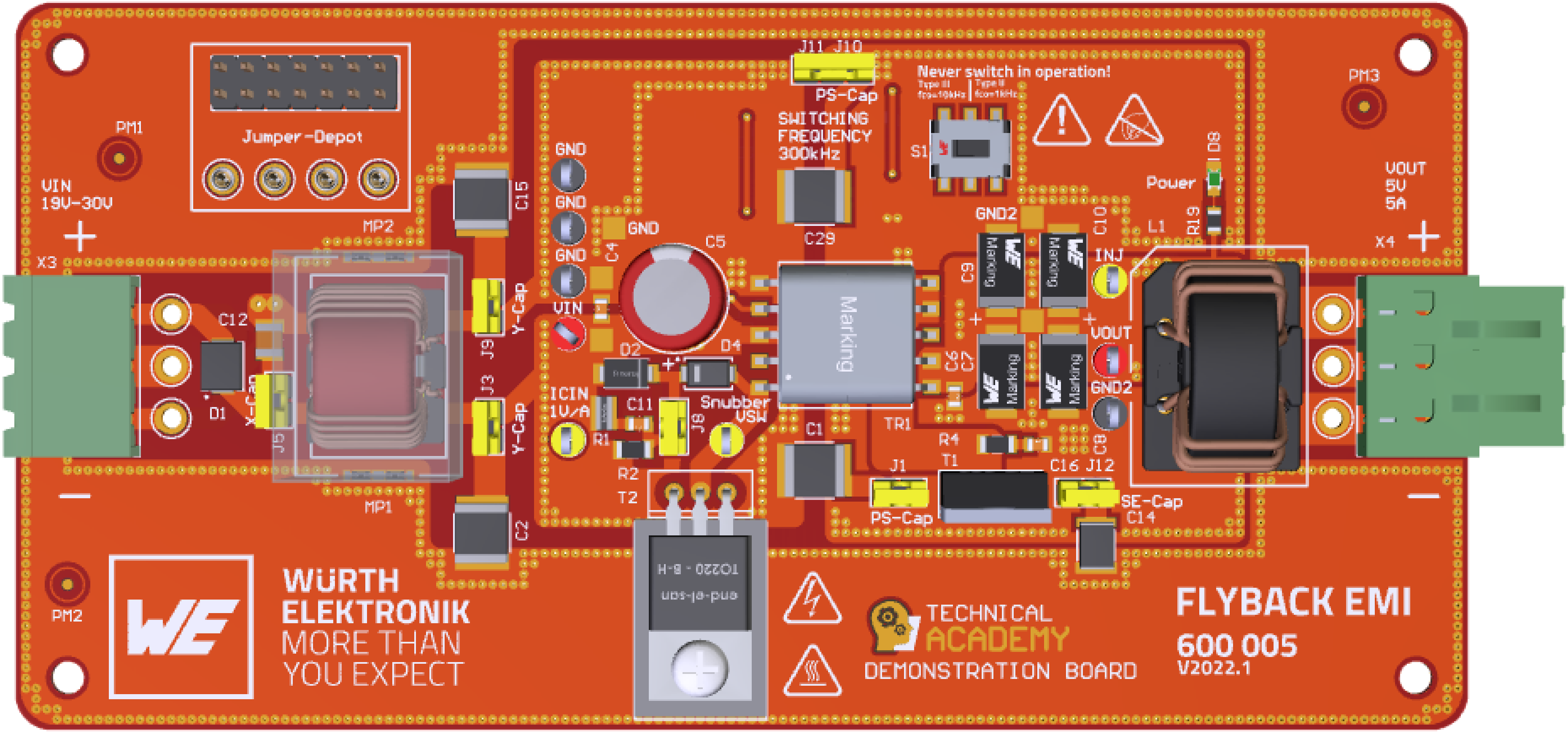
Flyback EMI - Demonstration Board - V2022.1 - Modification



- There is no short noise return path from Y-capacitor C15 to CM noise source (switch node, secondary side).
- CM noise bypasses the filter and couples inductively into the filter (parasitic loop antenna).
- CM/DM conversion

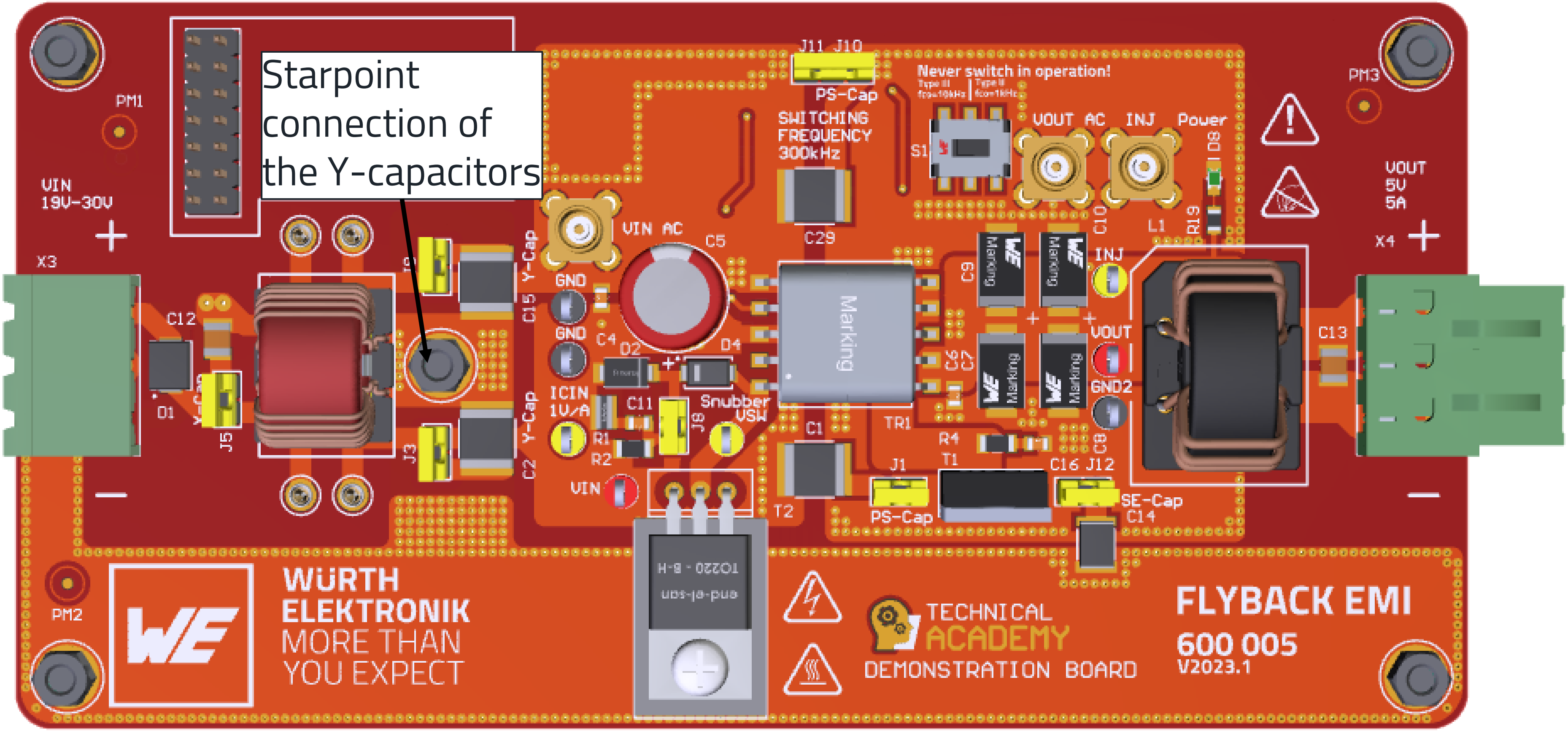
Introduction - Inductive coupling

Top - Flyback EMI - Demonstration Board - V2022.1



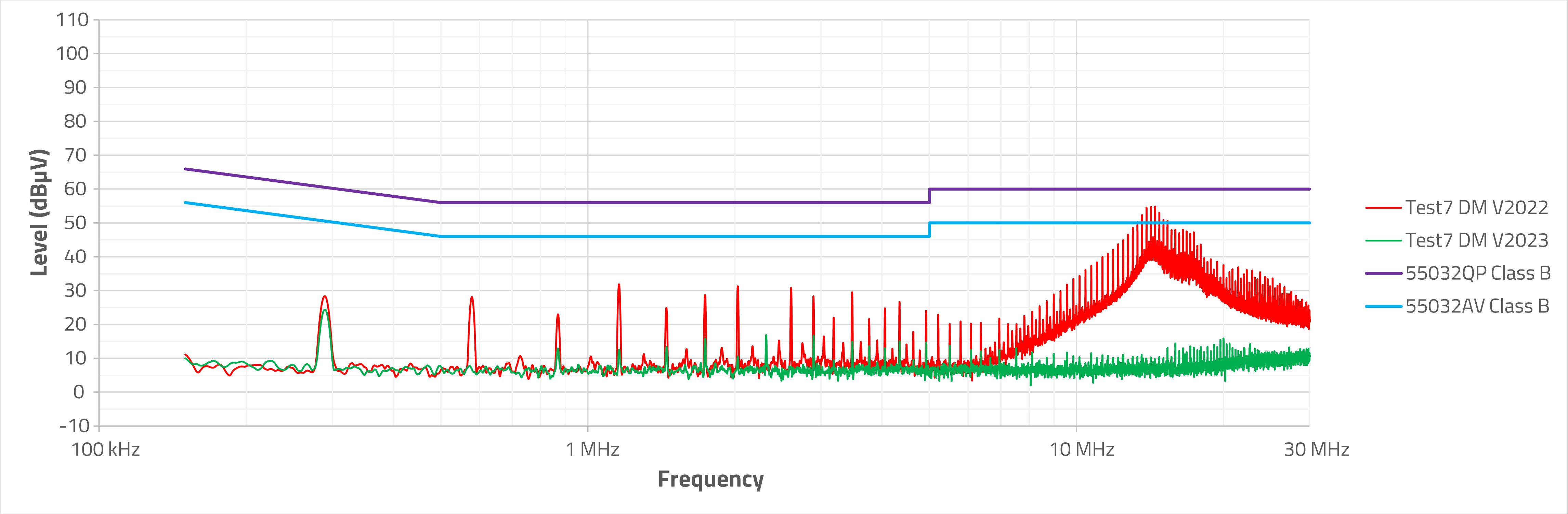
Introduction - Inductive coupling

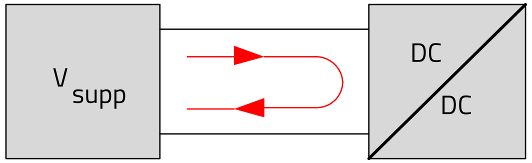
Top - Flyback EMI - Demonstration Board - V2023.1



Introduction - Inductive coupling

Layout improvement - Flyback EMI - Demonstration Board - V2022.1 vs. V2023.1



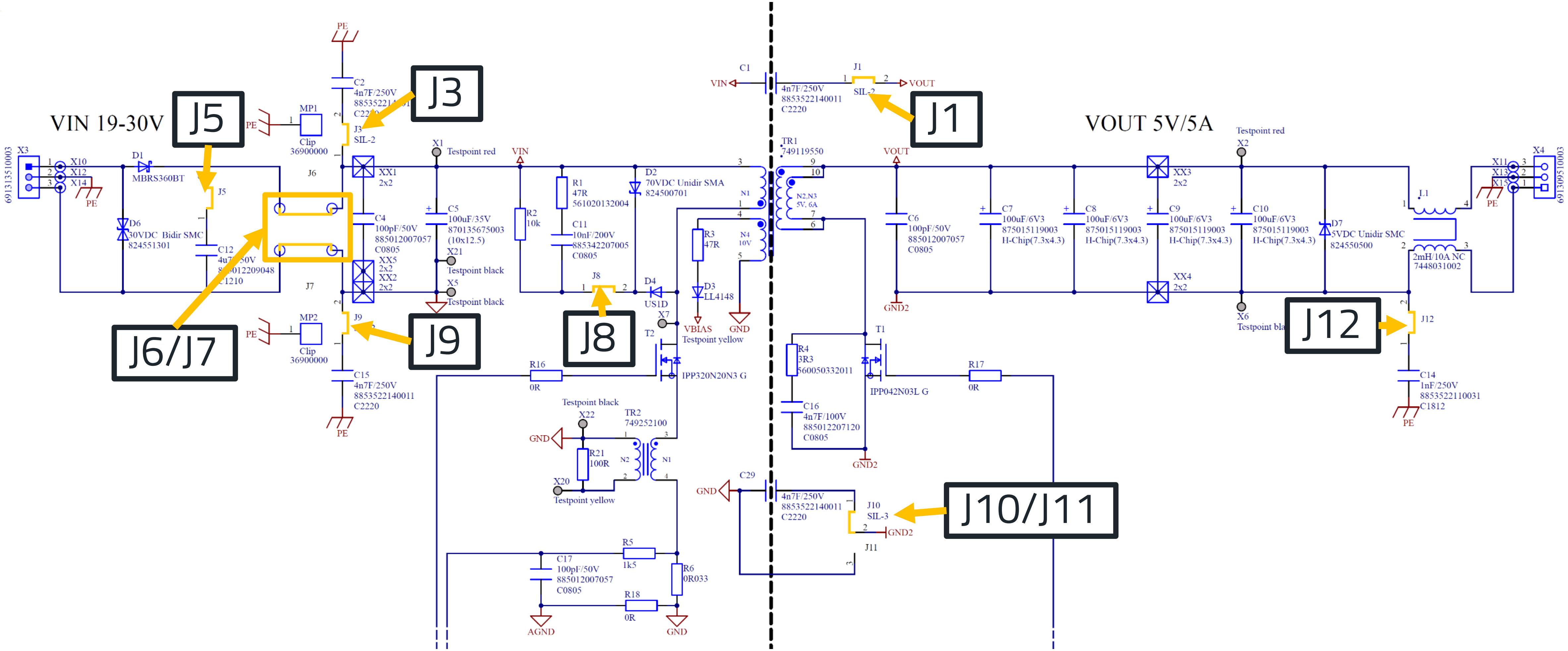


Differential Mode

Name	Description
Test7 DM V2022	All improvements – Test 7 Demonstration Board - 2022.1
Test7 DM V2023	All improvements – Test 7 Demonstration Board - 2023.1

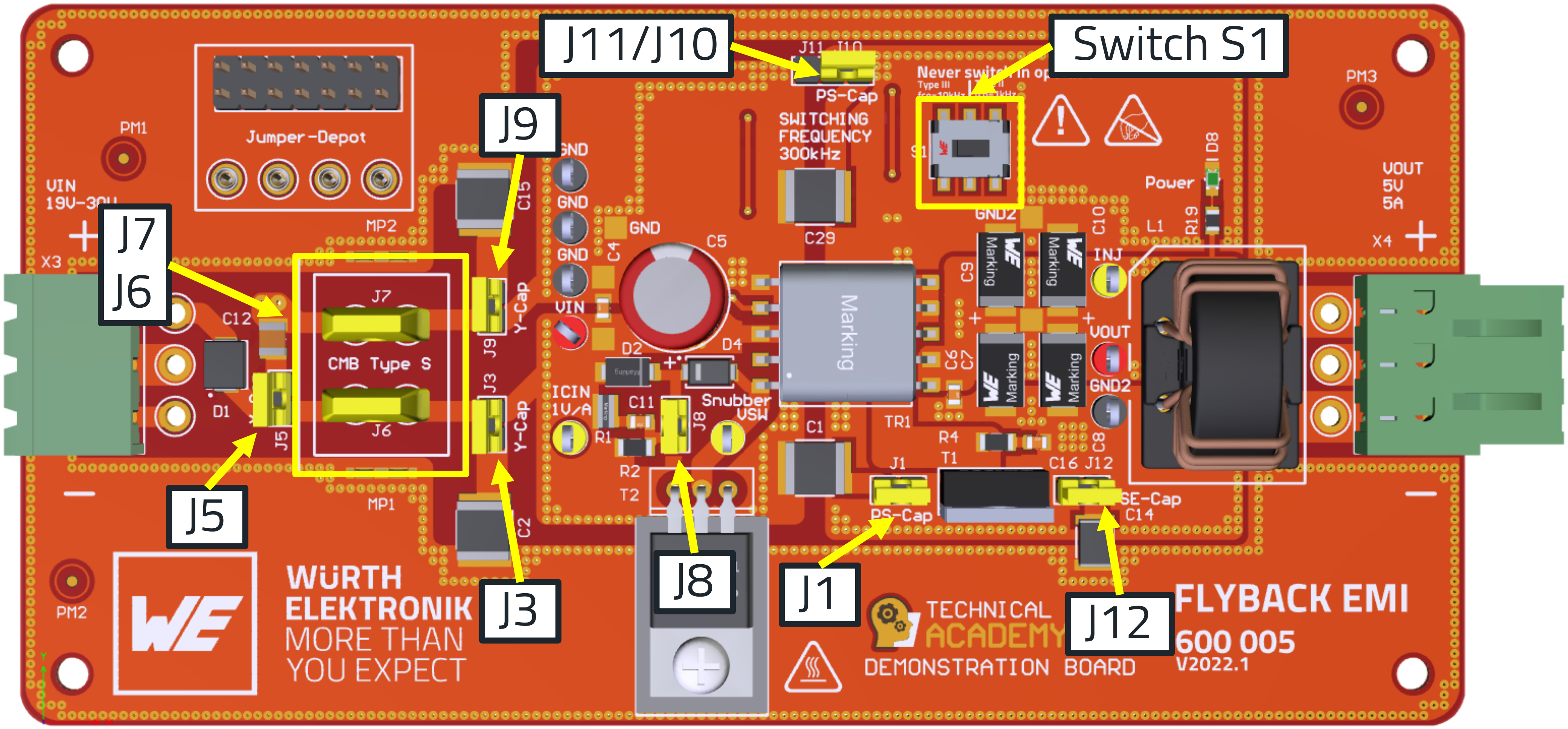
Schematic

Jumper location



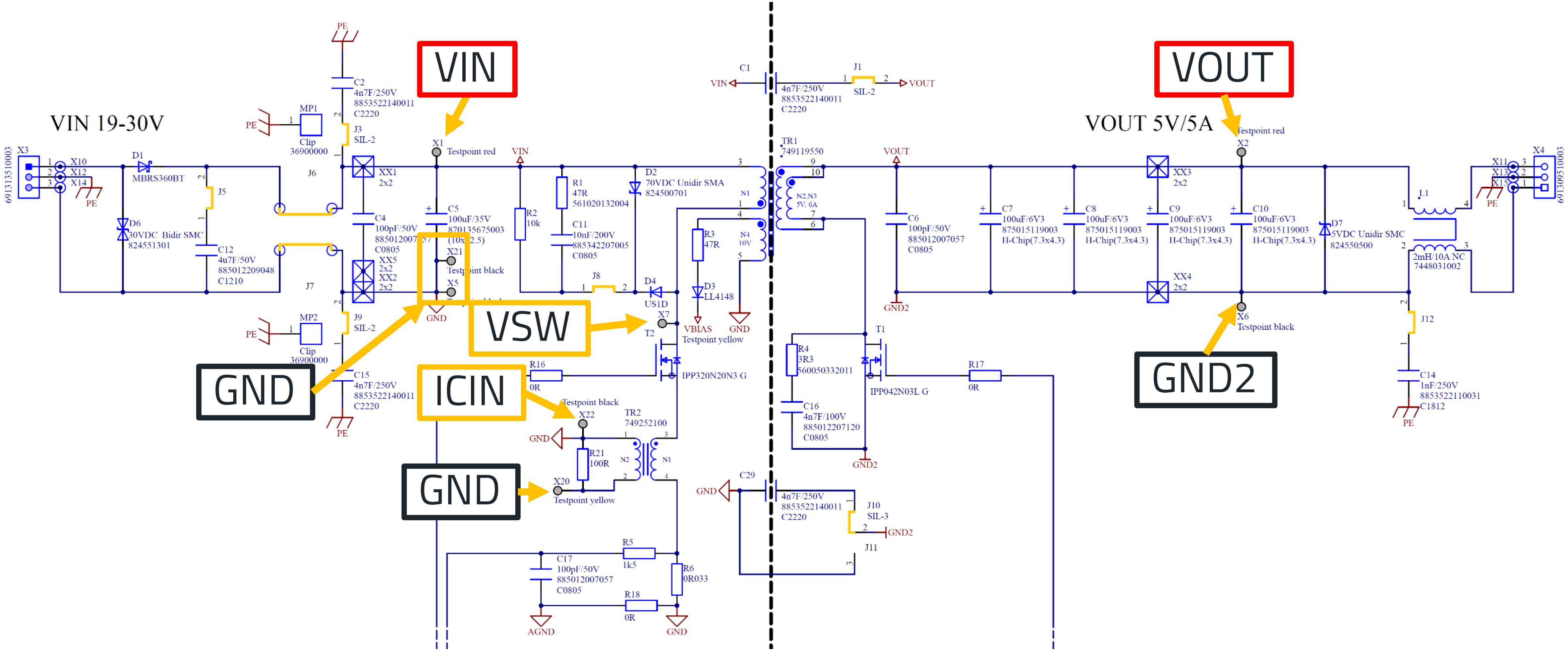
Board overview

Jumper location



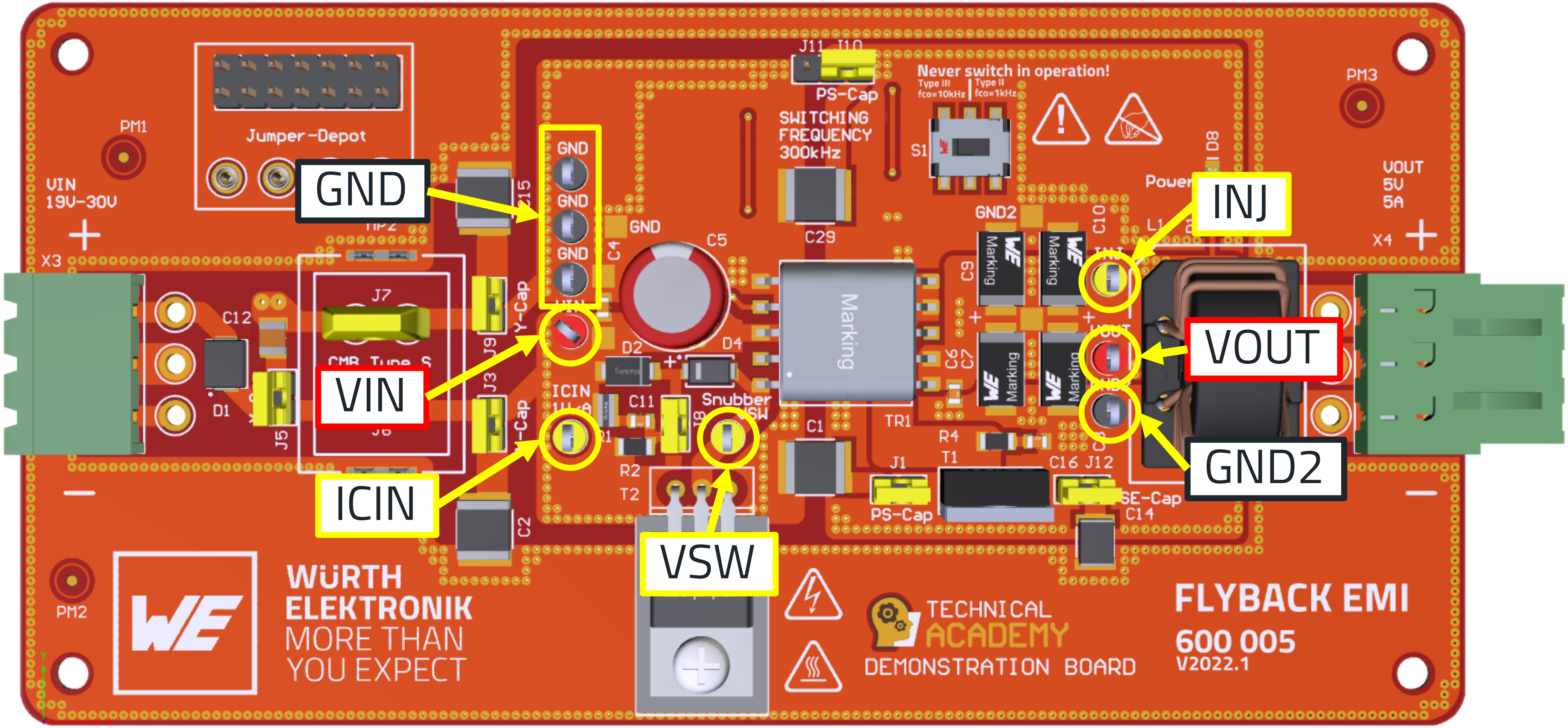
Schematic

Test point location

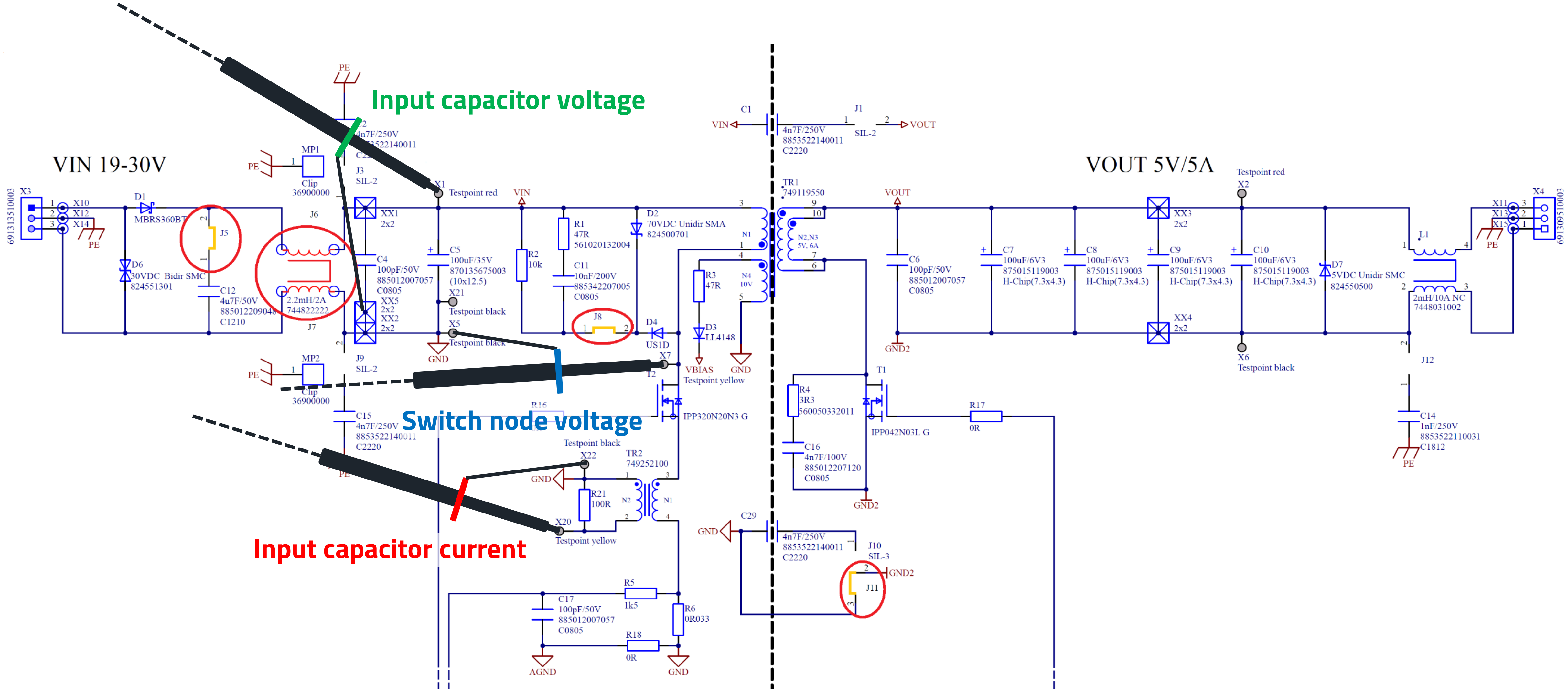


Board overview

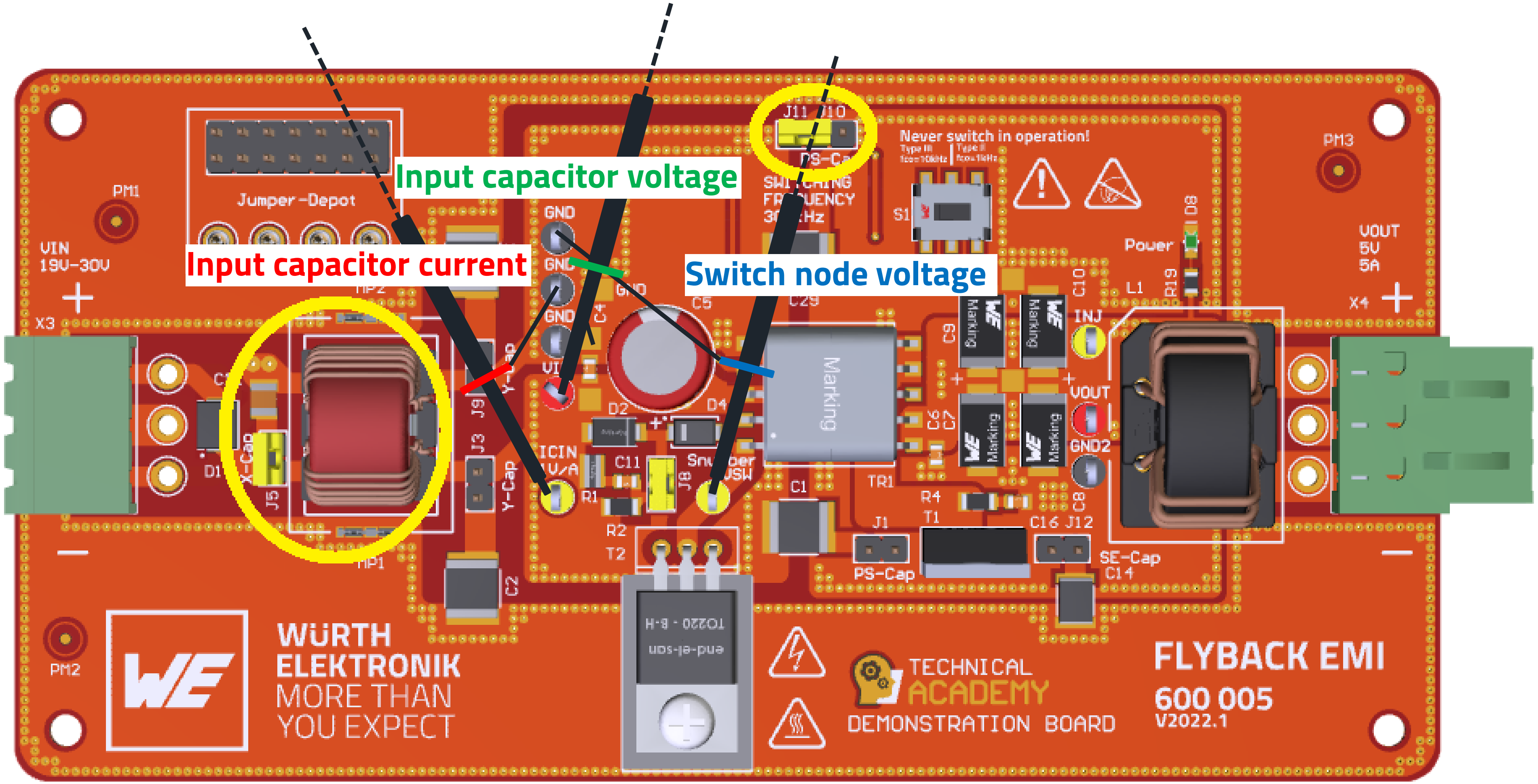
Test point location



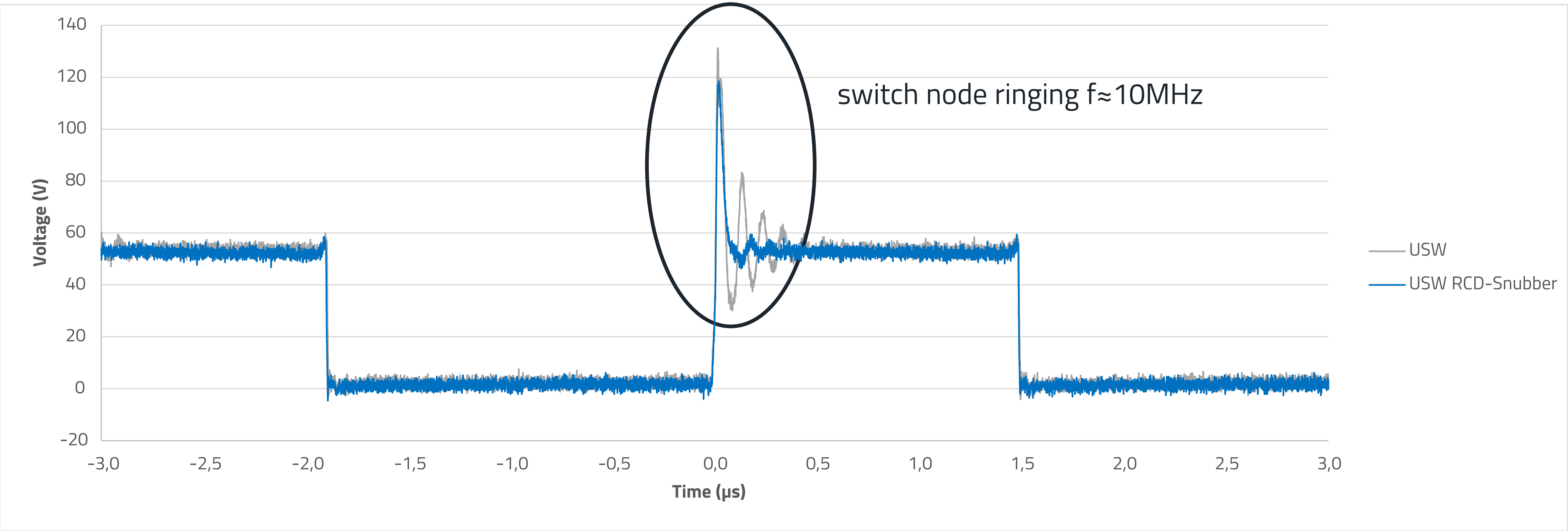
Test#1: Schematic



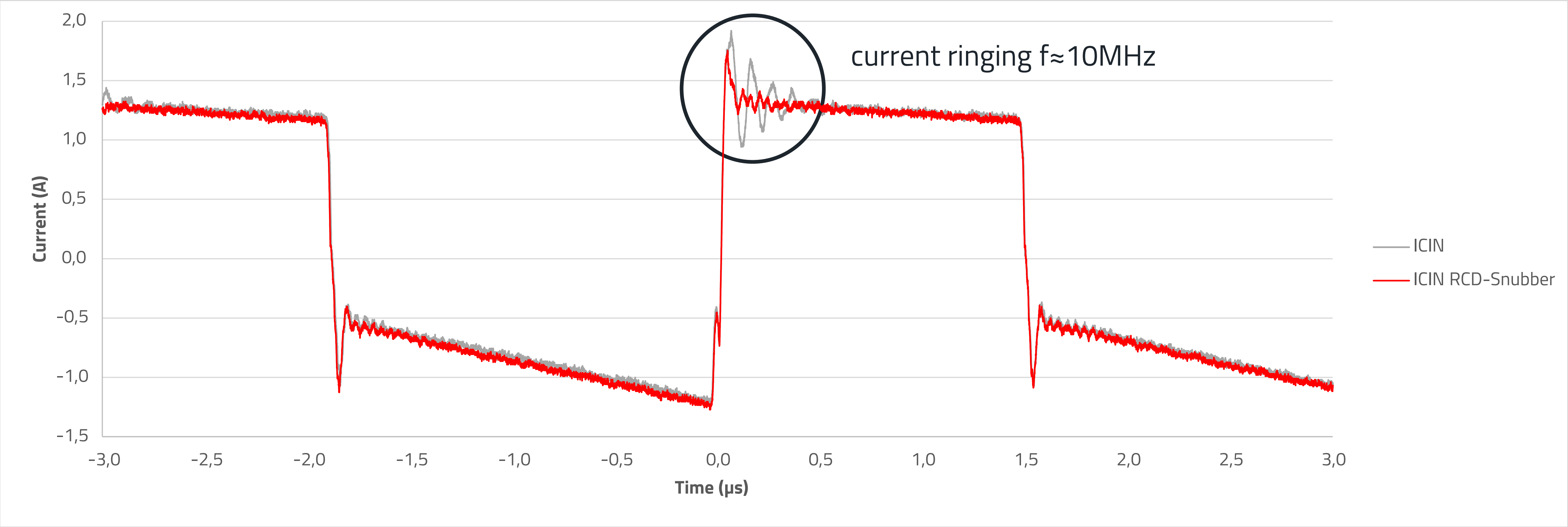
Test#1: Board configuration



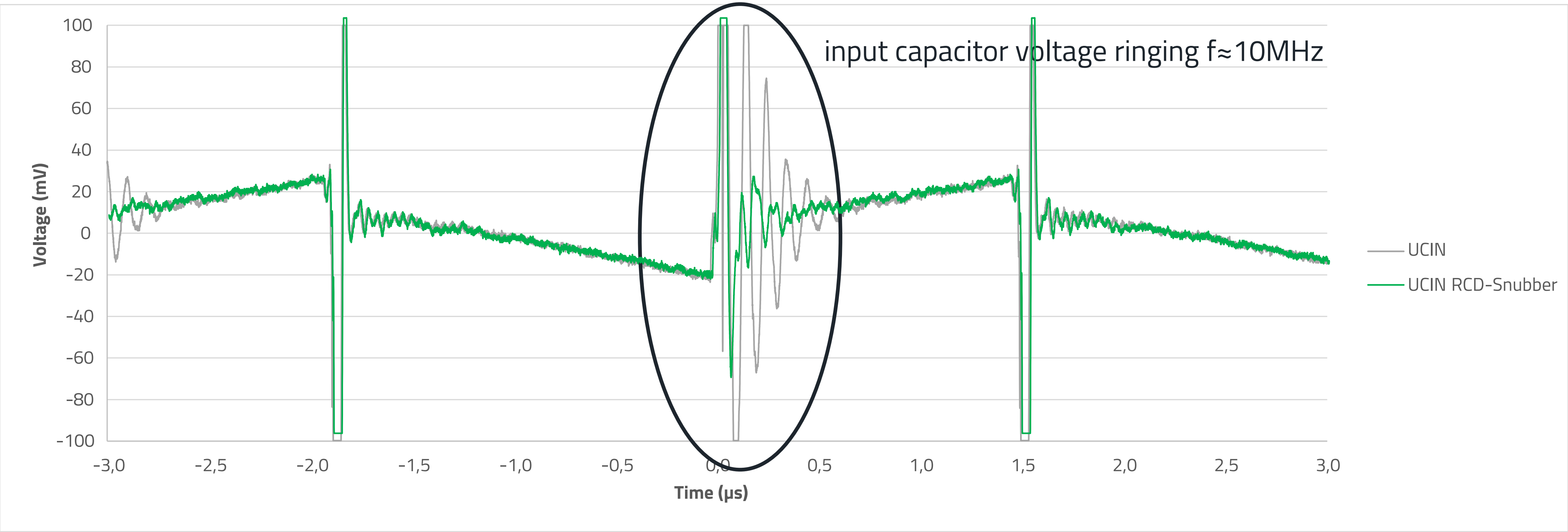
Test#1: Waveforms - Switch node voltage



Test#1: Waveforms - Input capacitor current

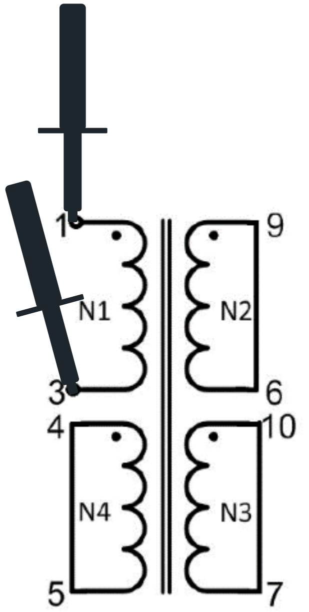


Test#1: Waveforms - Input capacitor voltage ripple

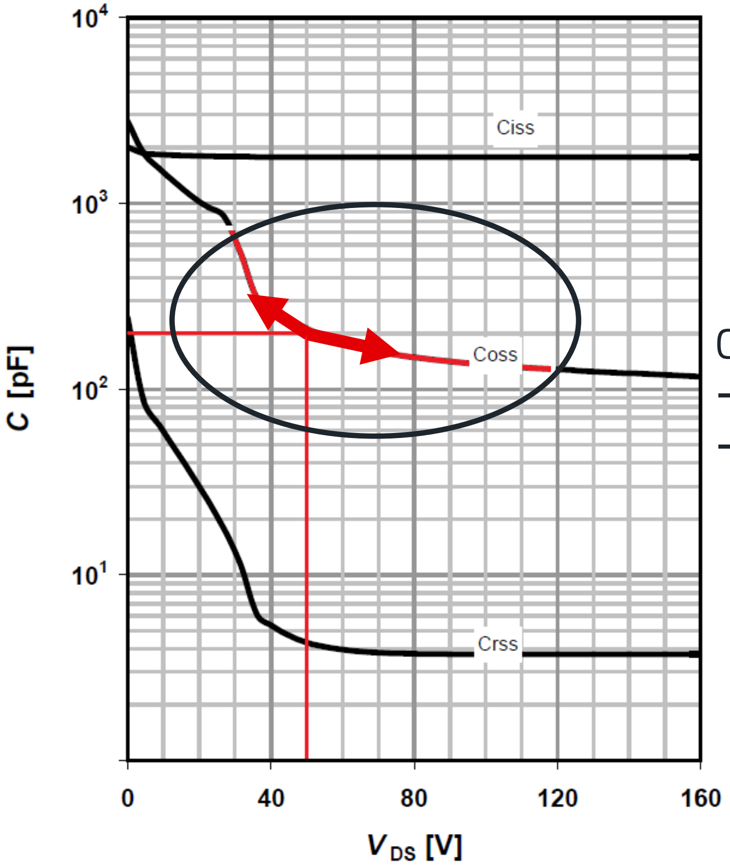


Test#1: Background

- The stray inductance of the transformer and the output capacitance C_{OSS} of the MOSFET (Infineon - IPP320N20) create a resonance circuit:



$$L_{S,Tr} \approx 0{,}4\mu H$$



$C_{OSS} \approx 200pF$?
→ C_{OSS} depending on V_{DS}
→ Spread spectrum

Test#1: Background

Theory

- The stray inductance of the transformer and the output capacitance of the MOSFET create a resonance circuit (Thomson's equation of oscillation):

$$L_{\text{parasitic}} \approx L_{\text{S,Tr}} = 0{,}4\mu H$$

$$C_{\text{parasitic}} \approx C_{\text{OSS}}$$

$$\rightarrow f_{\text{ring}} \approx \frac{1}{2\pi \cdot \sqrt{L_{\text{S,Tr}} \cdot C_{\text{OSS}}}}$$

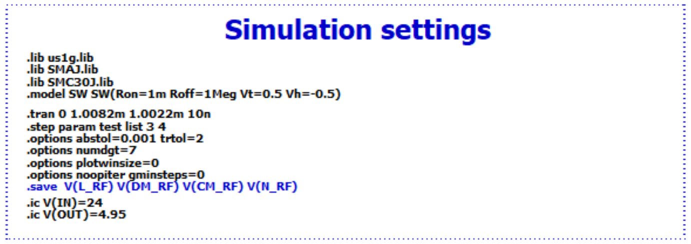
- The output capacitance of the MOSFET in this case is highly voltage dependent (not constant):

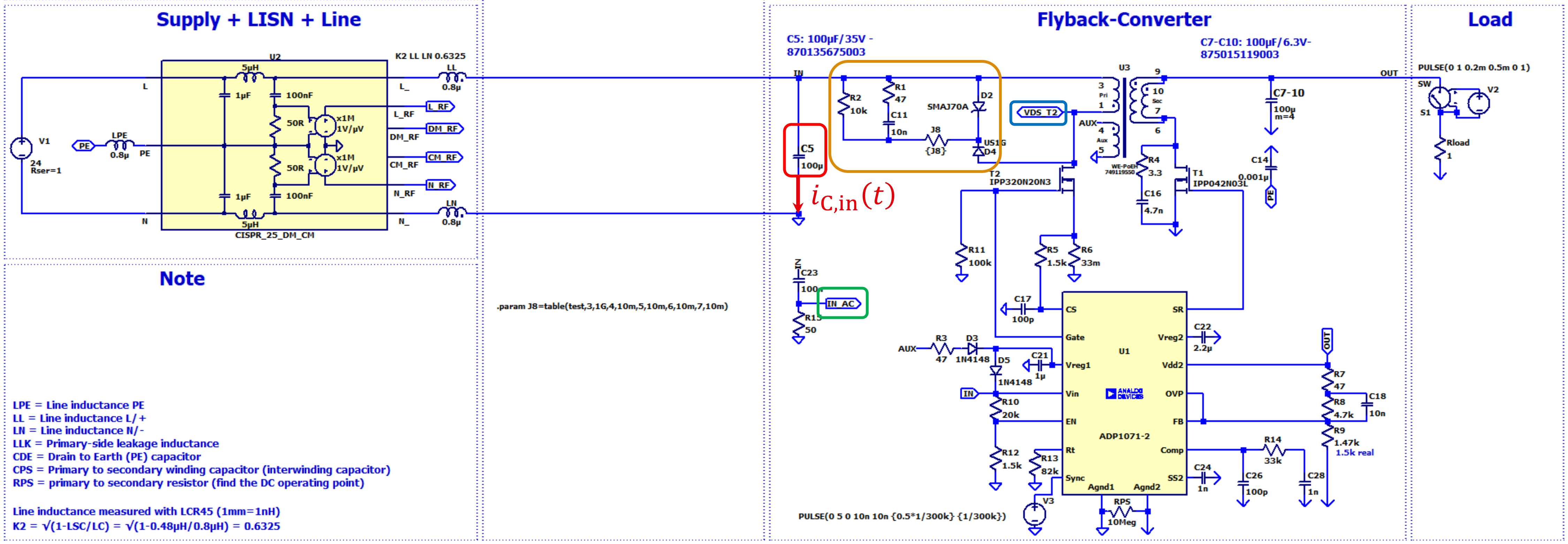
$$\rightarrow \overline{C_{\text{OSS}}} \approx \frac{1}{\left(2\pi f_{\text{ring}}\right)^2 \cdot L_{\text{S,Tr}}} = \frac{1}{(2\pi 10MHz)^2 \cdot 0{,}4\mu H} \approx 633pF$$

Test#1 - Simulation: Simulation\Test1-7\Flyback_EMI_Test1a.asc

Simulation in time domain; influence of the snubber circuit R1, R2, C11, D2, D4

Jumper **J8** as a variable resistor:
.param J8=table(test,3,1G,4,10m)
.step param test list 3 4

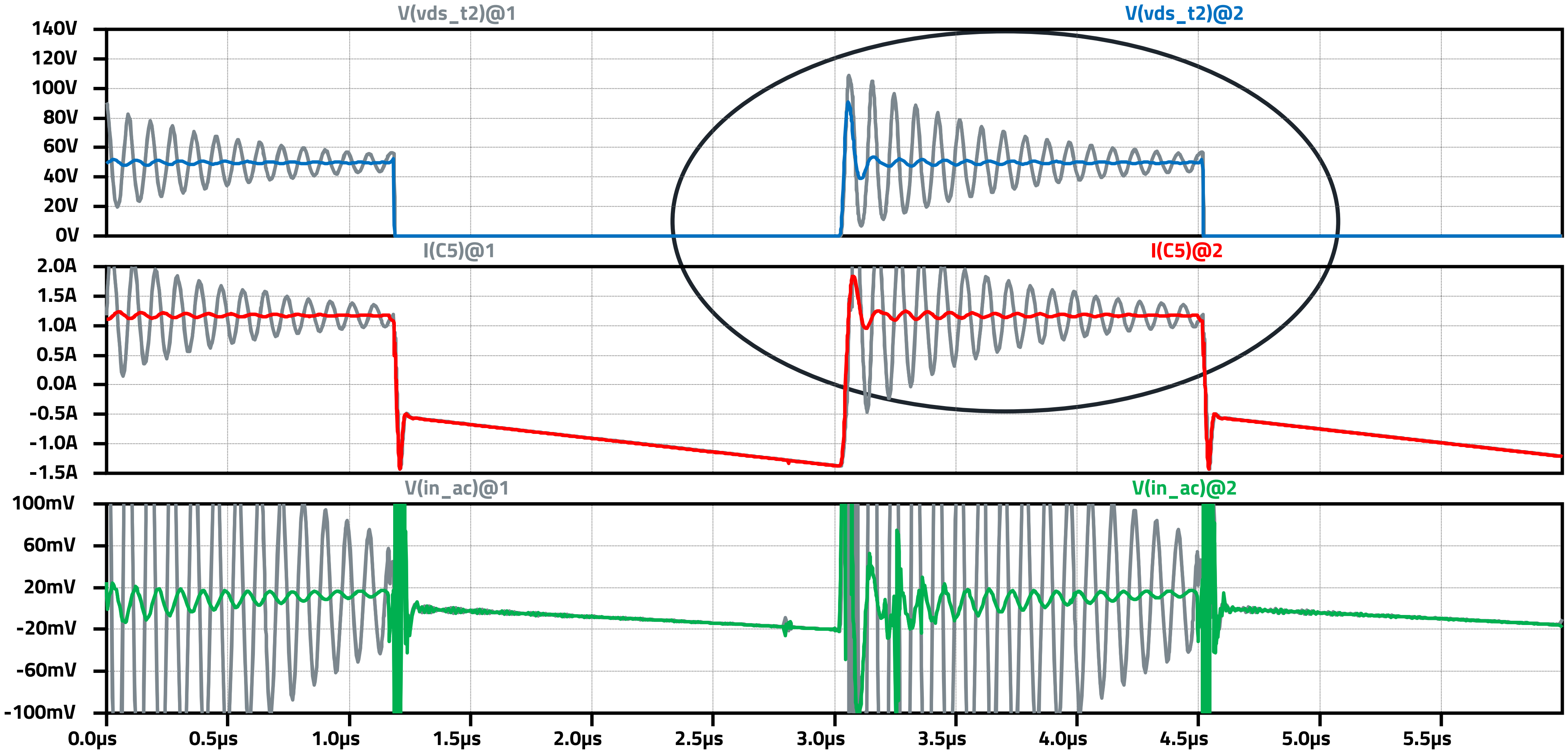




Test#1 - Simulation

[Simulation\Test1-7\Flyback_EMI_Test1a.asc]

Quality of the simulated parasitic oscillating circuit is not realistic!!

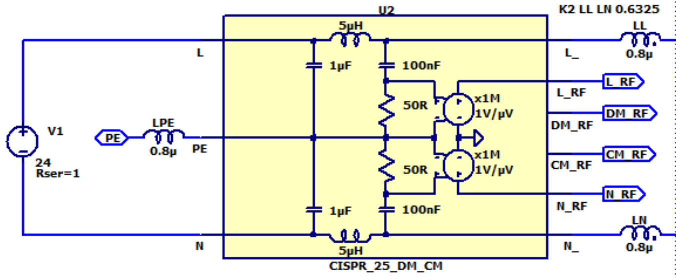


Test#1 - Simulation: Simulation\Test1-7\Flyback_EMI_Test1b.asc

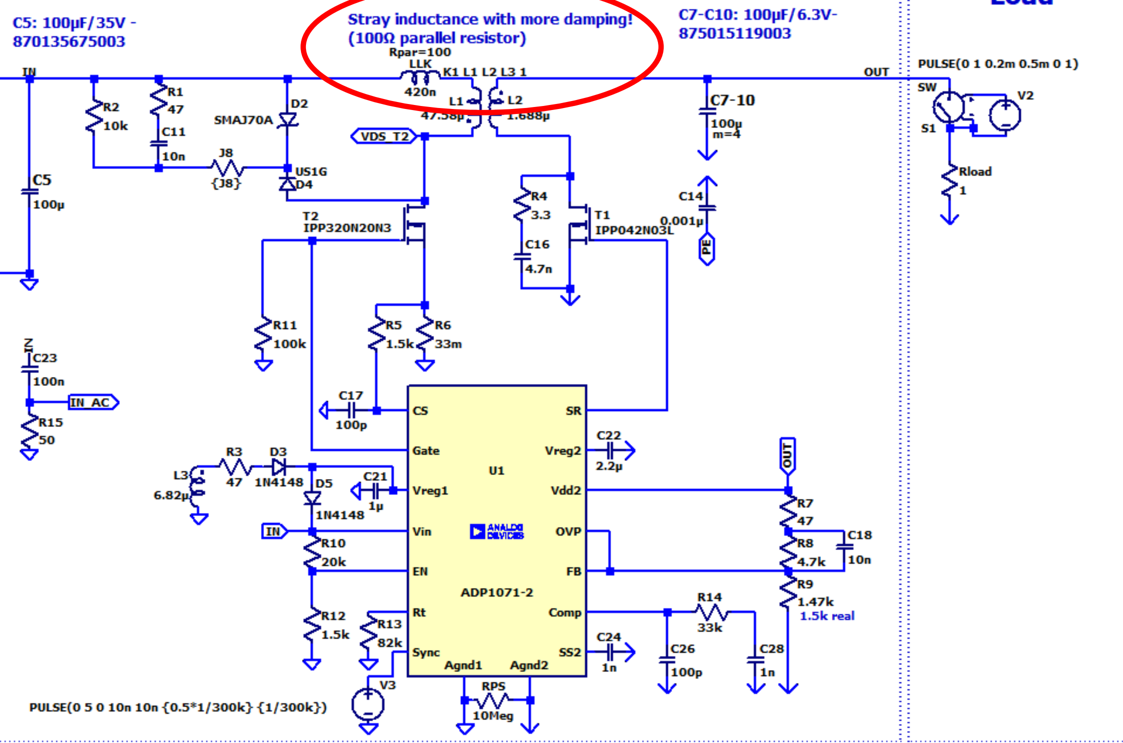
Simulation settings

```
.lib us1g.lib
.lib SMAJ.lib
.lib SMC30J.lib
.model SW SW(Ron=1m Roff=1Meg Vt=0.5 Vh=-0.5)
.tran 0 1.0082m 1.0022m 10n
.step param test list 3 4
.options abstol=0.001 trtol=2
.options numdgt=7
.options plotwinsize=0
.options noopiter gminsteps=0
.save V(L_RF) V(DM_RF) V(CM_RF) V(N_RF)
.ic V(IN)=24
.ic V(OUT)=4.95
```

Supply + LISN + Line




```
.param J8=table(test,3,1G,4,10m,5,10m,6,10m,7,10m)
```



Note

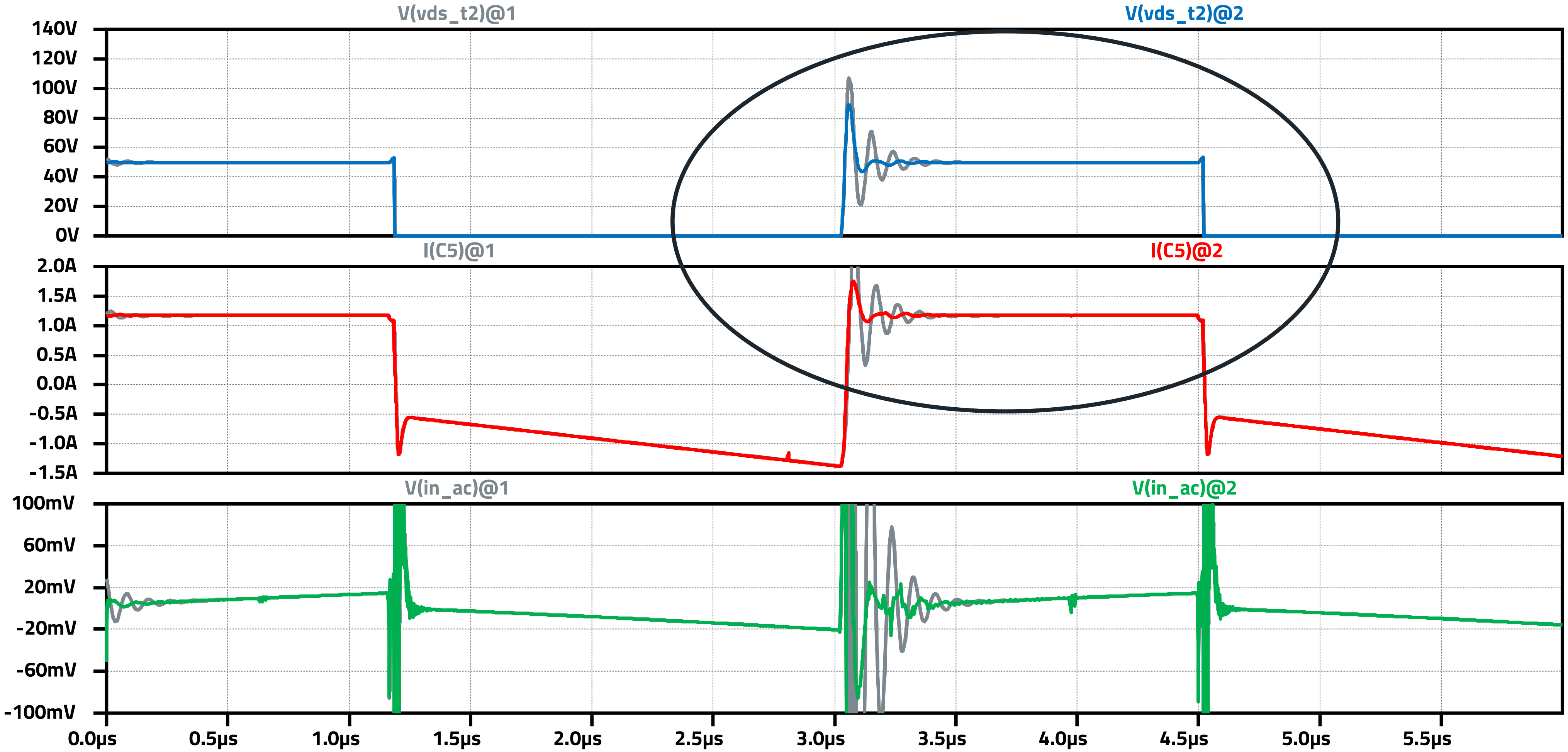
LPE = Line inductance PE
LL = Line inductance L/+
LN = Line inductance N/-
LLK = Primary-side leakage inductance
CDE = Drain to Earth (PE) capacitor
CPS = Primary to secondary winding capacitor (interwinding capacitor)
RPS = primary to secondary resistor (find the DC operating point)

Line inductance measured with LCR45 (1mm=1nH)
$K2 = \sqrt{(1-LSC/LC)} = \sqrt{(1-0.48\mu H/0.8\mu H)} = 0.6325$

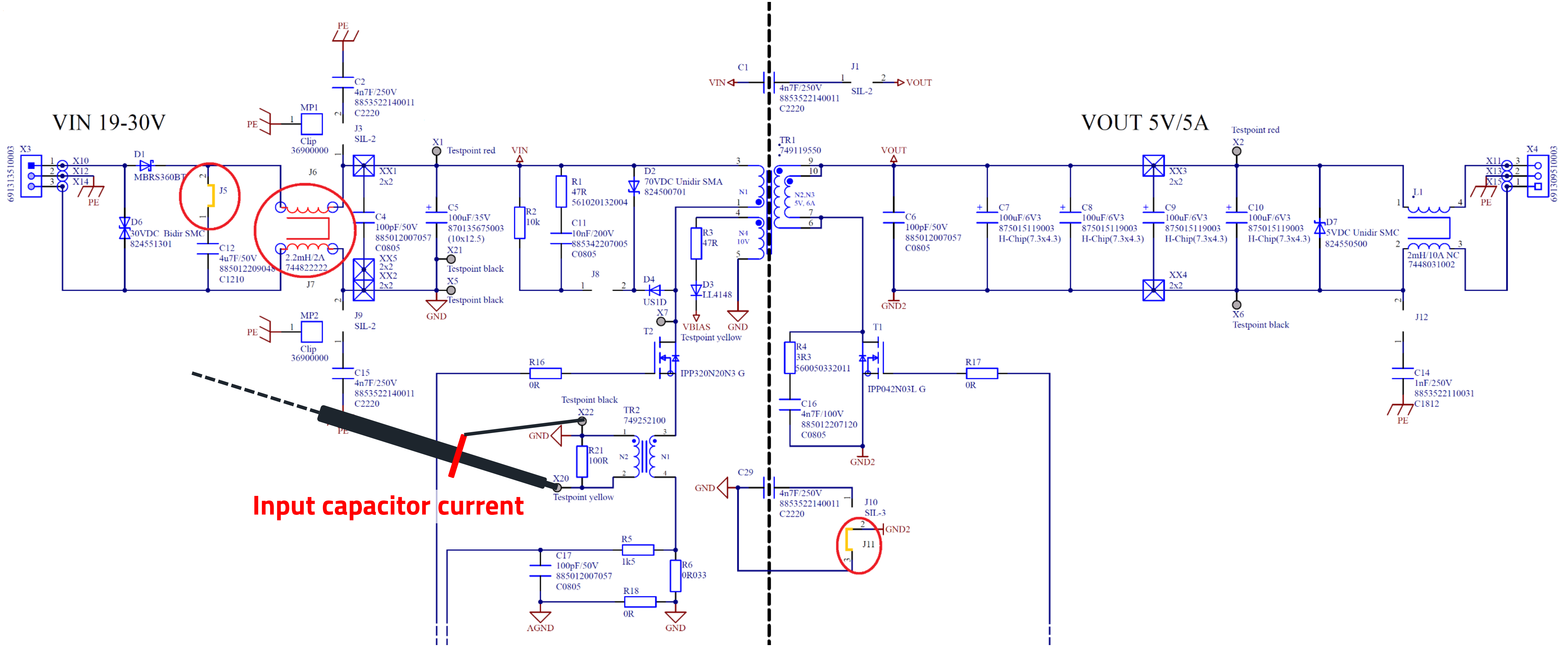
Test#1 - Simulation

Simulation\Test1-7\Flyback_EMI_Test1b.asc

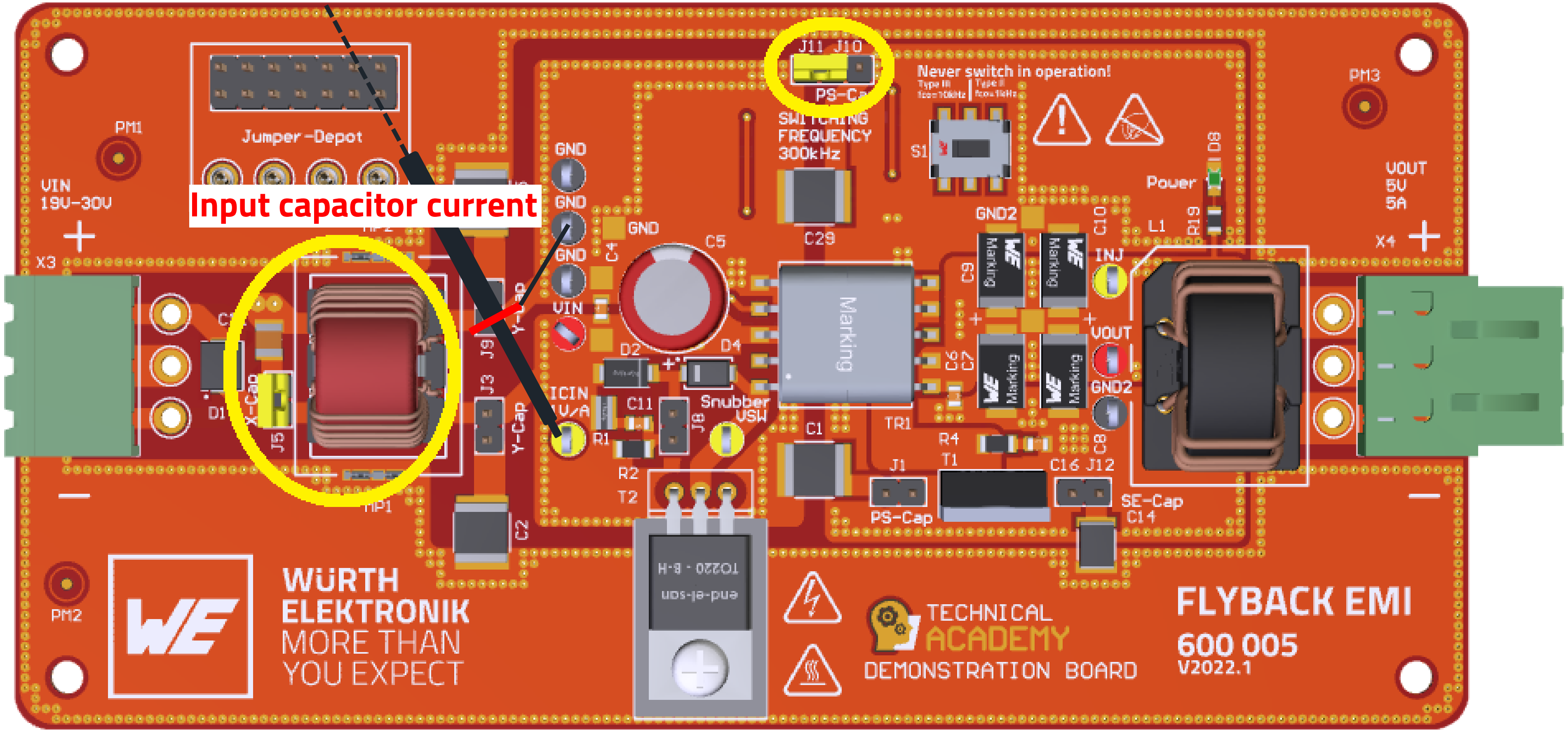
Now the simulated waveforms are nearly exact.



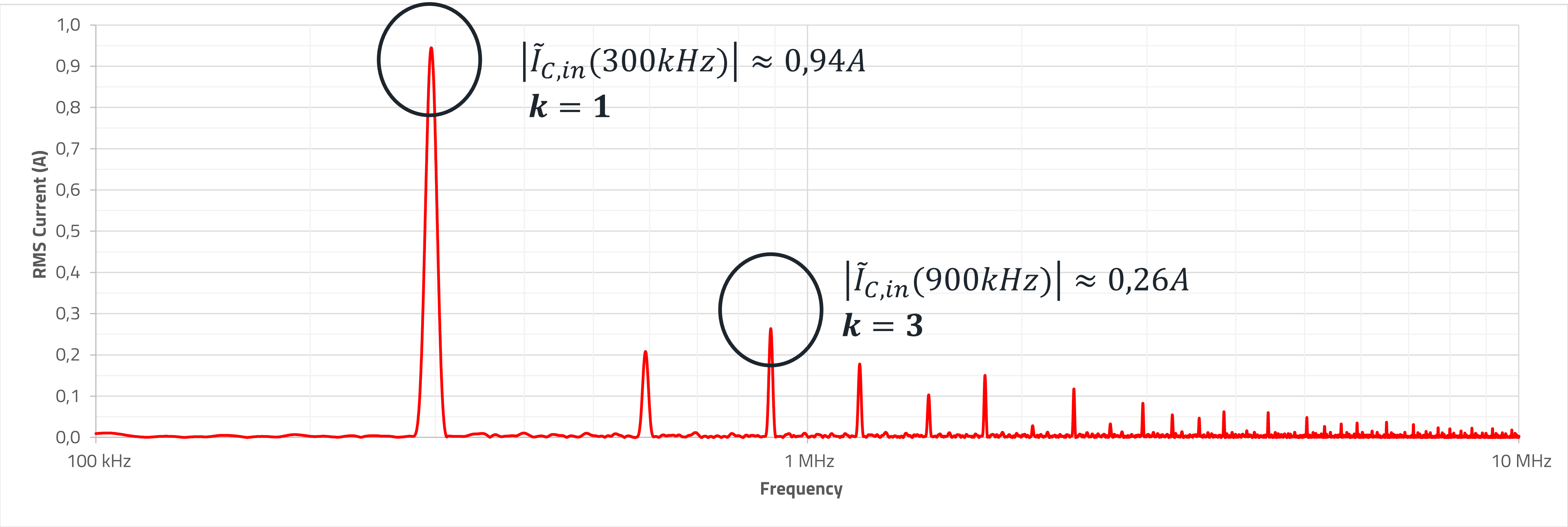
Test#2: Schematic



Test#2: Board configuration

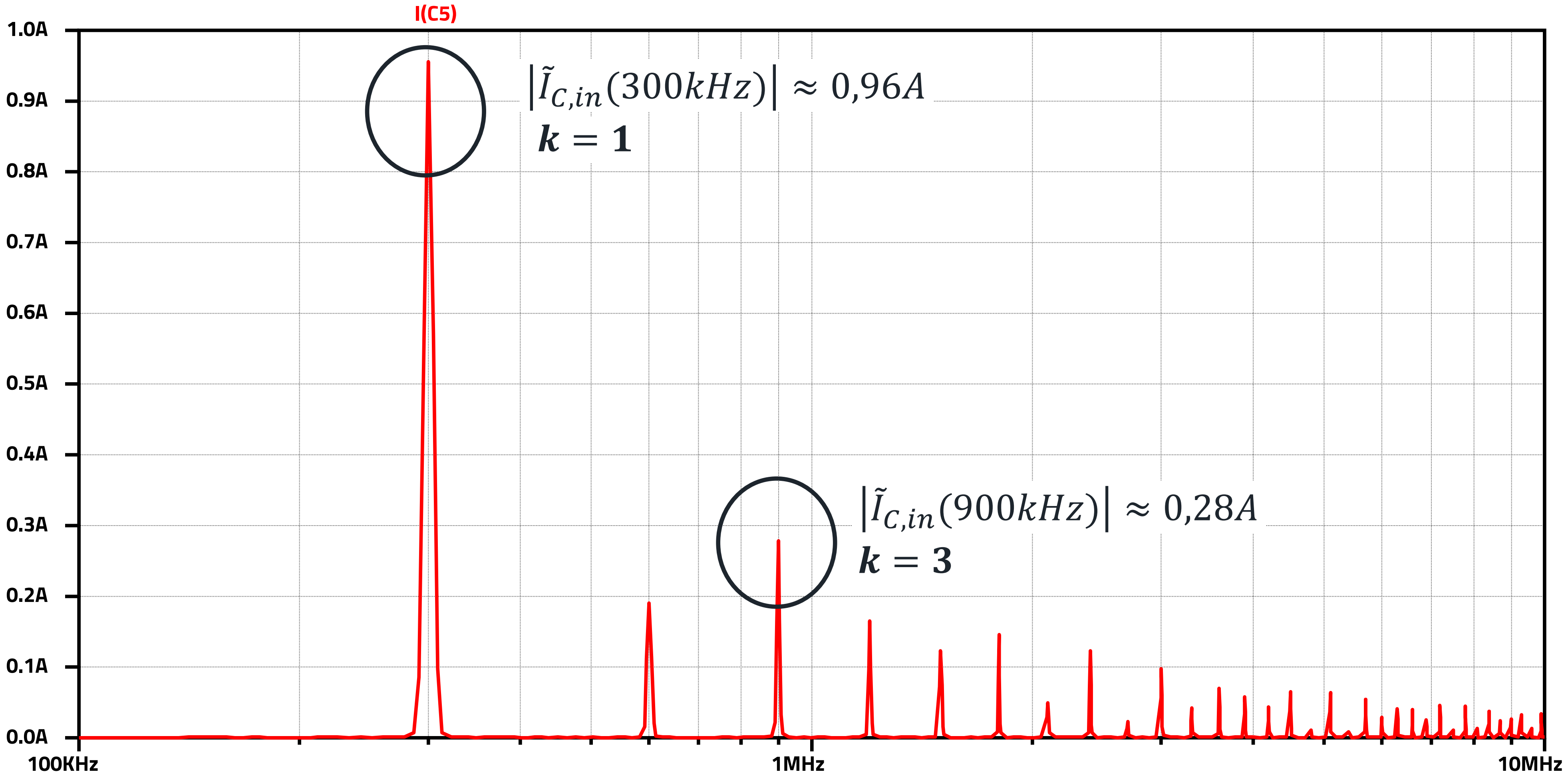


Test#2: FFT of input capacitor current



Test#2 - Simulation

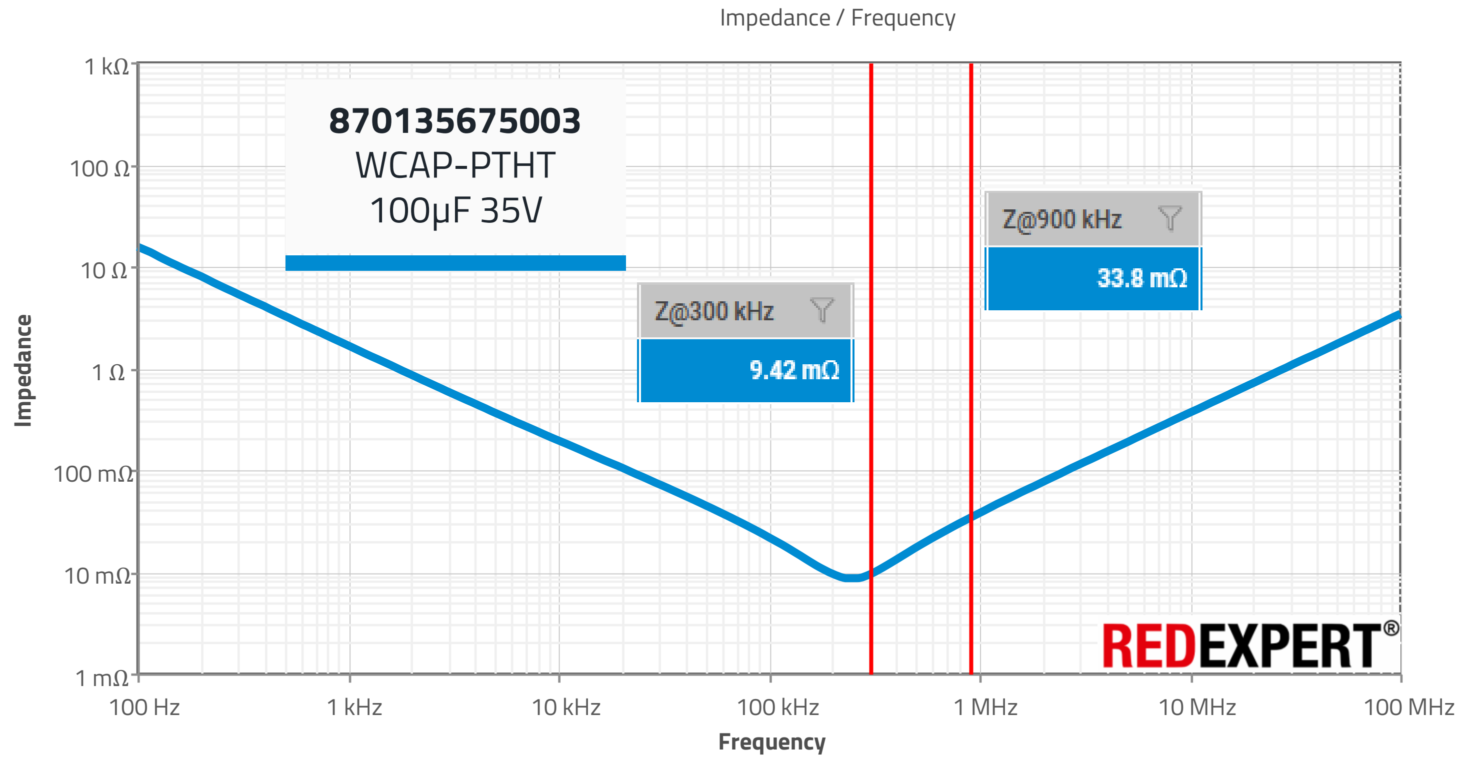
Simulation\Test1-7\Flyback_EMI_Test2.asc



Test#2: Background - EMI

REDEXPERT: Impedance

- Noise is generated by the voltage drop across the impedance of the input capacitor caused by the capacitor current
- Impedance of the input capacitor:



$$\boldsymbol{k = 1:}$$

$$\left|\tilde{U}_{C,in}(300kHz)\right| = \left|Z_{C,in}(300kHz)\right| \cdot \left|\tilde{I}_{C,in}(300kHz)\right|$$
$$= 9{,}42m\Omega \cdot 0{,}94A \approx 8{,}85mV$$

$$8{,}85mV \triangleq 20 \cdot \log\left(\frac{8{,}85mV}{1\mu V}\right) \approx 79dB\mu V$$

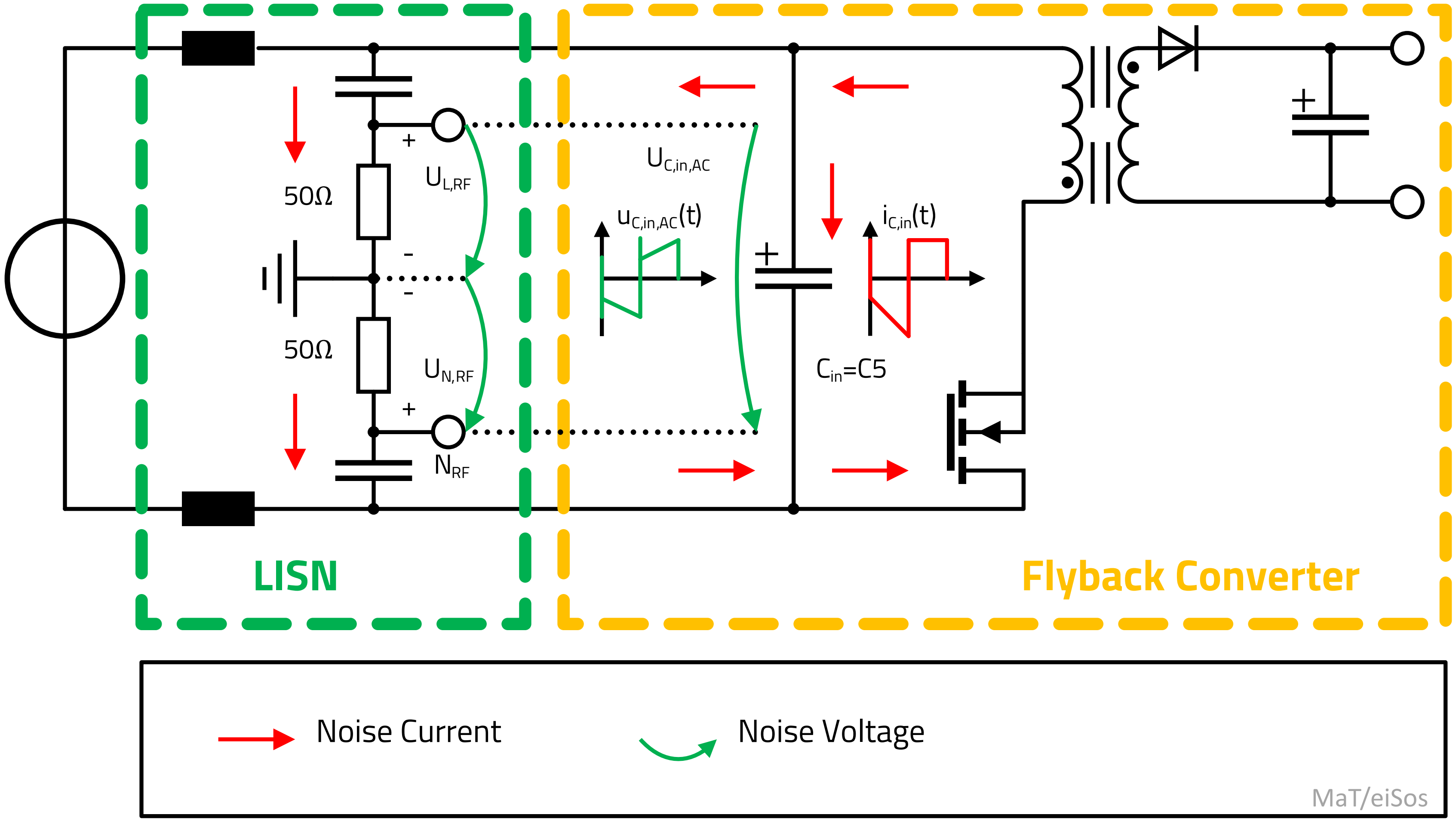
$$\boldsymbol{k = 3:}$$

$$\left|\tilde{U}_{C,in}(900kHz)\right| = \left|Z_{C,in}(900kHz)\right| \cdot \left|\tilde{I}_{C,in}(900kHz)\right|$$
$$= 33{,}8m\Omega \cdot 0{,}26A \approx 8{,}79mV$$

$$8{,}79mV \triangleq 20 \cdot \log\left(\frac{8{,}79mV}{1\mu V}\right) \approx 79dB\mu V$$

Test#2-3: Background - EMI

Theory: Conducted emissions measurement - Symmetrical LISN



$$U_{\mathrm{L,RF}} = U_{\mathrm{N,RF}} = \frac{U_{\mathrm{C,in,AC}}}{2}$$

$$20 \cdot \log\left(\frac{1}{2}\right) \approx -6dB$$

$\boldsymbol{k} = \mathbf{1}$:

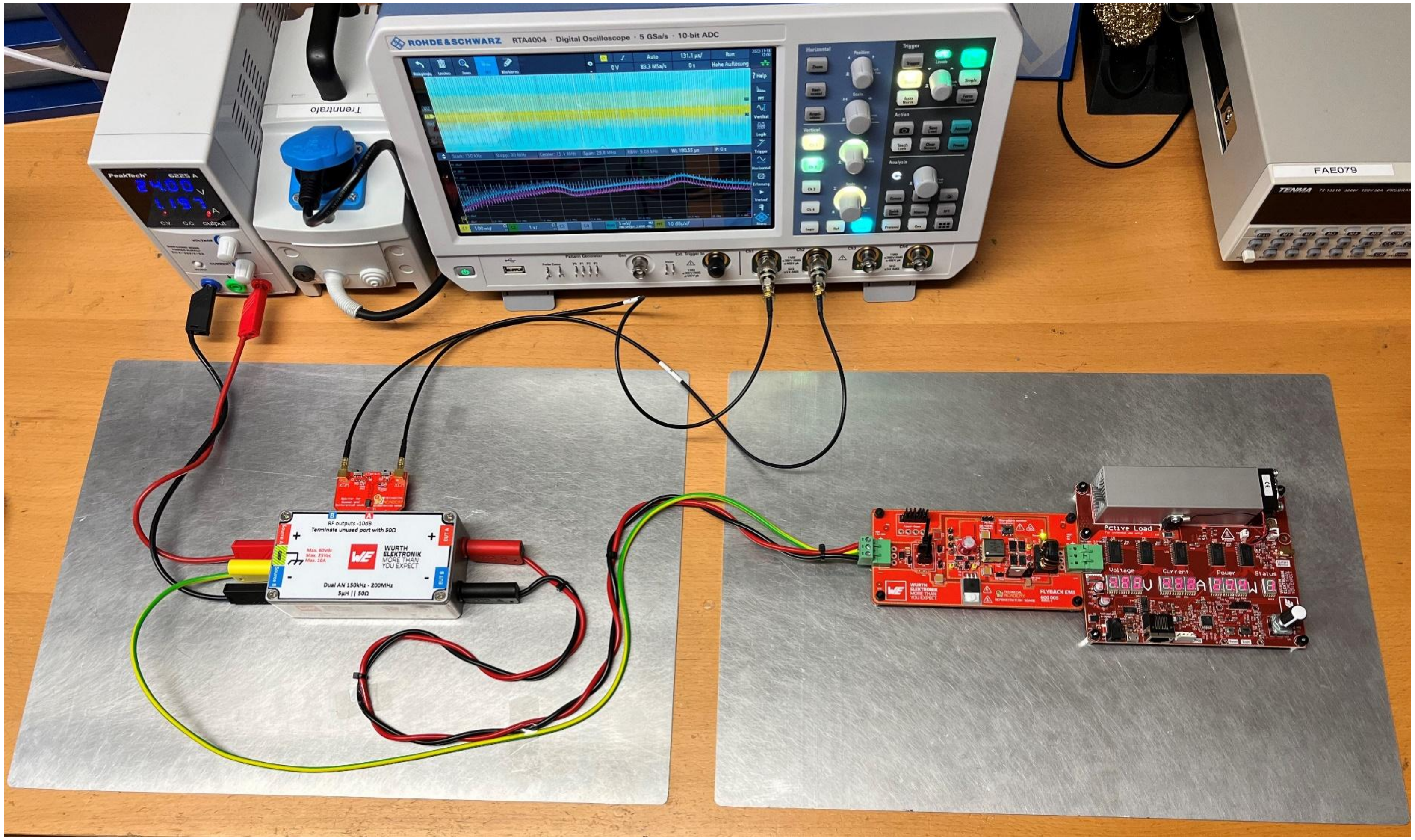
$$|\tilde{U}_{L,RF}(300kHz)| = |\tilde{U}_{C,in}(300kHz)| - 6dB$$
$$= 79dB\mu V \ - 6dB = \mathbf{73dB\mu V}$$

$\boldsymbol{k} = \mathbf{3}$:

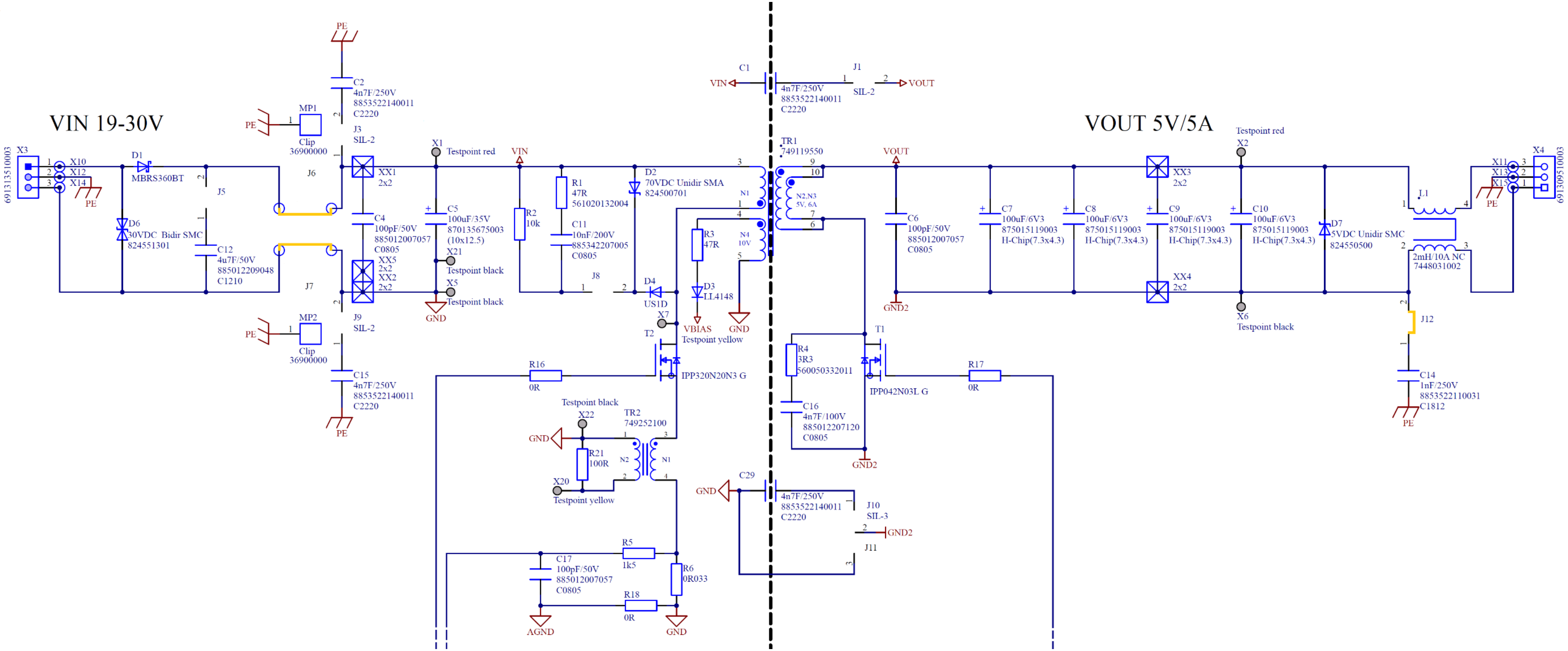
$$|\tilde{U}_{L,RF}(900kHz)| = |\tilde{U}_{C,in}(900kHz)| - 6dB$$
$$= 79dB\mu V \ - 6dB = \mathbf{73dB\mu V}$$

Test#3-7: Conducted emissions - Precompliance

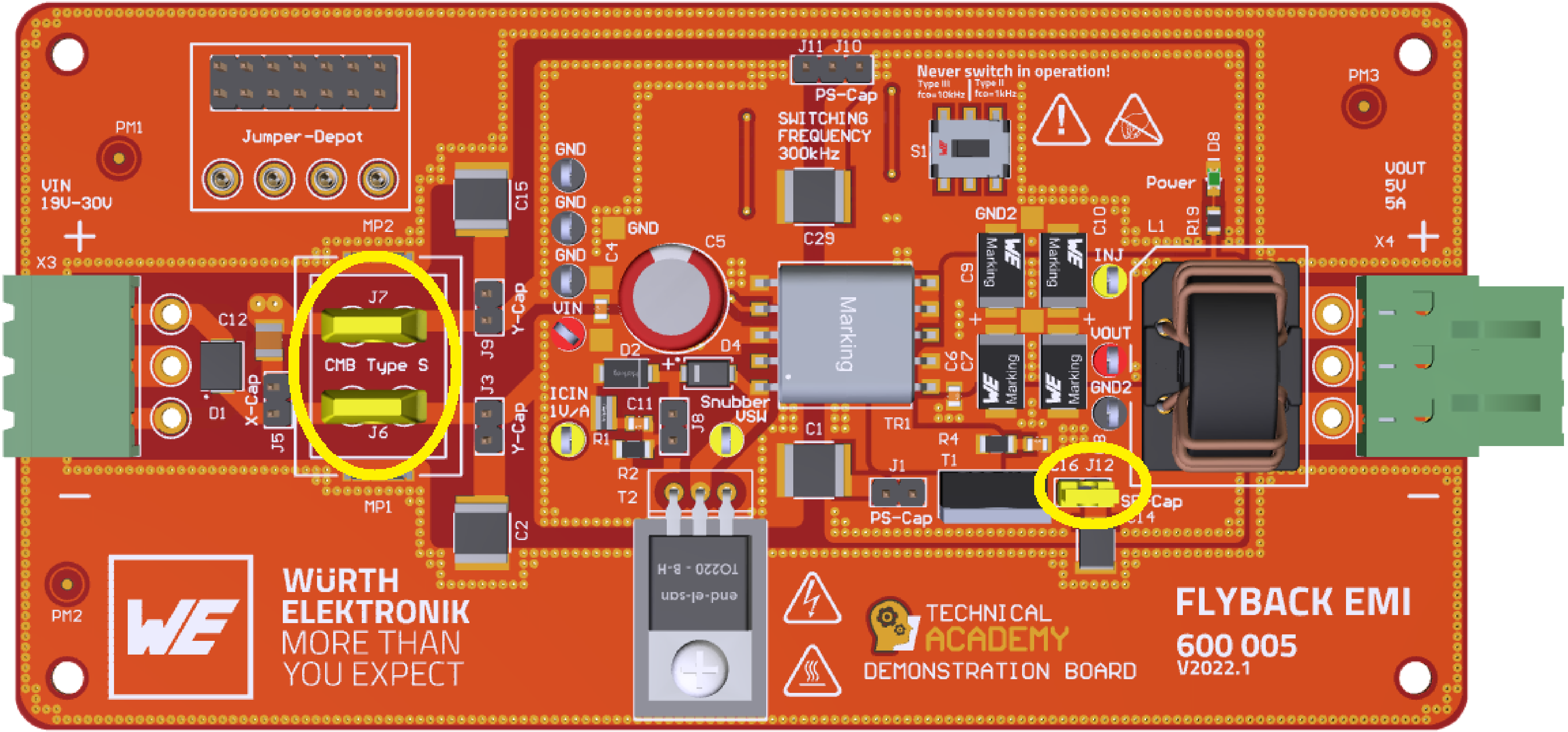
Test setup



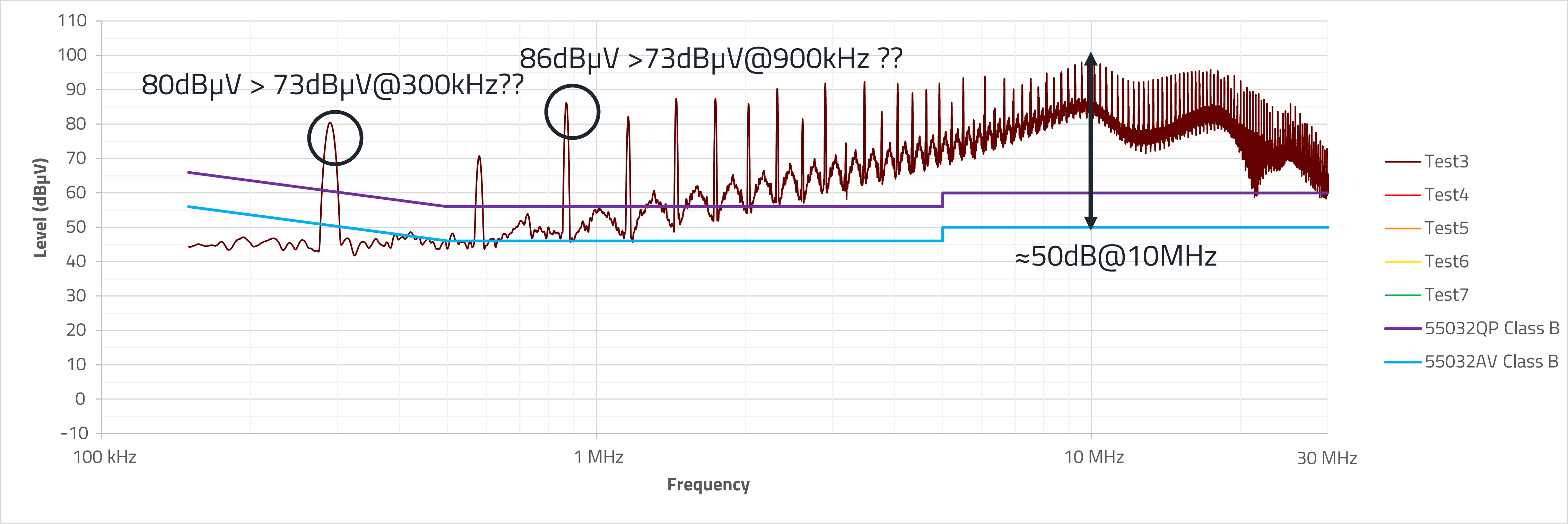
Test#3: Schematic



Test#3: Board configuration



Test#3: Total conducted emissions - Line



Name	Description
Test#3	Reference (no improvement)

Conducted EMI Simulation with LTspice

FFT Analysis

- The FFT (Fast Fourier Transform) is a method of calculating harmonics using a special algorithm.

- It requires that the number of samples N to be analyzed is a power of 2 ($N = 2^x$).

- When you perform a FFT, you're just taking a snapshot of the signal.
  - The snapshot (duration T) should contain complete periods of all your frequencies (signal).

- The FFT simulation uses a sliding time window (FFT window) to make the periodicity of the signal coincide with the time frame (duration T).
  - But a well chosen time frame which contains full periods of the signal is much better.

Conducted EMI Simulation with LTspice

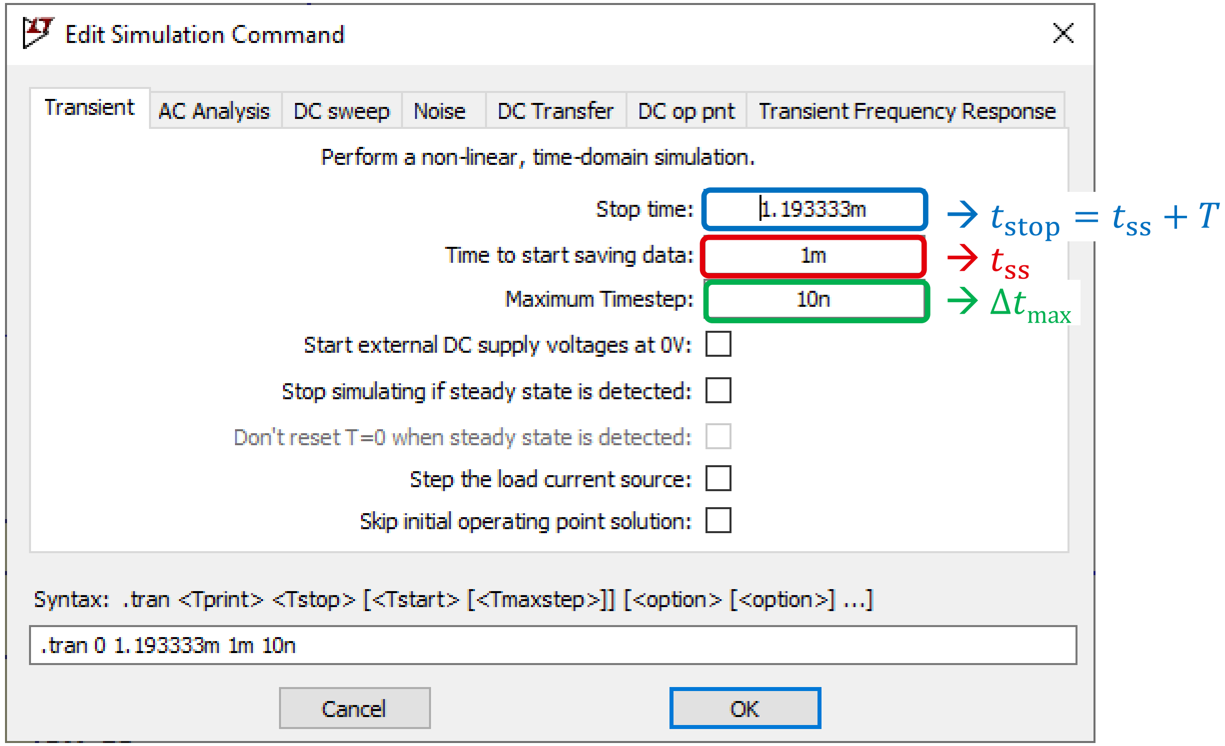
FFT Analysis

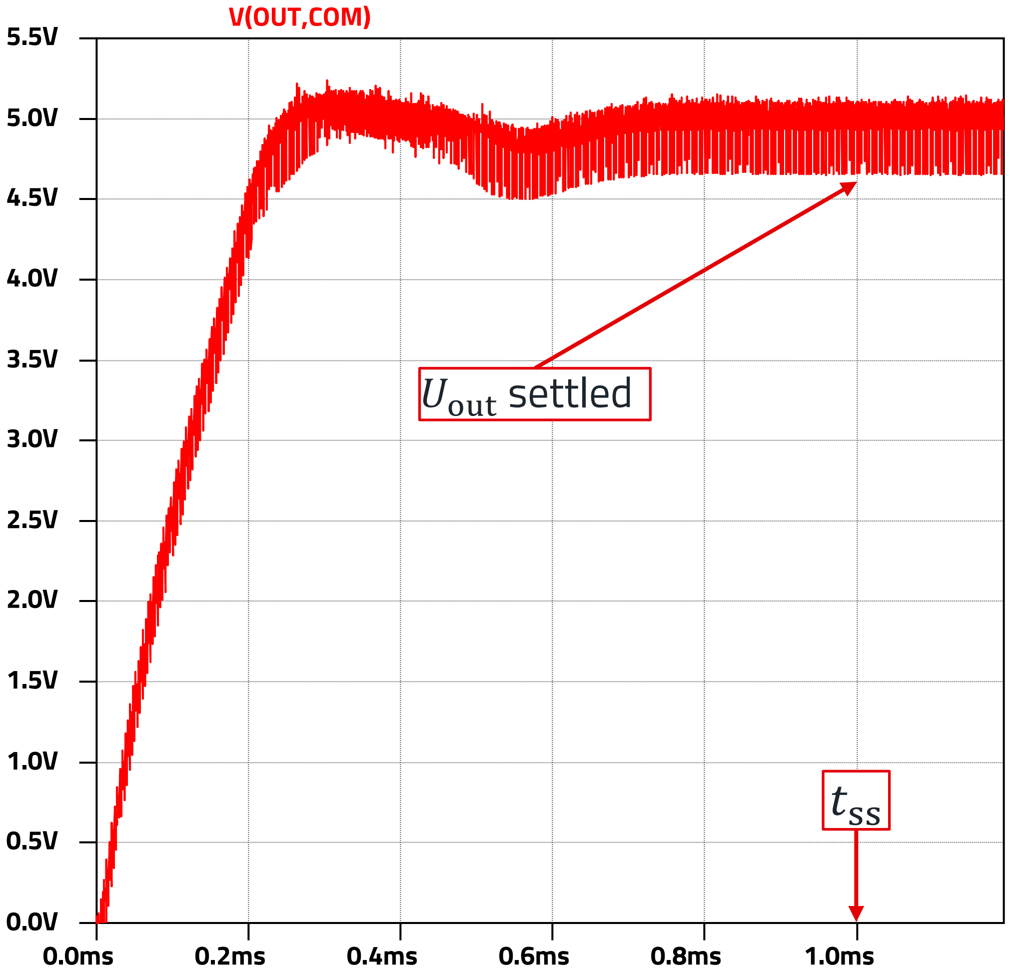
- N= number of points
- Δt= Resolution in the time domain
- F_s= sampling frequency= $1/\Delta t$
- T= Total sampling time= $N \cdot \Delta t = N/F_s$
- Δf= frequency resolution= $1/T = F_s/N$
- B_{3dB}= 3dB resolution bandwidth= $k \cdot F_s/N = k/T$
  - k= Window coefficient (Blackman: 1.74; Hamming: 1.64; Flattop: 3.73; Rectangle: 0.99)
- F_m= Maximum frequency $< F_s/2.56$
  - At least $F_s/2$ (Shannon theorem) and $F_s/2.56$ for $N = 2^x$
- f_{sw}= switching frequency of the converter
- T_{sw}= switching period= $1/f_{sw}$

- $F_m = 30\text{MHz}$ (CISPR 32, EN 55032)
  - $\Delta t_{max} < 1/F_s = 1/(2.56 \cdot F_m) = 1/(2.56 \cdot 30\text{MHz}) \approx 13\text{ns}$ → Selected: 10ns
- $B_{3dB} = 9\text{kHz}$ (CISPR band B)
- Window = Blackman (highest amplitude accuracy)
- $T = k/B_{3dB} = 1.74/9\text{kHz} = 193.33\mu\text{s}$
- Number of periods: $n = T \cdot f_{sw} = 58$ → Perfect!

Conducted EMI Simulation with LTspice

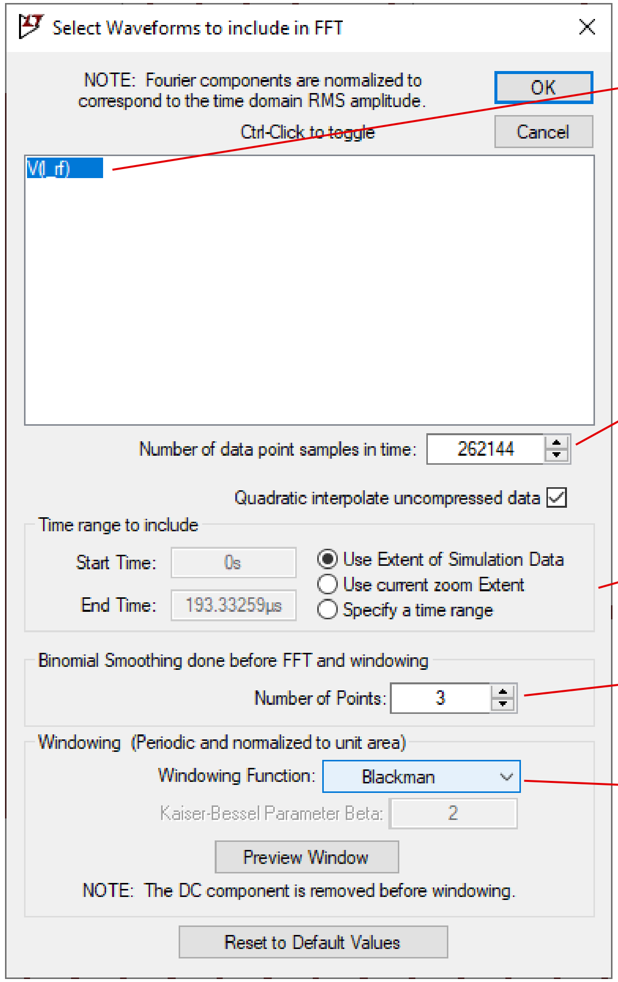
Simulation Command





Conducted EMI Simulation with LTspice

View → FFT (FFT directive)



- Signal to analyze
  - By default, LTspice scales the voltage in dBV
  - V(l_rf) is already divided by 1µV → result in dBµV
- Number of points in the time domain
  - Greater than 100000 (required minimum)
  - Power of two (here: 2^{18})
  - In principle, the standard value is ok
- Time section already defined by the simulation call (.tran 0 1.93333m 1m 10n)
- Smoothing of data values before FFT and windowing
  - Recommendation: 3 or 5 points
- Window function
  - Blackman for the highest amplitude accuracy

Conducted EMI Simulation with LTspice

Limit lines in LTspice using the plot file: [Limit_lines_calculator\LTspice_limit_lines_calculator_EN55032AV.xlsx](Limit_lines_calculator\LTspice_limit_lines_calculator_EN55032AV.xlsx)

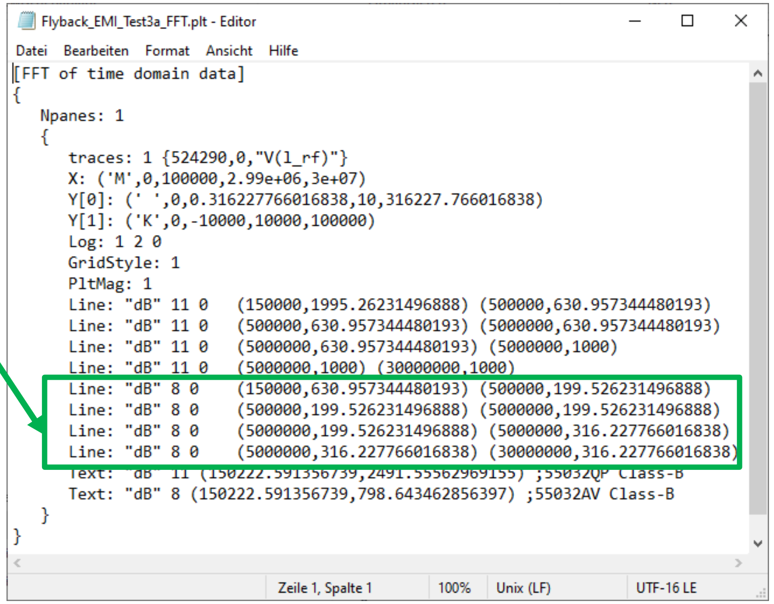
Include limit lines in the output graphic

Editing the **plot settings** file (*.plt) with a text editor

Generate the line definition using the Excel file **LTspice_limit_lines_calculator_EN55032AV.xlsx**

Line	Start	End	Amp dBµV start	Amp dBµV stop	Line def for LTSPICE	
1	150000	500000	56	46	Line: "dB" 8 0	(150000,630.957344480193) (500000,199.526231496888)
2	500000	5000000	46	46	Line: "dB" 8 0	(500000,199.526231496888) (5000000,199.526231496888)
3	5000000	5000000	46	50	Line: "dB" 8 0	(5000000,199.526231496888) (5000000,316.227766016838)
4	5000000	3E+07	50	50	Line: "dB" 8 0	(5000000,316.227766016838) (30000000,316.227766016838)

Definition of support points Cells to copy



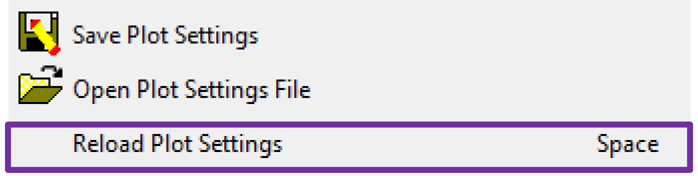

```
[FFT of time domain data]
{
   Npanes: 1
   {
      traces: 1 {524290,0,"V(l_rf)"}
      X: ('M',0,100000,2.99e+06,3e+07)
      Y[0]: (' ',0,0.316227766016838,10,316227.766016838)
      Y[1]: ('K',0,-10000,10000,100000)
      Log: 1 2 0
      GridStyle: 1
      PltMag: 1
      Line: "dB" 11 0   (150000,1995.26231496888) (500000,630.957344480193)
      Line: "dB" 11 0   (500000,630.957344480193) (5000000,630.957344480193)
      Line: "dB" 11 0   (5000000,630.957344480193) (5000000,1000)
      Line: "dB" 11 0   (5000000,1000) (30000000,1000)
      Line: "dB" 8 0    (150000,630.957344480193) (500000,199.526231496888)
      Line: "dB" 8 0    (500000,199.526231496888) (5000000,199.526231496888)
      Line: "dB" 8 0    (5000000,199.526231496888) (5000000,316.227766016838)
      Line: "dB" 8 0    (5000000,316.227766016838) (30000000,316.227766016838)
      Text: "dB" 11 (150222.591356739,2491.55562969155) ;55032QP Class-B
      Text: "dB" 8 (150222.591356739,798.643462856397) ;55032AV Class-B
   }
}
```

Information:

- "dB" = vertical scaling
- 8 = 8th color in the color palette that starts with (default).
- 0 = line style (solid)

Text can be freely placed in the diagram

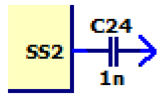
Reload definition: **Space**



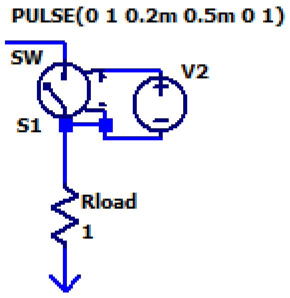
Conducted EMI Simulation with LTspice

Tips and Tricks

- Tricks to speed up simulation and increase accuracy:
  1. Reduce the startup time of the switching converter
     - Reduce the size of the soft start capacitor
     - The ADP1071-2 device has two soft start mechanisms.
       - In the simulation, the capacitor C24 is reduced from a real 1µF to 1nF.
       - The pull-down resistor R11 on the FET gate, which controls the open loop soft start, is increased from 10kΩ to 100kΩ .



  2. Delay switching on the load (here: 0.2ms)
     - Switch model with smooth transition between on and off
       .model SW SW(Ron=1m Roff=1Meg Vt=0.5 Vh=-0.5)



  3. Set initial conditions:
     - Voltage across input capacitor C5: .ic V(IN)=24
     - Output voltage: .ic V(OUT)=4.95

.ic V(OUT)=4.95

Conducted EMI Simulation with LTspice

Tips and Tricks

4. Increase SPICE tolerance:
   - Transient Error Tolerance (.options trtol=7)
     - Default: 1
     - Most commercial SPICE programs: 7
     - Value smaller → Fewer artifacts, but slow
     - Value larger → Faster, but with artifacts

   - Absolute Current Tolerance (.options abstol=0.01)
     - Defines the smallest current amplitude in a simulation run
     - Currents smaller than this value are ignored when checking convergence
     - 10mA is still okay for EMI simulations, as the noise level increases slightly, but the simulation speed increases significantly
     - For switching regulator simulations in the time domain, a value of 1nA should be used

Conducted EMI Simulation with LTspice

Tips and Tricks

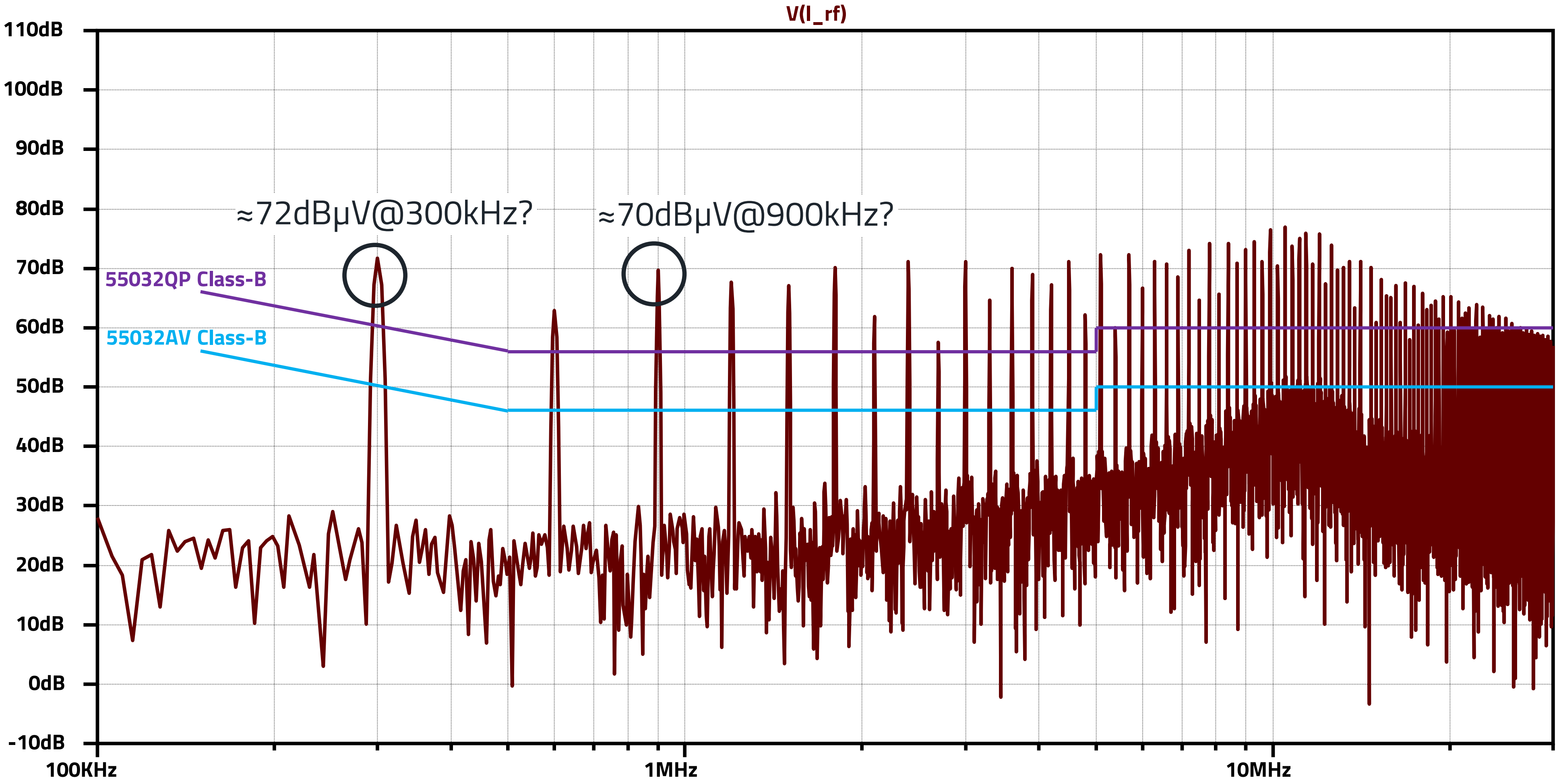
5. Increase the precision of number representation (.options numdgt=7)
   - Double precision arithmetic

6. Turn off lossy data compression (.options plotwinsize=0)

7. Save only the signals that are interesting (.save V(L_RF) V(DM_RF) V(CM_RF) V(N_RF))

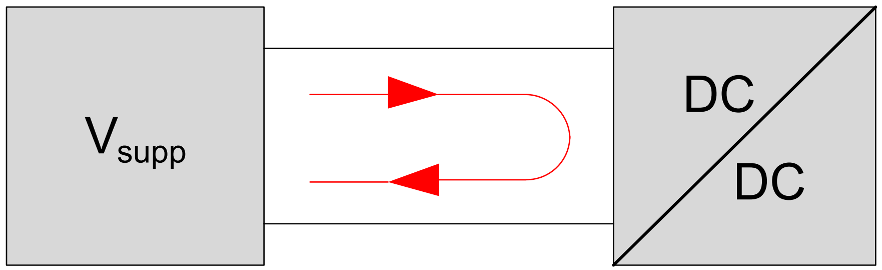
Test#3a: Simulation- Total conducted emissions - Line

Simulation\Test1-7\Flyback_EMI_Test3a_FFT.asc

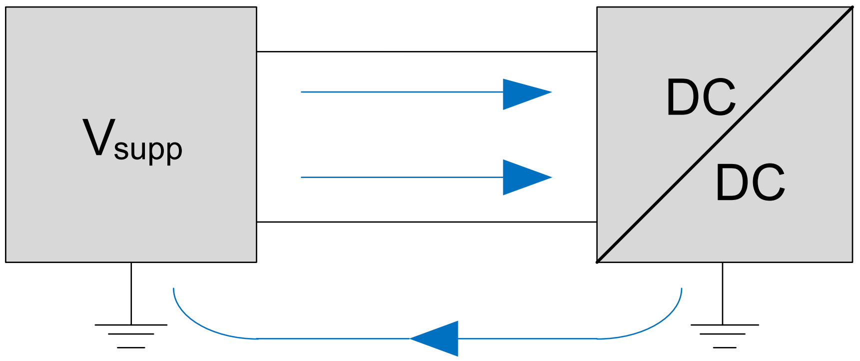


Test#3: Background - Noise categories

Theory: Noise categories



Differential Mode



Common Mode

Test#3: Background - Noise categories

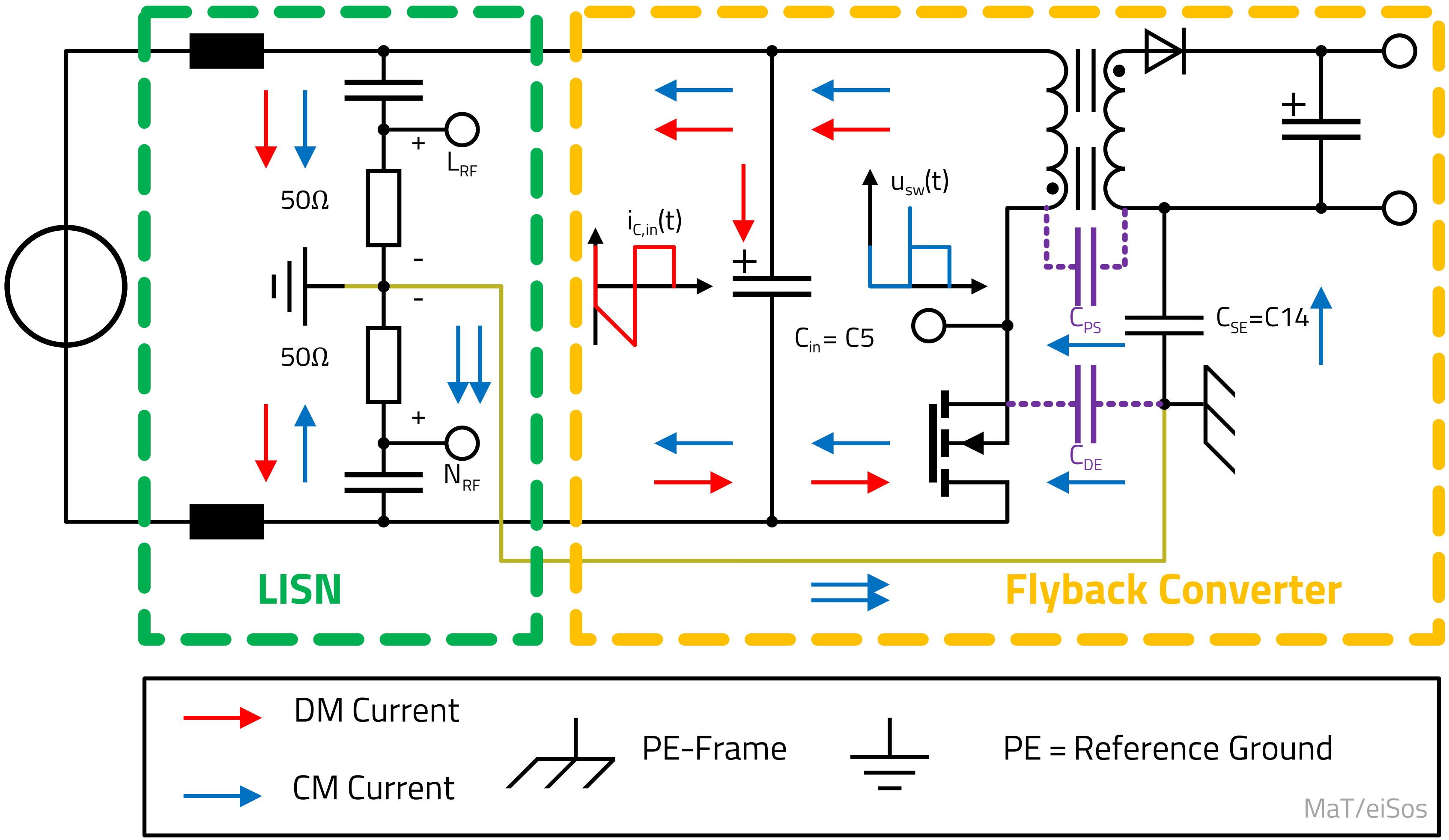
Theory: Noise categories

- **Differential mode currents**
  - Current path as in circuit diagram
  - Easy to follow paths
  - Return current path very close
  - Relatively large currents
  - Filters with LC, π, T topologies

- **Common mode currents**
  - Current path unexpected
  - Current via parasitic paths
  - Return current path very large
  - Relatively small currents (µA)
  - Filtering with CMC and Y-Caps

Test#3: Background - Noise categories

Theory: DM and CM noise paths in a flyback converter



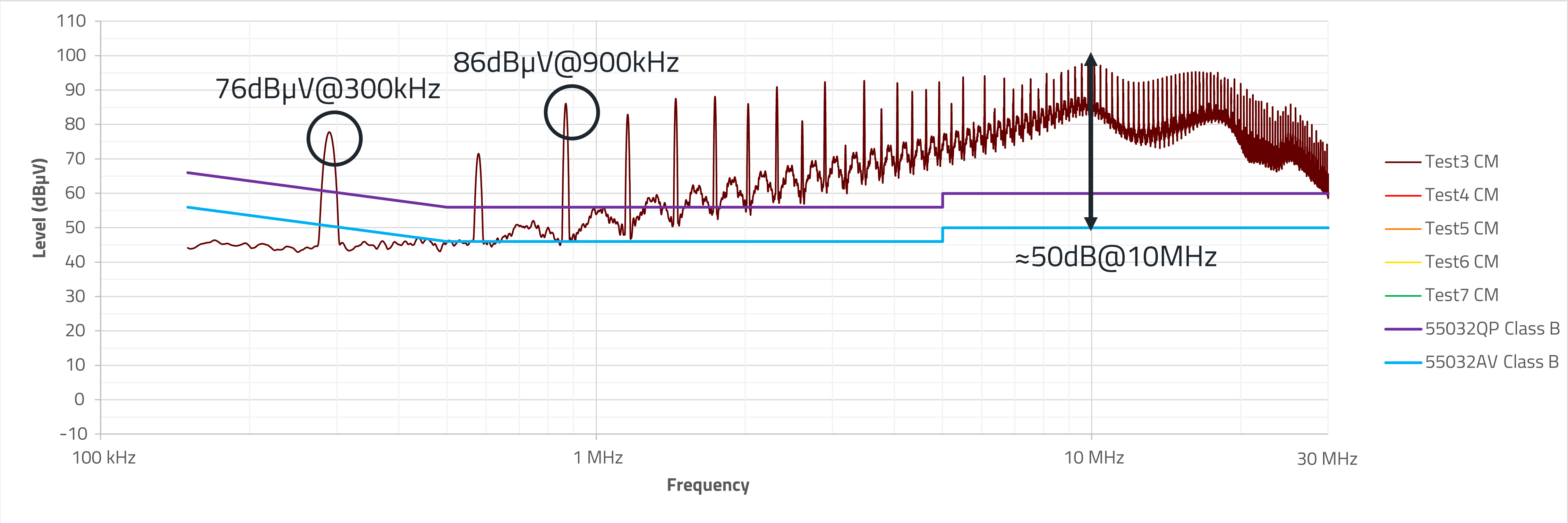
$$U_{L,RF} = U_{CM} + \frac{1}{2} U_{DM}$$

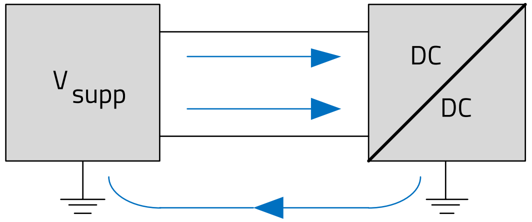
$$U_{N,RF} = U_{CM} - \frac{1}{2} U_{DM}$$

$$U_{DM} = U_{L,RF} - U_{N,RF}$$

$$U_{CM} = \frac{U_{L,RF} + U_{N,RF}}{2}$$

Test#3: Conducted emissions - Common mode

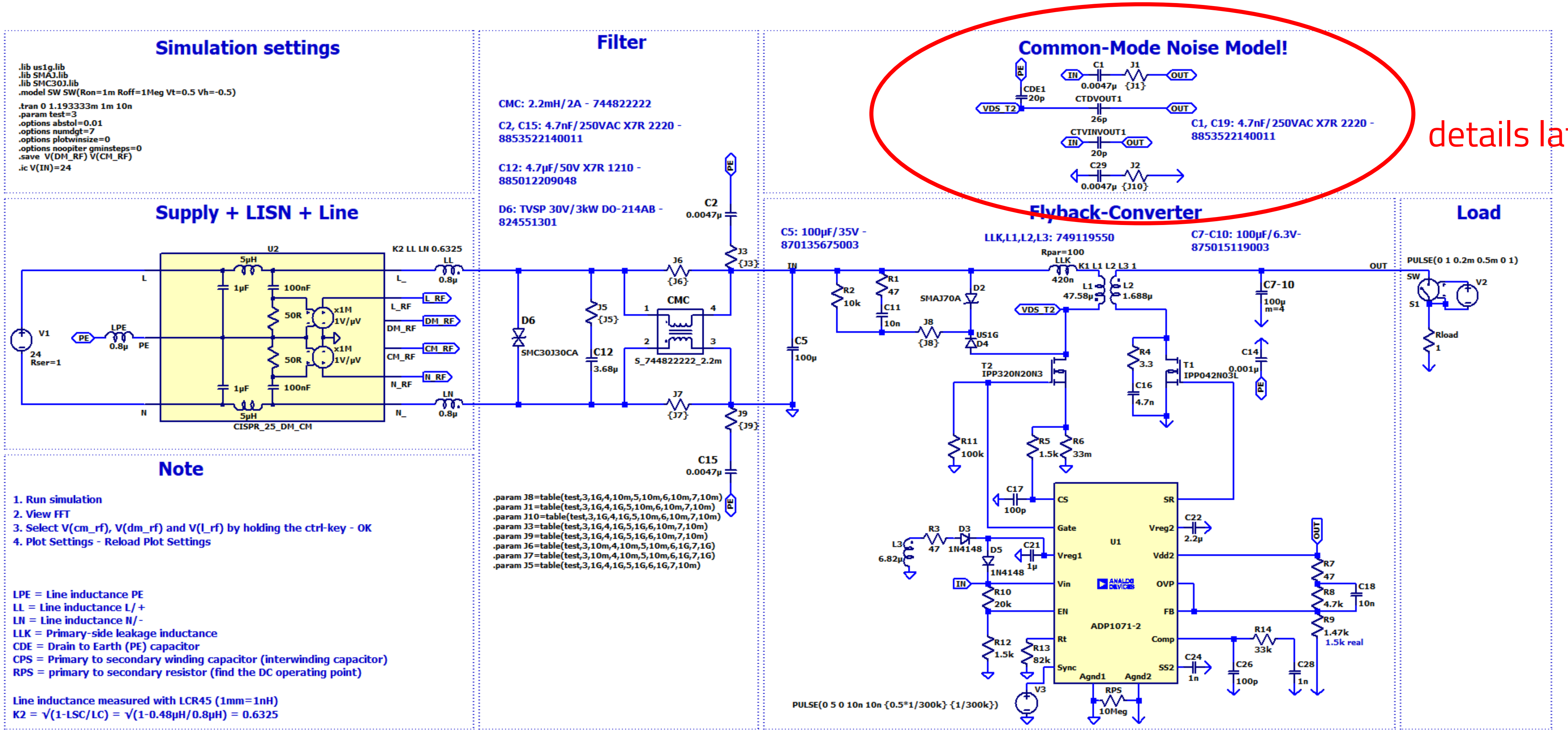




Common Mode

Name	Description
Test#3	Reference (no improvement)

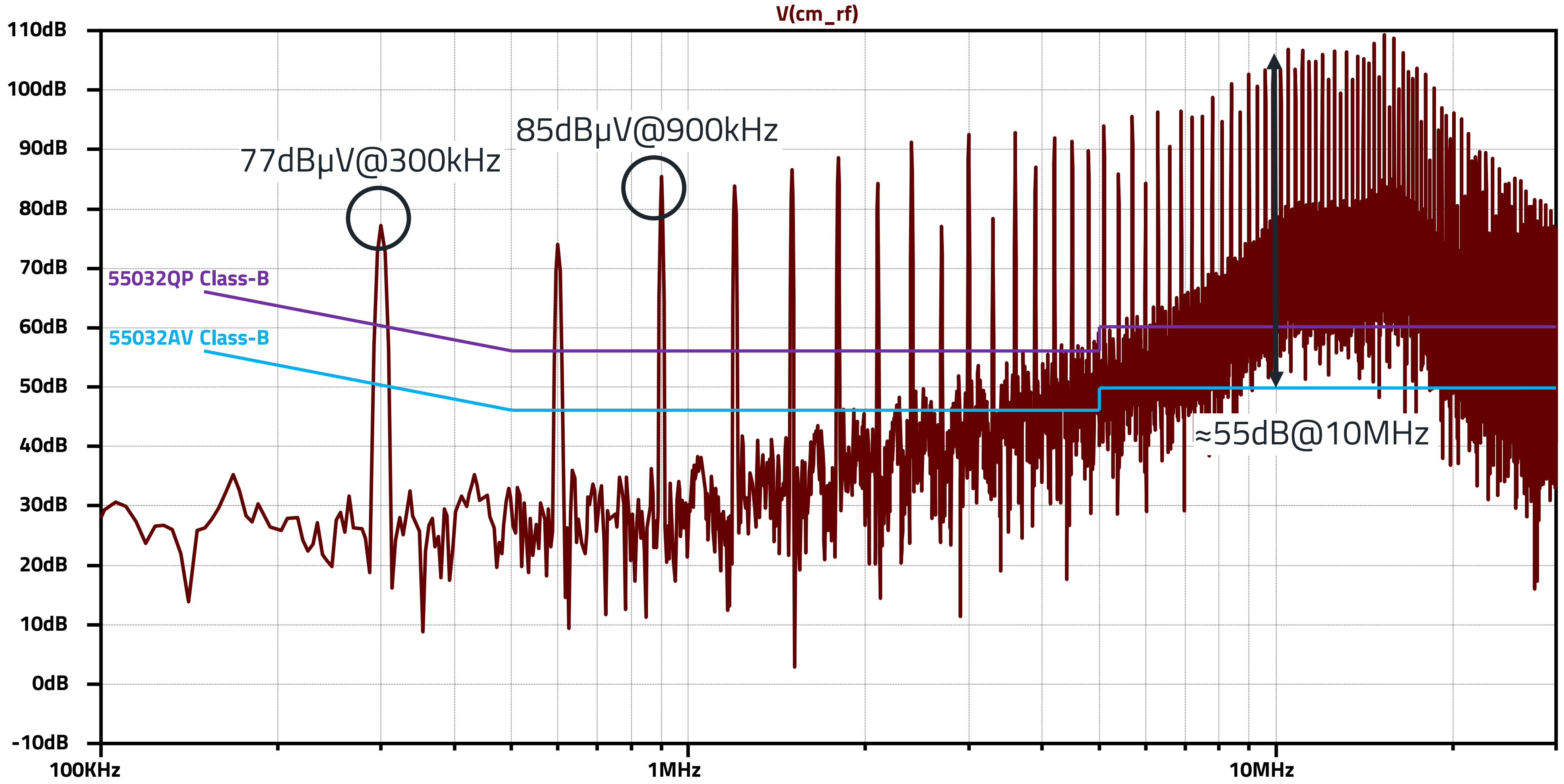
Test#3b - Simulation: Simulation\Test1-7\Flyback_EMI_Test3b_FFT.asc



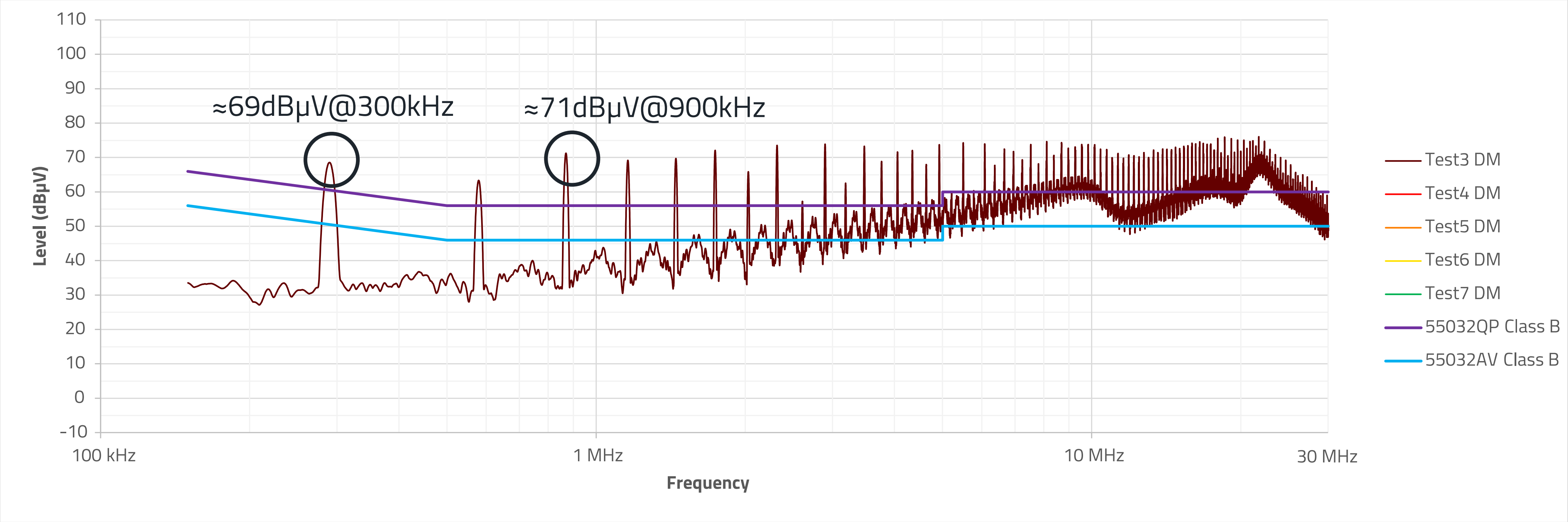
details later

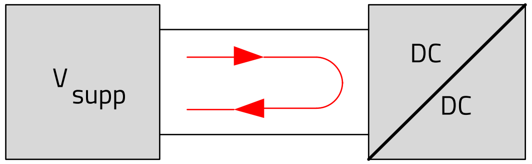
Test#3b: Simulation - Conducted emissions - Common mode

Simulation\Test1-7\Flyback_EMI_Test3b_FFT.asc



Test#3: Conducted emissions - Differential mode



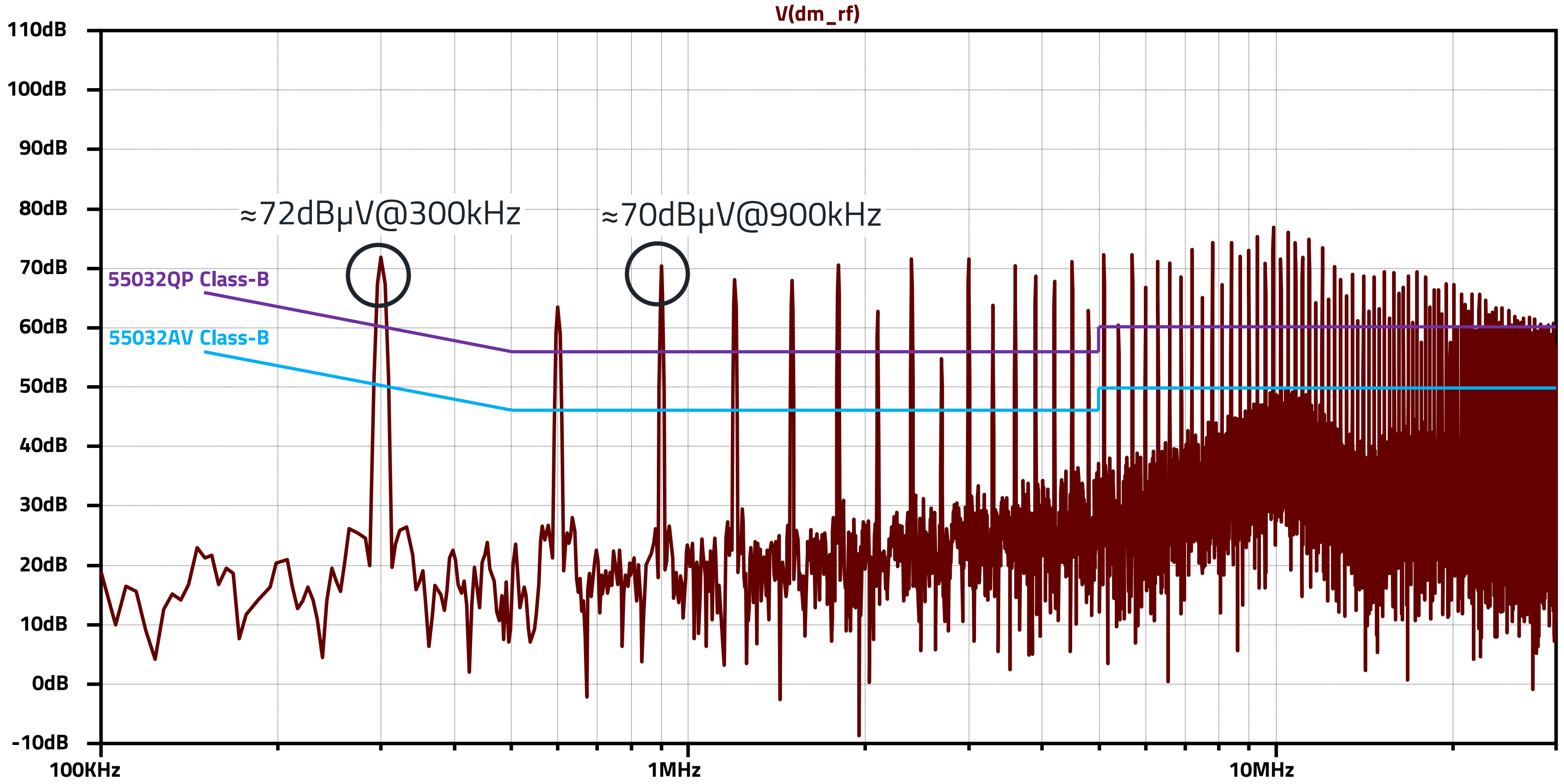


Name	Description
Test#3	Reference (no improvement)

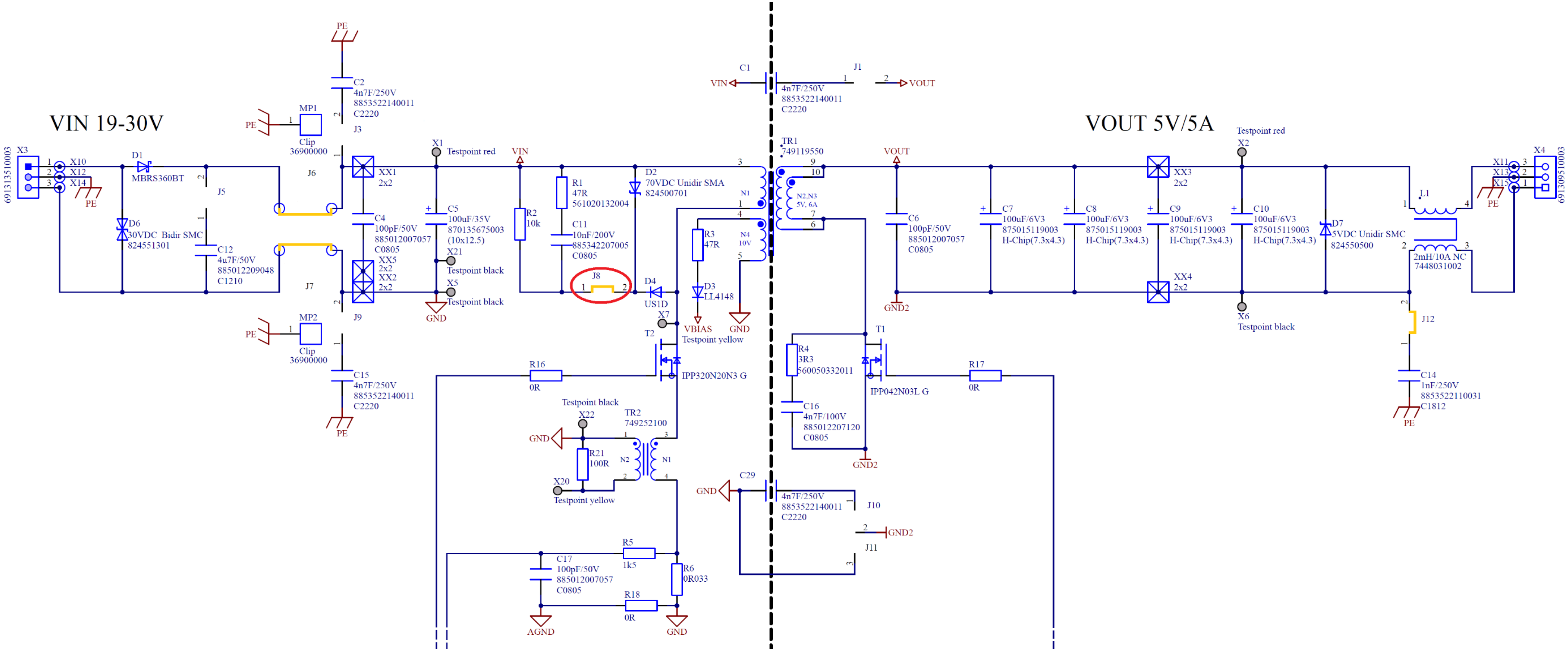
Differential Mode

Test#3b: Simulation - Conducted emissions - Differential mode

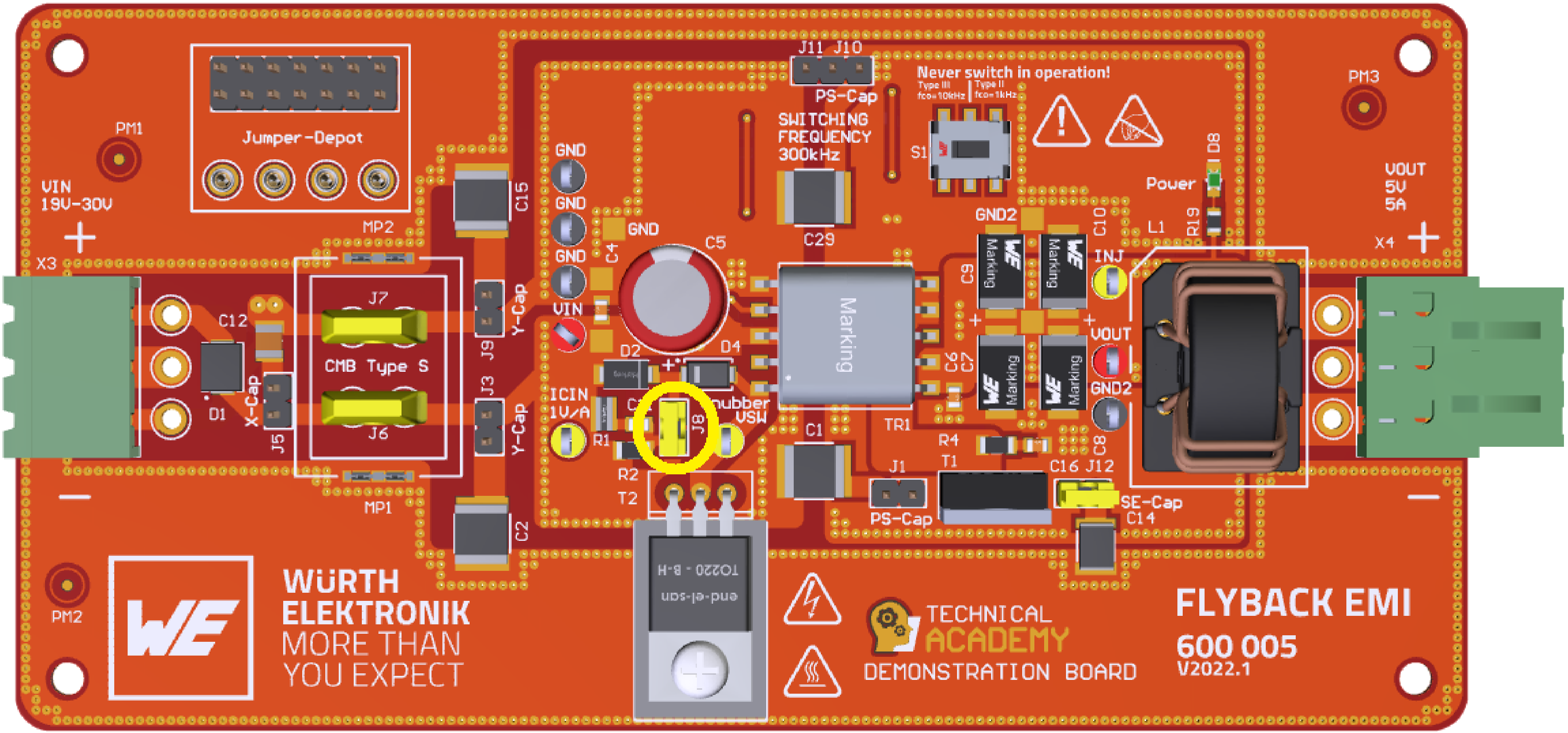
Simulation\Test1-7\Flyback_EMI_Test3b_FFT.asc



Test#4: Schematic



Test#4: Board configuration

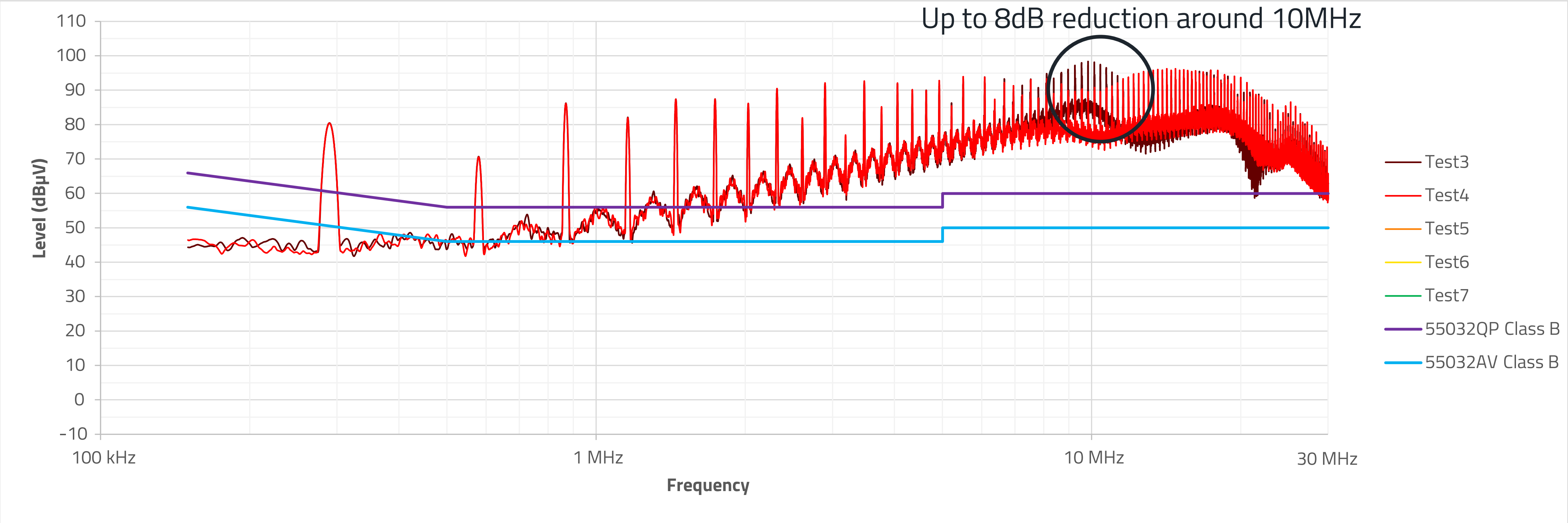


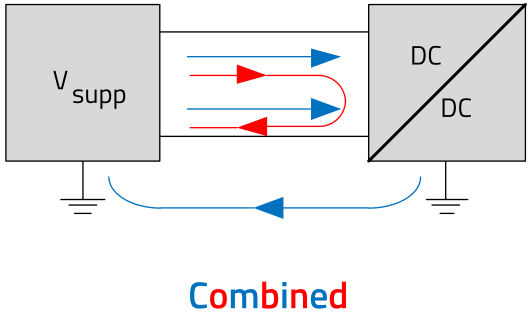
Test#4: Quiz

- Which type of noise (CM/DM) is influenced by the EMC improvement according to Test#4 (activating RCD snubber)?

  - A: Differential-mode noise
  - B: Common-mode noise
  - C: Both

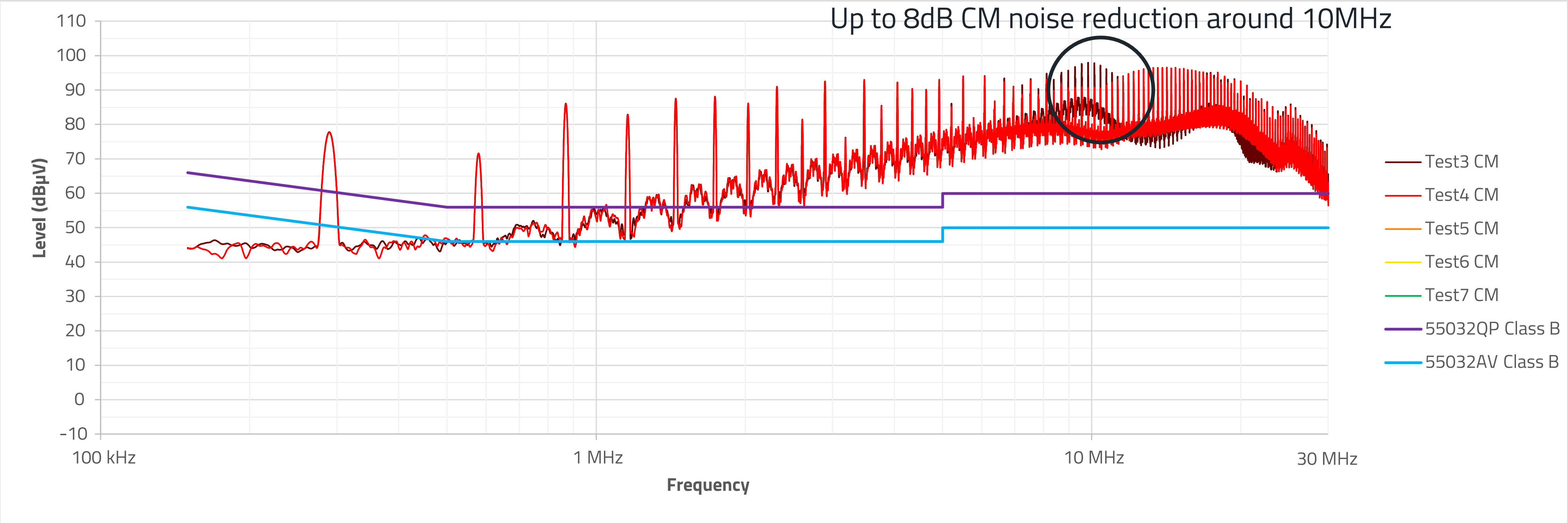
Test#4: Total conducted emissions - Line

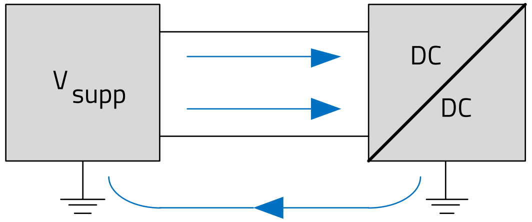




Name	Description
Test#3	Reference (no improvement)
Test#4	Test#3 + RCD-snubber

Test#4: Conducted emissions - Common mode

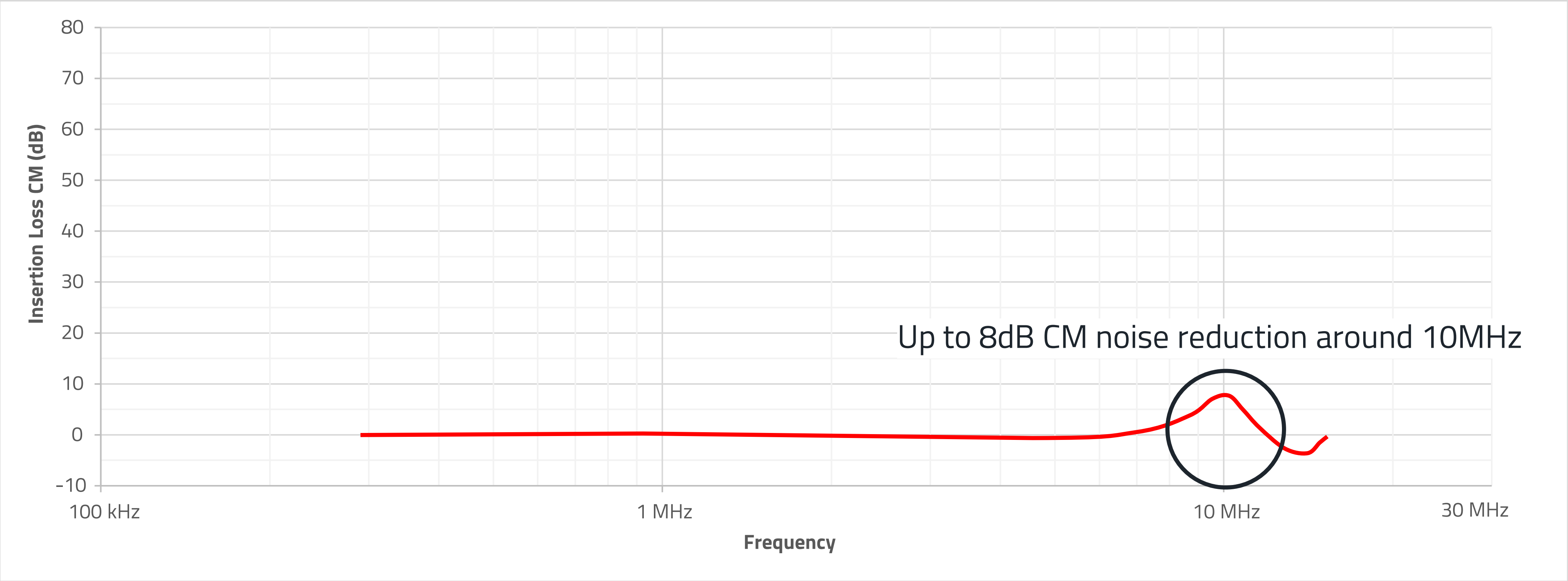


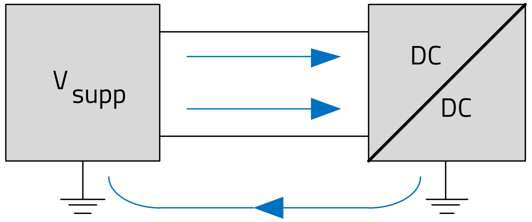


Common Mode

Name	Description
Test#3	Reference (no improvement)
Test#4	Test#3 + RCD-snubber

Test#4: Conducted emissions - Insertion loss CM

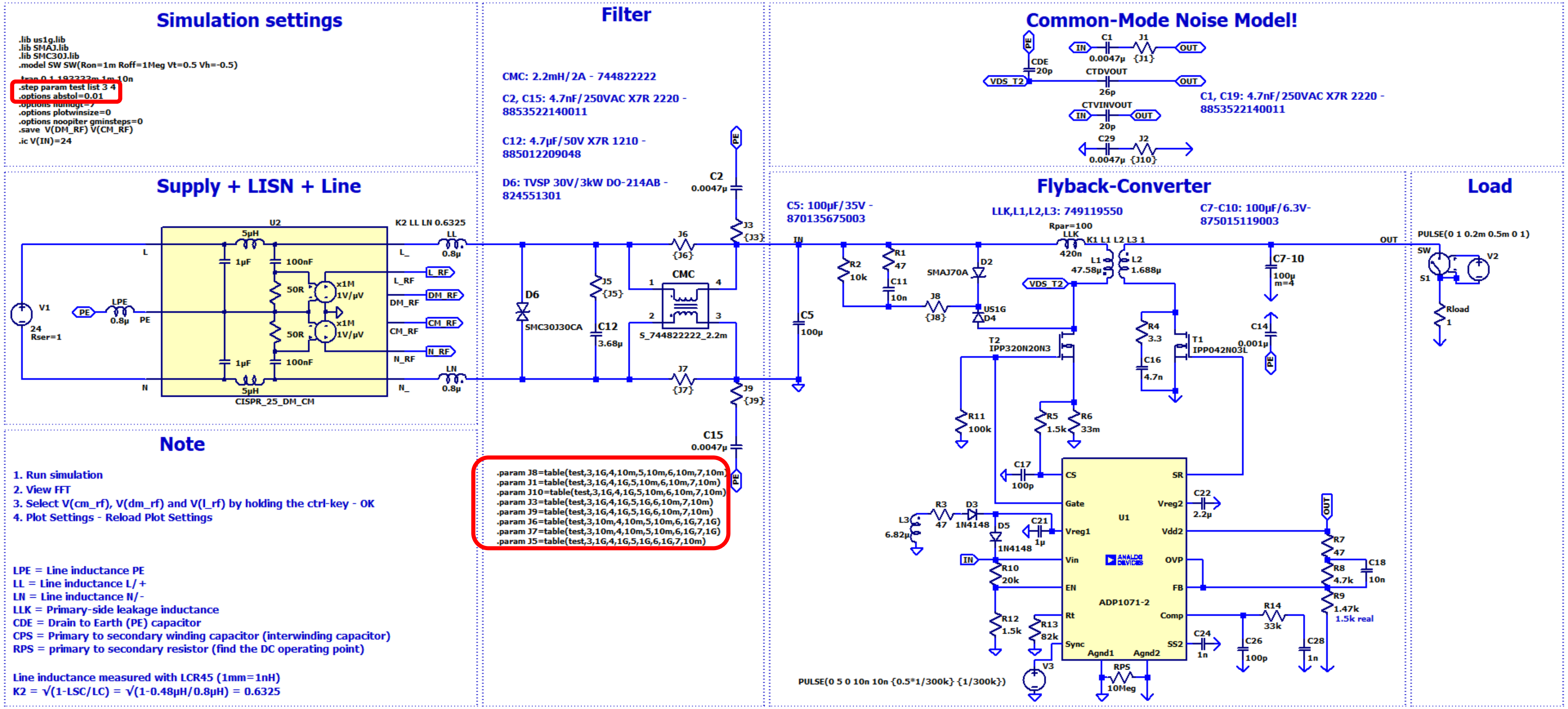




Common Mode

Description
+ RCD-snubber

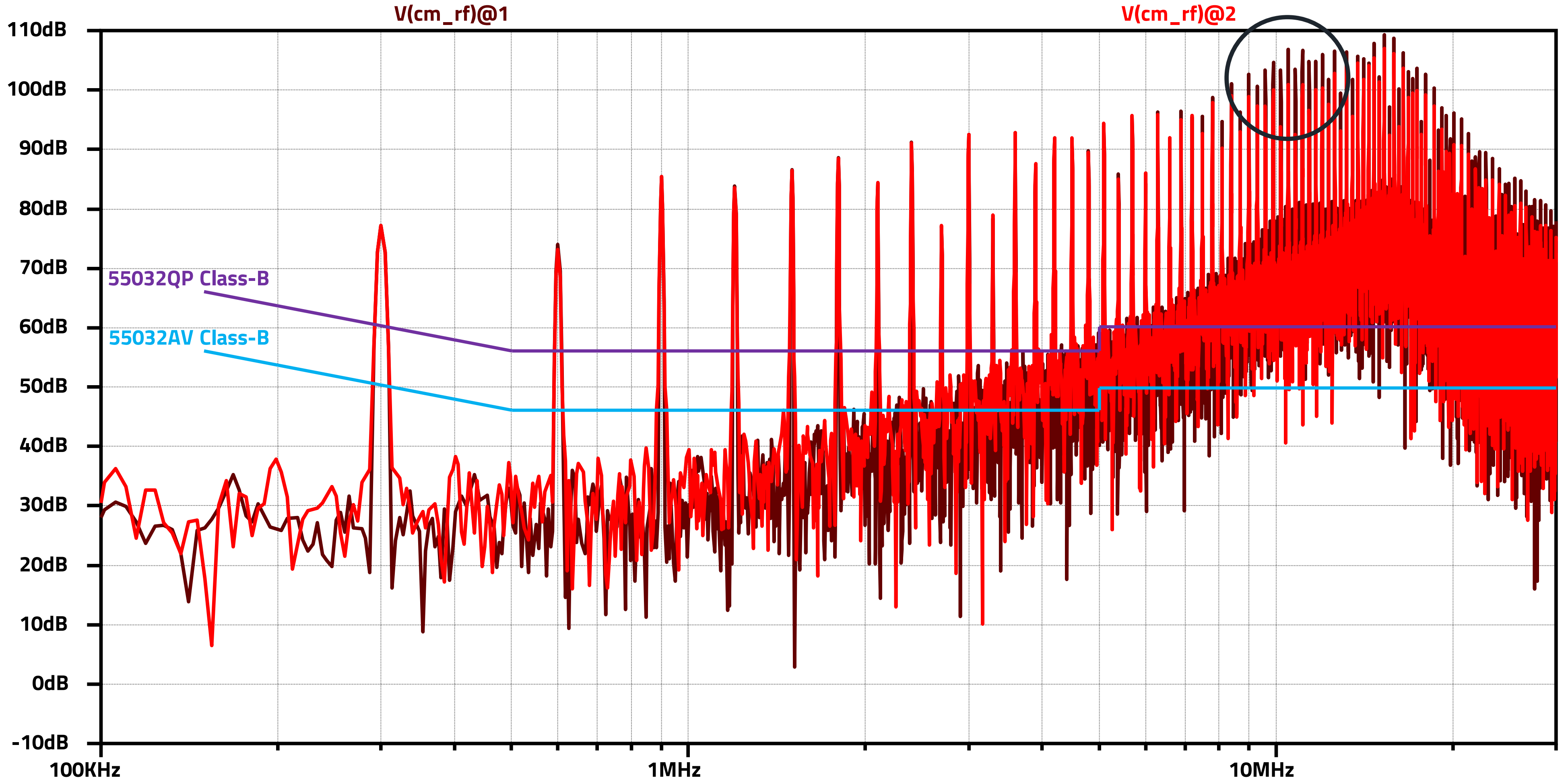
Test#4: Simulation configuration



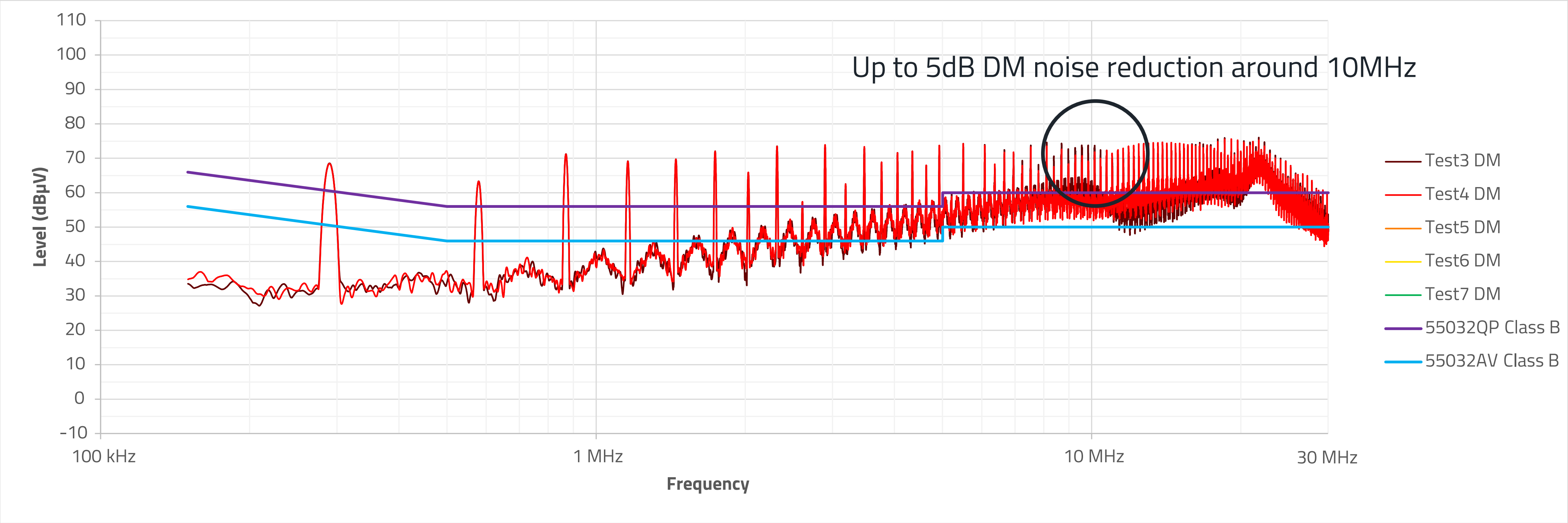
Test#4b: Simulation - Conducted emissions - Common mode

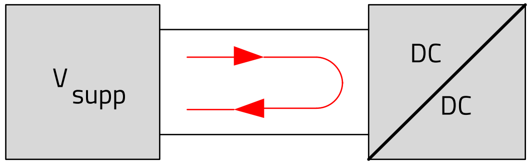
Simulation\Test1-7\Flyback_EMI_Test3-4b_FFT.asc

Up to 8dB CM noise reduction around 10MHz



Test#4: Conducted emissions - Differential mode

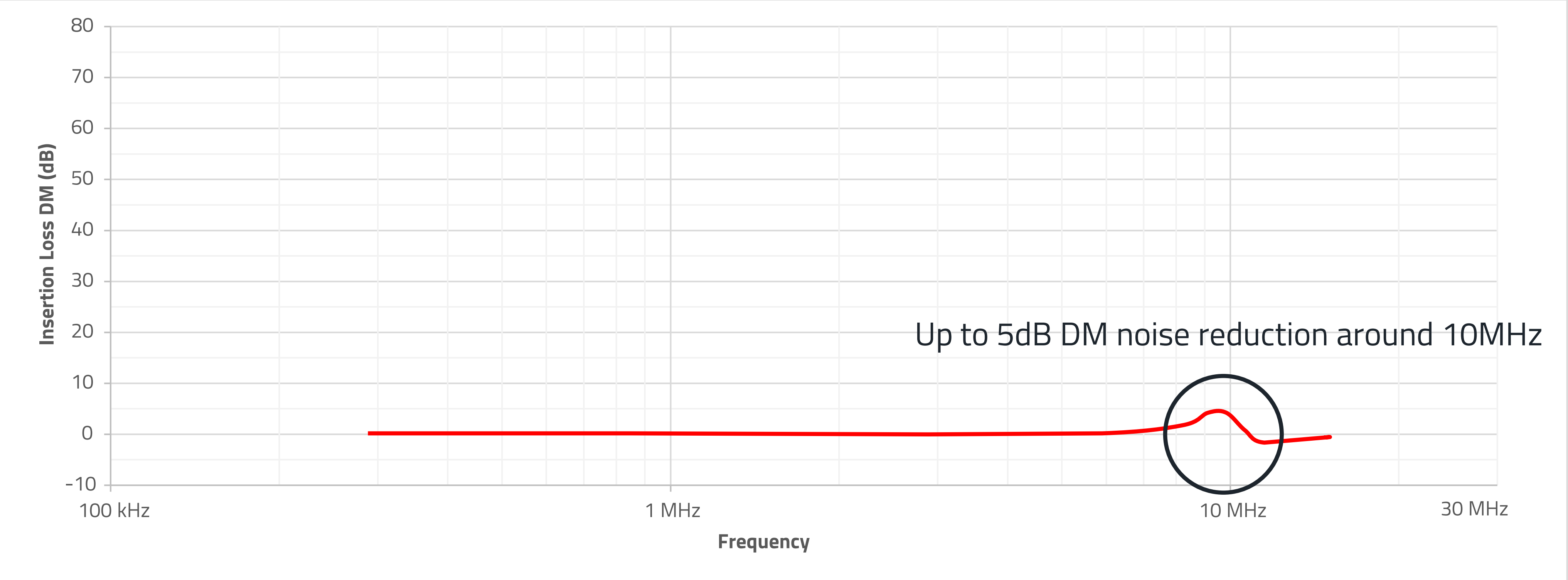


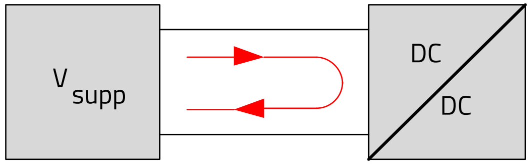


Name	Description
Test#3	Reference (no improvement)
Test#4	Test#3 + RCD-snubber

Differential Mode

Test#4: Conducted emissions - Insertion loss DM



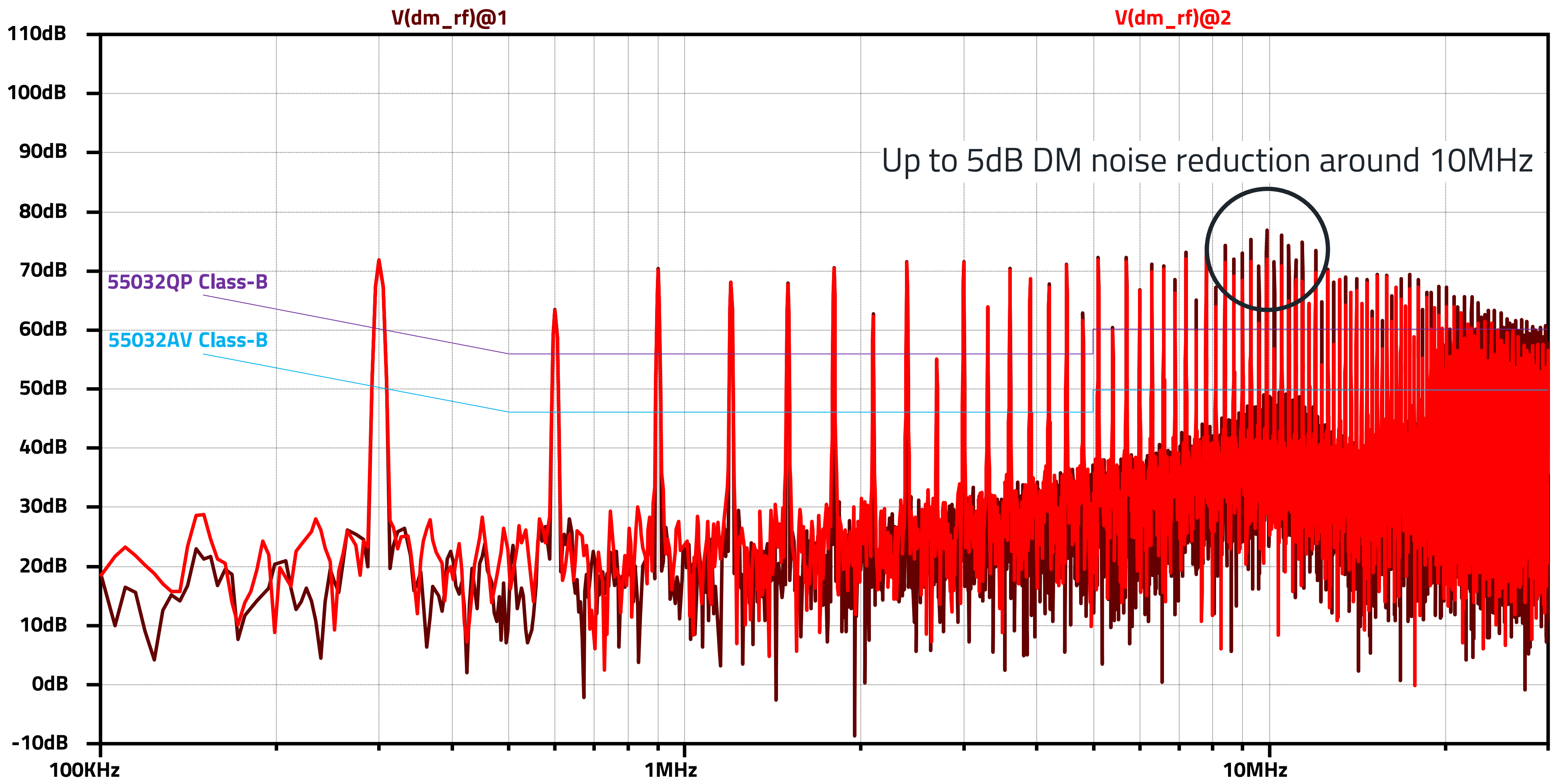


Description
+ RCD-snubber

Differential Mode

Test#4b: Simulation - Conducted emissions - Differential mode

Simulation\Test1-7\Flyback_EMI_Test3-4b_FFT.asc



Test#4: Quiz

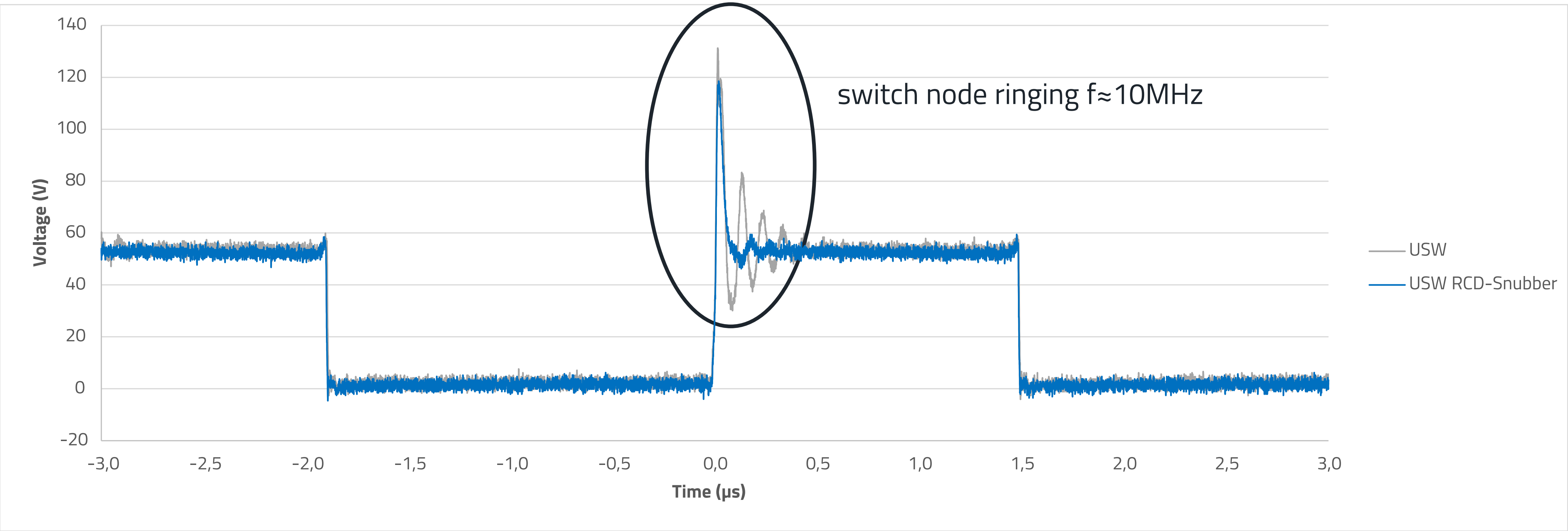
Answer

- Which type of noise (CM/DM) is influenced by the EMC improvement according to Test#4 (activating RCD snubber)?

  - A: Differential-mode noise
  - B: Common-mode noise
  - **C: Both**

Test#4: Background - Switch node voltage

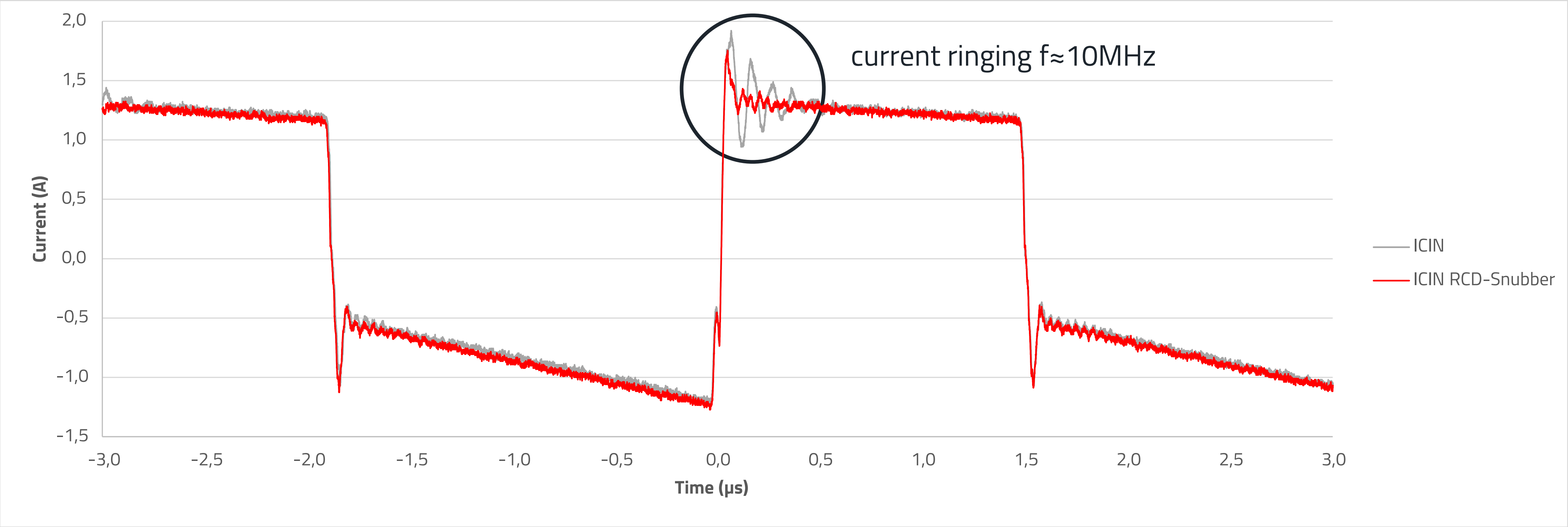
Common Mode



- The voltage change at the switch node is the cause of the CM noise
- The 10MHz switch node ringing is damped by the snubber

Test#4: Background - Input capacitor current

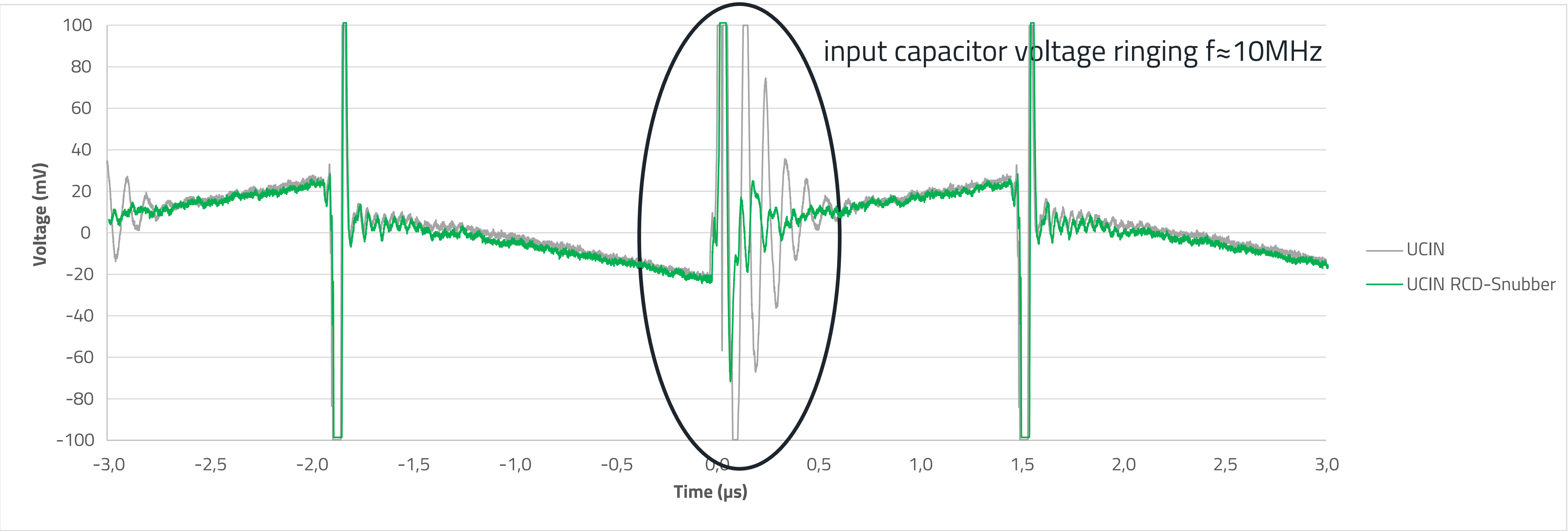
Differential Mode



- The input capacitor current waveform causes a voltage drop across the impedance of the input capacitor
- The 10MHz current ringing is damped by the snubber

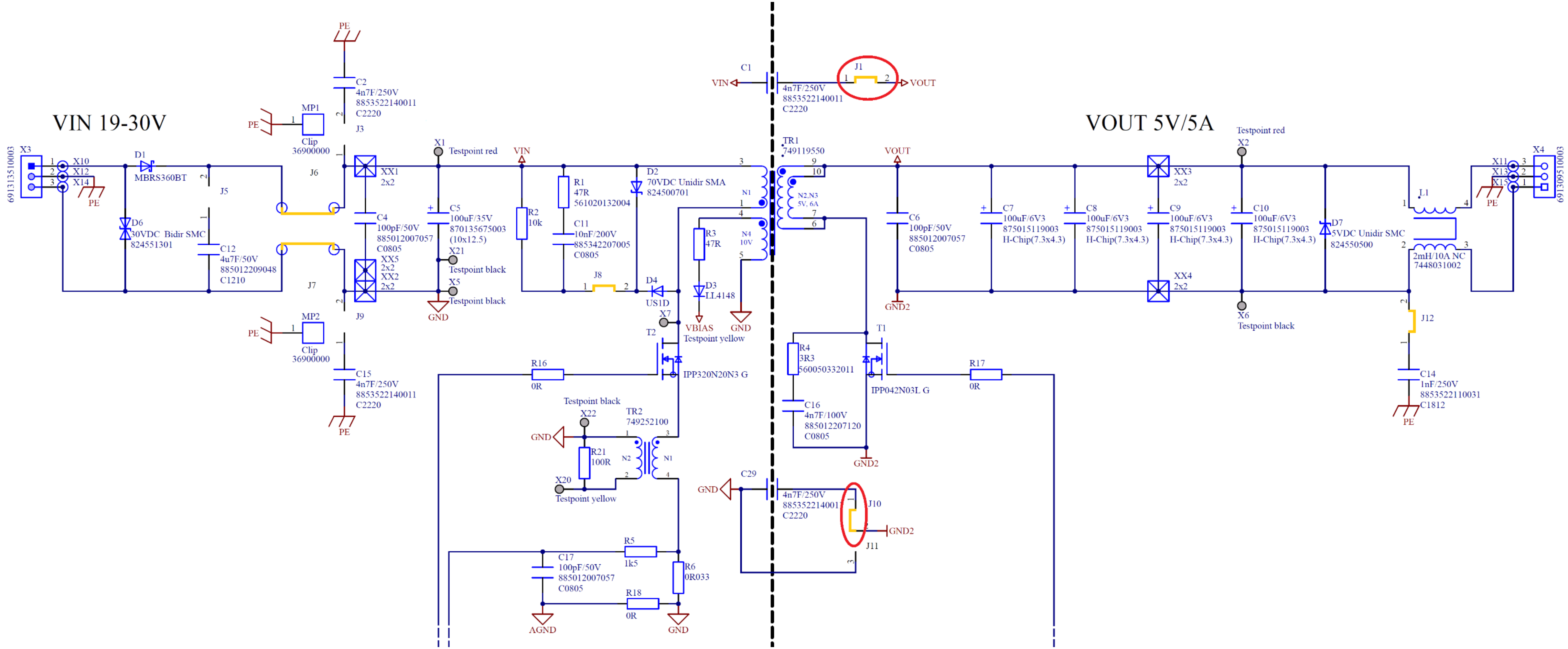
Test#4: Background - Input capacitor voltage ripple

Differential Mode

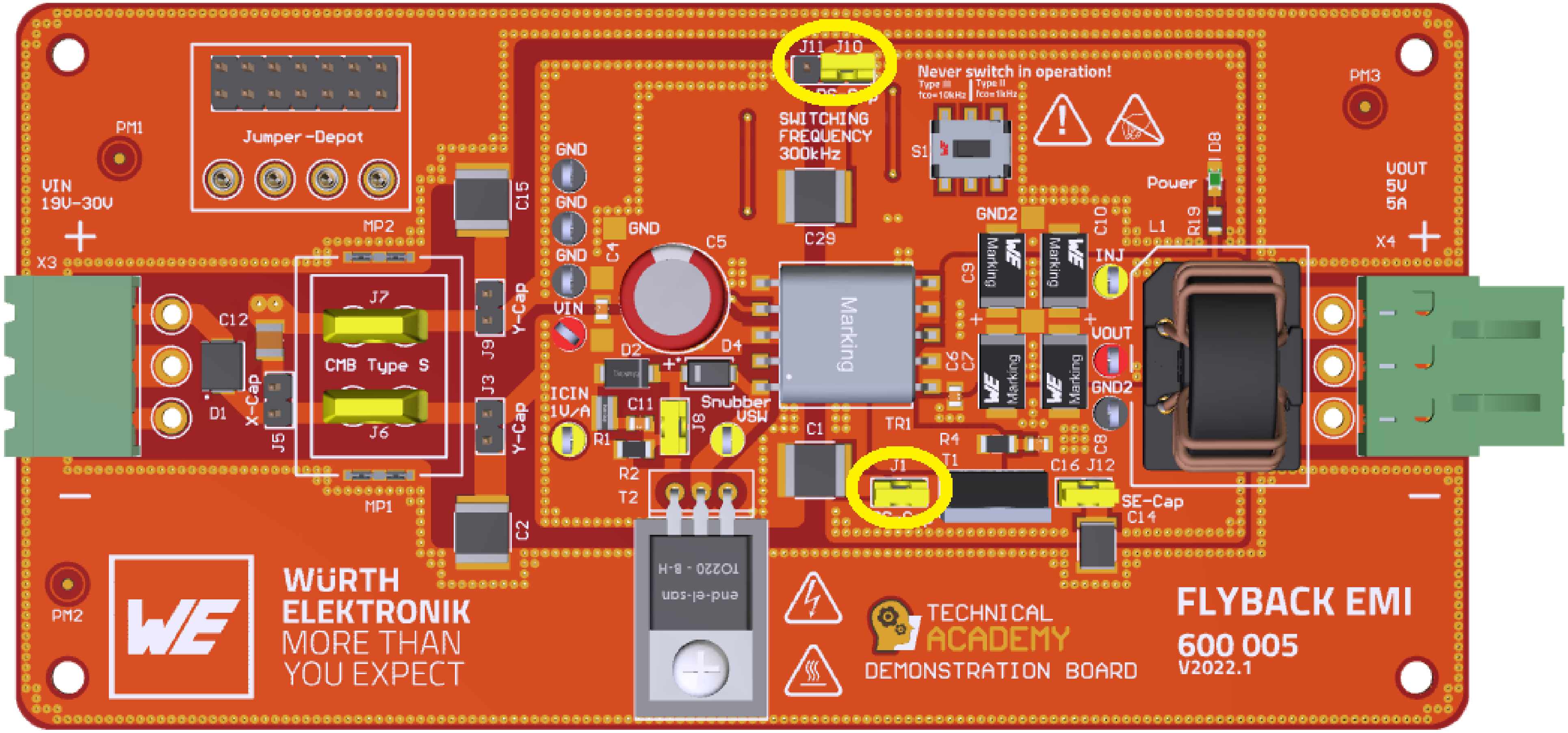


→ So the input capacitor voltage ripple ringing generated by the current waveform is damped too

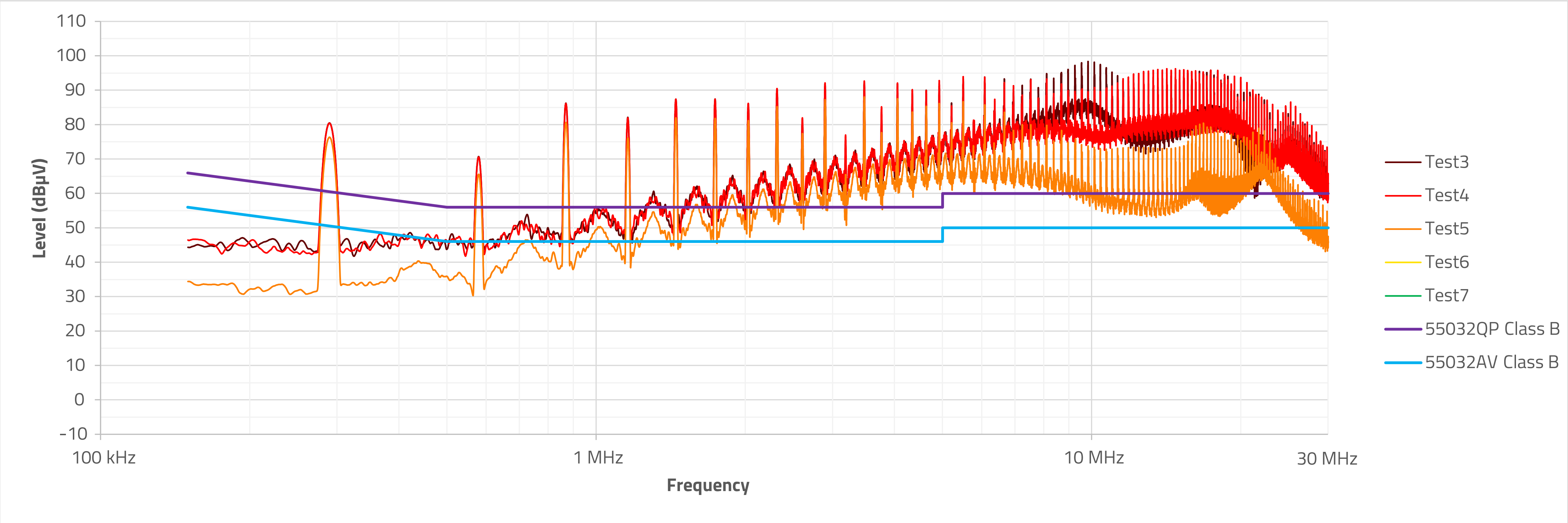
Test#5: Schematic

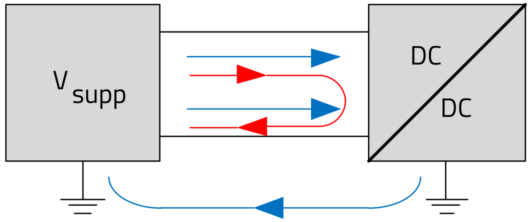


Test#5: Board configuration



Test#5: Total conducted emissions - Line

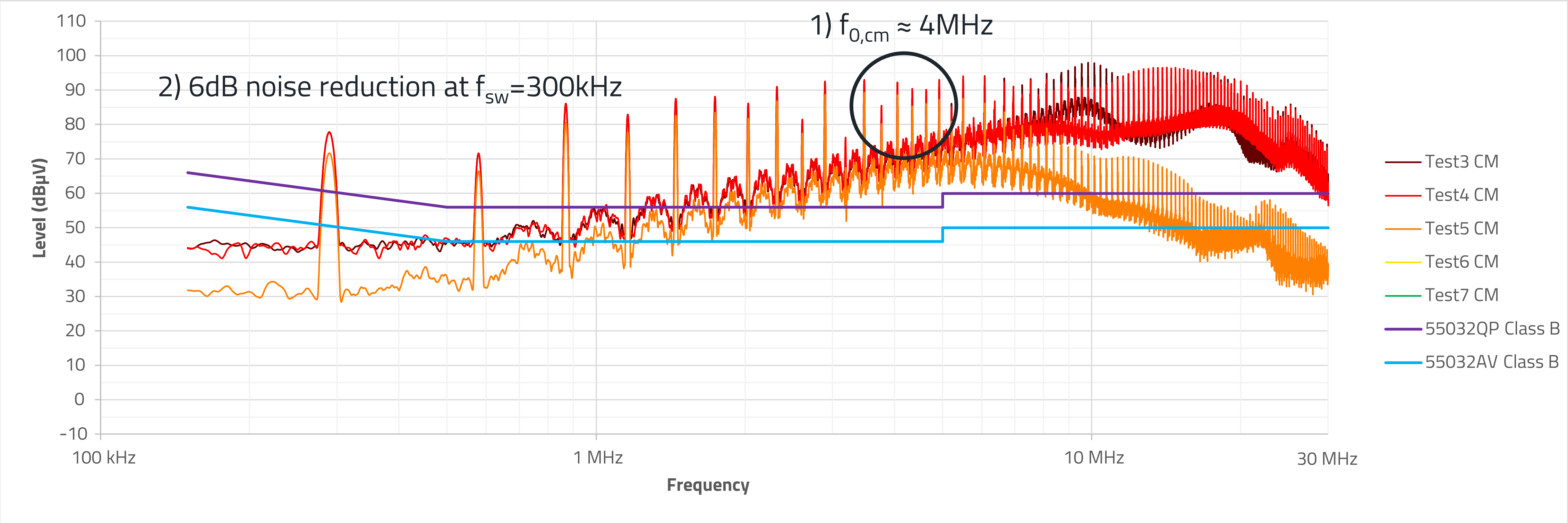


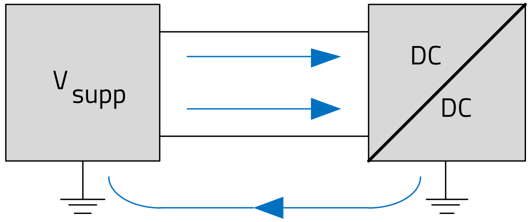


Combined

Name	Description
Test#3	Reference (no improvement)
Test#4	Test#3 + RCD-snubber
Test#5	Test#4 + primary to secondary y-capacitors

Test#5: Conducted emissions - Common mode

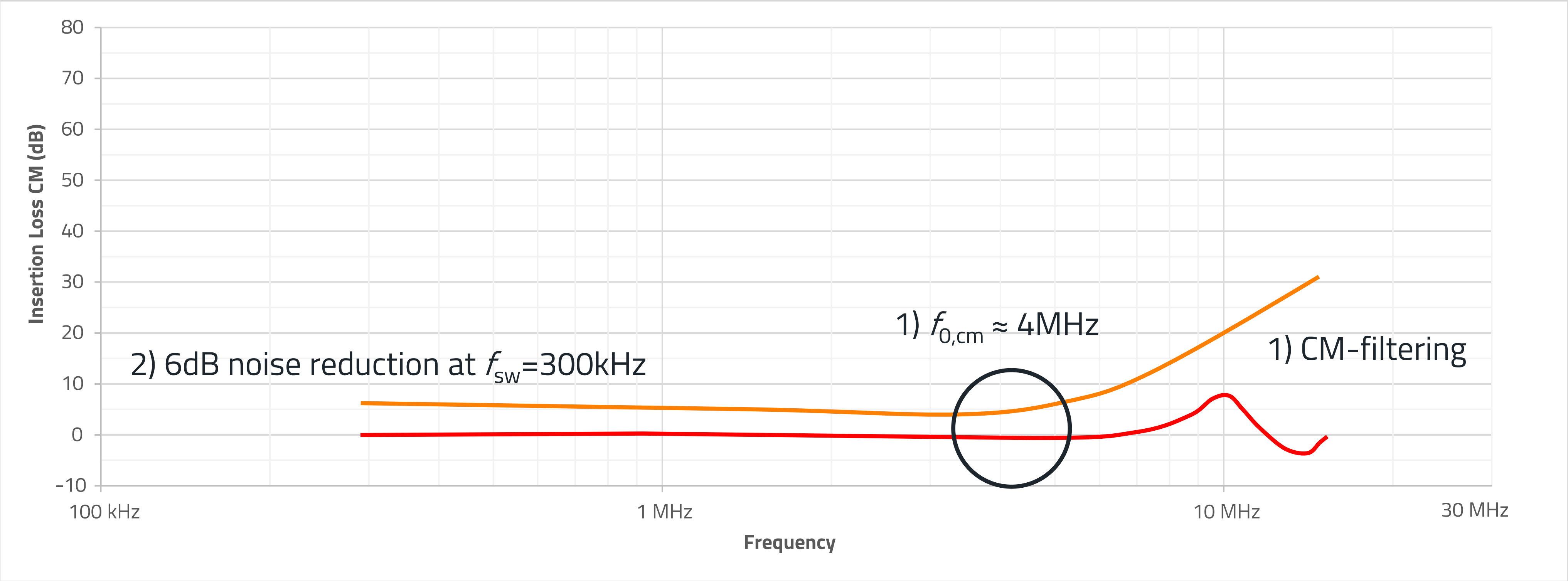


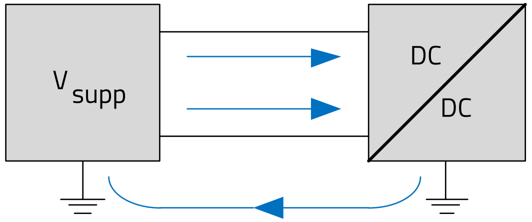


Common Mode

Name	Description
Test#3	Reference (no improvement)
Test#4	Test#3 + RCD-snubber
Test#5	Test#4 + primary to secondary y-capacitors

Test#5: Conducted emissions - Insertion loss CM



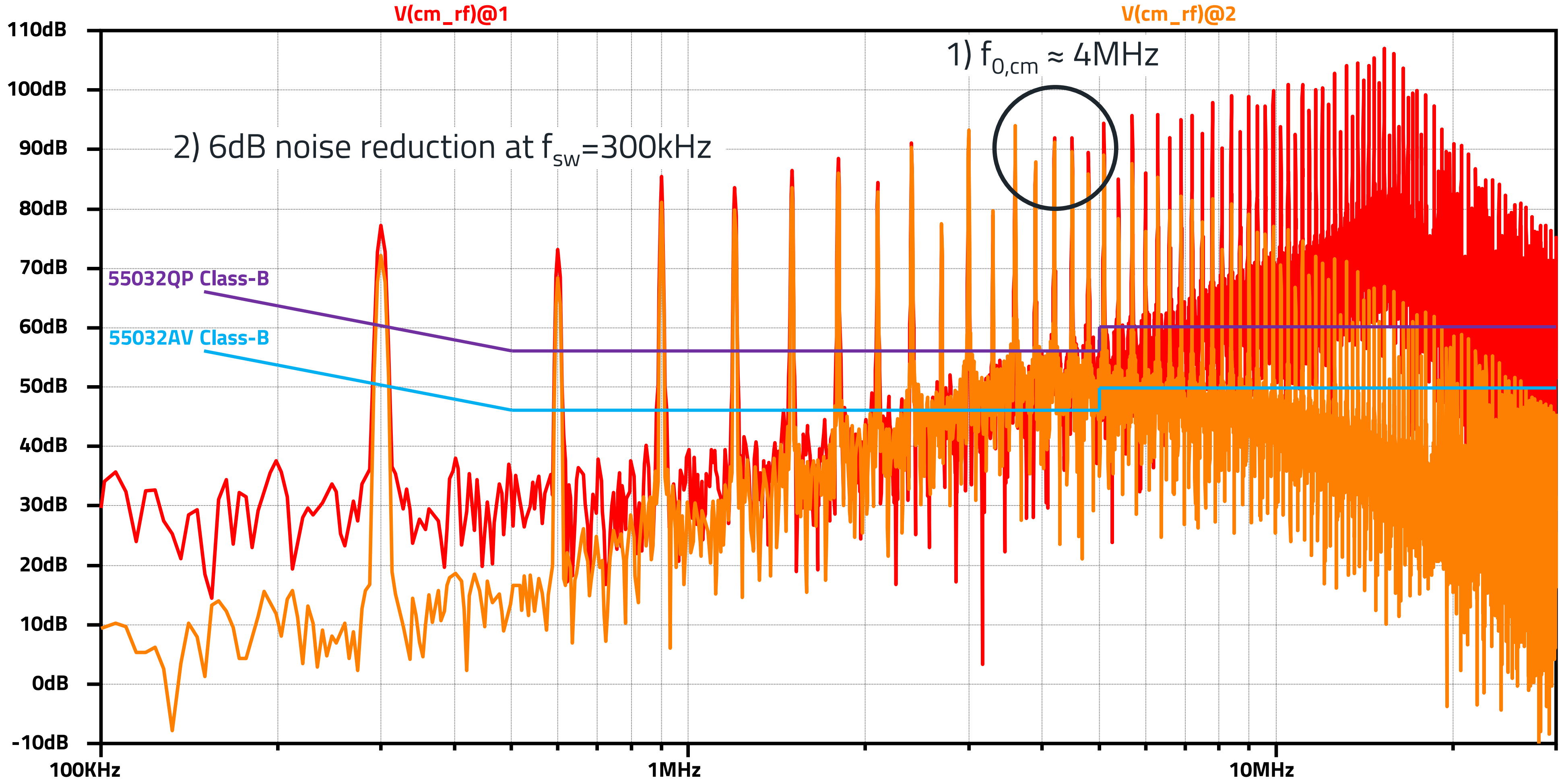


Common Mode

Description
+ RCD-snubber
+ primary to secondary y-capacitors

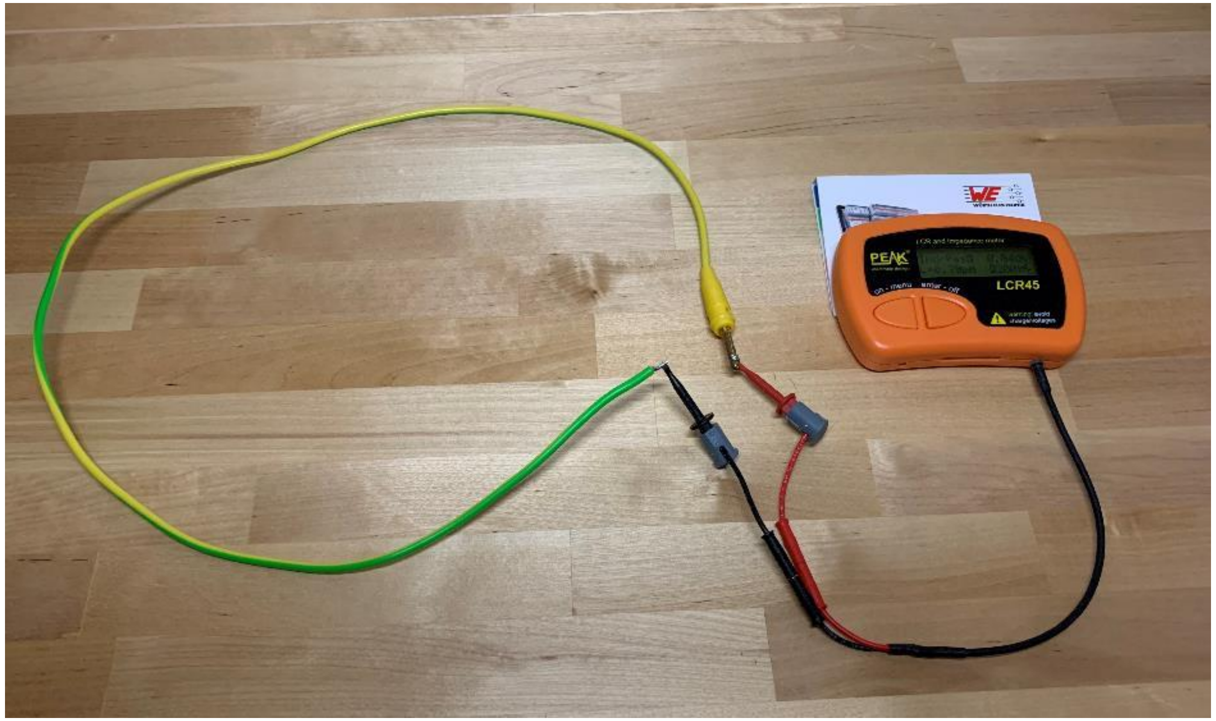
Test#5b: Simulation - Conducted emissions - Common mode

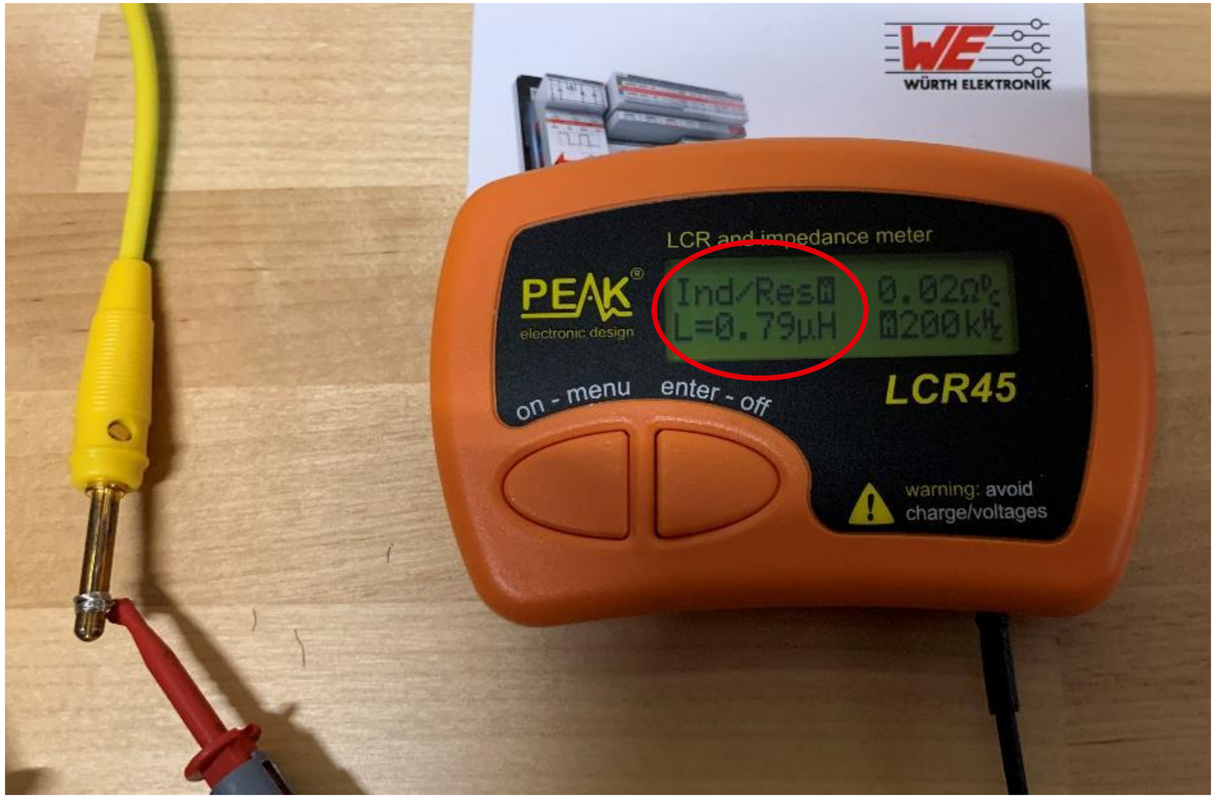
Simulation\Test1-7\Flyback_EMI_Test4-5b_FFT.asc



Test#5: Background - Line inductance

Measurement: 1) Line inductance PE - 0,8m

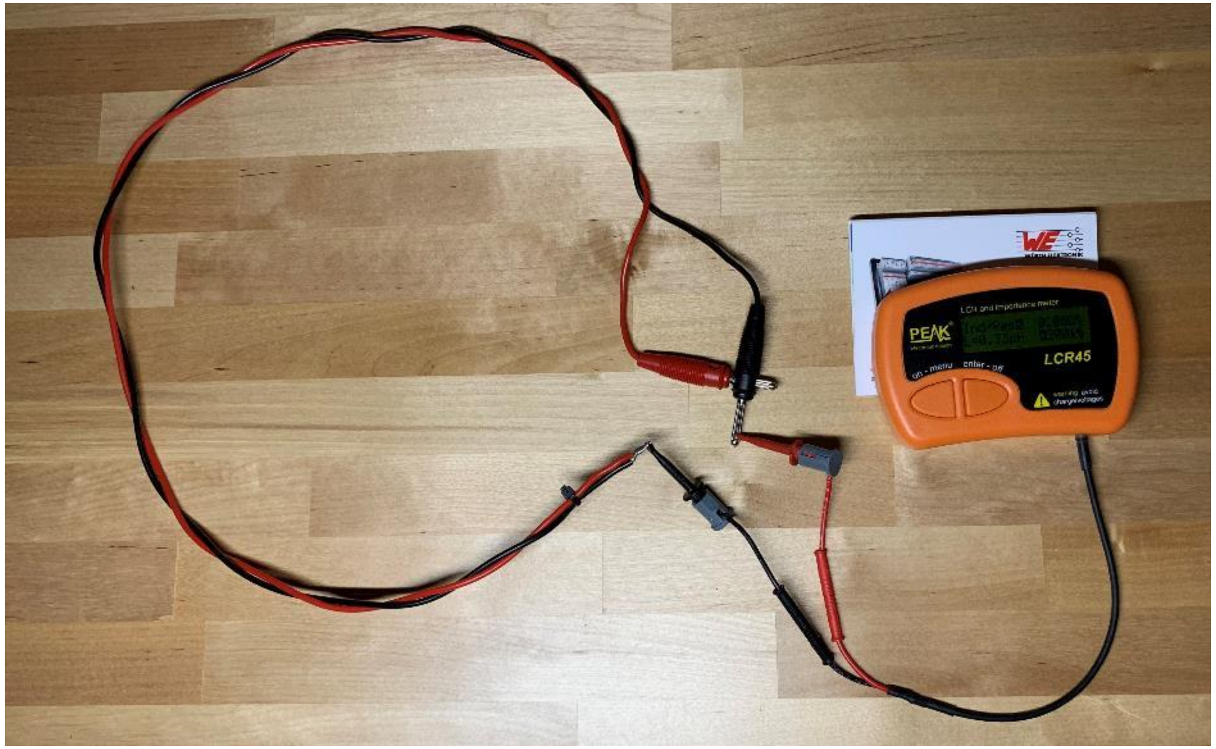




$$L_{\mathrm{PE}} \approx 0{,}8\mu H$$

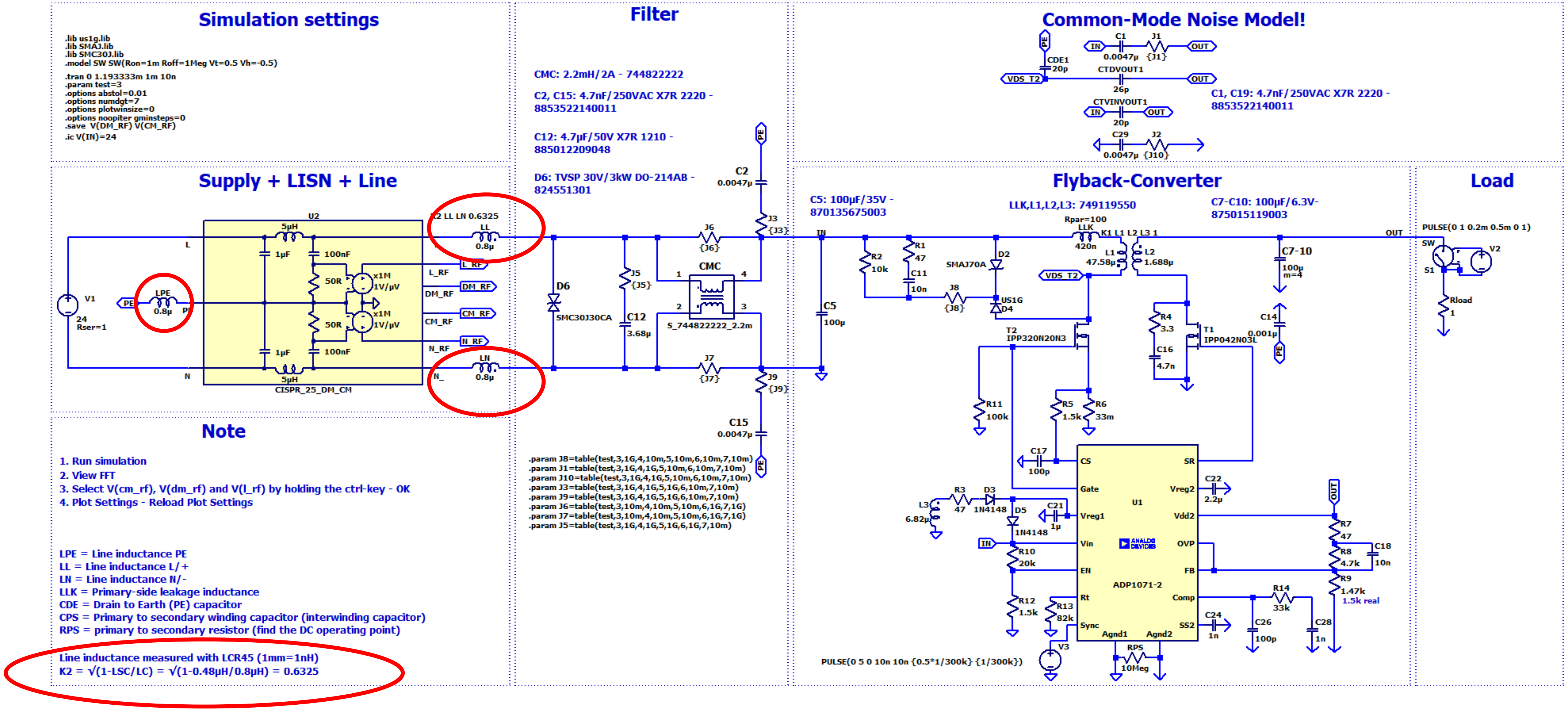
Test#5: Background - Line inductance

Measurement: 1) CM line inductance L+N (+/-) - 0,8m

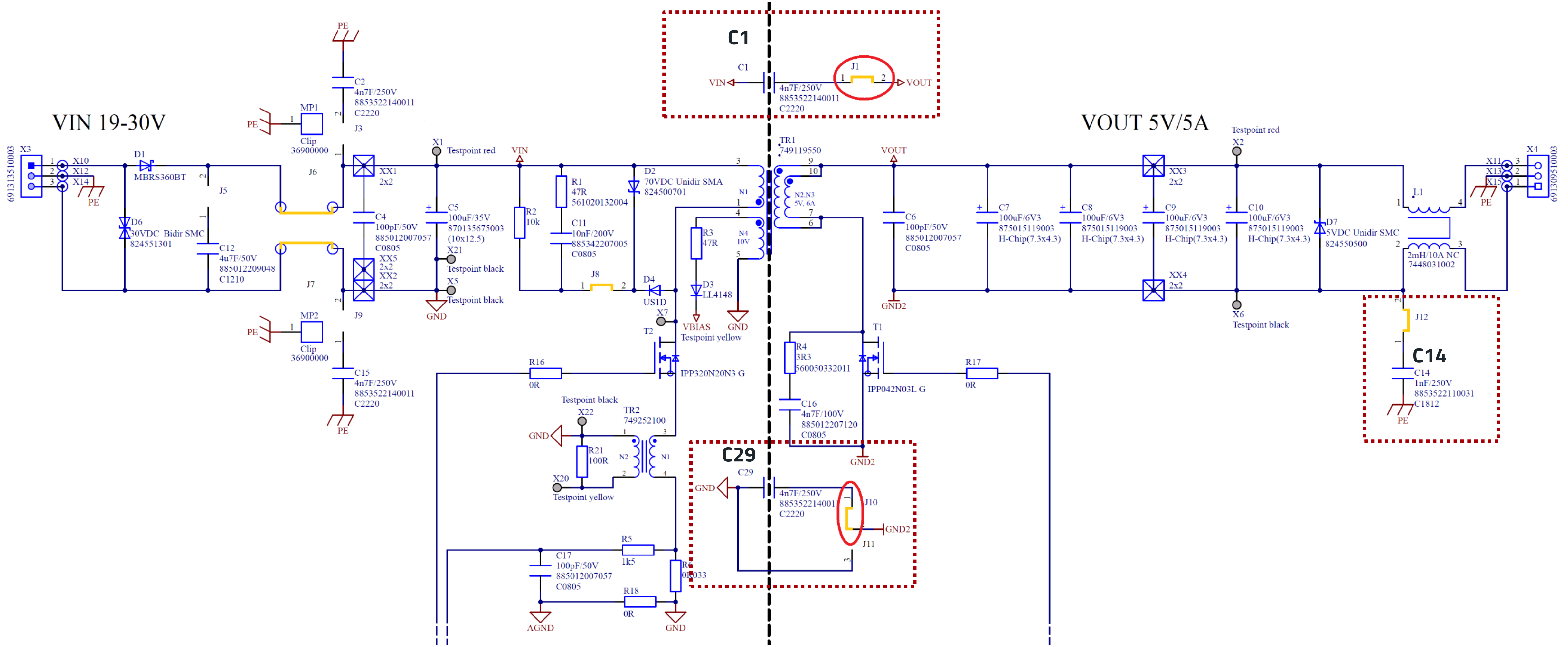


$$L_{\mathrm{cm,L+N}} \approx 0{,}8\mu H$$

Test#5: Background - Line inductance

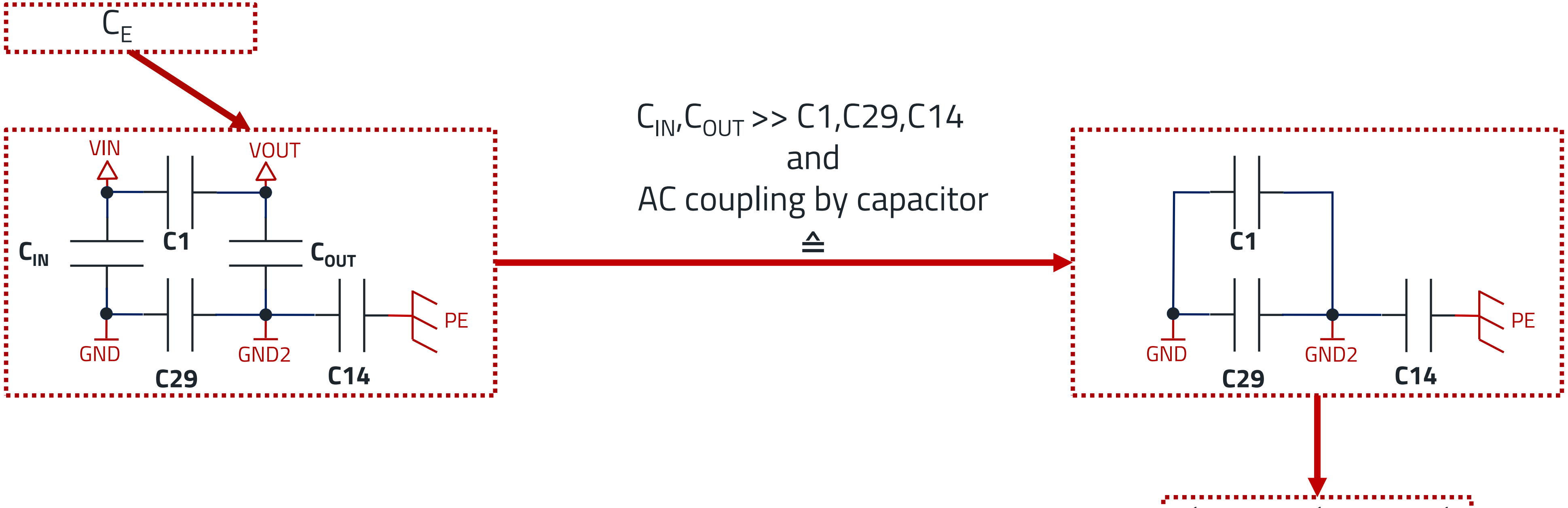


Test#5: Background - Ground capacitance C_E



Test#5: Background - Ground capacitance C_E

Theory: Effective ground capacitance in common mode



$$\frac{1}{C_\mathrm{E}} \approx \frac{1}{C_1 + C_{29}} + \frac{1}{C_{14}}$$

Test#5: Background - CM-Filtering

Theory

- 1) The line inductance and the reference ground capacitance act as common mode filter
  - Reference ground capacitance C_E:

$$\frac{1}{C_{\mathrm{E}}} \approx \frac{1}{C_1 + C_{29}} + \frac{1}{C_{14}}$$

$$\rightarrow C_{\mathrm{E}} \approx \frac{(C_1 + C_{29}) \cdot C_{14}}{C_1 + C_{29} + C_{14}} = \frac{(4{,}7nF + 4{,}7nF) \cdot 1nF}{4{,}7nF + 4{,}7nF + 1nF} \approx 0{,}904nF$$

  - Line inductance L_{line}:

Rule of thumb:

$$1\frac{\mu H}{m} \cdot 0{,}8m \rightarrow 0{,}8\mu H$$

$$\rightarrow L_{\mathrm{line}} = L_{\mathrm{PE}} + L_{\mathrm{cm,L+N}} = 0{,}8\mu H + 0{,}8\mu H = 1{,}6\mu H$$

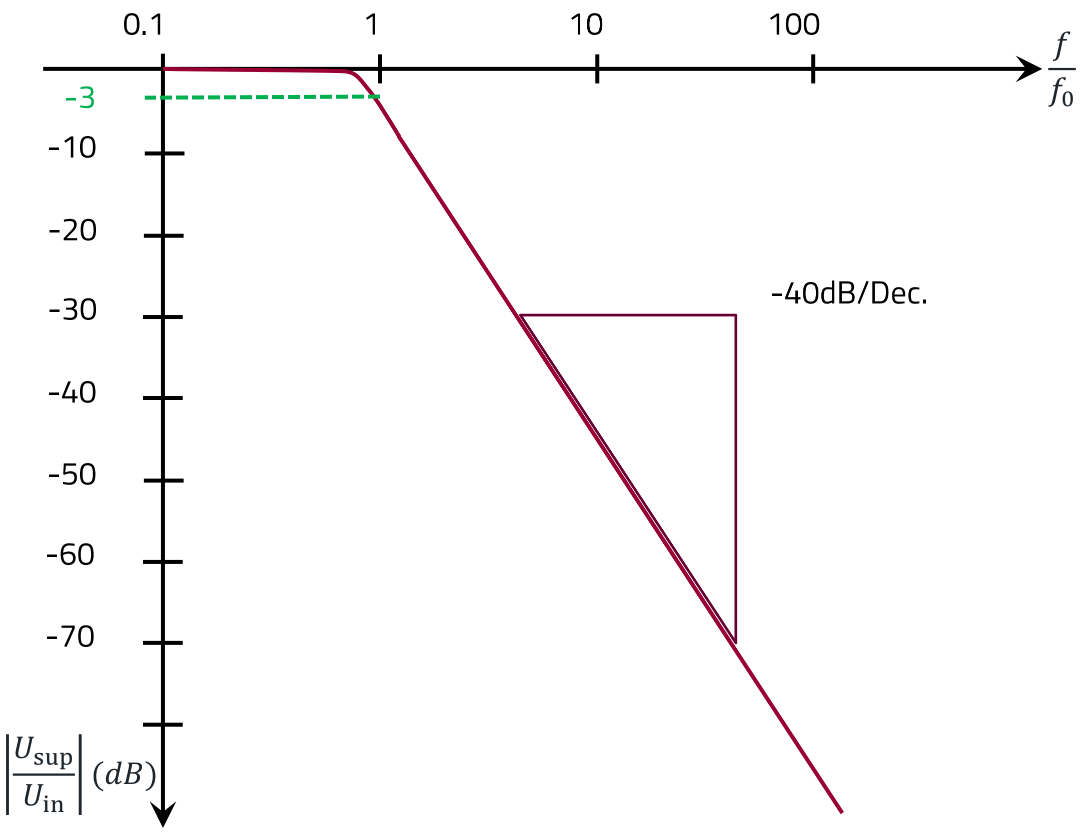
Test#5: Background - CM-Filtering

Theory

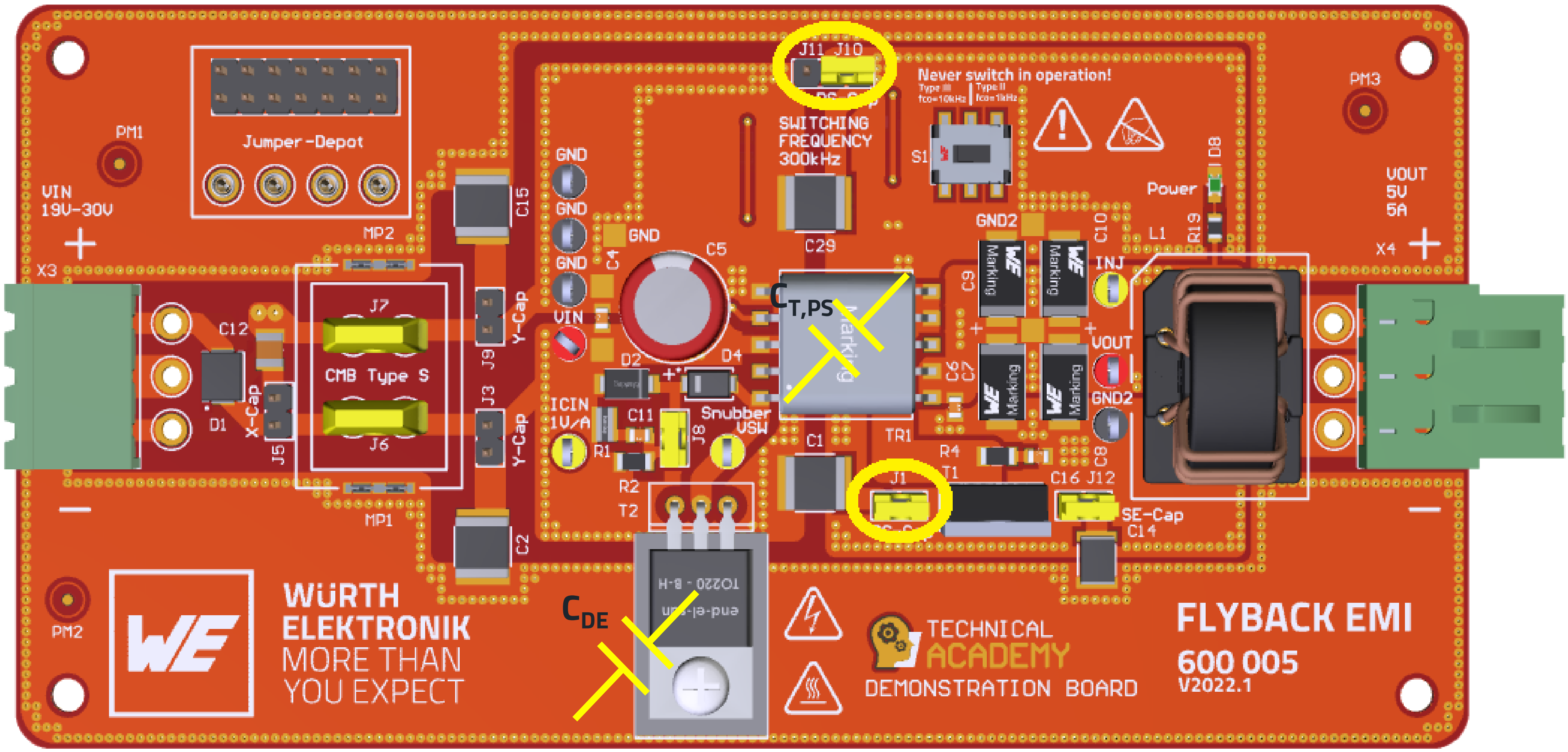
- The line inductance and the reference ground capacitance act as a common-mode filter for free.
- Corner frequency of the common-mode filter (Thomson's equation of oscillation):

$$f_{0,\mathrm{cm}} = \frac{1}{2\pi \cdot \sqrt{L_{\mathrm{line}} \cdot C_{\mathrm{E}}}} = \frac{1}{2\pi \cdot \sqrt{1{,}6\mu H \cdot 0{,}904nF}} \approx 4{,}2MHz$$

Gain Plot 2nd Order LC Filter



Test#5: Background - Switch node capacitance



Test#5: Background - Switch node capacitance

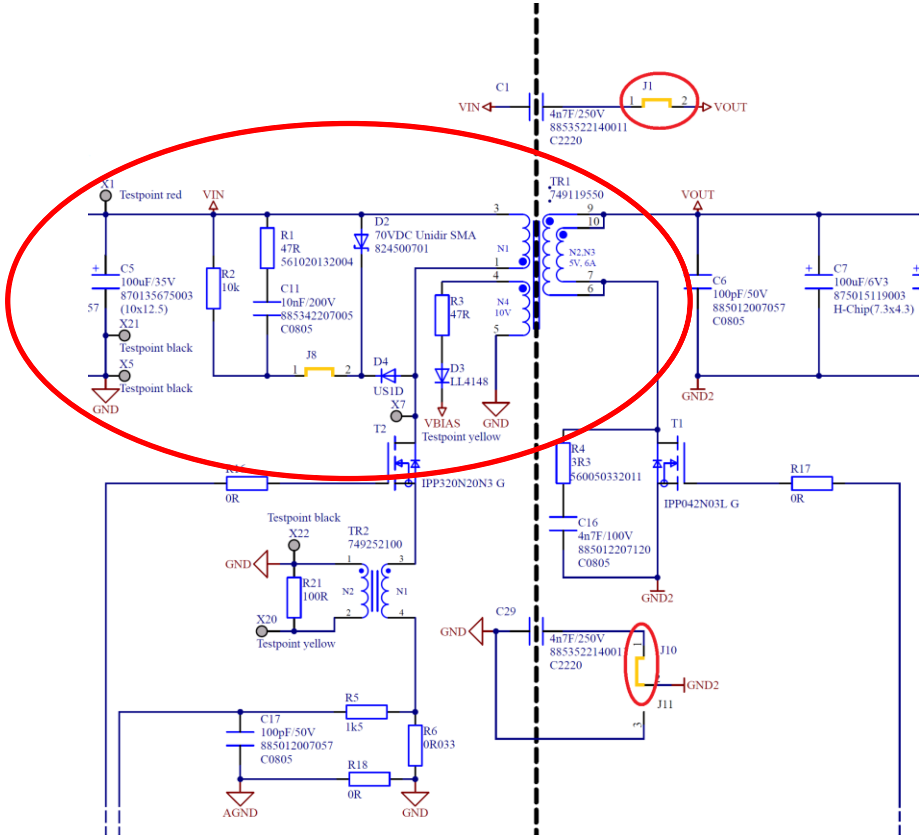
Measurement: 2) Parasitic capacitance

$C_{\mathrm{T,PS}} \approx 50\mathrm{pF}$

$C_{\mathrm{DE}} \approx 20\mathrm{pF}$

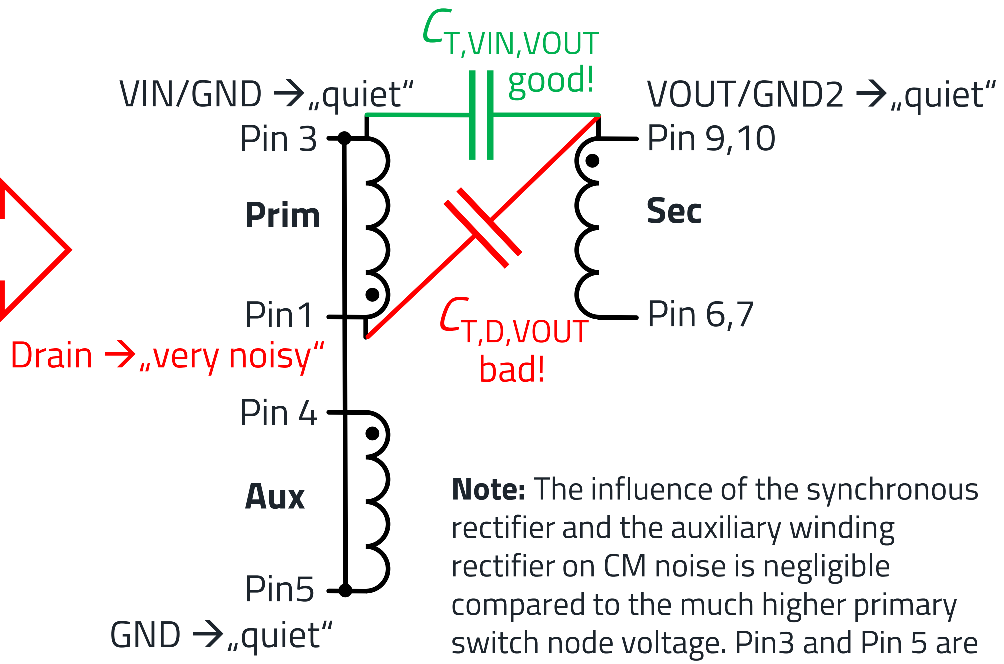
Test#5: Background – C_{PS}

Theory: Interwinding capacitance from primary to secondary side of the transformer



Schematic

$$C_{T,PS} = C_{T,VIN,VOUT} + C_{T,D,VOUT}$$



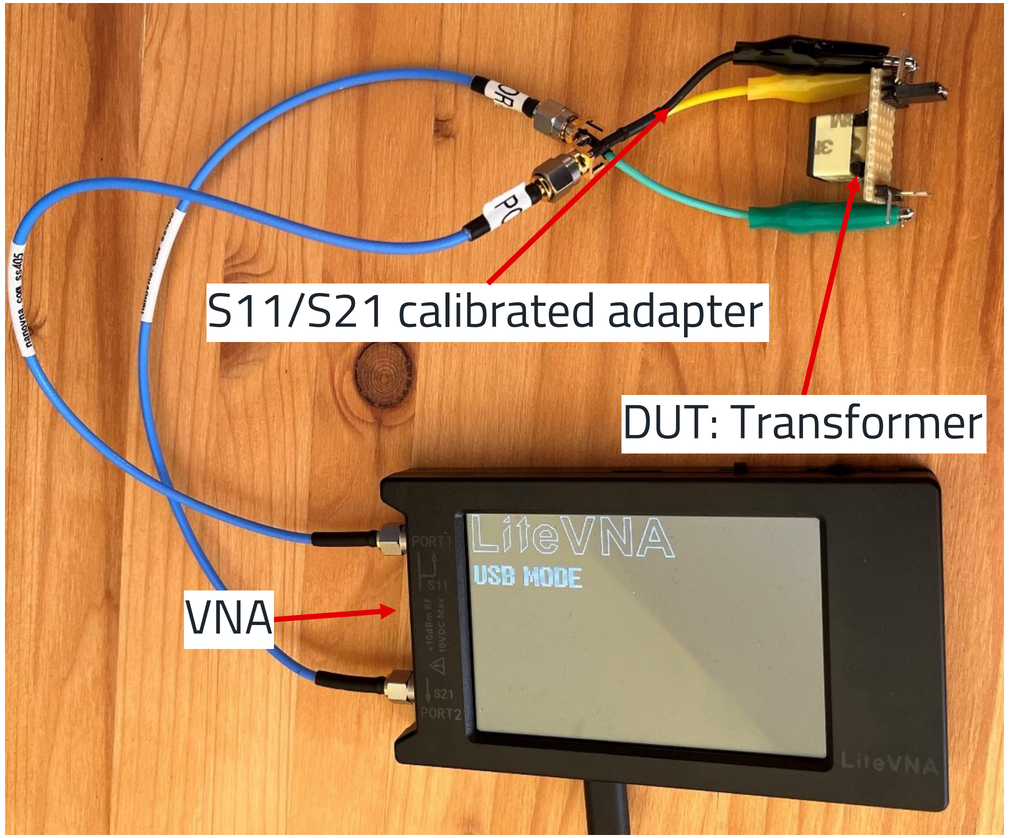
Note: The influence of the synchronous rectifier and the auxiliary winding rectifier on CM noise is negligible compared to the much higher primary switch node voltage. Pin3 and Pin 5 are "connected" in CM due the low impedance of the input capacitor (C5).

Simplified 2 capacitor transformer CM noise model

Test#5: Background – $C_{T,PS}$

Theory: Measuring $C_{T,PS}$, $C_{VT,VIN,VOUT}$ and $C_{D,VOUT}$

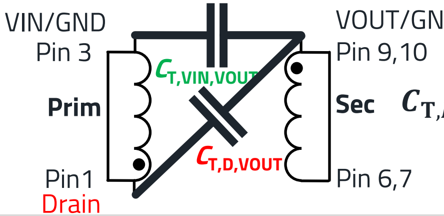
- $C_{T,PS} = C_{T,VIN,VOUT} + C_{T,D,VOUT}$
- C_{PS} can be determined with an LCR meter (≈50,5pF@200kHz) or with a 2 port VNA measurement (≈46pF@3MHz) between the shorted primary-referenced windings and shorted secondary winding
- $C_{T,VIN,VOUT}$ and $C_{T,D,VOUT}$ can be determined with a 2 port VNA measurement
  - The S21(Re_{S21}+j·Im_{S21}) gain can be converted into a series reactance assuming symmetrical properties of the DUT:
    - $X_S = -\frac{100\Omega \cdot Re_{S21}}{{Re_{S21}}^2 + {Im_{S21}}^2}$
    - $|X_S| = \sqrt{\left(-\frac{100\Omega \cdot Re_{S21}}{{Re_{S21}}^2 + {Im_{S21}}^2}\right)^2}$
  - Finally the parasitic coupling capacitance can be calculated from the series reactance:
    - $C_S = \frac{1}{\omega \cdot |X_S|}$



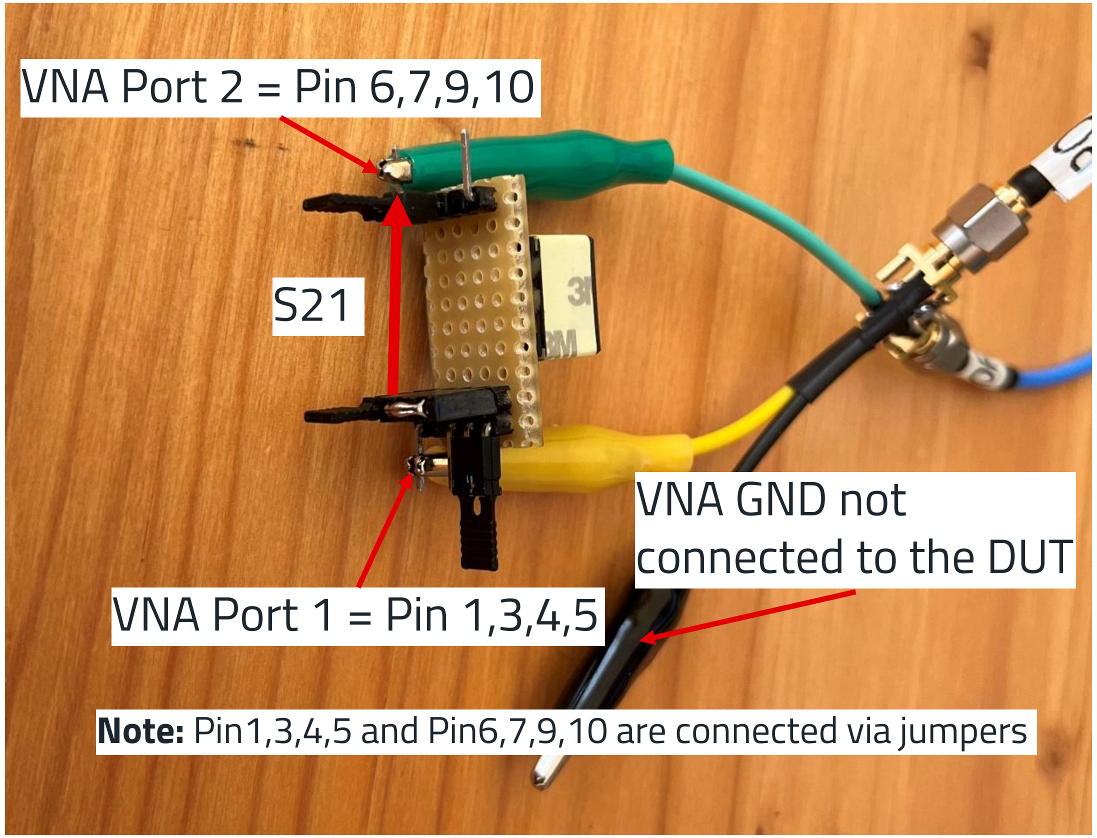
Measuring two-port S-parameters

Test#5: Background – $C_{T,PS}$

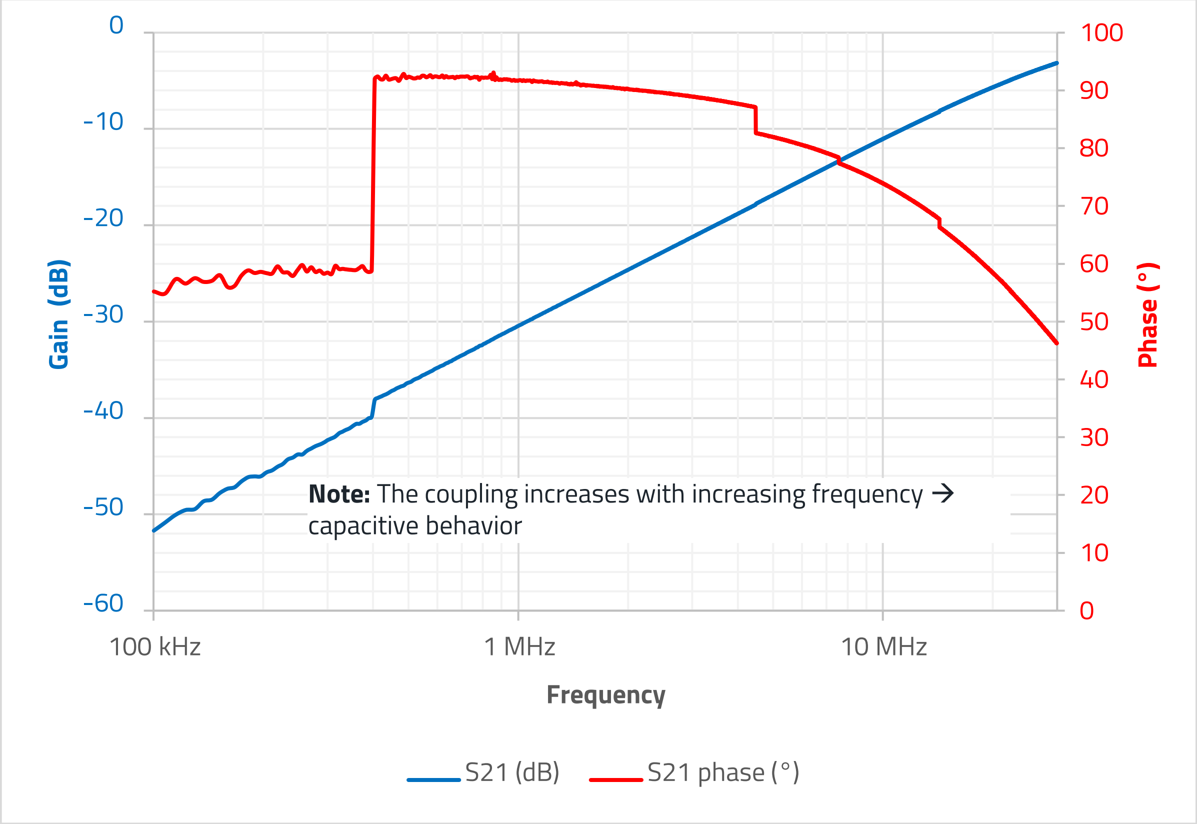
Theory: Measuring $C_{T,PS}$ with VNA



$C_{T,PS} = C_{T,VIN,VOUT} + C_{T,D,VOUT}$



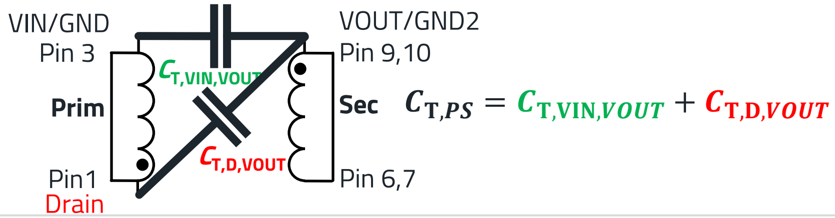
Measuring C_{PS}

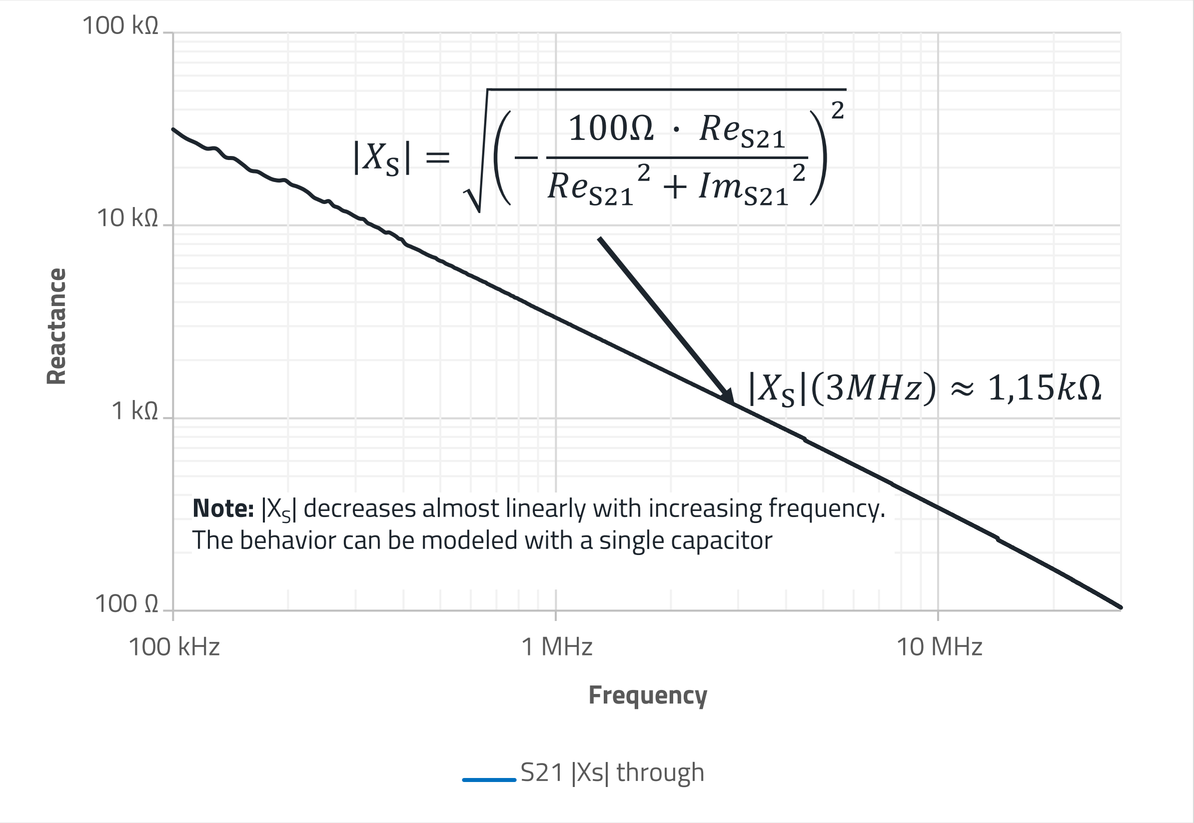


S21

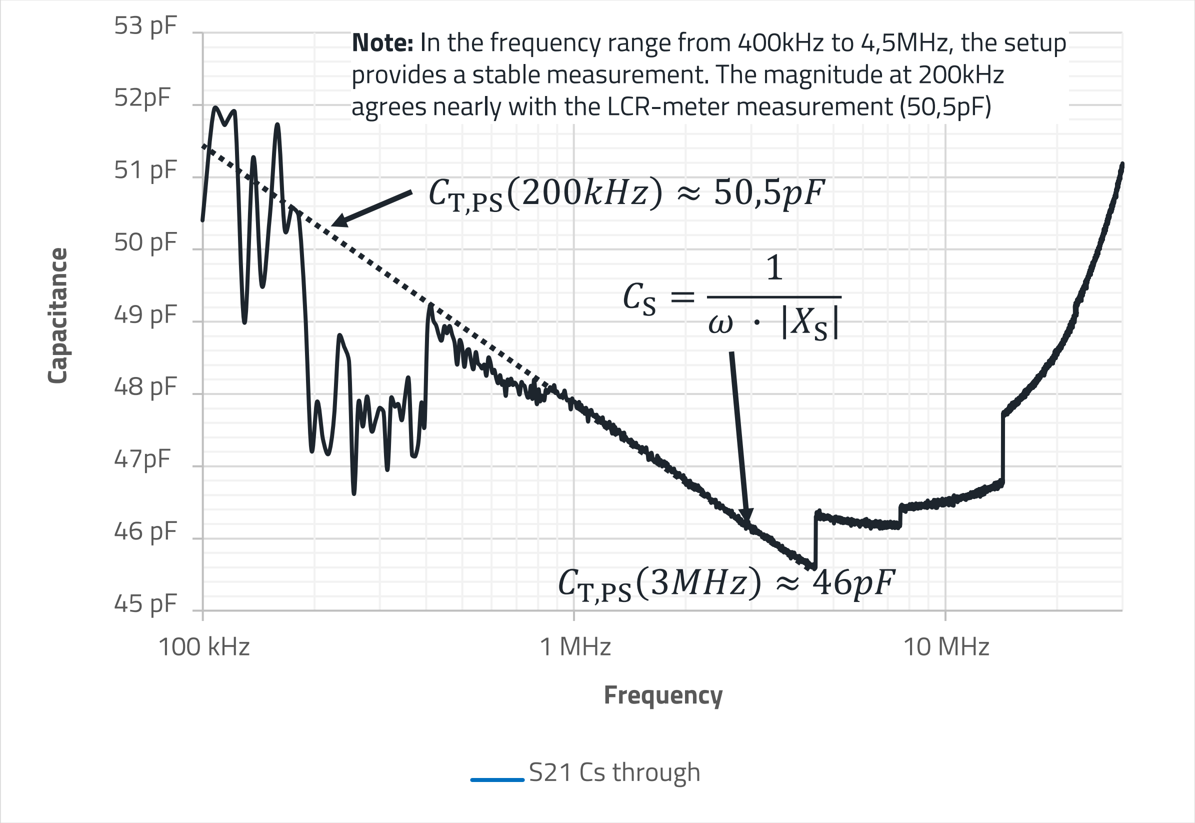
Test#5: Background – $C_{T,PS}$

Theory: Measuring $C_{T,PS}$ with VNA





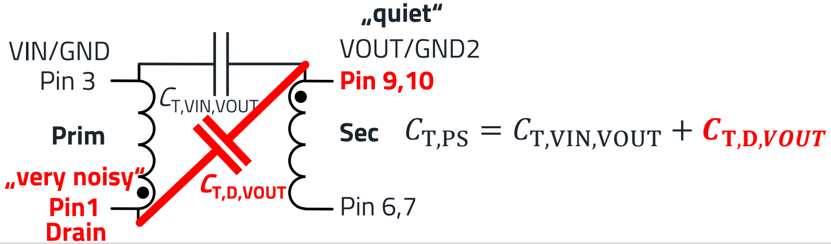
$|X_S|$

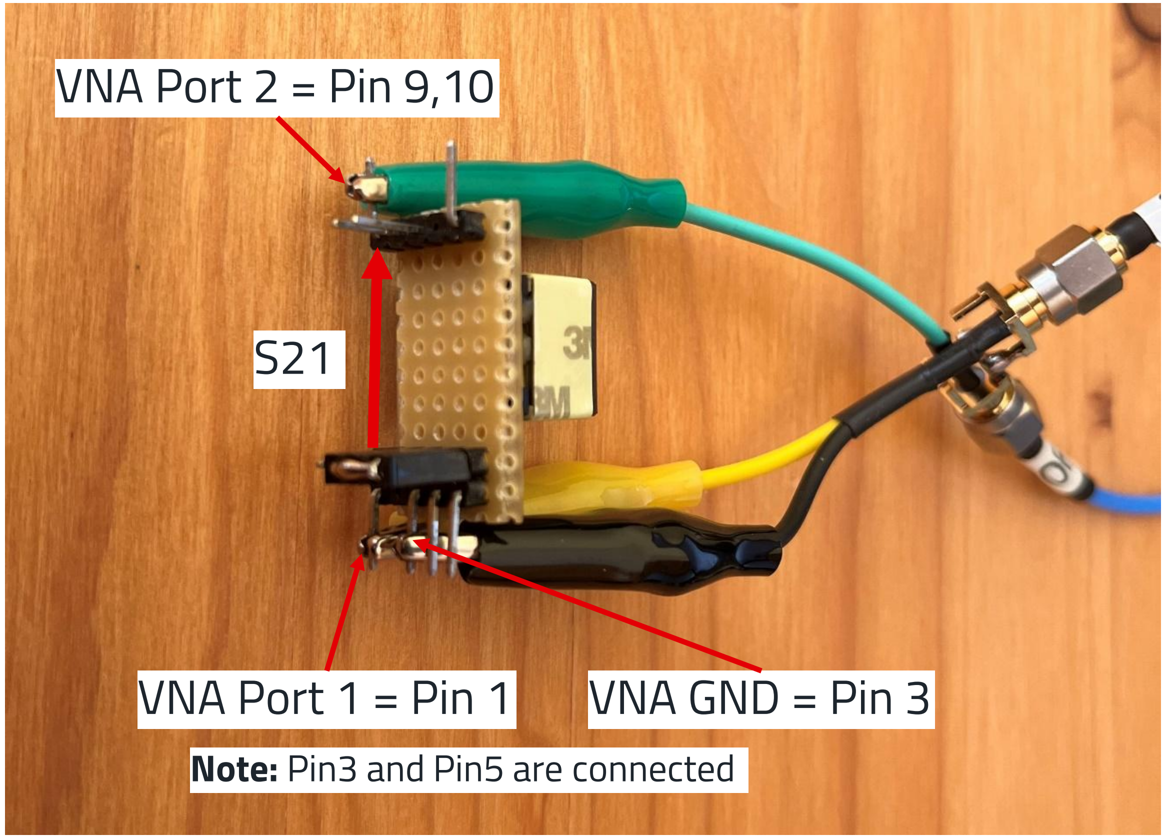


$C_{T,PS}$

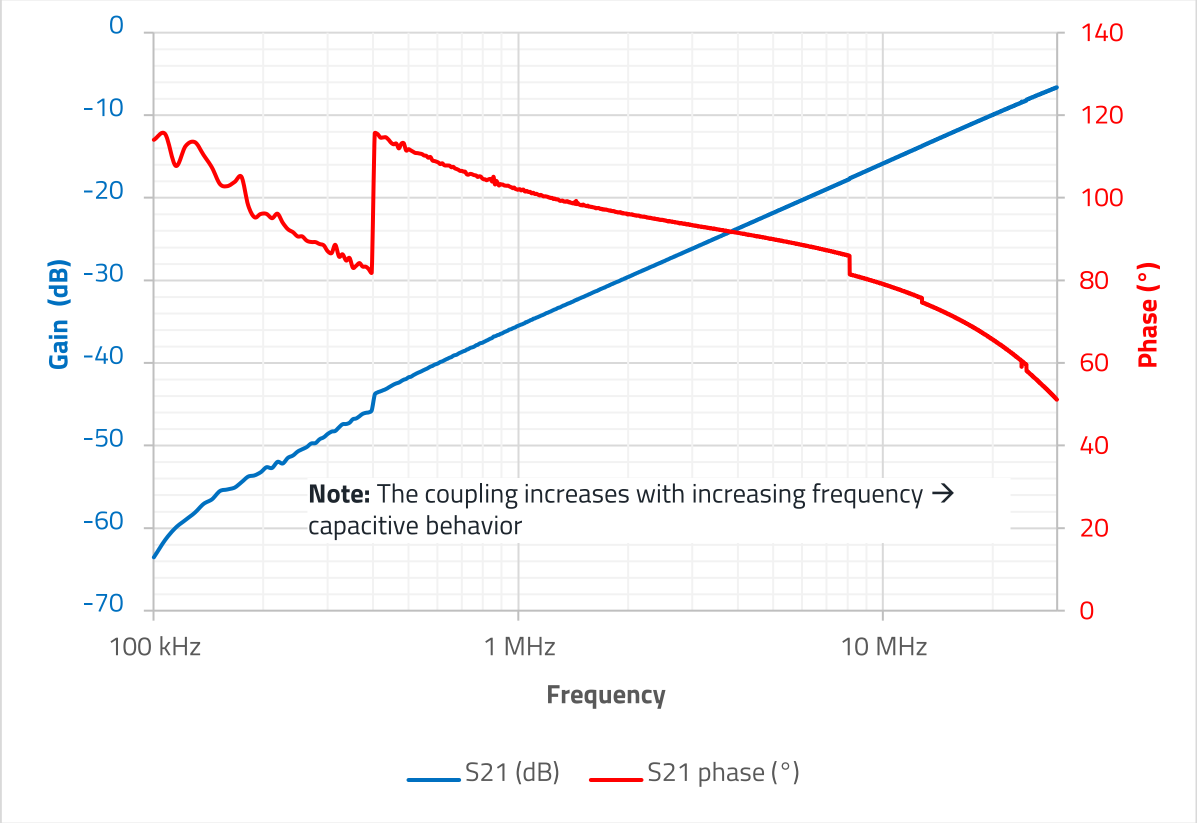
Test#5: Background – $C_{T,D,VOUT}$

Theory: Measuring $C_{T,D,VOUT}$ with VNA





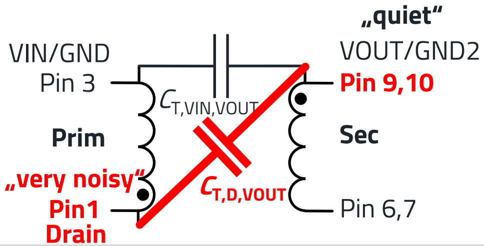
Measuring $C_{T,D,VOUT}$

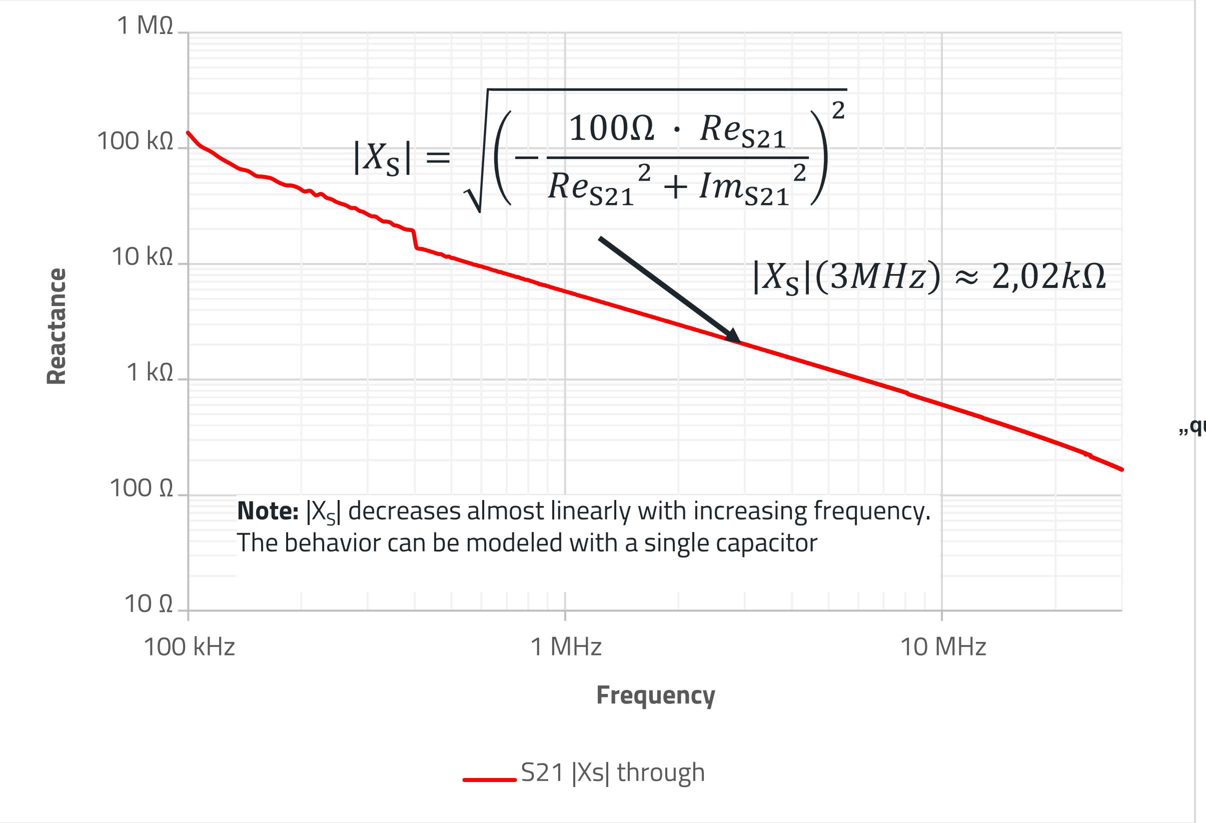


S21

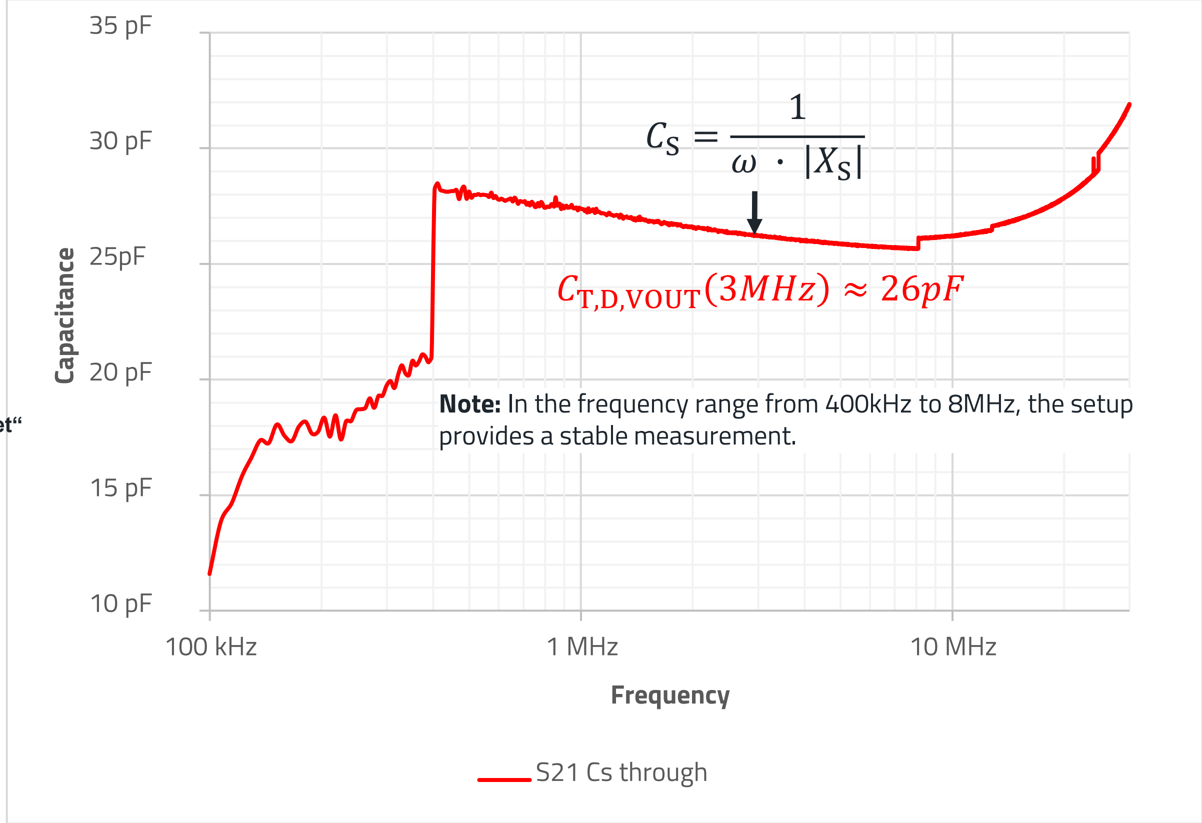
Test#5: Background – $C_{T,D,VOUT}$

Theory: Measuring $C_{T,D,VOUT}$ with VNA





„quiet“

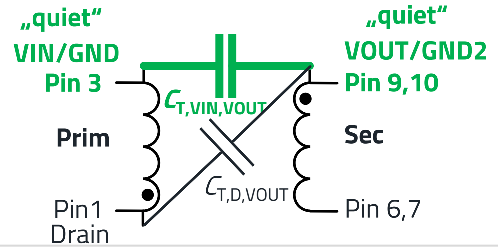


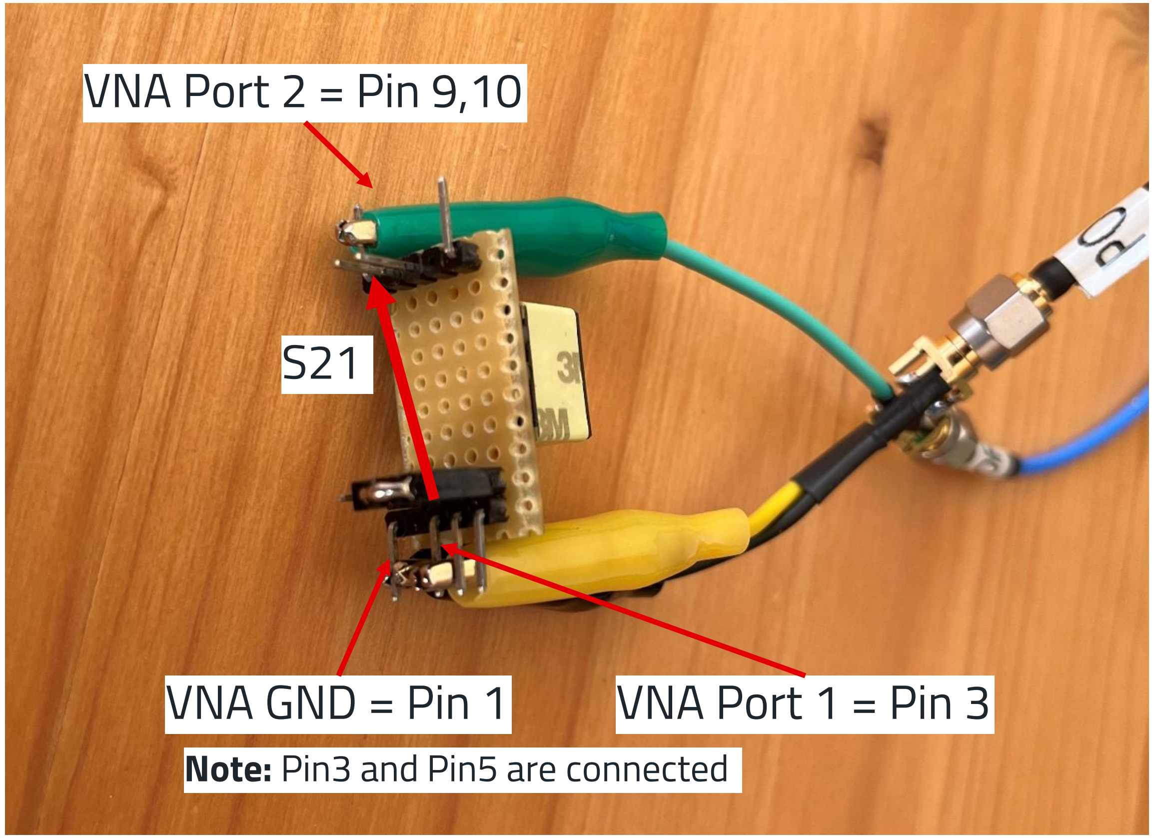
$|X_S|$

$C_{T,D,VOUT}$

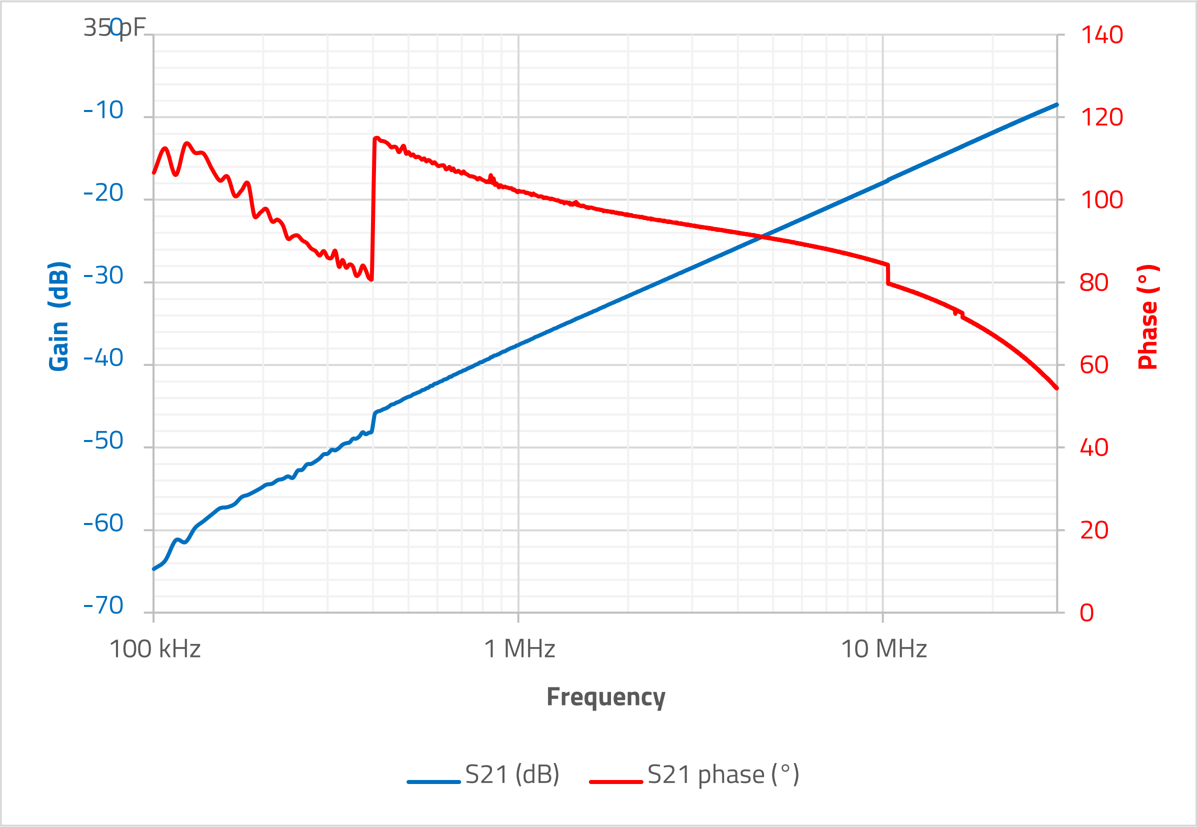
Test#5: Background – $C_{T,VIN,VOUT}$

Theory: Measuring $C_{T,VIN,VOUT}$ with VNA





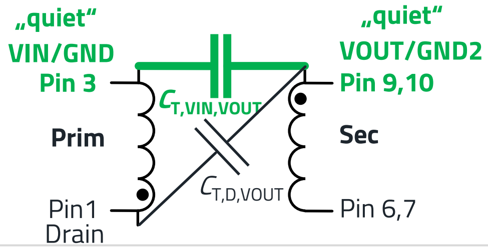
Measuring $C_{T,VIN,VOUT}$

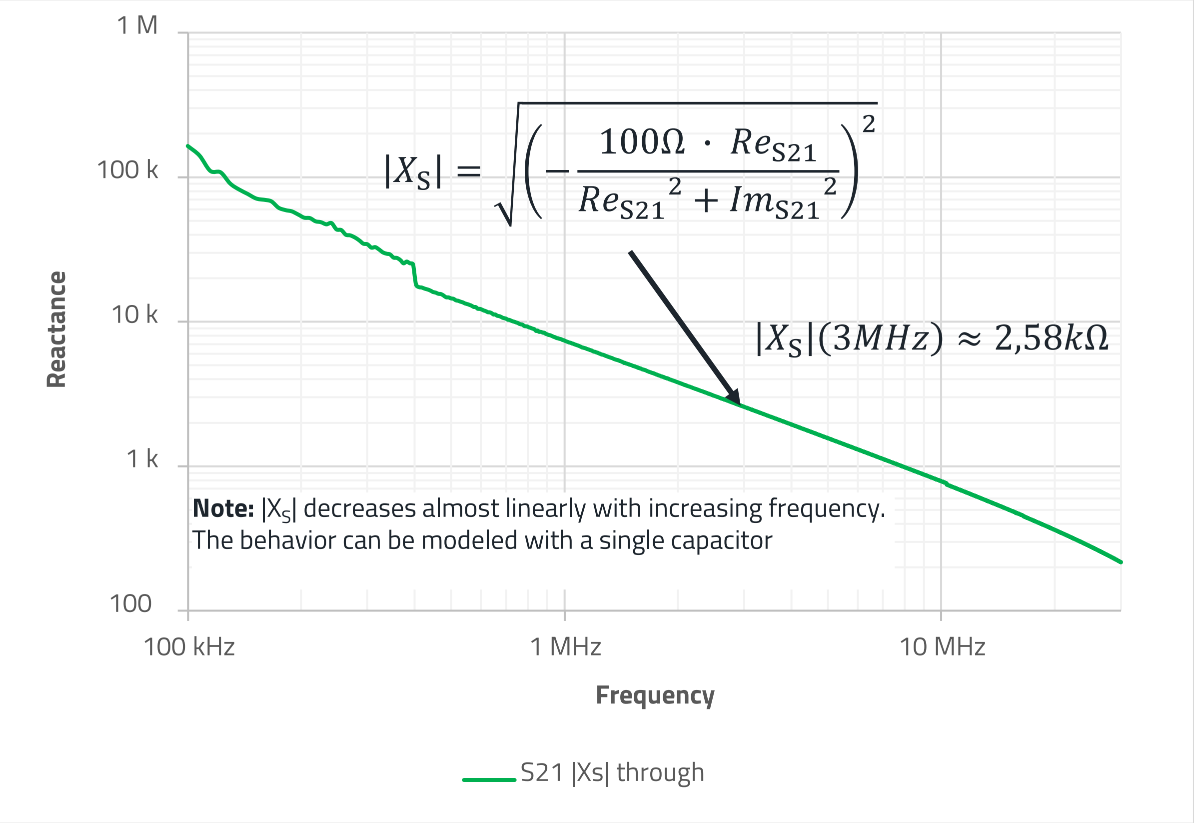


S21

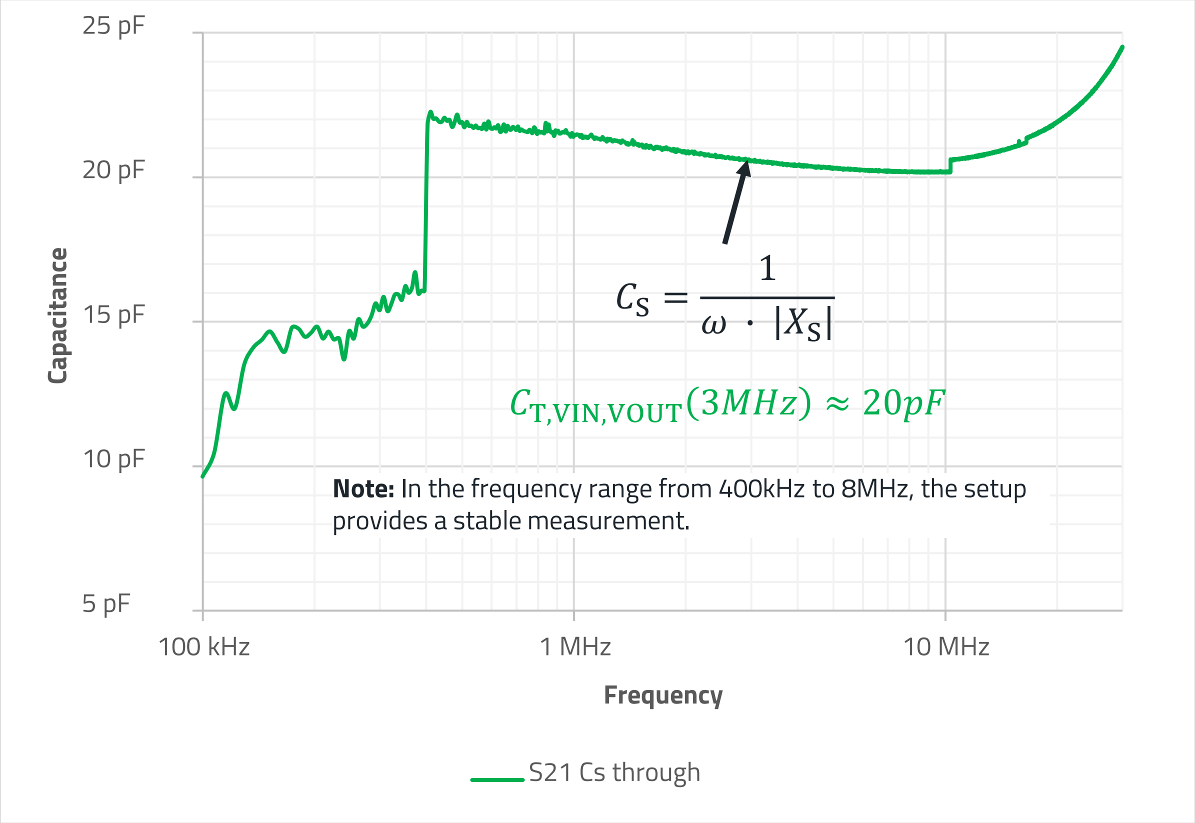
Test#5: Background – $C_{T,VIN,VOUT}$

Theory: Measuring $C_{T,VIN,VOUT}$ with VNA





$|X_S|$



$C_{T,VIN,VOUT}$

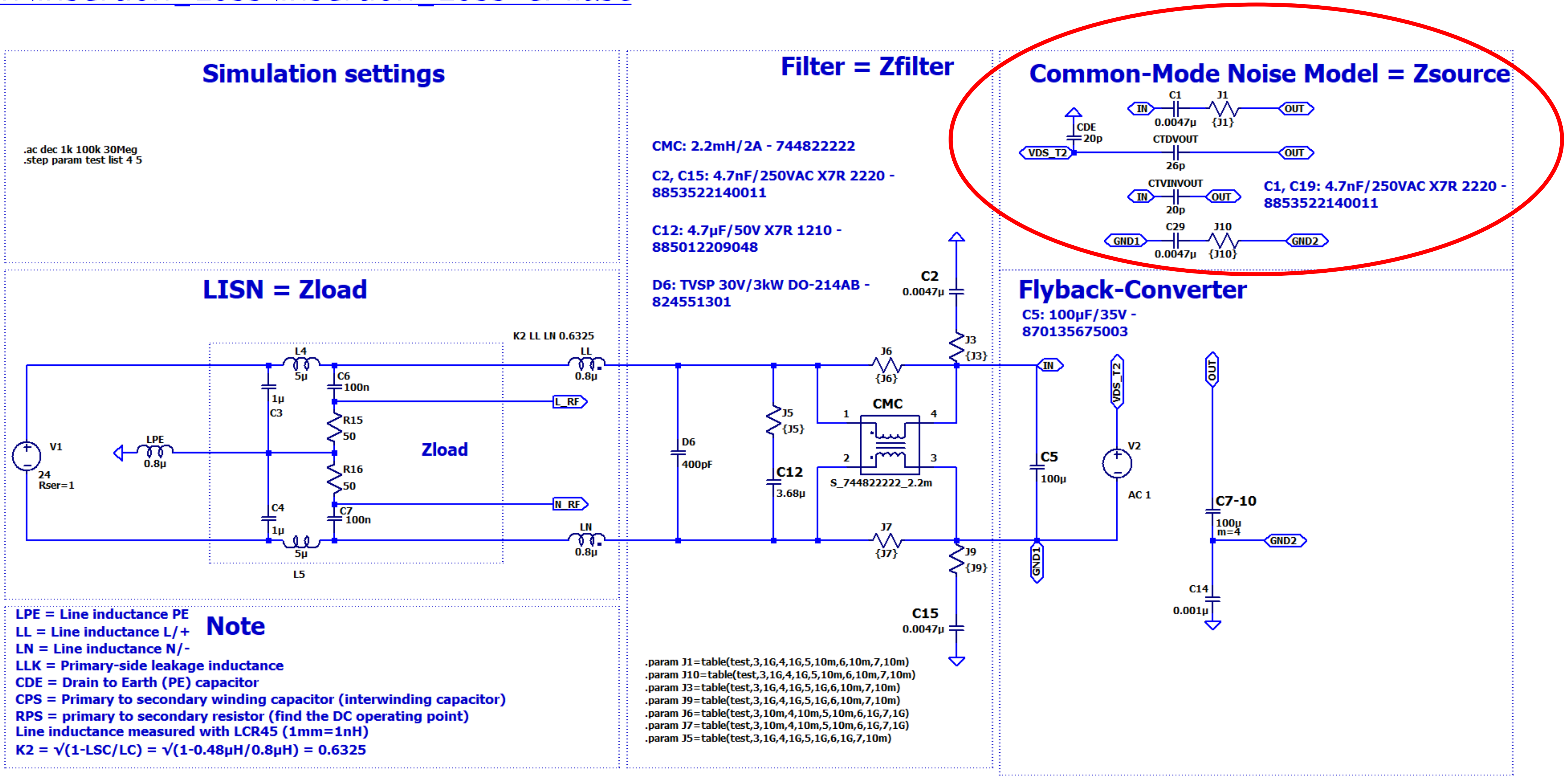
Test#5: Background - Lower noise level from switching frequency

Theory

- 2) The effective parasitic capacitance between switch node and reference ground is reduced
  - The CM noise is reduced as the effective parasitic capacitance acting against the switch node (drain) is reduced
  - It can be shown that approx. 26pF (@3MHz) of the interwinding capacitance ($C_{T,D,VOUT}$) acts from the switch node against the secondary-side
  - A large part of the resulting CM noise current is diverted directly through the Y-capacitors between the primary and secondary side (C1, C29)
  - This effect starts at the switching frequency (300kHz), which can also be shown in an LTspice simulation

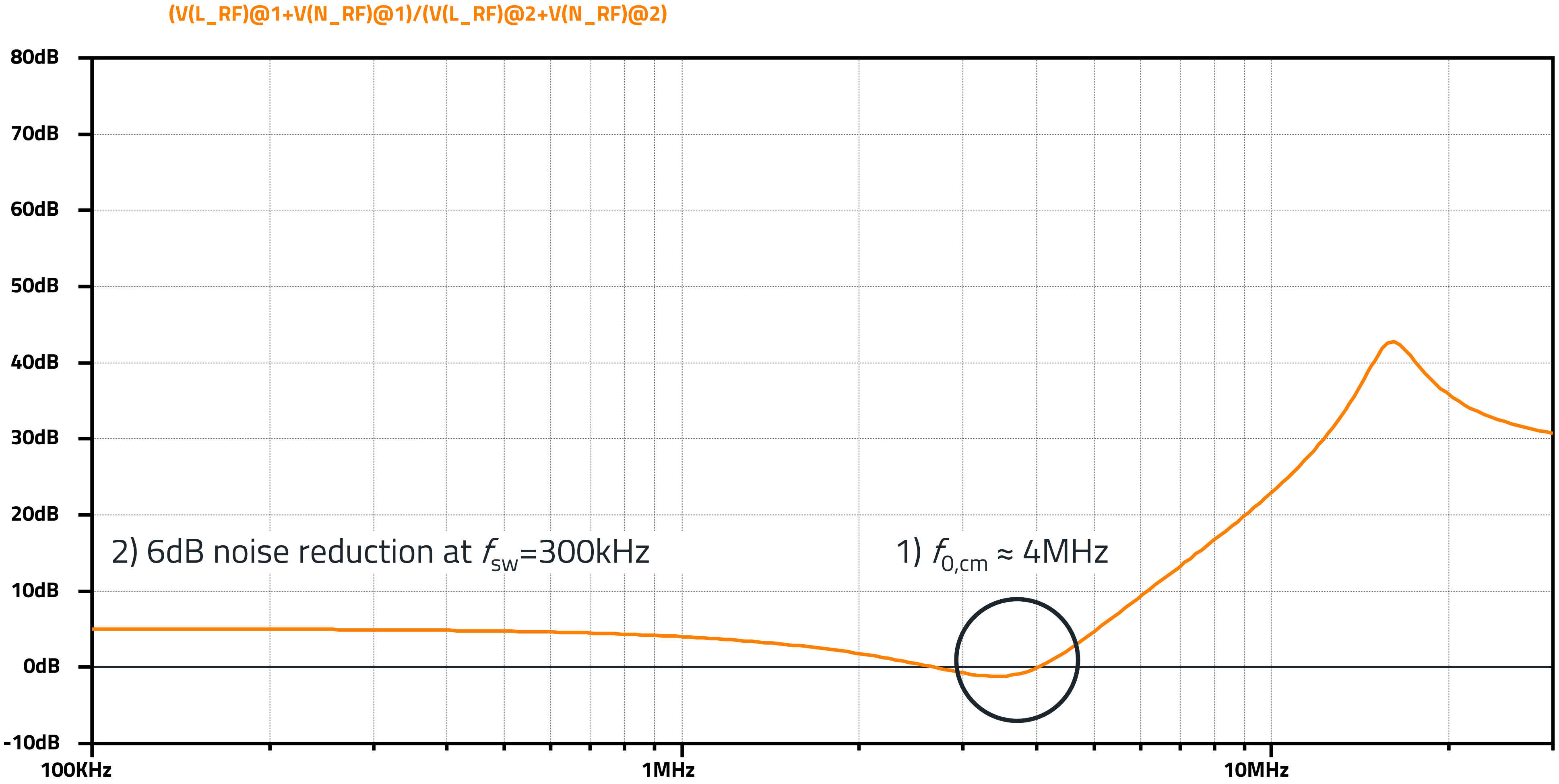
Test#5: Simulation - Conducted emissions - Insertion loss CM

Simulation\Insertion_Loss\Insertion_Loss-CM.asc

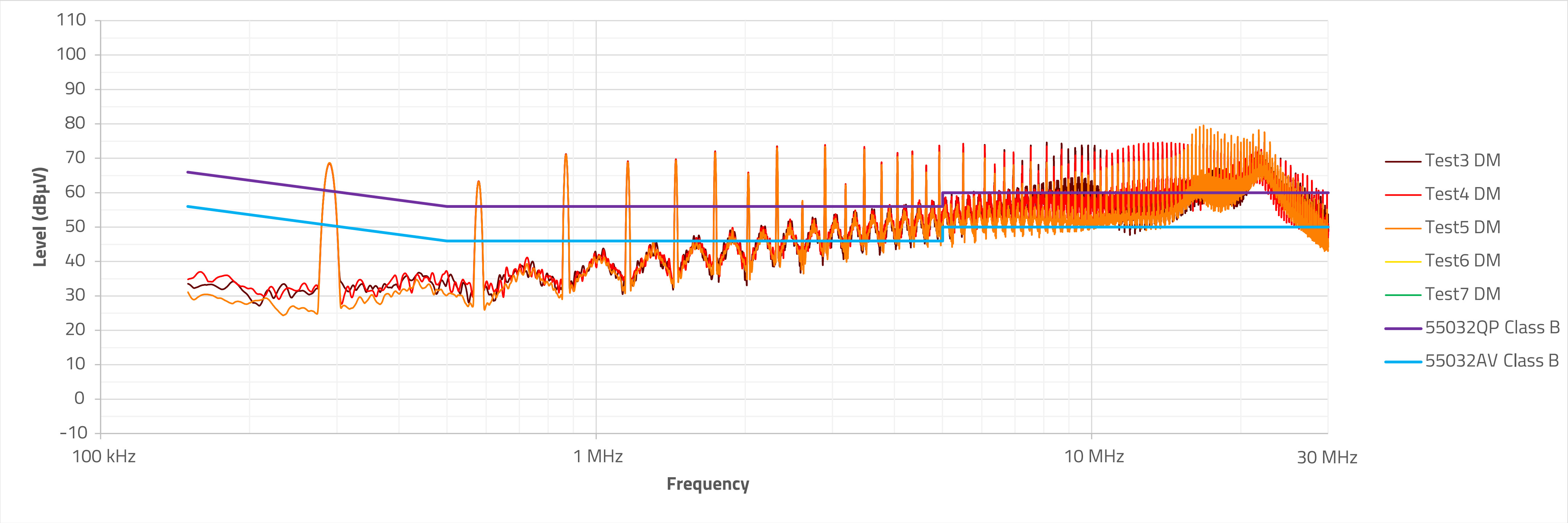


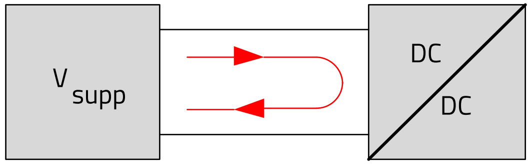
Test#5: Simulation - Conducted emissions - Insertion loss CM

Simulation\Insertion_Loss\Insertion_Loss-CM_Test5.asc



Test#5: Conducted emissions - Differential mode

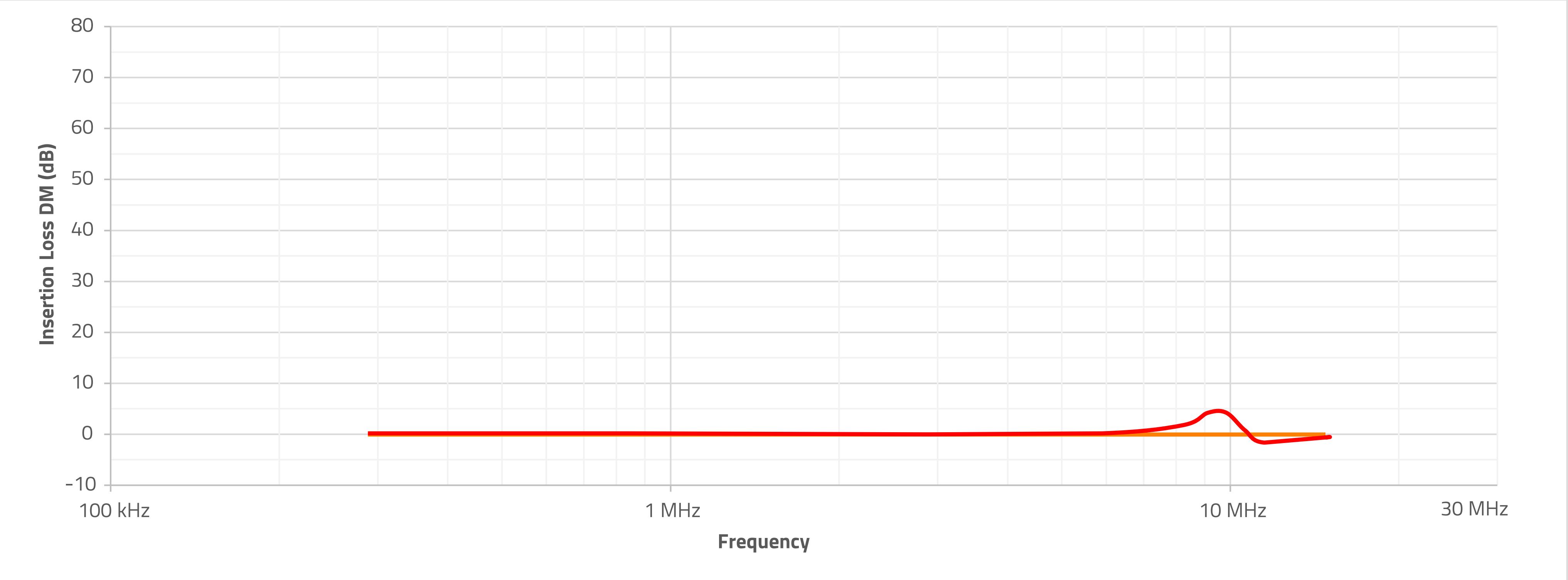


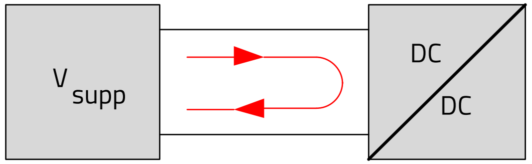


Name	Description
Test#3	Reference (no improvement)
Test#4	Test#3 + RCD-snubber
Test#5	Test#4 + primary to secondary y-capacitors

Differential Mode

Test#5: Conducted emissions - Insertion loss DM



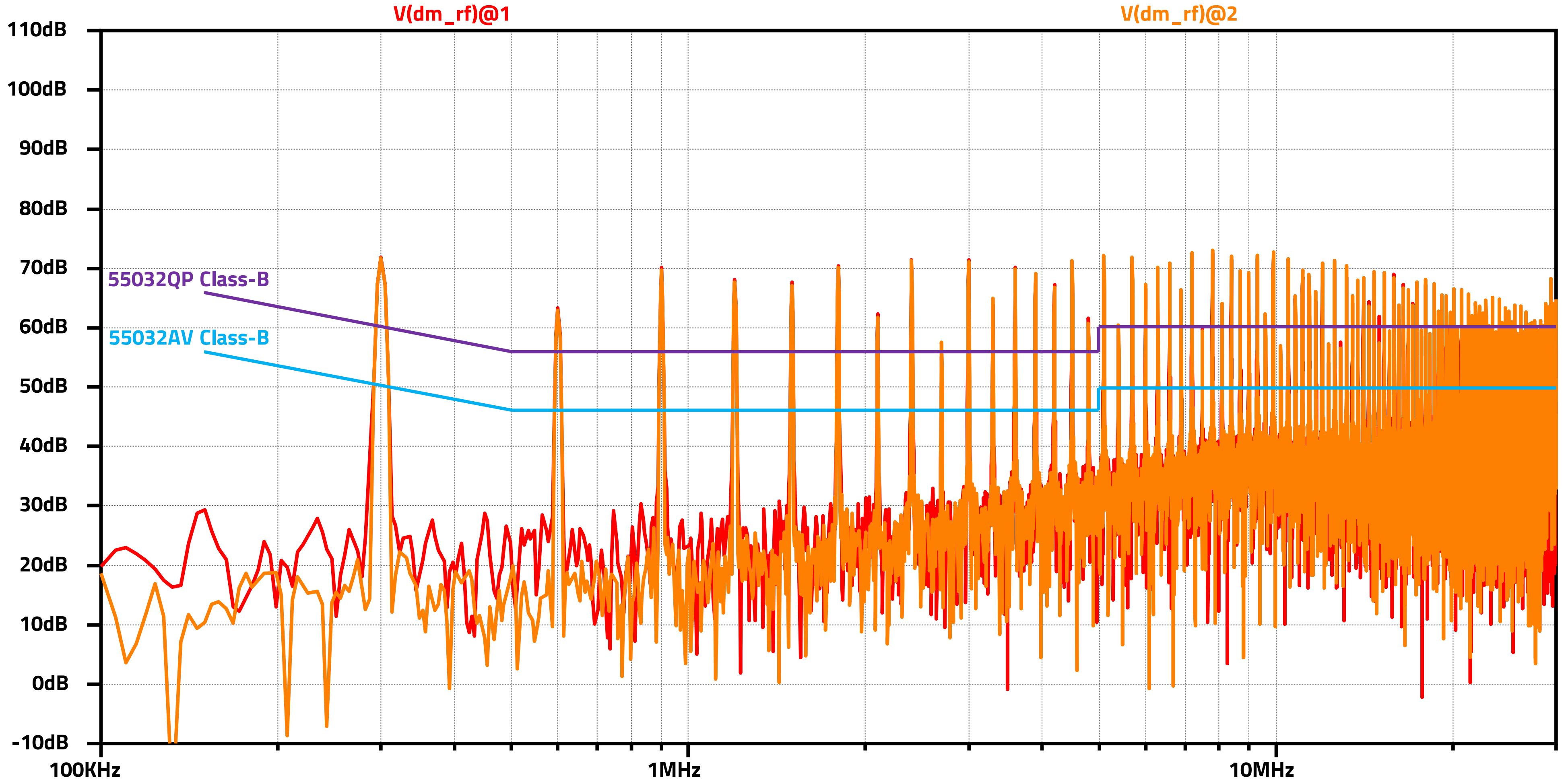


Description
+ RCD-snubber
+ primary to secondary y-capacitors

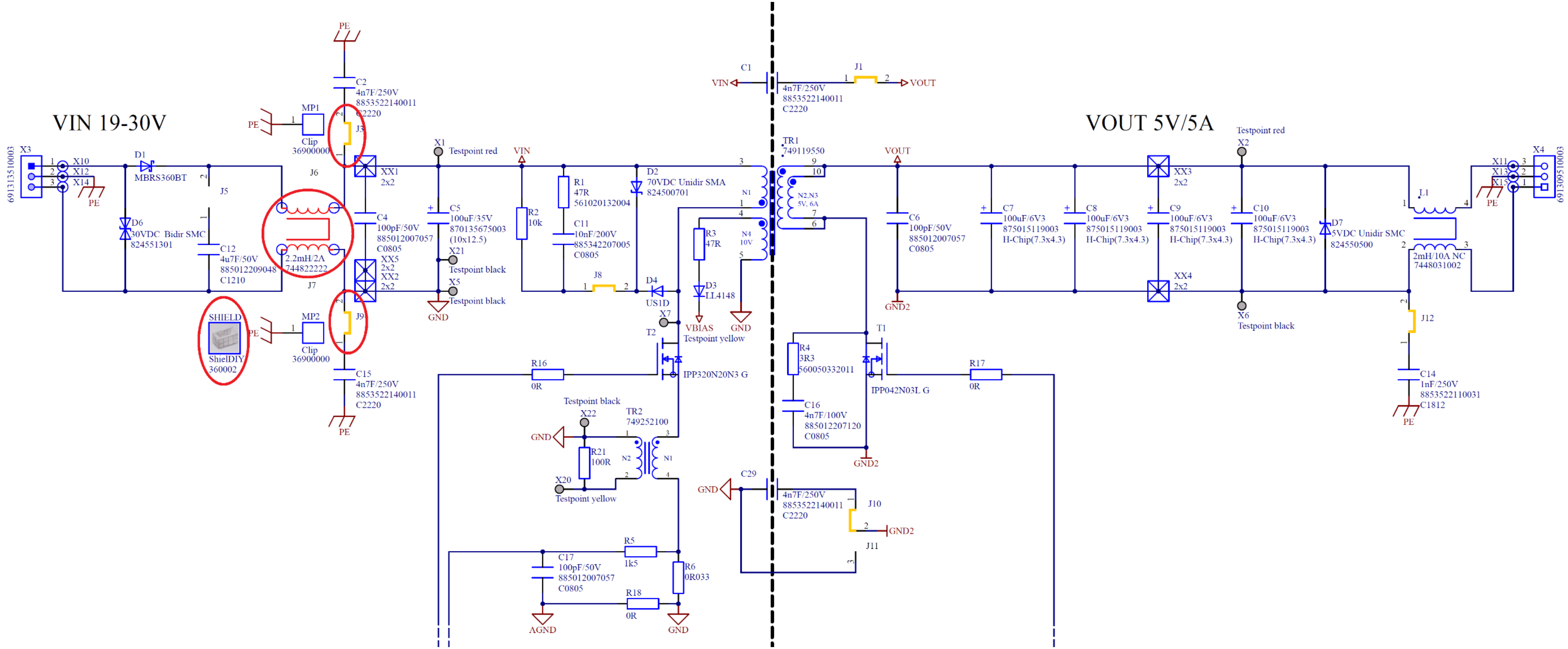
Differential Mode

Test#5b: Conducted emissions - Differential mode

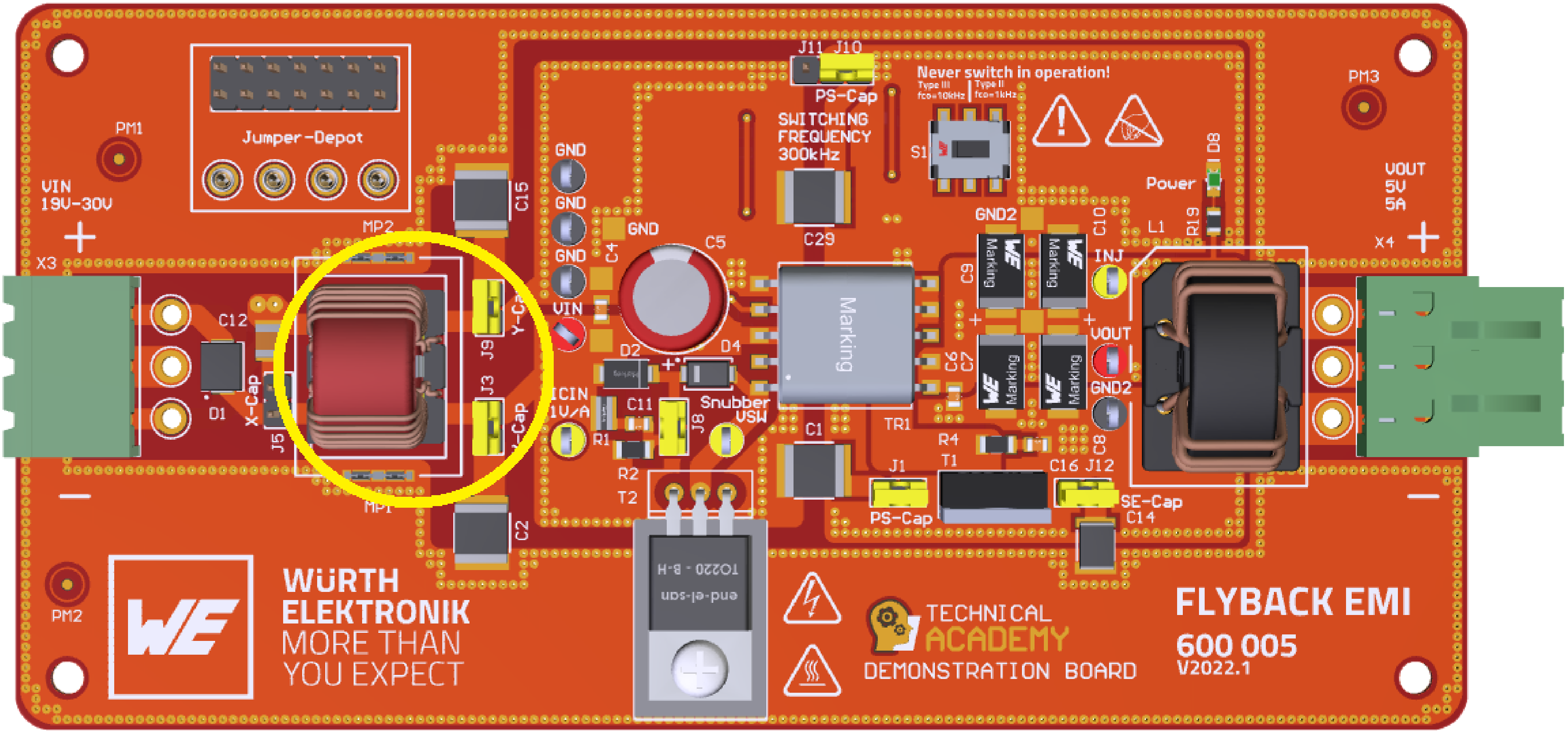
Simulation\Test1-7\Flyback_EMI_Test4-5b_FFT.asc



Test#6: Schematic



Test#6: Board configuration



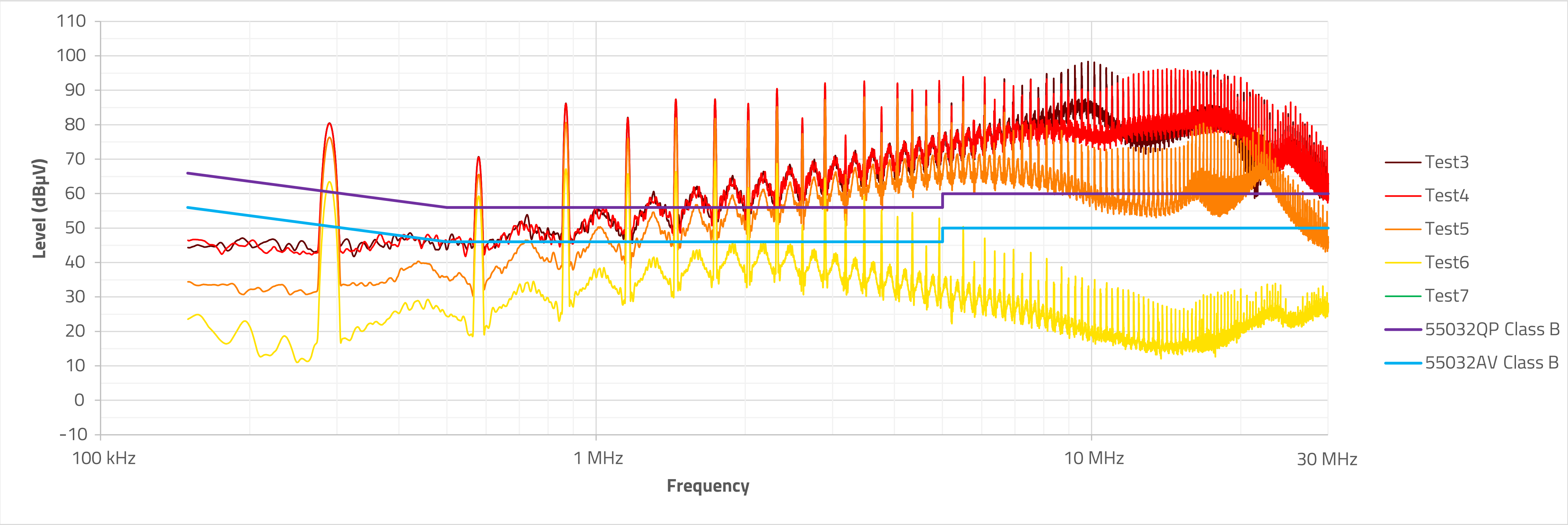
Test#6: Quiz

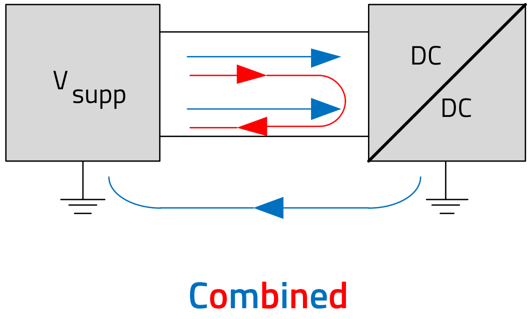
- Does the CMC have an influence on the differential-mode noise (without the X-capacitor)?

  - A: No, a CMC works in common mode, as the name suggests.

  - B: Yes, there is a differential-mode filter effect.

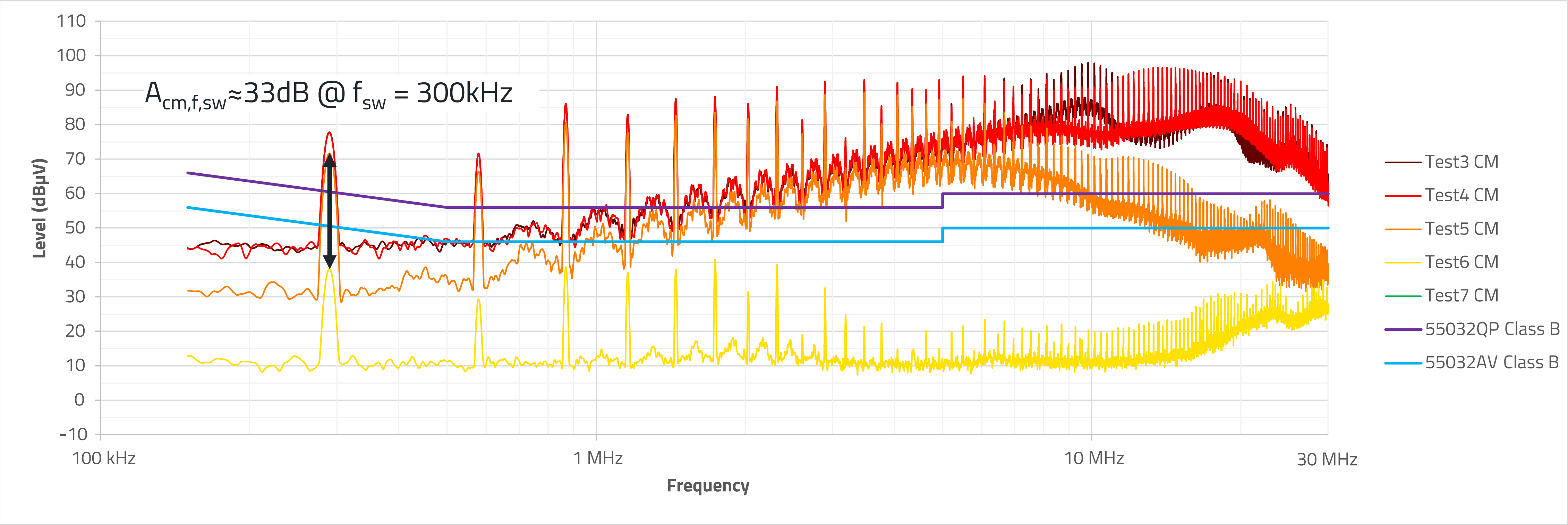
Test#6: Total conducted emissions - Line

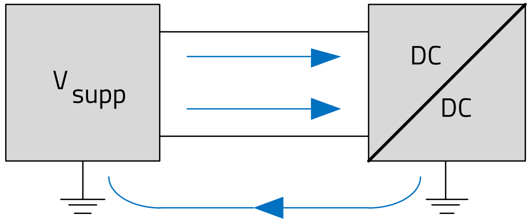




Name	Description
Test#3	Reference (no improvement)
Test#4	Test#3 + RCD-snubber
Test#5	Test#4 + primary to secondary y-capacitors
Test#6	Test#5 + CMC and y-capacitors (CM filter)

Test#6: Conducted emissions - Common mode

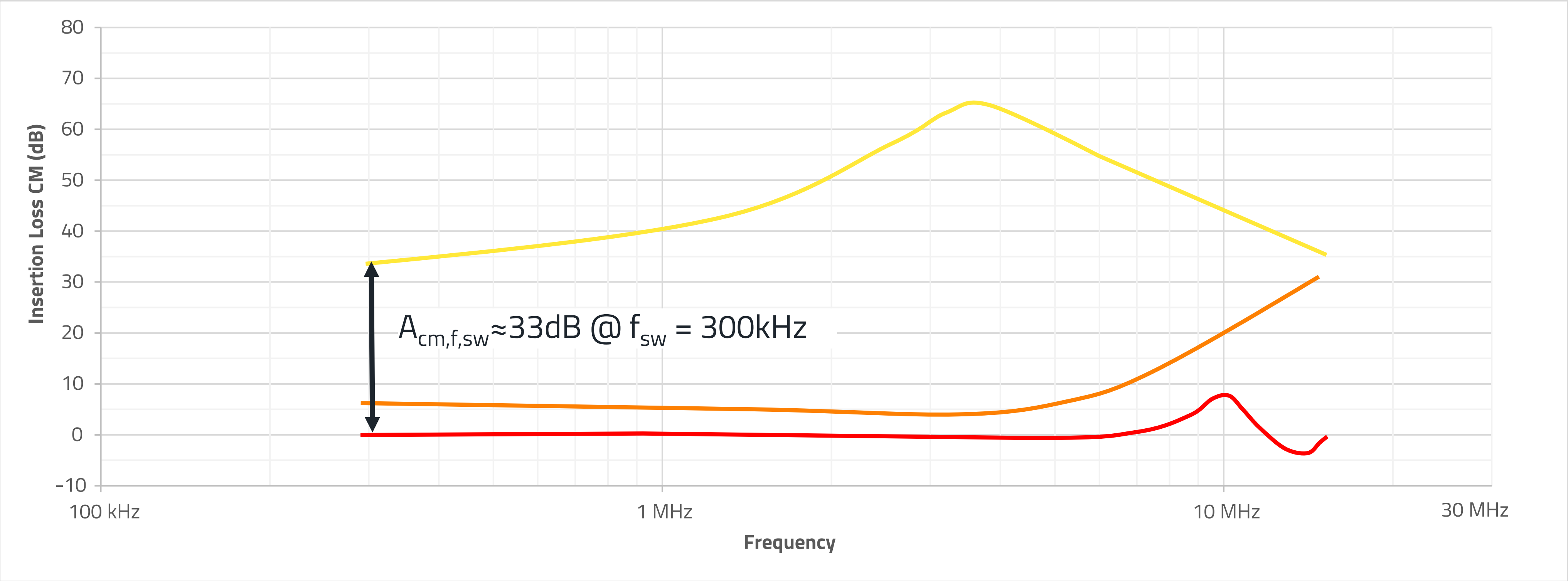


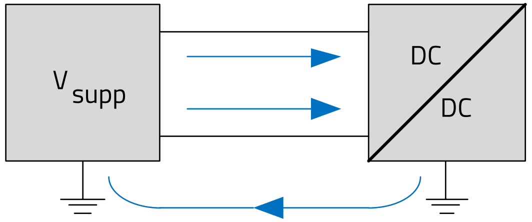


Common Mode

Name	Description
Test#3	Reference (no improvement)
Test#4	Test#3 + RCD-snubber
Test#5	Test#4 + primary to secondary y-capacitors
Test#6	Test#5 + CMC and y-capacitors (CM filter)

Test#6: Conducted emissions - Insertion loss CM



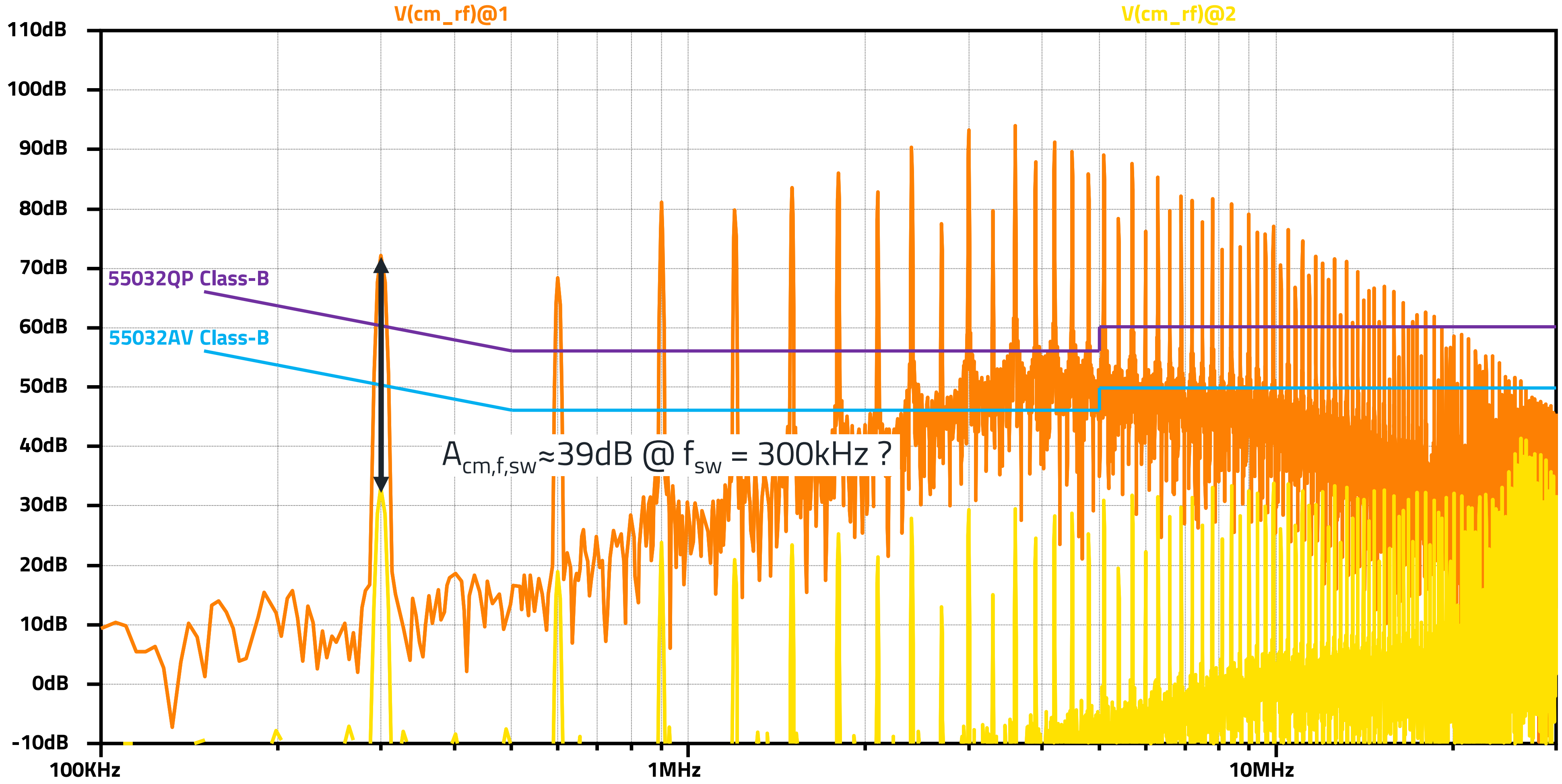


Common Mode

Description
+ RCD-snubber
+ primary to secondary y-capacitors
+ CMC and y-capacitors (CM filter)

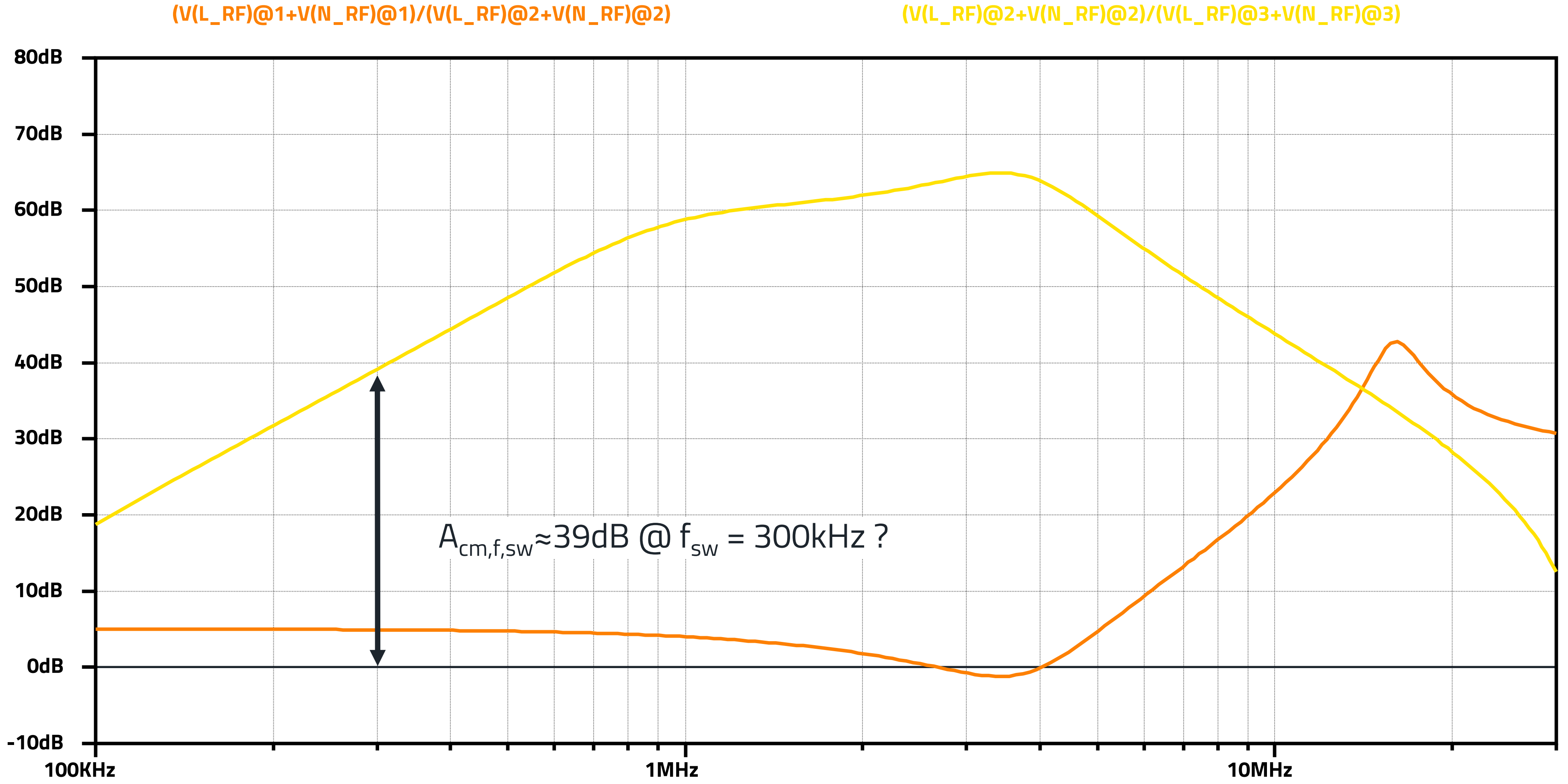
Test#6b: Simulation - Conducted emissions - Common mode

Simulation\Test1-7\Flyback_EMI_Test5-6b_FFT.asc



Test#6: Simulation - Conducted emissions - Insertion loss CM

[Simulation\Insertion_Loss\Insertion_Loss-CM_Test6.asc]()



Test#6: Background - CM-Filter

Theory

- The CM filter results from the inductance of the CMC and total capacitance to reference ground (overall Y-capacitance):
  - Inductance of the CMC = 2.2mH (744822222 – 2.2mH/2A, WE-CMB size S)
  - Y-capacitors C2/C15 = 2·4.7nF (8853522140011 – 4.7nF/250V, WCAP-CSSA)

$$f_{0,\mathrm{cm}} = \frac{1}{2\pi \cdot \sqrt{L_{\mathrm{cm}} \cdot C_{\mathrm{E,total}}}} = \frac{1}{2\pi \cdot \sqrt{L_{\mathrm{cm}} \cdot (2 \cdot C_{\mathrm{y}} + C_E)}} = \frac{1}{2\pi \cdot \sqrt{2.2mH \cdot (2 \cdot 4.7nF + 0.904nF)}} \approx 33.4kHz$$

$$A_{\mathrm{cm,f,sw}} = \log\left(\frac{f_{\mathrm{sw}}}{f_{0,\mathrm{cm}}}\right) \cdot 40dB = \log\left(\frac{300kHz}{33.4kHz}\right) \cdot 40dB \approx 38dB$$

Test#6: Background - CM-Filter

Selection

1. Selection of the Y-capacitors:
   - 8853522140011 (4.7nF/X7R/250V)

2. Cutoff frequency of the input filter min. @ 1/10 of the switching frequency of the switching regulator:
   - 300kHz/10 = 30kHz

3. Calculation of inductance:

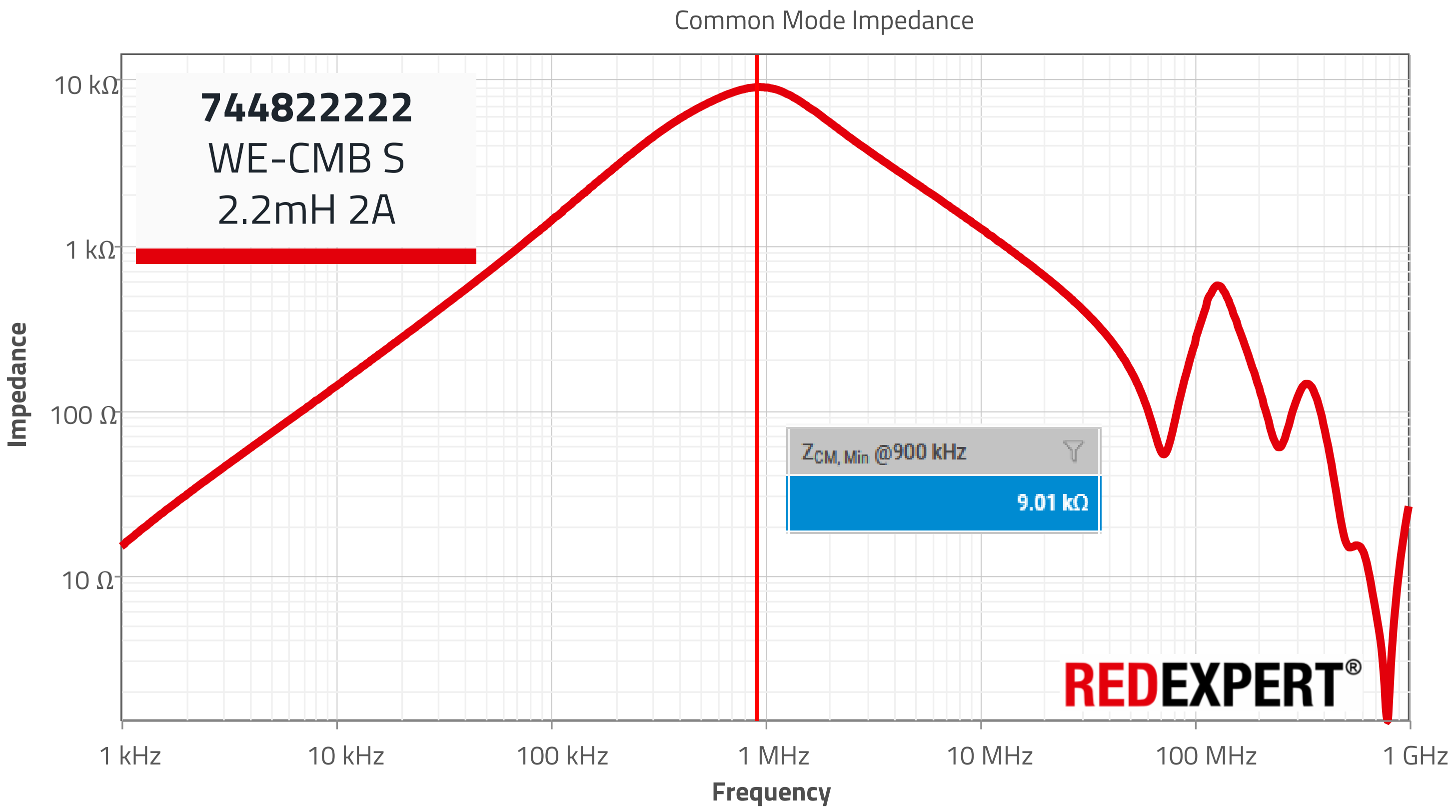
$$f_{0,\mathrm{cm}} = \frac{1}{2\pi\sqrt{LC}} \rightarrow L_{\mathrm{cm}} = \frac{1}{(2\pi f_{0,\mathrm{cm}})^2 \cdot C_{\mathrm{E,total}}} = \frac{1}{(2\pi \cdot 30kHz)^2 \cdot 2 \cdot 4.7nF} = 3mH$$

4. Selection of the component:
   - 744822222 (2.2mH/2A)
   - Due to smaller winding losses, SRF near the 3rd harmonic (900kHz)

Test#6: Background - CM-Filter

REDEXPERT: Common-mode impedance

- The attenuation of the CM filter is limited by the natural resonance of the CMC



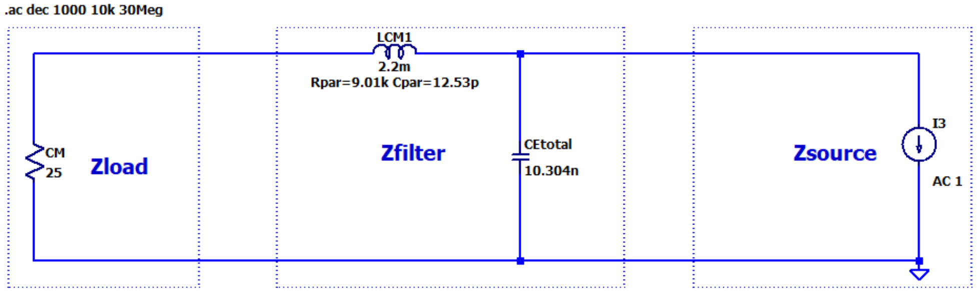
$$A_{\text{cm,max}} = \log\left(\frac{f_{\text{res,cmc}}}{f_{0,\text{cm}}}\right) \cdot 40dB$$

$$A_{\text{cm,max}} = \log\left(\frac{900kHz}{33{,}4kHz}\right) \cdot 40dB \approx 57dB$$

Test#6: Background - CM-Filter

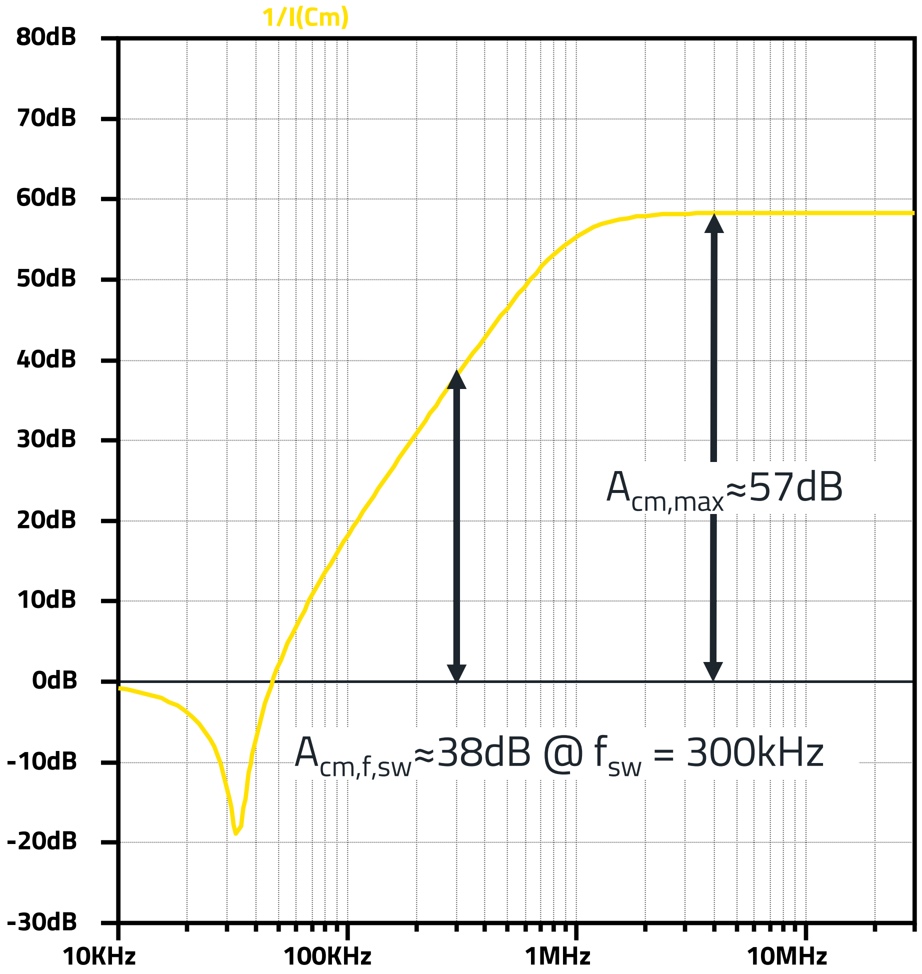
Simulation\Insertion_Loss\Insertion_Loss-CM_simple.asc

Insertion Loss CM:
Zload << ZOUTfilter
simplified AC-CM-model

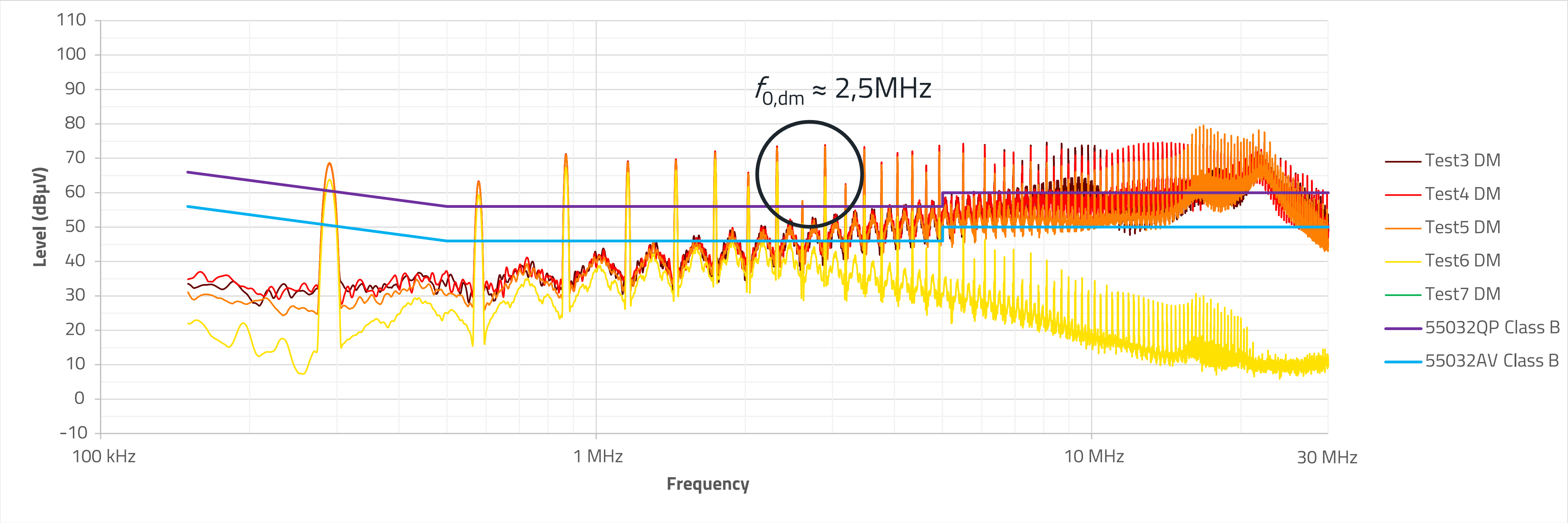


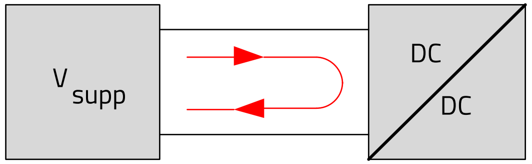
LCM = L2 = 2.2mH
CE = (C1+C29)*C14/(C1+C29 +C14) = (4.7nF+4.7nF)*1nF/(4.7nF+4.7nF+1nF) = 0.904n
2*CY = C2+C15 = 4.7nF+4.7nF = 9.4nF
CEtotal = 2*Cy+CE = 9.4nF+0.904nF = 10.304nF

Cpar = 1/(2*π*f*ZCM@10MHz) = 1/(2*π*10MHz*1.27kΩ)=12.53pF
Rpar = ZCM@fRes = 9.01kΩ
f0,cm= fLC =1/(2π*√(LCM*CEtotal))= 1/(2π*√(2.2mH*10.304nF))
= 33.4kHz (double pole / loss: +40dB/Decade)
fres,cmc= 900kHz (double zero / loss: -40dB/Decade)
Acm,f,sw = log(fsw/f0,cm)*40dB =log(300kHz/33,4kHz)*40dB = 38dB
Acm,max = log(900kHz/33.4kHz)*40dB = 57dB



Test#6: Conducted emissions - Differential mode

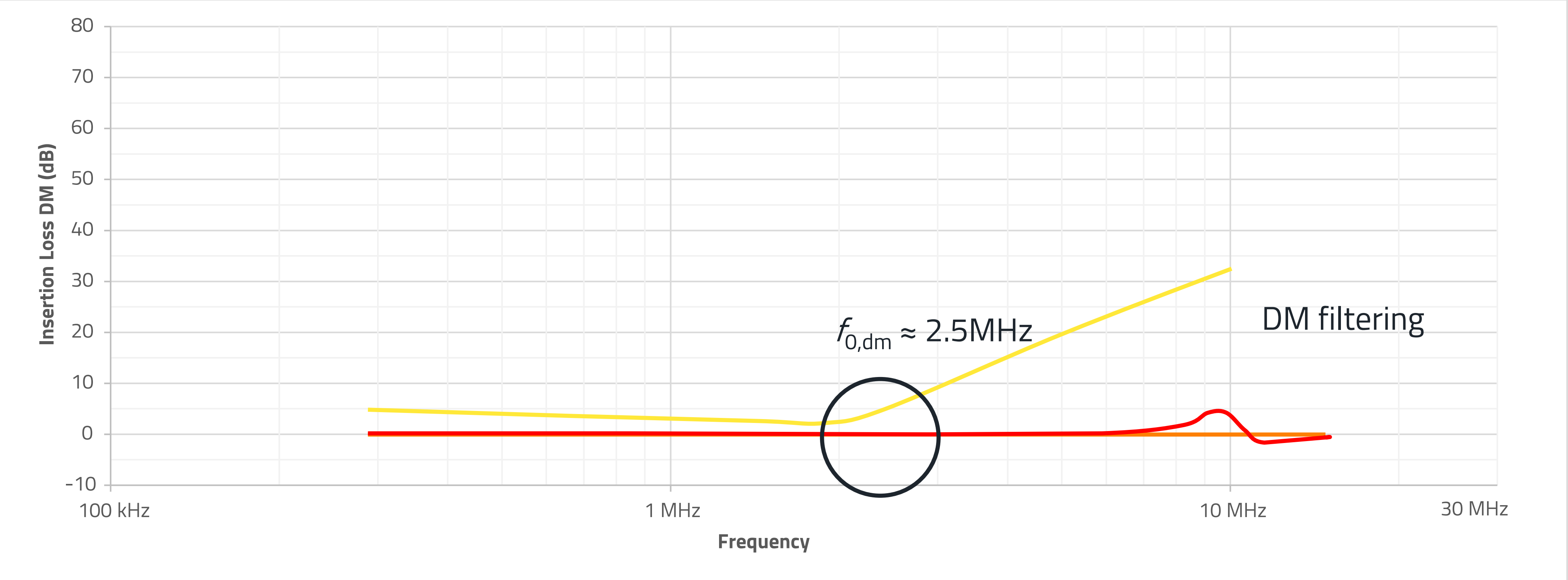


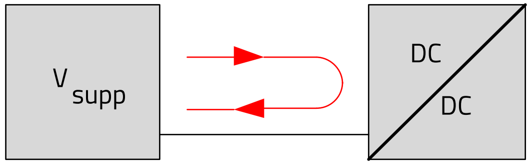


Name	Description
Test#3	Reference (no improvement)
Test#4	Test#3 + RCD-snubber
Test#5	Test#4 + primary to secondary y-capacitors
Test#6	Test#5 + CMC and y-capacitors (CM filter)

Differential Mode

Test#6: Conducted emissions - Insertion loss DM



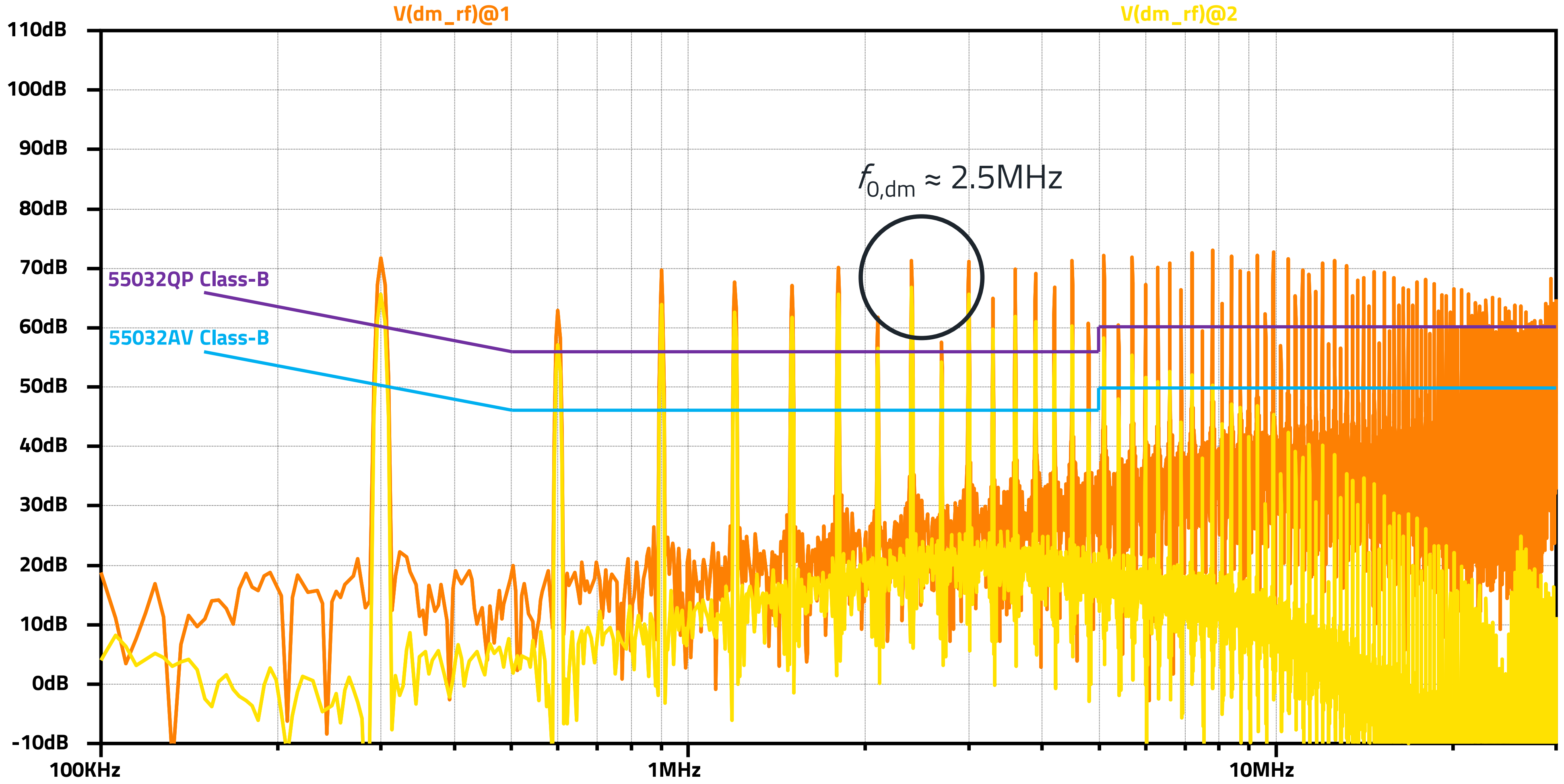


Description
+ RCD-snubber
+ primary to secondary y-capacitors
+ CMC and y-capacitors (CM filter)

Differential Mode

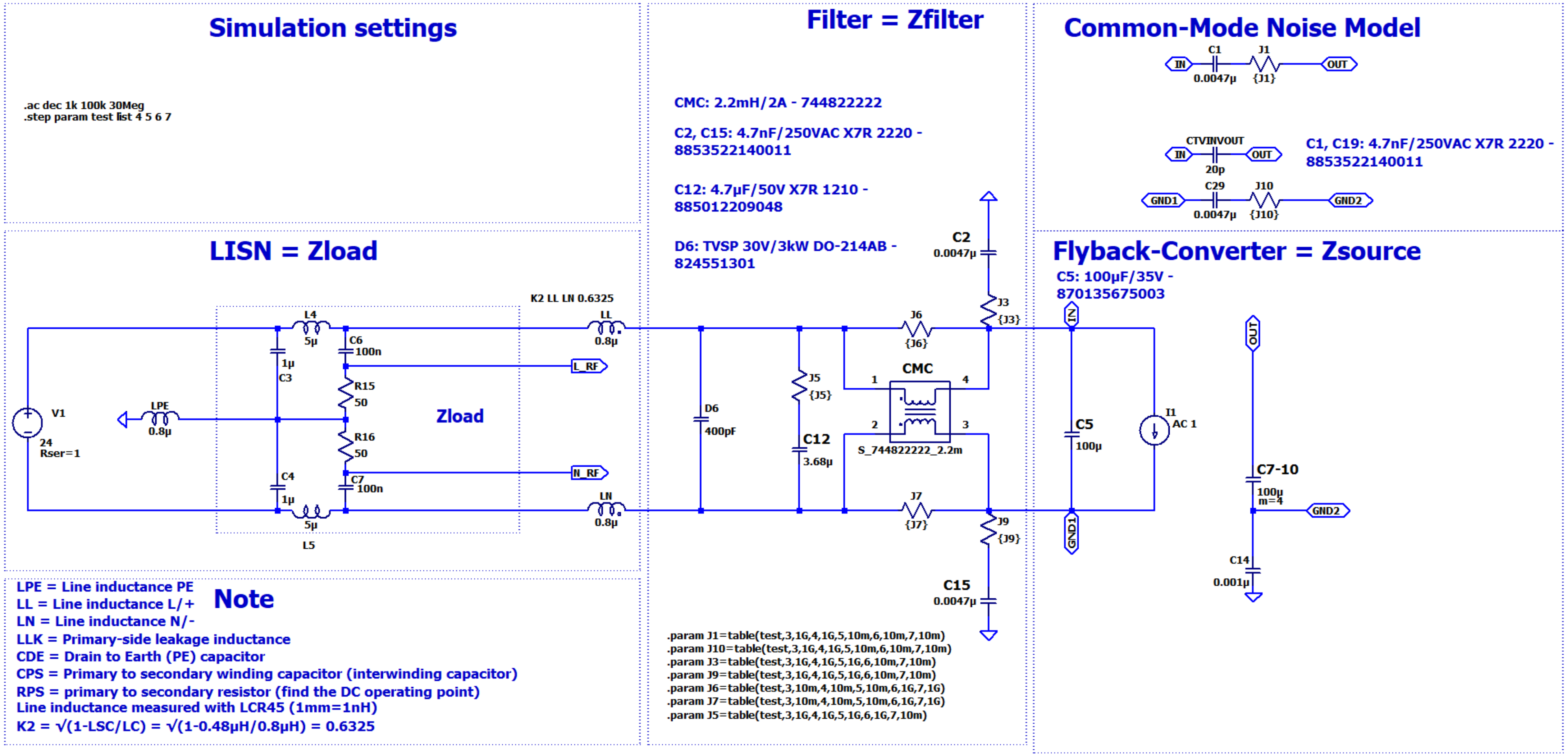
Test#6b: Simulation - Conducted emissions - Differential mode

Simulation\Test1-7\Flyback_EMI_Test5-6b_FFT.asc



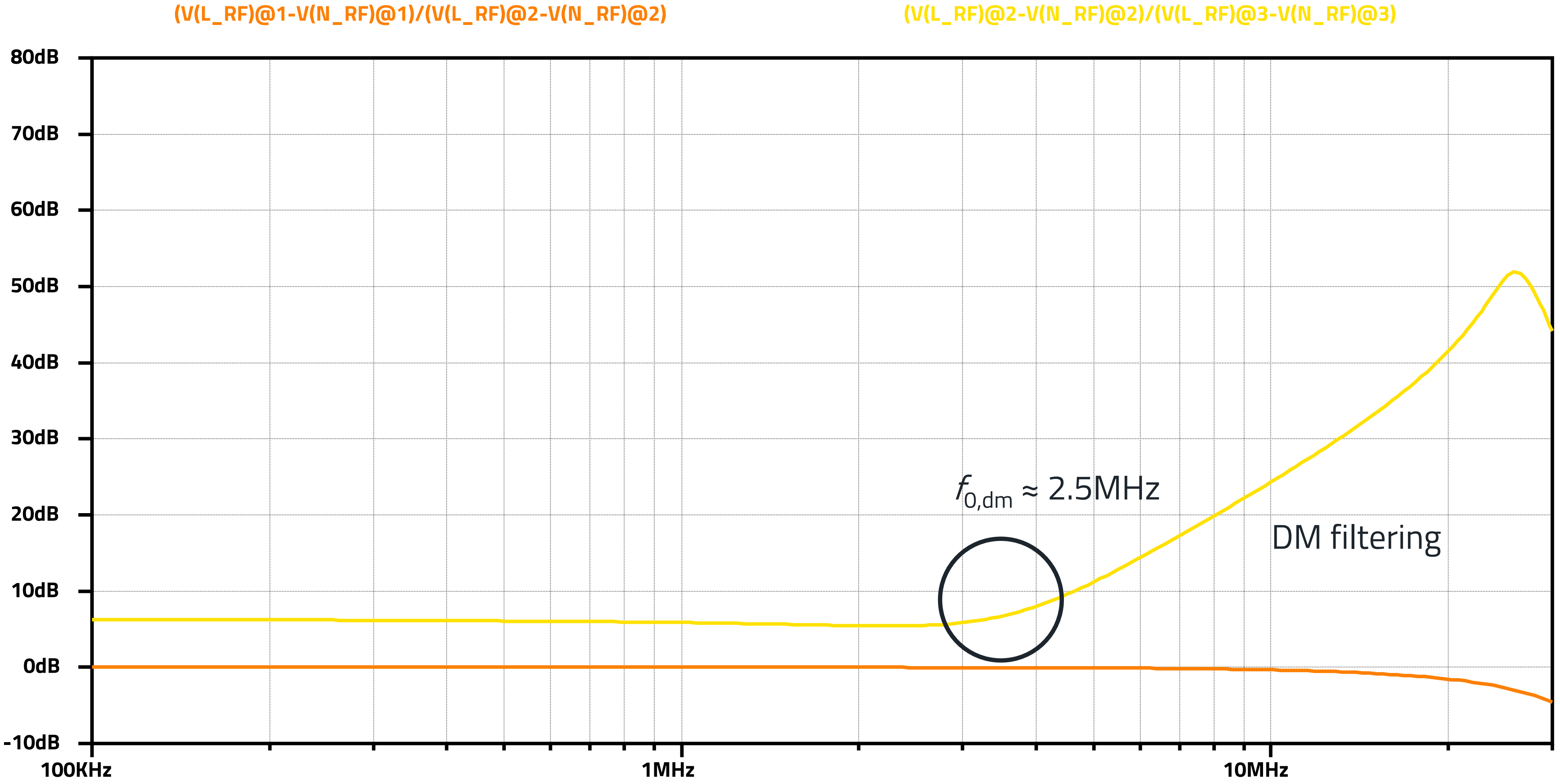
Test#6: Simulation - Conducted emissions - Insertion loss DM

Simulation\Insertion_Loss\Insertion_Loss-DM.asc



Test#6: Simulation - Conducted emissions - Insertion loss DM

Simulation\Insertion_Loss\Insertion_Loss-DM_Test6.asc



Test#6: Quiz

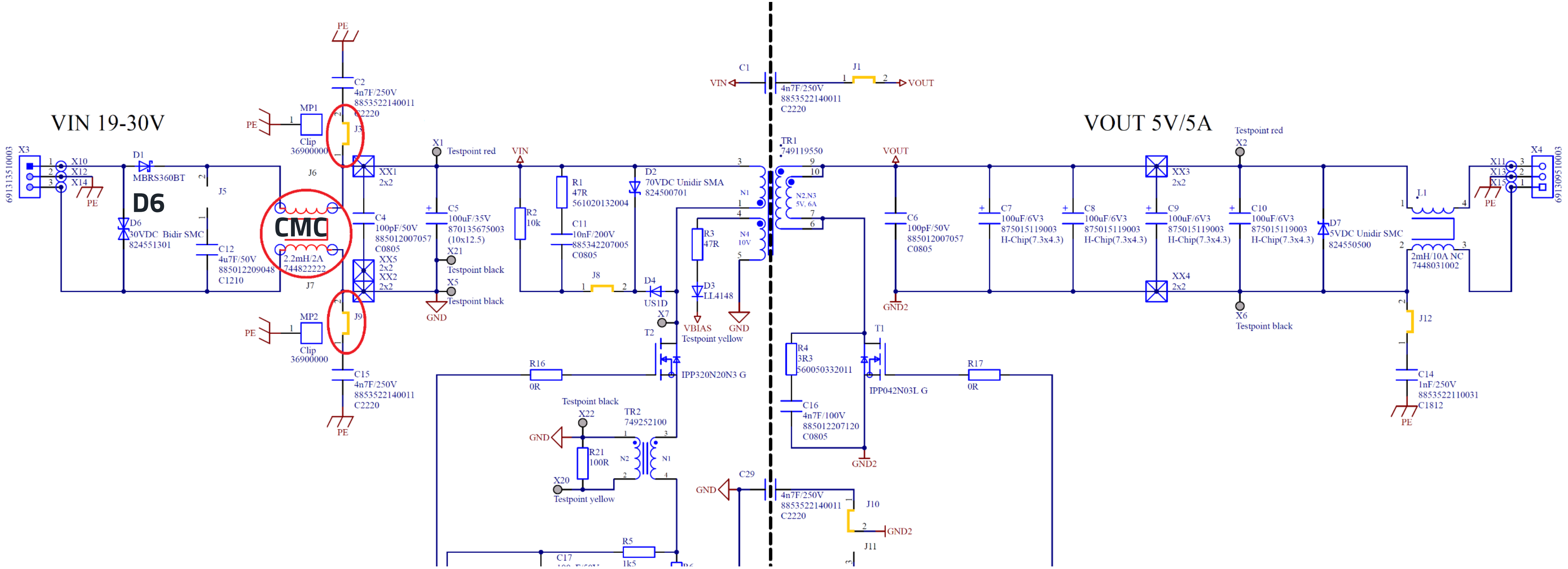
Answer

- Does the CMC have an influence on the differential-mode noise (without the X-capacitor)?

  - A: No, a CMC works in common mode, as the name suggests.

  - **B: Yes, there is a differential-mode filter effect.**

Test#6: Background - DM-Filtering

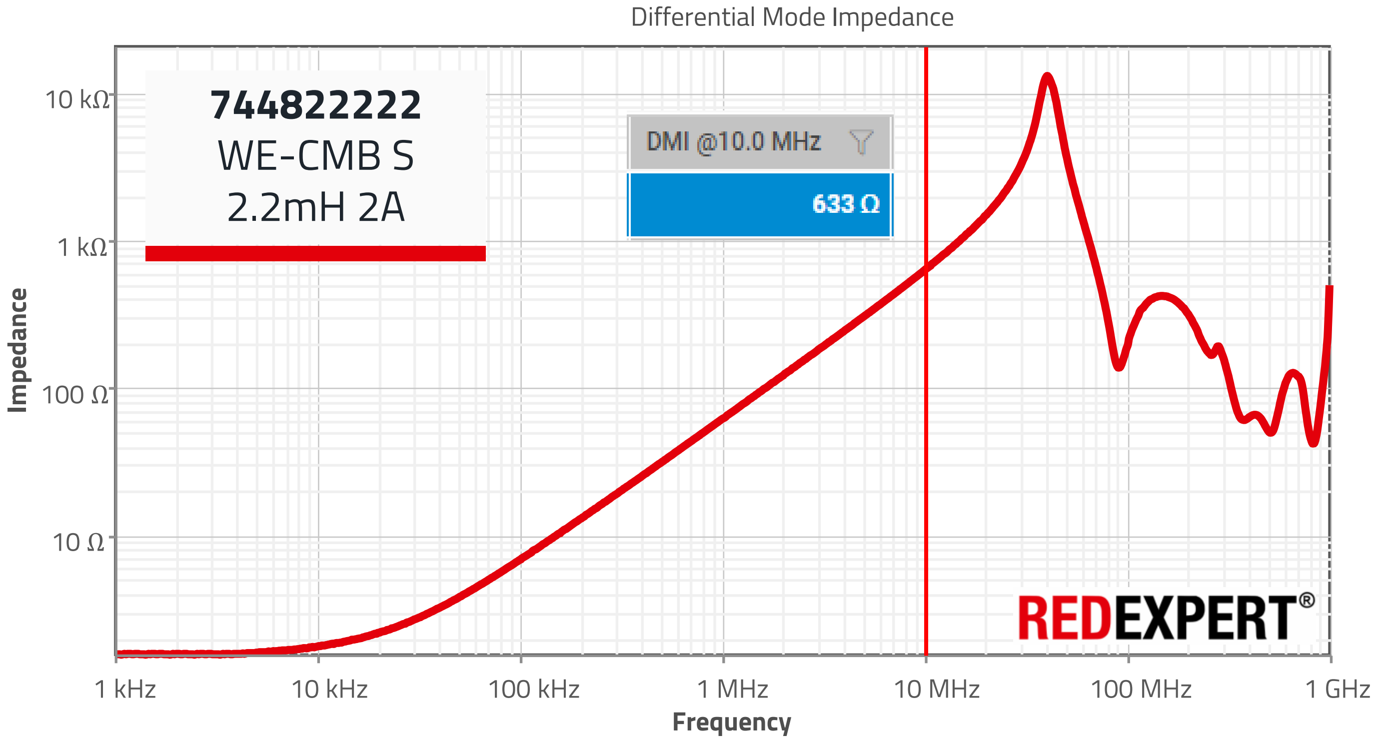


- The stray inductance of the CMC and the junction capacitance of D6 (input protection WE-TVSP) act as a differential-mode filter (LC filter) for free.

Test#6: Background – DM Filtering

REDEXPERT: Stray inductance

- Stray inductance of the CMC:

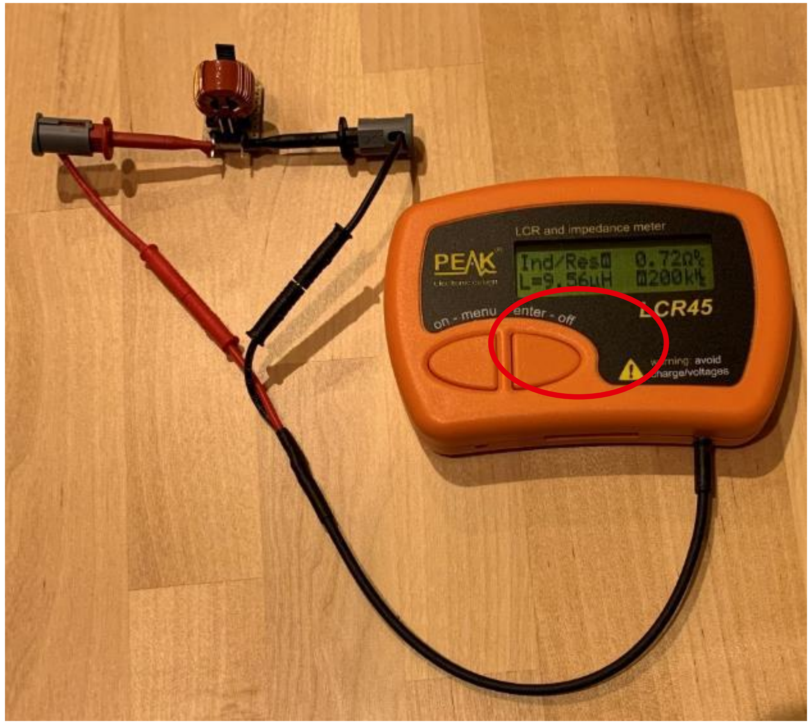


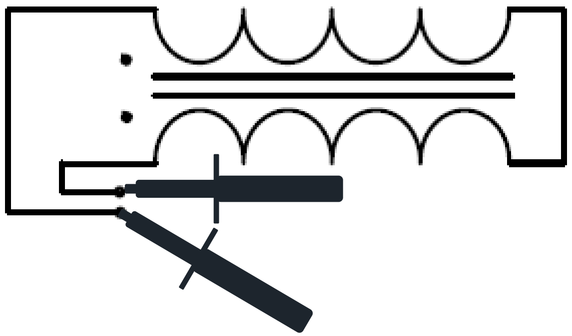
$$L_{s,cmc} = L_{dm} = \frac{|Z_{dm}|}{2\pi \cdot f} = \frac{633\Omega}{2\pi \cdot 10MHz} \approx 10\mu H$$

Test#6: Background – DM Filtering

Measurement: Stray inductance

- Stray inductance of the CMC:





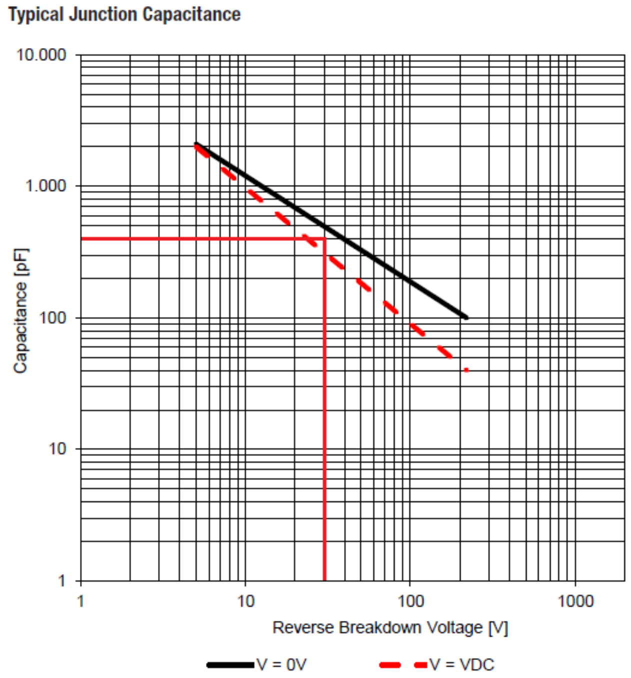
$$L_{\mathrm{s,cmc}} \approx 10\mu H$$

Test#6: Background – DM Filtering

Datasheet: Junction capacitance

- Junction capacitance of D6 (824551301 – WE-TVSP, 30V/3kW, DO-214AB):

$C_{J,D6} \approx 400pF$

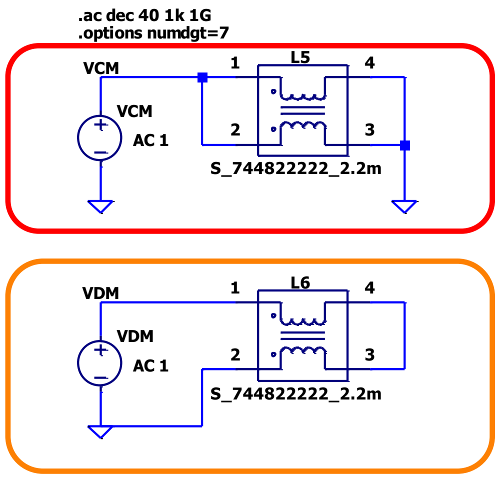


$$f_{0,\mathrm{dm}} = \frac{1}{2\pi \cdot \sqrt{L_{\mathrm{s,cmc}} \cdot C_{\mathrm{J,D6}}}} = \frac{1}{2\pi \cdot \sqrt{10\mu H \cdot 400pF}} \approx 2{,}5MHz$$

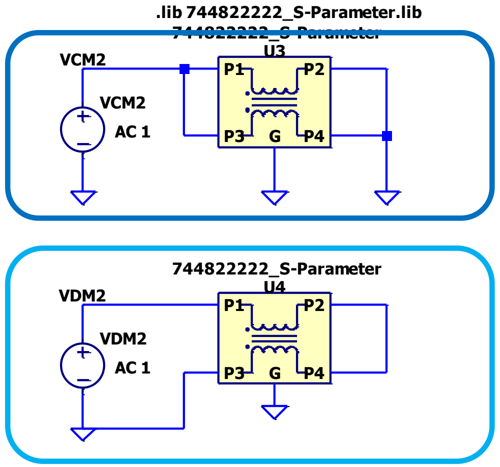
Test#6: Background - Simulation model CMC - S-Parameter vs. WE-LTspice model

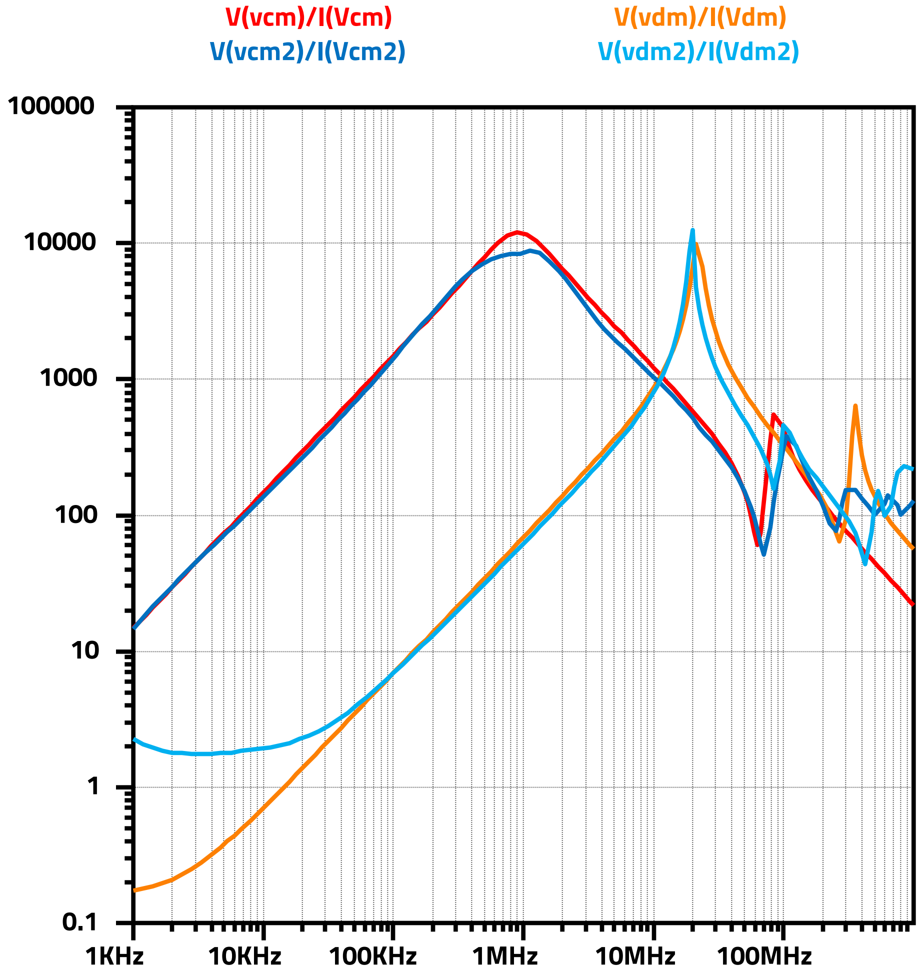
Simulation\CMC\CMC_744822222.asc

WE LTSpice-model:



S-Parameter:

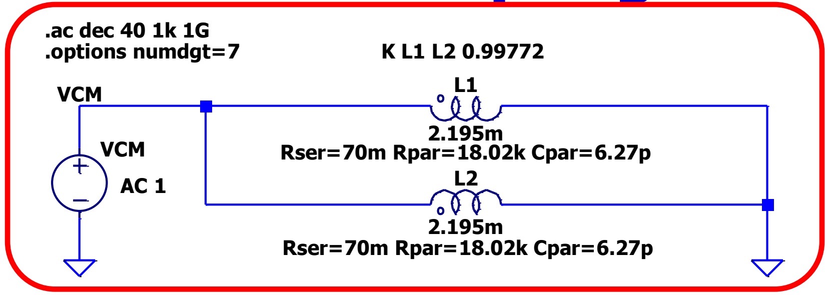




Test#6: Background - Simulation model CMC - Simple

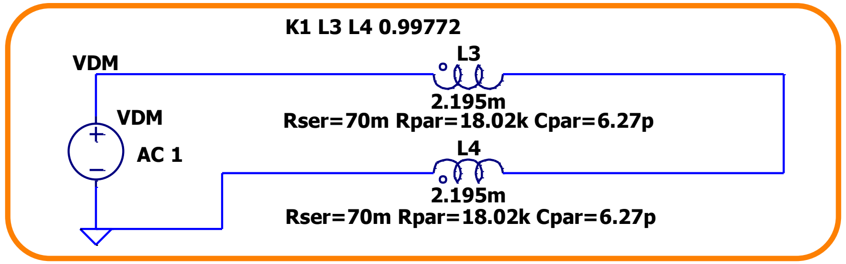
Simulation\CMC\CMC_744822222_simple_1.asc

Simple 1: REDEXPERT Data based on coupling coefficient



Cpar = 1/(2*2*π*f*ZCM@10MHz) = 1/(4*π*10MHz*1.27kΩ)=6.27pF

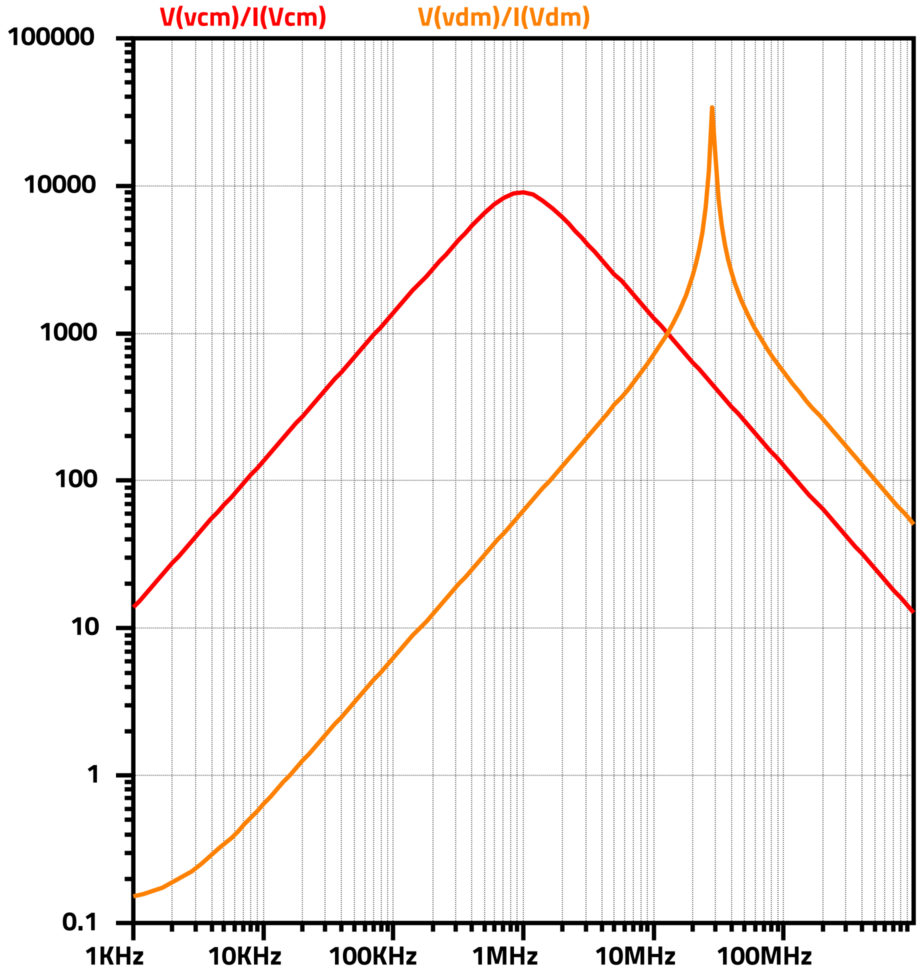
Rpar = ZCM@fRes*2 = 9.01kΩ*2 = 18.02kΩ



LS =ZDM@10MHz/(2*π*f) = 633/(2*π*10MHz)=10µH

K = √(1-LS/L) = √(1-10µH/2.2mH) = 0.99772

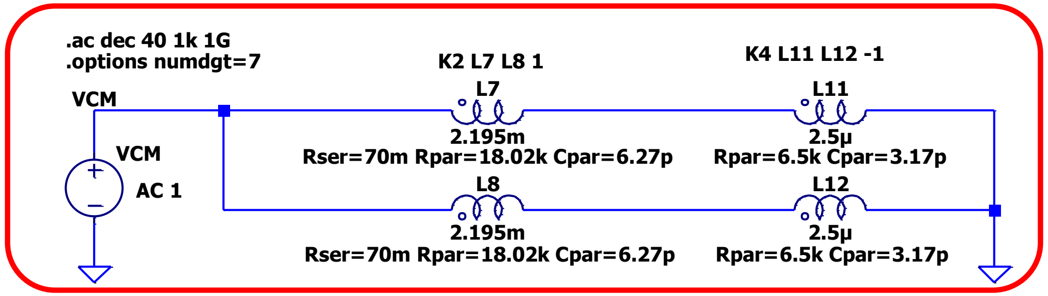
LCM = K*L = 0.99772*2.2mH= 2.195mH



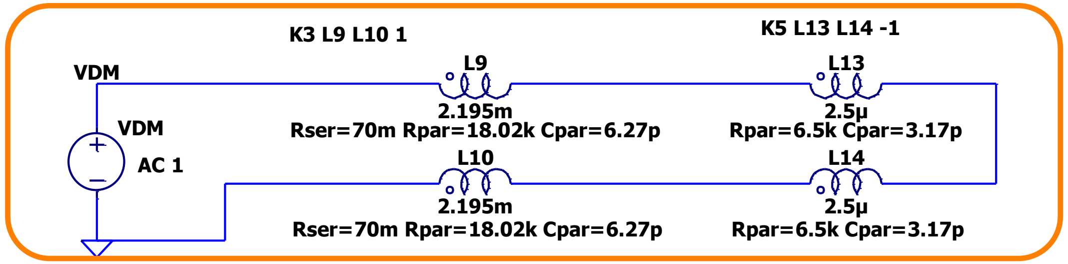
Test#6: Background - Simulation model CMC - Simple 2

Simulation\CMC\CMC_744822222_simple_2.asc

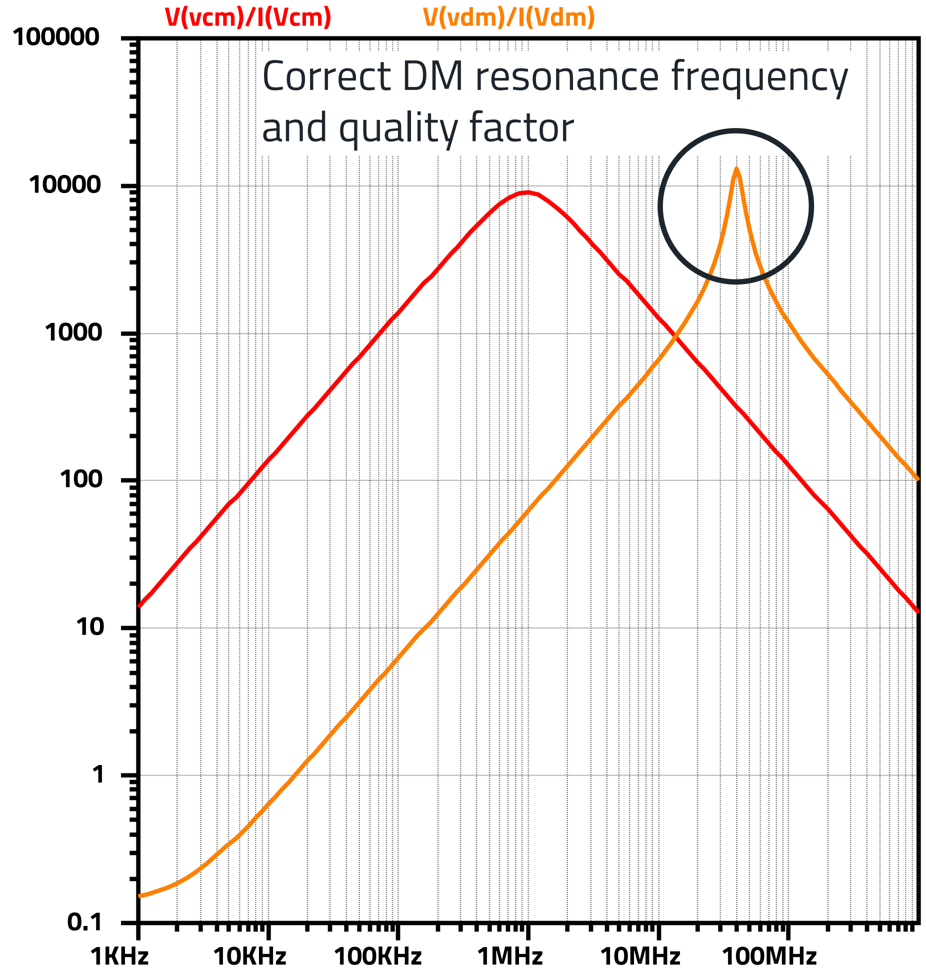
Simple 2: REDEXPERT Data independent DM-resonance



Cpar = 1/(2*2*π*f*ZCM@10MHz) = 1/(4*π*10MHz*1.27kΩ)=6.27pF
Rpar = ZCM@fRes*2 = 9.01kΩ*2 = 18.02kΩ

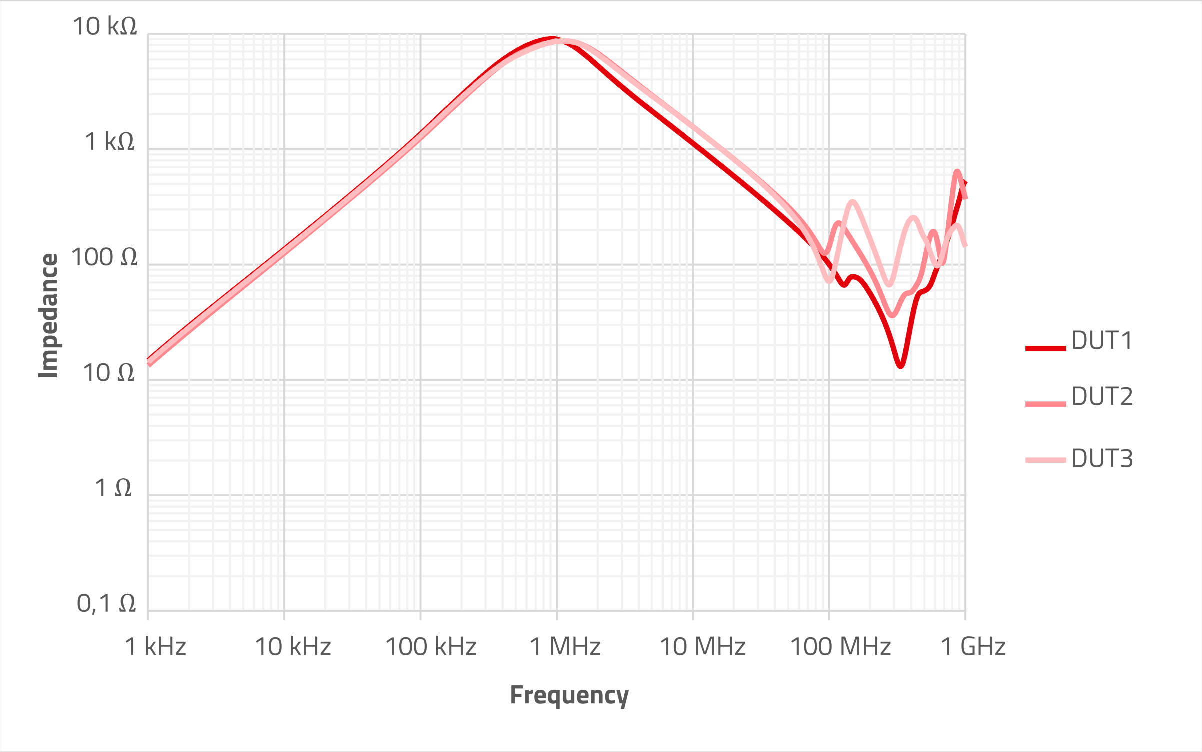


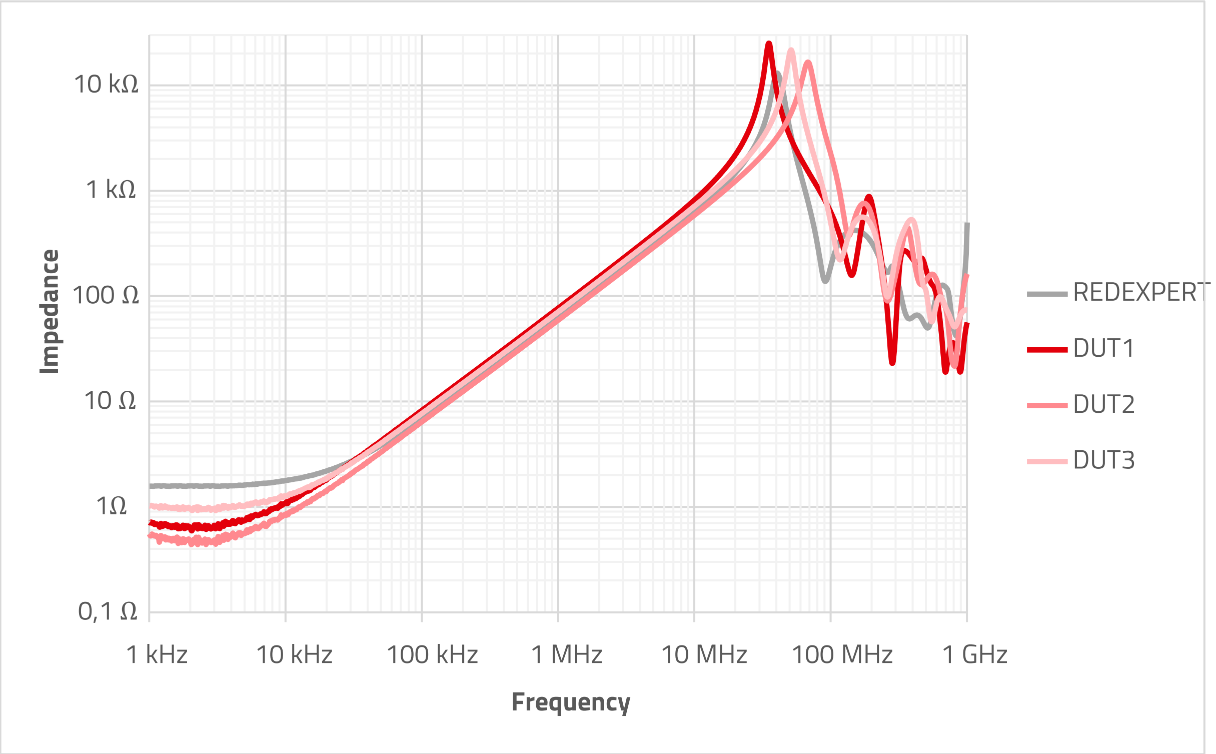
LDM=LS/4 =ZDM@10MHz/(4*2*π*f) = 633Ω/(8*π*10MHz)=2.5µH
RparDM = ZDM@fRes/2 =13kΩ/2 = 6.5kΩ
CparDM = 2/((2*π*fResDM)²*LS) = 2/((2*π*40MHz)²*10µH)=3.17pF



Test#6: Background - Real CMC

Series spread – Do we need an exact spice model?

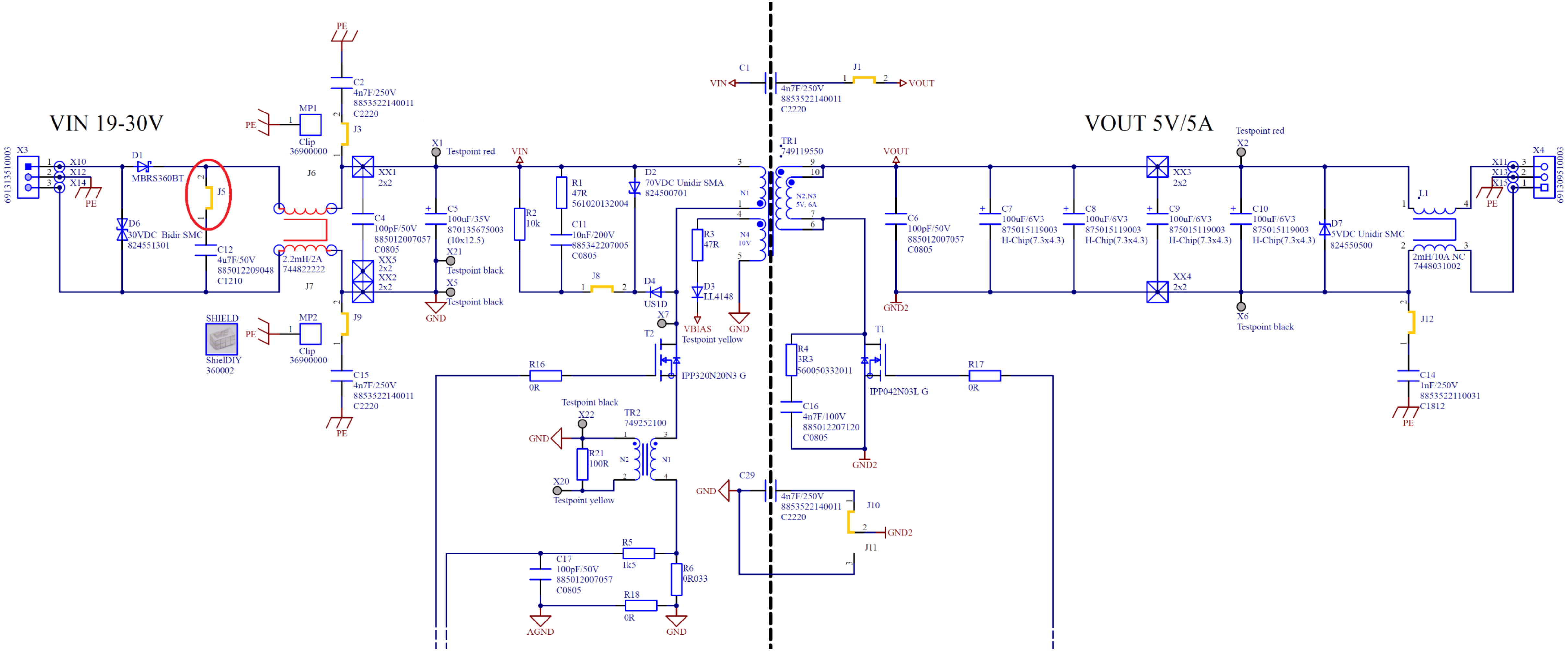




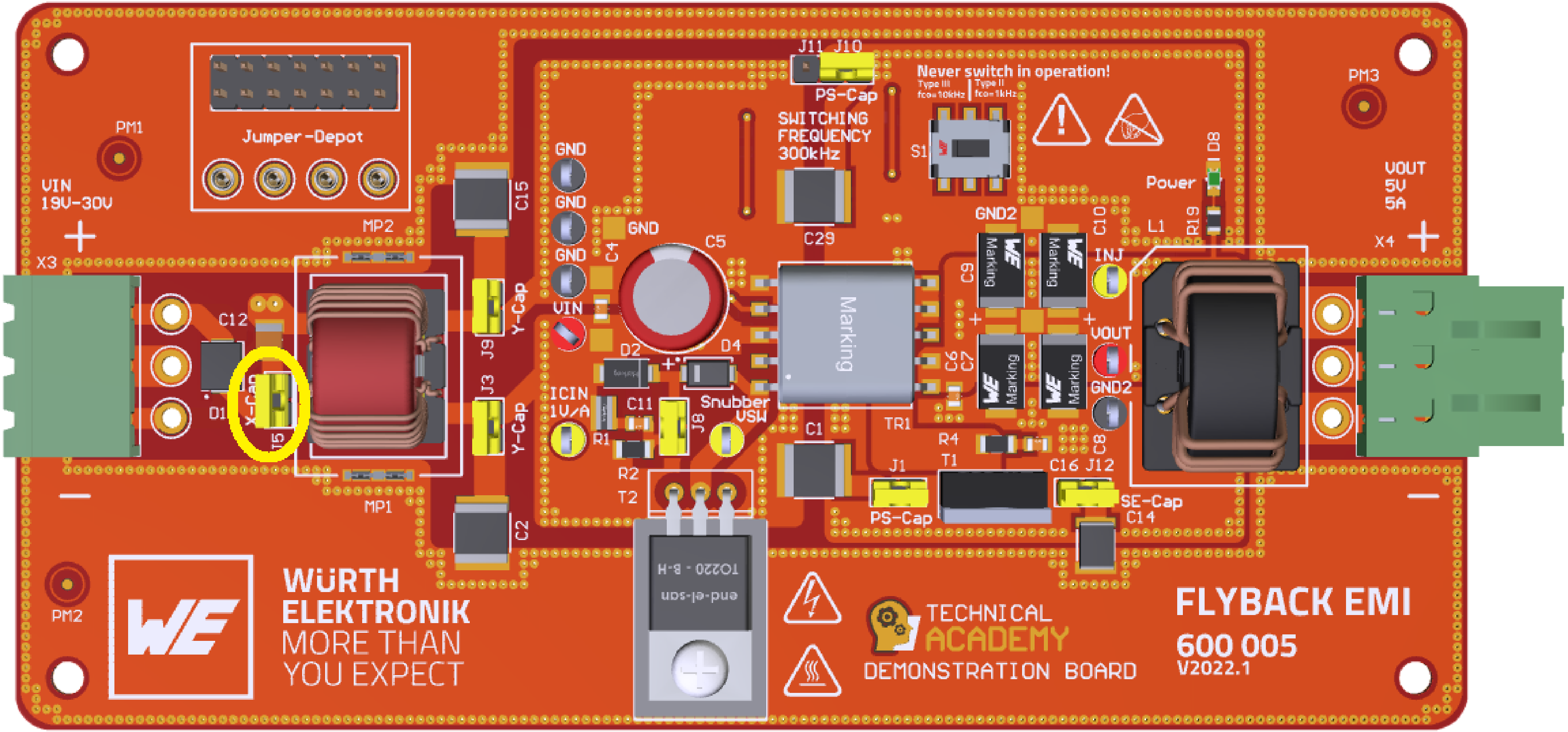
Common-mode impedance (744822222)

Differential-mode impedance (744822222)

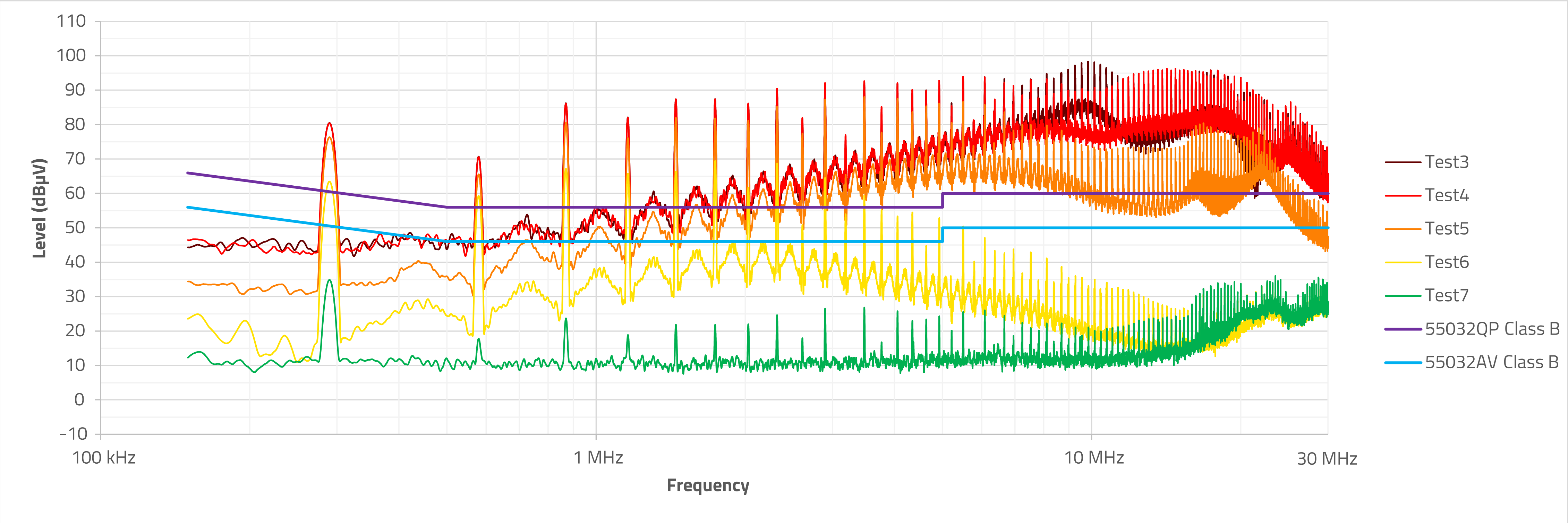
Test#7: Schematic

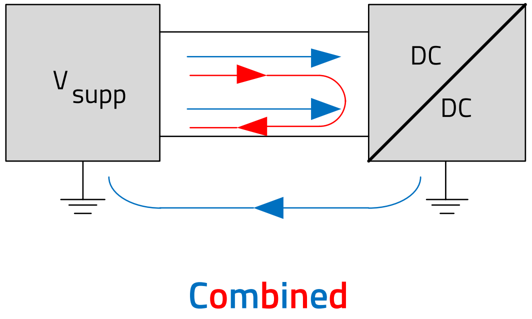


Test#7: Board configuration



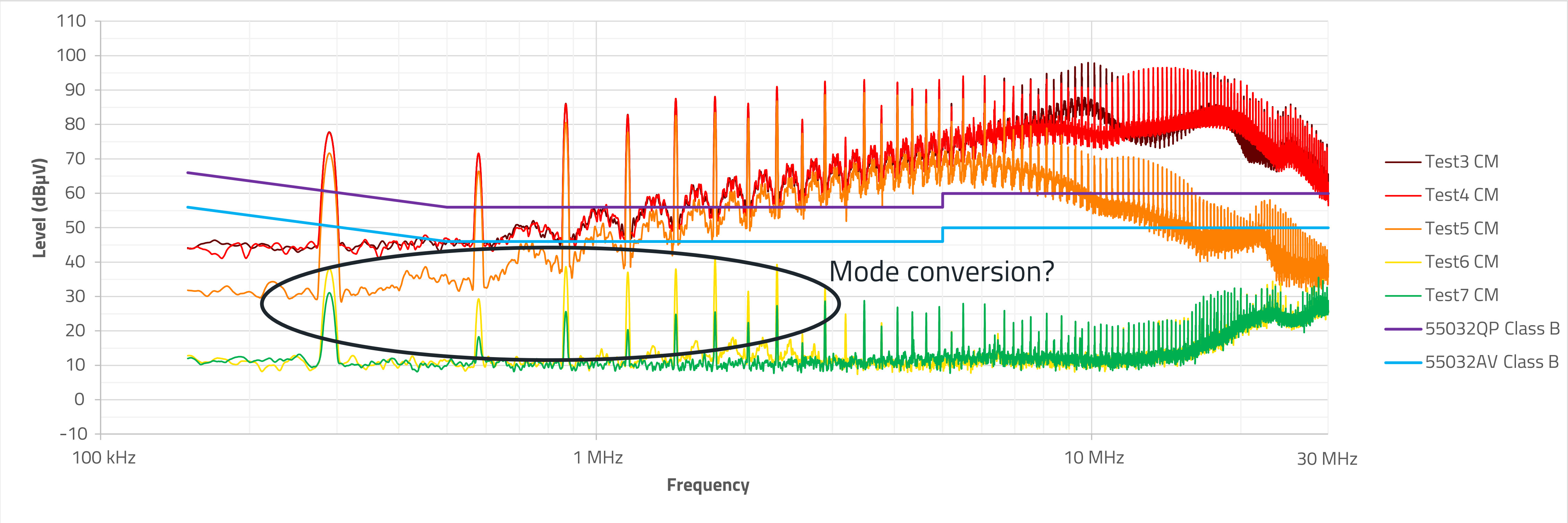
Test#7: Total conducted emissions - Line

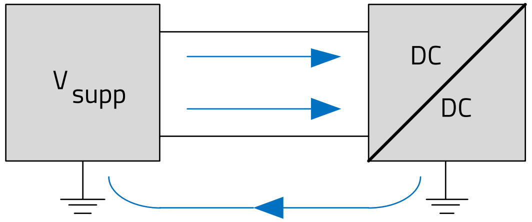




Namec	Description
Test#3	Reference (no improvement)
Test#4	Test#3 + RCD-snubber
Test#5	Test#4 + primary to secondary y-capacitors
Test#6	Test#5 + CMC and y-capacitors (CM filter)
Test#7	Test#6 + x-capacitor (DM filter)

Test#7: Conducted emissions - Common mode

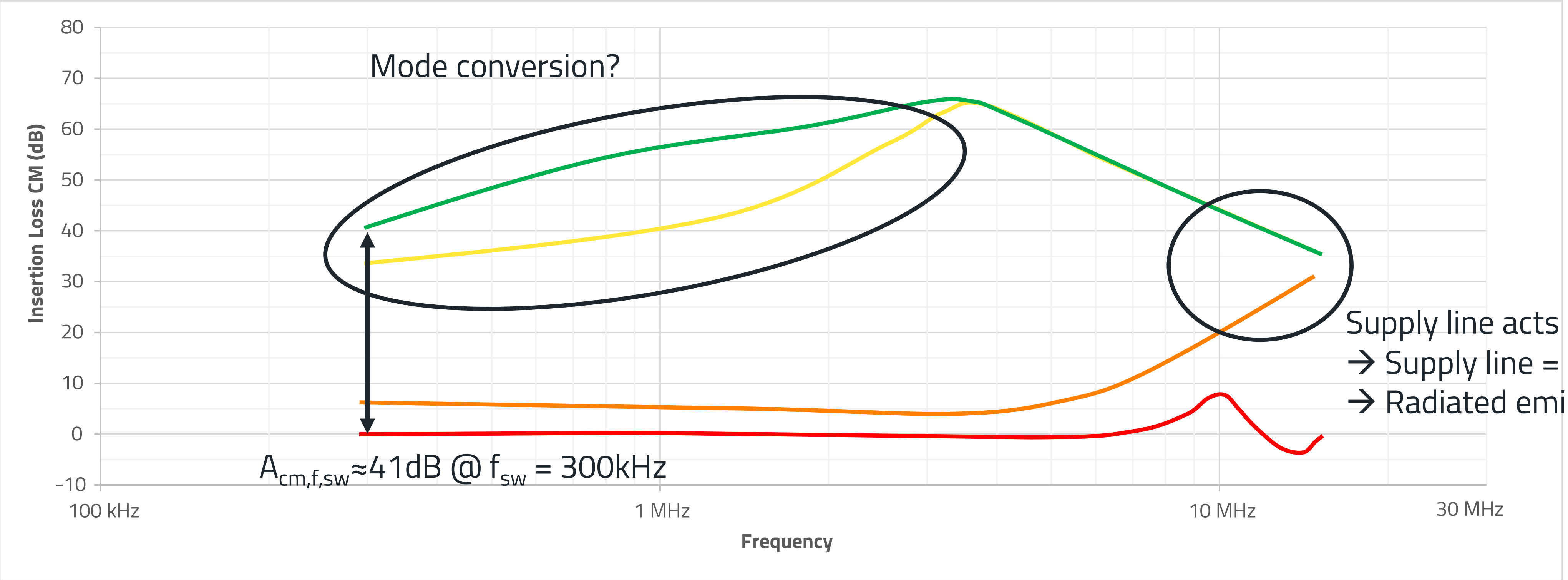




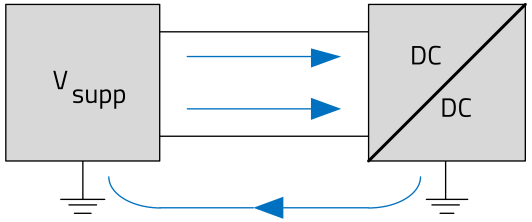
Common Mode

Name	Description
Test#3	Reference (no improvement)
Test#4	Test#3 + RCD-snubber
Test#5	Test#4 + primary to secondary y-capacitors
Test#6	Test#5 + CMC and y-capacitors (CM filter)
Test#7	Test#6 + x-capacitor (DM filter)

Test#7: Conducted emissions - Insertion loss CM



Supply line acts as a CM filter
→ Supply line = antenna
→ Radiated emissions!

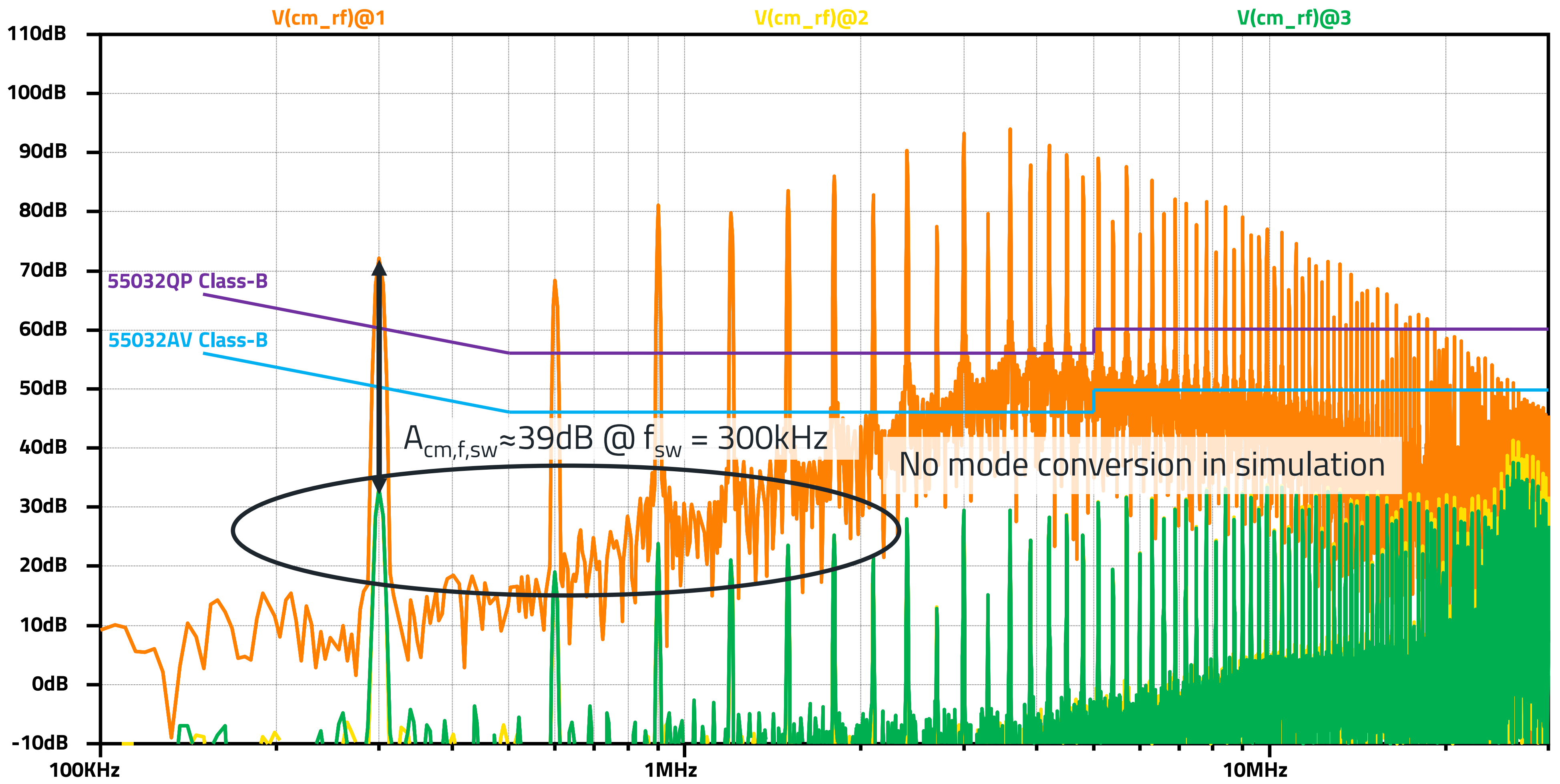


Common Mode

Description
+ RCD-snubber
+ primary to secondary y-capacitors
+ CMC and y-capacitors (CM filter)
CMC and y-capacitors (CM filter) + x-capacitor (DM filter)

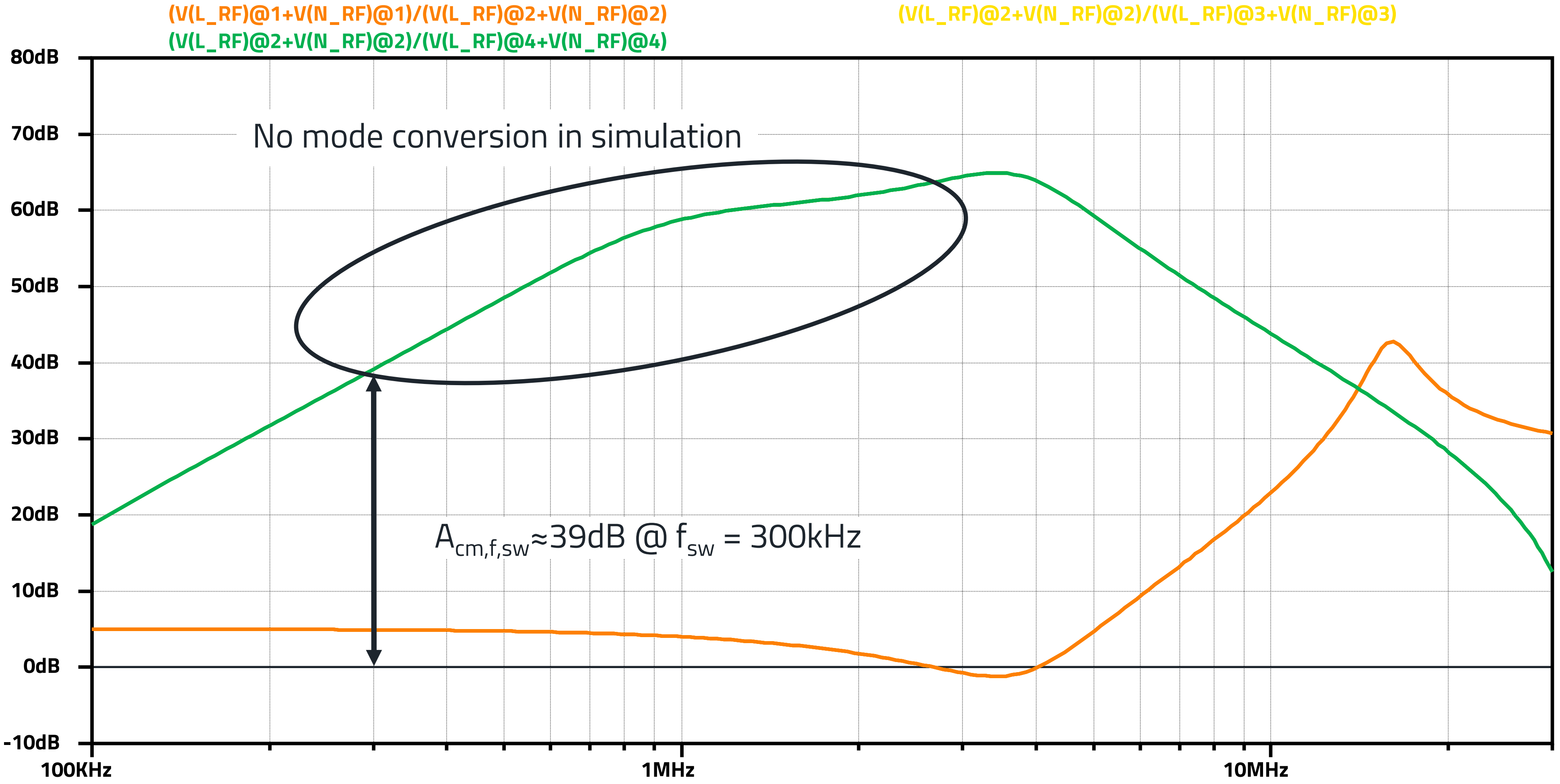
Test#7b: Simulation - Conducted emissions - Common mode

Simulation\Test1-7\Flyback_EMI_Test5-7b_FFT.asc

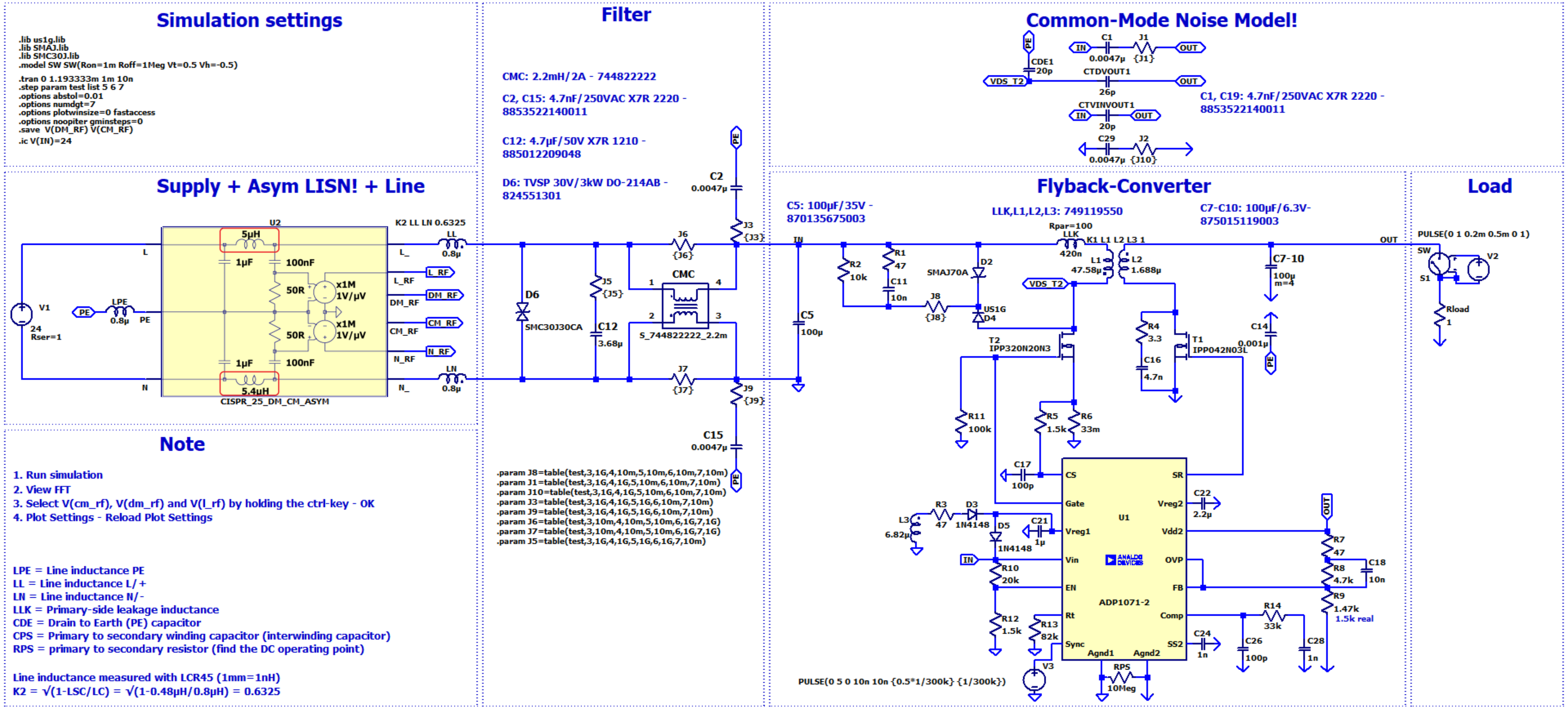


Test#5: Simulation - Conducted emissions - Insertion loss CM

[Simulation\Insertion_Loss\Insertion_Loss-CM.asc]

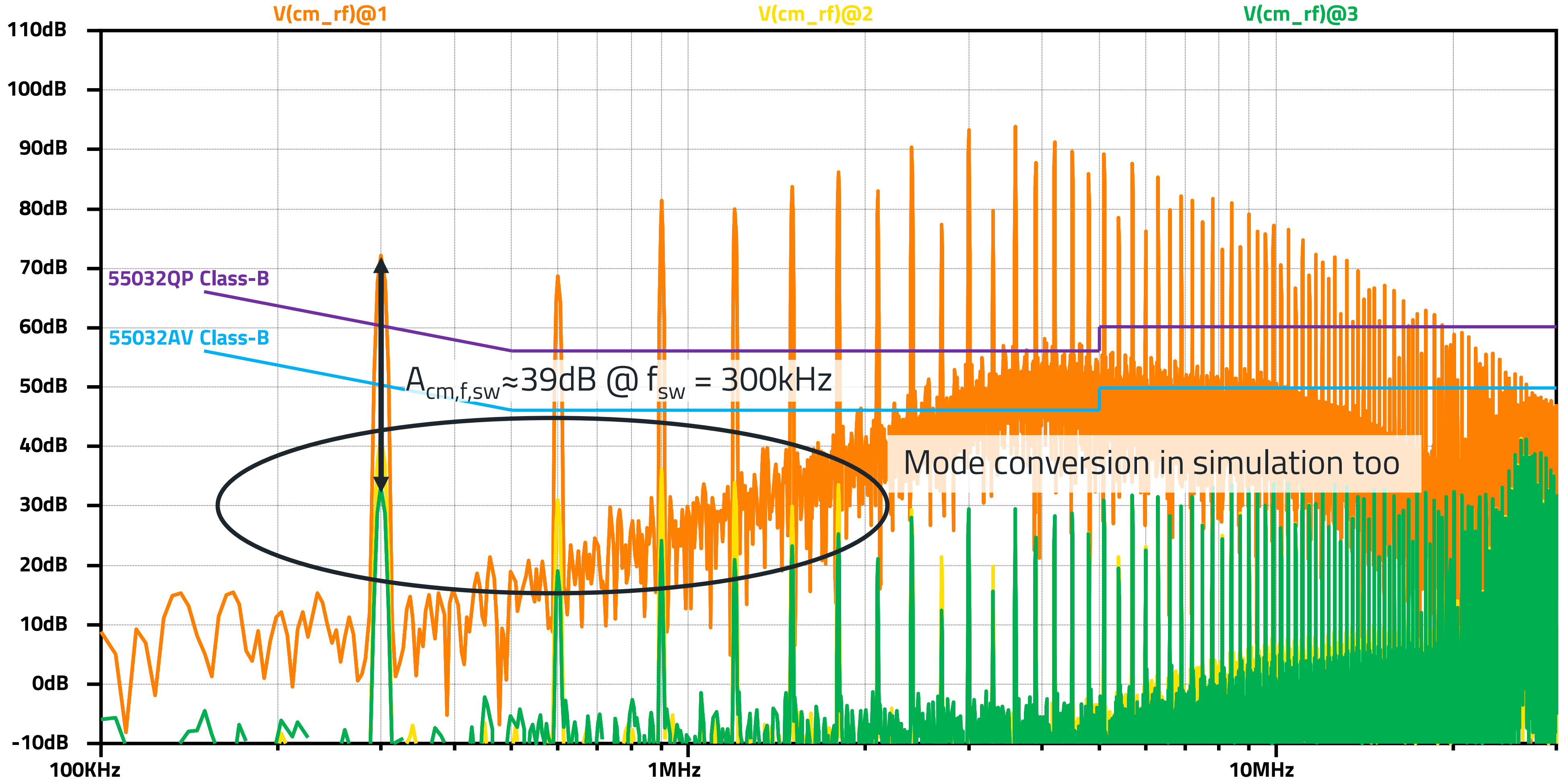


Test#7c - Simulation: Simulation\Test1-7\Flyback_EMI_Test5-7c_FFT.asc

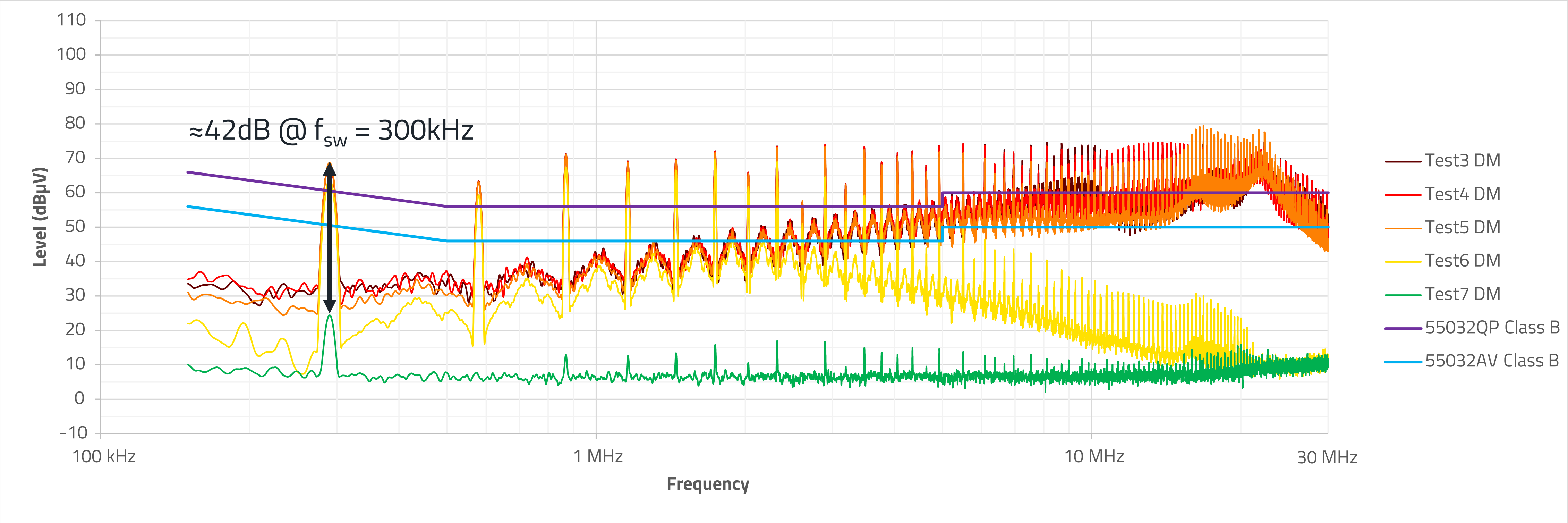


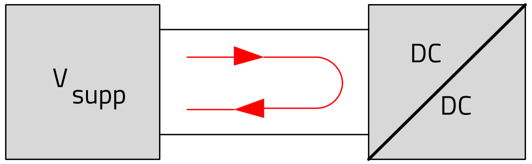
Test#7c: Simulation - Conducted emissions - Common mode

Simulation\Test1-7\Flyback_EMI_Test5-7c_FFT.asc



Test#7: Conducted emissions - Differential mode

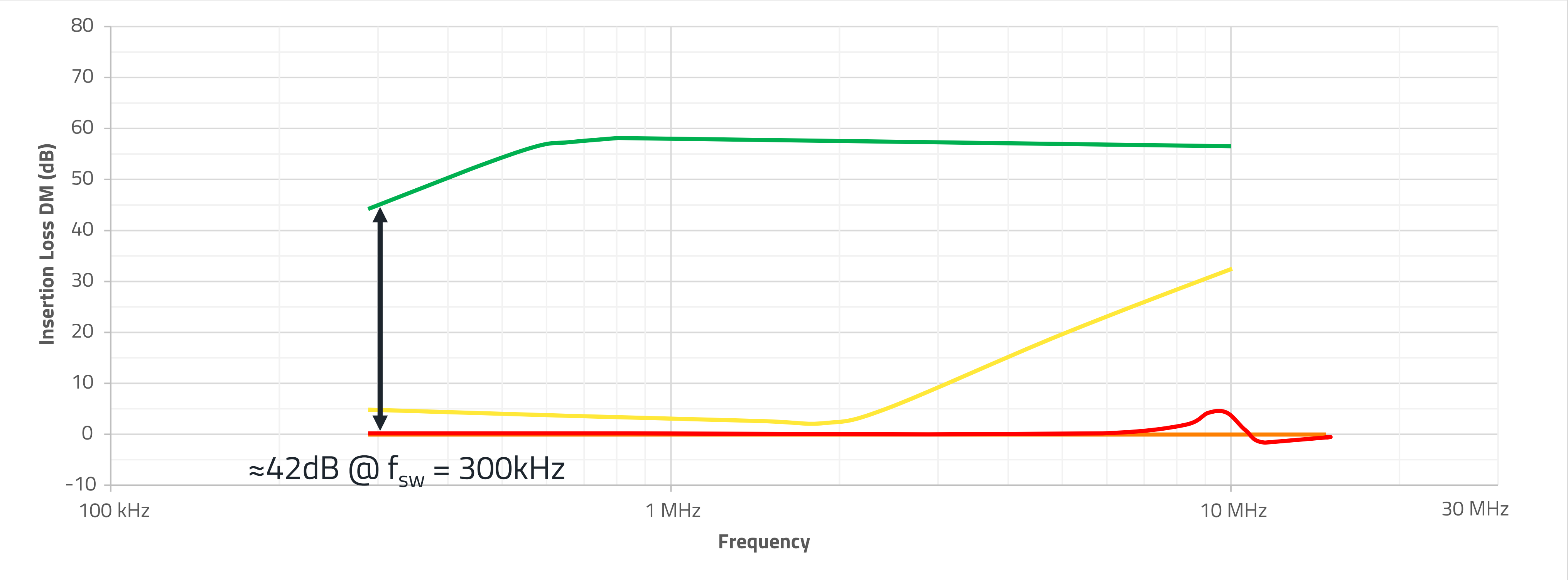


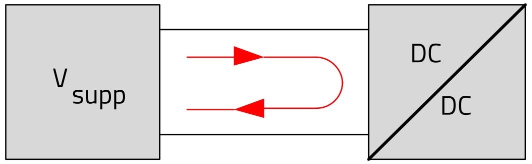


Differential Mode

Name	Description
Test#3	Reference (no improvement)
Test#4	Test#3 + RCD-snubber
Test#5	Test#4 + primary to secondary y-capacitors
Test#6	Test#5 + CMC and y-capacitors (CM filter)
Test#7	Test#6 + x-capacitor (DM filter)

Test#7: Conducted emissions - Insertion loss DM



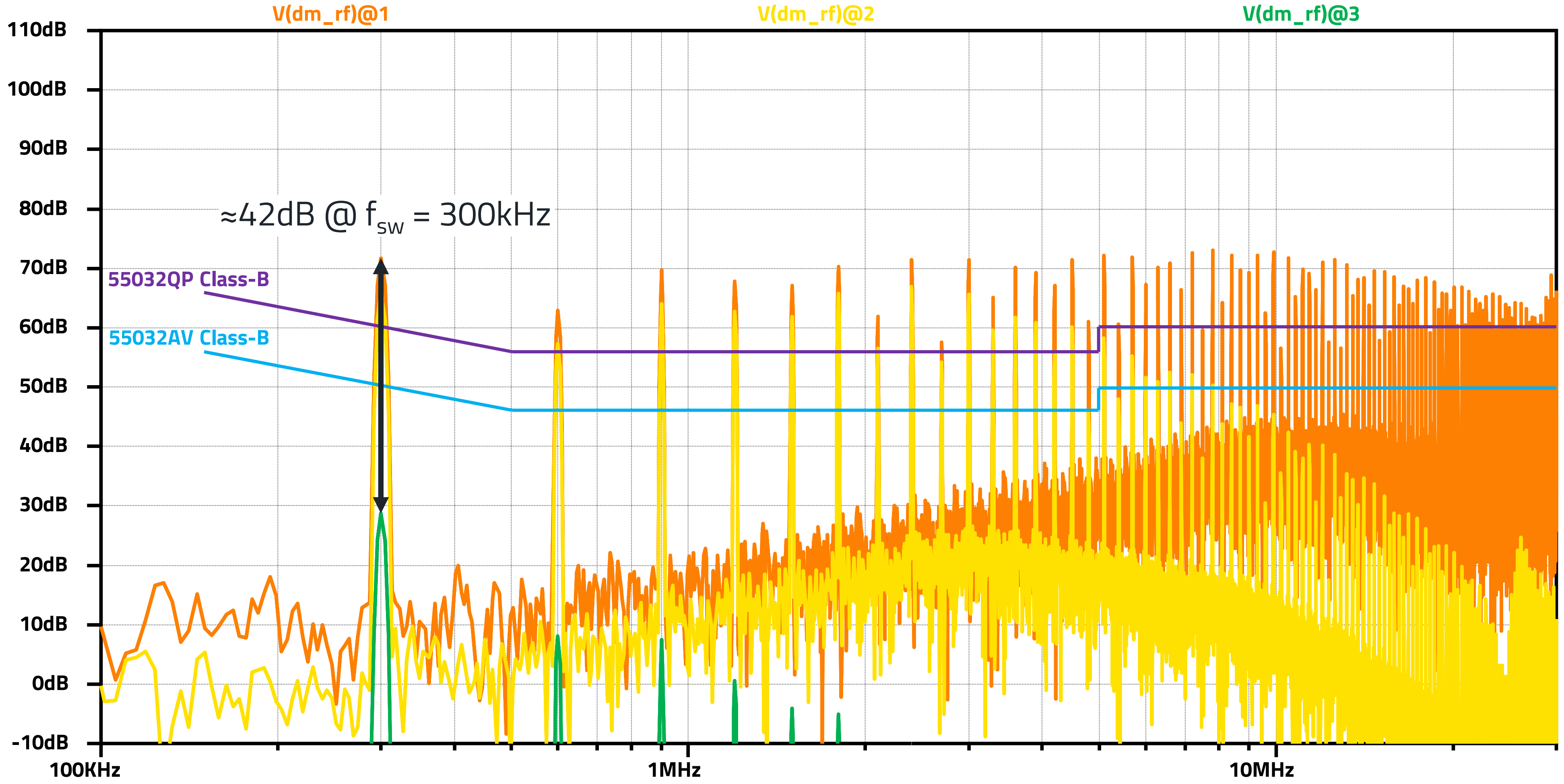


Differential Mode

Description
+ RCD-snubber
+ primary to secondary y-capacitors
+ CMC and y-capacitors (CM filter)
+ CMC and y-capacitors (CM filter) + x-capacitor (DM filter)

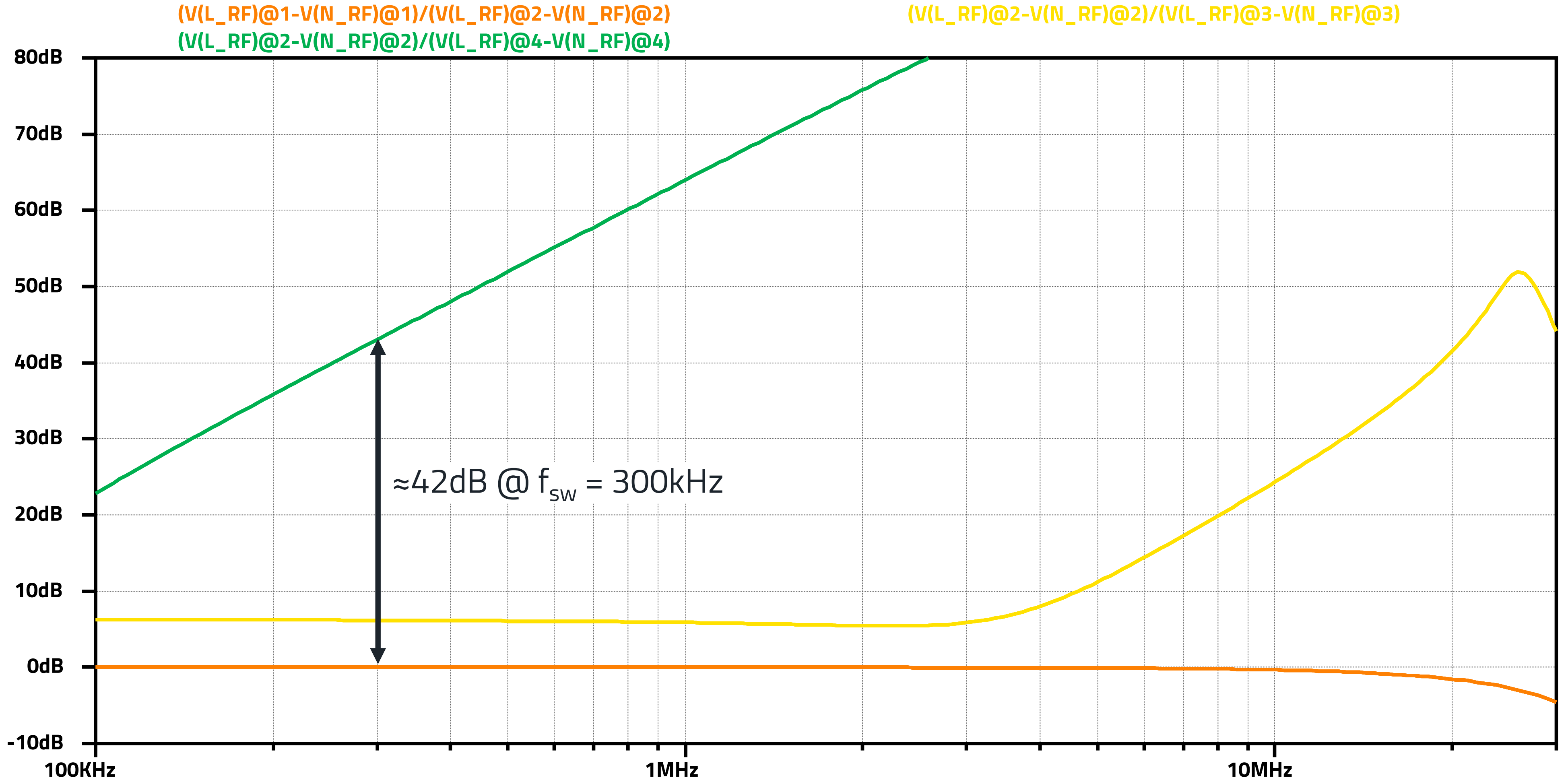
Test#7c: Simulation - Conducted emissions - Differential mode

Simulation\Test1-7\Flyback_EMI_Test5-7c_FFT.asc



Test#7: Simulation - Conducted emissions - Insertion loss DM

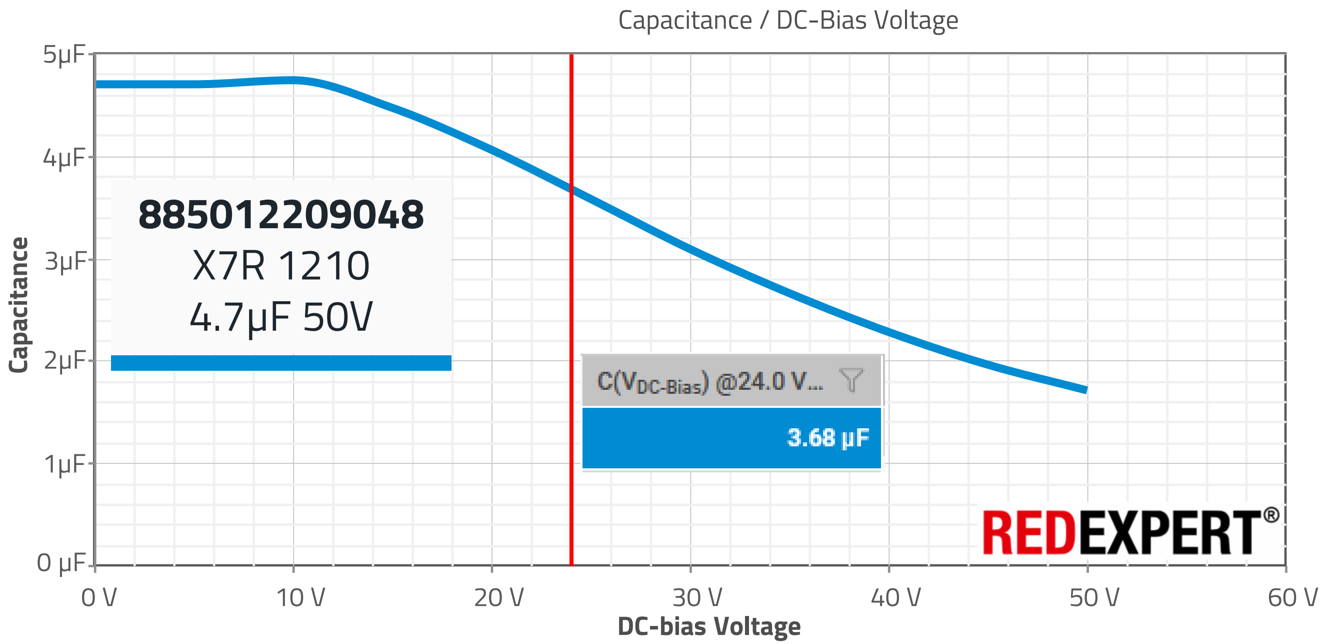
[Simulation\Insertion_Loss\Insertion_Loss-DM.asc]



Test#7: Background - DM-Filter

REDEXPERT: Capacitance / DC-Bias

- The DM filter results from the stray inductance of the CMC and the X-capacitor
  - Stray inductance of the CMC ≈10µH
  - X-capacitor C12: 4.7µF/50V, 1210, MLCC



$$C_x \approx 3.68\mu F@24VDC$$

Test#7: Background - DM-Filter

Theory

- Without DC bias:
  - $f_{0,\mathrm{dm}} = \frac{1}{2\pi\cdot\sqrt{L_{\mathrm{S,cm}}\cdot C_{\mathrm{x}}}} = \frac{1}{2\pi\cdot\sqrt{10\mu H\cdot 4{,}7\mu F}} \approx 23{,}2kHz$
  - $A_{\mathrm{dm,f,sw}} = \log\left(\frac{f_{\mathrm{sw}}}{f_{0,\mathrm{dm}}}\right)\cdot 40dB = \log\left(\frac{300kHz}{23{,}2kHz}\right)\cdot 40dB \approx 44{,}5dB$
- With DC bias:
  - $f_{0,\mathrm{dm}} = \frac{1}{2\pi\cdot\sqrt{L_{\mathrm{S,cm}}\cdot C_{\mathrm{x}}}} = \frac{1}{2\pi\cdot\sqrt{10\mu H\cdot 3{,}68\mu F}} \approx 26{,}2kHz$
  - $A_{\mathrm{dm,f,sw}} = \log\left(\frac{f_{\mathrm{sw}}}{f_{0,\mathrm{dm}}}\right)\cdot 40dB = \log\left(\frac{300kHz}{26{,}2kHz}\right)\cdot 40dB \approx 42{,}3dB$

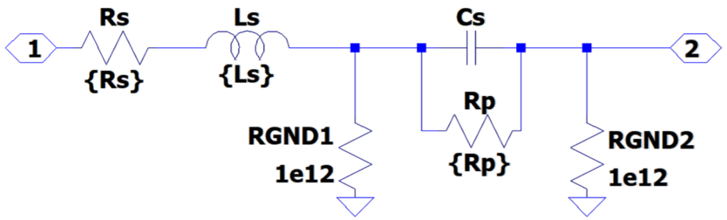
➢ $\Delta A_{\mathrm{dm,f,sw}} \approx 2{,}2dB$

➢ Simulation\DC-Bias\Insertion_Loss-DM_DC-Bias.asc

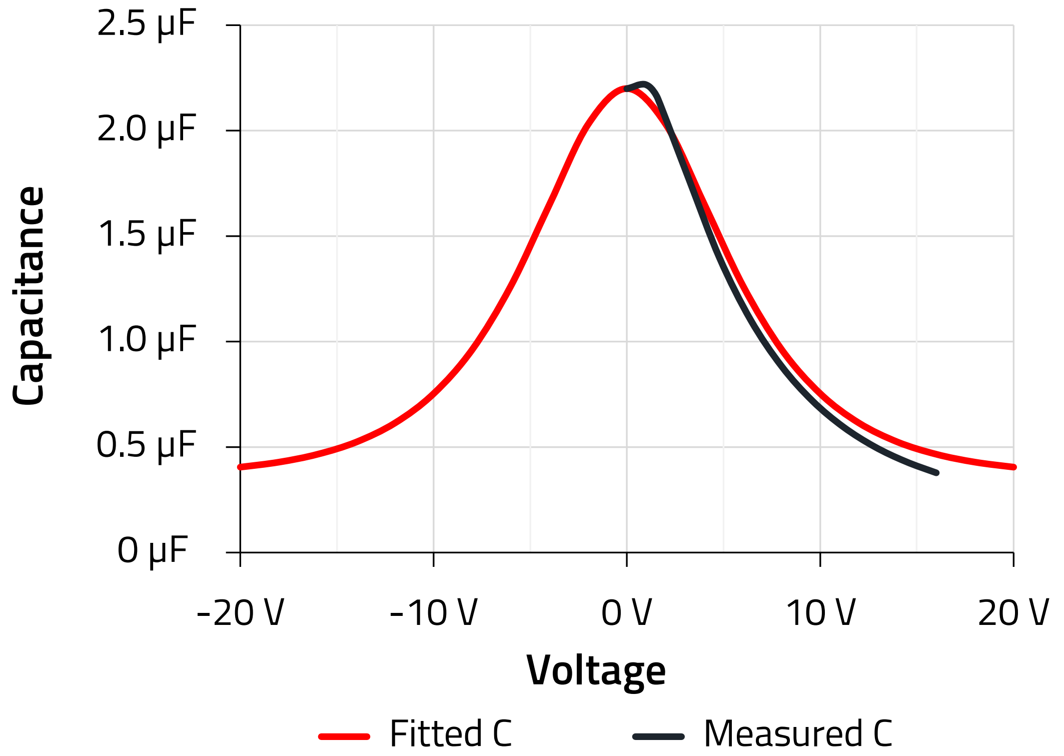
Würth Elektronik - LTspice MLCC DC bias model

Capacitance

- The new Würth Elektronik MLCC DC bias models are already integrated in LTspice XXVI.
- Path: \Contrib\Wurth\Capacitors\MLCC
- Voltage vs. capacitance implementation:
  - $C = (C_0 - C_{SAT}) \cdot \operatorname{sech}\left(\frac{V}{V_{th}}\right) + C_{SAT}$
    - sech() = Hyperbolic secant




```
Q=(x*{Csat})+({C0}*{Vth}*arctan(sinh(x/{Vth})))-({Csat}*{Vth}*(arctan(sinh(x/{Vth}))))
.param Rs=2.2E-6 Ls=2.59E-10 Rp=5e7 C0=2.2E-6 Csat=3.62E-7 Vth=4.49
```

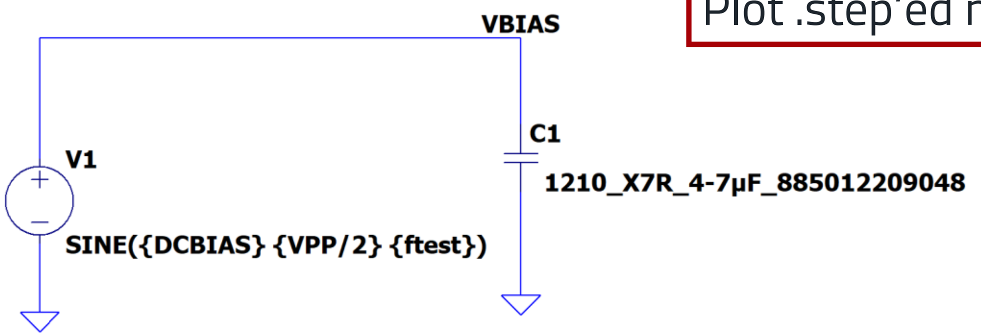


Measured and fitted voltage dependent behavior of capacitance.
Part number: 885012106018, C: 2.2µF, Matchcode: WCAP-CSGP, Size: 0603, Material: X5R, V_R: 16 V.

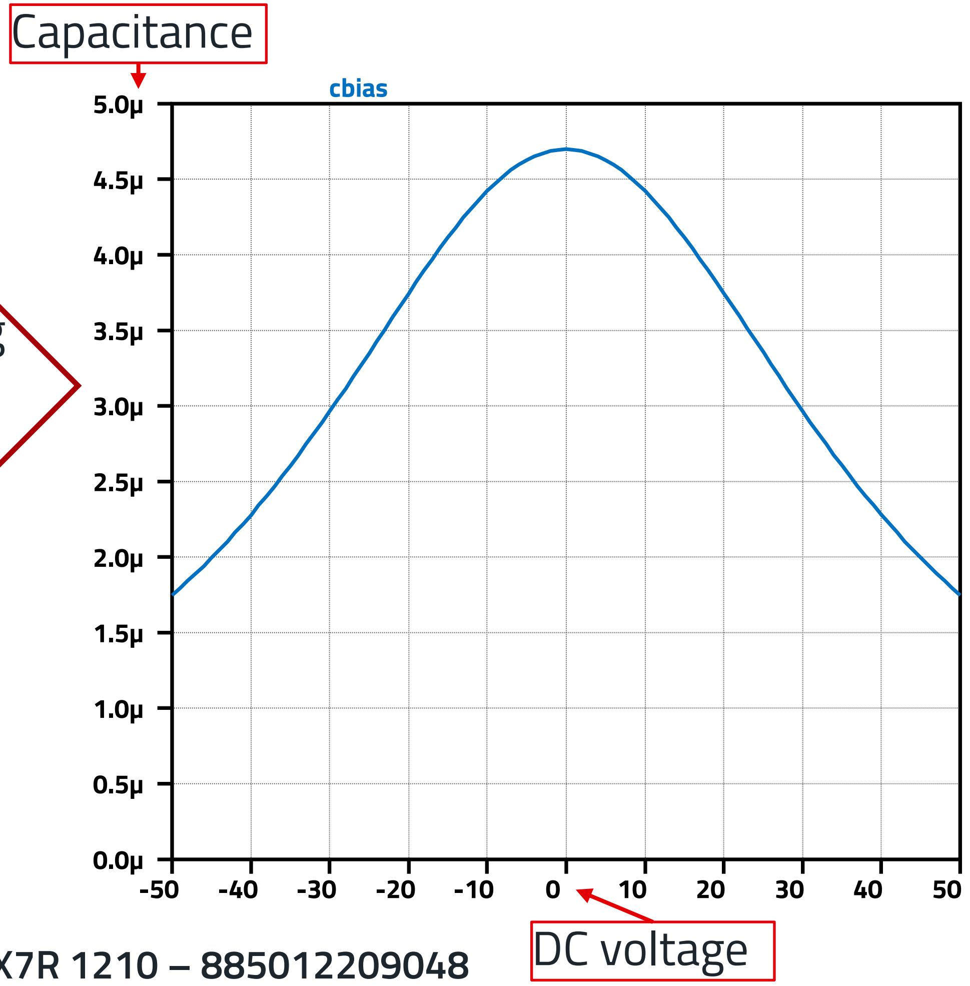
Würth Elektronik - LTspice MLCC DC bias model

Capacitance simulation

```
.tran 0 {1m+1/ftest} 1m
.step param dcbias -50 50 1
.param ftest=1k
.param VPP=1
.meas TRAN IPP PP Ix(C1:A) FROM 0m TO {1/ftest}
.meas CBIAS PARAM 1/(2*pi*ftest*VPP/IPP)
```



View → SPICE Error Log
Right mouse click →
Plot .step'ed meas data

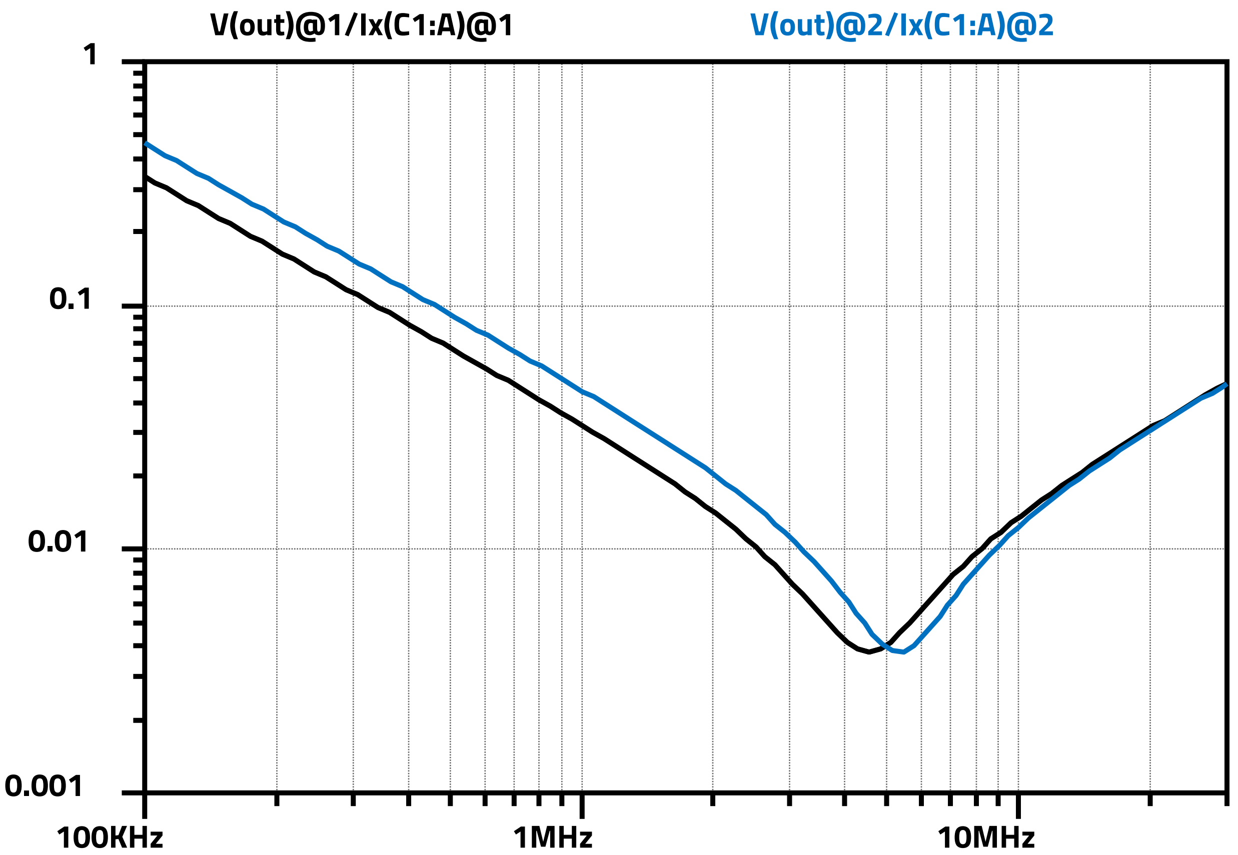


Capacitance Simulation: 4.7µF/50V X7R 1210 – 885012209048

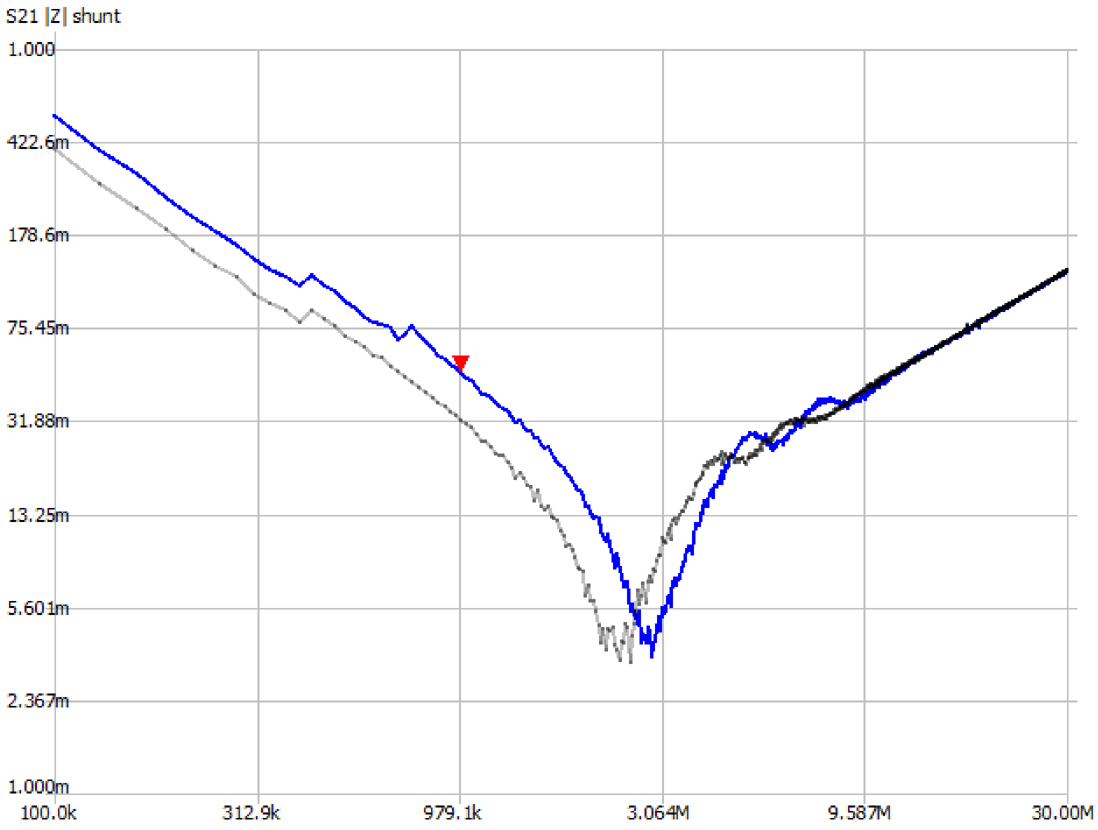
[Simulation\DC-Bias\DC-Bias_885012209048.asc]

Würth Elektronik - LTspice MLCC DC bias model

Impedance Simulation vs. Measurement



Impedance Simulation:[Simulation\DC-Bias\DC-Bias_Impedance_885012209048.asc]



Impedance Measurement: 4.7µF/50V X7R 1210 - 885012209048)
0V vs. 24V

Würth Elektronik - LTspice MLCC DC bias model

Transient simulation with DC bias model

- Simulation time without DC bias model: Simulation\Test1-7\Flyback_EMI_Test7c.asc
  - Total elapsed time: **13.692 seconds**

- Simulation time with DC bias model: Simulation\Test1-7\Flyback_EMI_Test7c_dcbias.asc
  - Total elapsed time: **13.219 seconds**

- Device: 11th Gen Intel(R) Core(TM) i7-1165G7 / 16GB RAM / Windows 10 Enterprise / LTspice 17.1.15

Test#7: Background - DM-Filter

Selection

1. Choosing the CMC – Determining the leakage inductance using RedExpert
   - ~10µH

2. Cutoff frequency of the input filter min. @ 1/10 of the switching frequency of the switching regulator:
   - 300kHz/10 = 30kHz

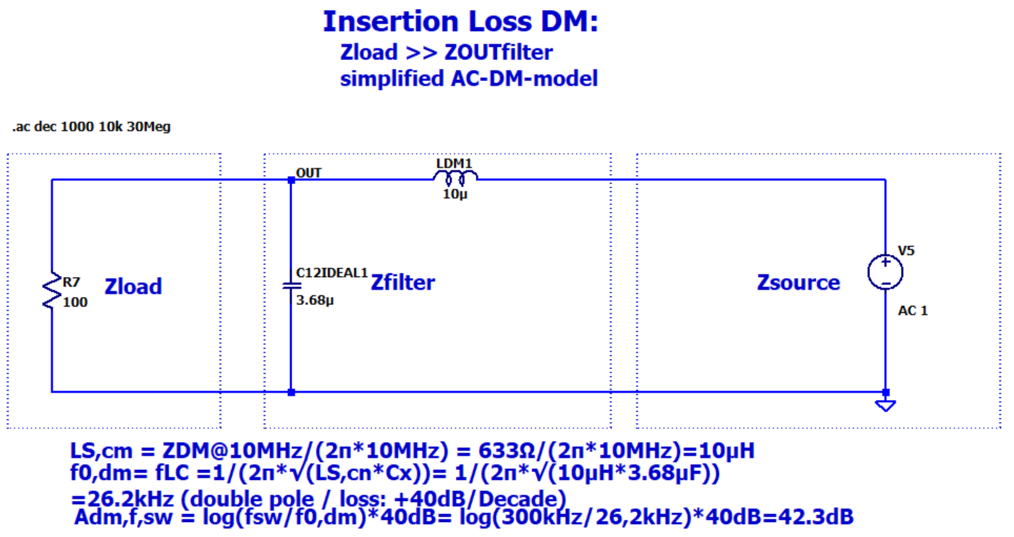
3. Calculation of capacitance:

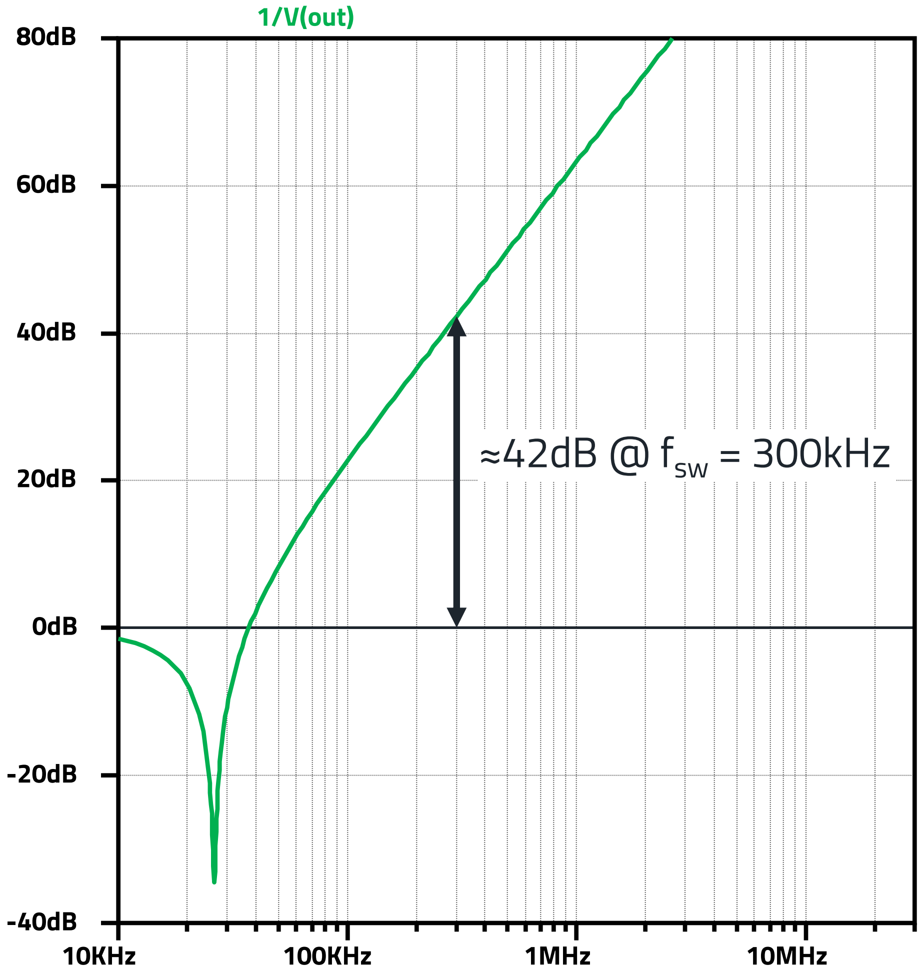
$$f_{0,\mathrm{dm}} = \frac{1}{2\pi\sqrt{LC}} \rightarrow C_{\mathrm{x}} = \frac{1}{(2\pi \cdot f_{0,dm})^2 \cdot L_{\mathrm{S,cm}}} = \frac{1}{(2\pi \cdot 30KHz)^2 \cdot 10\mu H} = 2{,}8\mu F$$

4. Selection of the component:
   - 885012209048 (4.7µF/50V1210)
   - Tolerance margin and DC bias!

Test#7: Background - DM-Filter

Simulation\Insertion_Loss\Insertion_Loss-DM_simple.asc





The LTspice XVII Book

Commands and Applications

- The application manual for the simulation software LTspice XVII is an indispensable tool for beginners and advanced users alike. For the beginner, the book offers instructions on installation and updates, file types and circuit examples.

- All users will appreciate the detailed explanations of editors and views, simulation commands, component models and their use, special functions, and even more in-depth topics such as modeling inductors and transformers with saturation.