GLOBAL POWER DESIGN SEMINAR TOUR

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INTERNAL

WÜRTH ELEKTRONIK MORE THAN YOU EXPECT
ANALOG Ahead of What's Possible

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GLOBAL POWER DESIGN SEMINAR TOUR

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Global agenda

- **8:30 - 9H Registration and welcome coffee**
- 9H-9H50: SMPS tips and tricks — ADI
- **9:55-10:45: Filtering considerations for DC/DC converters** — WE
  - 10:45-11:10: Break – Networking
- **11:10-12:00: Art of Loop Compensation** — WE
  - 12:00-13:00: Lunch
- 13:00-13:50: LTspice examples — ADI
- **13:55-14:45: Smart selection of inductors and capacitors** — WE
  - 14:45-15:10: Break - Networking
- 15:10-16:00: PCB board layout optimization — ADI

3 | JULY 4, 2025 TECHNICAL ACADEMY

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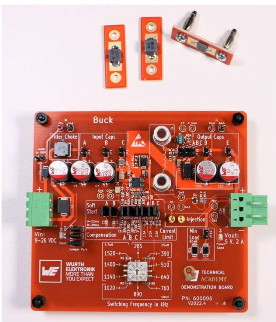
SMPS TOPOLOGIES TIPS AND TRICKS



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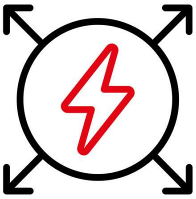
GLOBAL POWER DESIGN SEMINAR TOUR

SMPS tips and tricks

- SMPS tips and tricks



ANALOG DEVICES

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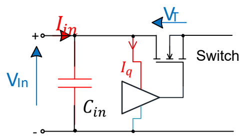


SMPS tips and tricks

- MOSFETs selection
  - Gate current consumption

  Depending, U (Vgate), Input gate capacitance and frequency of switching

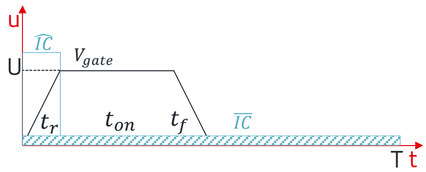
$$\overline{Ic} = \frac{1}{T} \cdot \int_0^t \widehat{Ic} = \frac{1}{T} \cdot \int_0^{t_r} \widehat{Ic} = \frac{1}{T} \cdot \widehat{Ic} \cdot \boldsymbol{t_r}$$

and

$$\widehat{Ic} = C \cdot \frac{\Delta U}{\Delta t} = C \cdot \frac{U}{\boldsymbol{t_r}}$$

Finaly cancel time : $\overline{Ic} = \frac{1}{T} \cdot C \cdot \frac{U}{\boldsymbol{t_r}} \cdot \boldsymbol{t_r} = U \cdot C \cdot \frac{1}{T} = Q_g \cdot f$

$$\boldsymbol{\overline{Ic} = U \cdot C \cdot f = Q_g \cdot f}$$



ANALOG DEVICES

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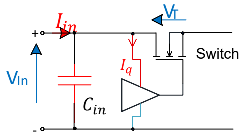
SMPS tips and tricks



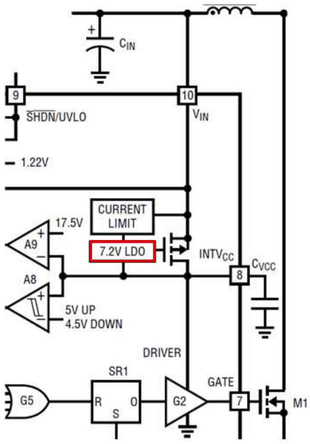
- Driver limits
  - Power limits
  - We know how much current is necessary to power the MOSFET gate:

$$\overline{Ic} = U \cdot C \cdot f = Q_g \cdot f$$

  - A special care must be observed about power limits of the driver for MOSFET driving, here an example with an internal LDO; specially at "high" voltages.
  - Internal quiescent current I_q is in general quite small regarding gate driving needs.

$$P_{diss} = (V_{in} - V_{LDO}) * (\overline{IC} + I_q)$$

  - Depending overall thermal resistance of the IC mounted on PCB, too much dissipation could lead to thermal runaway or self-protection.



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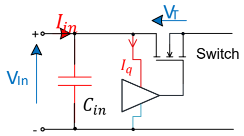
SMPS tips and tricks



- MOSFETs selection
  - Gate drive capabilities
  - Based on some datasheet info :

Gate Driver

t_r Gate Driver Output Rise Time	C_L = 3300pF (Note 5), $INTV_{CC}$ = 7.5V		22		ns
t_f Gate Driver Output Fall Time	C_L = 3300pF (Note 5), $INTV_{CC}$ = 7.5V		20		ns

$$\hat{I} = C \cdot \frac{\Delta U}{\Delta t} = \mathrm{C_{gate}} \cdot \frac{V_{gate}}{t_r} = 3{,}3\mathrm{nF} \cdot \frac{7{,}5}{20ns} \approx 1{,}2A$$

$$\mathrm{C_{gate}} = \mathrm{C_{iss}} \text{ in datasheets}$$

Despite of lack of information maximum drive strength could be retrieved.
Source : LT3758-3758A

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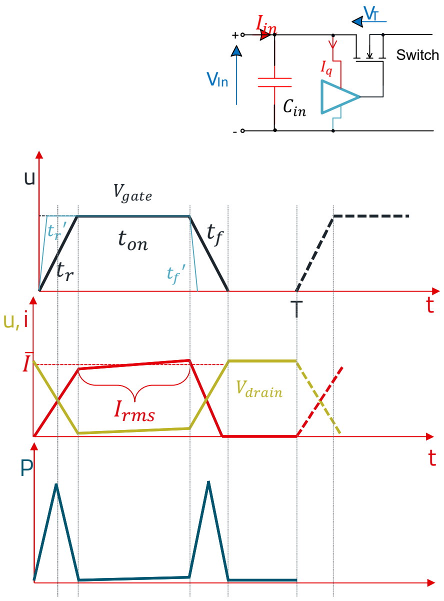
SMPS tips and tricks

- MOSFETs losses
  - Conduction losses, when closed
  - Switching losses, during transitions
  - Leak losses, when open

Consider **driver** rise and fall timings t_r' and t_f' insignificant vs MOSFET
Consider MOSFET delays td_{on} and td_{off} as null
Consider $I_{rms} \approx \bar{I}$ for realistic current ripple

- $P_{Cond} = Rds_{on} \cdot I_{rms}^2$ — Rds_{on}=MOSFET closed resistance
- $P_{sw} \approx \frac{U \cdot \bar{I} \cdot t_r}{2 \cdot T} + \frac{U \cdot \bar{I} \cdot t_f}{2 \cdot T}$ — U=voltage accros MOSFET
- $P_{leak} = U \cdot I_{leak}$ — I_{leak}=*leakage current*

$$\boldsymbol{P_{Tot} = U \cdot I_{leak} + RDS_{ON} \cdot I_{RMS}^2 + \frac{U \cdot \bar{I}}{2 \cdot T} \cdot (t_r + t_f)}$$



ANALOG DEVICES

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SMPS tips and tricks

- What is the **best** MOSFET ?!
  - Sometimes parameters could confuse designer and make mistakes happen

Most common: speak about $\boldsymbol{RDS_{ON}}$ all other parameters already selected
  - What is the best choice for best performances in a converter ?

BSC066N06NS		
Parameter	**Value**	**Unit**
Vds	60	V
RDSon	**6,6**	**mΩ**
Id	64	A
Qoss	19	nC
Qg	17	nC
tr	3	ns
tf	3	ns

BSC028N06NS		
Parameter	**Value**	**Unit**
Vds	60	V
RDSon	**2,8**	**mΩ**
Id	132	A
Qoss	43	nC
Qg	37	nC
tr	38	ns
tf	8	ns

ANALOG DEVICES

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GLOBAL POWER DESIGN SEMINAR TOUR

SMPS tips and tricks

Example converter with :

$24V_{in}$; $5V_{out}$; $f_{sw} = 250kHz$; $Iout = 5A$

BSC066N06NS | **BSC028N06NS**

$$P_{Tot} = U \cdot I_{DSS} + RDS_{ON} \cdot I_{RMS}^2 + \frac{U \cdot \bar{I} \cdot f_{SW}}{2} \cdot (t_r + t_f)$$

2,3x less RDS_{ON}

$$P_{Tot} = 24V \cdot 100\mu A + 6{,}6m\Omega \cdot 25 + \frac{19 \cdot 5 \cdot 250kHz}{2} \cdot (3ns + 3ns)$$

$$P_{Tot} = 24V \cdot 100\mu A + 2{,}8m\Omega \cdot 25 + \frac{19 \cdot 5 \cdot 250kHz}{2} \cdot (38ns + 8ns)$$

$$P_{Tot} = 2{,}4mW + \mathbf{165mW} + \mathbf{71mW} = 238mW$$

$$P_{Tot} = 2{,}4mW + \mathbf{70mW} + \mathbf{546mW} = 618mW$$

x2,6 more losses !

Despite of more than half RDS_{ON}, dynamic behavior is near catastrophic and no so huge frequency

The best choice is not the one who seems to be

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FILTERING CONSIDERATIONS FOR DC/DC CONVERTERS

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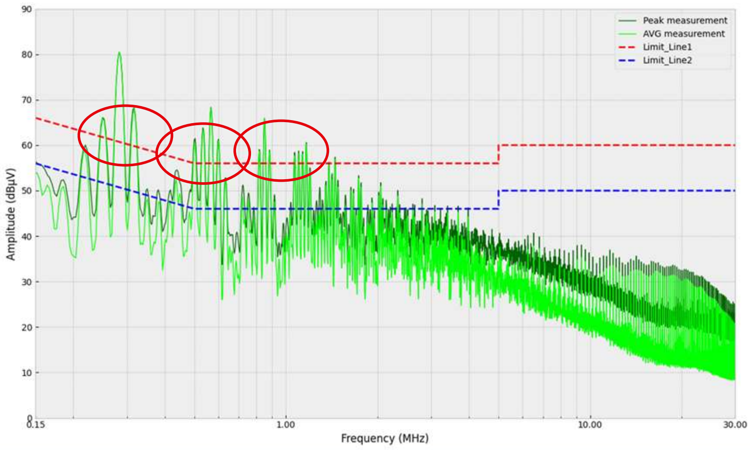
SMPS FILTERING

Why do we need a filter ?

- How to meet EMC standards requirements?



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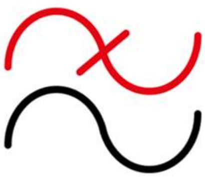
GLOBAL POWER DESIGN SEMINAR TOUR

Filtering considerations

- SMPS filtering
  - Common mode
  - Differential mode



  - Input filtering
  - Output filtering

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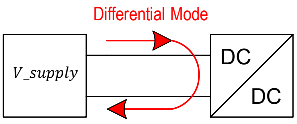
SMPS FILTERING

EMI noises sources and types : Two different coupling schemes exists

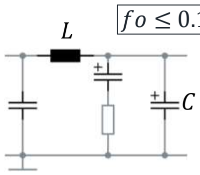
- Differential mode



  - Source from current loop $^{di}/_{dt}$
  - Coupling by inductive way
  - More related to main switch frequency and harmonics

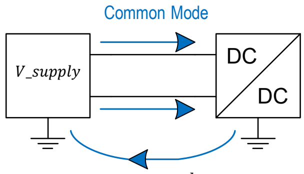
  ➢ Filtered by LC filter

$$f_0 = \frac{1}{(2 \cdot \pi \cdot \sqrt{L \cdot C})}$$



$fo \leq 0.1 \cdot f_{sw}$

- Common mode

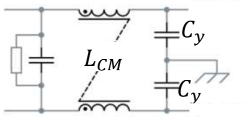


  - Source from voltage $^{dv}/_{dt}$
  - Coupling via capacitive way
  - More related to switching noises and ringing

  ➢ Filtered by **C**ommon **M**ode **C**hoke filter and Y-Caps

$fo \leq 0.1 \cdot f_{sw}$

$$f_0 = \frac{1}{(2 \cdot \pi \cdot \sqrt{L_{CM} \cdot 2 \cdot C_y})}$$



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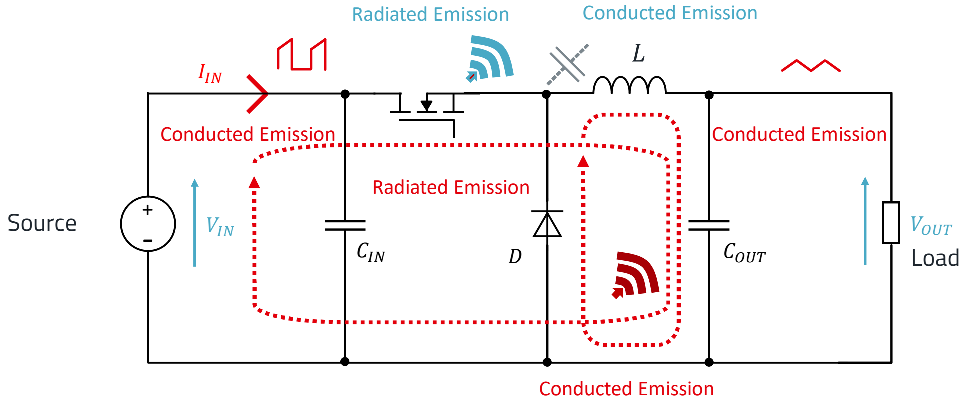
WHERE THE NOISE COME FROM

Buck topology



High di/dt cause differential mode currents by magnetic loops
High dv/dt common mode currents through parasitic capacitances

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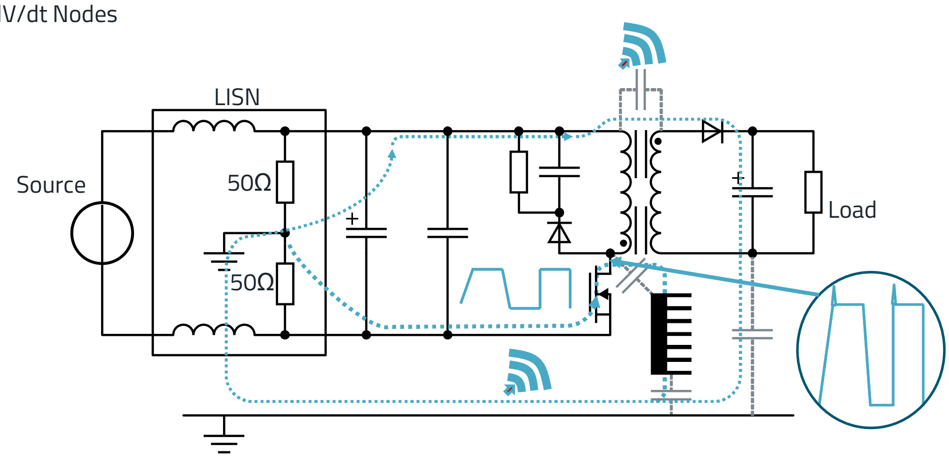
WHERE THE NOISE COME FROM

Flyback : High dV/dt Nodes



High dV/dt common mode currents through parasitic capacitances
(electric dipole and monopole antennas)

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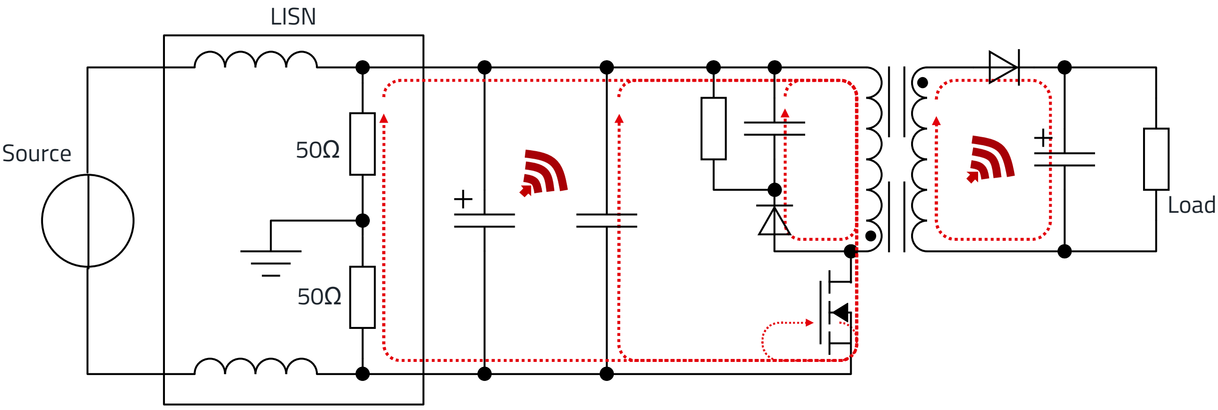
WHERE THE NOISE COME FROM

Flyback : High di/dt Loops



Inductive coupling caused by high di/dt differential mode currents
(magnetic loop antennas)

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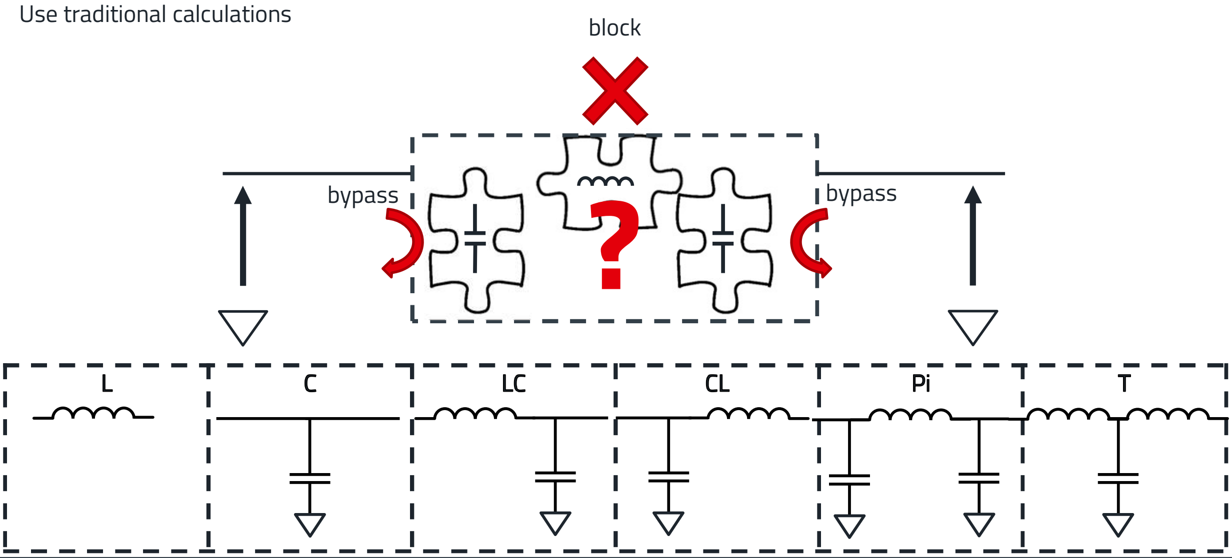
FILTER TOPOLOGIES FOR IMPEDANCE SYSTEM

Use traditional calculations

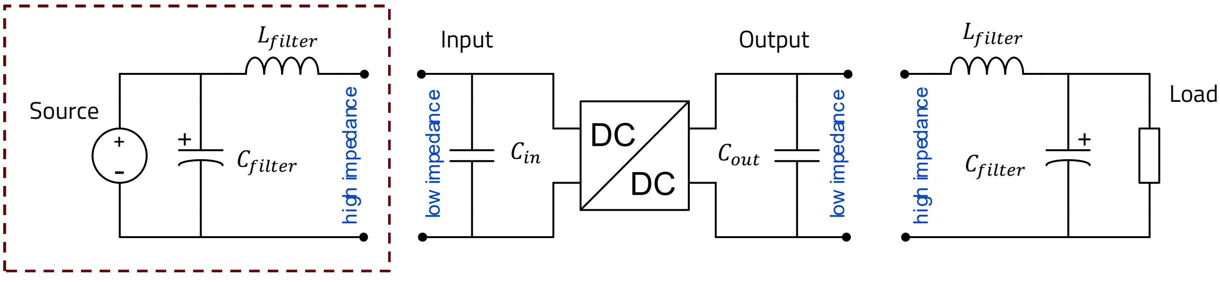


GLOBAL FILTERING

SMPS filtering : differential mode

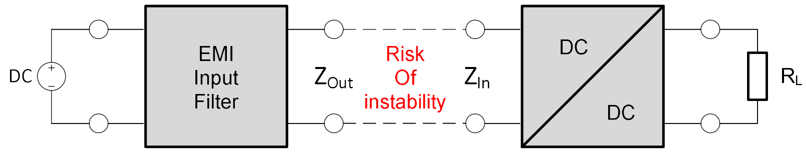
- Quick design : differential mode filtering
  - A rule of thumb is to set first -40dB attenuation noises, to set filter frequency $\frac{1}{10}$ of switching frequency.

$$L_{filter} = \frac{1}{\left(2 \cdot \pi \cdot \frac{f_{sw}}{10}\right)^2 \cdot C_{filter}}$$



OSCILLATION AT CONVERTER INPUT

CE DIFFERENTIAL MODE INPUT FILTER DESIGN



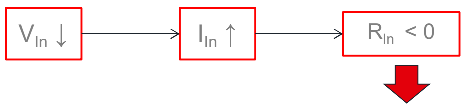
- Adding an input EMI filter to converter input can cause oscillation at converter input
- Problem could arise : the converter no longer meets response specification and may even become unstable!!!

Why????

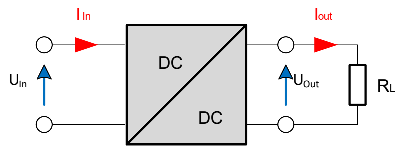
INPUT IMPEDANCE OF CONVERTER (AN EXPLANATION)

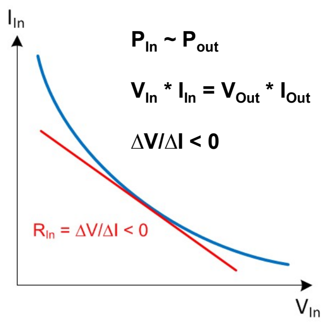
CE DIFFERENTIAL MODE INPUT FILTER DESIGN

- Input and output power of converter is near the same (efficiency drop)
- Under stable conditions output power is constant
- If the input voltage falls, the input current increases
- Voltage-current line has a negative slope



NEGATIVE DC INPUT RESISTANCE

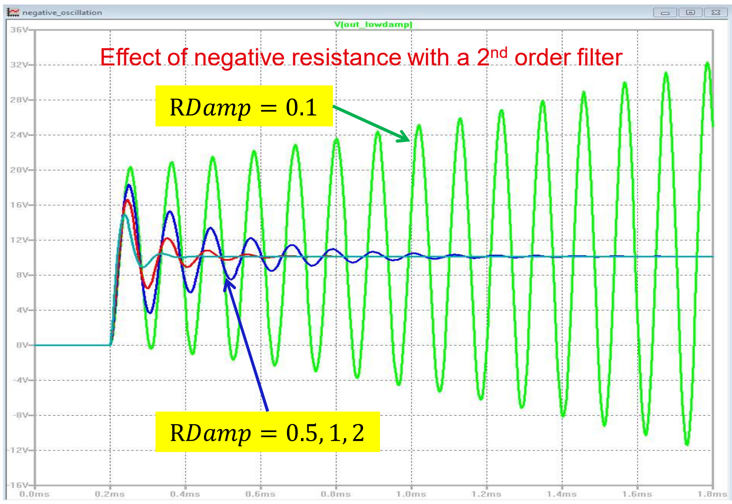




INSTABILITY

CE DIFFERENTIAL MODE INPUT FILTER DESIGN

Take care



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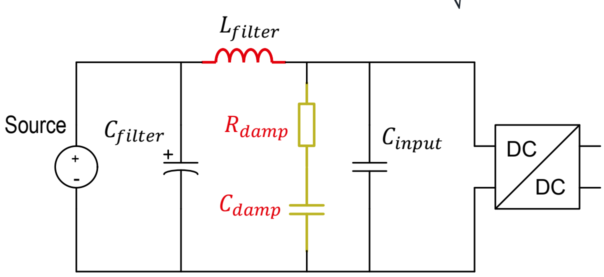
FILTERING DRAWBACK SOLUTION

SMPS filtering

- **Filter fitting**
  - Caution must be observed with filtering, when inserting **magnetics** in power lines
  - Dampening is necessary to calm down any resonance effect
    - A dampening factor ζ of 0.707 is sufficient
  - A rule of thumb is to set few ohms max to *R_damp*
  - C_{damp} value near to C_{input} to avoid high '*n*' value
  - '*n*' should be 4 or 6
    - Possible with different capacitor technologies

$$n = \frac{C_{damp}}{C_{filter}}$$

$$\zeta = \frac{n+1}{n} \cdot \frac{L_{filter}}{2 \cdot R_{damp} \cdot \sqrt{L_{filter} \cdot C_{input}}}$$



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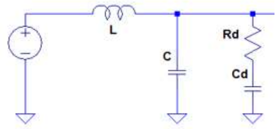
CALCULATING INPUT FILTER COMPONENTS VALUES

1) Calculate damping capacitor $C_d = \mathrm{n} \cdot Cf \quad with\ n = 4\ or\ 6$

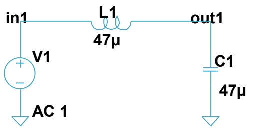
2) Calculate damping Resistor $R_d = \sqrt{\frac{L_f}{C_f}\frac{(n+1)}{2n}}\sqrt{\frac{2n^2(4+n)}{(2+n)(4+3n)}}$

Keeping the same values of undamped filter, we can add an Rd and a Cd as follows:

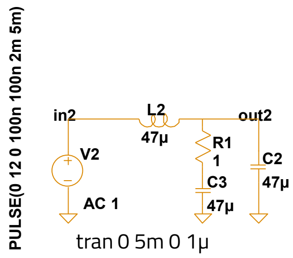


GLOBAL FILTERING

SMPS filtering : differential mode

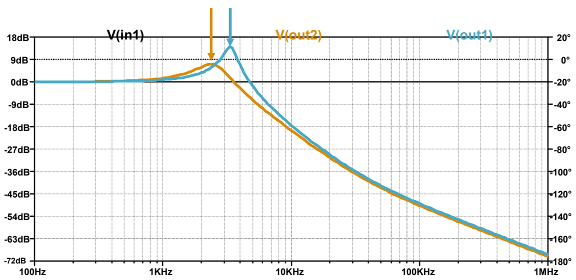


.ac dec 100 100 1Meg

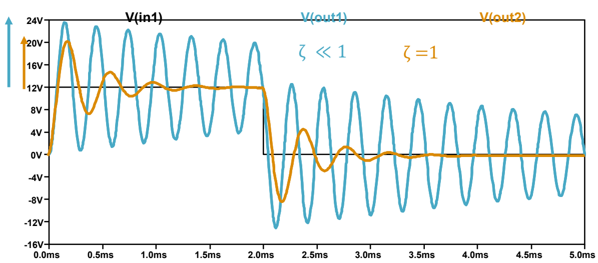


tran 0 5m 0 1µ

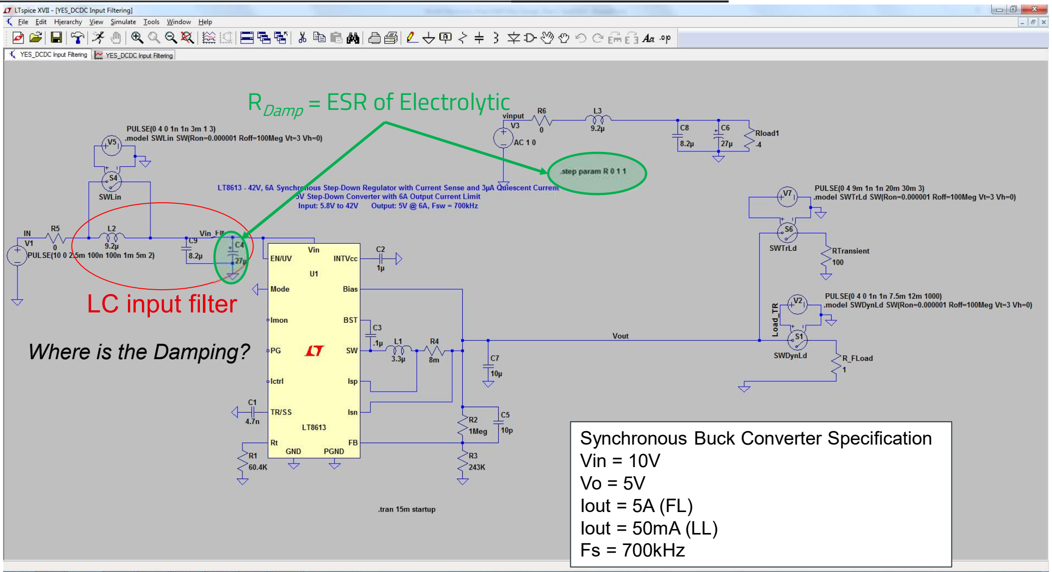
- **Frequency domain :**



- **Time domain:**



CE DIFFERENTIAL MODE FILTER DESIGN – BUCK EXAMPLE



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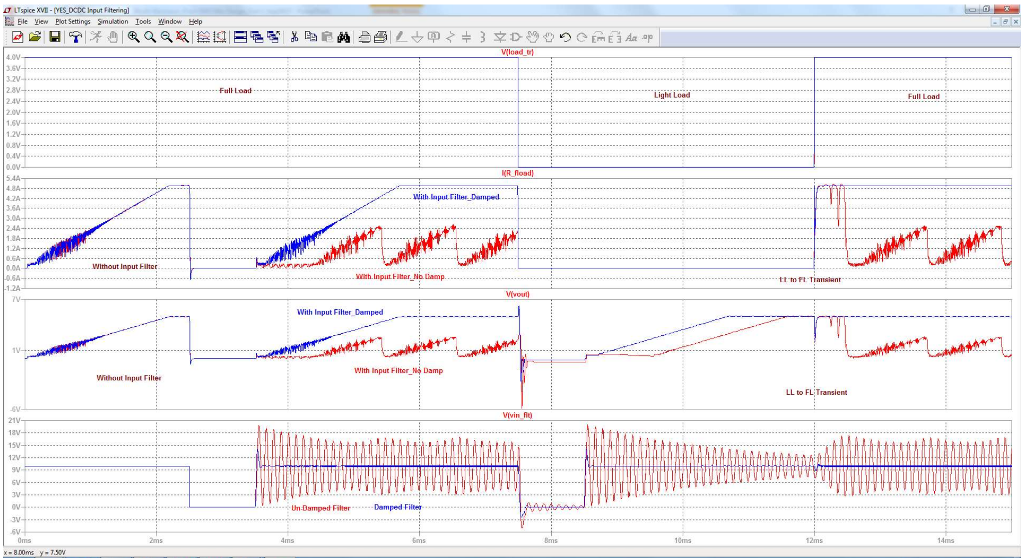
CE DIFFERENTIAL MODE FILTER DESIGN – BUCK EXAMPLE



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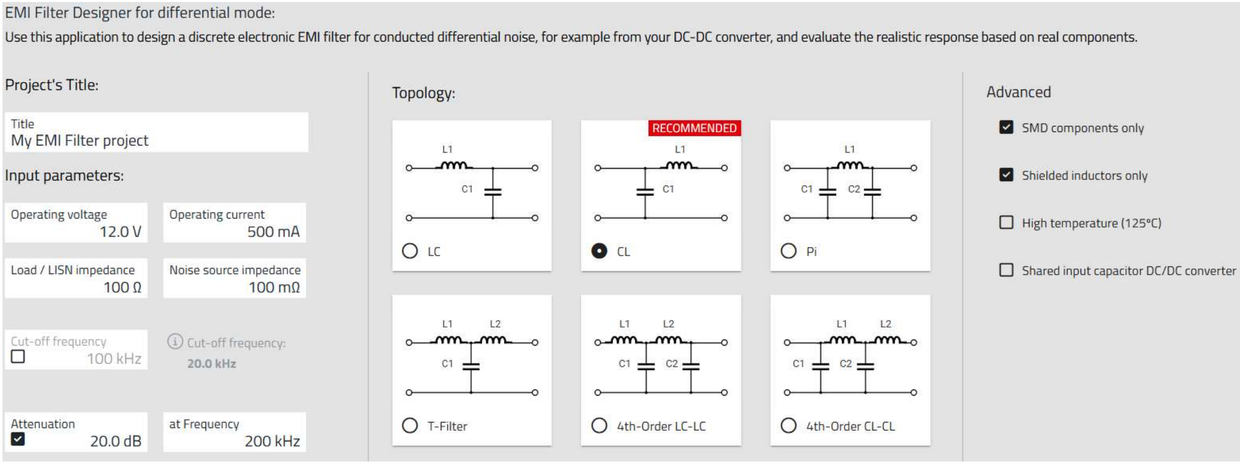
REDEXPERT

FILTER TOPOLOGIES FOR IMPEDANCE SYSTEM

Use **REDEXPERT** Tool: SMART way



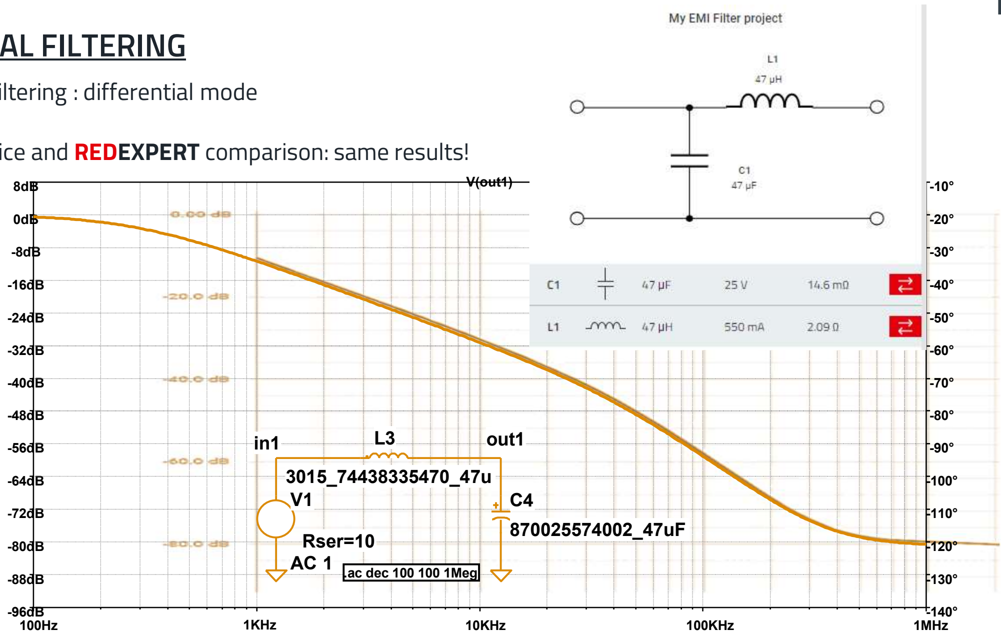
https://redexpert.we-online.com/we-redexpert/en/#/emifd-embedded

REDEXPERT

GLOBAL FILTERING

SMPS filtering : differential mode

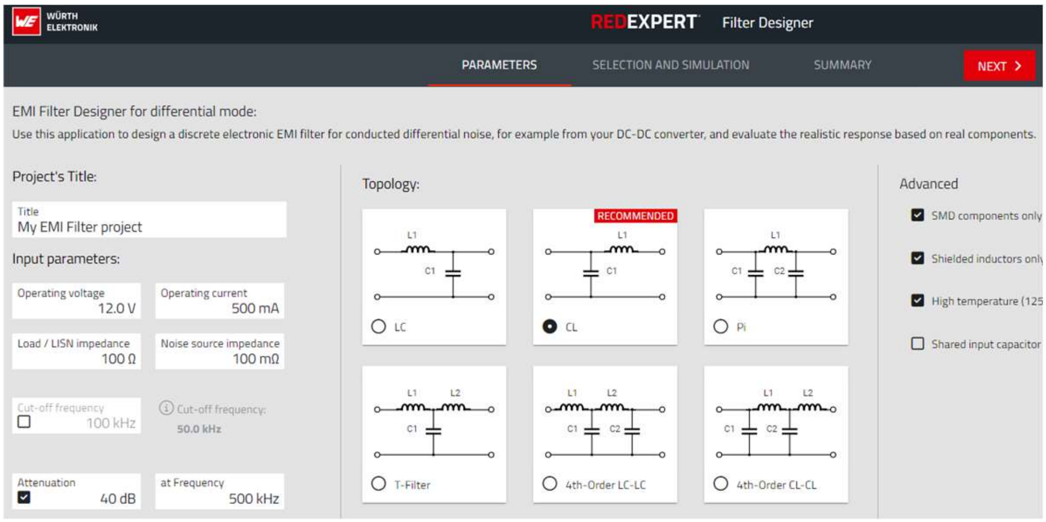
- LtSpice and **REDEXPERT** comparison: same results!



REDEXPERT

FILTER TOPOLOGIES FOR IMPEDANCE SYSTEM

Use **REDEXPERT** Tool: SMART way → EMI Filter Designer

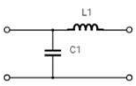


ANALOG DEVICES

FILTER TOPOLOGIES FOR IMPEDANCE SYSTEM

REDEXPERT EMI Filter Designer

Circuit Schematic



Specifications Edit

"My EMI Filter project"

TYPE: CL
V_{op}: 12.0 V
I_{op}: 500 mA
LOAD / LISN IMPEDANCE: 100 Ω
NOISE SOURCE IMPEDANCE: 100 mΩ
ILOSS -46.6 dB@500 kHz

Bill Of Materials ADD

#	N...	Order Code	Value	Properties	Qty
1.	C1	875105445006	47.0 µF	Capacitance = 47.0 µF Footprint = 43.6 mm² Rated Voltage = 20.0 V Height = 7.70 mm	1
2.	L1	744383130082	820 nH	Footprint = 2.56 mm² Inductance = 820 nH Rated Current = 2.35 A DC Resistance = 115 mΩ	1

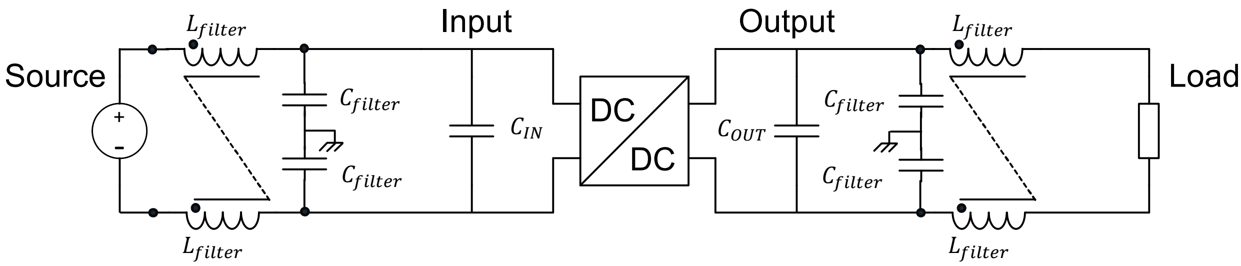
ANALOG DEVICES

GLOBAL FILTERING

SMPS filtering : common mode

- Quick design : common mode filtering
  - To reach around 30dB~40dB attenuation :
  - ➔ Corner frequency of LC filter < 5~10 time less than converter working frequency.

$$L_{filter} = \frac{1}{\left(2 \cdot \pi \cdot \frac{f_{SW}}{5\sim10}\right)^2 \cdot C_{filter}}$$



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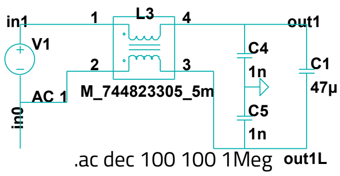
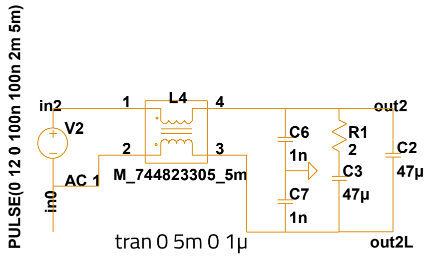
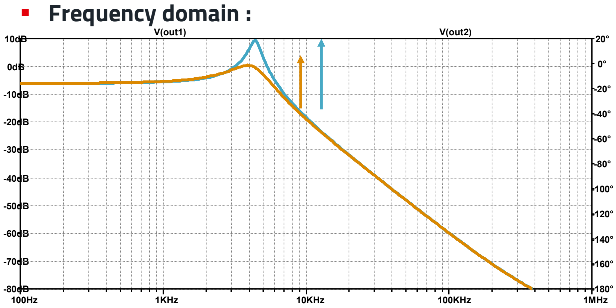
GLOBAL FILTERING

SMPS filtering : common mode





- **Frequency domain :**



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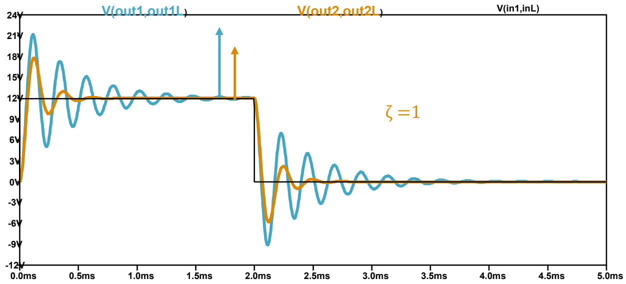

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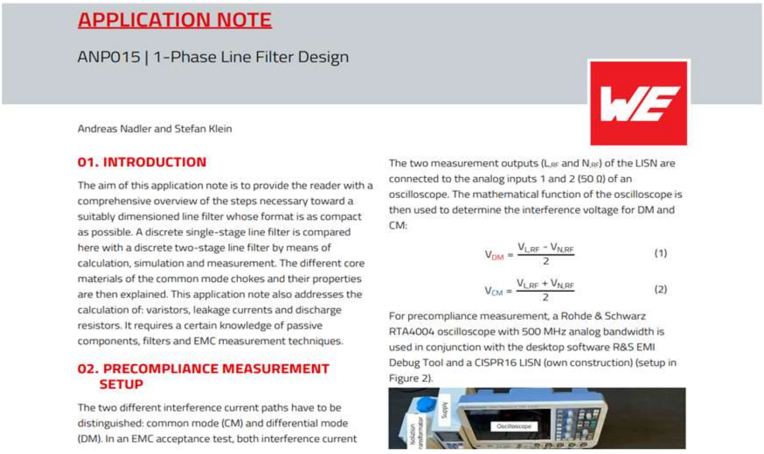
APPNOTE ANP015

DCDC & ACDC Filter Calculation / LT Spice Simulation / Measurement / Layout

ANP015



APPLICATION NOTE

ANP015 | 1-Phase Line Filter Design

Andreas Nadler and Stefan Klein

01. INTRODUCTION

The aim of this application note is to provide the reader with a comprehensive overview of the steps necessary toward a suitably dimensioned line filter whose format is as compact as possible. A discrete single-stage line filter is compared here with a discrete two-stage line filter by means of calculation, simulation and measurement. The different core materials of the common mode chokes and their properties are then explained. This application note also addresses the calculation of: varistors, leakage currents and discharge resistors. It requires a certain knowledge of passive components, filters and EMC measurement techniques.

02. PRECOMPLIANCE MEASUREMENT SETUP

The two different interference current paths have to be distinguished: common mode (CM) and differential mode (DM). In an EMC acceptance test, both interference current

The two measurement outputs (L_{RF} and N_{RF}) of the LISN are connected to the analog inputs 1 and 2 (50 Ω) of an oscilloscope. The mathematical function of the oscilloscope is then used to determine the interference voltage for DM and CM:

$$V_{DM} = \frac{V_{L,RF} - V_{N,RF}}{2} \quad (1)$$

$$V_{CM} = \frac{V_{L,RF} + V_{N,RF}}{2} \quad (2)$$

For precompliance measurement, a Rohde & Schwarz RTA4004 oscilloscope with 500 MHz analog bandwidth is used in conjunction with the desktop software R&S EMI Debug Tool and a CISPR16 LISN (own construction) (setup in Figure 2).

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REAL SHOWCASE

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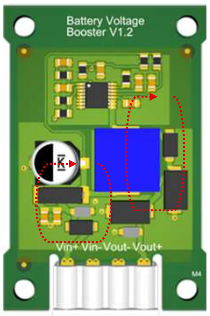
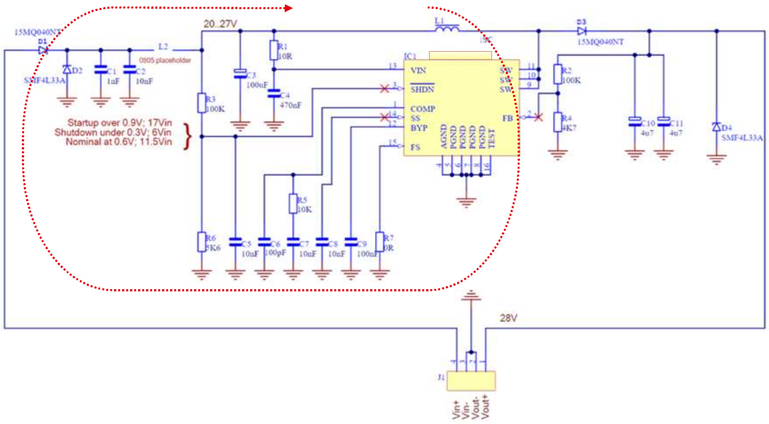
SMPS FILTERING

Real board from a customer support : First release(s)

- Board
- Schematic





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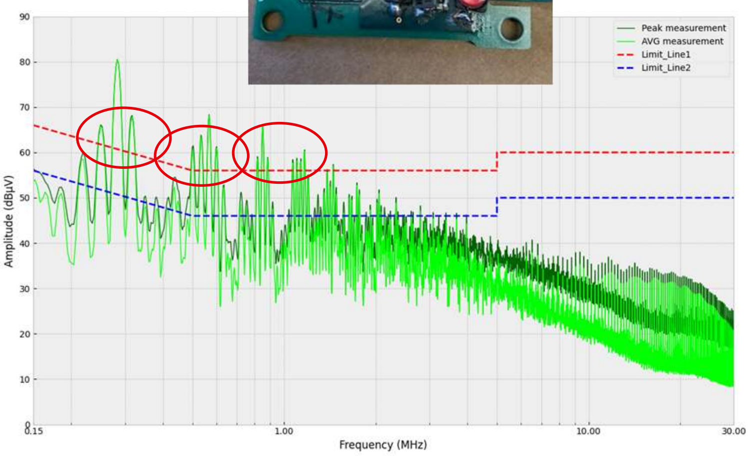
SMPS FILTERING

EMC conducted emissions

- No filter : no chance to pass EMC



ANALOG DEVICES

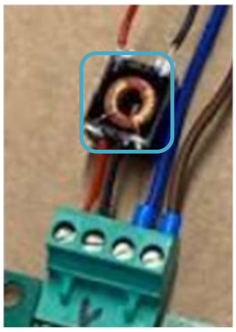
SMPS FILTERING

Why do we need a filter ?

- Real case : application CM + 2* DM (input / output)
  - CM : WE-UCF

  - DM : 2* WE-LHMI

- Modifications on the first release



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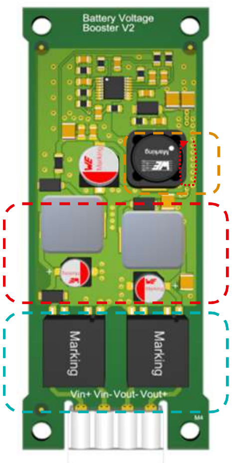
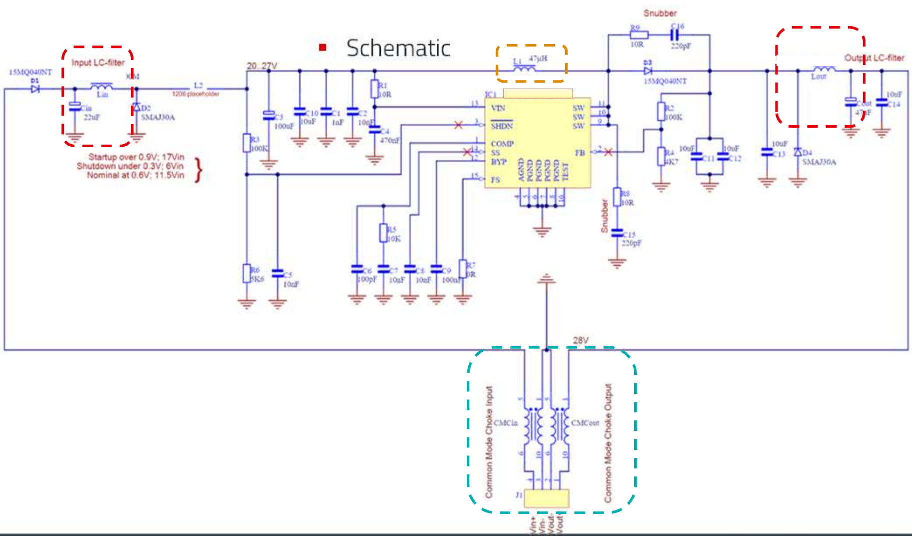
SMPS FILTERING

Last release

- Board



- Schematic



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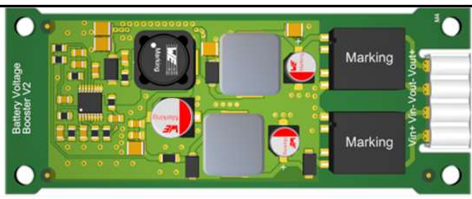
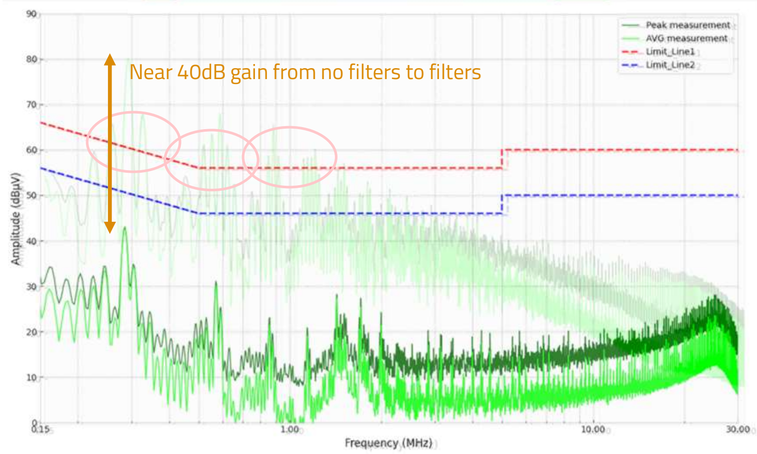
SMPS FILTERING

Final results with a filter!

- Final version !





- But what should be improved?

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EMC SIMULATION

- The most portable Lab

LTspice®

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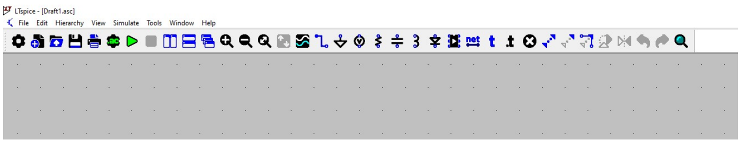

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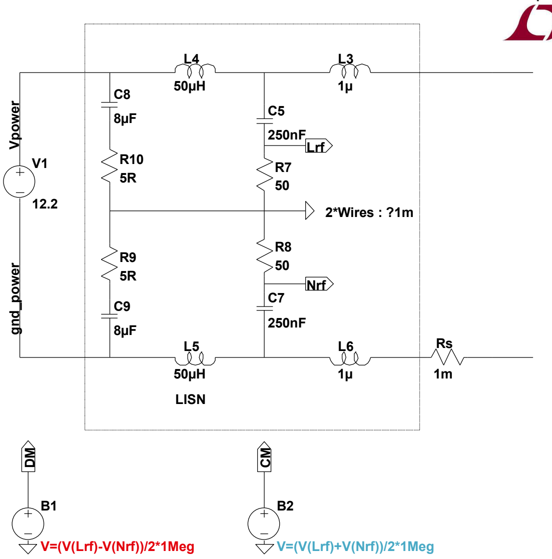
LTSPICE SIMULATION

LISN

- Schematic
  - Typical schematic for a LISN, very common
- Common mode / differential mode
  - **CM** and **DM** are made from noise nodes Lrf and Nrf with a sum or difference



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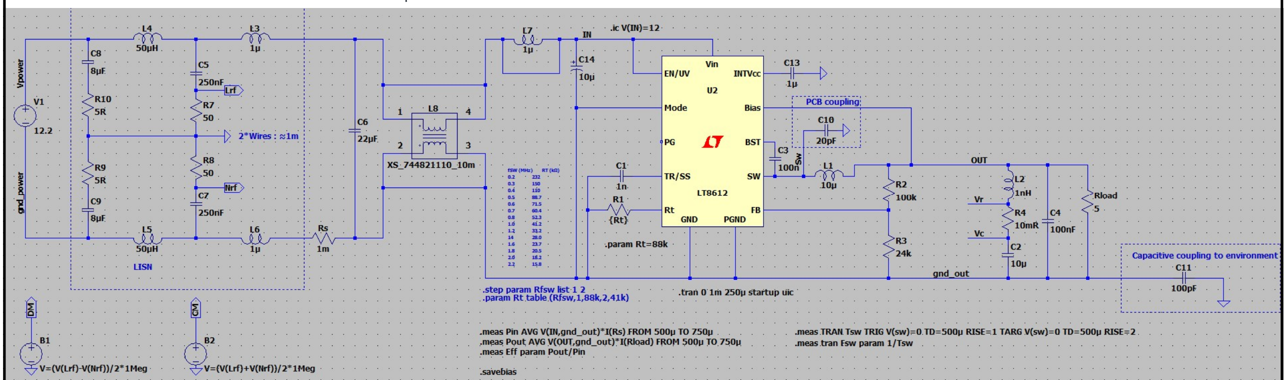
LTSPICE SIMULATION

Fsw=500kHz, Buck LT8612 12-5V 1A

- Schematic
  - $V_{DM}(\mu V) = \frac{V_{LRF}-V_{NRF}}{2} * 1\,000\,000$ $\quad V_{CM}(\mu V) = \frac{V_{LRF}+V_{NRF}}{2} * 1\,000\,000$

$dB\mu V = 20 \cdot \log(\frac{U(V)}{1\mu V})$ ⇔ $1\mu V = 0dB\mu V$ $\quad 1V = 1\,000\,000\mu V = 20 \cdot \log(10^6) = 120dB\mu V$



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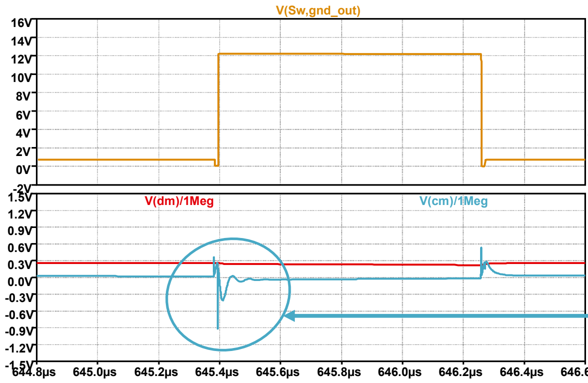
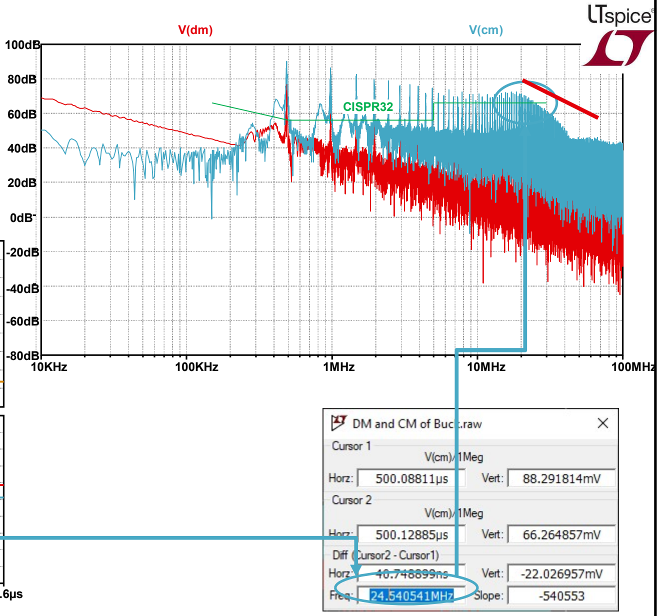
LTSPICE SIMULATION

Fsw=500kHz, Buck LT8612 12-5V 1A

- Time and frequency link
  - Perturbation frequency





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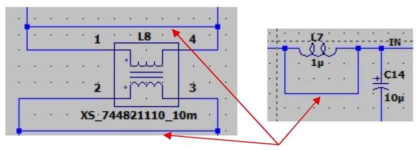
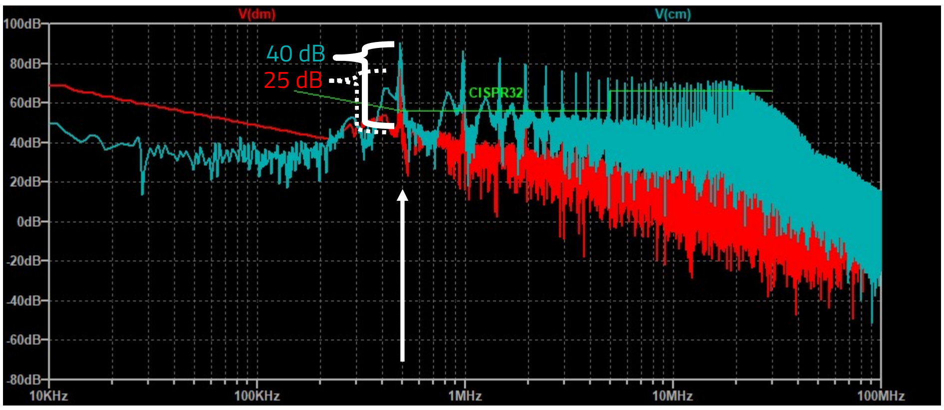
LTSPICE SIMULATION

Fsw=500kHz, Buck LT8612 12-5V 1A

- **No filter** :extra wideband noises, Fsw main disturbance



Short Circuit



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LTSPICE SIMULATION

RED EXPERT Selection of the differential Mode Inductor

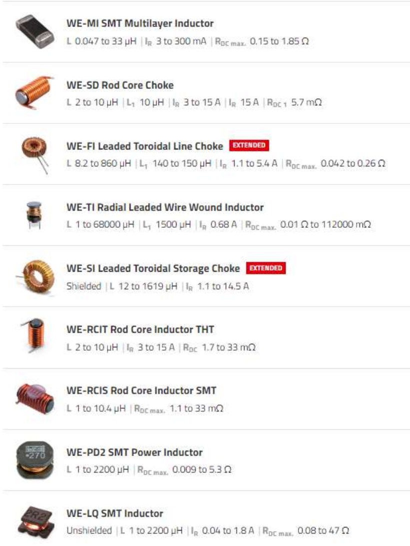
- Quick calculation example

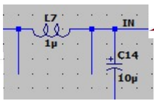
$$L_{filter} = \frac{1}{\left(2 \cdot \pi \cdot \frac{f_{sw}}{10}\right)^2 \cdot C_{filter}} = \frac{1}{\left(2 \cdot \pi \cdot \frac{500k}{10}\right)^2 \cdot 10\mu F}$$

$$L_{filter} = \frac{1}{(2 \cdot \pi \cdot 50k)^2 \cdot 10\mu F}$$

$$L_{filter} = 1\mu H$$

Iterative calculation could be used to reach a common value, **frequency does not be ultra precise.**





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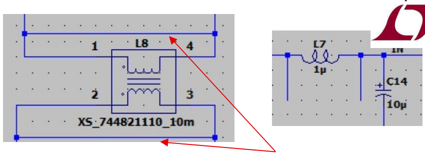
LTSPICE SIMULATION

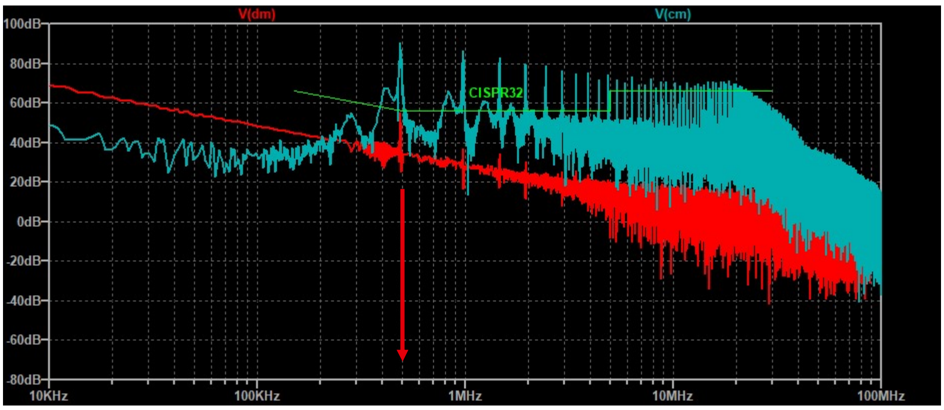
LtSpice simulation

- **With DM only** : DM filtering action !



Short Circuit

$$L_{filter} = 1\mu H$$



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LTSPICE SIMULATION

Selection of the Common Mode chokes (Fsw=500kHz, Buck LT8612 12-5V 1A ($I_{in} > 400mA$)

- Need 40 dB for 500kHz and try to find wide BW : 100kHz to 10MHz

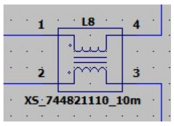
Use **REDEXPERT**

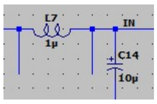
WE-CMB – XS comparison

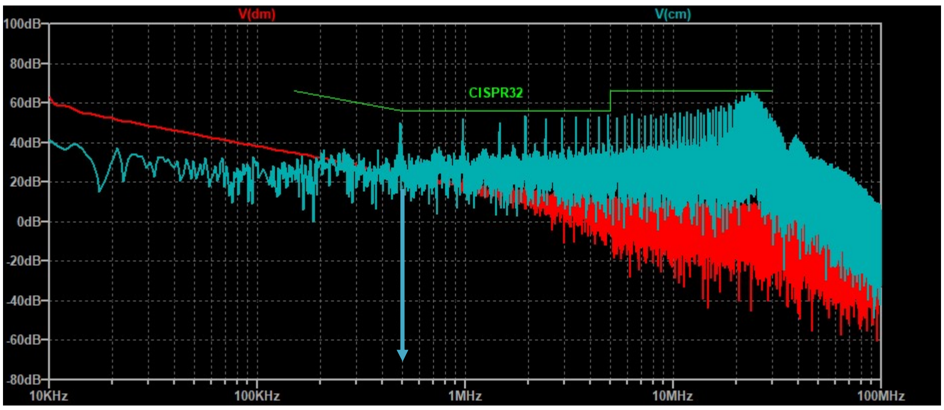
10mH 744821110 seems to be well centered and enough attenuation

LtSpice simulation

- With DM+CM : Noise killer… Ready to go to EMC Lab!







$L_{CMC}=10mH$

BREAK

Networking : Take a rest !

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CLOSE THE LOOP!

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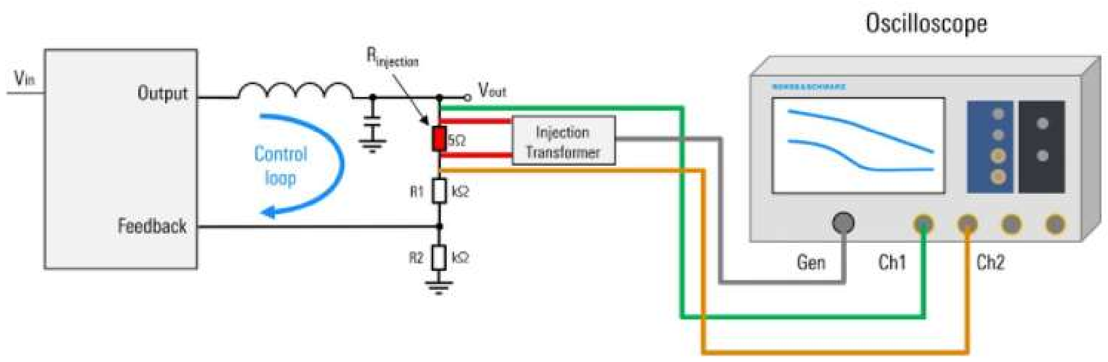
ART OF LOOP COMPENSATION

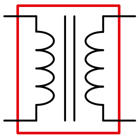
Control theory and loop

POSSIBLE SETUP

Bode plot of the control loop (plant + compensator)

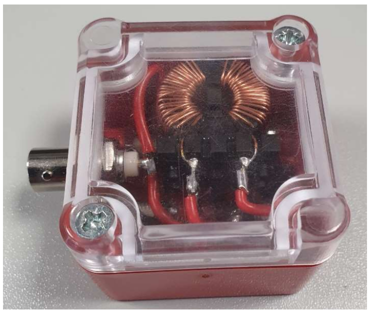


LOOP COMPENSATION



DIY Injection transformer

- Use a wideband common mode choke as small signal transformer
- BOM:
  - Choke: **35mH** WE-CMBNC #7448040435
  - Box: Z116PH/RD by Kradex
  - Bananas: bil-20-sw & bil-20-rt HIRSCHMANN T&M
  - Coax: 4067878 Amphenol RF



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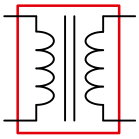
LOOP COMPENSATION



DIY Injection transformer : flat response from 10Hz to 1 MHz!

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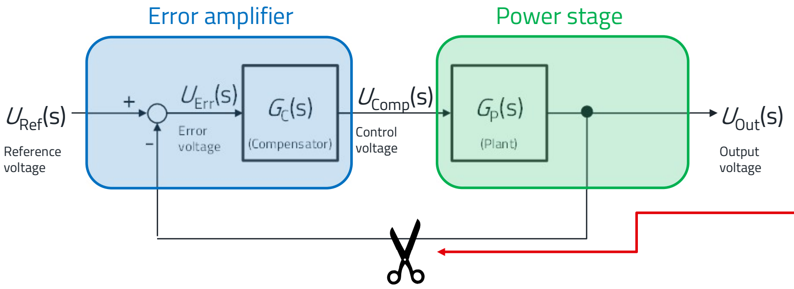
BASICS OF CONTROL THEORY

Open / Close loop transfer function

$$\text{transfer function (s)} = \frac{\text{Output (s)}}{\text{Input (s)}}$$



Closed Loop / Block-diagram

- **U_{Ref}(s):** Reference voltage = setpoint
- **U_{Err}(s):** Error voltage = Error
- **U_{Comp}(s):** Control voltage = system input
- **U_{Out}(s):** Output voltage = system output
- **G_C(s):** Transfer function of the compensator
- **G_P(s):** Transfer function of the plant
- target/actual comparison + compensator = **Error amplifier**

$$G_{OL}(s) = \frac{U_{Out}(s)}{U_{Err}(s)} = G_C(s) \cdot G_P\,(s)$$

- Open loop transfer function

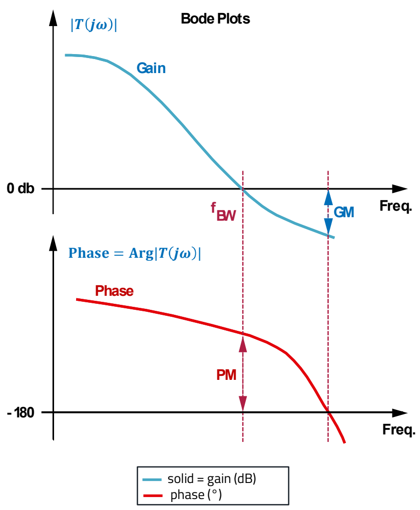
$$G_{CL}(s) = \frac{U_{Out}(s)}{U_{Ref}(s)} = \frac{G_{OL}(s)}{1+G_{OL}(s)}$$

- Closed loop transfer function

LOOP COMPENSATION

Theory refresh

- **Cross over frequency (bandwidth) - f_{BW}**
  - Frequency at which the gain crosses 0dB („1“)
- **Phase margin - P_M**
  - Phase left to -180° when the gain reaches 0dB
  - **Important note:**
    - If the open loop transfer function is measured in a closed loop configuration (by Frequency Response Analysis) -180° corresponds to 0°
    - Reason is the inverting behavior of the error amplifier which is automatically considered
    - The phase margin can be read directly from 0° (this is the case in all following slides)
- **Gain margin - G_M**
  - Gain below 0dB when the phase reaches -180° („-“)

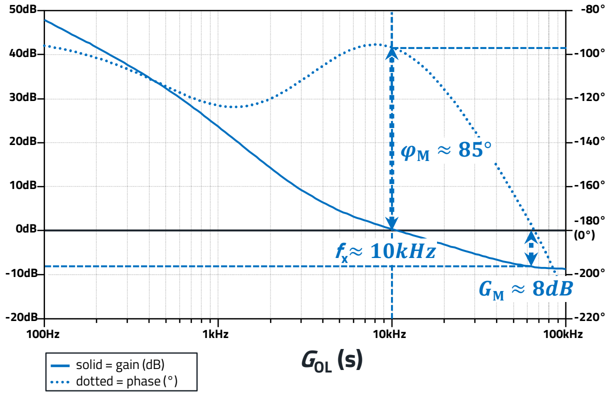


Typical bode plot – Open loop

BASICS OF CONTROL THEORY

Identify stability on an open loop bode plot

- **Cross over frequency (bandwidth) - f_x**
  - Frequency at which the gain crosses 0dB („1“)
  - Usually a maximum of 1/10th of the switching frequency is desired
  - **Higher cross over frequency → Faster transient response**
- **Phase margin - φ_M**
  - Phase left to -180° when the gain reaches 0dB
  - Should be ≥ 45°(60° preferred)
  - **Lower phase margin → more oscillating in transient response (load step)**
- **Gain margin - G_M**
  - Gain below 0dB when the phase reaches -180° („-“)
  - 10-15dB is considered good
  - **Gain margin too low → low variation robustness → oscillations could be the result**



Typical bode plot – Open loop

If the open loop transfer function is measured in a closed loop configuration (by Frequency Response Analysis) -180° corresponds to 0°. Reason is the inverting behavior of the error amplifier which is automatically considered. The phase margin can be read directly from 0° (this is the case in all following slides)

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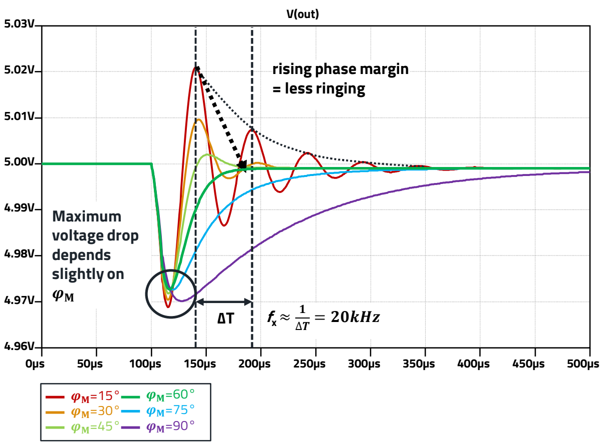
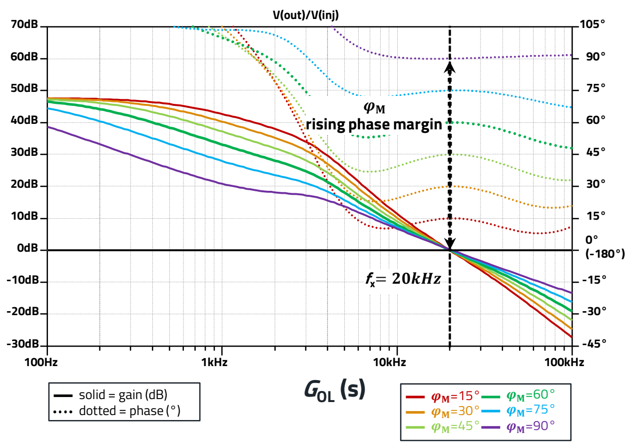
IMPACT OF PHASE MARGIN

Simulation – Buck Demo Board with various compensators



Load step response: I_{Out} 1A → 2A / U_{In}=19V



Bode plot - Open loop: I_{Out}=2A / U_{In}=19V

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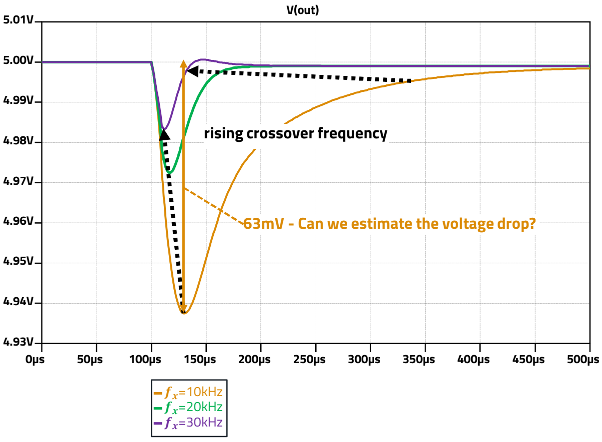
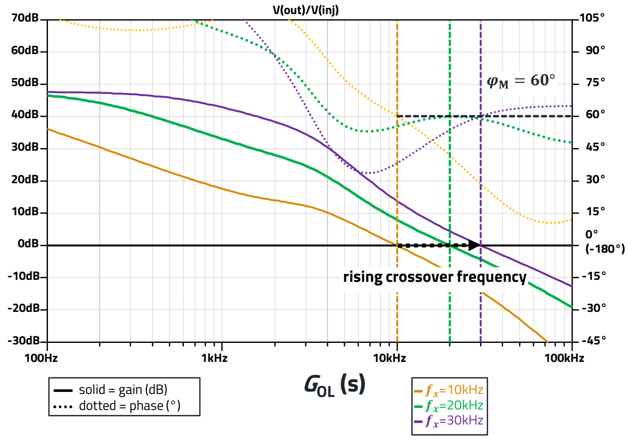
IMPACT OF CROSSOVER FREQUENCY

Simulation – Buck Demo Board with various compensators



Load step response: I_{Out} 1A → 2A / U_{In}=19V



Bode plot - Open loop: I_{Out}=2A / U_{In}=19V

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PLANT TRANSFER FUNCTION

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TRANSFER FUNCTION OF THE PLANT

What does it depend on?

- The plant transfer function depends on:
  - Control technique (e.g. voltage- / current-mode control)
  - Topology of the converter (e.g. buck, boost)
  - Conduction mode (DCM – discontinuous conduction mode, CCM – continuous conduction mode)
  - Controller IC (internal gains, compensation ramp)
  - Components used (capacitors, inductors, power semiconductors)
  - Input- and output-voltage
  - Load

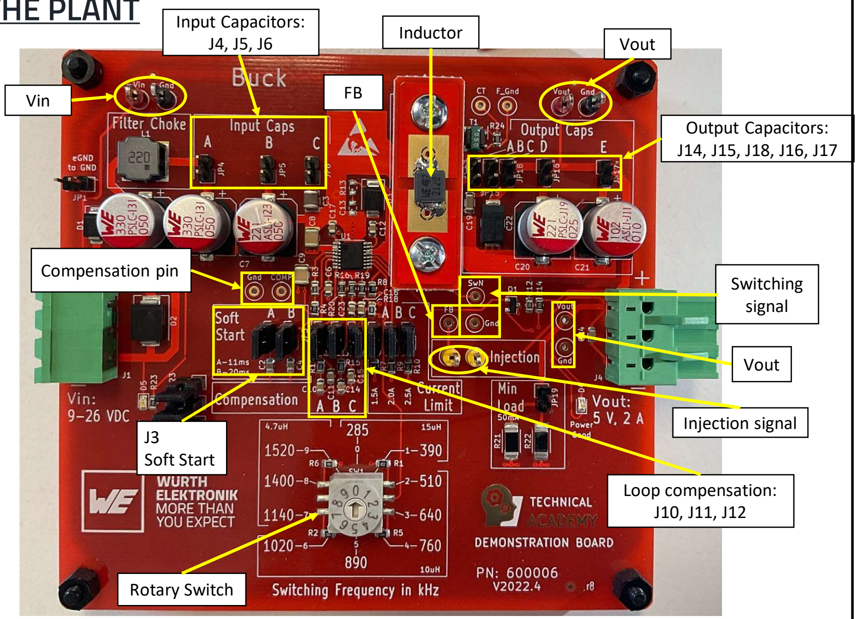
TRANSFER FUNCTION OF THE PLANT

Buck Demo Board

General Specification

- DC/DC Buck Converter
  - *Voltage Mode control*
  - *CCM*
  - V_{in} = 9-26V
  - V_{out} = 5V
  - $I_{out,max}$ = 2A
  - $P_{out,max}$ = 10W
  - f_{sw} = 285kHz – 1.52MHz

- Inductor: 10µH/3A WE-LHMI 74437346100

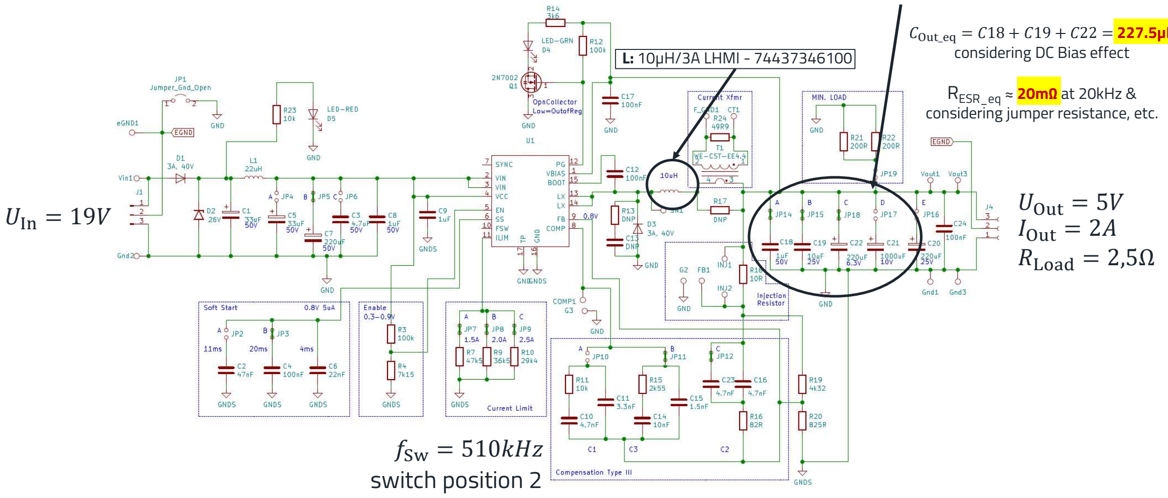


TRANSFER FUNCTION OF THE PLANT

Schematic and setup - Buck Demo Board

REDEXPERT

	C18	C19	C22
	885012207103 WCAP-CSGP X7R 0805 1µF 50V	885012108021 WCAP-CSGP X5R 1206 10µF 25V	875015119006 WCAP-PHGP H-Chip Polymer 220µF 6.3V
$ESR\ @\ 20kHz$	45mΩ	22mΩ	5mΩ



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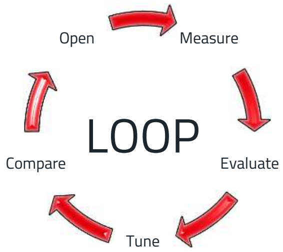
TRANSFER FUNCTION OF THE PLANT

Evaluate the transfer function



- How?
  - IC **datasheet**
  - **Mathematical** modeling (MATLAB, Mathcad, etc.)
  - **Simulation** (average model of the plant)
  - **Measurements**

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TRANSFER FUNCTION OF THE PLANT

Plant transfer function - model accuracy

$$G_P(s) = A_{PWM} \cdot \frac{1 + \frac{s}{\omega_{Z,ESR}}}{1 + \frac{s}{Q_0 \cdot \omega_0} + \frac{s^2}{{\omega_0}^2}}$$

- **simplified transfer function**
  - Plant (in CCM) is basically a second-order response (like a LC-filter)
  - LC double pole (complex conjugate pole)
  - ➢ $\omega_0 = \frac{1}{\sqrt{L \cdot C_{Out}}} \rightarrow f_0 = \frac{1}{2\pi\ \sqrt{L \cdot C_{Out}}} \rightarrow f_0 = \frac{1}{2\pi \cdot \sqrt{10\mu H \cdot 22\ \ ,5\mu F}} \approx \mathbf{3,338kHz}$
  - Quality of the LC double pole:
  - ➢ $Q_0 = \frac{R_{Load}}{\sqrt{\frac{L}{C_{Out}}}} = \frac{2{,}5\Omega}{\sqrt{\frac{10\mu H}{227.5\mu F}}} \approx \mathbf{11.92}$

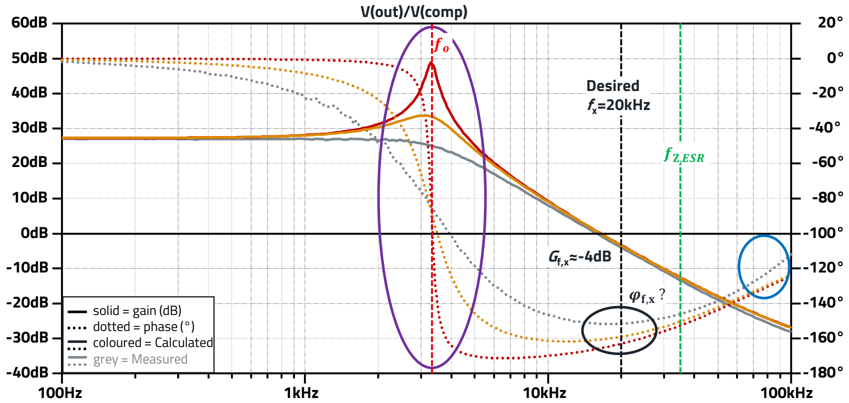
- **more detailed transfer function**
  - **LC double pole (complex conjugate pole)**
  - ➢ $\omega_0 = \frac{1}{\sqrt{L \cdot C_{Out} \cdot \left(1 + \frac{R_{ESR}}{R_{Load}}\right)}} = \frac{1}{\sqrt{10\mu H \cdot 227{,}5\mu F \cdot \left(1 + \frac{20m\Omega}{2{,}5\Omega}\right)}} \approx 20{,}882 \cdot 10^3 \frac{rad}{s}$
    $\rightarrow f_0 \approx \mathbf{3,325kHz}$
  - **ESR-zero:**
  - ➢ $\omega_{Z,ESR} = \frac{1}{R_{ESR} \cdot C_{Out}} \rightarrow f_{Z,ESR} = \frac{1}{2\pi \cdot R_{ESR} \cdot C_{Out}}$
  - ➢ $f_{Z,ESR} = \frac{1}{2\pi \cdot 20m\Omega \cdot 227{,}5\mu F} \approx \mathbf{34,997kHz}$
  - ➢ $OR\ f_{Z,ESR} = \frac{1}{2\pi \cdot 10m\Omega \cdot 231\mu F} \approx \mathbf{68,9kHz}$ **??**
  - **Quality of the LC double pole:**
  - ➢ $Q_0 = \frac{1}{\omega_0 \cdot \left(\frac{L}{R_{Load}} + C_{Out} \cdot \left(R_{ESR} + \left(1 + \frac{R_{ESR}}{R_{Load}}\right) \cdot R_{Ldc}\right)\right)} =$
    $\frac{1}{20{,}88 \cdot 10^3 \frac{rad}{s} \cdot \left(\frac{10\mu H}{2{,}5\Omega} + 227{,}5\mu F \cdot \left(20m\Omega + \left(1 + \frac{20m\Omega}{2{,}5\Omega}\right) \cdot 75m\Omega\right)\right)} \approx \mathbf{1,86}$

As in real life, quality makes the difference!

TRANSFER FUNCTION OF THE PLANT

Bode plot – calculation and measurement (model accuracy)

- The model accuracy depends heavily on the parasitics included
  - Red: Simplified transfer function (Laplace transform) from the slide before
  - Yellow: Transfer function (Laplace transform) including the damping effect and the natural frequency shift of the double pole due the ESR and DCR (inductor)
  - Grey: Measurement of the plant transfer function using RTA4000 Oscilloscope.
  - ➢ The quality is strongly influenced by the parasitic resistances simulated
  - ➢ If you start from the simplification, you get an overcompensated control loop
  - ➢ The ESL has an effect at higher frequencies

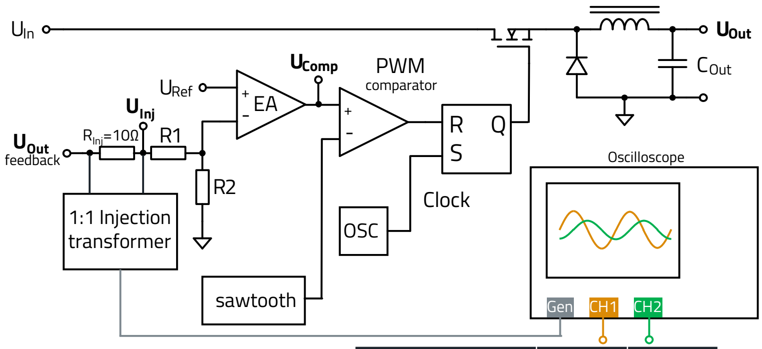


G_P (s)

TRANSFER FUNCTION OF THE PLANT

Frequency response measurement - Bode plot

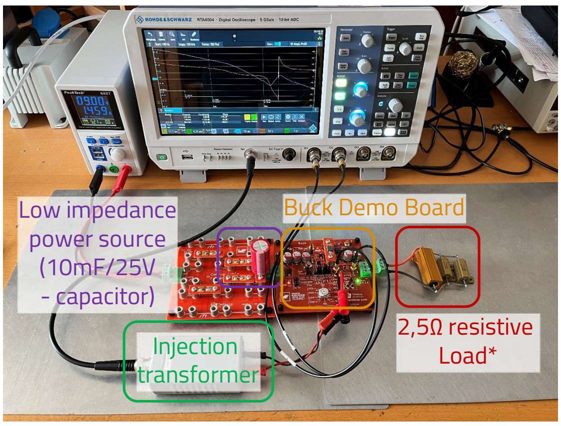
- A small injection resistor is inserted into the feedback voltage divider
  - The injection resistance is small compared to the series resistance of R1 (4,32kΩ) and R2 (825Ω)
  - The test signal (sinusoidal frequency sweep) is fed in via the injection resistor with an injection transformer
- The oscilloscope plots the gain and the phase by measuring the signal input/output ratio at each test frequency
  - Depending on which input/output ratio is evaluated, the plant, compensator or open loop transfer function can be determined

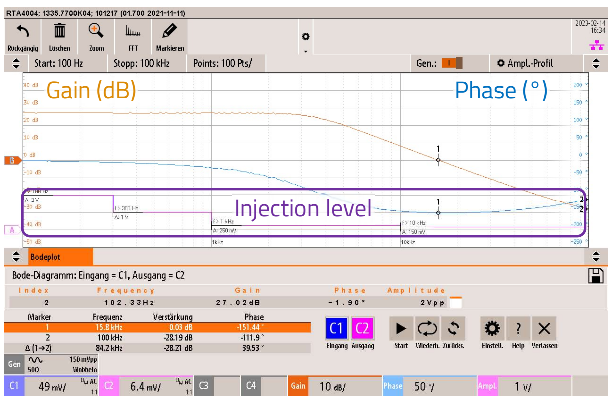


Transfer function		Input - CH1	Output - CH2
Plant	$G_P(s)$	U_{Comp}	U_{Out}
Compensator	$G_C(s)$	U_{Inj}	U_{Comp}
Open loop	$G_{OL}(s)$	U_{Inj}	U_{Out}

TRANSFER FUNCTION OF THE PLANT

Frequency response measurement – Bode plot with RTA4004-K36 (Rohde&Schwarz)





Test setup

*An resistive load is mandatory for frequency response analysis because a controlled electronic load affects the measurement

Measurement

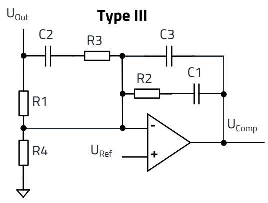
*The injection level must be chosen carefully:
Too big: wrong result
(not the small signal behaviour)
Too small: bad SNR (noisy)

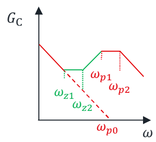
COMPENSATOR DESIGN

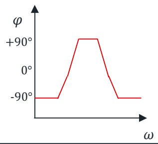
COMPENSATOR DESIGN

Type III - Compensator

- 1 pole of origin (integrator)
  - High gain at low frequencies
    - ➢ Small static error
- 2 poles & 2 zeros
- Gain and phase at crossover frequency can be affected
- Phase boost up to 180°
  - ➢ Due 2 zeros
  - ➢ Suitable for voltage mode
- Commonly used for voltage mode







- $G_C = (-)\,\frac{\omega_{P0}}{s} \cdot \frac{\left(1+\frac{s}{\omega_{Z1}}\right)\cdot\left(1+\frac{s}{\omega_{Z2}}\right)}{\left(1+\frac{s}{\omega_{P1}}\right)\cdot\left(1+\frac{s}{\omega_{P2}}\right)}$

- **Type III:**
  - ➢ $\omega_{Z1} = \frac{1}{R2 \cdot C1}$
  - ➢ $\omega_{Z2} = \frac{1}{C2 \cdot (R1 + R3)}$
  - ➢ $\omega_{P0} = \frac{1}{R1 \cdot (C1 + C3)}$
  - ➢ $\omega_{P1} = \frac{(C1 + C3)}{R2 \cdot C1 \cdot C3}$
  - ➢ $\omega_{P2} = \frac{1}{R3 \cdot C2}$

STABILITY INTERACTIONS OF DC/DC-CONVERTERS

- Type I compensation is stable but with small bandwidth (slow time response) due to falling gain profile.
- Type II compensation extend bandwidth (keep gain) with a little phase margin add-on.
- Type III compensation extend bandwidth with high gain (better time response) also with a high phase margin (good stability)

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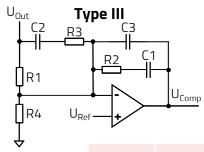
COMPENSATOR DESIGN

Type III - Compensator - Design example*

*Based on the plant transfer function of the Buck Demo Board



	Comp A	Comp B	Comp B+C
R1	4.33E+03	4.33E+03	4.33E+03
R2	1.00E+04	2.55E+03	2.55E+03
R3	8.20E+01	8.20E+01	8.20E+01
C1	4.70E-09	1.00E-08	1.00E-08
C2	4.70E-09	4.70E-09	9.40E-09
C3	3.30E-09	1.50E-09	1.50E-09

- Compensator A (R1=4,33kΩ; R2=10kΩ; R3=82Ω; C1=4,7nF; C2=4,7nF; C3=3.3nF)
- Compensator B (R1=4,33kΩ; R2=2.55kΩ; R3=82Ω; C1=10nF; C2=4,7nF; C3=1.5nF)*
- Compensator B + C (R1=4,33kΩ; R2=2.55kΩ; R3=82Ω; C1=10nF; C2=9,4nF; C3=1.5nF)

	Comp A	Comp B	Comp B+C
fz1	3387.99	6244.54	6244.54
fz2	7679.04	7679.04	3839.52
fp0	4596.87	3197.82	3197.82
fp1	8213.32	47874.78	47874.78
fp2	413169.87	413169.87	206584.94

- Different locations for poles and zeros result in different open loop characteristics.
- Optimized performance going from compensator A -> B -> B+C.

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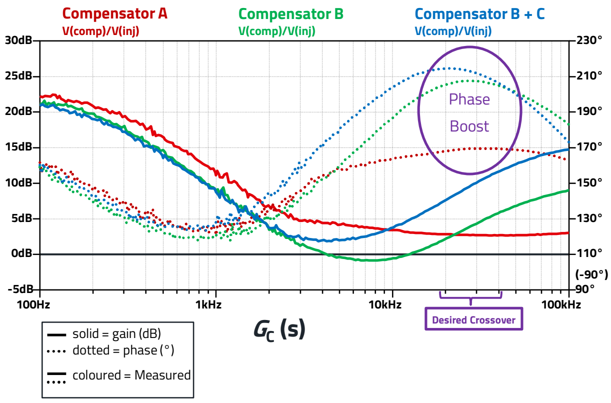
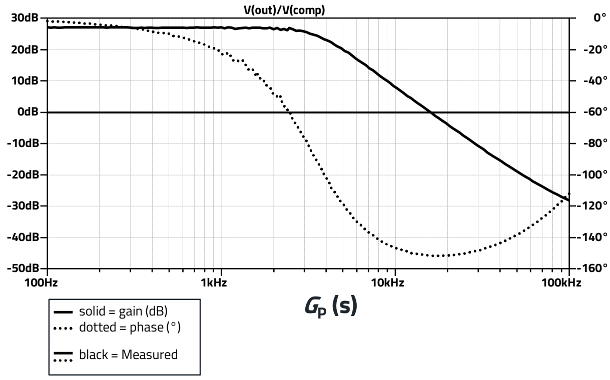
STABILITY THROUGH THE COMPENSATOR - BUCK DEMO BOARD

Compensator and plant





Bode plot – Compensator X

Bode plot – Plant: I_{Out}=2A / U_{In}=19V

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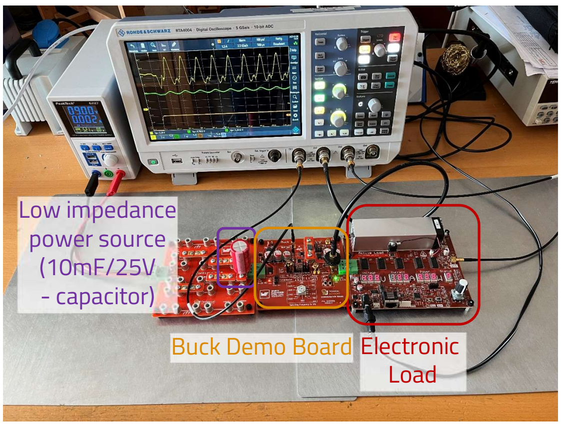
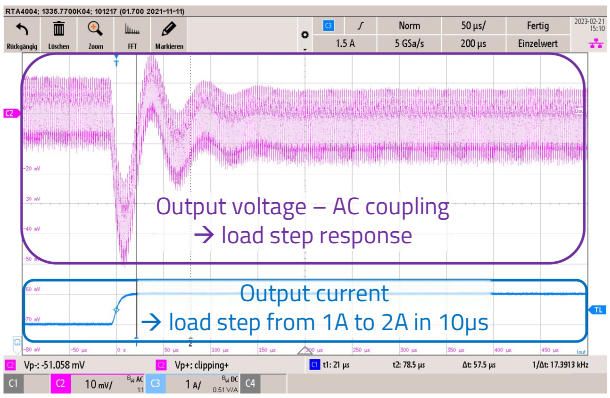
STABILITY THROUGH THE COMPENSATOR - BUCK DEMO BOARD

Load step response - Test setup





Test setup

Measurement

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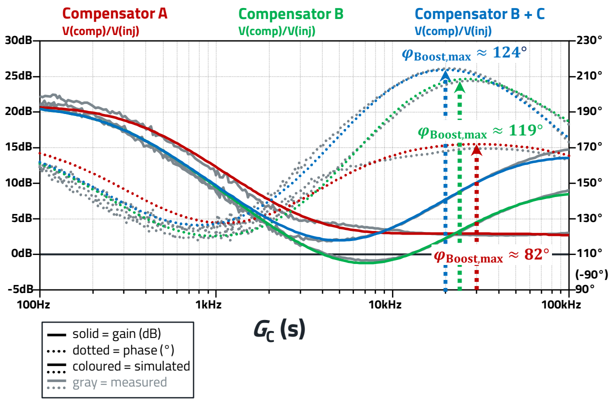
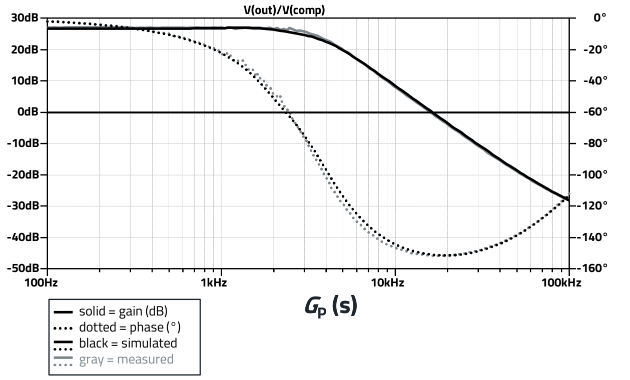
STABILITY THROUGH THE COMPENSATOR - BUCK DEMO BOARD

Compensator and plant



Bode plot – Compensator X



Bode plot – Plant: I_{Out}=2A / U_{In}=19V

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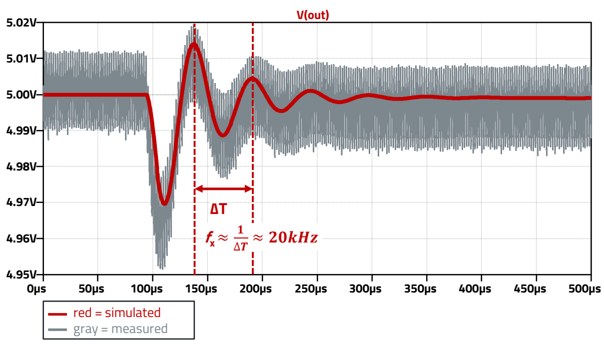
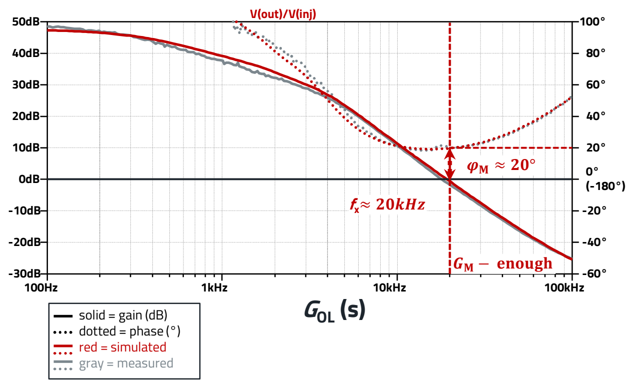
STABILITY THROUGH THE COMPENSATOR - BUCK DEMO BOARD

Compensator A (R1=4,33kΩ; R2=10kΩ; R3=82Ω; C1=4,7nF; C2=4,7nF; C3=3.3nF)



Load step response: I_{Out} 1A → 2A / U_{In}=19V



Bode plot - Open loop: I_{Out}=2A / U_{In}=19V

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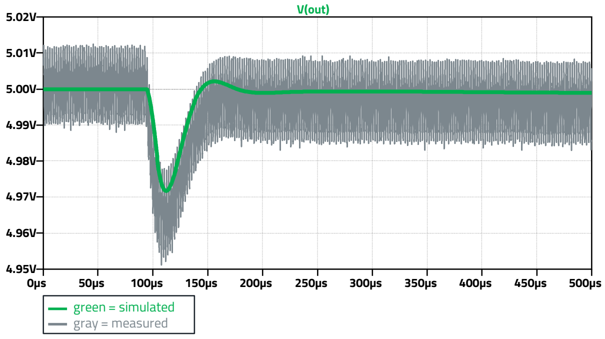
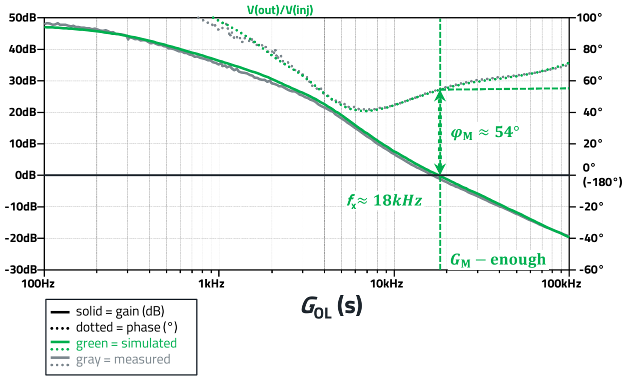
STABILITY THROUGH THE COMPENSATOR - BUCK DEMO BOARD

Compensator B (R1=4,33kΩ; R2=2.55kΩ; R3=82Ω; C1=10nF; C2=4,7nF; C3=1.5nF)*

*Design analyzed before





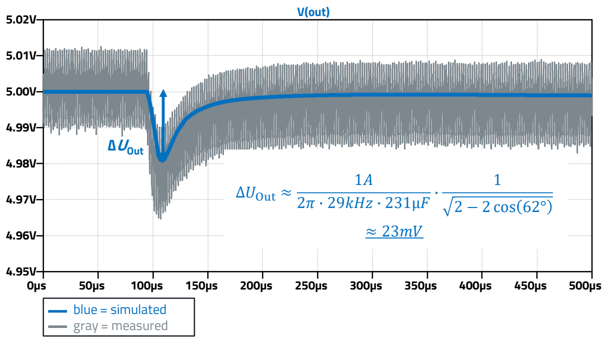
Load step response: I_{Out} 1A → 2A / U_{In}=19V

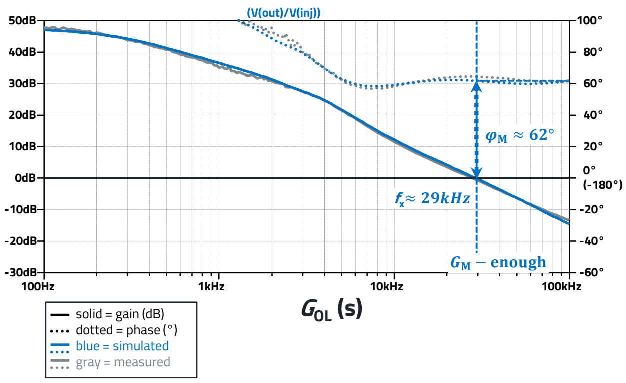
Bode plot - Open loop: I_{Out}=2A / U_{In}=19V

ANALOG DEVICES

STABILITY THROUGH THE COMPENSATOR - BUCK DEMO BOARD

Compensator B + C (R1=4,33kΩ; R2=2.55kΩ; R3=82Ω; C1=10nF; C2=9,4nF; C3=1.5nF)





Load step response: I_{Out} 1A → 2A / U_{In}=19V

Bode plot - Open loop: I_{Out}=2A / U_{In}=19V

ANALOG DEVICES

STABILITY THROUGH THE COMPENSATOR - BUCK DEMO BOARD

Demo: Load step response

- 1 to 2Amps step
  - Comp Type3 (Jump A)

CH2 : $V_{out}\ AC$
CH3 : $I_L\ Ac$ through transformer
CH4 : $I_{out}DC$
MATH : $I_L\ Total\ (AC + DC)$

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STABILITY THROUGH THE COMPENSATOR - BUCK DEMO BOARD

Demo: Load step response

- 1 to 2Amps step
  - Comp Type3 (Jump B+C)

CH2 : $V_{out}\ AC$
CH3 : $I_L\ Ac$ through transformer
CH4 : $I_{out}DC$
MATH : $I_L\ Total\ (AC + DC)$

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BASICS OF CONTROL THEORY

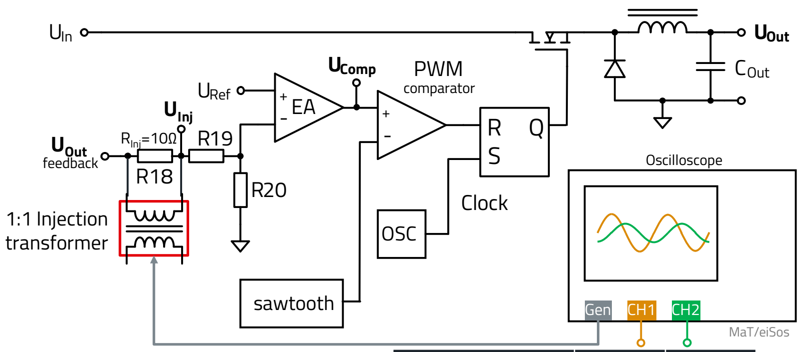
Closed loop transfer function - conclusions

- $U_{\mathrm{Out}}(s) = U_{\mathrm{Ref}}(s) \cdot \frac{G_{\mathrm{OL}}(s)}{1+G_{\mathrm{OL}}(s)}$ [$G_{\mathrm{OL}}(0) \rightarrow \infty$] ⇒ $U_{\mathrm{Out}} \approx U_{\mathrm{Ref}}$ → No static error
- $U_{\mathrm{Out}}(s) = U_{\mathrm{Ref}}(s) \cdot \frac{G_{\mathrm{OL}}(s)}{1+G_{\mathrm{OL}}(s)}$ [$G_{\mathrm{OL}}(s) \rightarrow -1$] ⇒ $U_{\mathrm{Out}} \neq U_{\mathrm{Ref}}$ → Instability → Nyquist stability criterion!
- **Task of the Error amplifier:**
  - high amplification for small frequencies (we need an integrator in the loop = pole at origin)
  - keep the open loop transfer function away from -1 !

LOOP COMPENSATION

Control Loop on real world

- Buck board
  - Use of all caps but Polymer (better sine response)
- Measure FRA : „Open Loop behavior" G_{OL} Generator
- $G_{OL}(s) = \frac{V\_out}{V_{inj}}$
  - $U_{Inj} = 250mVpp$
  - $U_{out}\ (AC)$

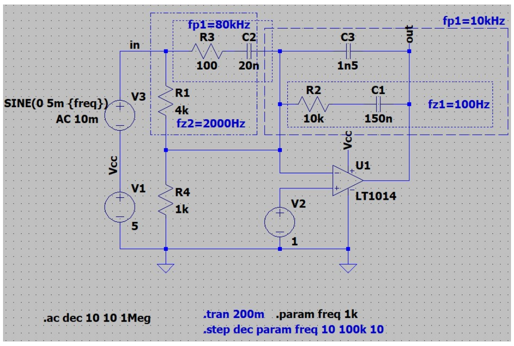


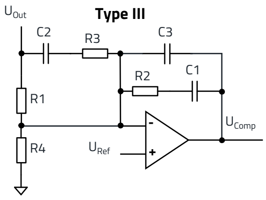
Transfer function		Input - CH1	Output - CH2
Plant	$G_P(s)$	U_{Comp}	U_{Out}
Compensator	$G_C(s)$	U_{Inj}	U_{Comp}
Open loop	$G_{OL}(s)$	U_{Inj}	U_{Out}

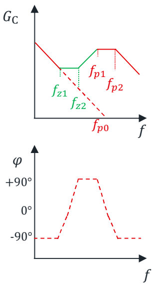
LOOP COMPENSATION

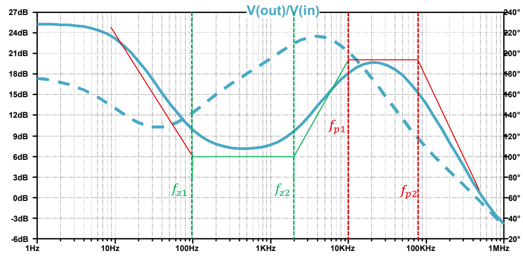
POWER : Compensation Type 3, simulation results

- $G_0 = \frac{R2}{R1 \therefore R3} = 100 \approx +40dB$
- ✓ $f_{z1} = \frac{1}{2\pi\ (R2 \cdot C1)} = \frac{1}{2\pi{\cdot}10k{\cdot}150n} = 100Hz$
- ✓ $f_{Z2} = \frac{1}{2\pi{\cdot}C2\ (R1\ \ \ R3)} = \frac{1}{2\pi{\cdot}20n{\cdot}(4k+10\ )} = 2kHz$
- ✓ $f_{P1} = \frac{C1+C3}{2\pi{\cdot}R2 \cdot C1{\cdot}C3} = \frac{150n+1n5}{2\pi{\cdot}10k{\cdot}150n{\cdot}1n5} = \frac{151{,}5^{-9}}{14{,}13^{-12}} = 10{,}7kHz$
- ✓ $f_{P2} = \frac{1}{2\pi{\cdot}R\ \ {\cdot}C2} = \frac{1}{2\pi{\cdot}10\ \ {*}20n} = \frac{1}{12{,}56^{-6}} \approx 80kHz$





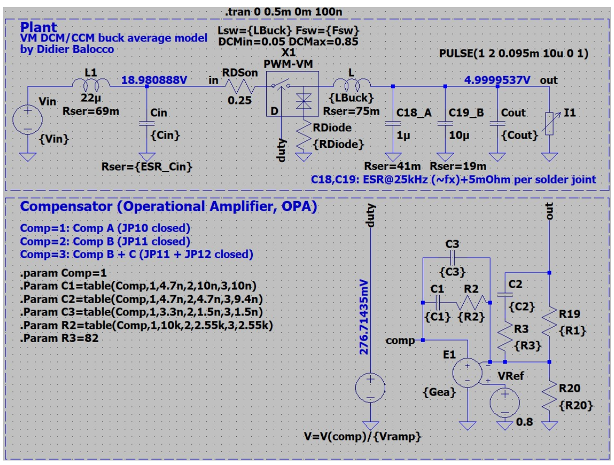




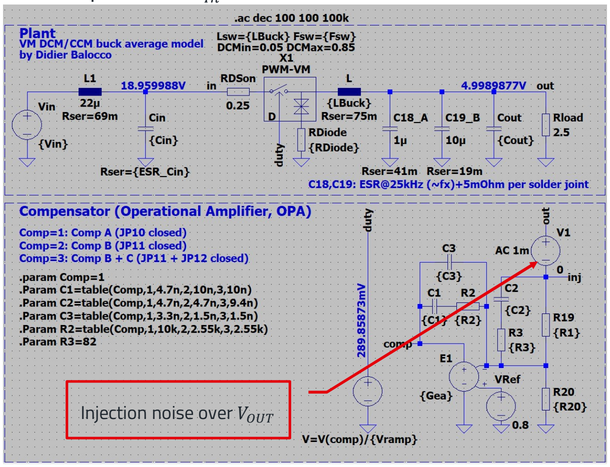
ANALOG DEVICES

STABILITY THROUGH THE OUTPUT CAPACITOR

Compensator A and output capacitor A + B + C : simulations and comparisons; $U_{In} = 19V$



DC Simulation(Transient Time Domain)



AC Simulation(Frequency Domain)

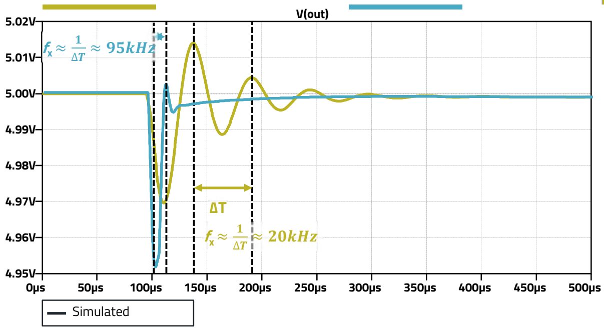
ANALOG DEVICES

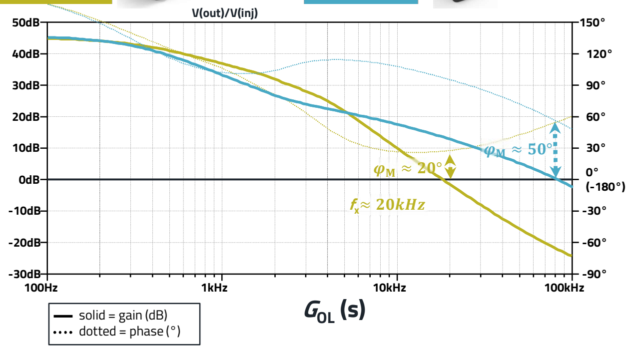
STABILITY THROUGH THE OUTPUT CAPACITOR

Compensator A and output capacitor A + B + C : simulations and comparisons

865080257014
WCAP-ASLI
Aluminium
1000µF 10V

875075561008
WCAP-PSLC
Polymer
220µF 25V





Load step response: $I_{Out}\ 1A \rightarrow 2A; U_{In} = 19V$

Bode plot - Open loop: $I_{Out} = 2A\ ; U_{In} = 19V$

ANALOG DEVICES

REDEXPERT

STABILITY THROUGH THE OUTPUT CAPACITOR

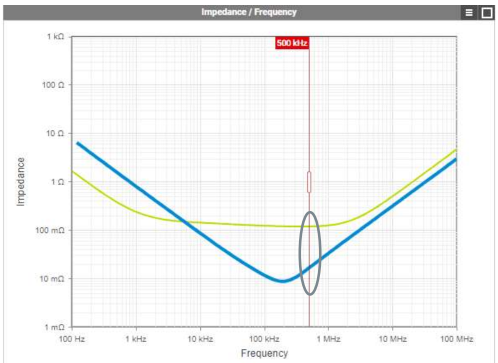
RedExpert comparison

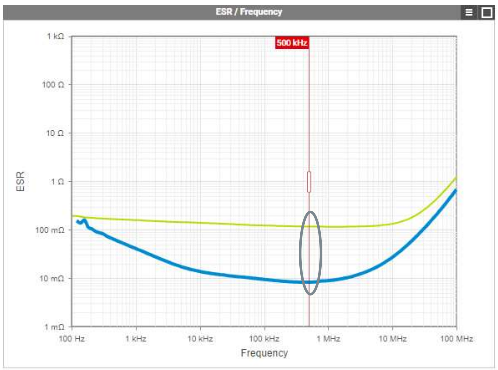
- 1000µF Aluminum Vs 220µF Polymer
  - 5x Less value but… : 10x better in ESR !

865080257014
WCAP-ASLI
Aluminium
1000µF 10V

875075561008
WCAP-PSLC
Polymer
220µF 25V

Order Code	Series	Spec		Technology	Series Description	C	To...	V_R	DF	Z@500 kHz	ESR @500 kHz	I@20°C @1 k...	Specified Max. I_{Ripple}	I_{leak}	T_{min}	T_{max}	Lifetime	Asse...
875075561008	WCAP-PSLC			Alum. Polymer	SMT - Large Capacitance	220 µF	±20%	25.0 V	< 10 %	16.4 mΩ	8.24 mΩ	1.44 A	4.80 A @100 kHz @105°C	1.10 mA	-55°C	105°C	2000.0 h	SMT
865080257014	WCAP-ASLI			Alum. Electrolytic	SMT - Low Impedance +105°C	1.00 mF	±20%	10.0 V	< 19 %	118 mΩ	116 mΩ	659 mA	740 mA @100 kHz @105°C	100 µA	-55°C	105°C	2000.0 h	SMT





ANALOG DEVICES

DEMO

LUNCH

Bon appétit !

LTSPICE EXAMPLES

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TECHNICAL ACADEMY

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SMART SELECTION OF INDUCTORS AND CAPACITORS

ANALOG DEVICES

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INDUCTOR THEORY

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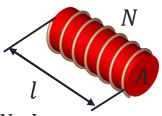
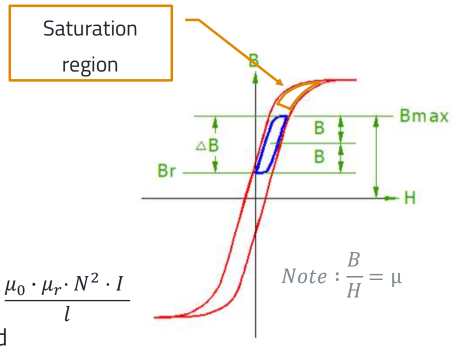
POWER INDUCTORS

Inductors : theory of operation



- Maths behind physics
  - Inductor current I make some excitation H $H = \frac{N \cdot I}{l}$
  - Physical construction make flux induction B $B = \mu_0 \cdot \mu_r \cdot H$



- Physical limits
  - Inductor magnetic field B is limited by core material properties
  - Math translation is less and less µr form the material

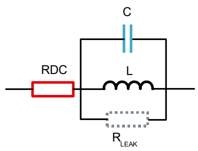
Only physical change related into the equation! $L = \frac{\mu_0 \cdot \mu_r \cdot N^2 \cdot I}{l}$

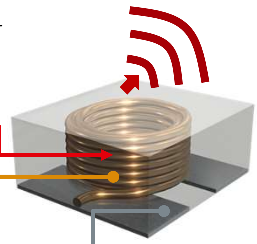
Into saturation region current increase lead to less and less magnetic field

Energy storage start to be **inefficient**

INDUCTORS

Theory : Inductor and parasitic

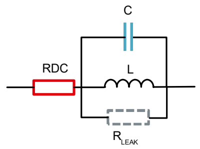




- DC Losses:
  - copper losses with average DC current through the component
    - estimation of DC loss is straight forward: $P_{dc} = R_{dc} \cdot I_{RMS}^2$
- AC Losses:
  - winding losses due to skin effect, proximity effect, etc.
  - core losses : eddy current & hysteresis loss in the core due to magnetization
    - Related to (f, B, H)
- EMI losses from leakages and parasitic couplings
- Total Losses:
  - $P_{tot} = P_{dc} + P_{ac}$

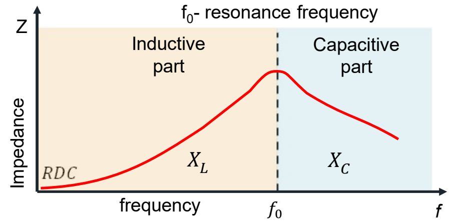
INDUCTOR : IMPEDANCE Z

Well known behavior ?!



- $Z = \sqrt{RDC^2 + \left(\frac{X_L}{1-\frac{X_L}{X_C}}\right)^2}$
- $Z = \sqrt{RDC^2 + \left(\frac{L\cdot\omega}{1-L\cdot C\cdot\omega^2}\right)^2}$ $\qquad \omega = 2\cdot\pi\cdot f$
- $f_0 = \frac{1}{2*\pi*\sqrt{L*C}}$

Note: R_{DC} is resistance for $f = 0Hz$



- Component itself act as a filter

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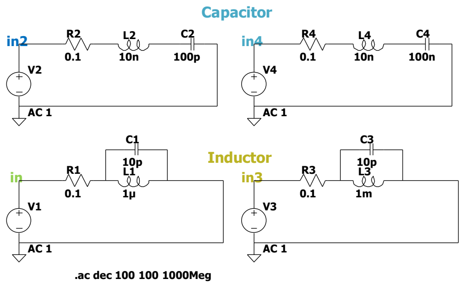
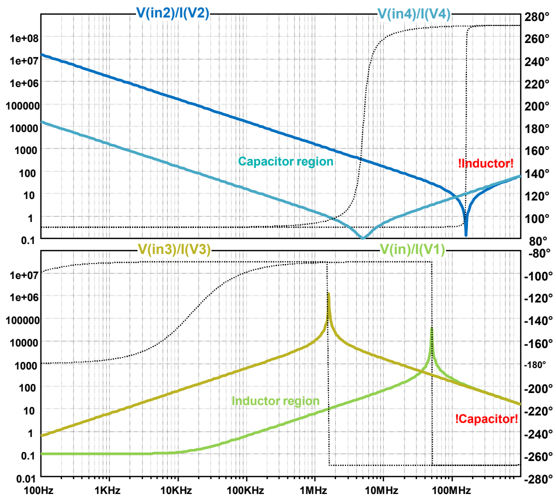
REAL CAPACITOR AND INDUCTOR BEHAVIOR



$Z = \sqrt{RDC^2 + \left(L\cdot\omega\cdot\frac{1}{1-L\cdot C\cdot\omega^2}\right)^2}$ $\quad Z = \sqrt{ESR^2 + \left(ESL\cdot\omega - \frac{1}{C\cdot\omega}\right)^2}$

$|Z_L| \approx L\cdot\omega$, R=0,C=0 $\qquad |Z_C| \approx \frac{1}{C\cdot\omega}, ESR = 0, ESL = 0$



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POWER INDUCTOR SELECTION

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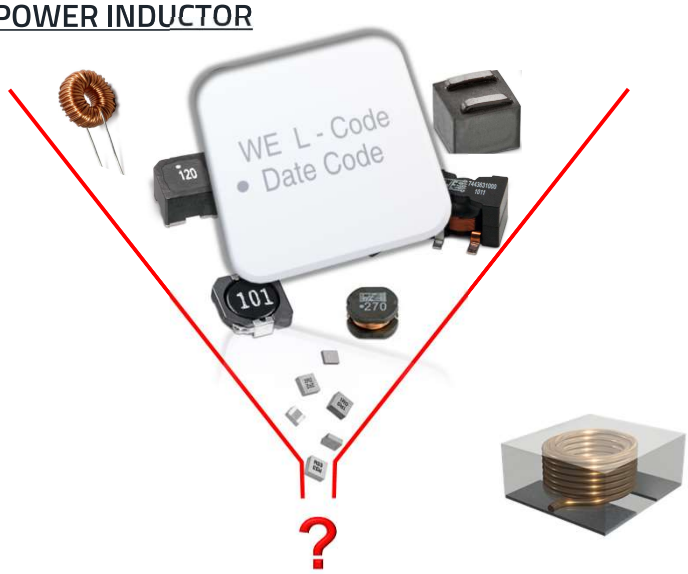
HOW TO CHOOSE A POWER INDUCTOR

Key parameters



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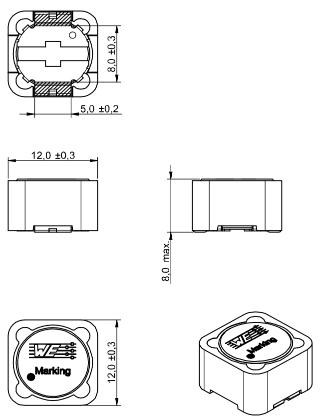
SMART SELECTION OF INDUCTORS

Key parameters and use

- Requirements for customer
  - Value
    - Behavior & tolerances
  - Currents
  - DC resistance (DC losses)
  - AC losses ??
    - **RED EXPERT !**
  - System voltage
  - Temperature limits and behavior
    - **RED EXPERT !**
  - Mechanical aspects
  - Qualifications and standards

- Product parameters: datasheet

Dimensions: [mm]



Electrical Properties:

Properties		Test conditions	Value	Unit	Tol.
Inductance	L	100 kHz/ 250 mV	10	µH	±20%
Rated Current	$I_{R,40K}$	ΔT = 40 K	7	A	max.
Performance Rated Current [1)]	$I_{RP,40K}$	ΔT = 40 K	8.2	A	max.
Saturation Current @ 10%	$I_{SAT,10\%}$	|ΔL/L| < 10 %	7.5	A	typ.
Saturation Current @ 30%	$I_{SAT,30\%}$	|ΔL/L| < 30 %	9.7	A	typ.
DC Resistance	R_{DC}	@ 20 °C	15	mΩ	typ.
DC Resistance	R_{DC}	@ 20 °C	20	mΩ	max.
Self Resonant Frequency	f_{res}		18	MHz	typ.
Operating Voltage	V	DC	120	V	max.

1) refer to IEC 62024-2-2020

Certification:

RoHS Approval	Compliant [2011/65/EU&2015/863]
REACh Approval	Conform or declared [(EC)1907/2006]
Halogen Free	Conform [JEDEC JS709B]
Component Qualification	AEC-Q200 Grade 1
Automotive Approval	Released

General Information:

Ambient Temperature (referring to I_{RP})	-40 °C up to +85 °C
Operating Temperature	-40 °C up to +125 °C
Storage Conditions (in original packaging)	< 40 °C ; < 75 % RH
Moisture Sensitivity Level (MSL)	1
Test conditions of Electrical Properties: +20 °C, 33 %RH if not specified differently	
Test conditions of Performance Rated Current: refer to IEC 62024-2-2020, Class B (PCB Copper Width: 40 mm; PCB Copper Thickness: 35 µm)	

ANALOG DEVICES

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INDUCTOR SELECTION

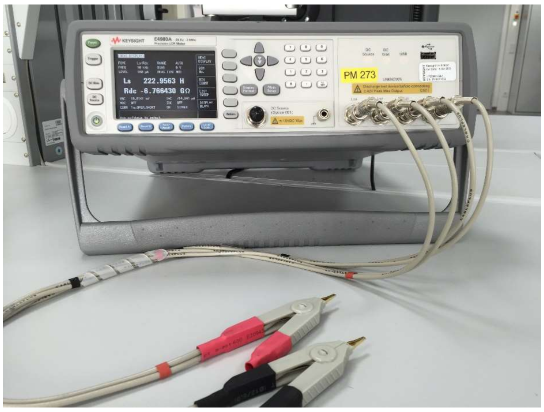
Inductance value production and quality measurement

- Inductance is measured with LCR meter
  - With a specific set up

- Samples can be ordered with the nearest standard values

Electrical Properties:

Properties	Test conditions		Value	Unit	Tol.
Inductance	1 kHz/ 250 mV	L	10	µH	±20%
Rated current	ΔT = 40 K	I_R	7.1	A	max.
Saturation current	|ΔL/L| < 10%	I_{sat}	10.5	A	typ.
DC Resistance	@ 20°C	R_{DC}	0.013	Ω	typ.
DC Resistance	@ 20°C	R_{DC}	0.021	Ω	max.
Self resonant frequency		f_{res}	21	MHz	typ.



ANALOG DEVICES

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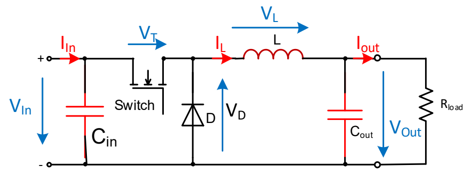
INDUCTOR SELECTION

Inductance value : the buck converter example



$$D = \frac{V_{out}}{V_{in}} \qquad D = \frac{V_{out} + Vd}{V_{in} - Vsw + Vd}$$

$D = 0{,}208$ $\qquad$ $D = 0{,}22$

$$L = \frac{(V_{in} - Vout) \cdot D}{f_{switch} \cdot r \cdot I_{out}}$$

$$I_{peak} = Iout + \frac{\Delta I}{2}$$

$$I_{nom} = Iout$$

- $V_{in} = 24V$
- $V_{out} = 5V$
- $I_{out} = 2A$
- $F_{sw} = 535\ kHz$
- $V_{sw} = 0{,}3V$
- $V_D = 0{,}3V$

$r = 20\%$

I_{peak} =2,2A

$L = 18{,}5\mu H \ - 19{,}4\mu H$

$r = 40\%$

I_{peak} =2,4A

$L = 9{,}3\mu H \ - 9{,}7\mu H$

Standard value : 8,2µH; 10µH, 12µH, 15µH, 18µH, 22µH

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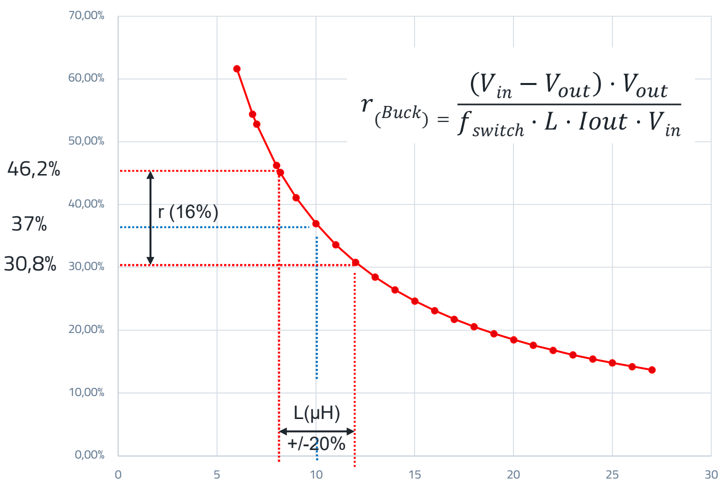
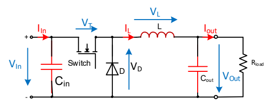
INDUCTOR SELECTION

Ripple VS Inductance value :



$$r_{(Buck)} = \frac{(V_{in} - V_{out}) \cdot V_{out}}{f_{switch} \cdot L \cdot Iout \cdot V_{in}}$$



- $V_{in} = 24V$
- $V_{out} = 5V$
- $I_{out} = 2A$
- $F_{sw} = 535\ kHz$
- $V_{sw} = 0{,}3V$
- $V_D = 0{,}3V$

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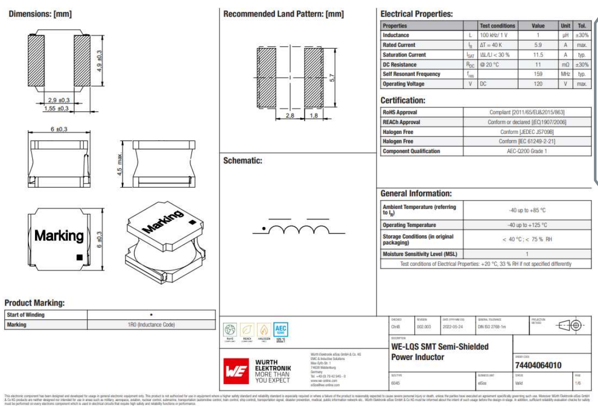
RATED CURRENT

RATED CURRENT

Heating shown in the Datasheet

- Datasheet sample



- Rated current mention in the datasheet

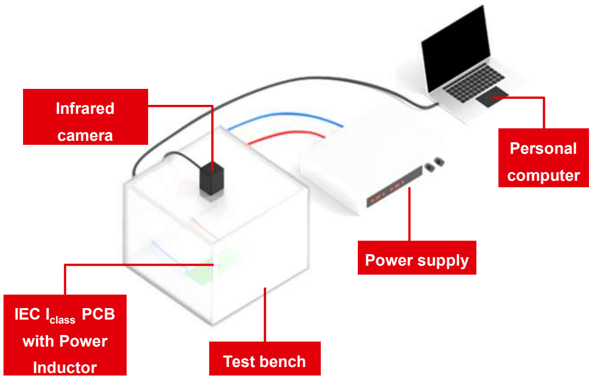
Electrical Properties:

Properties		Test conditions	Value	Unit	Tol.
Inductance	L	100 kHz/ 1 V	1	µH	±30%
Rated Current	I_R	ΔT =	5.9	A	max.
Saturation Current	I_{SAT}	|ΔL/L| < 30 %	11.5	A	typ.
DC Resistance	R_{DC}	@ 20 °C	11	mΩ	±30%
Self Resonant Frequency	f_{res}		159	MHz	typ.
Operating Voltage	V	DC	120	V	max.

RATED CURRENT

Explained setup

- This value describes the direct current at which the component self heating increases (ΔT)
- The method Würth Elektronik uses to measure the rated current is based upon section 6 of the IEC 62024-2:2020 standard to provide transparent and comparable Ir values. A test PCB with a Power Inductor is contained within a box of roughly 20 cm on each side and does not contact directly with the surrounding box. Only natural heat exchange occurs, with no forced heat transfer applied to the test PCB.
- Overall setup



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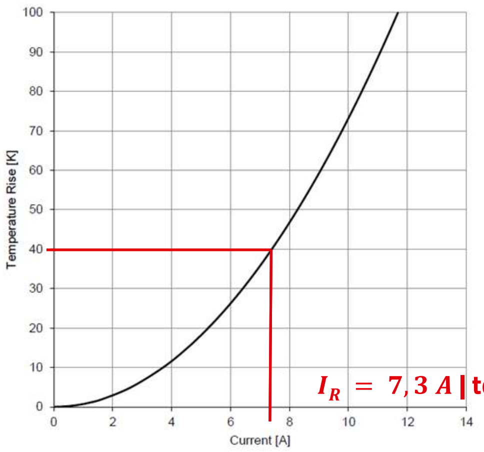
RATED CURRRENT

Definition with temperature rise

- Temperature rise vs Current



$I_R = 7,3\ A$ | test condition ΔT = 40K

- Losses vs current
  - DC current injection is more convenient and very accurate to define losses and temperature rise accordingly

$$P_{loss} = R_{DC} \cdot {I_{DC}}^2$$

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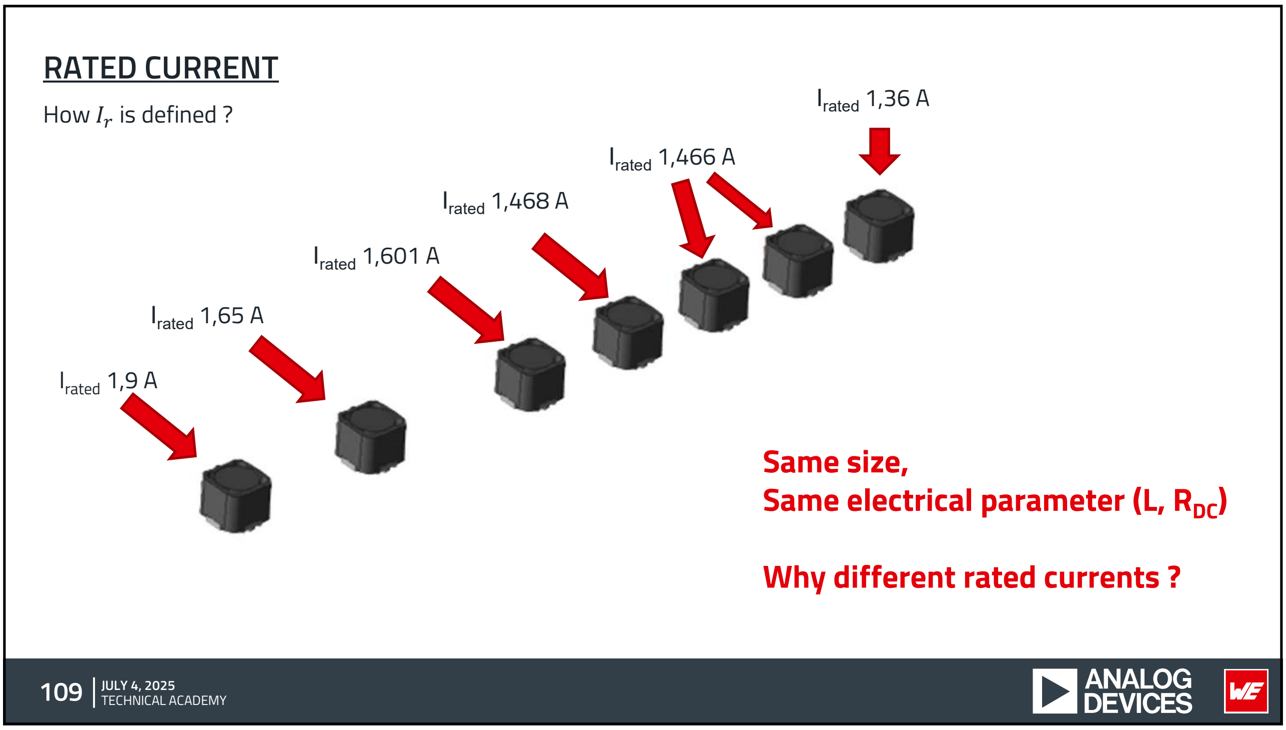
RATED CURRENT
How I_r is defined ?
I_{rated} 1,9 A
I_{rated} 1,65 A
I_{rated} 1,601 A
I_{rated} 1,468 A
I_{rated} 1,466 A
I_{rated} 1,36 A
Same size,
Same electrical parameter (L, R_{DC})
Why different rated currents ?
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ANALOG DEVICES

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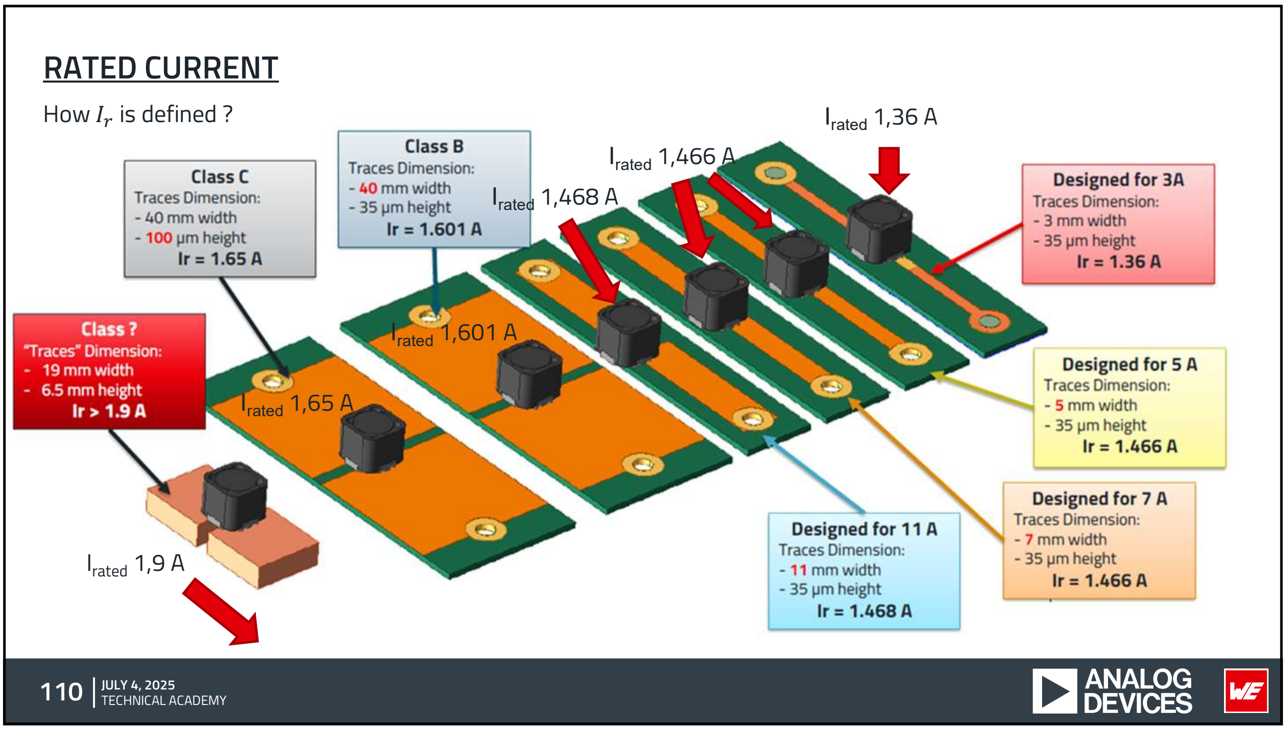
RATED CURRENT
How I_r is defined ?
Class C
Traces Dimension:
- 40 mm width
- 100 µm height
Ir = 1.65 A
Class B
Traces Dimension:
- 40 mm width
- 35 µm height
Ir = 1.601 A
Class ?
"Traces" Dimension:
- 19 mm width
- 6.5 mm height
Ir > 1.9 A
I_{rated} 1,36 A
I_{rated} 1,466 A
I_{rated} 1,468 A
I_{rated} 1,601 A
I_{rated} 1,65 A
I_{rated} 1,9 A
Designed for 3A
Traces Dimension:
- 3 mm width
- 35 µm height
Ir = 1.36 A
Designed for 5 A
Traces Dimension:
- 5 mm width
- 35 µm height
Ir = 1.466 A
Designed for 7 A
Traces Dimension:
- 7 mm width
- 35 µm height
Ir = 1.466 A
Designed for 11 A
Traces Dimension:
- 11 mm width
- 35 µm height
Ir = 1.468 A
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ANALOG DEVICES

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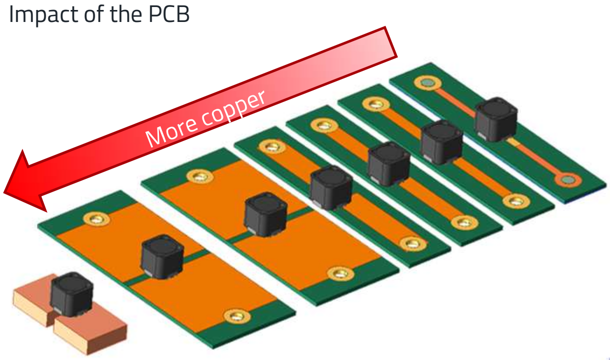
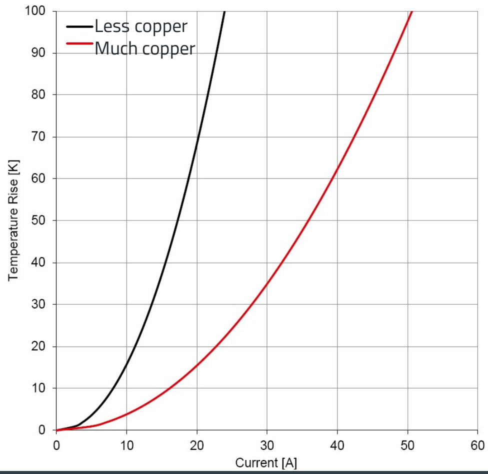
RATED CURRENT

Impact of the PCB





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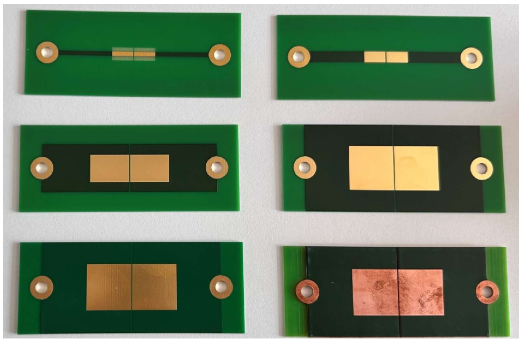
IEC 62024-2:2020

WE Definition and uses of Rated current

- Class B: Product Series with standard requirement profile
- Class C: Product which are used in high packing density application
- Class D: Products with current capability higher then 30A



PCB for Demo
PN 999 900 96

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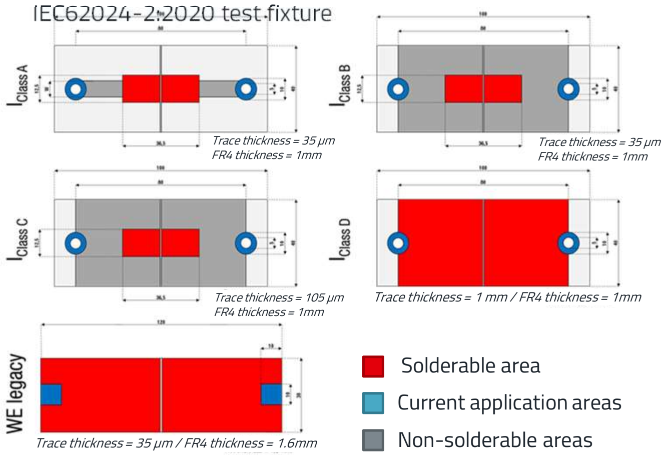
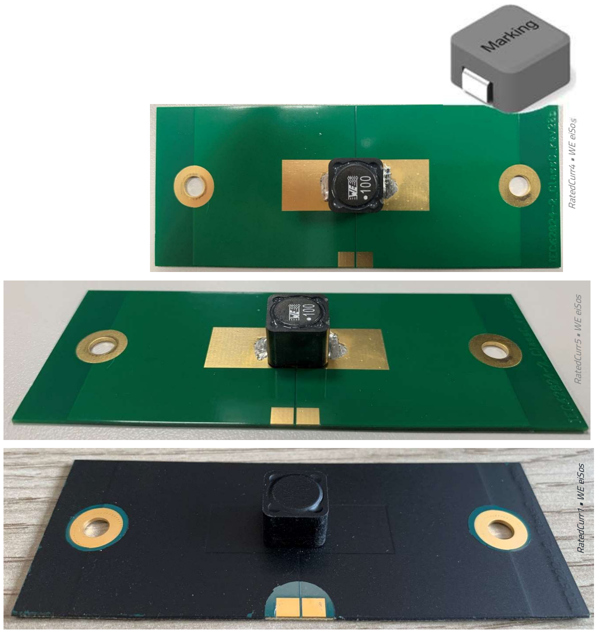
POWER INDUCTORS

IEC62024-2:2020 test fixture



- Solderable area
- Current application areas
- Non-solderable areas
- FR4 areas



ANALOG DEVICES

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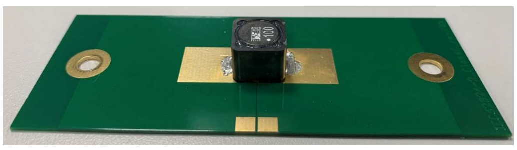
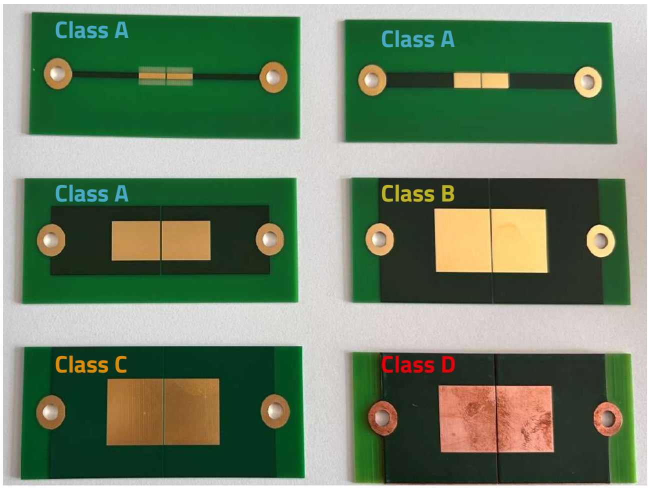
IEC 62024-2:2020

WE Definition and uses of Rated current

- **Class A**: 1 to 22mm pattern width
- **Class B**: Product Series with standard requirement profile
- **Class C**: Product which are used in high packing density application
- **Class D**: Products with current capability higher then 30A





ANALOG DEVICES

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POWER INDUCTORS

Wurth Elektronik current definition ; the truth about it

Redefining Rated Current Measurements for Power Inductors

- The rated current is related from temperature elevation
  - 40K is a "standard" common value often the difference between component temperature and ambient temperature.
  - 40K is also the maximum temperature rise of the **IEC62024-2:2020 standard**; practical to evaluate maximum performances.
    §6.4.3 i) into standard page 15
-

Table 2 – Circuit pattern width and thickness

Rated current class	Pattern width W mm	Pattern thickness t µm	Example application
$I_{class\ A}$	(1,0 to 22,0) ± 0,2 to 0,5	35 ± 10	Consumer application (single-sided printed circuit boards application)
$I_{class\ B}$	40 ± 0,2	35 ± 10	Consumer application (double-sided printed circuit boards application)
$I_{class\ C}$	40 ± 0,2	105 ± 10	Consumer application (multilayer printed circuit boards application)
$I_{class\ D}$	40 ± 0,2	1000 ± 50	Automotive or large current power line application

NOTE 1 $I_{class\ A}$: see Figure 2a).

NOTE 2 $I_{class\ B}$, $I_{class\ C}$, $I_{class\ D}$: see Figure 2b).

Electrical Properties:

Properties		Test conditions	Value	Unit	Tol.
Inductance	L	100 kHz/ 10 mA	1	µH	±20%
Rated Current	$I_{R,40K}$	ΔT = 40 K	15	A	max.
Performance Rated Current [1)]	$I_{RP,40K}$	ΔT = 40 K	23.5	A	max.
Saturation Current @ 10%	$I_{SAT,10\%}$	|ΔL/L| < 10 %	15.4	A	typ.
Saturation Current @ 30%	$I_{SAT,30\%}$	|ΔL/L| < 30 %	38	A	typ.
DC Resistance	R_{DC}	@ 20 °C	2.7	mΩ	typ.
DC Resistance	R_{DC}	@ 20 °C	3.5	mΩ	max.
Self Resonant Frequency	f_{res}		41	MHz	typ.

[1)] refer to IEC 62024-2-2020

General Properties:

Ambient Temperature (referring to I_R)	-40 up to +85 °C
Operating Temperature	-40 up to +125 °C
Storage Conditions (in original packaging)	< 40 °C ; < 75 % RH
Moisture Sensitivity Level (MSL)	1
Test conditions of Electrical Properties: +20 °C, 33 % RH if not specified differently	
Test conditions of Performance Rated Current: refer to IEC 62024-2, Class C (PCB Copper Width: 40 mm; PCB Copper Thickness: 105 µm)	
Temperature rise is highly dependent on many factors including PCB land pattern, trace size, and proximity to other components. Therefore, temperature rise should be verified in application conditions.	

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EXAMPLE CLASS C

7447707033 [1280] size code

- WE-PD **P**erformance variant

Electrical Properties:

Properties		Test conditions	Value	Unit	Tol.
Inductance	L	100 kHz/ 5 mA	3.3	µH	±30%
Rated Current	$I_{R,40K}$	ΔT = 40 K	9.4	A	max.
Performance Rated Current [1)]	$I_{RP,40K}$	ΔT = 40 K	12.8	A	max.
Saturation Current @ 10%	$I_{SAT,\ 10\%}$	|ΔL/L| < 10 %	17.5	A	typ.
Saturation Current @ 30%	$I_{SAT,30\%}$	|ΔL/L| < 30 %	17.5	A	typ.
DC Resistance	R_{DC}	@ 20 °C	9	mΩ	max.
Self Resonant Frequency	f_{res}		32.3	MHz	typ.
Operating Voltage	V	DC	120	V	max.

[1)] refer to IEC 62024-2-2020

Test conditions of Performance Rated Current: refer to IEC 62024-2-2020 Class C PCB Copper Width: 40 mm; PCB Copper Thickness: 105 µm)

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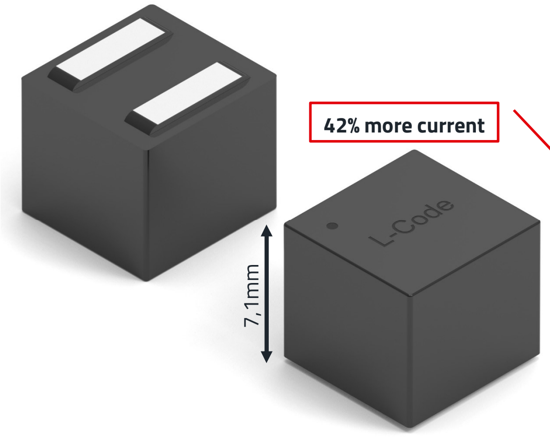
EXAMPLE CLASS C

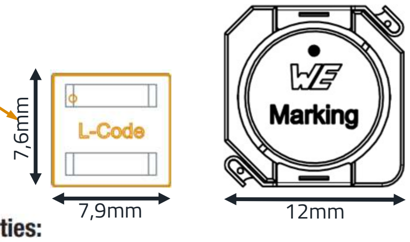
74439387033 [7070] size code

- WE-XHMI



42% more current

X2,4 less surface than PD [1280]



Electrical Properties:

Properties		Test conditions	Value	Unit	Tol.
Inductance	L	100 kHz/ 10 mA	3.3	µH	±20%
Rated Current	$I_{R,40K}$	ΔT = 40 K	18.2	A	max.
Performance Rated Current [1]	$I_{RP,40K}$	ΔT = 40 K	18.2	A	max.
Saturation Current @ 10%	$I_{SAT,10\%}$	|ΔL/L| < 10 %	8.8	A	typ.
Saturation Current @ 30%	$I_{SAT,30\%}$	|ΔL/L| < 30 %	18.6	A	typ.
DC Resistance	R_{DC}	@ 20 °C	6.4	mΩ	typ.
DC Resistance	R_{DC}	@ 20 °C	8.76	mΩ	max.
Self Resonant Frequency	f_{res}		23	MHz	typ.

[1] refer to IEC 62024-2-2020

Test conditions of Performance Rated Current: refer to IEC 62024-2-2020 Class C PCB Copper Width: 40 mm; PCB Copper Thickness: 105 µm)

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SATURATION CURRENT

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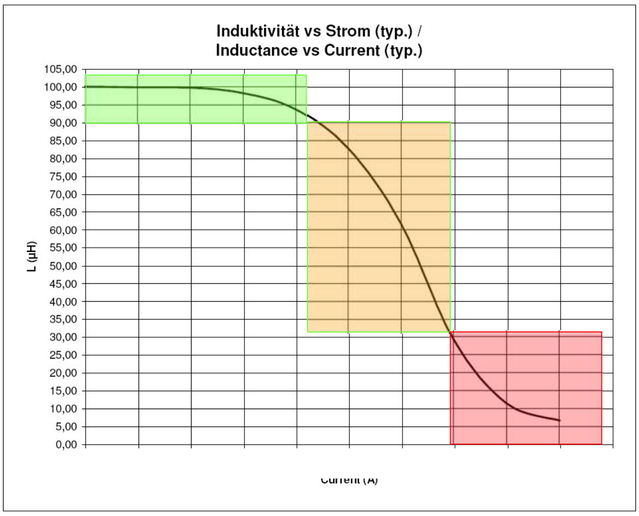
INDUCTOR SELECTION : L VS CURRENT

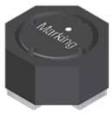


safe operation area

critical operating area

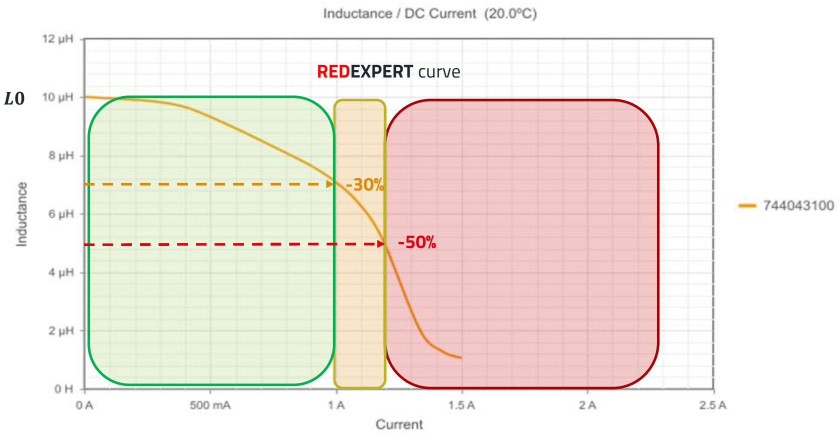
total saturation area

POWER INDUCTORS



Inductor value Vs current

- Calculation with estimated reduction of L value (into saturation)



safe operation area

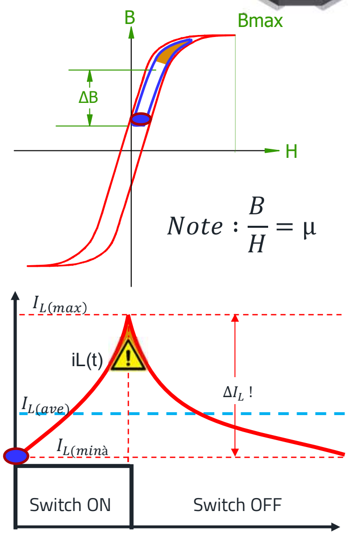
critical operating area

total saturation area

POWER INDUCTORS

REDEXPERT WE-TPC# 744043100 deviation explanation for 10µH I_{sat} = 1,0A

Saturation behavior



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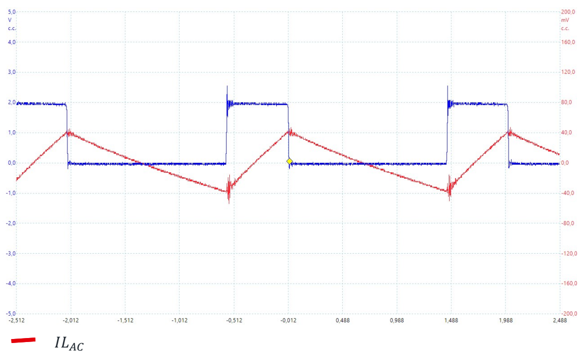
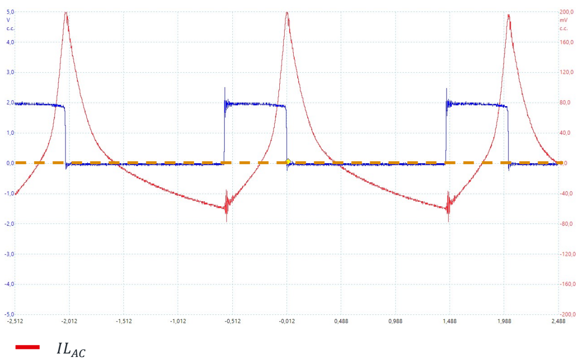
POWER INDUCTORS

Without saturation

- Saturation effect $I_{out}(Buck) = 1{,}0A$
- Saturation effect : real measurements



10µH WE-LHMI# 74437346100 original Isat=7,3A



10µH WE-TPC# 744043100 Isat=1,0A

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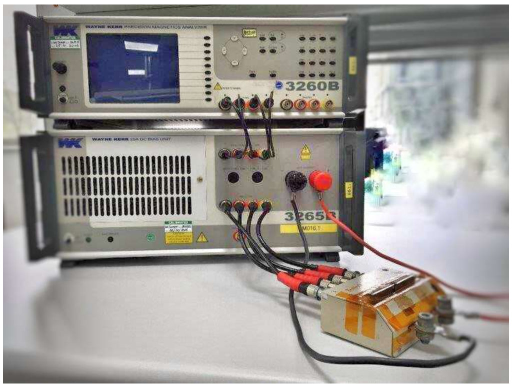
INDUCTOR SELECTION

Saturation Current

- The current that causes an inductance drop compared to it initial inductance value. In most cases for our inductors a drop of 10% is specified.

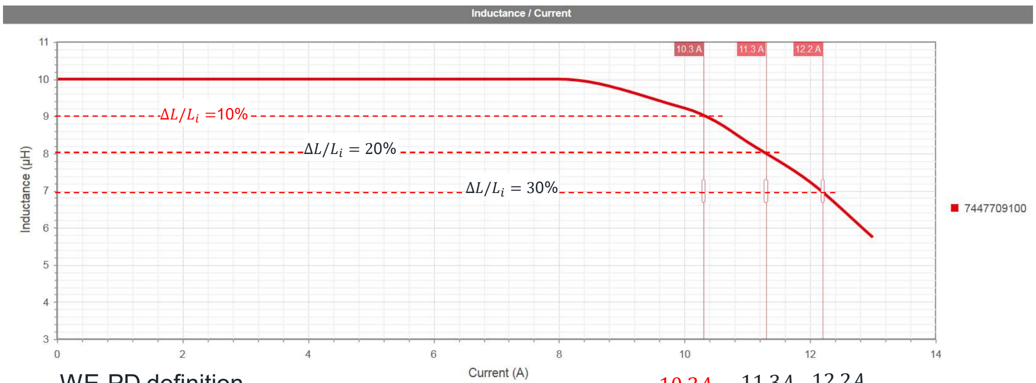
Electrical Properties:

Properties	Test conditions		Value	Unit	Tol.
Inductance	1 kHz/ 250 mV	L	10	µH	±20%
Rated current	ΔT = 40 K	I_R	7.1	A	max.
Saturation current	|ΔL/L| < 10%	I_{sat}	10.5	A	typ.
DC Resistance	@ 20°C	R_{DC}	0.013	Ω	typ.
DC Resistance	@ 20°C	R_{DC}	0.021	Ω	max.
Self resonant frequency		f_{res}	21	MHz	typ.



ANALOG DEVICES

INDUCTOR SELECTION : SATURATION CURRENT



WE-PD definition

$Isat\ @\Delta L/L_i = 10\%$

$10,3A$ $11,3A$ $12,2A$

I_{sat} *depends on the definition*

ANALOG DEVICES

GOOD TO KNOW

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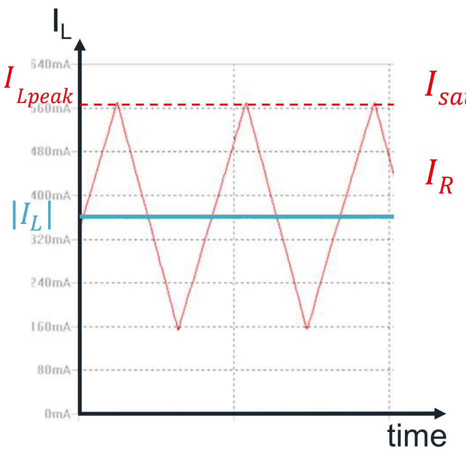
INDUCTOR SELECTION : CURRENT



$I_{sat} > I_{Lpeak}$

$I_R > I_L$

- Buck

$$|I_L| \approx I_{out}$$

- Boost

$$|I_L| \approx \frac{V_{out}}{V_{in}} \cdot I_{out}$$

Electrical Properties:

Properties	Test conditions	
Inductance	1 kHz/ 250 mV	L
Rated current	$\Delta T = 40\ K$	I_R
Saturation current	$\lvert\Delta L/L\rvert < 10\%$	I_{sat}

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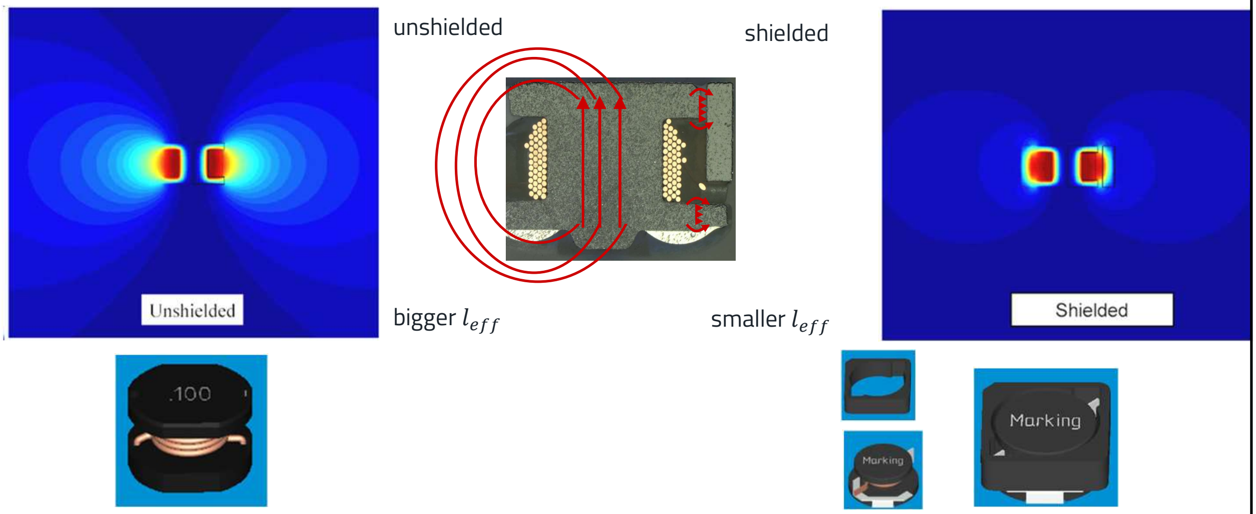
EMC : SHIELDING VS. UNSHIELDING



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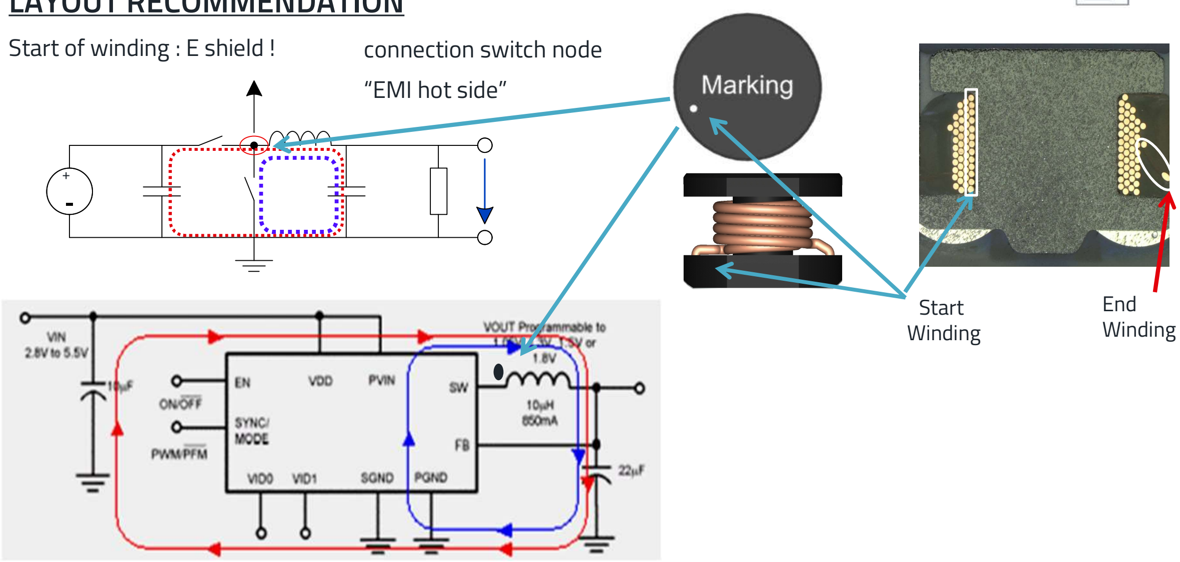
LAYOUT RECOMMENDATION

ANP047

Start of winding : E shield !



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DIFFERENT TECHNOLOGIES

All shielded : WE-SI fully symmetrical , WE-MAPI

WE-PD with start dot

WE-HCF flat wire

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INDUCTOR SMART SELECTION

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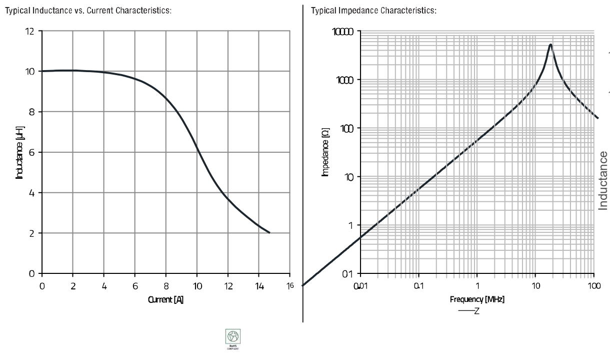
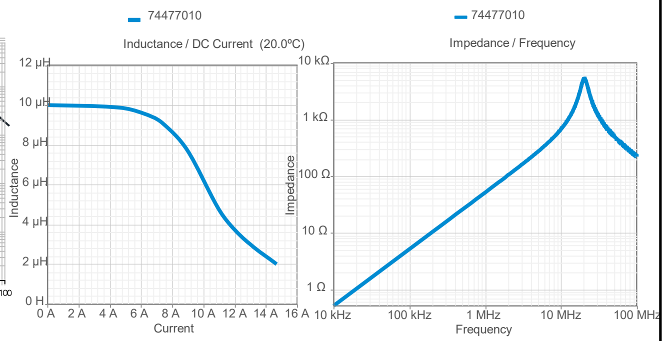
SMART SELECTION OF INDUCTORS

Various tools same results, old VS smart method

- Datasheet



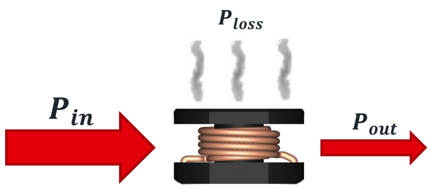
- **REDEXPERT**

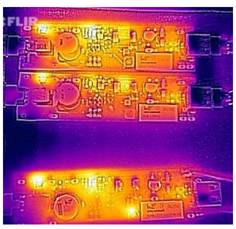


TEMPERATURE VS LOSSES

Why does the component heat up ?

- Losses from energy transit





- Temperature rise specification
  - The overall behavior is :

$$P_{loss} = P_{DC} + P_{AC}$$

  - To be able to simplify measurement only DC is used:

$$P_{loss} = R_{DC} \cdot {I_{DC}}^2$$

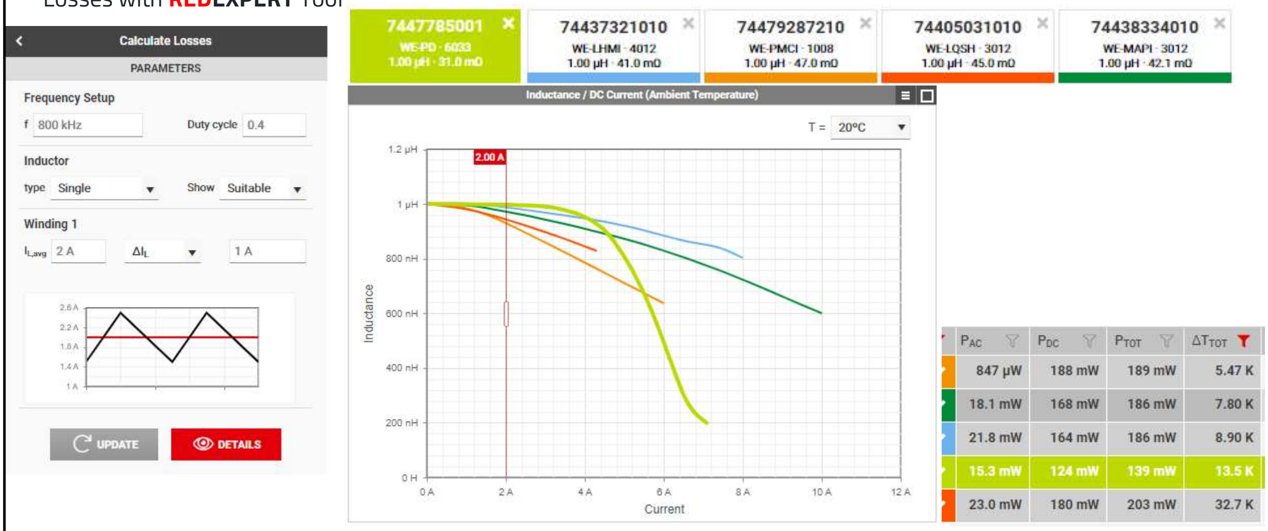
- How estimate overall losses?
  - Launch :

REDEXPERT

REDEXPERT

INDUCTOR : SATURATION AND PACKAGE

Losses with **RED**EXPERT Tool



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TECHNICAL ACADEMY

ANALOG DEVICES

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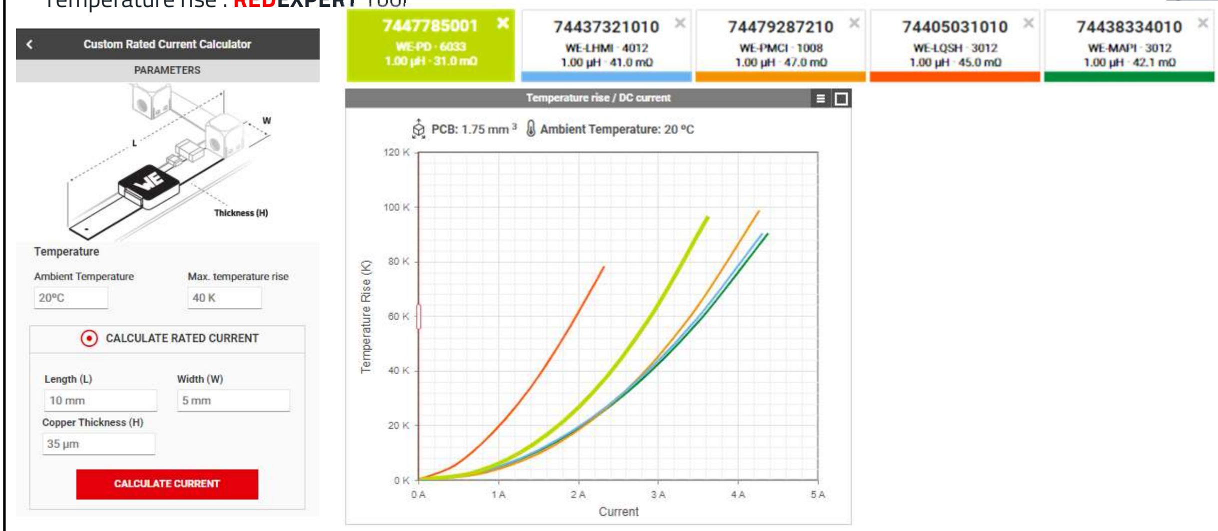
REDEXPERT

INDUCTOR : RATED CURRENT, TEMPERATURE RISE AND LAYOUT

Temperature rise : **RED**EXPERT Tool



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ANALOG DEVICES

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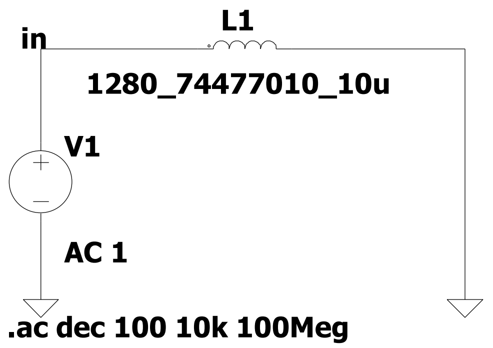
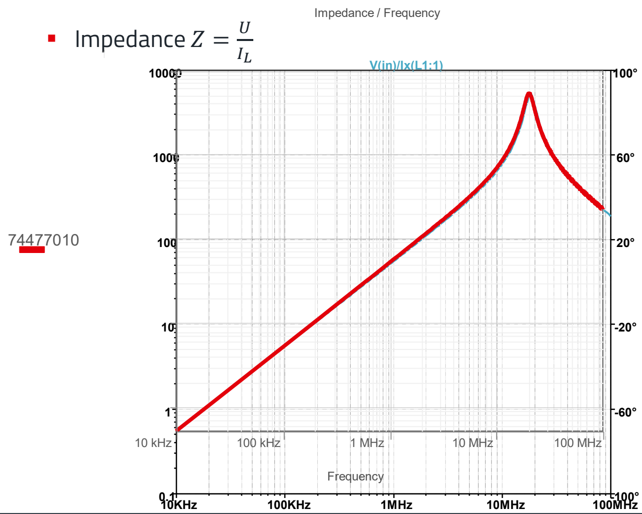
SMART SELECTION OF INDUCTORS

Various tools same results, just choose your preferred

- LtSpice simulation



- Impedance $Z = \frac{U}{I_L}$



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CAPACITOR SELECTION

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CAPACITOR THEORY

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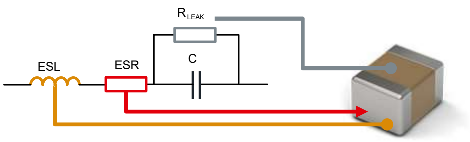
CAPACITORS

Theory : capacitor and parasitic



- The equivalent circuit for a capacitor is as follows:
  - parasitic elements
- ESR - Equivalent series resistor
  - Causes self-heating $P = ESR \cdot I_{RMS}^2$
  - Maximum value is typically specified at 120Hz and 20°C (typ.)
  - Can be calculated as follows:

$$ESR = \frac{tan\ \delta}{2 \cdot \pi \cdot f \cdot C} = tan\ \delta \cdot X_C \qquad X_C = \frac{1}{C \cdot \omega} = \frac{1}{2 \cdot \pi \cdot f \cdot C}$$

- ESL - Equivalent series inductor

$$X_L = 2 \cdot \pi \cdot f \cdot ESL$$

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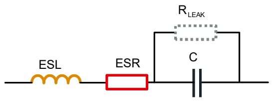
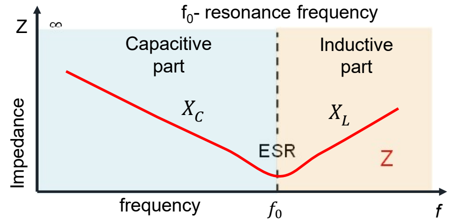
CAPACITOR : IMPEDANCE Z

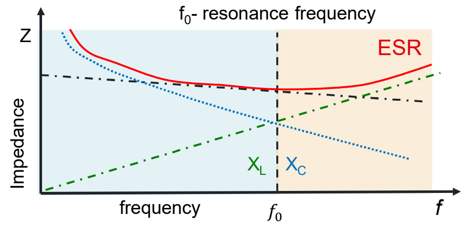
Well known behavior ?!



- $Z = \sqrt{ESR^2 + (X_L - X_C)^2}$
- $Z = \sqrt{ESR^2 + \left(ESL \cdot \omega - \frac{1}{C \cdot \omega}\right)^2}$ $\qquad \omega = 2 \cdot \pi \cdot f$
- $f_0 = \frac{1}{2 * \pi * \sqrt{ESL * C}}$

Note: the ESR of any capacitor have a certain frequency dependance

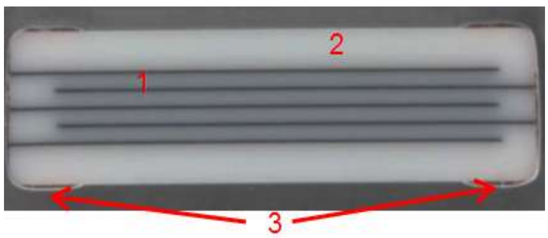


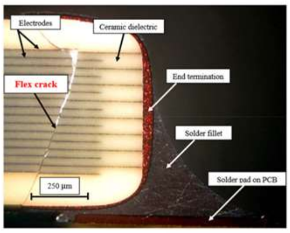


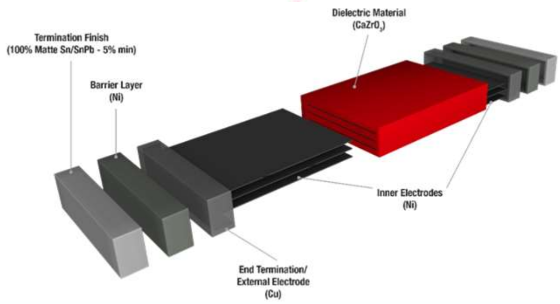
CAPACITORS

Ceramic : **M**ulti **L**ayer **C**eramic **C**apacitor

- Different classes
  - Class 1 : NP0, C0G
  - Class 2 : X7R, X5R…
- Low ESR : few mΩ
- Ultra Low ESL : ≈x100 pH
- Soft termination versions (aid to prevent cracks)







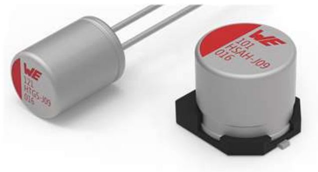
CAPACITORS

Aluminum: Electrolytic / Polymer / Hybrid polymer

- Electrolytic
  - Wet electrolyte
  - Higher voltage / values
    - Voltage ≤ 450V
    - Capacity up to 33000µF
  - THT / SMT / Snap in mount

- Polymer
  - Solid electrolyte
  - Lower ESR / ESL
    - Voltage ≤100V
    - Capacity up to 2000µF
  - THT / SMT / H-Chip: Low profile & Low ESR versions
  - Lifetime

- Hybrid polymer
  - Low ESR & Low leakage current
  - High ripple current characteristics
  - High stability over the temperature range
  - High lifetime performance



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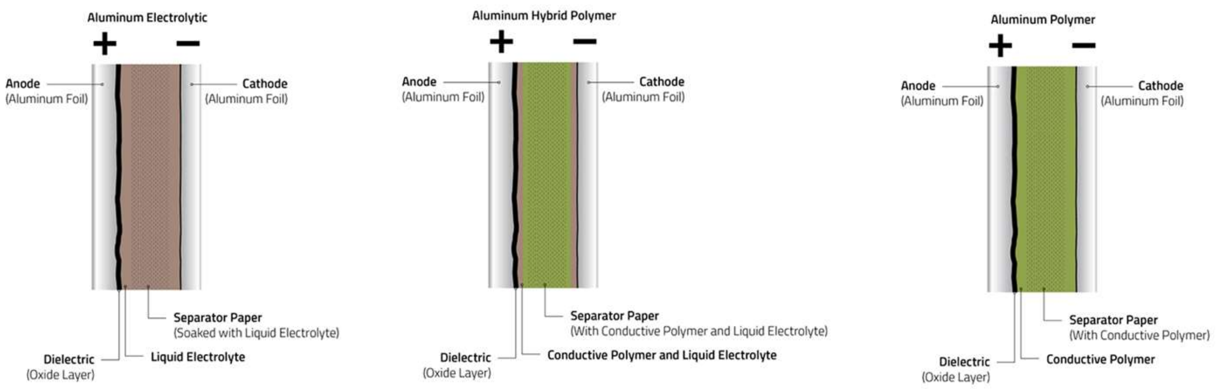
CAPACITORS

Aluminum: Electrolytic / Polymer / Hybrid polymer

- Physical construction



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CAPACITORS

Electrolytic : aging & lifetime with **RED**EXPERT

Lifetime Calculator

REDEXPERT

- Formula :
  - Aluminum electrolytic

$$L_X = L_{nom} \cdot 2^{\frac{T_{Max}-T_a}{10}}$$

  - Aluminum Polymer

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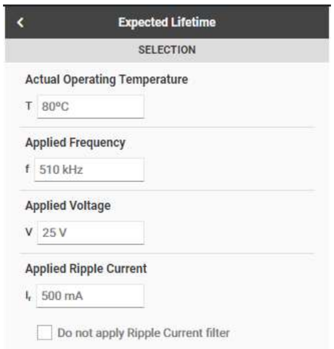
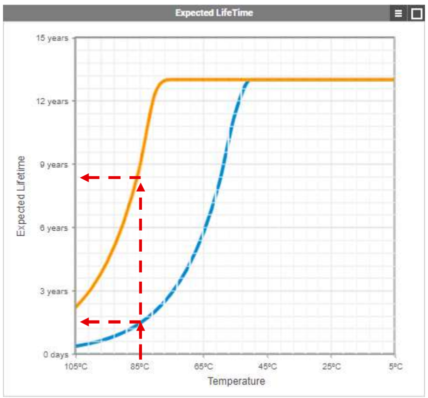
$$L_X = L_{nom} \cdot 10^{\frac{T_{Max}-T_a}{20}}$$





  - Example: comparison of two 1000µF/35V 105°C
    - ATG5 general purpose WCAP-ATG5# 860020578018
    - AT1H long life WCAP-AT1H# 860240580011
    - PTG5 Polymer WCAP-PTG5# 870025175010

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ANALOG DEVICES

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CAPACITOR SMART SELECTION

ANALOG DEVICES

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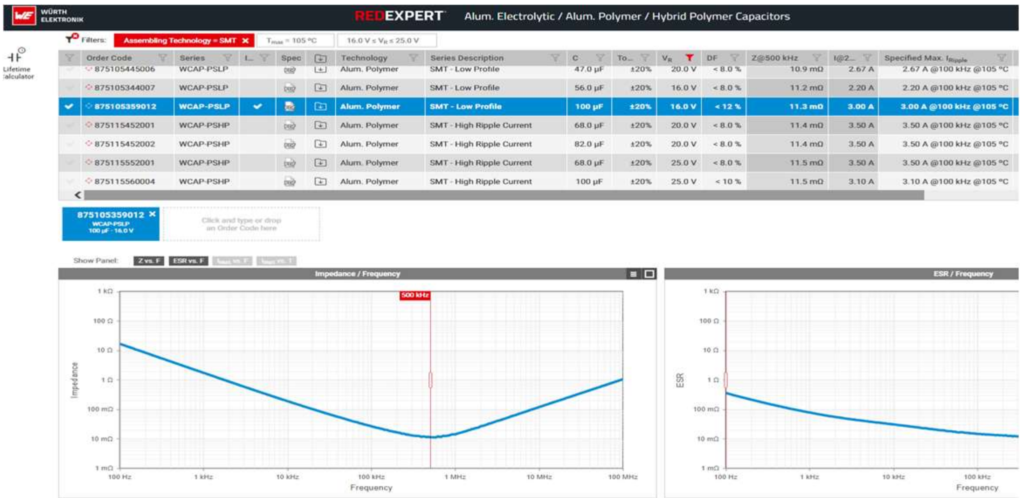
HOW DO YOU FIND THE BEST FITTING INPUT CAP FOR DCDC?

e.g. fsw: 500kHz / Vin: 12V → https://we-online.com/re/5syv8W1J



ANALOG DEVICES

e.g. fsw: 500kHz / Vin: 12V → https://we-online.com/re/5syxRGEc

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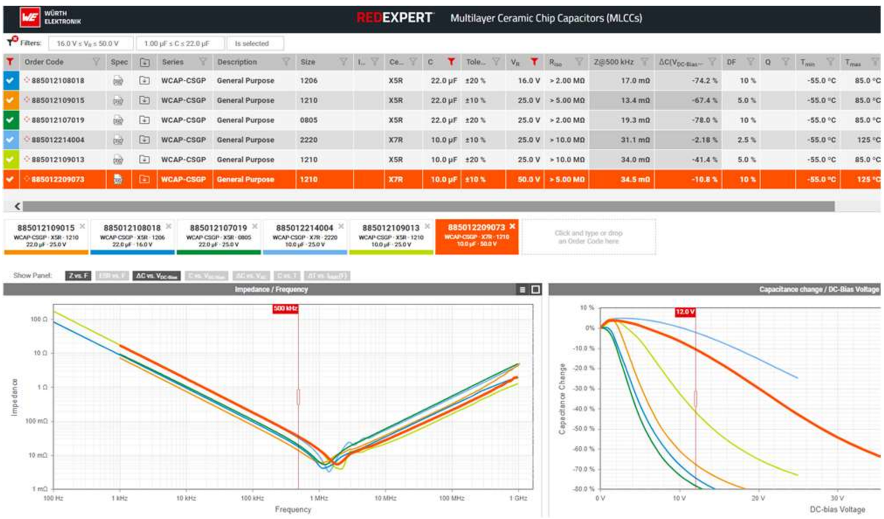
OK, BUT WHY NOT A MLCC?

Do you know Bias effect ? Two values two with two packages comparision



ANALOG DEVICES

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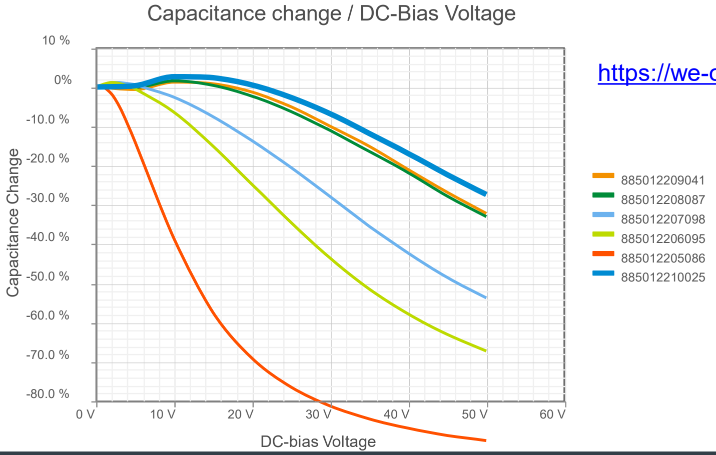
CAPACITORS : BIAS AND PACKAGE

MLCC DC Bias behavior : Size impact onto technology

885012210025	885012209041	885012208087	885012207098	885012206095	885012205086
WCAP-CSGP · X7R · 1812	WCAP-CSGP · X7R · 1210	WCAP-CSGP · X7R · 1206	WCAP-CSGP · X7R · 0805	WCAP-CSGP · X7R · 0603	WCAP-CSGP · X7R · 0402
100 nF · 50.0 V	100 nF · 50.0 V	100 nF · 50.0 V	100 nF · 50.0 V	100 nF · 50.0 V	100 nF · 50.0 V



https://we-online.com/re/5t07mVB4

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ANALOG DEVICES

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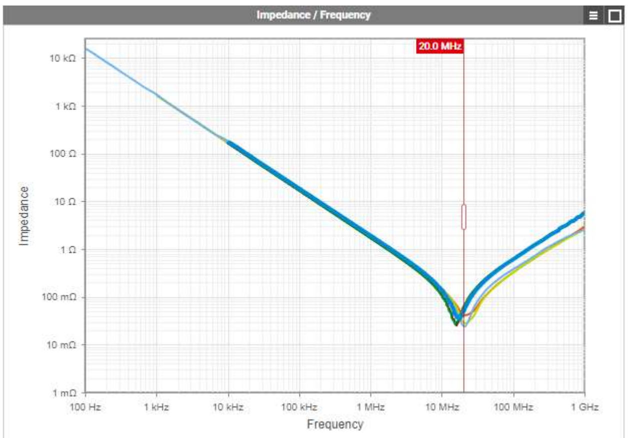
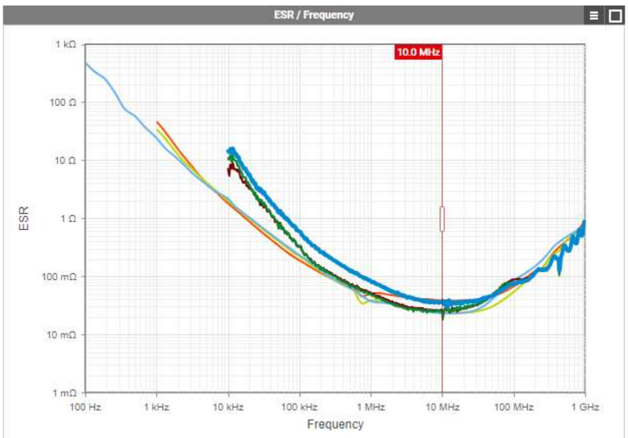
CAPACITORS : ESR AND FREQUENCY

MLCC behavior : global impedance and ESR behavior

885012205086	885012206095R	885012206095	885012208087	885012209041	885012210025	885012207098
WCAP-CSGP · X7R · 0402	WCAP-CSGP · X7R · 0603	WCAP-CSGP · X7R · 0603	WCAP-CSGP · X7R · 1206	WCAP-CSGP · X7R · 1210	WCAP-CSGP · X7R · 1812	WCAP-CSGP · X7R · 0805
100 nF · 50.0 V	100 nF · 50.0 V	100 nF · 50.0 V	100 nF · 50.0 V	100 nF · 50.0 V	100 nF · 50.0 V	100 nF · 50.0 V





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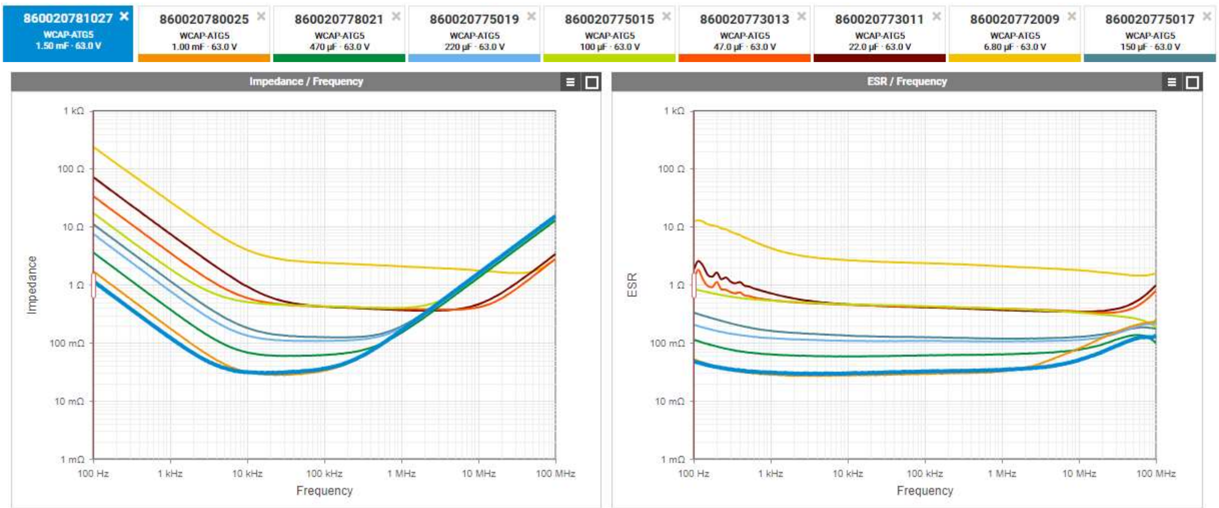
CAPACITORS : ESR AND FREQUENCY

Aluminum caps behavior : global impedance and ESR behavior



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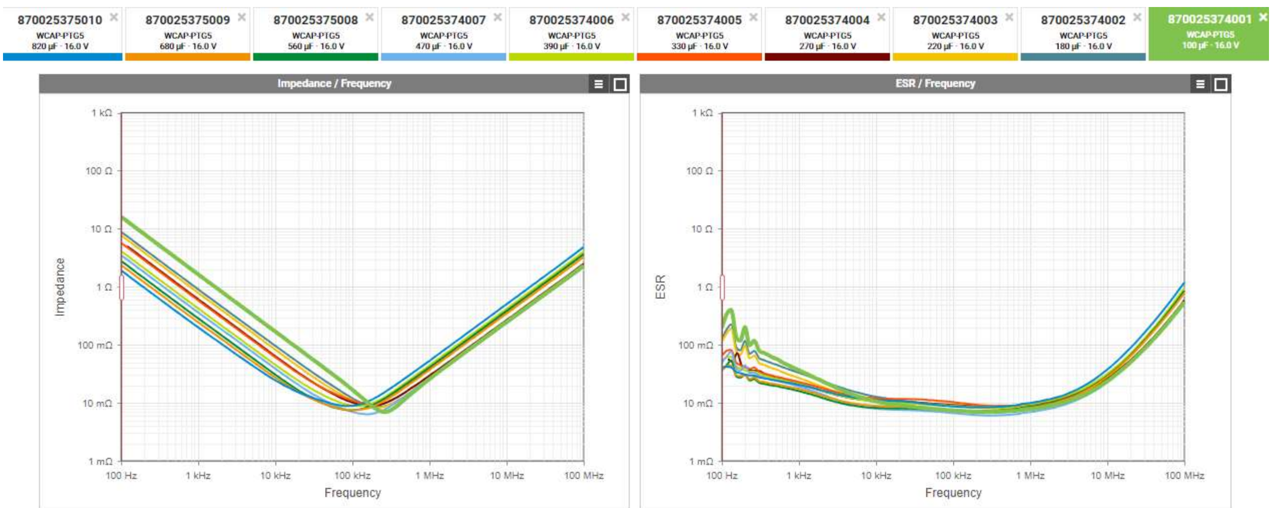
CAPACITORS : ESR AND FREQUENCY

Aluminum Polymer caps behavior : global impedance and ESR behavior



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ANALOG DEVICES

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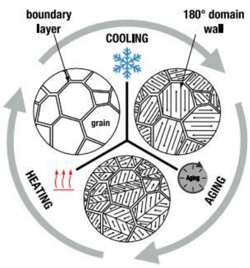
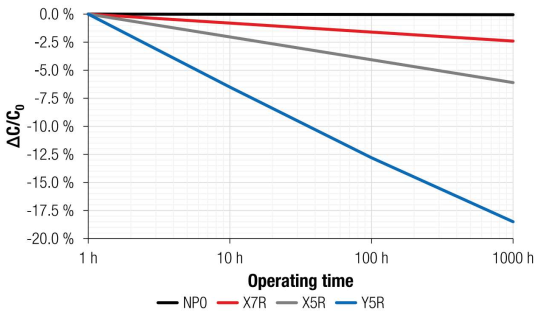
MLCC (MULTILAYER CERAMIC CAPACITOR)

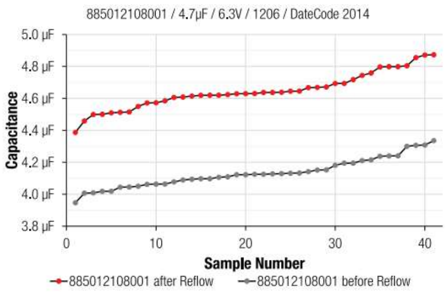
Aging of MLCCs

- Aging process due to changes in crystal structure
- Decreased permittivity cause capacitance loss
- Class 1 (NP0) no aging
- Class 2 has different aging
- Behavior depends on ceramic materials



Check the **Application Note SN011** for more information about MLCC Aging



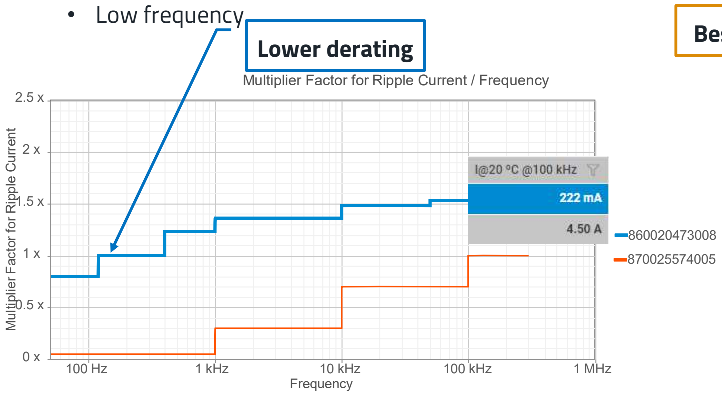


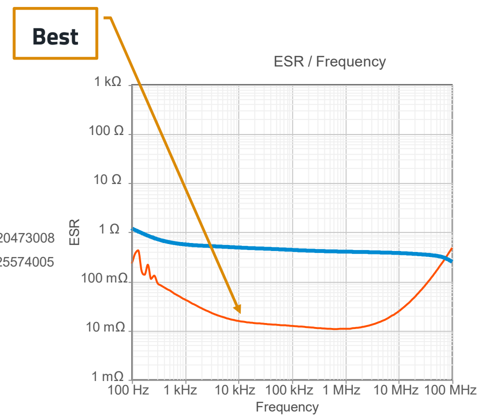
ANALOG DEVICES

RIPPLE CURRENT

	Order Code	Series	Spec		Technology	Series Description	C	To...	V_R	DF
✓	860020473008	WCAP-ATG5			Alum. Electrolytic	THT - General Purpose +105°C	100 µF	±20%	25.0 V	< 14 %
✓	870025574005	WCAP-PTG5			Alum. Polymer	THT - General Purpose +105°C	100 µF	±20%	25.0 V	< 8.0 %

- **Aluminum Electrolytic** Capacitors
  - **Recommended** for mains rectification / filtering
    - Low frequency
- **Aluminum Polymer** Capacitors
  - **Lower** ESR and high frequency dedicated





ANALOG DEVICES

CAPACITIVE POWER SUPPLY

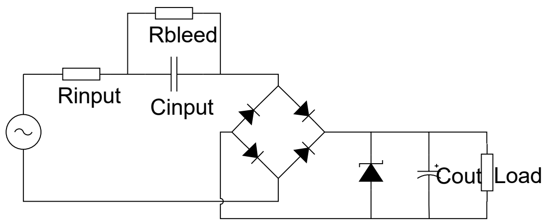
LTspice

CAPACITOR

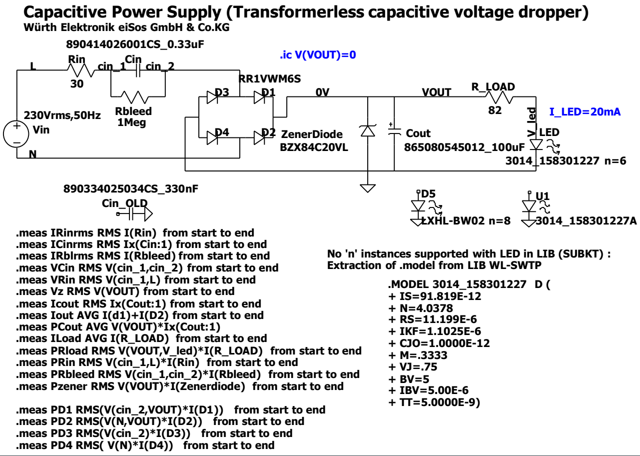
Special use and simulation

- Capacitive Power Supplies: with FTXH series WCAP-FTXH _2

Cinput: fixed impedance act as current source
Rinput: inrush current limiter $\widehat{V_{ac}} = 325V$ and $Vout = 0V$
Rbleed: security discharge resistor



- LtSpice Schematic



CAPACITOR

Capacitive Power Supplies

- Log results (truncated)
"CTRL L" to display log file for measurements

```
Simulate: transient analysis
.tran 600ms startup
; Power Efficiency Calculation

.meas start PARAM 300ms
.meas end param 600ms
.meas PRectAgain  param PD1 + PD2 + PD3 + PD4
.meas PCin param (V(cin_1,cin_2)*Ix(Cin:1)) from start to end
.meas Plosses param PRectAgain  + PCout + Pzener + PRbleed + PRin
;.meas Pin_S RMS V(L,N) * RMS I(VIN) from start to end
;.meas Pin param Pout/(Pout+Plosses) from start to end
.meas Pin_P AVG (-I(Vin)*V(L,N))  from start to end
.meas Pout AVG V(VOUT)*I(R_LOAD)  from start to end
.meas Effic param Pout/Pin_P
;.meas Effic2 param Pout/Pin
; Power Factor Calculation

.meas Irms RMS I(VIN) from start to end
.meas Vrms RMS V(L,N) from start to end
.meas Pin_S param Vrms*Irms
.meas PF param Pin_P/Pin_S
```

Param Name	Formula	Values	FROM	Start	TO	Stop
start:	300ms	0.3				
end:	600ms	0.6				
prectagain:	pd1+pd2+pd3+pd4	0.0515952				
pcin:	(v(cin_1,cin_2)*ix(cin:1))	-0.148631				
plosses:	prectagain+pcout+pzener+prbleed+prin	0.174153				
pin_p:	AVG(-i(vin)*v(l,n))	0.492995	FROM	0.3	TO	0.6
pout:	AVG(v(vout)*i(r_load))	0.388436	FROM	0.3	TO	0.6
effic:	pout/pin_p	0.78791				
irms:	RMS(i(vin))	0.0233345	FROM	0.3	TO	0.6
vrms:	RMS(v(l,n))	229.81	FROM	0.3	TO	0.6
pin_s:	vrms*irms	5.36251				
pf:	pin_p/pin_s	0.0919336				

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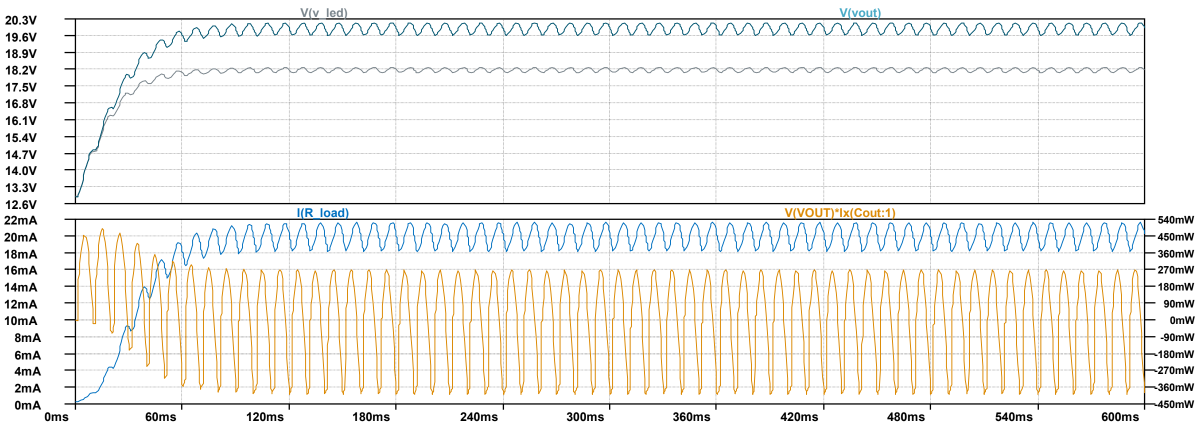
CAPACITOR

Capacitive Power Supplies

- Scopes of main current and voltages :



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GOOD TO KNOW

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CAPACITORS

Some other technologies and structure

- Snap-in and screw…

https://www.we-online.com/en/components/products/pbs/capacitors/aluminium_electrolytic_capacitors/aluminium_electolytic_snap-in_capacitors

https://www.we-online.com/en/components/products/pbs/capacitors/aluminium_electrolytic_capacitors/wcap_screw_capacitors

- Non polar

https://www.we-online.com/en/components/products/WCAP-ASNP

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CAPACITOR

Vibration-proof Aluminum Electrolytic- and Aluminum Hybrid Polymer Capacitors!

- Capacitors with high base plates are available on request for Aluminum Electrolytic- and Aluminum Hybrid Polymer Capacitors, as project parts.
- What are the benefits? - The SMT capacitor is surrounded by a high base plate that also has larger soldering pads, due to that, the results in vibration tests improve and the parts can withstand up to 30G.
- Ask us for more information about the High Baseplate

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