WE MEET
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ESSENTIALS FOR THE DESIGN OF AN GB ETHERNET FRONT END

Dr.-Ing. Heinz Zenkner
Consultant in behalf of Application Engineering and Technical Marketing
Würth Elektronik eiSos

Agenda

- 1 GB Ethernet front end design, overview
- Block diagram of a typical design
- Hardware design of a GB front end
- Schematic of the Ethernet interface
- Necessary key parameters of the components
- Some facts about signal integrity
- Layout considerations
- EMC results

1 GB Ethernet front end design, overview

- The 1GB Ethernet interface operates according to the 802.3ab-1999 (CL40) standard
- 4 wire pairs / channels for signal transmission → 4 symmetric data transmission channels
- Symbol rate: 125 megabaud (MBd) = symbols per second
- Bandwidth: 62.5 MHz per channel (2 bits per symbol)
- Some special features of the GB-Ethernet protocol
  - 1000Base-X PHY includes a connection configuration protocol (AutoNegotiation)
  - 8-bit data bytes are converted into 10-bit code groups, advantages:
    - Control of the transmission density
    - Run length limitation (of the data strings)
    - DC compensation
    - Error robustness: All single, double and triple bit errors in a frame are detected with 100% reliability.
  - Signal voltage: Average 750 mV differential, limits are > 670 mV, < 820 mV
  - Impedance 100 Ω

1 GB Ethernet front end design, overview

- Cable types, which one should be used?

  - CAT-5 cable, currently most commonly used (consumer sector) usable up to a bandwidth of 100 MHz, not recommended for 1GB Ethernet
  - CAT-6 cable, usable up to 250 MHz, above 100 MHz bandwidth is clearly dependent on cable length, for 1GB-Ethernet (bandwidth 250 MHz, 62,5 MHz per channel) only conditionally usable
  - CAT-6a cable reaches a bandwidth of up to 500 MHz (higher common mode impedance)
  - CAT-7 cable achieves a bandwidth of up to 600 MHz, 4 separately shielded wire pairs in one overall shielding
  - CAT-7a achieves up to 1,000 MHz
  - CAT-8 cable achieves a bandwidth of up to 2 GHz, only used for short distances
  - CAT 8.1 compatible with normal Ethernet plugs
  - CAT 8.2 uses a connector specially designed for professional use

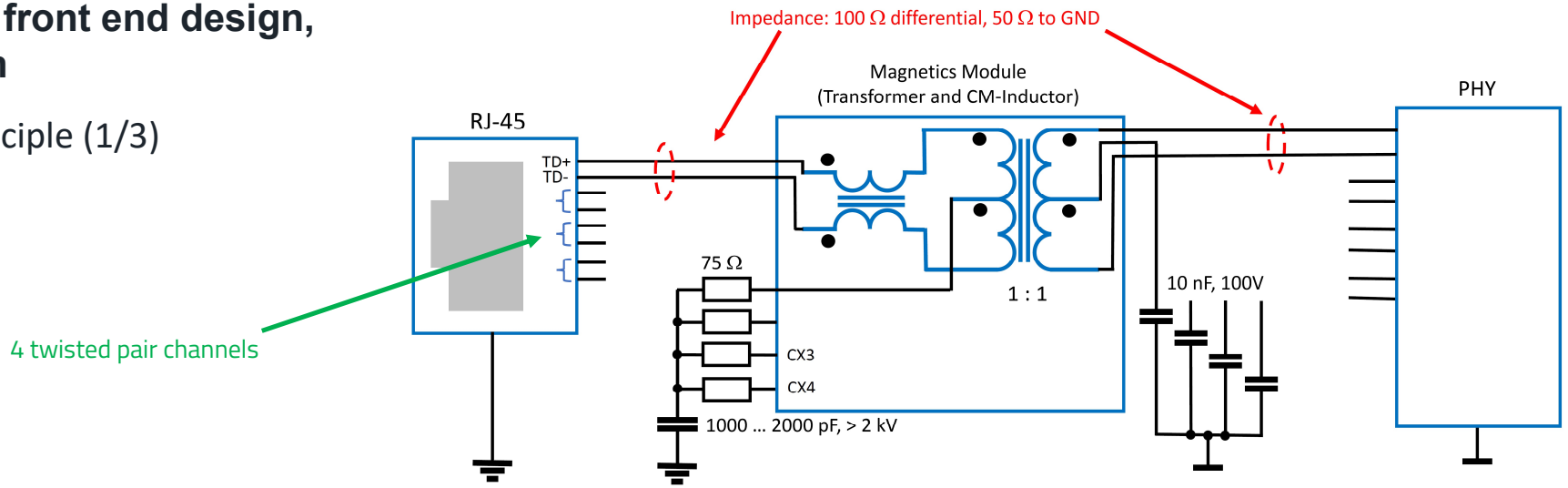
1 GB Ethernet front end design, overview

- Most common causes of network problems are rule violations.
  - Do not use cables of any length and use only suitable cable categories
  - When cascading, do not use not any number of hubs
  - Unfavourably chosen network structure can lead to errors in the network
  - If the quality of the cables and the "hardware performance" are low, the data rates cannot be achieved

1GB Ethernet Front End Design

1 GB Ethernet front end design, block diagram

- Functional principle (1/3)



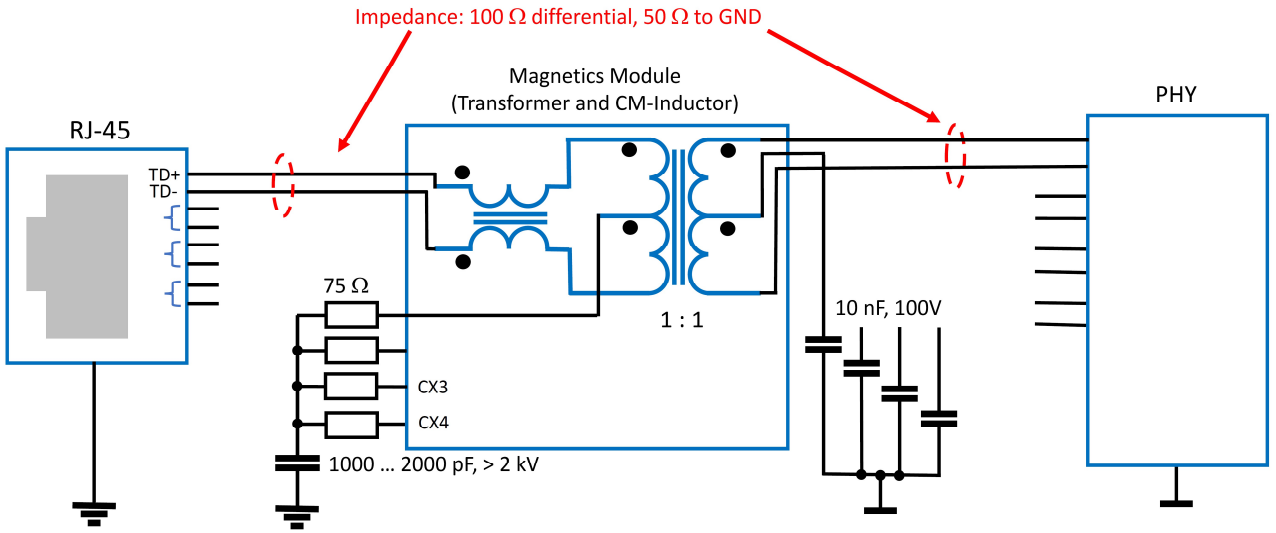
- Full duplex transmission (simultaneous transmission of transmit and receive data).
- UTP impedance: 100 Ω and STP: 150 Ω (1000BASE-T: IEEE 802.3, e.g. section 39).
- CAT 5e, 6 and 6a: Both shielded and unshielded available.
- CAT 7 and 7a are always shielded.

} Impedance problem!

- IEEE standard requires galvanic isolation by means of a transformer
  - Protects equipment from damage by high voltage.
  - Prevents voltage offsets caused by potential differences between the devices.

1 GB Ethernet front end design, block diagram

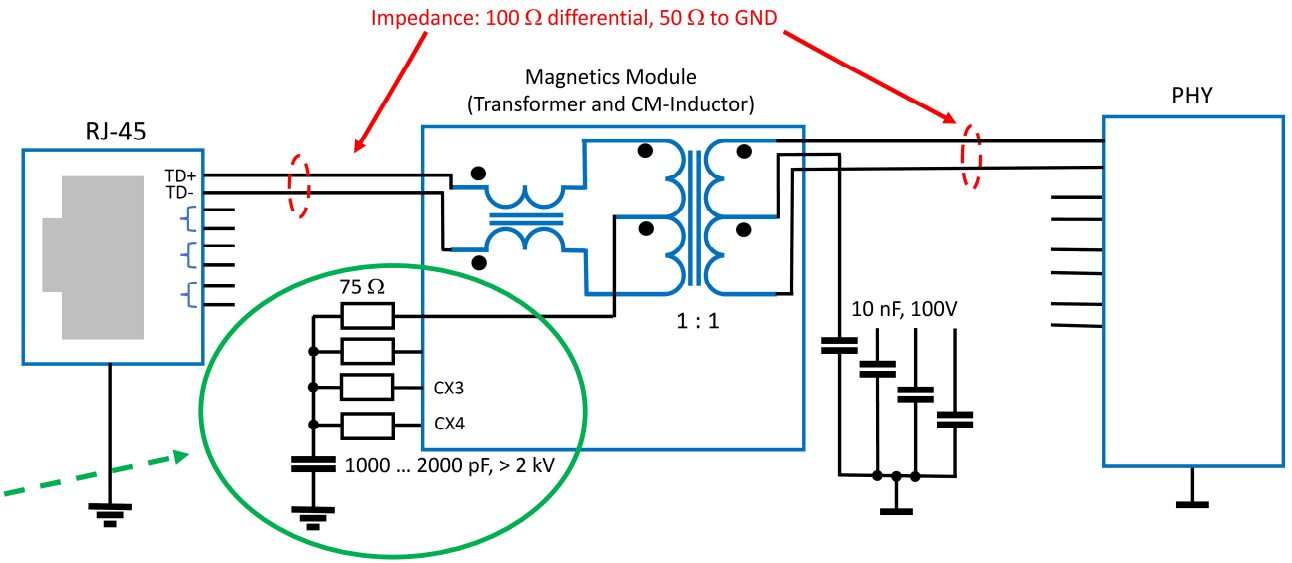
- Functional principle (2/3)



- Transformer (1:1) with center taps: Signal-technically zero potential.
  - Unbalances cause voltage at the center taps
    - Draining of the unbalanced voltage via 75 Ω resistors and capacitor to ground
  - Terminating capacitor on primary side, typ. 200 ... 2000 pF/ 2 kV
  - Transformer 1:1, with a prim. / sec. impedance: 100 Ω differential / each with 50 Ω to ground
  - Secondary side center tapping via capacitors AC (HF) connected to ground

1 GB Ethernet front end design, block diagram

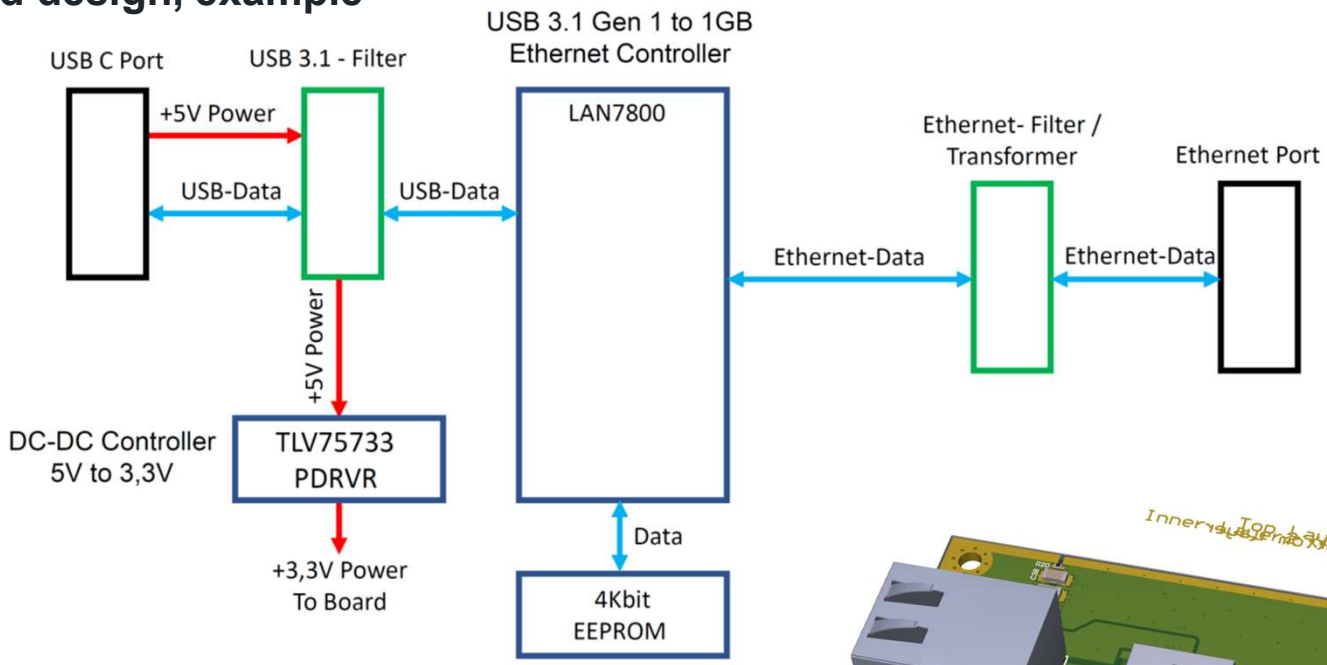
- Functional principle (3/3)

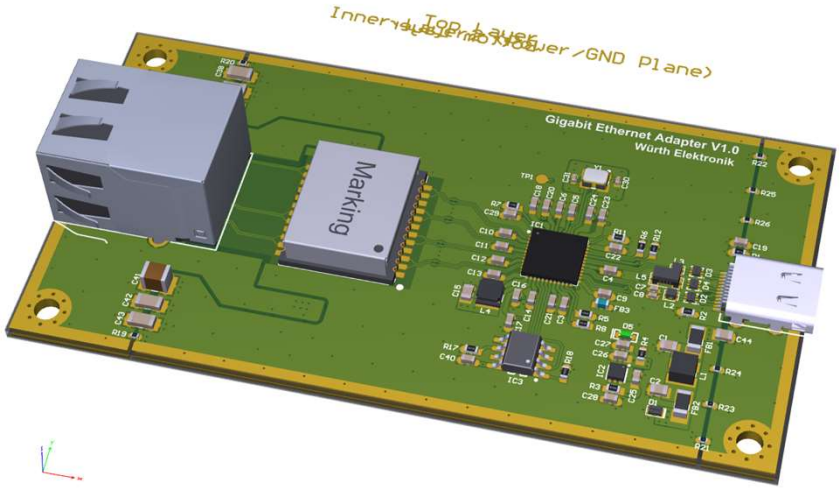


- "Bob Smith" termination
  - Reduces interference caused by common mode current flows.
  - Reduces susceptibility to interference caused by unused wire pairs on the RJ-45 - connector.
  - Bob Smith was referring to the CAT5 cable (Imp. 150 Ω per wire pair), problem:
    - Different cable types have different impedances.
    - A cable does not show a constant impedance over its length due to twisting.
    - Common mode chokes have been implemented, which cannot correct the deviations in impedance matching!
    - However, common-mode chokes improve the EMC.

1 GB Ethernet front end design, example of a hardware design

- Block diagram

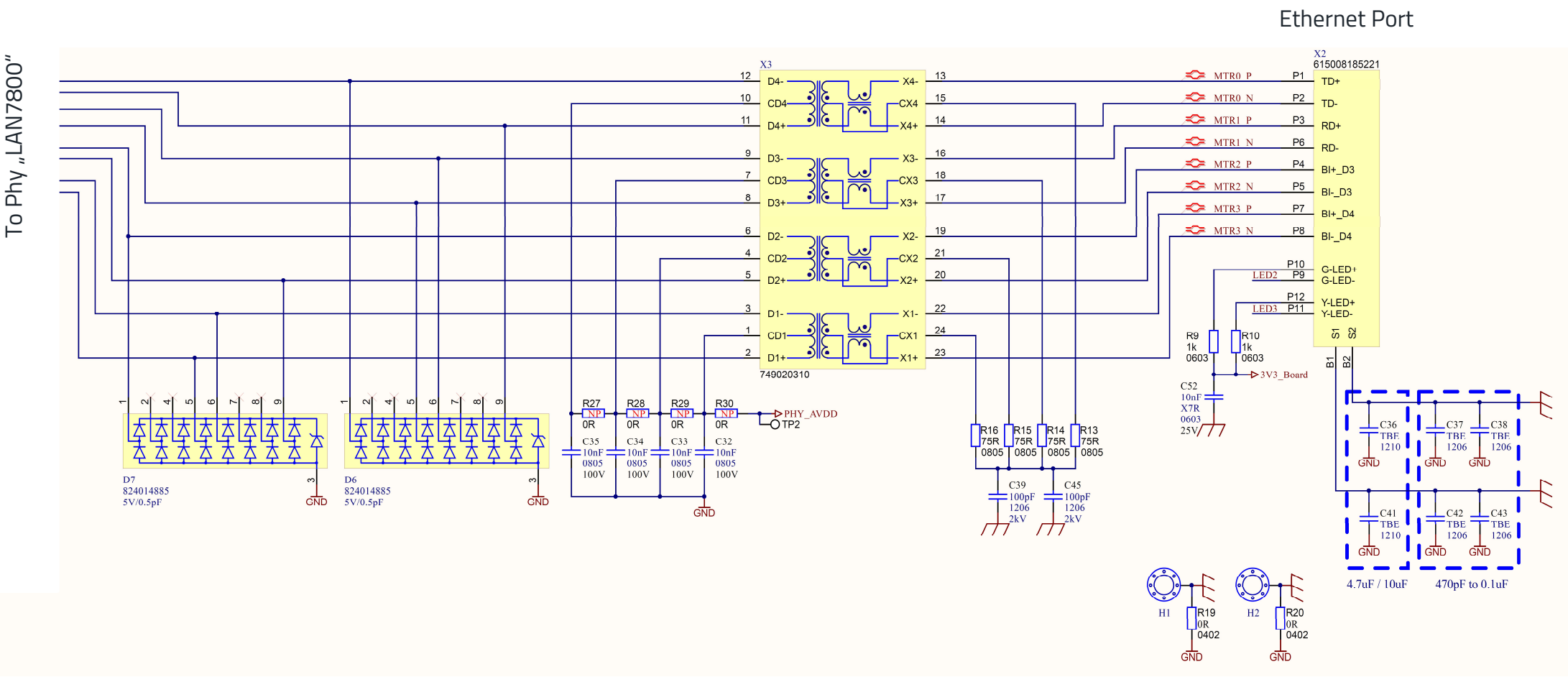




- 1GB Ethernet - USB3.1 converter based on the LAN-Ethernet controller LAN7800 from Microchip Technology.
- Firmware enables real-time measurement of data rate and bit error rate.
- USB side: +5 V and an onboard DC-DC controller (+3.3 V).
- Additional 4kbit EEPROM for FW.

1 GB Ethernet front end design, example of a hardware design

- Schematic, Ethernet interface, overview

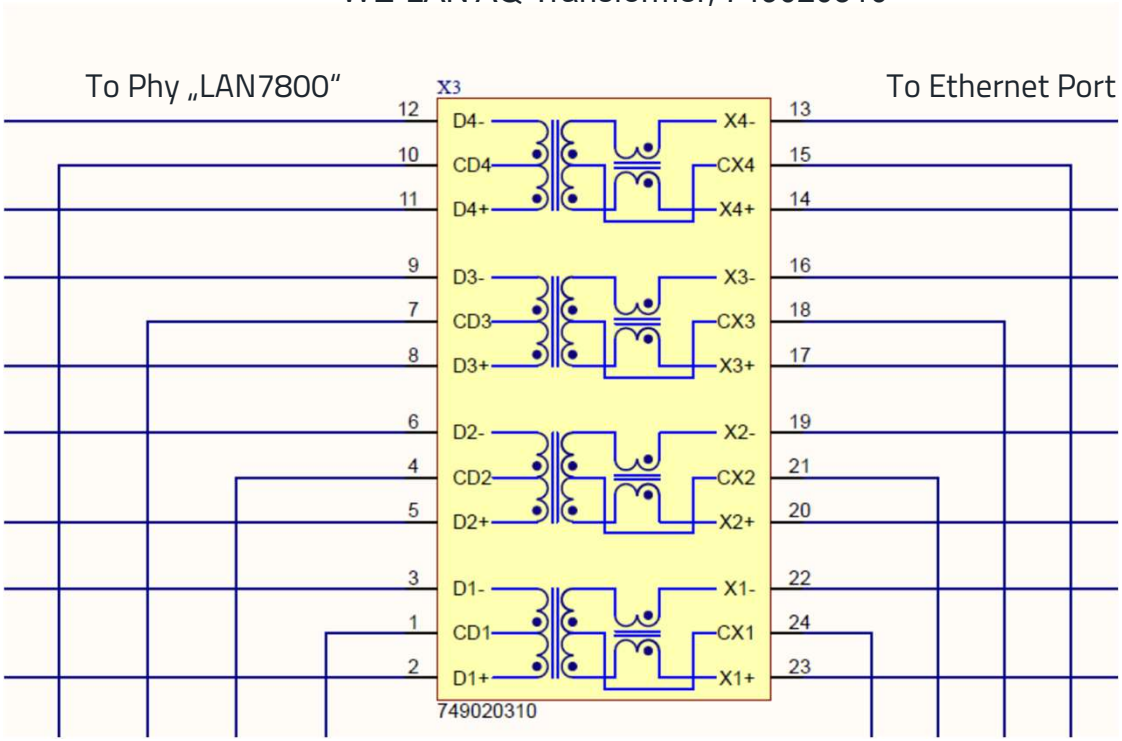


1 GB Ethernet front end design, example of a hardware design

- Schematic, Ethernet Interface, detailed explanations

- Transformer
  - DC (galvanic) isolation between the electronics and the network cable.
  - Integrated common mode chokes, to reduce interference from the cable.
  - The middle tap of the primary winding has the so-called Bob Smith termination network.

WE-LAN AQ Transformer, 749020310



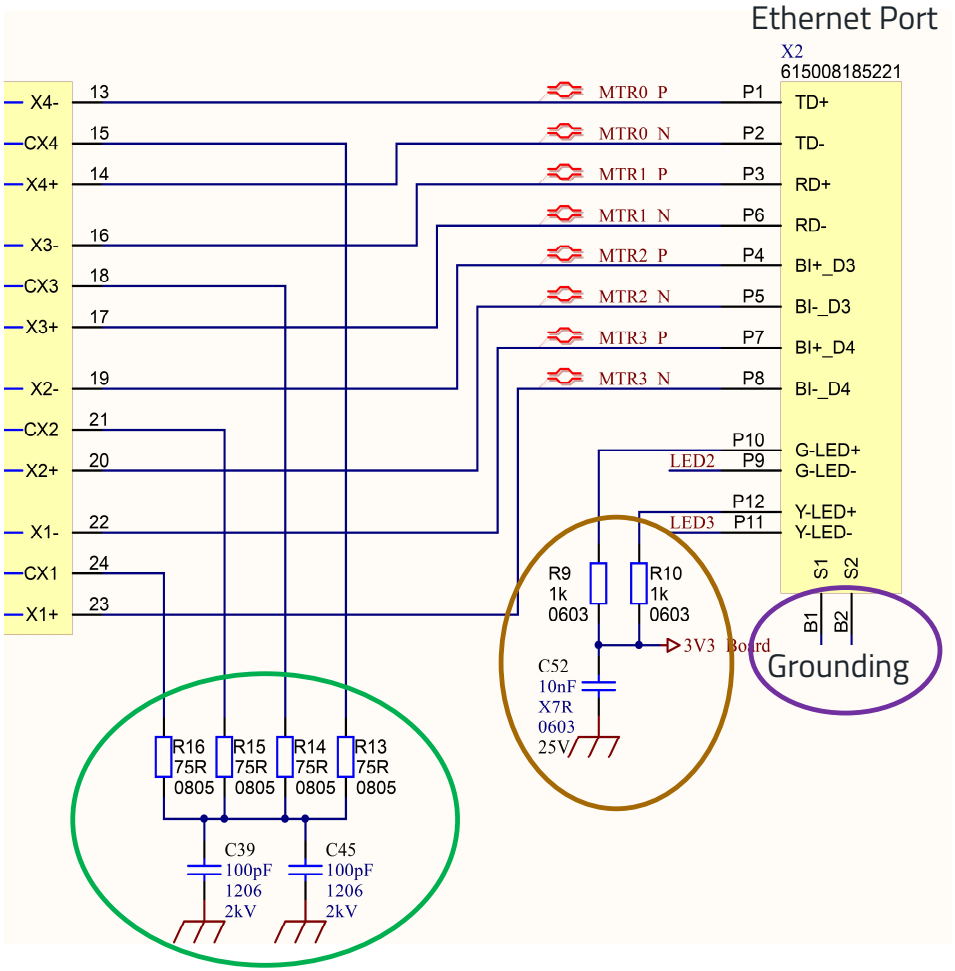
1 GB Ethernet front end design, example of a hardware design

- Schematic, Ethernet Interface, detailed explanations

- "Bob Smith" termination with one 75 Ω resistor per wire pair to a "star point", galvanic isolation with 2 x 100 pF / 2kV to the enclosure ground.

- R9, R10 and C52 are for the power supply of the LEDs integrated in the connection socket.

- B1 and B2 are connections of the socket-housing ground -> connection to the housing.



1 GB Ethernet front end design, example of a hardware design

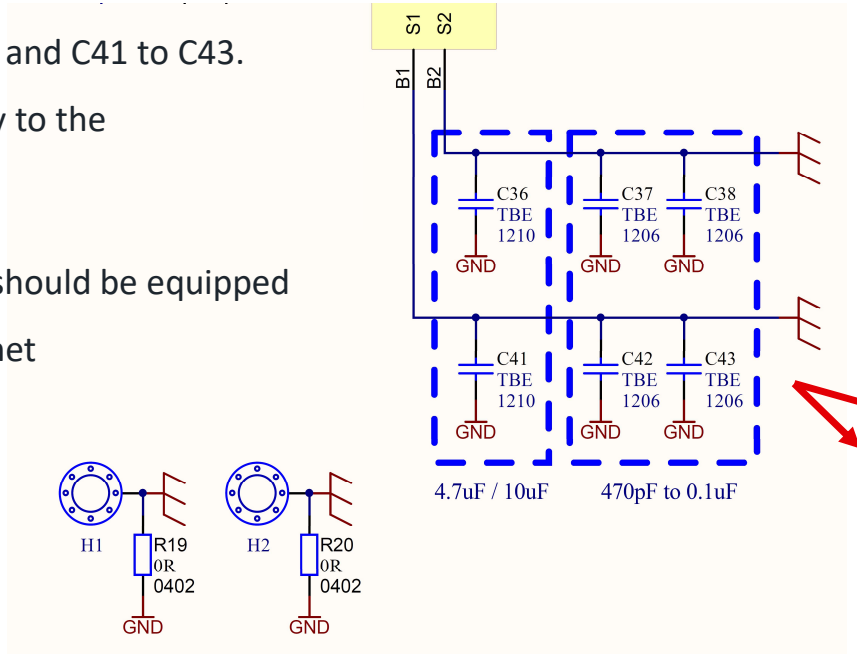
- Schematic, Ethernet Interface, detailed explanations

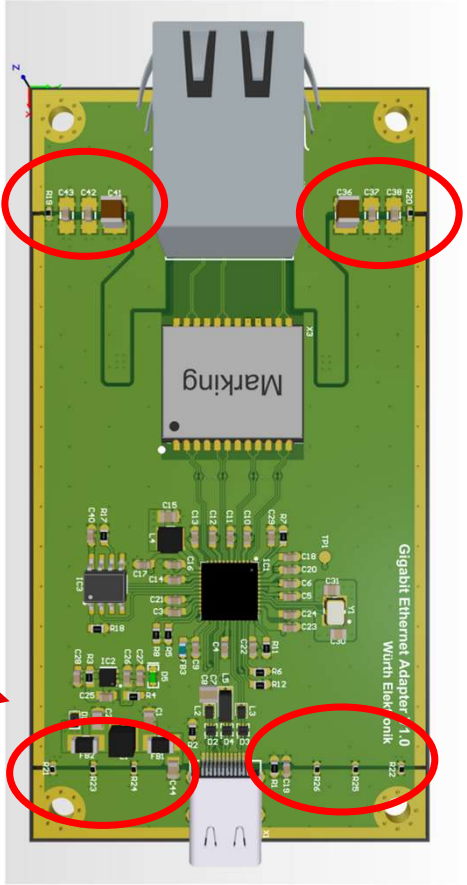
- By C36 to C38 and C41 to C43, the shielding of the Ethernet socket can be connected to the board ground (GND).

- In the case of sheet metal enclosures
  - Do not assemble the capacitors C36 to C38 and C41 to C43.
  - Connect the GND of the electronics directly to the enclosure via screws.

- In the case of plastic enclosures, the capacitors should be equipped
  - In order to connect the shield of the Ethernet cable to the reference ground.

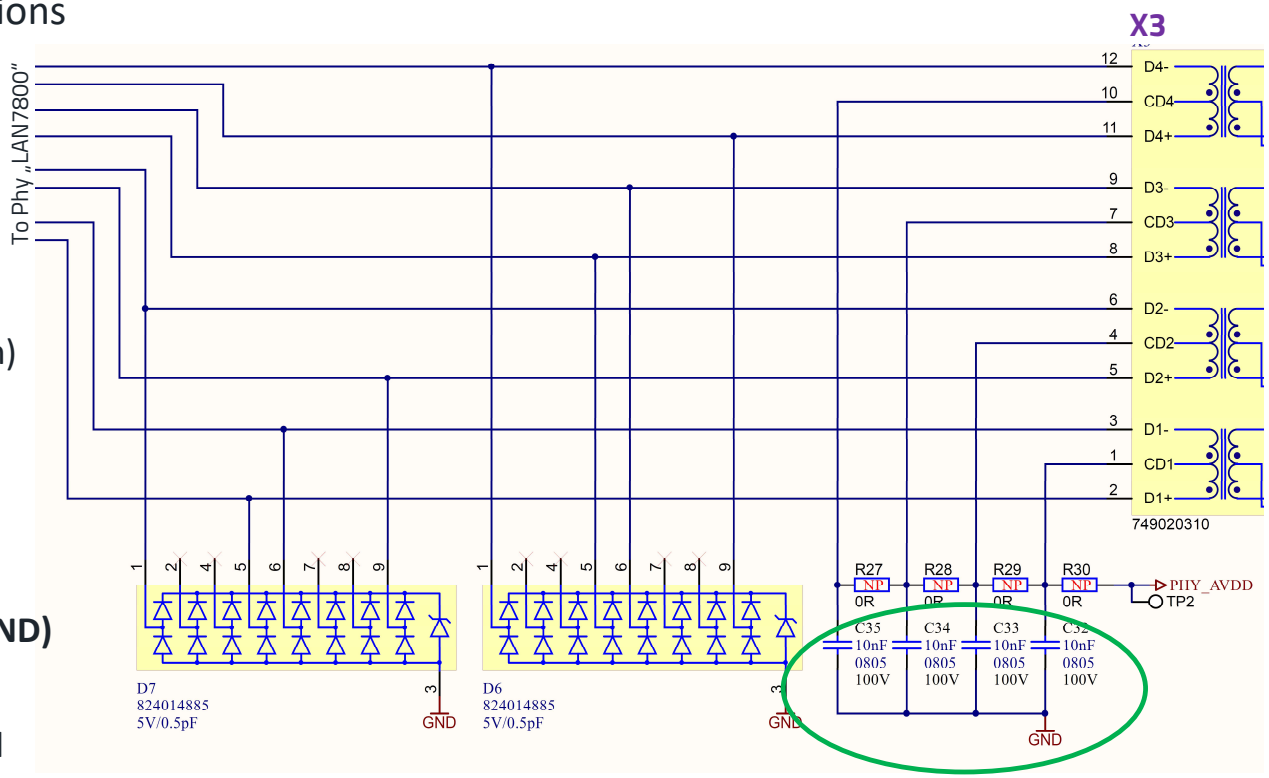
- 0 Ω resistors R19, R20 have the same purpose. The alternative configurations are intended for "experimental" purposes.





1 GB Ethernet front end design, example of a hardware design

- Schematic, Ethernet Interface, detailed explanations
- C32 to C35, DC decoupled connection between the centre taps of the transformers to the ground (GND).
  - Avoid DC equalising currents from the PHY.
- R27 to R30 are provided due to requirements of some PHY manufacturers (Current Mode Line Driver - Option)
  - Not needed if the PHY operates in Standard Voltage Mode.
- TVS diode arrays D6, D7 for limiting transient interferences to the PHY **against the circuit ground (GND)**
  - After X3 module, transient interferences occur in common mode. -> TVS diodes must be connected to each connection of the transformers **to the reference ground of the PHY.**
    - Interference levels are lower on the secondary side of the transformer than on the primary side.
    - TVS diodes need a **low-impedance connection**, looped into the signal lines and bonded directly to GND.

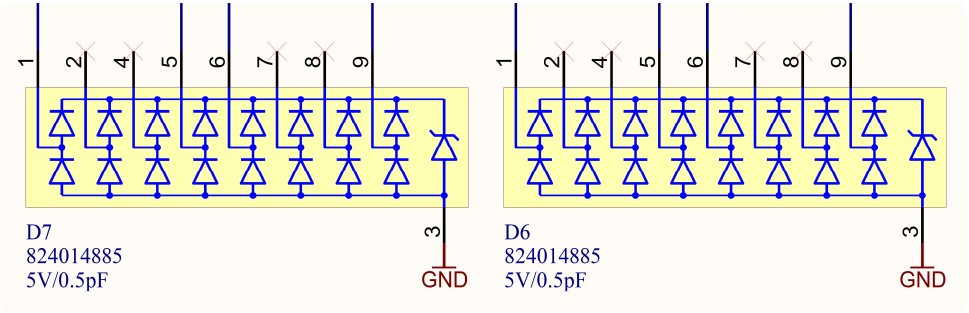


1 GB Ethernet front end design, example of a hardware design

- TVS-Diode Arrays

- For proper functioning of the data transmission the capacitance between the signal lines must be small.
  - Here: C_{Cross} max.: 0.08pF.
  - This is the capacitance of the diode with which the "Ethernet signal" is loaded.

- Parasitic capacitances of the entire design must be added: PCB solder points, vias, capacitance between components to the housing.



I/O to GND

I/O to I/O

Properties		Test conditions	Value			Unit
			min.	typ.	max.	
Channel Operating Voltage	V_{Ch}	I/O to GND			5	V
(Reverse) Breakdown Voltage	V_{BR}	I/O to GND; I_{BR}=1mA	6		9	V
Channel (Reverse) Leakage Current	$I_{Ch\ Leak}$	I/O to GND $V_{I/O}=V_{Ch}$; V_{GND}= 0V			1	µA
Forward Voltage	V_F	GND to I/O; I_F=15mA		0.9	1.2	V
(Channel) Input Capacitance	C_{Ch}	I/O to GND $V_{I/O}$=2.5V; V_{GND}=0V; f=1MHz		0.5	0.65	pF
Channel to Channel Input Capacitance	C_{Cross}	between I/O pins $V_{I/O}$=2.5V; V_{GND}=0V; f=1MHz		0.03	0.08	pF
Channel ESD Clamping Voltage	$V_{Ch\ Clamp\ ESD}$	IEC 61000-4-2 +8kV (TLP=16A) Contact Mode; I/O to GND		10.5		V
Polarity	Unidirectional					

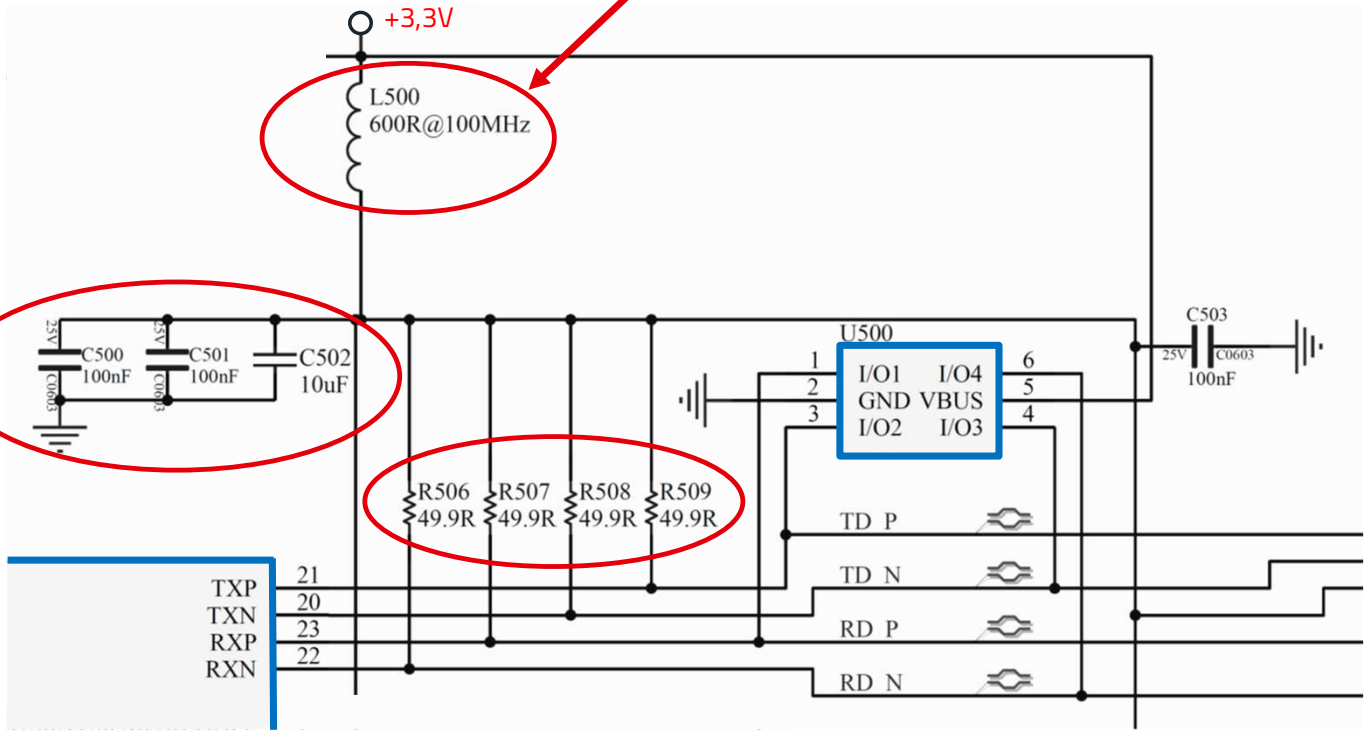
1 GB Ethernet front end design, example of a hardware design

- Additional Pull-Up resistors (not implemented in our design)

  - Some Phys need additional Pull-Up resistors.

  - 49.9 Ω, 1.0% pull-up resistor to +3.3V.

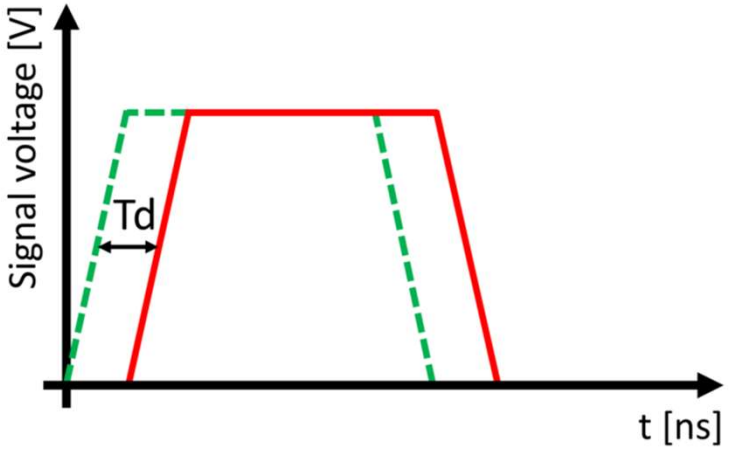
Noise (HF) - decoupling



Low impedance connection to GND, to keep the 50 Ω Impedance of the system!

1 GB Ethernet front end design, signal integrity <-> EMC

- Some facts about signals
- Signals with very short rise time, definition and impacts
  - Switching transition (0 ->1 / 1 -> 0) is completed before the signal has travelled along the conductor and reached the load.
  - Signal can be reflected back to the source, which can distort or destroy the original signal. The following signal from the source is already on its way and there is signal mixing between the "old" reflected signal and the already newly transmitted signal.
  - Radiates, couples into neighbouring tracks
    - Interference emission (EMC)
    - Functional impact, malfunction (signal integrity)



  - PCB factors
    - Impedance matching and propagation time, i.e. trace impedance and trace length, must be taken into account.

1 GB Ethernet front end design, signal integrity <-> EMC

- Some facts about signals

- Rule of thumb
  - If the trace is longer than 1/3 of the rise time, reflections may occur.

  - Example
    - Signal rise time at source of 1 ns.
    - PCB: FR4, propagation speed (propagation time): ≈ 15 cm/ns.

    - Critical length of the conductor path on FR4 material: 5 cm (corresponding to 0.33 ns)

In case of data busses like the Ethernet differential pairs.

- Scew, maximum permissible offset t_v [ns] results in a maximum permissible length difference of the tracks ΔL [mm]
  - e.g.: t_v = 0.1 ns -> maximum length difference ΔL
  - Vp (FR4) = 146.28 mm/ns ΔL = (146.28 mm/ns) x 0.1 ns = 14.6 mm
  - The maximum time offset between the signals is given in corresponding specifications.

1 GB Ethernet front end design, signal integrity <-> EMC

- Layout considerations

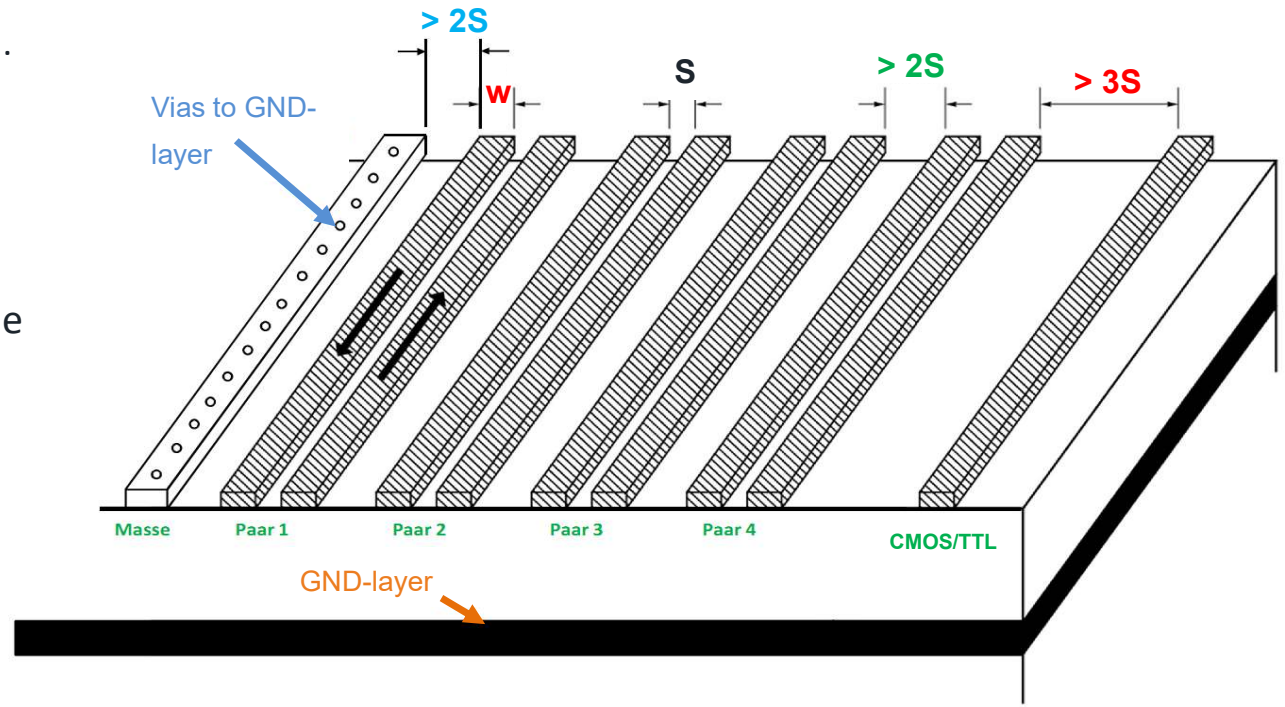
- Use of at least 4-layer PCBs, VCC and GND on the inside.
- Blocking capacitors for the Phy must be placed directly at the IC.
  - 4,7uF/0,1uF/1nF capacitors at each V_{CC}-Pin.
  - The inductance of the traces L < 1,5 nH - 2 nH.

- Distance from other traces to the Ethernet traces **> 3S**, to avoide cross coupling.
- Distance between the Ehternet traces and the ground islands in the same layer **> 2S**.
- Distance between adjacent Ethernet differential pairs **> 2S**.

Dependign on the substrate:

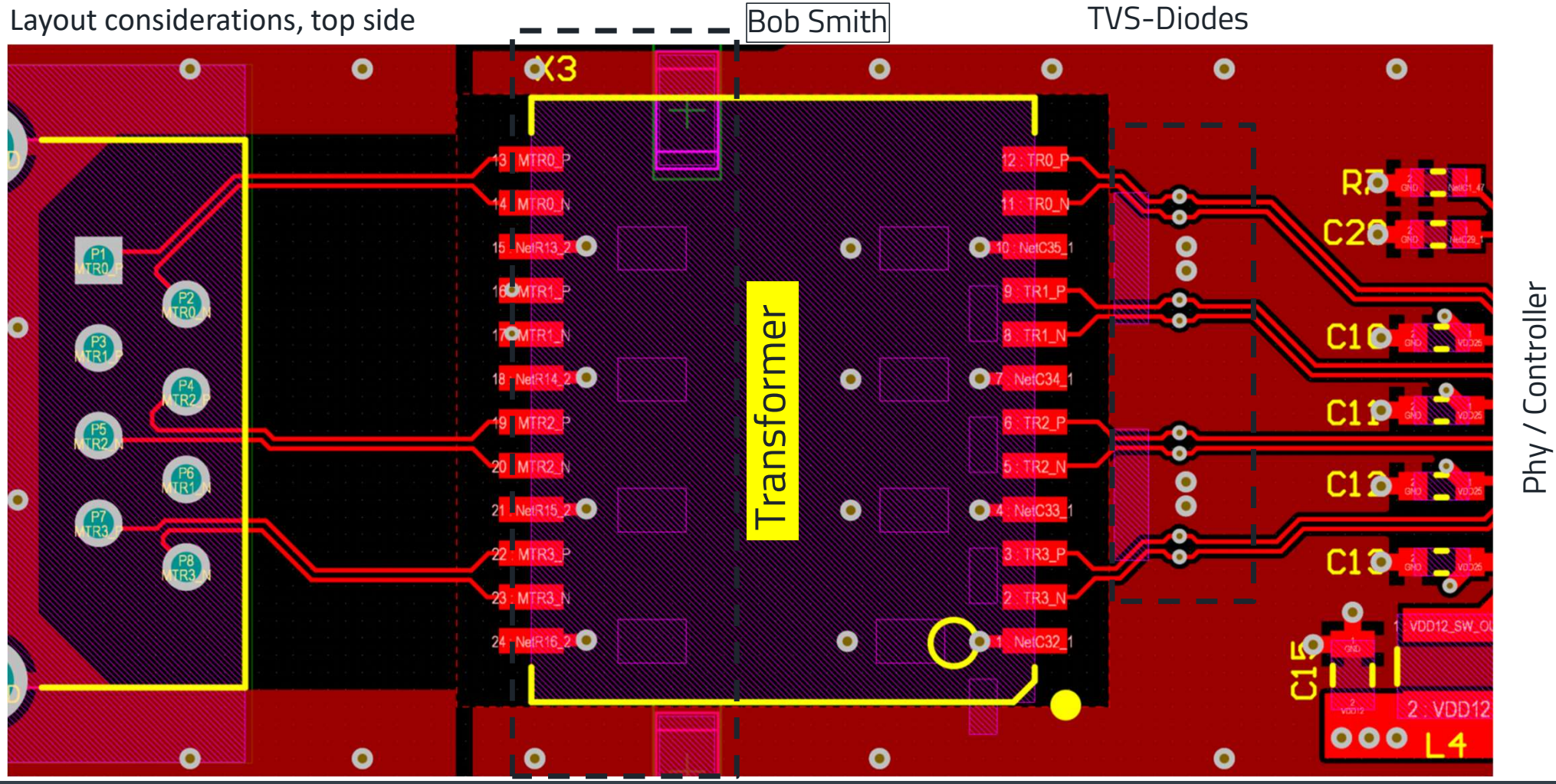
S: 0,125 mm

W: 0,154 mm



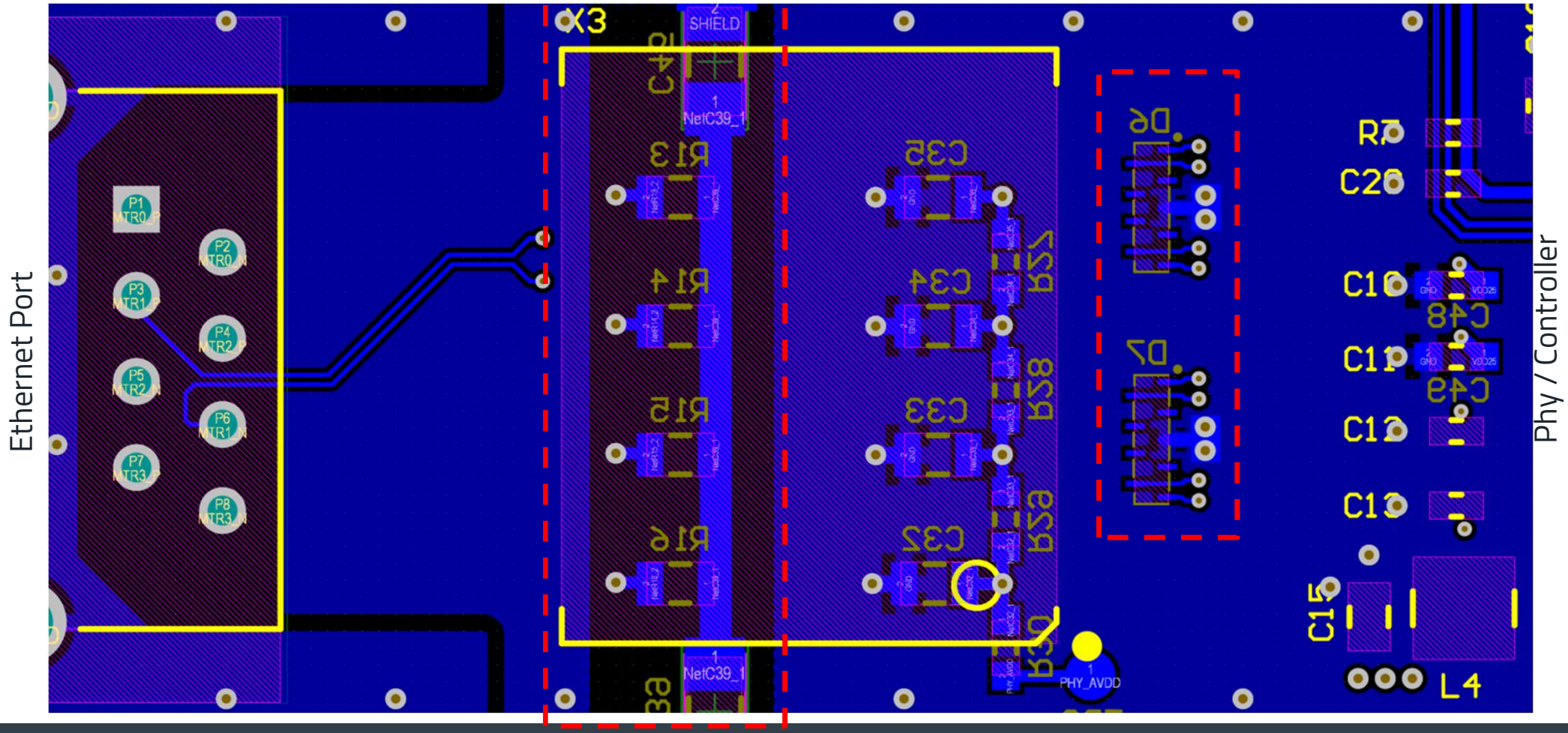
1 GB Ethernet front end design, example of a hardware design

- Layout considerations, top side



1 GB Ethernet front end design, example of a hardware design

- Layout considerations, bottom side

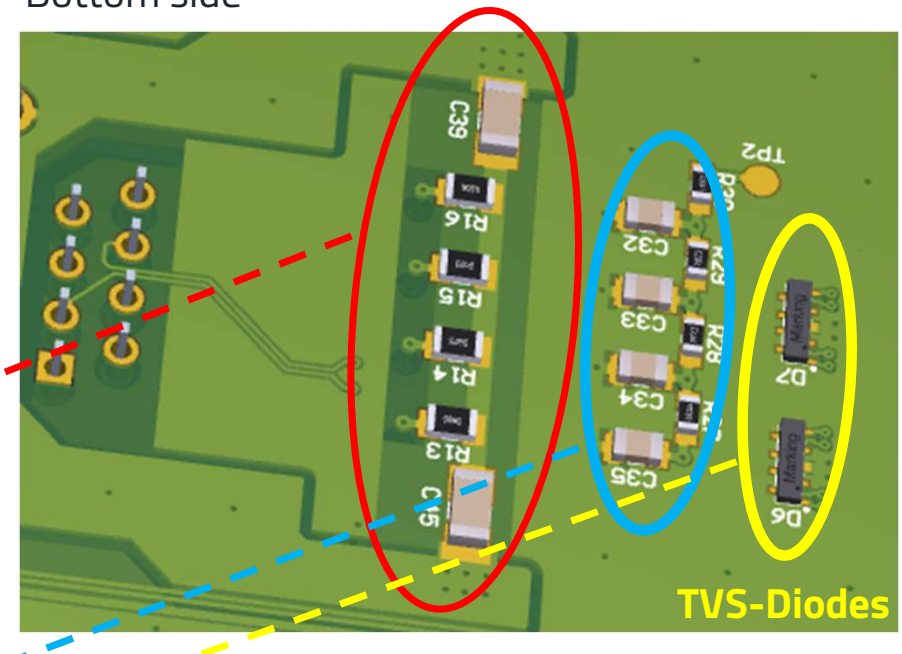


1 GB Ethernet front end design, example of a hardware design

- Layout considerations

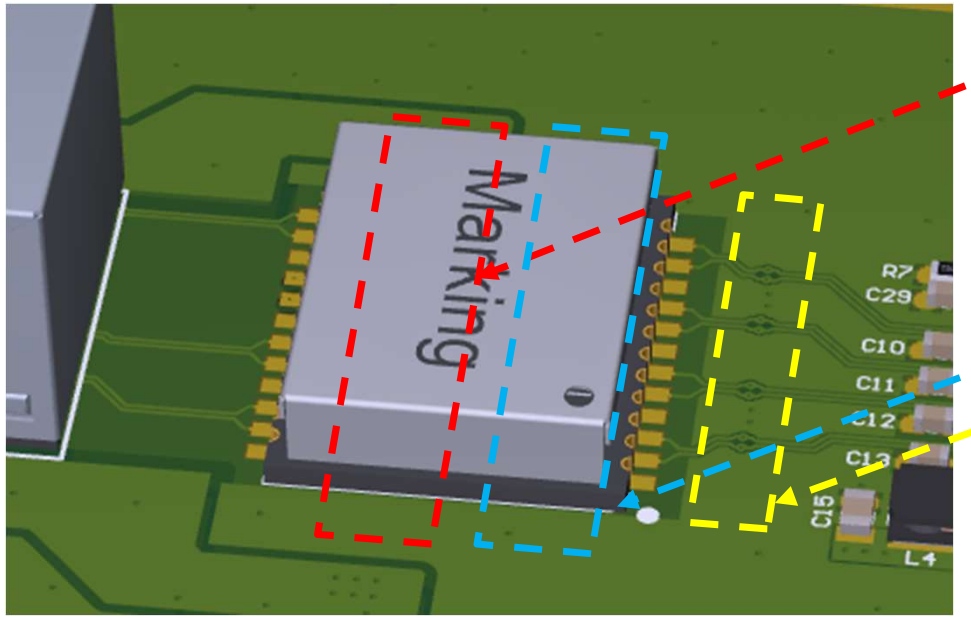
Bottom side

Bob Smith



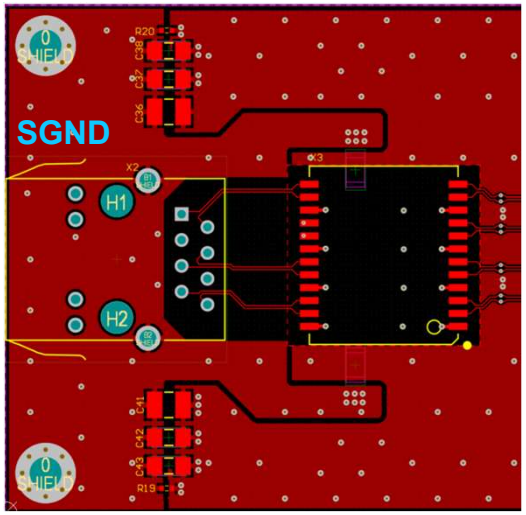
Center Tab decoupling

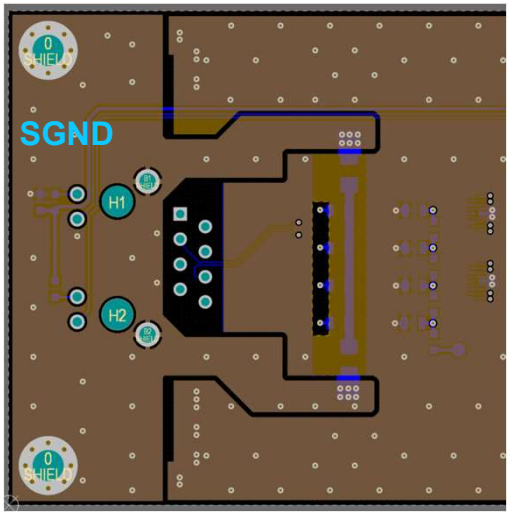
Top side

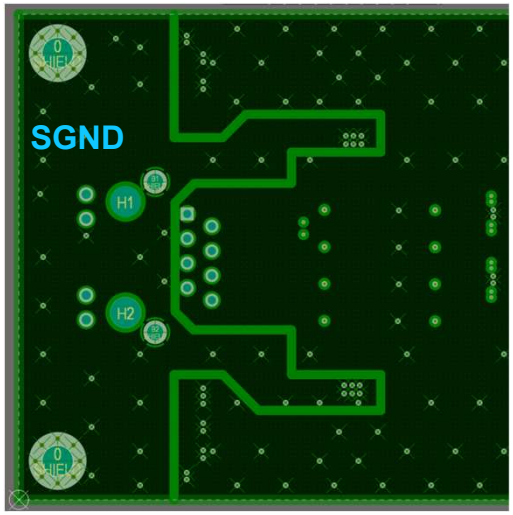


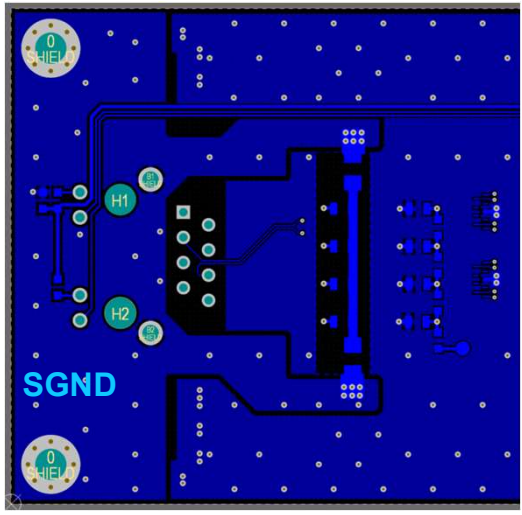
1 GB Ethernet front end design, example of a hardware design

- Layout considerations (1/5)
  - Enclosure/connector ground to electronics GND is separated in all four layers.
  - Do not overlap areas of the enclosure GND (SGND) with other layers.
  - Capacitive coupling as low as possible
    - Ground plane areas plated through (vias) in a grid approx. every 4 mm.
    - Signal lines balanced, differential impedance of 100 Ω against reference ground.
    - Symmetric signal lines: Width of traces: 0,154 mm / distance between traces: 0,125 mm.





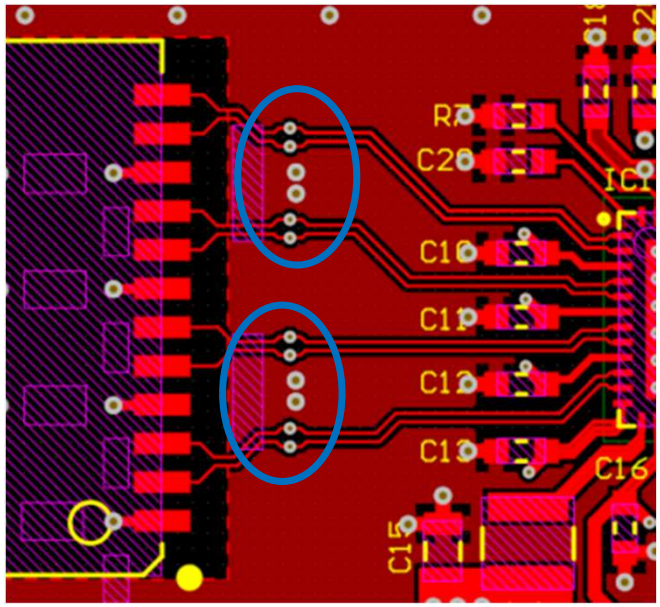




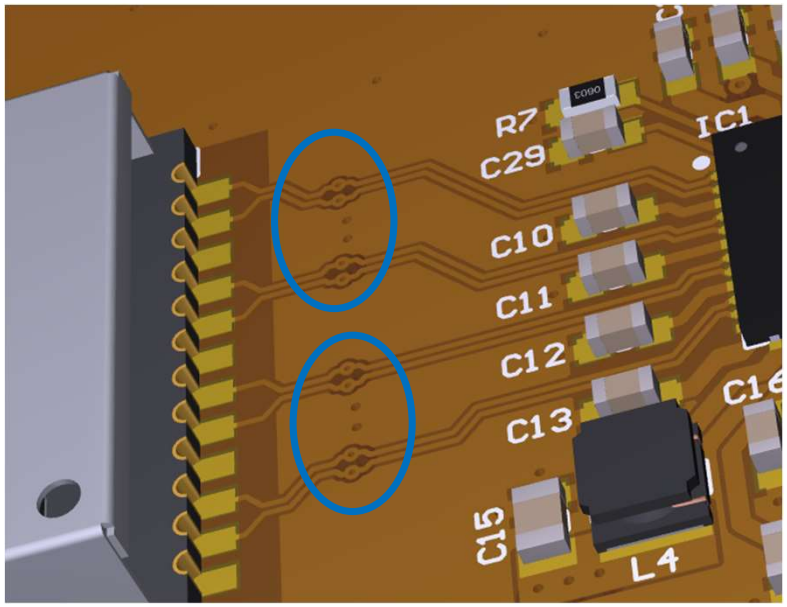
1 GB Ethernet front end design, example of a hardware design

- Layout considerations (2/5)
  - Transformer (X3): Placement directly at the Ethernet socket
  - **TVS arrays**: Connect directly **into the signal path** and against GND

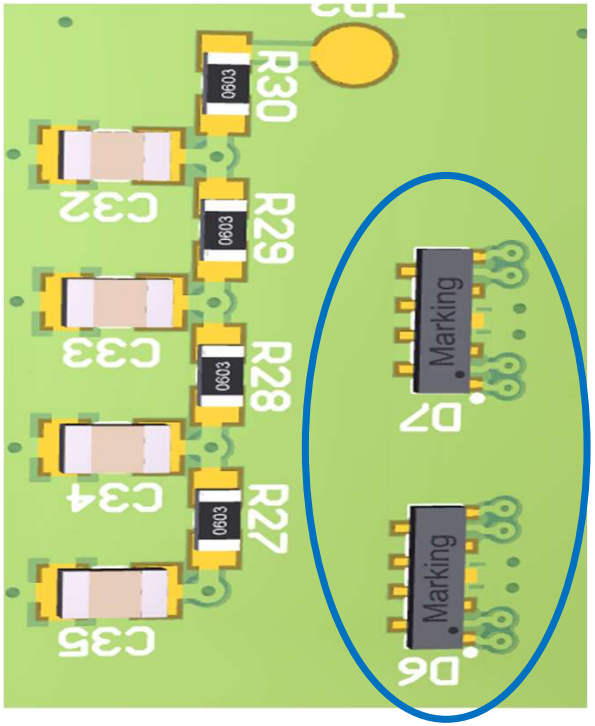
Top



Top 3D view



Bottom



1 GB Ethernet front end design, example of a hardware design

- Layout considerations (3/5)
  - Layer stacking

#	Name	Material	Type	Weight	Thickness	Dk
	Top Overlay		Overlay			
	Top Solder	Solder Resist	Solder Mask		0.0127mm	3.8
1	**Top Layer**		Signal	1oz	0.035mm	
	Dielectric 1	7628	Prepreg		0.2mm	4.6
2	**GND**		Plane	1/2oz	0.0175mm	
	Dielectric 2	FR4	Core		1.065mm	4.6
3	**Power plane/GND**		Signal	1/2oz	0.0175mm	
	Dielectric 3	7628	Prepreg		0.2mm	4.6
4	**Bottom Layer**		Signal	1oz	0.035mm	
	Bottom Solder	Solder Resist	Solder Mask		0.0127mm	3.8
	Bottom Overlay		Overlay			

1 GB Ethernet front end design, example of a hardware design

- Layout considerations (4/5)
  - Layout Points to Note – Summary (1/2)

    - Each TRxP/TRxN signal group should be routed as a **differential trace pair**. This includes the entire length of the traces from the RJ45 connector to the Phy. The differential pairs should be **as short as possible** and have a differential impedance of 100 Ω, i.e. 50 Ω each to ground.

    - A single differential pair should be **routed as close to each other as possible**. Typically, the smallest trace spacing (0.1 - 0.13 mm) is chosen at the beginning of the impedance calculation. Then the trace width is adjusted to achieve the required impedance. This ensures a **high coupling between the signal pairs**.

    - Differential pairs should be **routed away from all other traces** to avoid coupling to other traces and thus asymmetry. The distance should be at least 4 mm. The intra-pair and inter-pair **offset** between the signal pairs should be **less than 1.3 mm over the entire length**. For optimal noise immunity, each pair should be routed as far apart as possible.

1 GB Ethernet front end design, example of a hardware design

- Layout considerations (5/5)
  - Layout Points to Note – Summary (2/2)

    - For optimal separation, **GND planes** can be inserted **between the differential pairs**. A **distance of 3-5 times the dielectric distance** (distance between the copper layers within the PCB, 0,2mm) should be maintained from this ground plane to one of the tracks, which is here then 0,6 mm to 1,0 mm.

    - The use of vias should be minimised. If vias are used, they must be adjusted so that the **differential pairs remain symmetrical**. Layer changes shall be minimised. The differential pairs must be referenced to the same power supply/ground plane. **Never route across different planes**.

    - When routing the four differential pairs from the Phy to the RJ45 jack, generally at least one pair requires a via to the opposite external plane. In this case, ensure that the routing on the other side of the board (usually layer 4) is via a **adjacent reference plane that has low impedance to ground**.

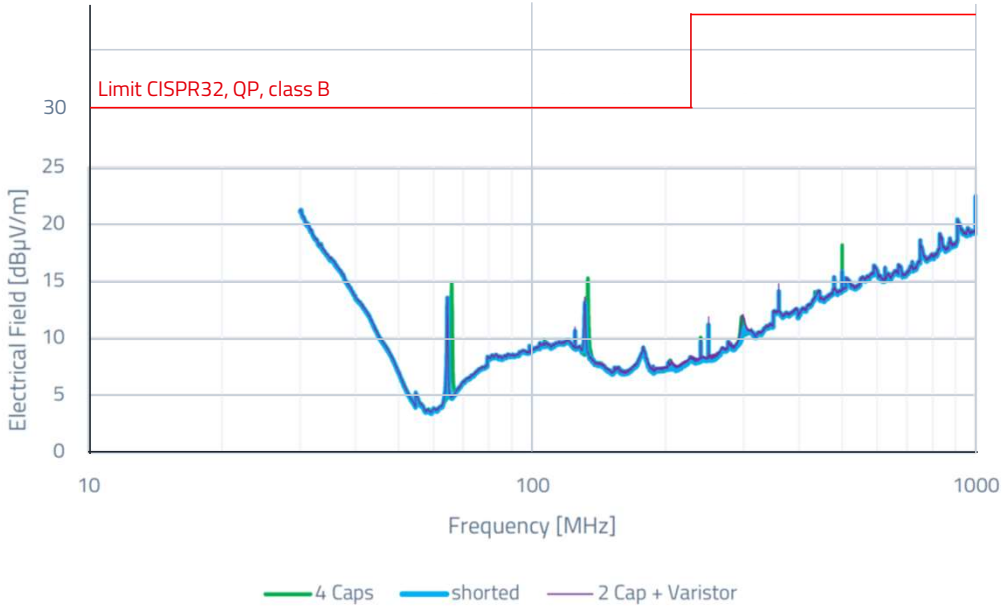
    - Always relate **all impedance terminations** to the **same reference plane as the differential lines**. The resistive terminations, i.e. resistors, should have values with 1.0 % tolerance. All capacitive terminations, i.e. capacitors in the Ethernet front end should have close tolerances and high quality dielectrics.

1 GB Ethernet front end design, example of a hardware design

- EMC, result of radiated emission (CISPR32, limits: 30 MHz to 230 MHz: 30 dBuV/m, 30 MHz to 1 GHz: 37 dBuV/m)

QP horizontal radiated emissions

QP vertical radiated emissions



- Immunity to EN IEC 61000-6-2 VDE 0839-6:2019-11 (industrial levels)
  - Passed

Questions, Comments, Complaints ?