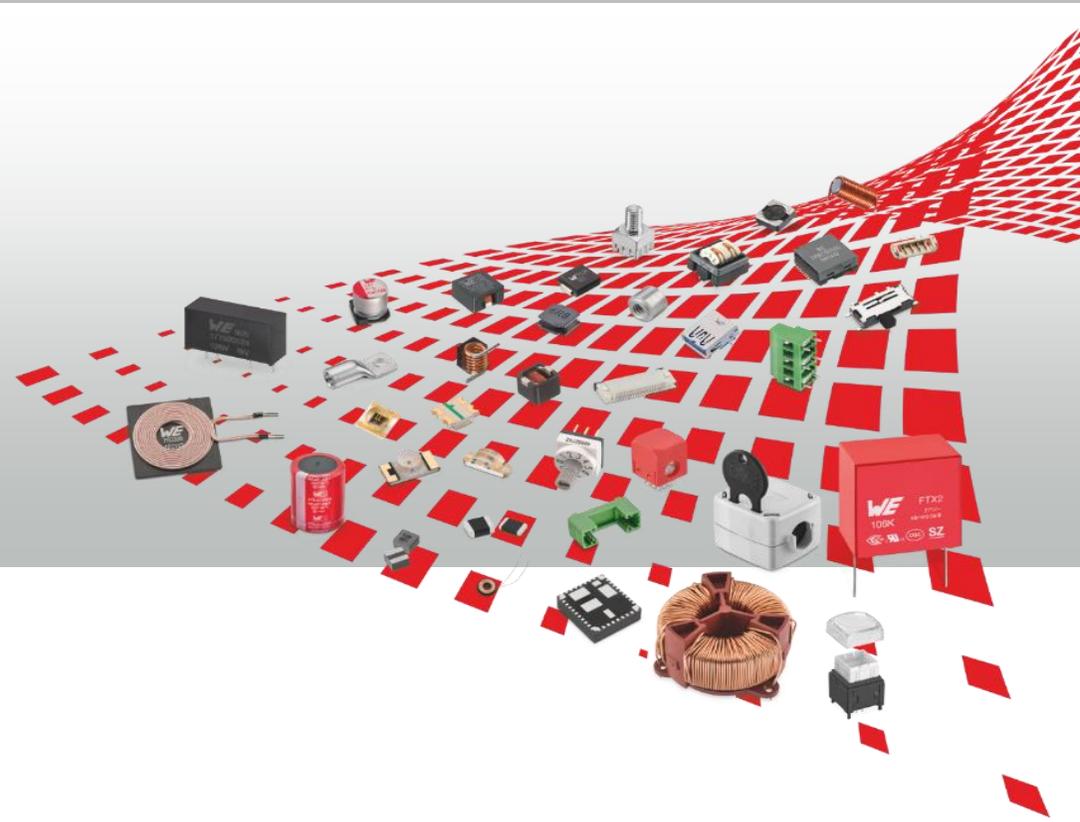


# Anticipate EMC with LTSPICE

more  
than you  
expect



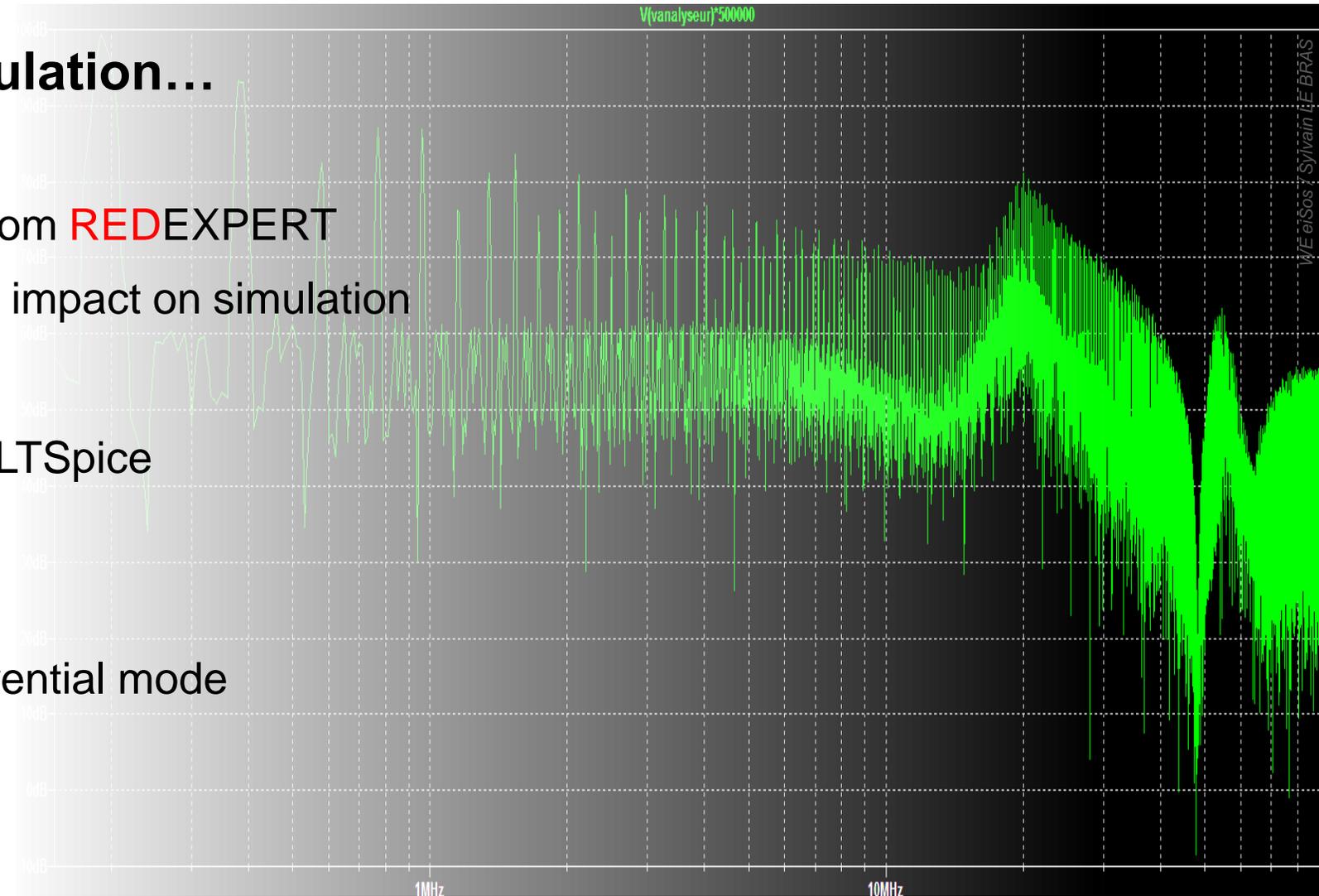
**Sylvain Le Bras**  
Field Application Engineer

[Sylvain.LeBras@we-online.com](mailto:Sylvain.LeBras@we-online.com)

# Anticipate EMC with LTSpice

## Using LTSPICE and Redexpert to check power supply designs

- **Intro : From functional simulation...**
  - Output ripple of a Buck
  - Extracting EMC accurate data from **REDEXPERT**
  - Example of (non) EMC accurate impact on simulation
- **...To EMC simulation**
  - Enabling EMC measurement in LTSpice
  - Getting Seriously Accurate ?
  - Going further with simulation
    - Splitting Common and Differential mode
    - Making simulation look real
  - Examples



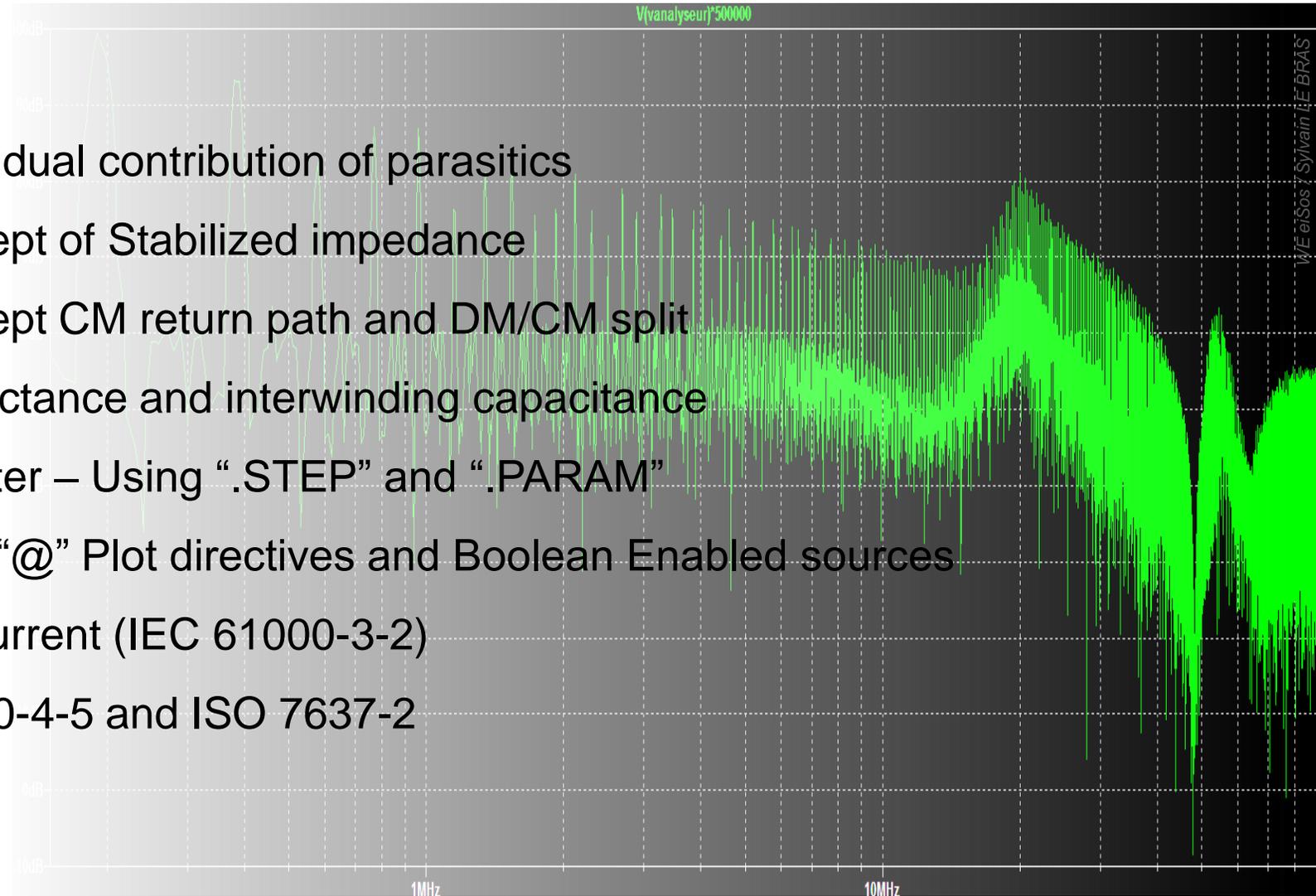
# Anticipate EMC with LTSpice

Using LTSPICE and Redexpert to check power supply designs



## ■ Available examples

1. Output ripple of a Buck – Individual contribution of parasitics
2. Noise at Input of Buck – Concept of Stabilized impedance
3. Noise at Input of Buck – Concept CM return path and DM/CM split
4. Flyback converter – Stray inductance and interwinding capacitance
5. Brushless DC motor and inverter – Using “.STEP” and “.PARAM”
6. Evaluation of filter response – “@” Plot directives and Boolean Enabled sources
7. Power Factor and Harmonic current (IEC 61000-3-2)
8. Surges according to IEC 61000-4-5 and ISO 7637-2



# Setup

## Getting the tools ready



NOW PART OF



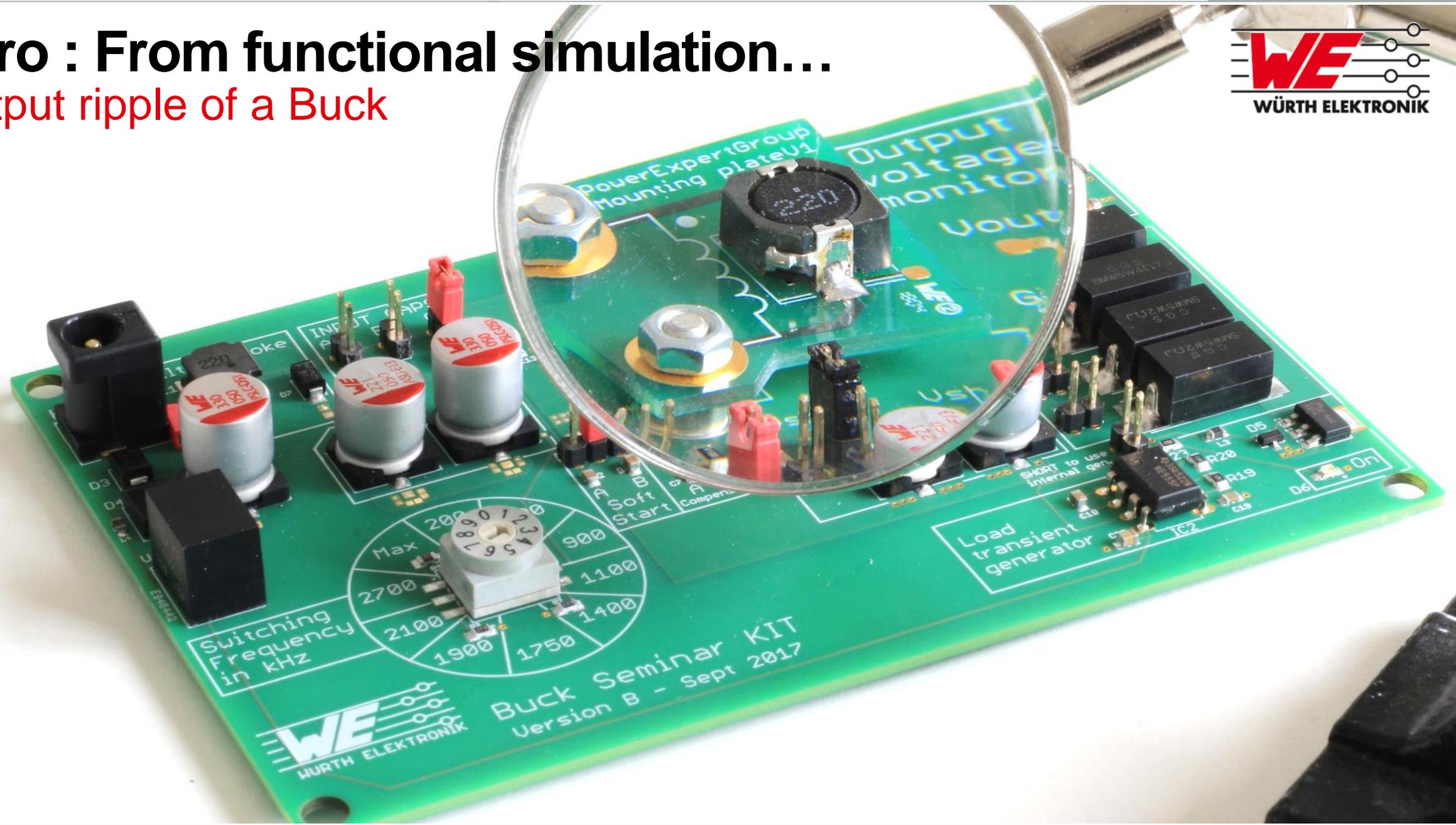
<https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html>

# REDEXPERT

<https://www.we-online.com/redexpert>



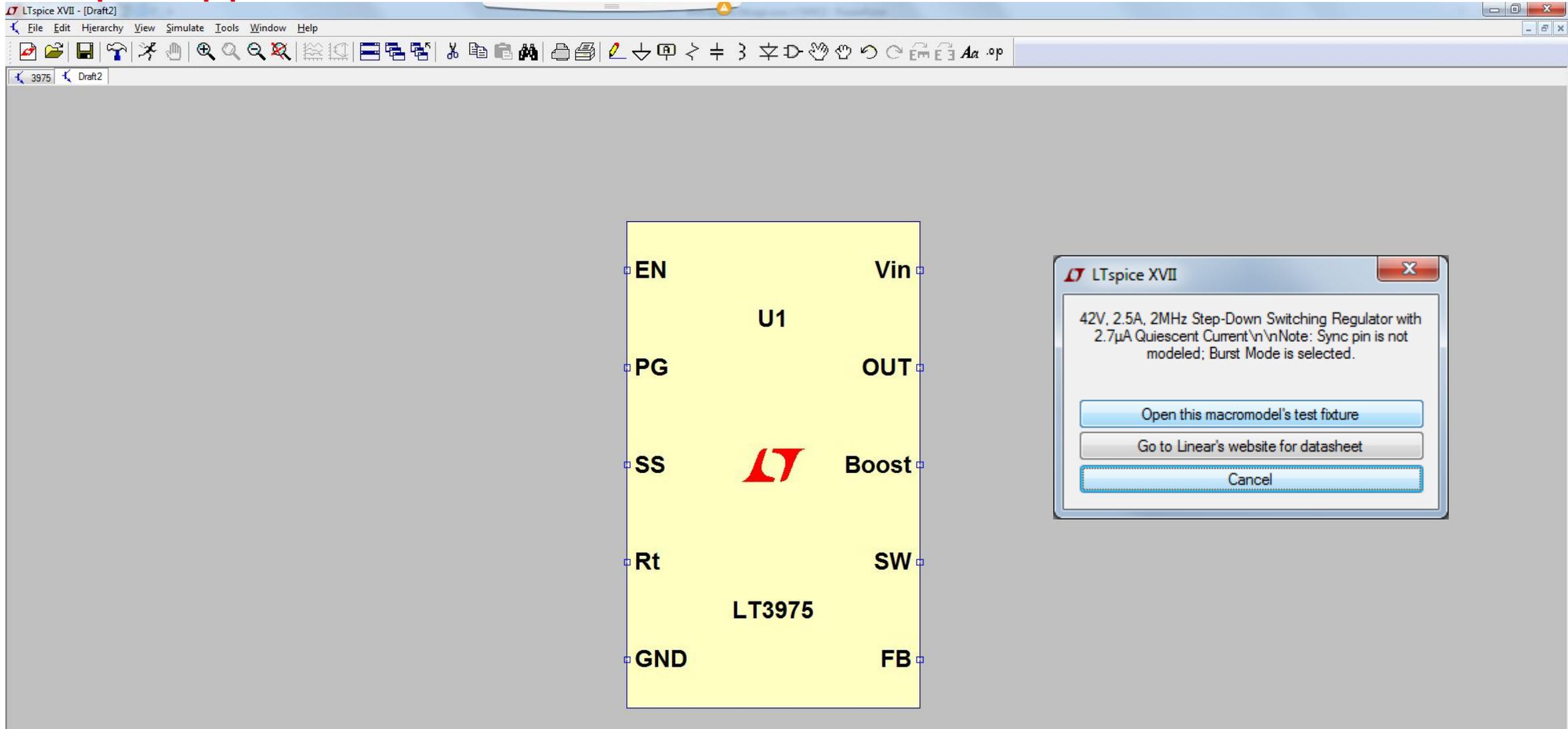
# Intro : From functional simulation... Output ripple of a Buck



WE eiSos / Sylvain LE BRAS

# Intro : From functional simulation...

## Output ripple of a Buck



The screenshot shows the LTspice XVII interface. The main workspace displays a schematic for a regulator component labeled 'U1' and 'LT3975'. The pins are connected as follows:

- EN (Enable) is connected to Vin.
- PG (Power Good) is connected to OUT.
- SS (Soft Start) is connected to Boost.
- Rt (Resistor Timing) is connected to SW.
- GND (Ground) is connected to FB (Feedback).

A dialog box titled 'LTspice XVII' is open, displaying the following text:

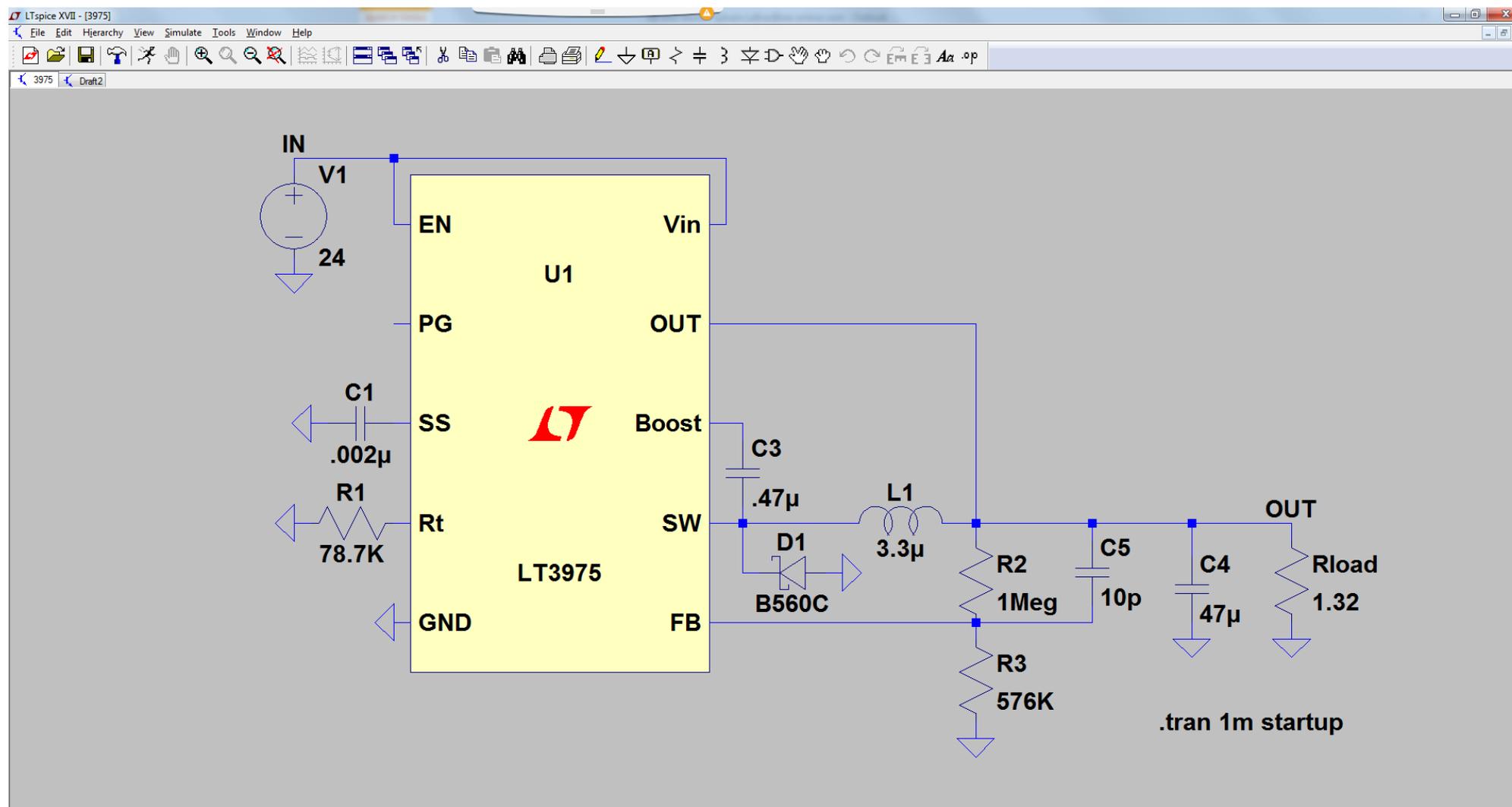
42V, 2.5A, 2MHz Step-Down Switching Regulator with 2.7µA Quiescent Current\n\nNote: Sync pin is not modeled; Burst Mode is selected.

The dialog box contains three buttons:

- Open this macromodel's test fixture
- Go to Linear's website for datasheet
- Cancel

# Intro : From functional simulation...

## Output ripple of a Buck (without the “hardcore mathematics”)

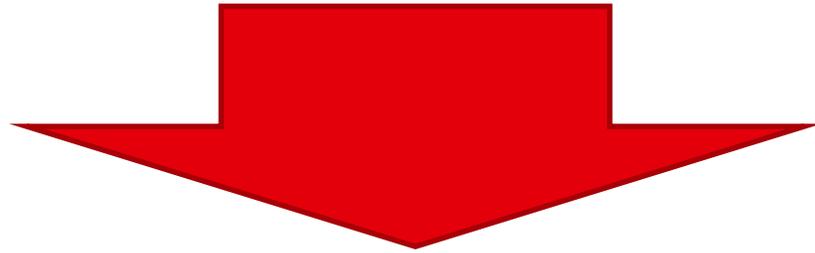


Alternate

# Output ripple of a Buck

Hardcore maths ?

$$V = R \cdot I$$



$$\Delta V = Z_C \cdot \Delta I_L$$

# Output ripple of a Buck

## Redexpert : an ode to laziness



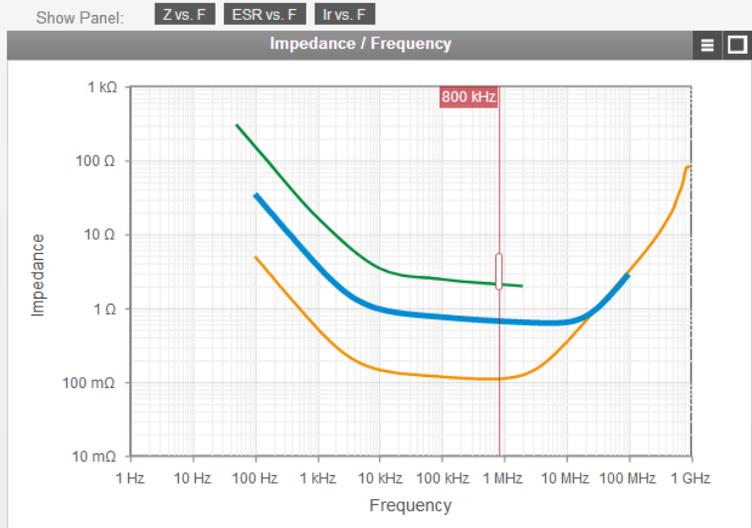
REDEXPERT® ALUMINIUM ELECTROLYTIC CAPACITORS | APPLICATIONS

Order Code	Series	Spec	C
865230440002	WCAP-AS5H		10.0
865230343004	WCAP-AS5H		47.0
865230357007	WCAP-AS5H		330

# Z<sub>C</sub>

2.10 Ω
668 mΩ
110 mΩ

865230343004 WCAP-AS5H 47.0 μF - 16.0 V	865230357007 WCAP-AS5H 330 μF - 16.0 V	865230440002 WCAP-AS5H 10.0 μF - 25.0 V
---	--	---



REDEXPERT® POWER INDUCTORS | APPLIC

### Buck Converter

PARAMETERS				
Input	Output	Switch	Inductor	Diode
24.0 V 19.0-30.0 V	5.00 V 3.00 A	800 kHz	40 % Single	0.30 V

DETAILS		
I <sub>rms</sub>	I <sub>max</sub>	L <sub>opt</sub>
≥ 3.00 A	≥ 3.60 A	4.32 μH

**WE-MAPI - 74438356033**

t <sub>on</sub>	DC	ΔI <sub>L</sub>	I <sub>peak</sub>
273 ns	0.22	1.57 A	3.79 A

# ΔI<sub>L</sub>

# Output ripple of a Buck

## Redexpert : an ode to laziness



REDEXPERT® ALUMINIUM ELECTROLYTIC CAPACITORS | APPLICATIONS | HOW TO | SHARE

ITEMS LE BRAS

Filters: Is selected 3 items

Order Code	Series	Sp...	C	V <sub>R</sub>	Z@800 kHz	DF	Z <sub>max</sub> @ 100kHz	I <sub>ripple</sub> @T <sub>max</sub> °C 120Hz	I <sub>ripple</sub> @T <sub>max</sub> 100kHz	Description	I <sub>leak</sub>
865230440002	WCAP-AS5H		10.0 µF	25.0 V	2.10 Ω	< 16 %		23.0 mA		ASDB055100M025DVCTAE000	3.00
865230343004	WCAP-AS5H		47.0 µF	16.0 V	668 mΩ	< 22 %		50.0 mA		ASDD055470M016DVCTBE000	7.52
865230357007	WCAP-AS5H		330 µF	16.0 V	110 mΩ	< 22 %		300 mA		ASDF105331M016DVCTEE000	52.8

**865230343004**  
WCAP-AS5H  
47.0 µF · 16.0 V

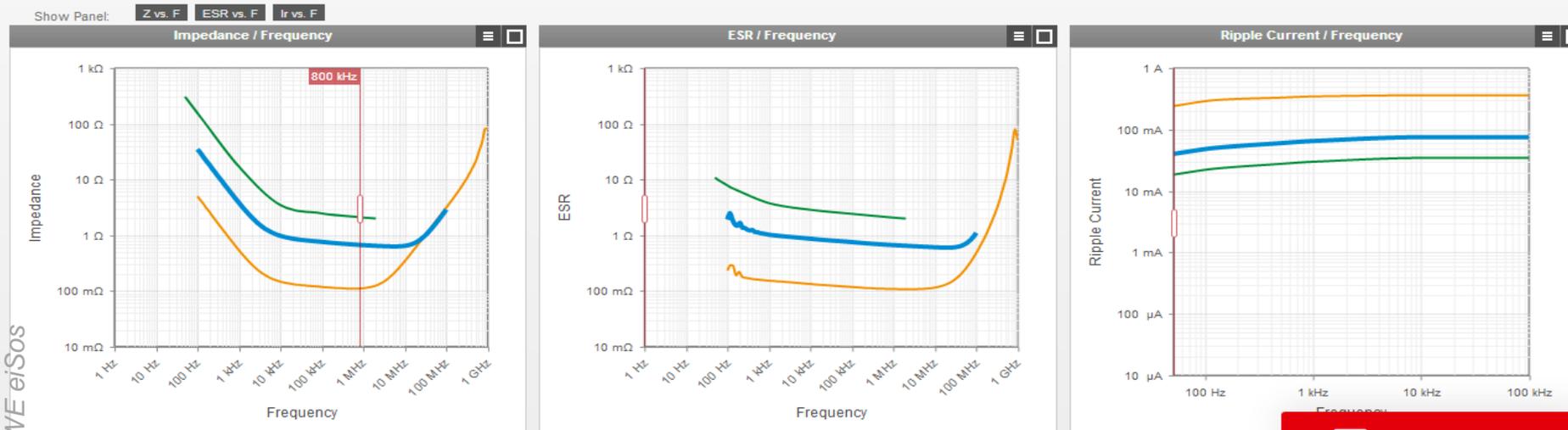
**865230357007**  
WCAP-AS5H  
330 µF · 16.0 V

**865230440002**  
WCAP-AS5H  
10.0 µF · 25.0 V

Click and type or drop an Order Code here

Add to Cart

More...



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[Link](#)

# Output ripple of a Buck

## Redexpert : an ode to laziness



REDEXPERT®

POWER INDUCTORS

APPLICATIONS

HOW TO

SHARE

ITEMS

LE BRAS

**Buck Converter**

PARAMETERS				
Input	Output	Switch	Inductor	Diode
24.0 V 19.0-30.0 V	5.00 V 3.00 A	800 kHz	40 % Single	0.30 V

**DETAILS**

$I_{rms}$ ≥ 3.00 A	$I_{max}$ ≥ 3.60 A	$L_{opt}$ 4.32 $\mu$ H
-----------------------	-----------------------	---------------------------

**WE-MAPI - 74438356033**

$t_{on}$ 273 ns	DC 0.22	$\Delta I_L$ 1.57 A	$I_{peak}$ 3.79 A
--------------------	------------	------------------------	----------------------

AC Losses 179 mW	DC Losses 359 mW	Total Losses 538 mW	$\Delta T_{TOT}$ 42.0 K
---------------------	---------------------	------------------------	----------------------------

P vs.  $V_{in}$

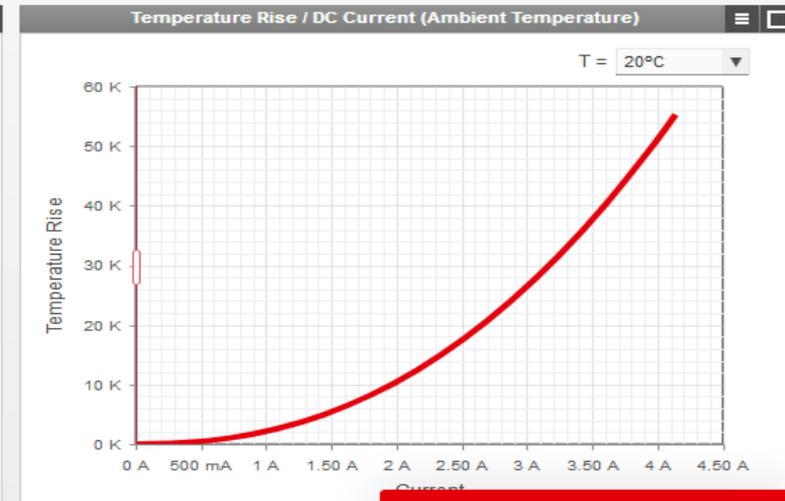
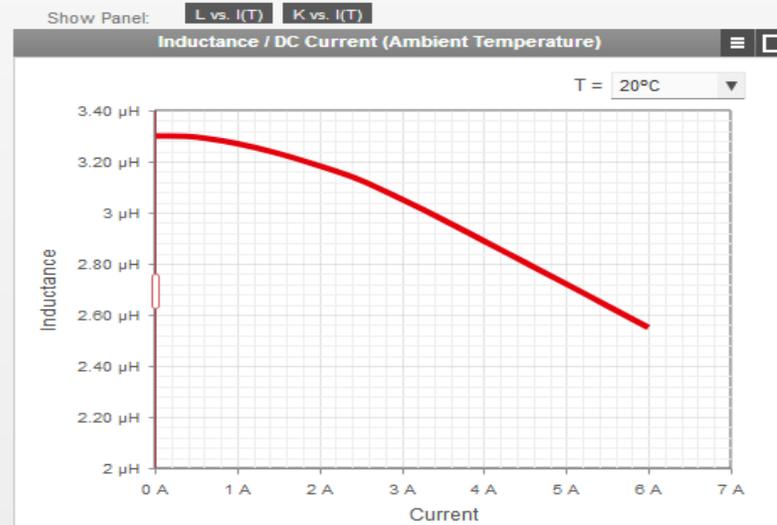
Filters: Type = Single  $I_R \geq 3.00$  A  $I_{sat} \geq 3.60$  A  $3.02 \mu\text{H} \leq L_0 \leq 5.62 \mu\text{H}$

Order Code	Series	Size	Sp...	Type	$L_0$	$R_{DC,typ}$	$I_R$	$I_{sat}$	$P_{AC}$	$P_{DC}$	$P_T$
74438356033	WE-MAPI	4020	PDF	Single	3.30 $\mu$ H	39.9 m $\Omega$	3.60 A	5.50 A	179 mW	359 mW	538 mW
74438357047	WE-MAPI	4030	PDF	Single	4.70 $\mu$ H	39.9 m $\Omega$	3.90 A	6.40 A	102 mW	359 mW	461 mW
74438357056	WE-MAPI	4030	PDF	Single	5.60 $\mu$ H	46.5 m $\Omega$	3.60 A	6.00 A	94.9 mW	418 mW	513 mW
744071039	WE-TPC	8043	PDF	Single	3.90 $\mu$ H	13.0 m $\Omega$	4.90 A	4.50 A	241 mW	117 mW	358 mW
744071047	WE-TPC	8043	PDF	Single	4.70 $\mu$ H	17.0 m $\Omega$	4.80 A	4.30 A	200 mW	153 mW	353 mW
744071056	WE-TPC	8043	PDF	Single	5.60 $\mu$ H	20.0 m $\Omega$	4.00 A	4.00 A	168 mW	180 mW	348 mW

Click and type or drop an Order Code here

Add to Cart

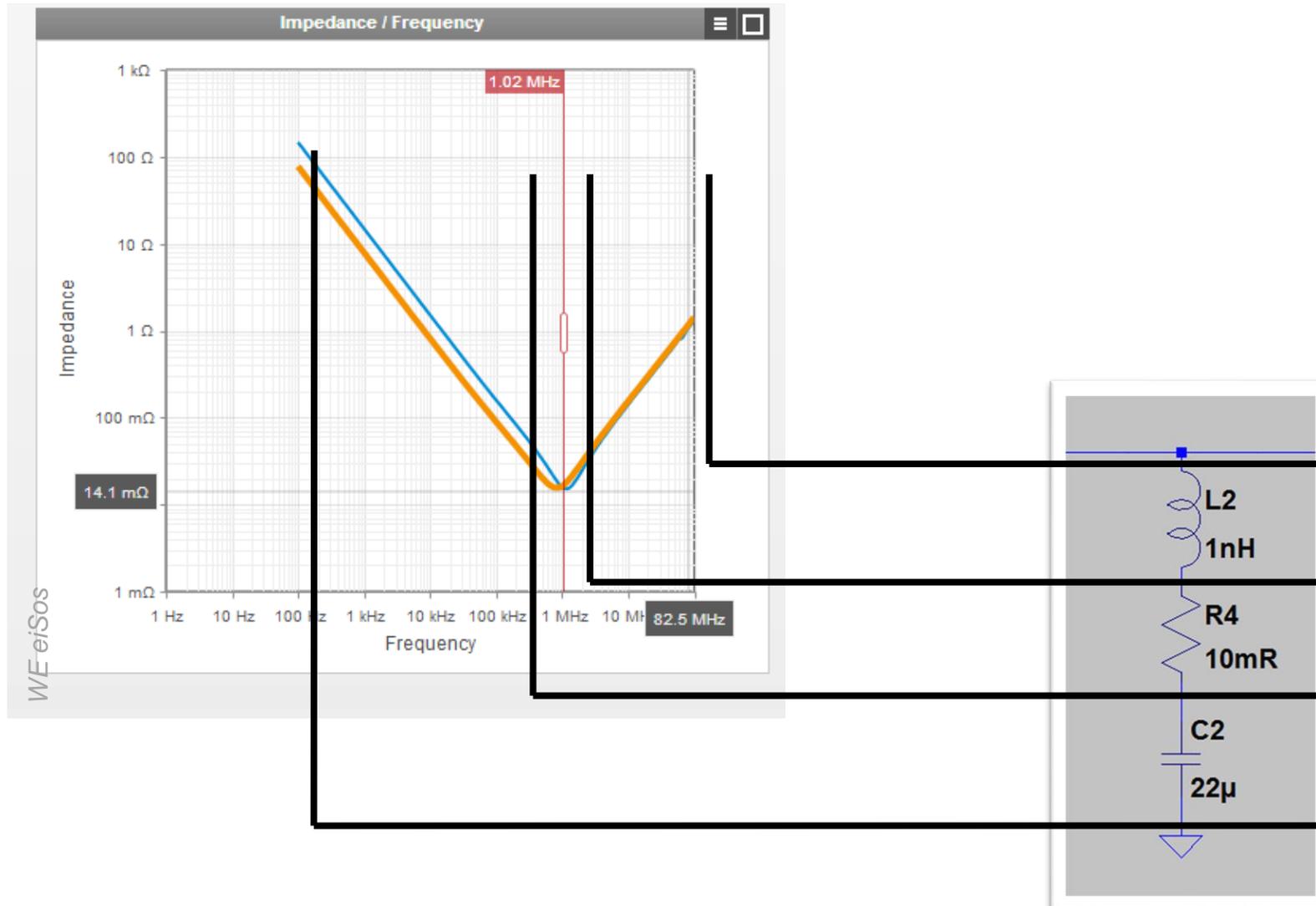
More...



Link

# Output ripple of a Buck

## Extracting EMC accurate data from RED EXPERT



WE eiSos

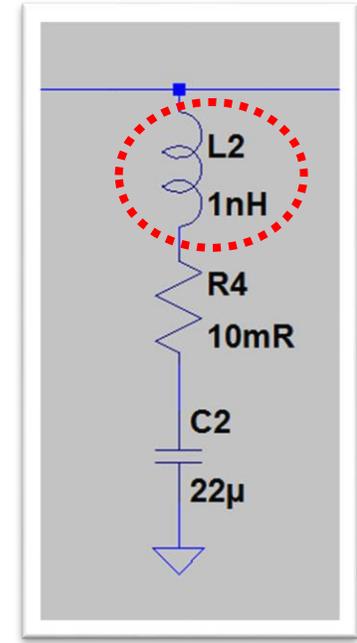
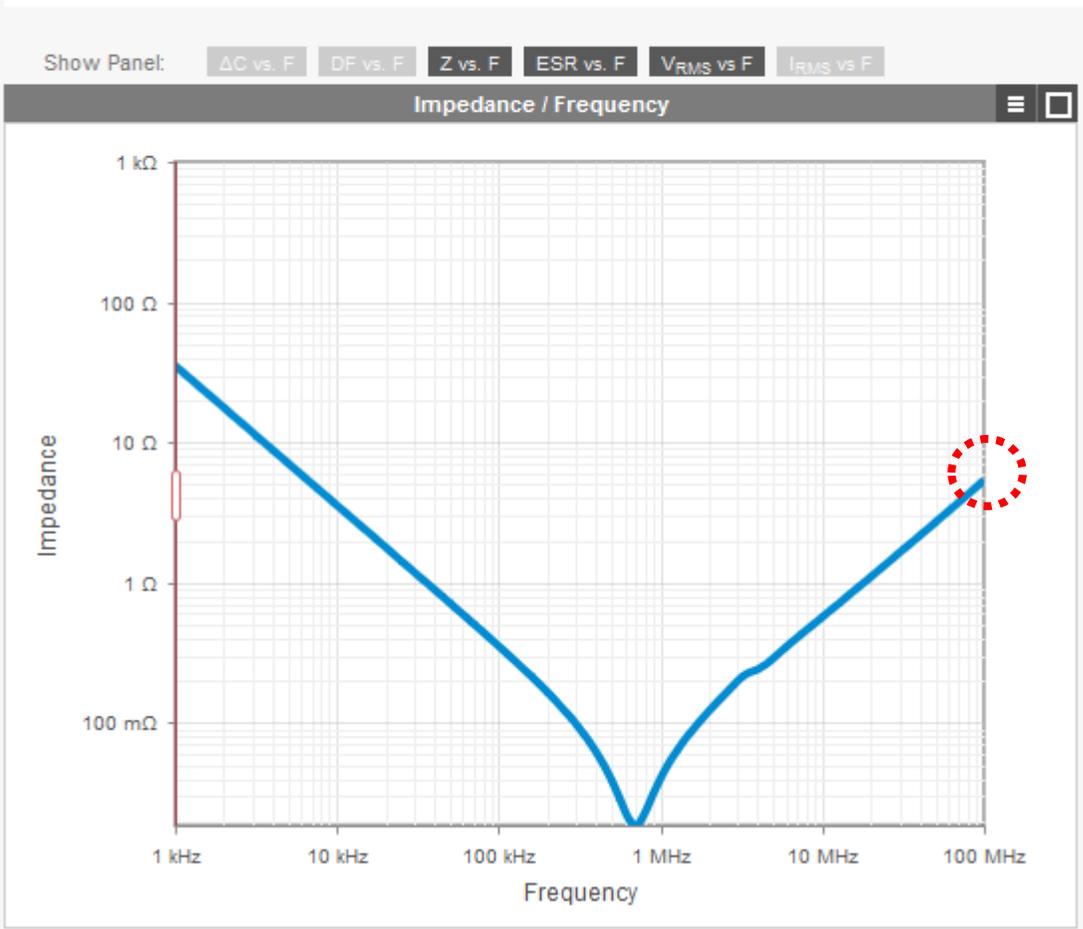


# Output ripple of a Buck

## Extracting EMC accurate data from RED EXPERT

890273427005C\*  
WCAP-FTBE · 27.5 mm  
4.70 µF · 250 V

### ESL identification



$$|Z_L| = L\omega$$

$$\frac{Z_L}{\omega} = L$$

$$L = \frac{|Z_L|}{2\pi F} = \frac{5}{100 \times 10^6 \times 2\pi} \cong 8 \text{ nH}$$

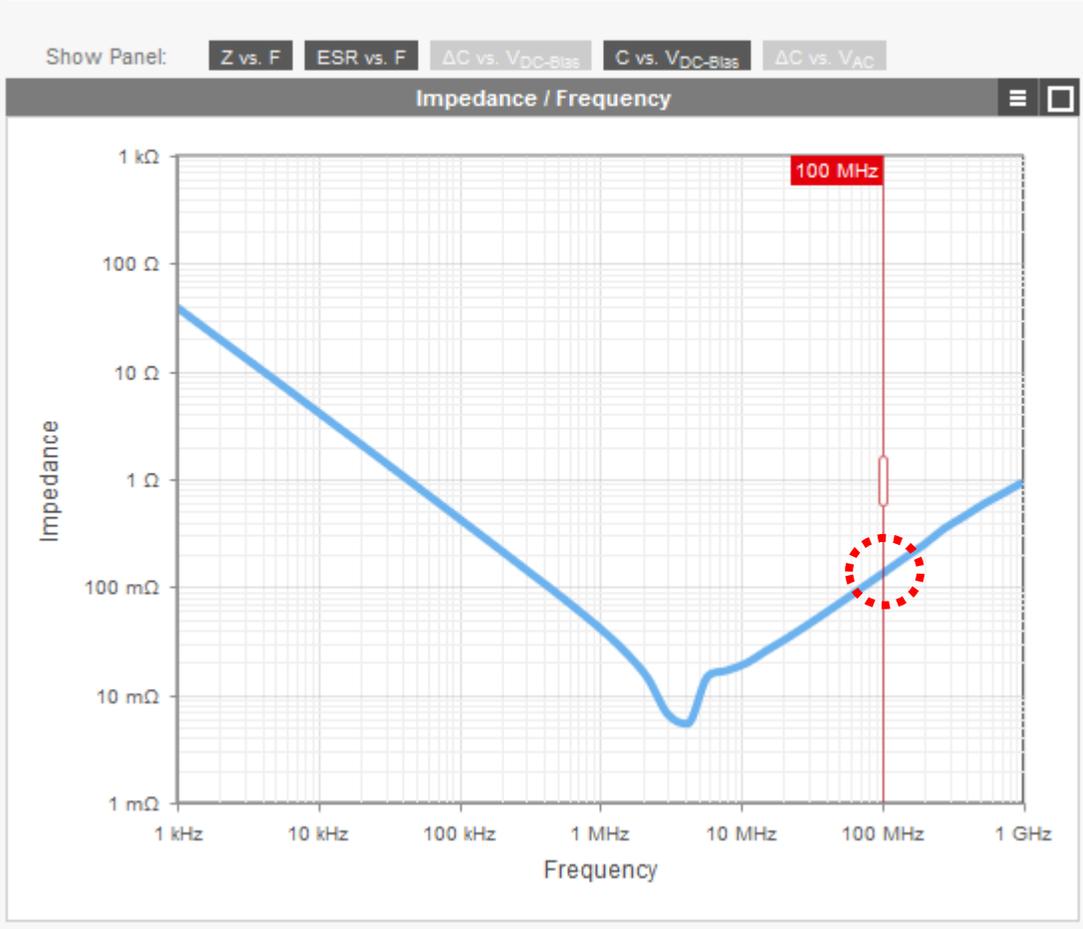


# Output ripple of a Buck

## Extracting EMC accurate data from RED EXPERT

885012107018 ✖  
 WCAP-CSGP · X5R · 0805  
 4.70 µF · 25.0 V

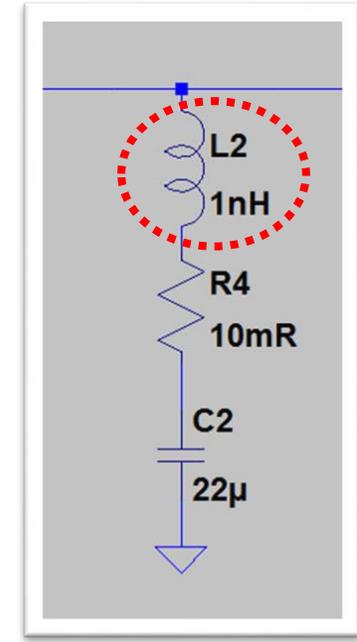
# ESL identification



$$|Z_L| = L\omega$$

$$\frac{Z_L}{\omega} = L$$

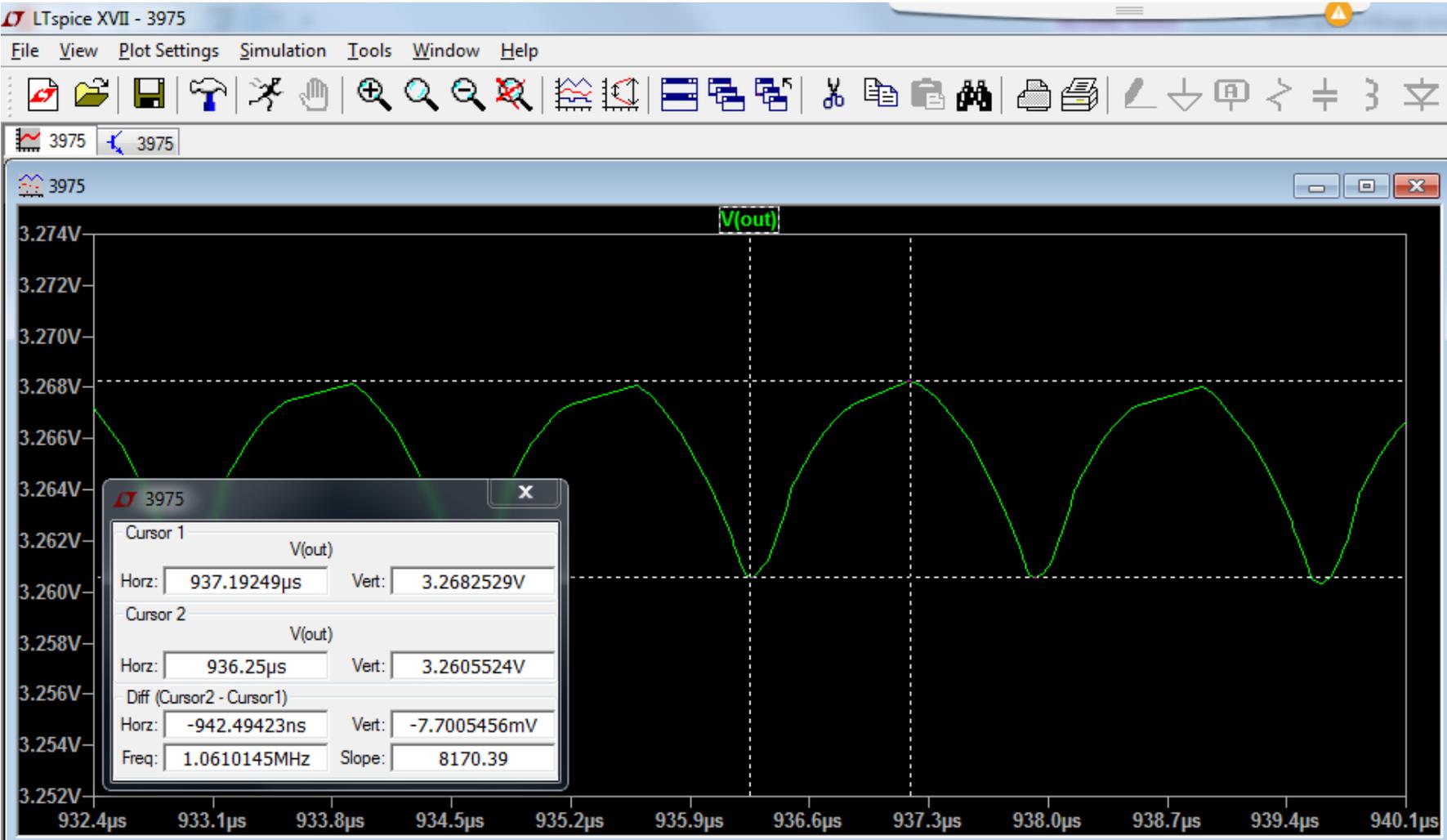
$$L = \frac{|Z_L|}{2\pi F} = \frac{0,132}{100 \times 10^6 \times 2\pi} \cong 0.2 \text{ nH}$$





# Output ripple of a Buck

## Example of (non) EMC accurate impact on simulation



Capacitor - C4

Manufacturer: TDK  
Part Number: C4532X5R0J47@M  
Type: X5R

OK  
Cancel

Select Capacitor

Capacitor Properties

Capacitance[F]: 47µ

Voltage Rating[V]: 6.3

RMS Current Rating[A]: 0

Equiv. Series Resistance[Ω]: 0.002

Equiv. Series Inductance[H]: 0

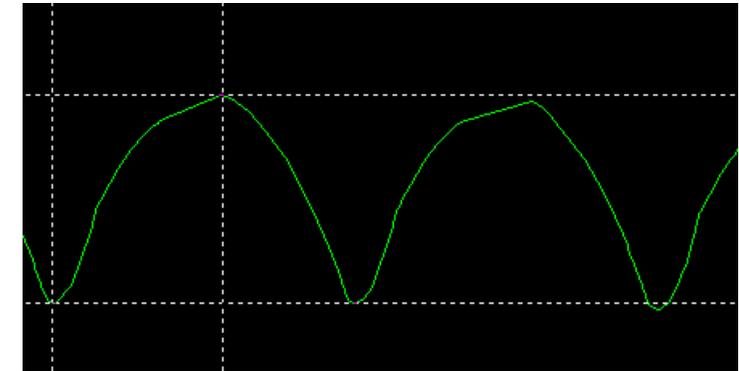
Equiv. Parallel Resistance[Ω]:

Equiv. Parallel Capacitance[F]:

- ESR = 2 mOhms
  - ESL = 0 nH
  - DC bias
- (DC ? Like don't care ?)

# Output ripple of a Buck

Example of (non) EMC accurate impact on simulation





# Output ripple of a Buck

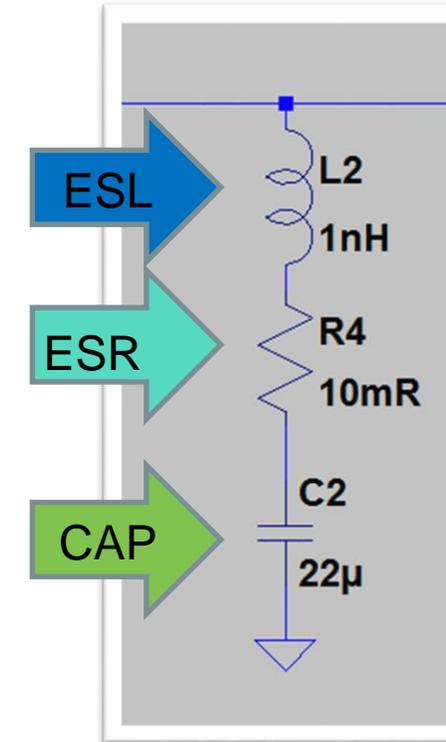
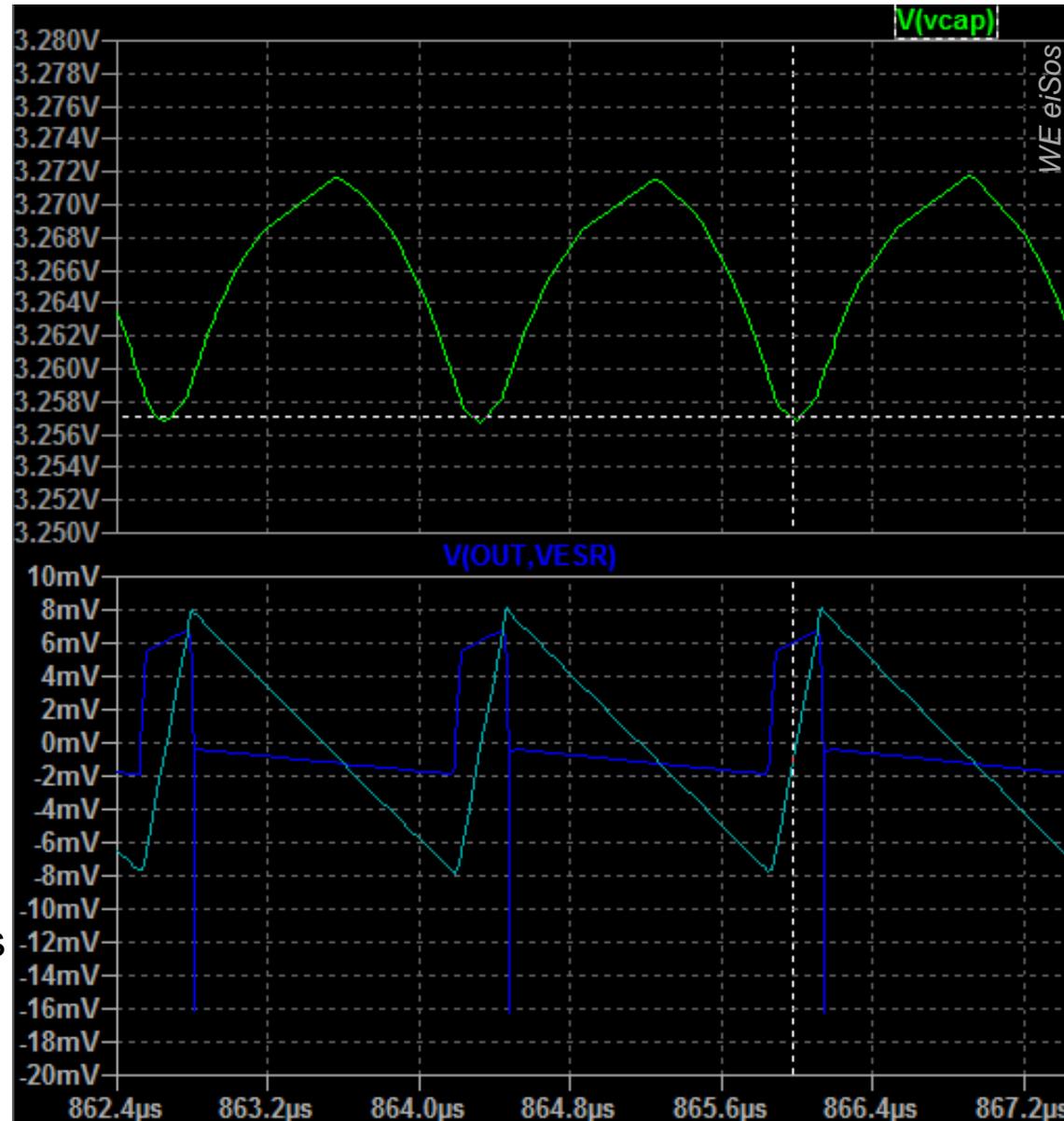
Example of EMC accurate simulation

Charge and discharge of cap

**CAP** →  $14\text{ mV}_{p-p}$

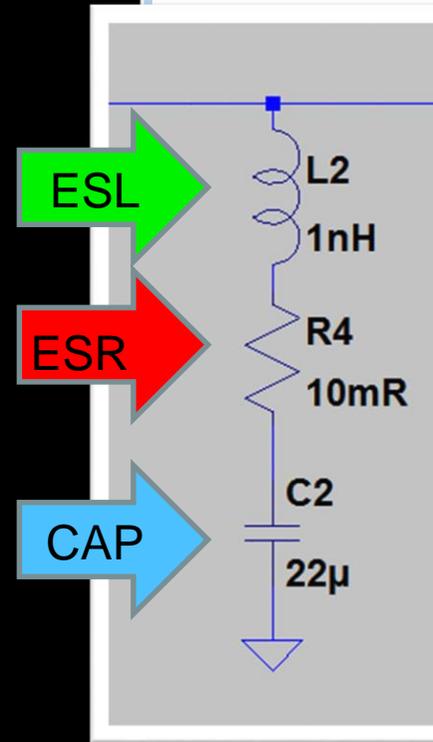
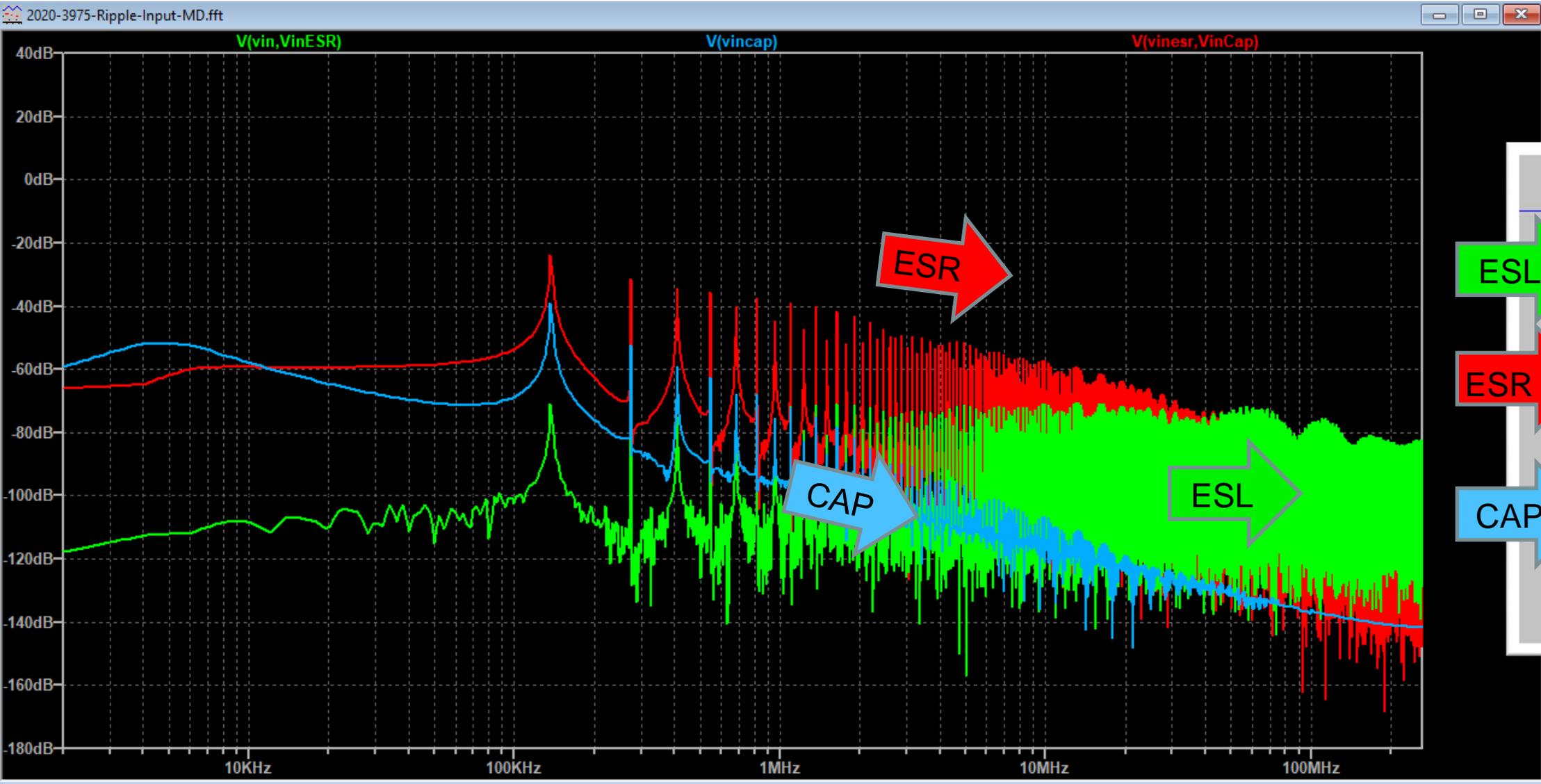
**ESR** →  $16\text{ mV}_{p-p}$

**ESL** →  $10\text{ mV}_{p-p}$  at low frequencies  
 $25\text{ mV}_{p-p}$  at high frequencies



# Capacitor ripple voltage example

## ESR / ESL / CAP breakdown in frequency



# ... To EMC simulation

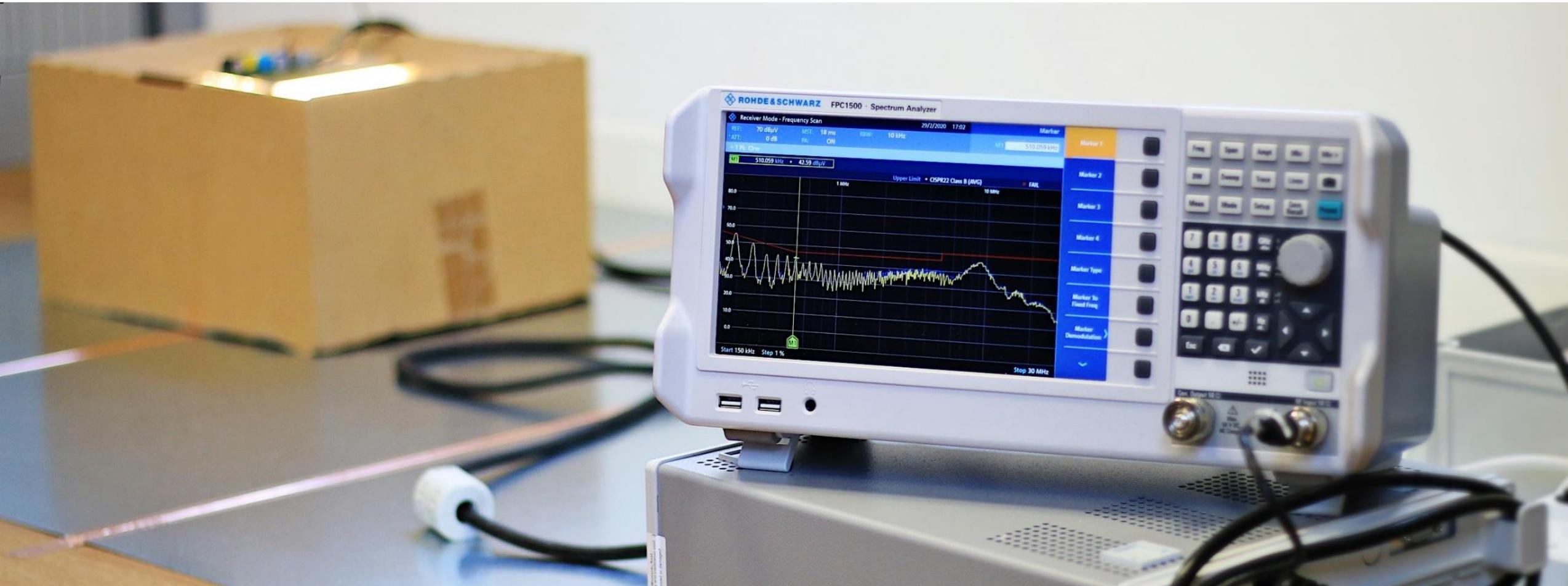
## The missing link



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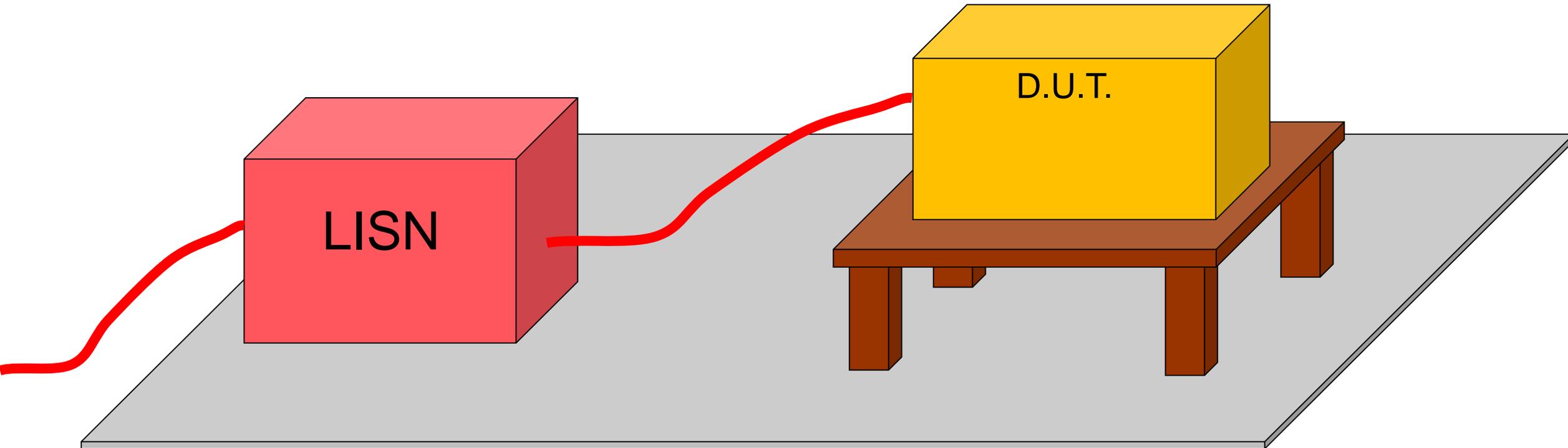
# Enabling EMC accurate measurement in LTSpice

## What is the keystone of conducted emissions ?



# Enabling EMC accurate measurement in LTSpice

What is the keystone of conducted emissions ?

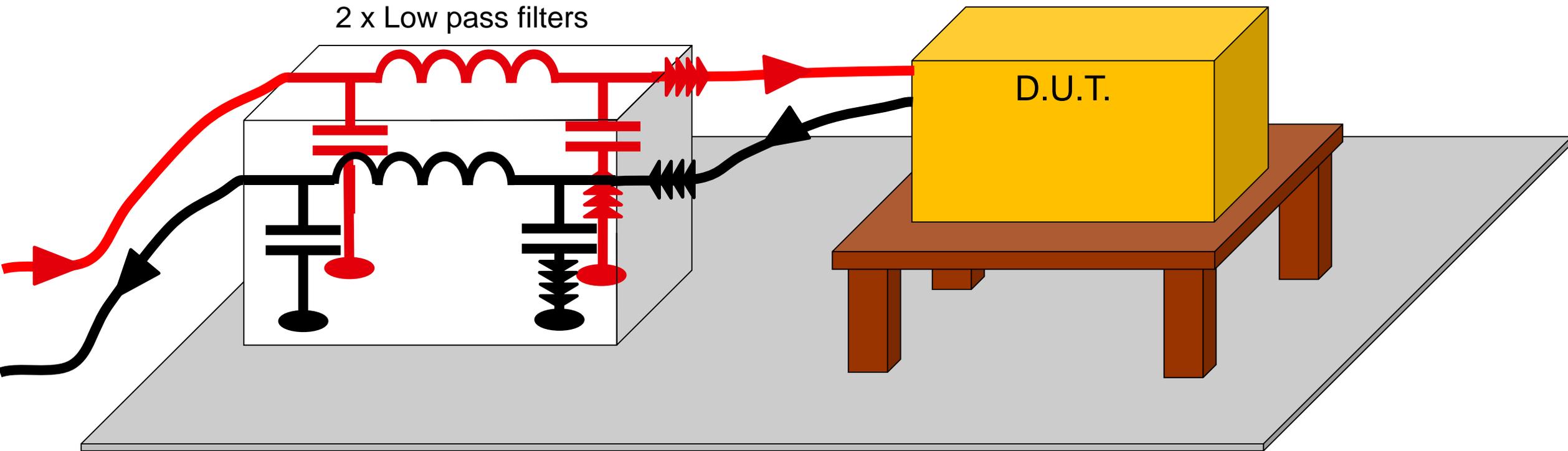


# Enabling EMC accurate measurement in LTSpice

What is the keystone of conducted emissions ?



- ▶ Low Frequency
- ▄▄▄ High Frequency

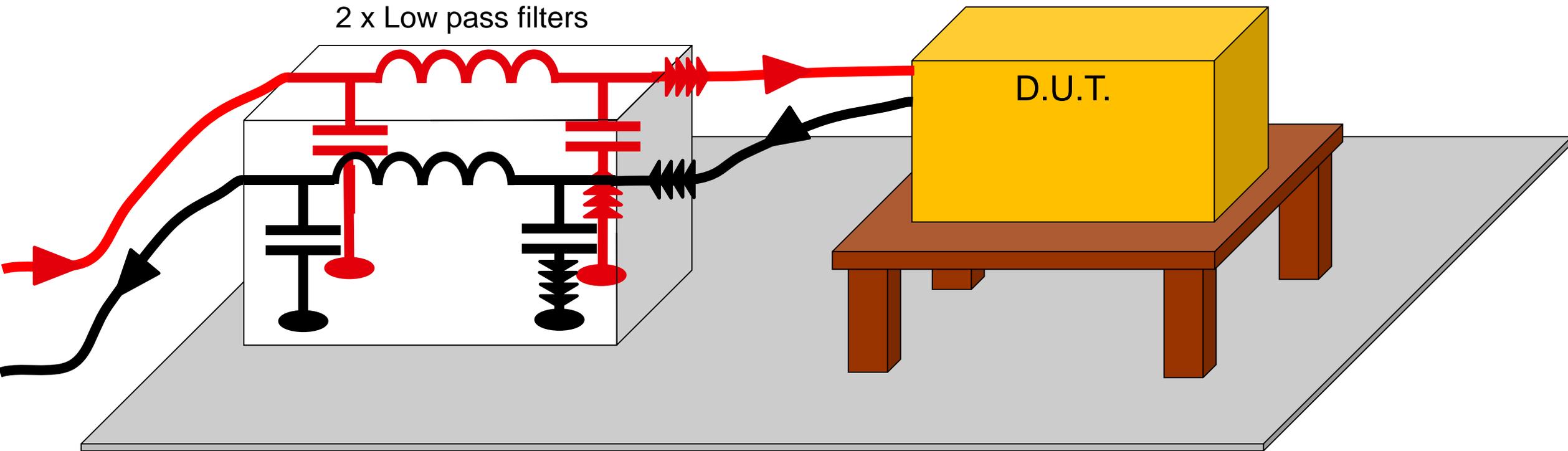


# Enabling EMC accurate measurement in LTSpice

What is the keystone of conducted emissions ?

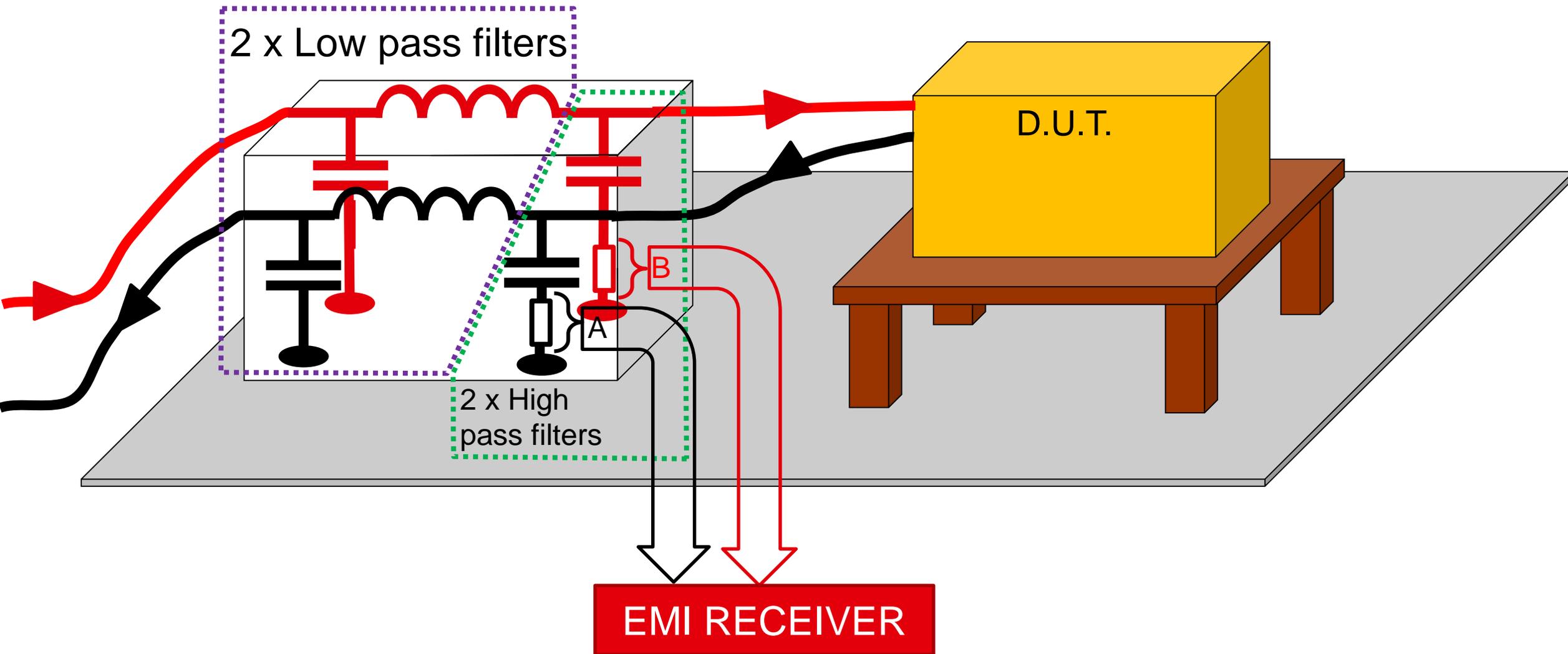


- ▶ Low Frequency
- ▄ High Frequency



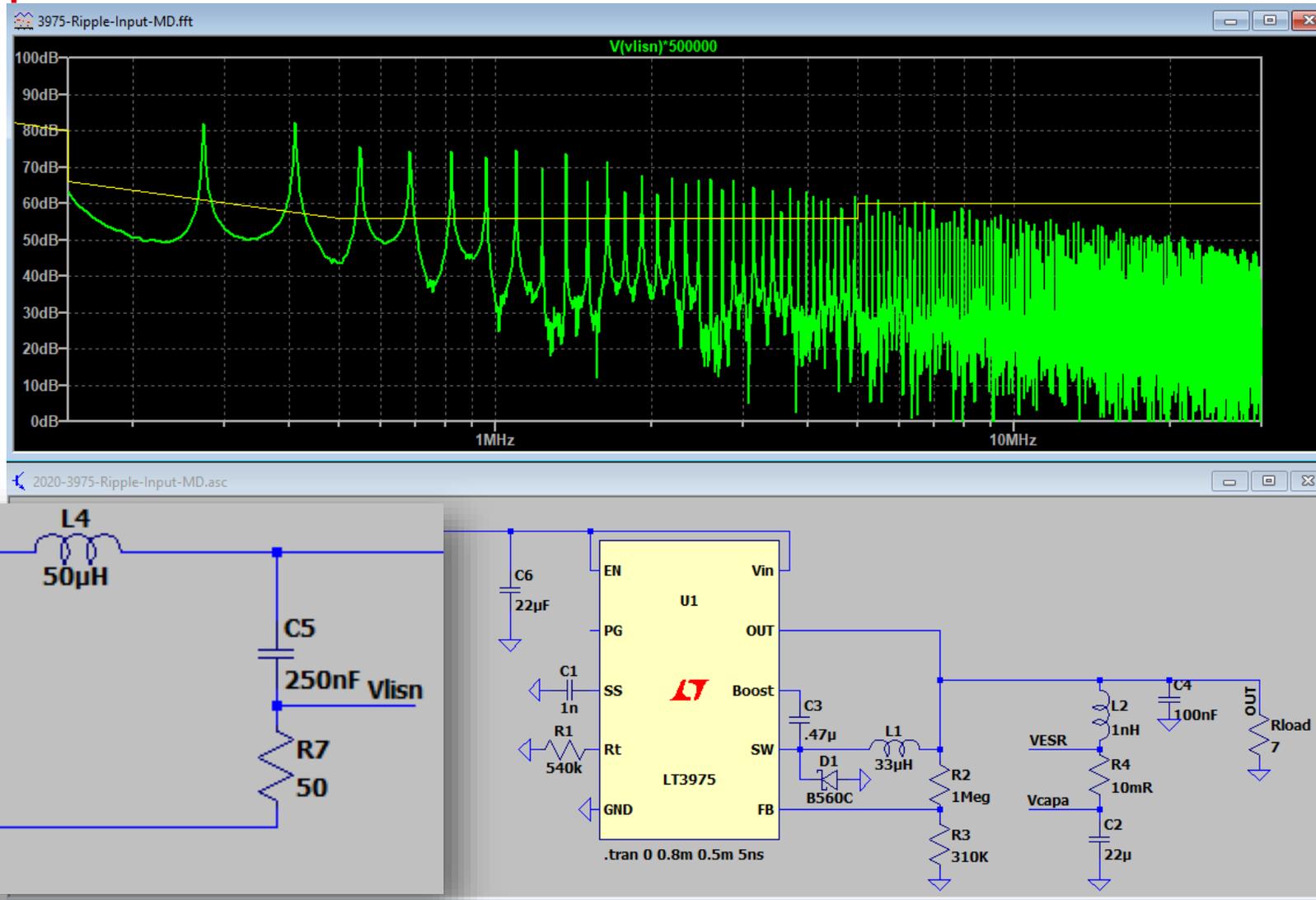
# Enabling EMC accurate measurement in LTSpice

What is the keystone of conducted emissions ?



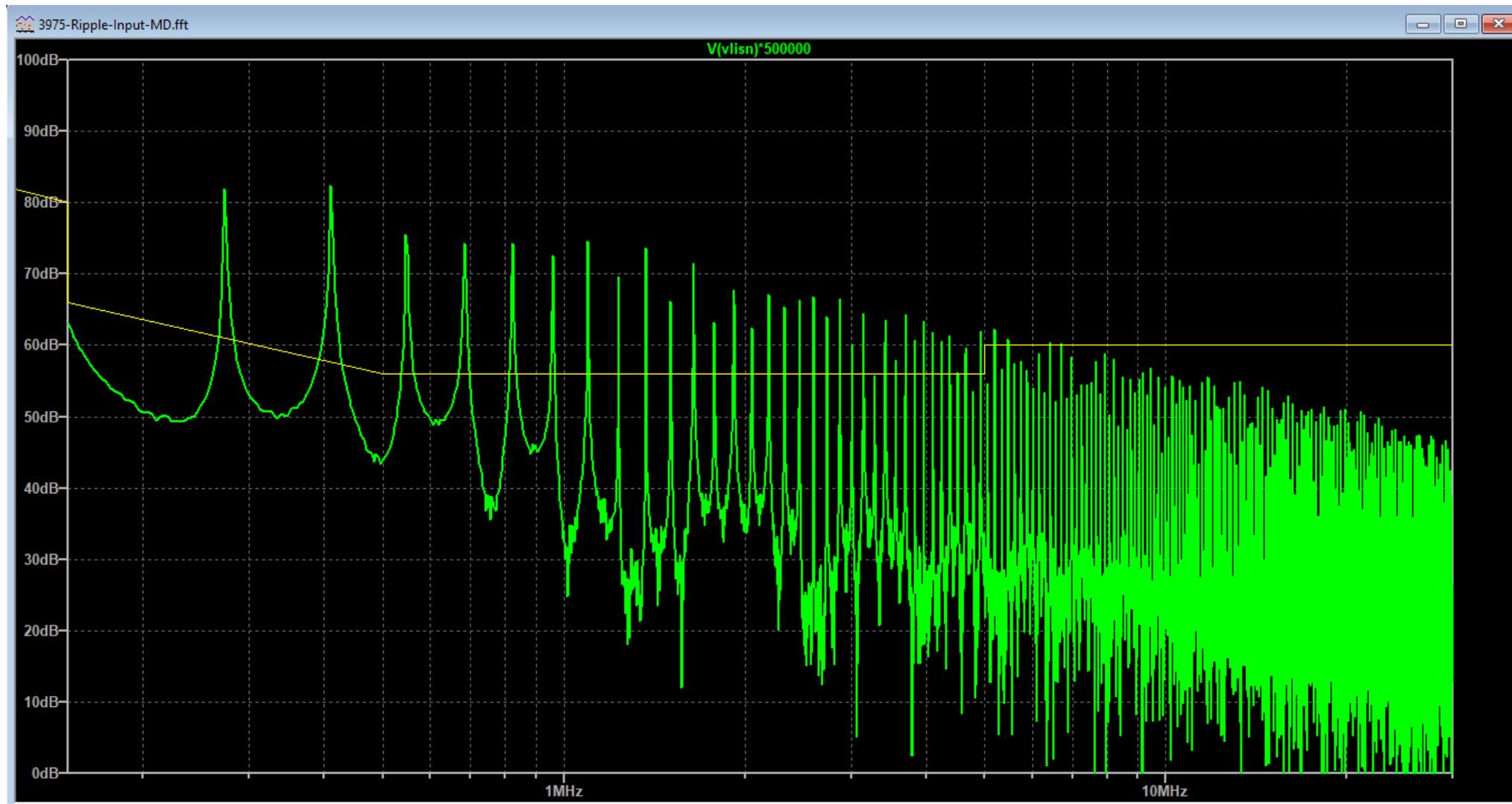
# Enabling EMC accurate measurement in LTSpice

## FFT with simplified LISN



# Reality VS Simulation

## FFT with simplified LISN



# Reality VS Simulation

## Conducted Emissions measurement



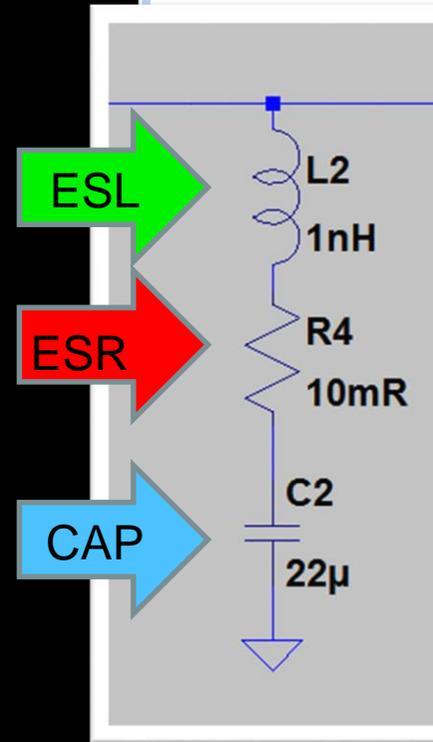
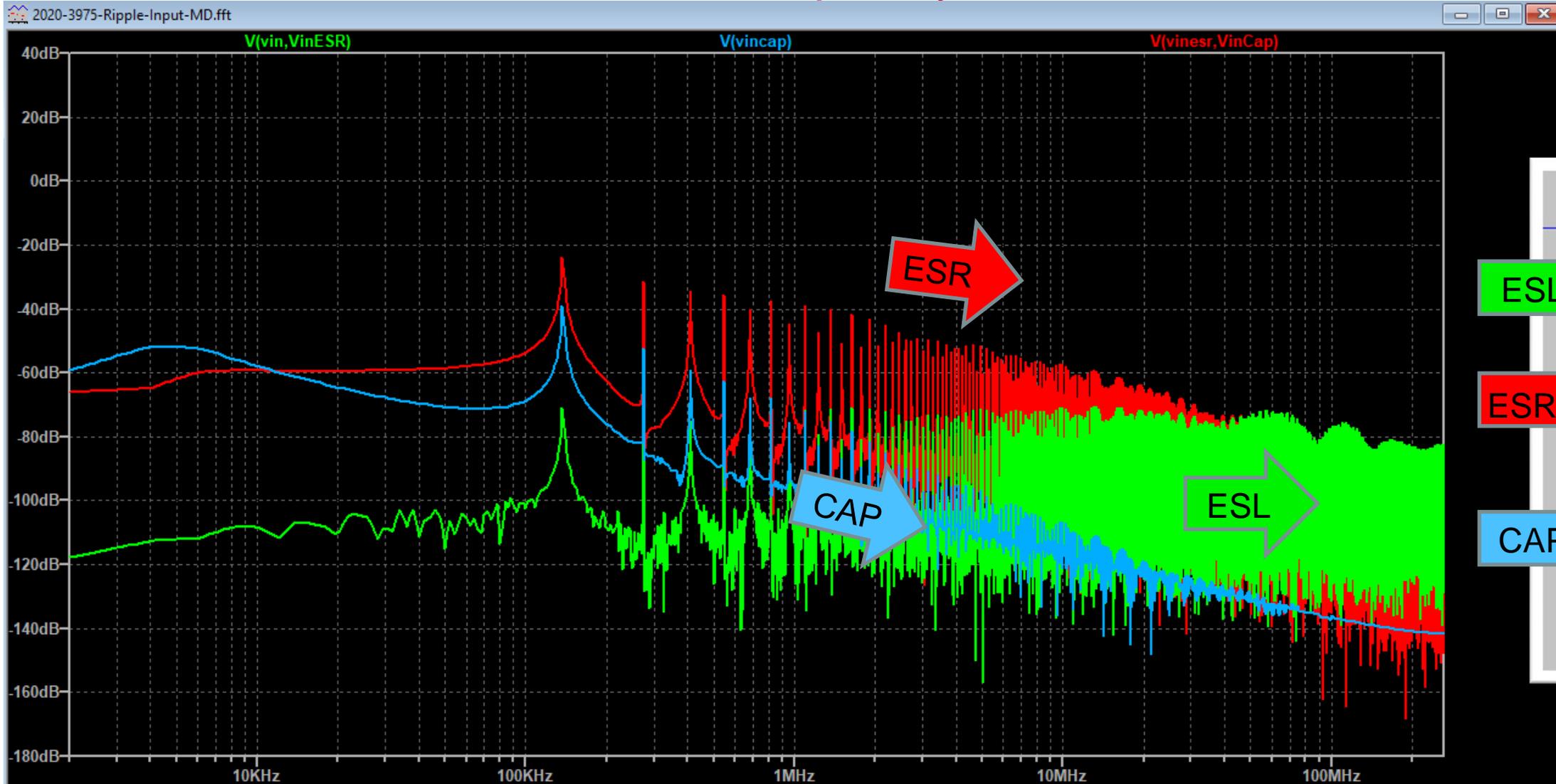
# Reality VS Simulation

## Conducted Emissions measurement



# Reality VS Simulation

## ESR / ESL / CAP breakdown in frequency



# Reality VS Simulation

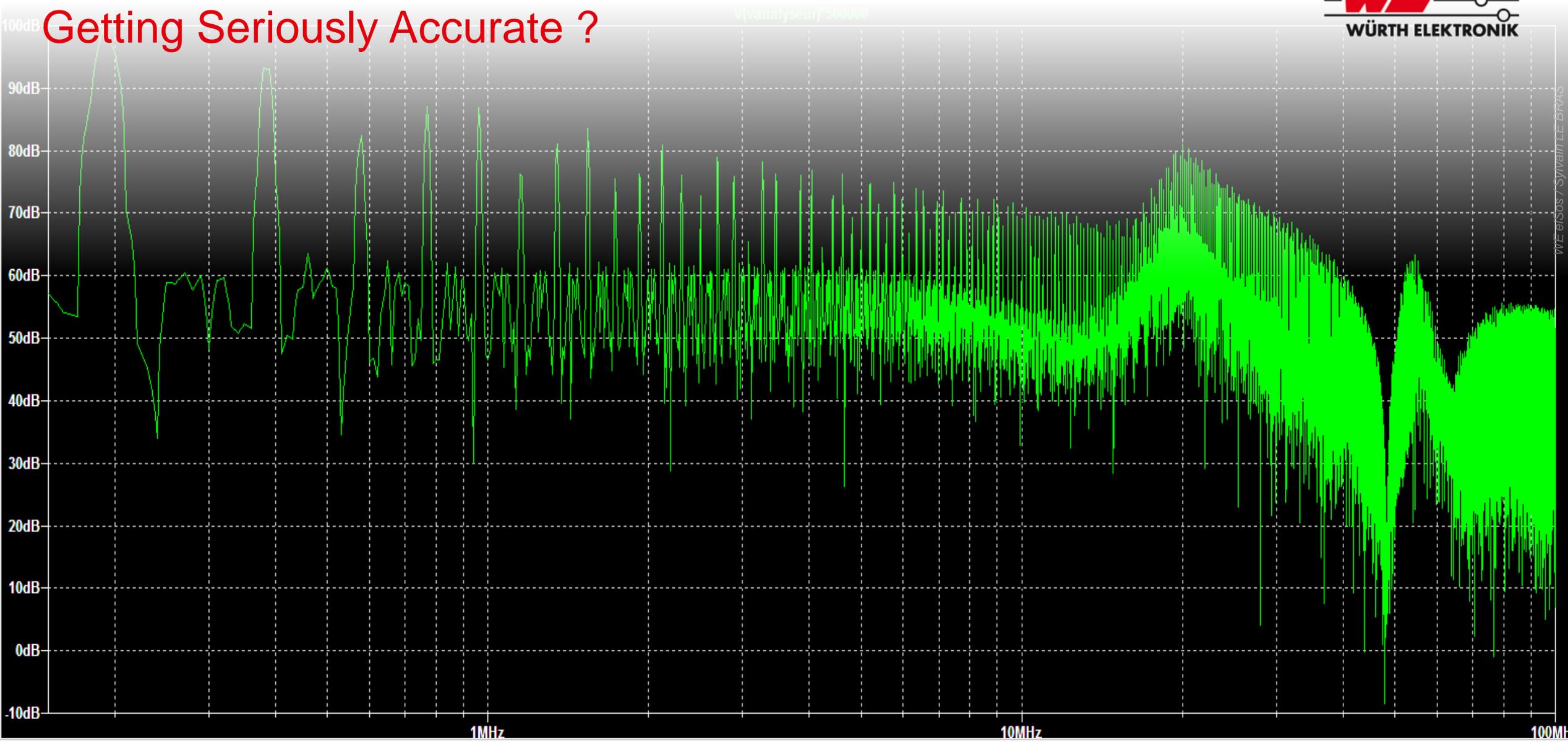


EMI measurement =  $\sum$  (Common Mode + Differential Mode)



# ... To EMC simulation

## Getting Seriously Accurate ?

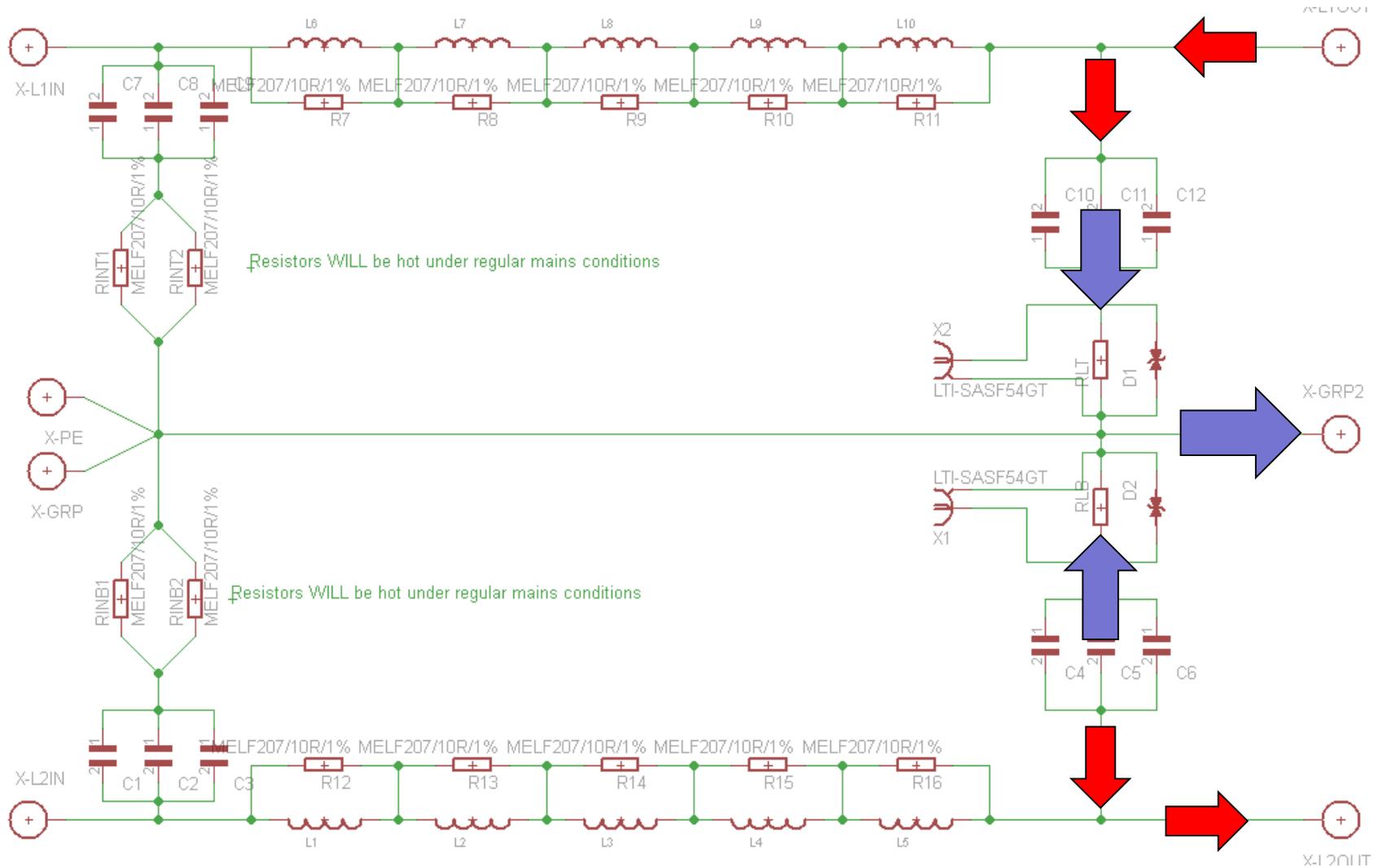


Vivianalyse by 500kHz

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# Getting Seriously Accurate ?

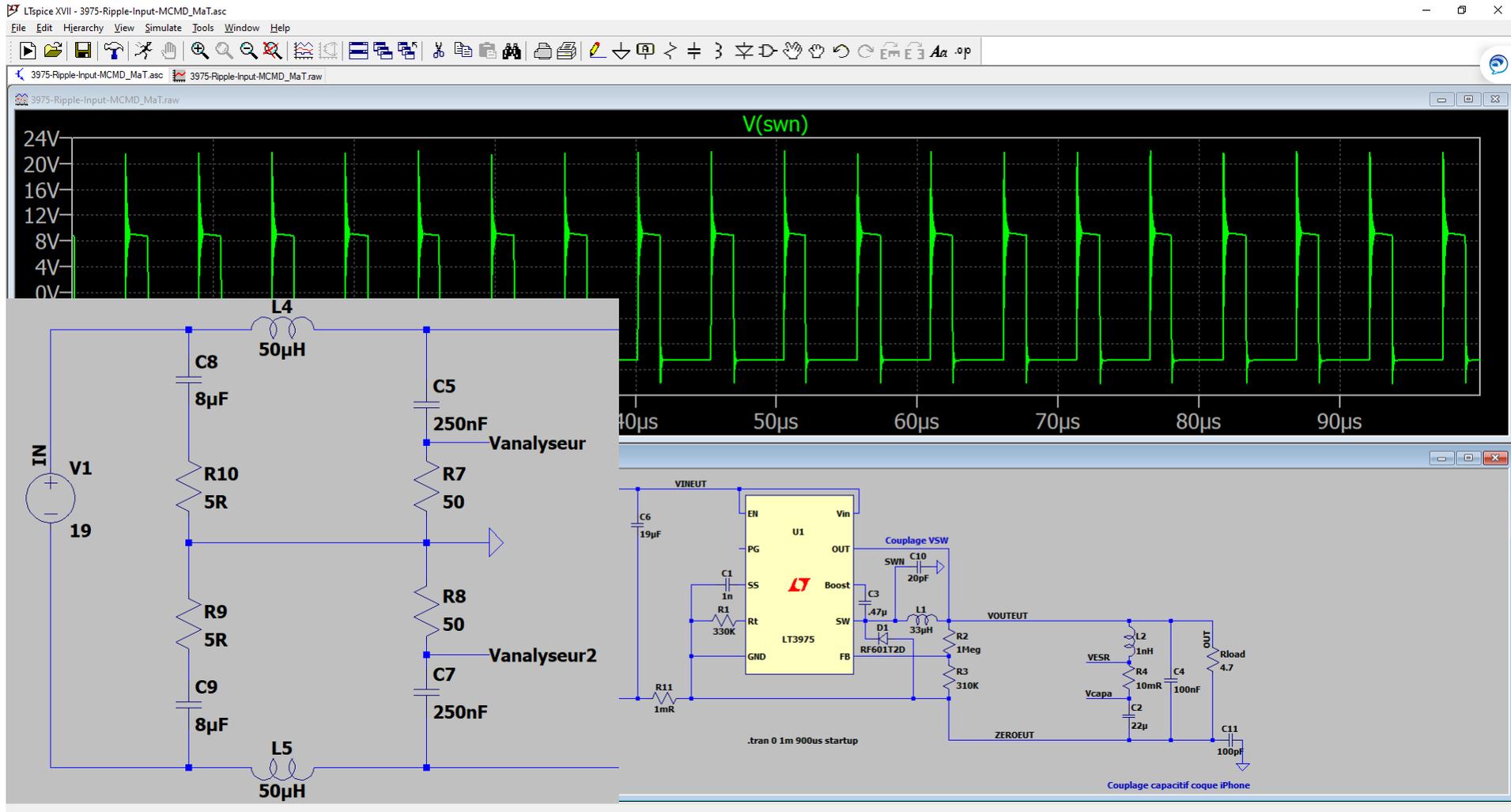
## Actual LISN design





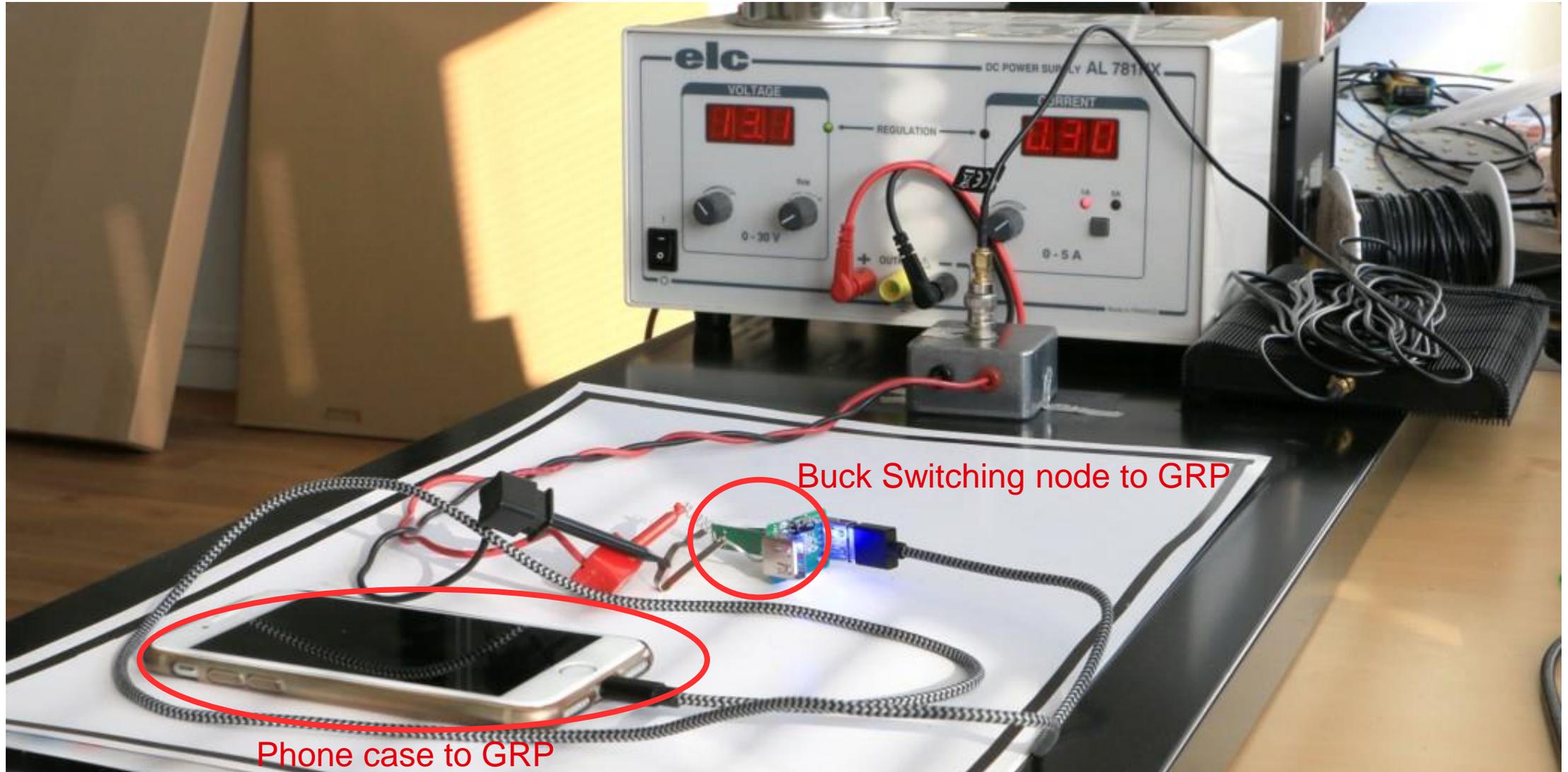
# Getting Seriously Accurate ?

## Simulation Ready LISN design



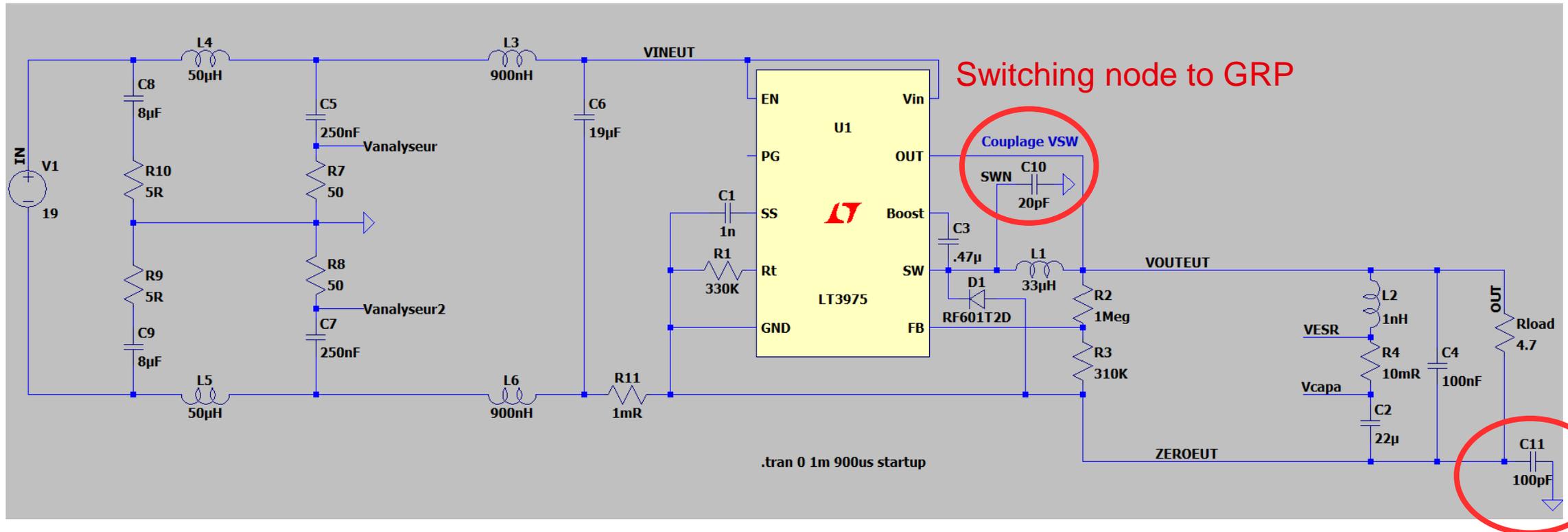
# Getting Seriously Accurate ?

## Adding E-Field parasitic coupling



# Getting Seriously Accurate ?

## Adding E-Field parasitic coupling



Phone case to GRP

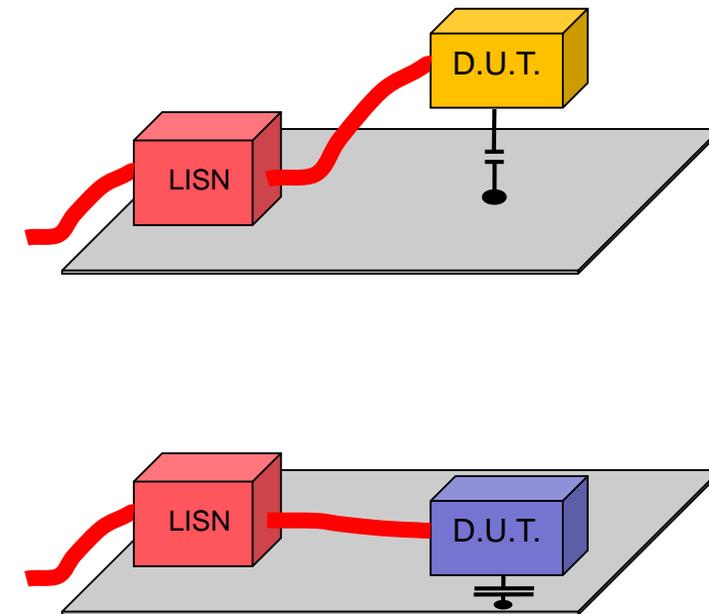
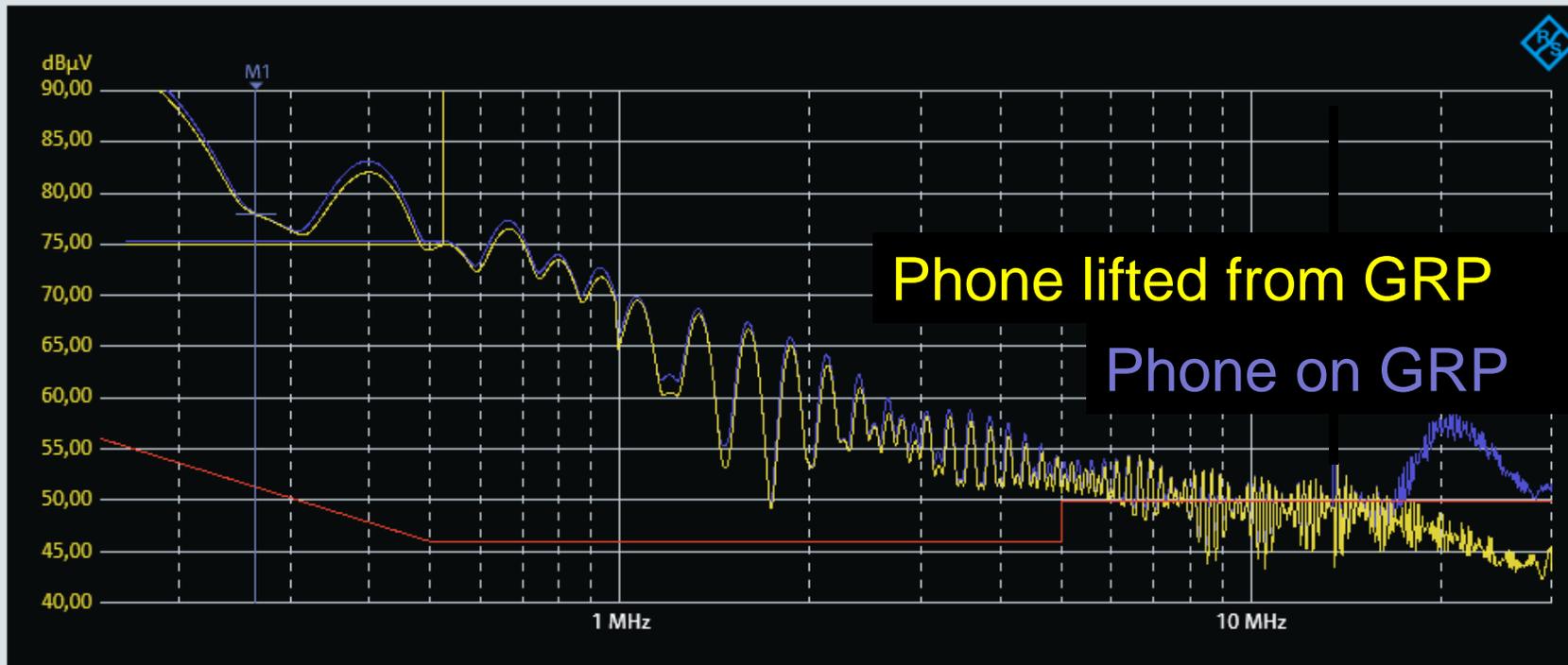
# Getting Seriously Accurate ?

## Reality VS Simulation

### Frequency Scan

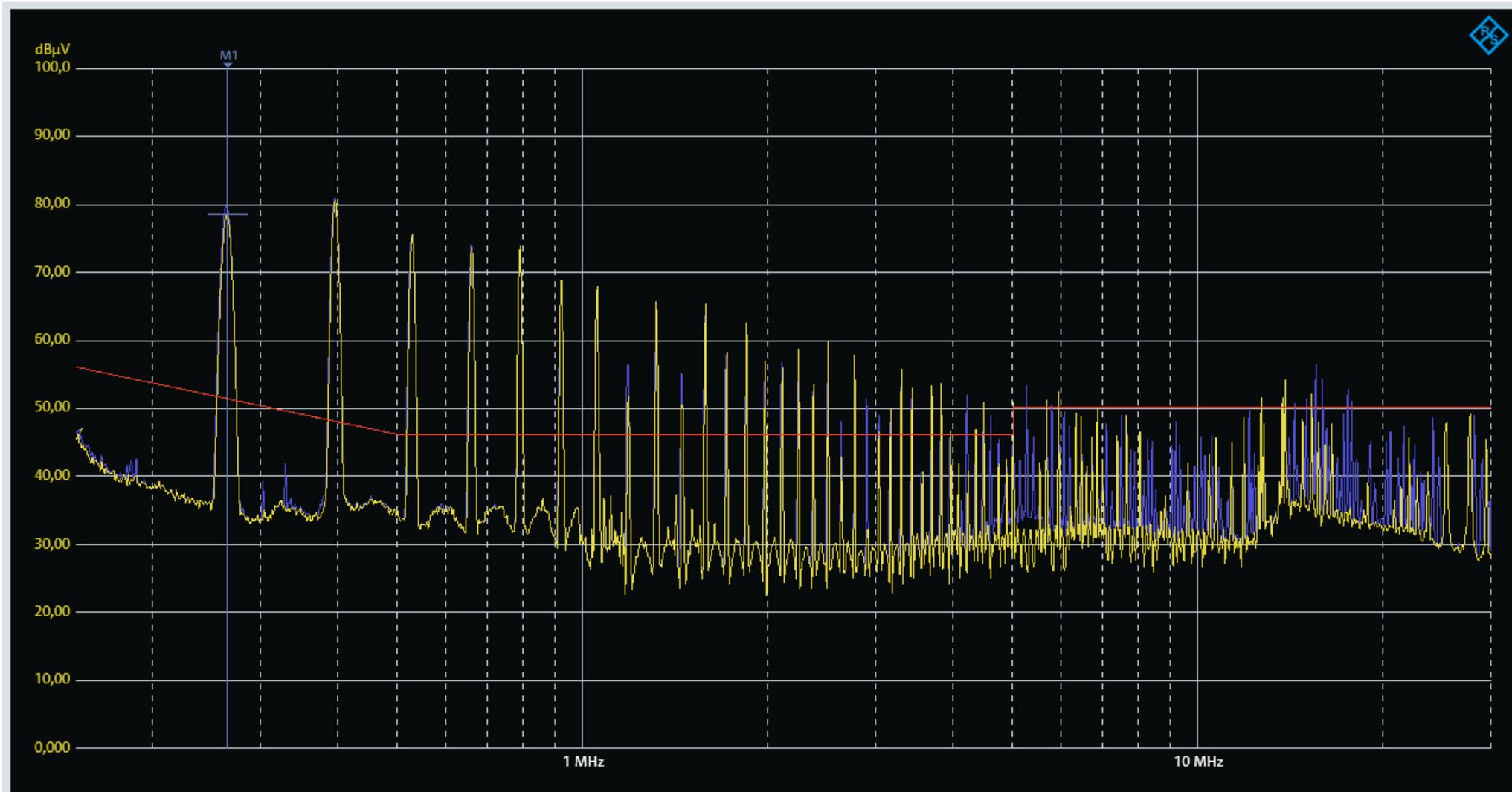
Ref Level 80 dB $\mu$ V  
 RF Attenuator 10 dB  
 RBW 100 kHz  
 Start Frequency 150 kHz  
 Stop Frequency 30 MHz

Measurement Time 10 ms  
 Trace Mode Clear / Write  
 Trigger Mode Free Run  
 Trace Detector Average  
 Scan step 0,5 %



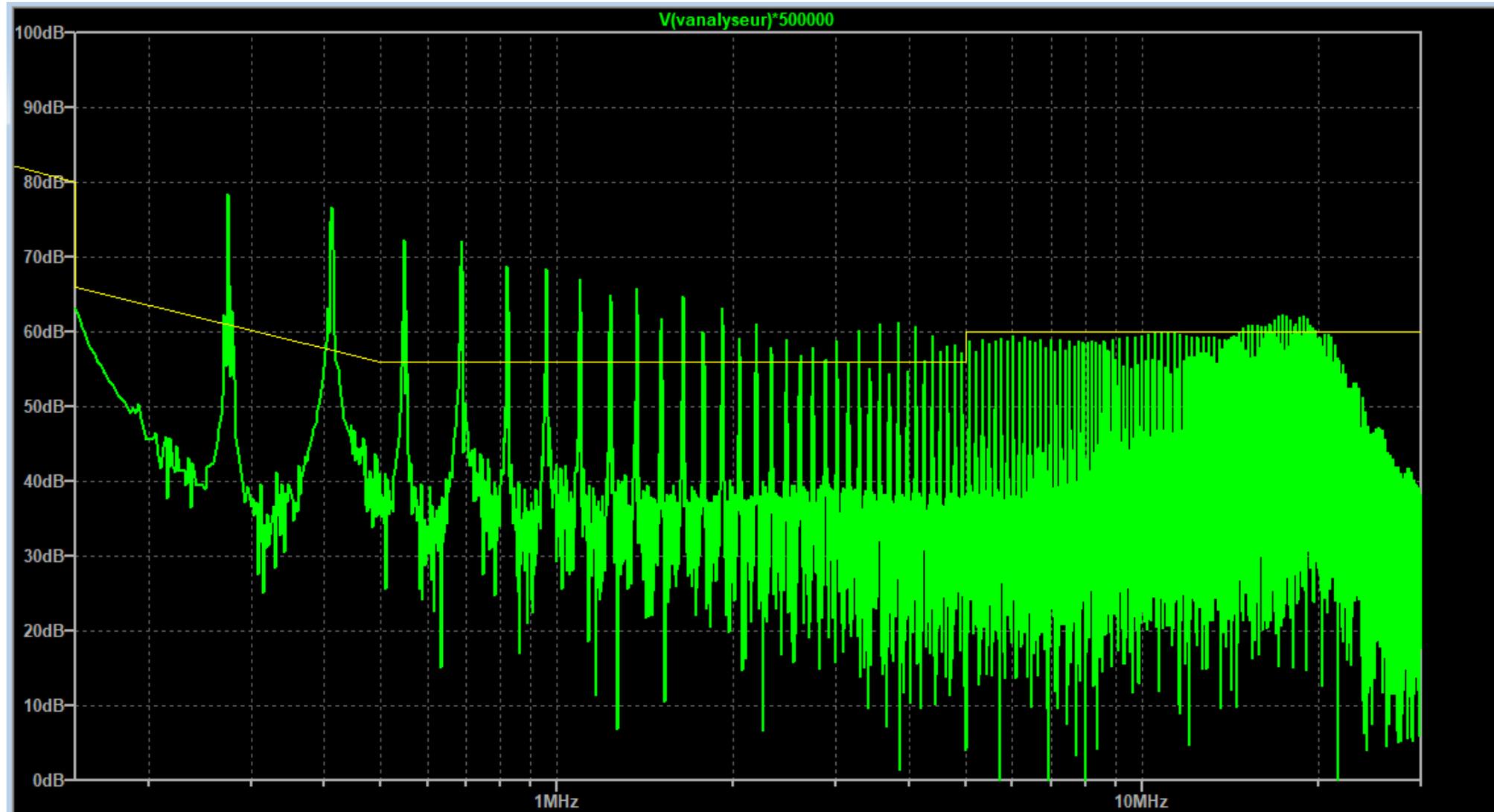
# Getting Seriously Accurate ?

## Reality VS Simulation



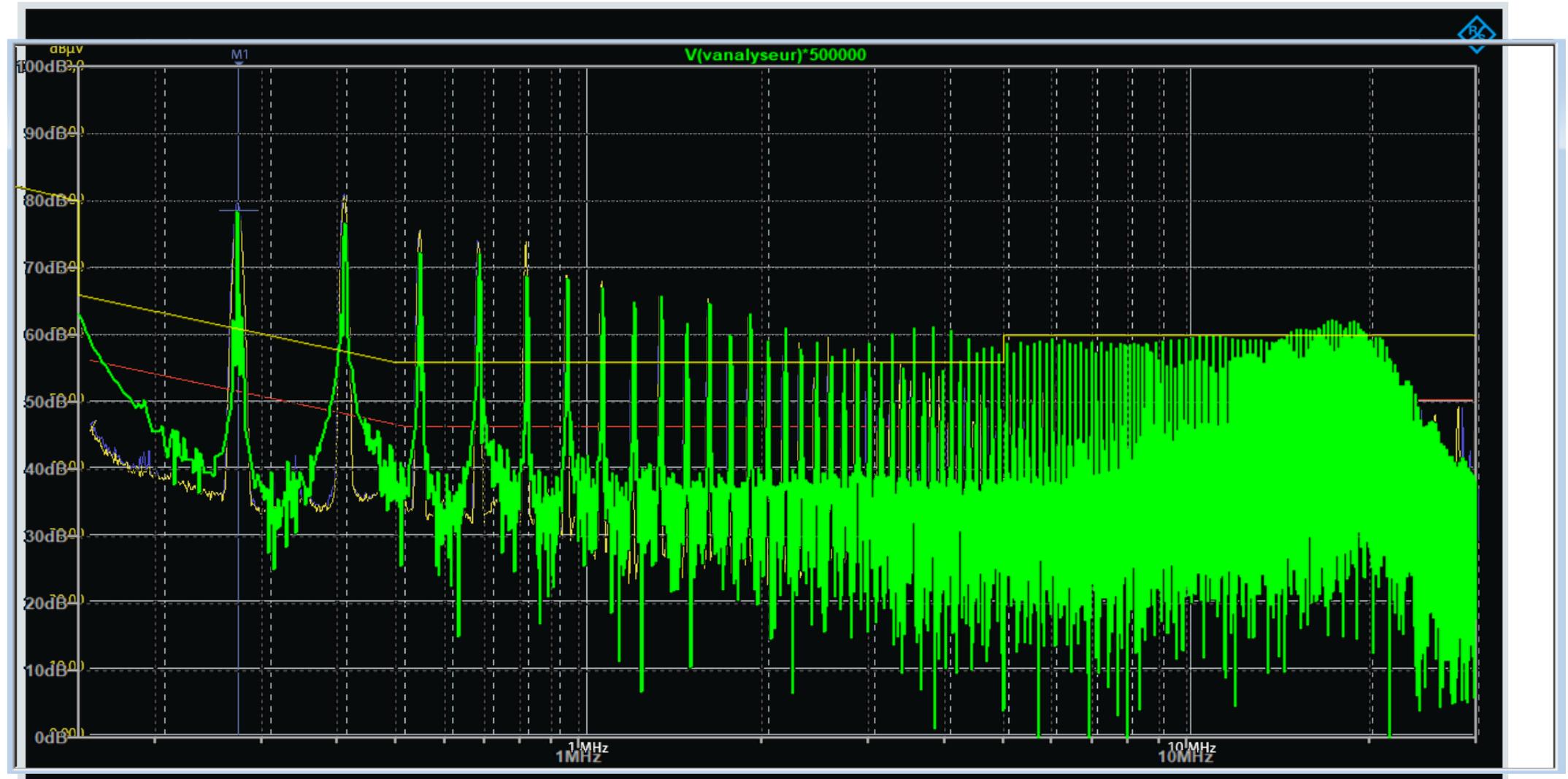
# Getting Seriously Accurate ?

## Reality VS Simulation



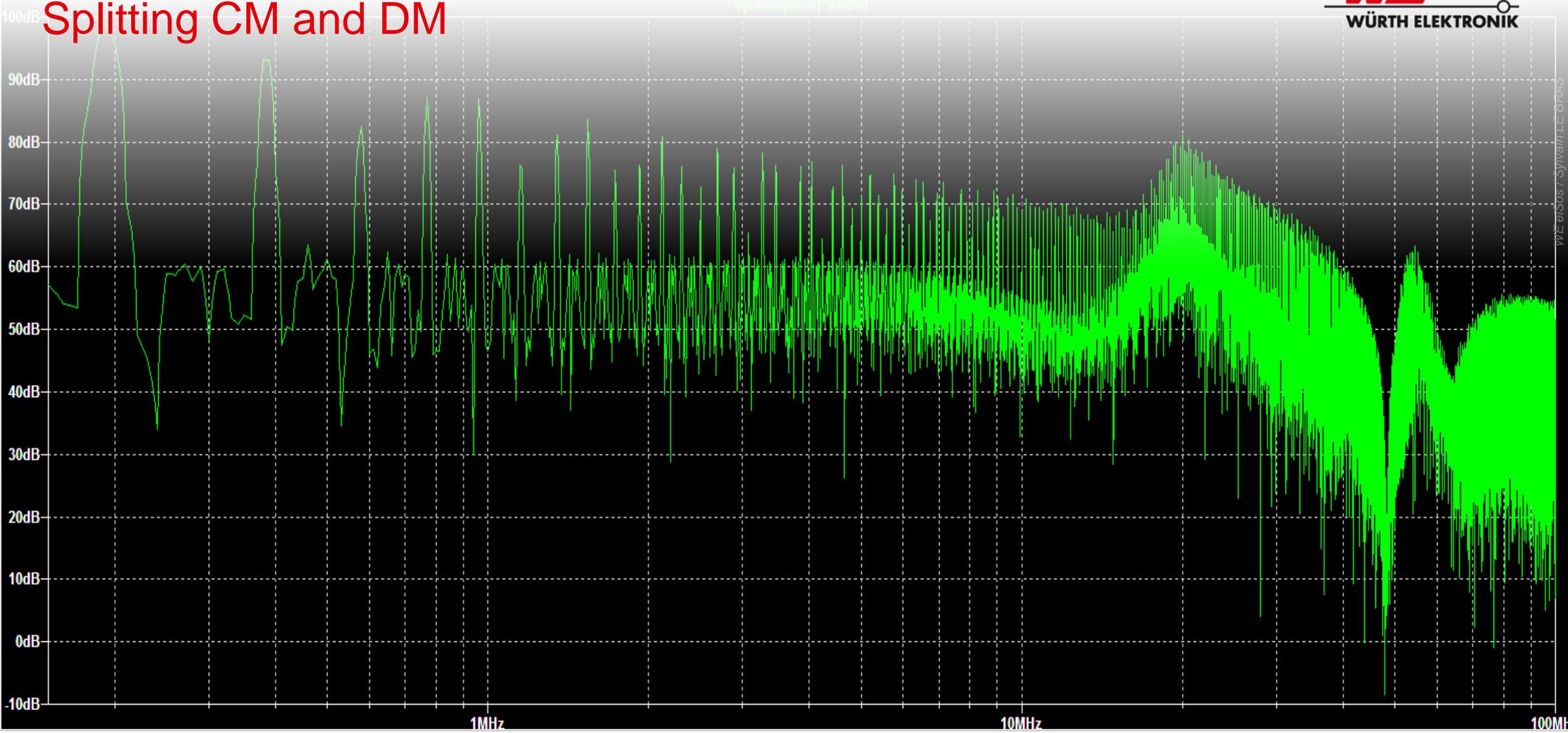
# Getting Seriously Accurate ?

## Reality VS Simulation



# Going further with simulation

## Splitting CM and DM

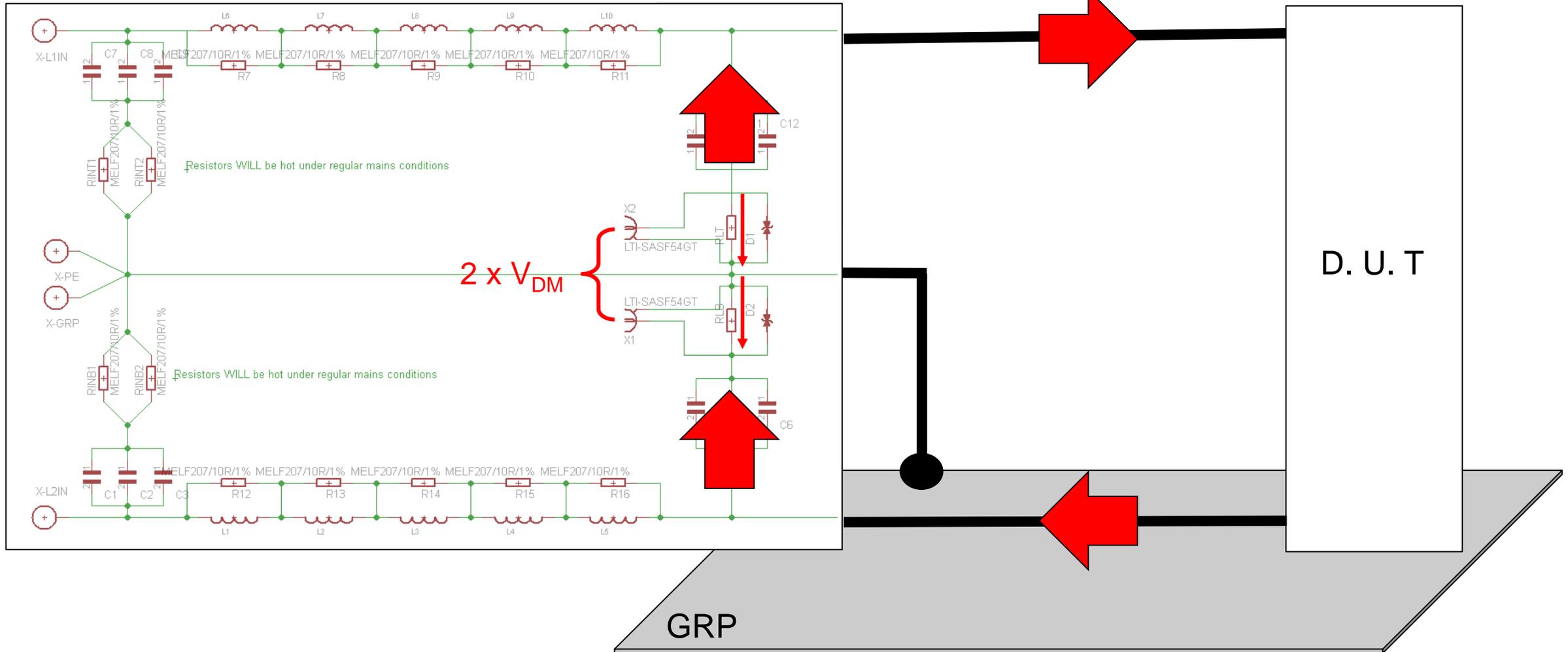


WE eiSos 7 Syvaim LE BRAS

# Going further with simulation

## Splitting CM and DM

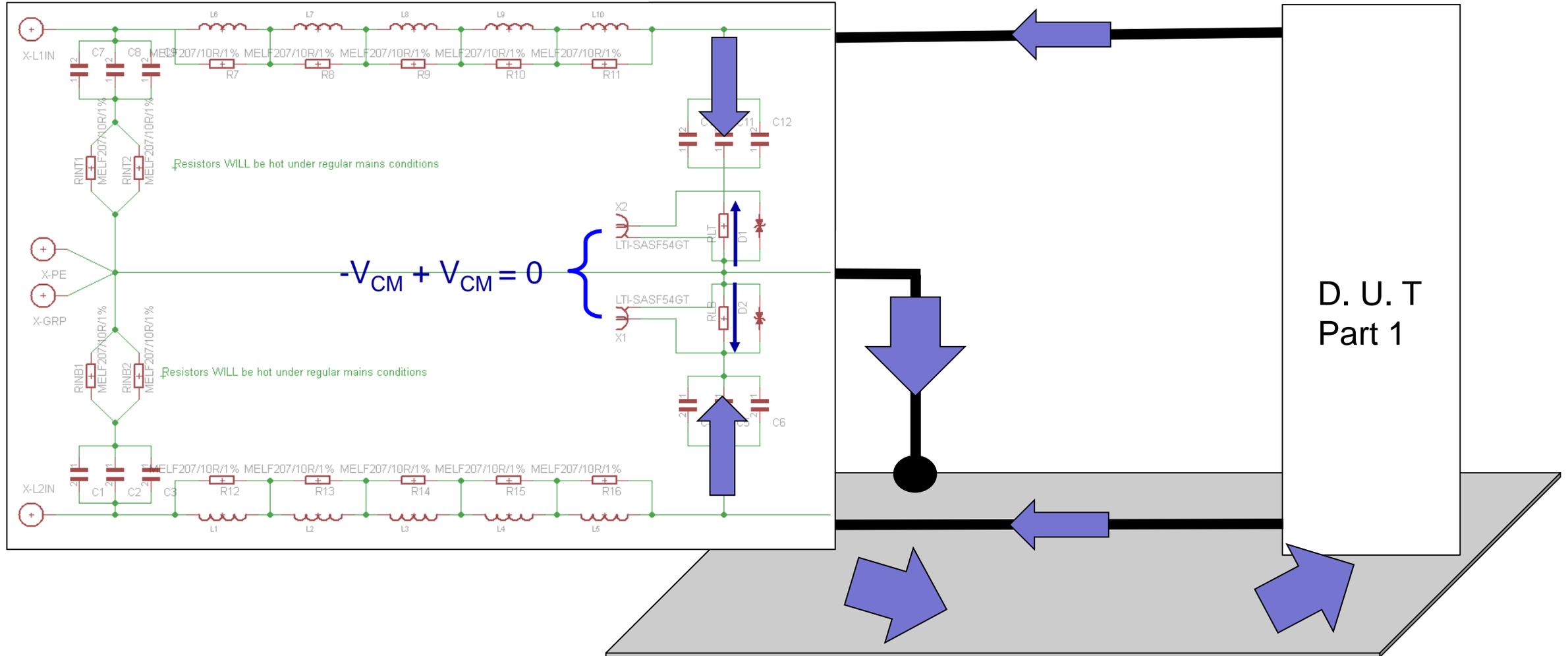
- Symmetrical interference ?



# Going further with simulation

## Splitting CM and DM

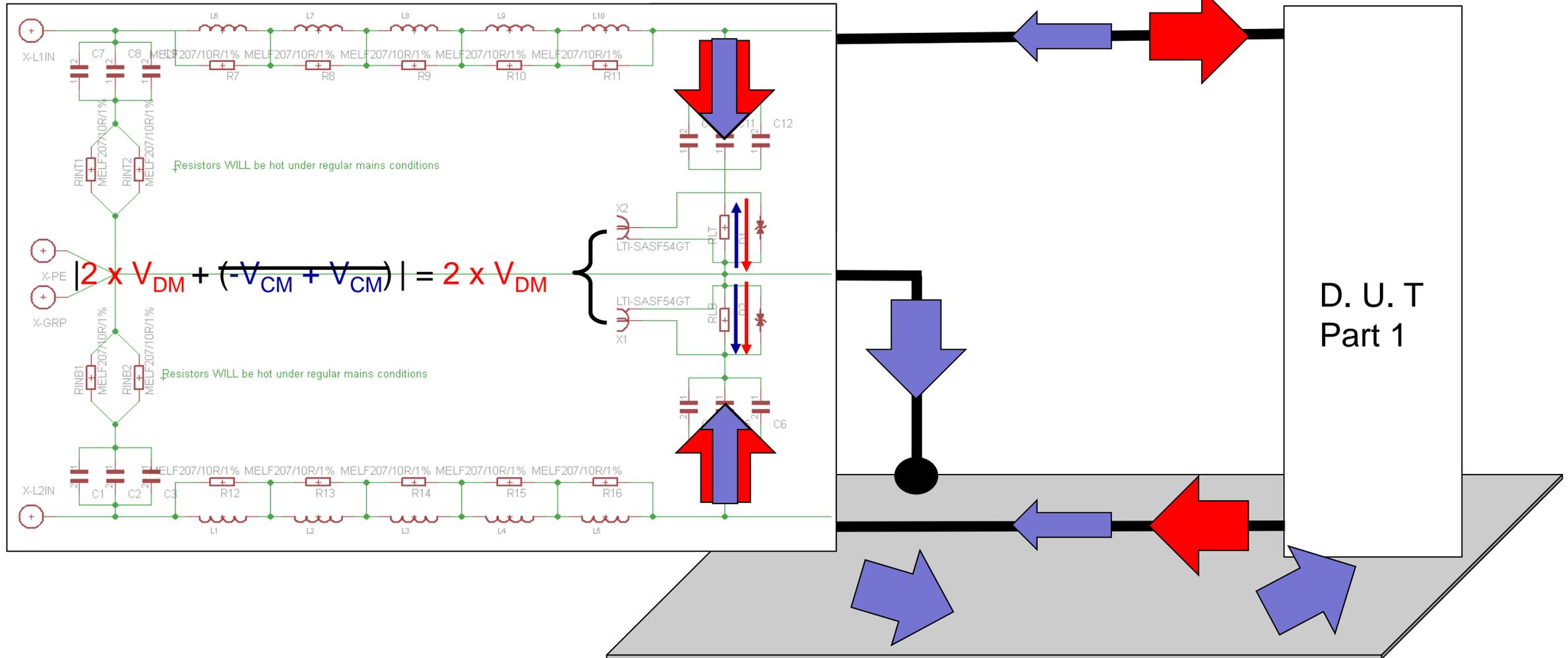
- Asymmetrical interference ?



# Going further with simulation

## Splitting CM and DM

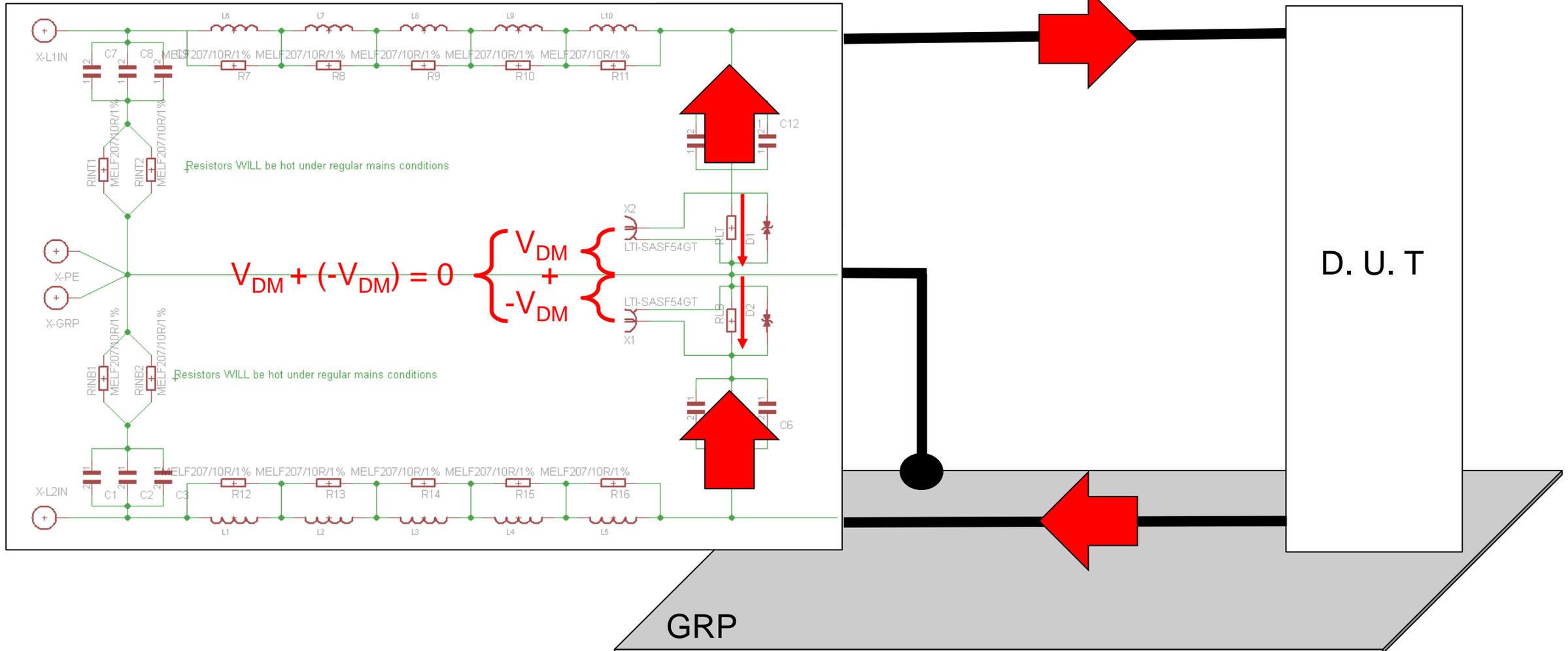
- Asymmetrical interference ?



# Going further with simulation

## Splitting CM and DM

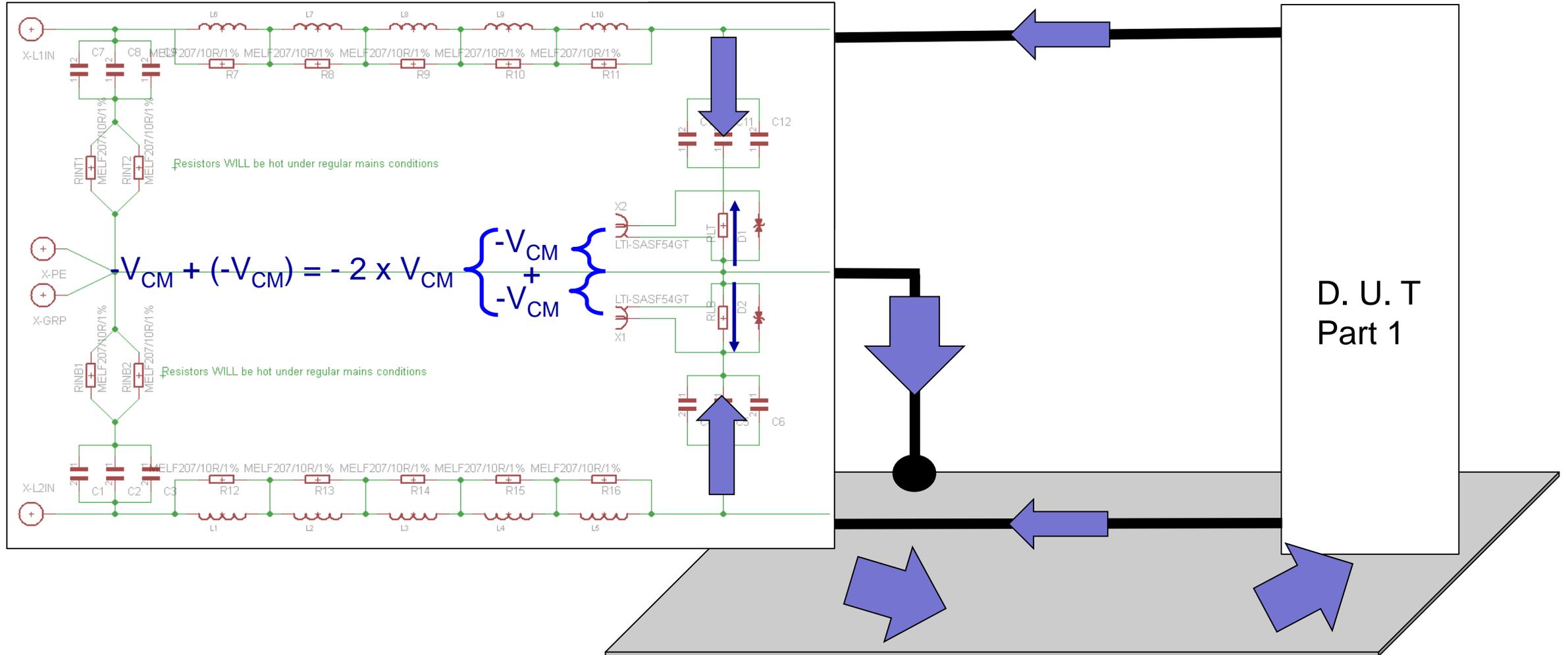
- Symmetrical interference ?



# Going further with simulation

## Splitting CM and DM

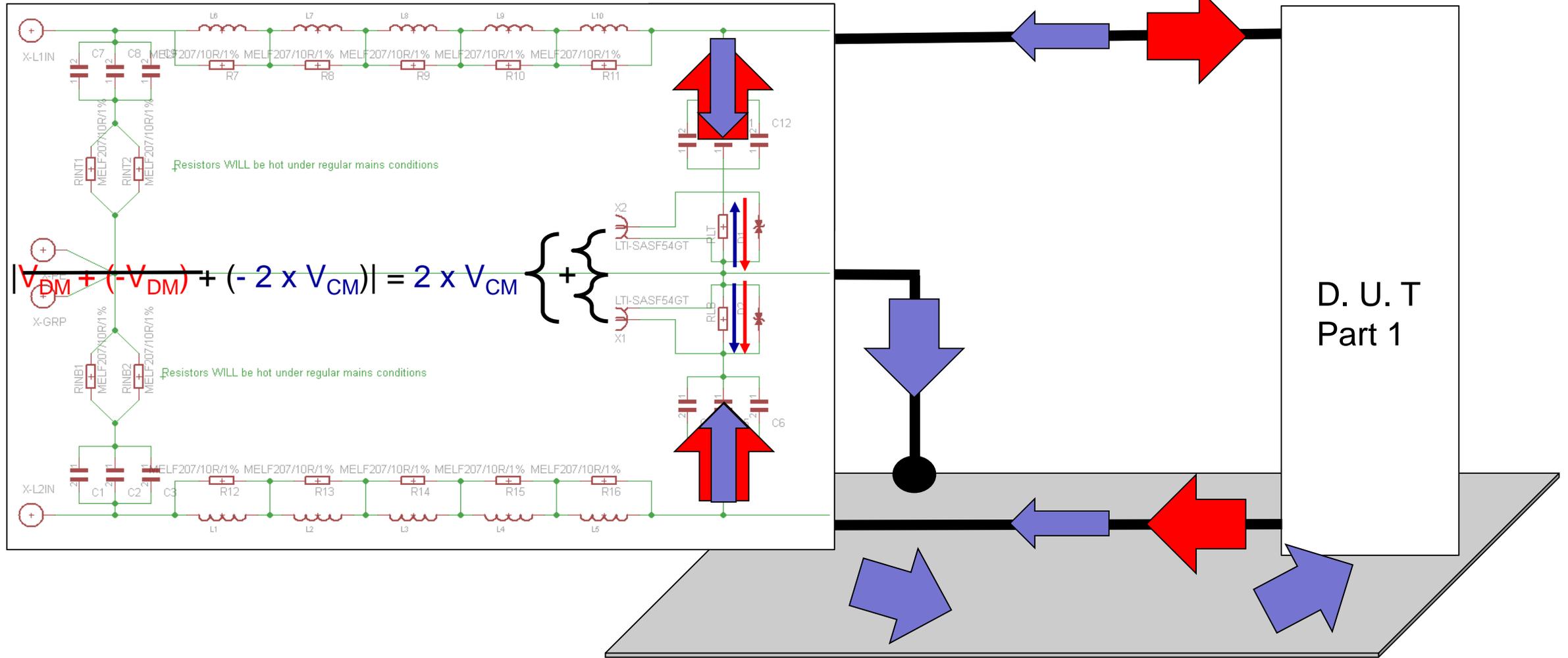
- Asymmetrical interference ?



# Going further with simulation

## Splitting CM and DM

- Asymmetrical interference ?





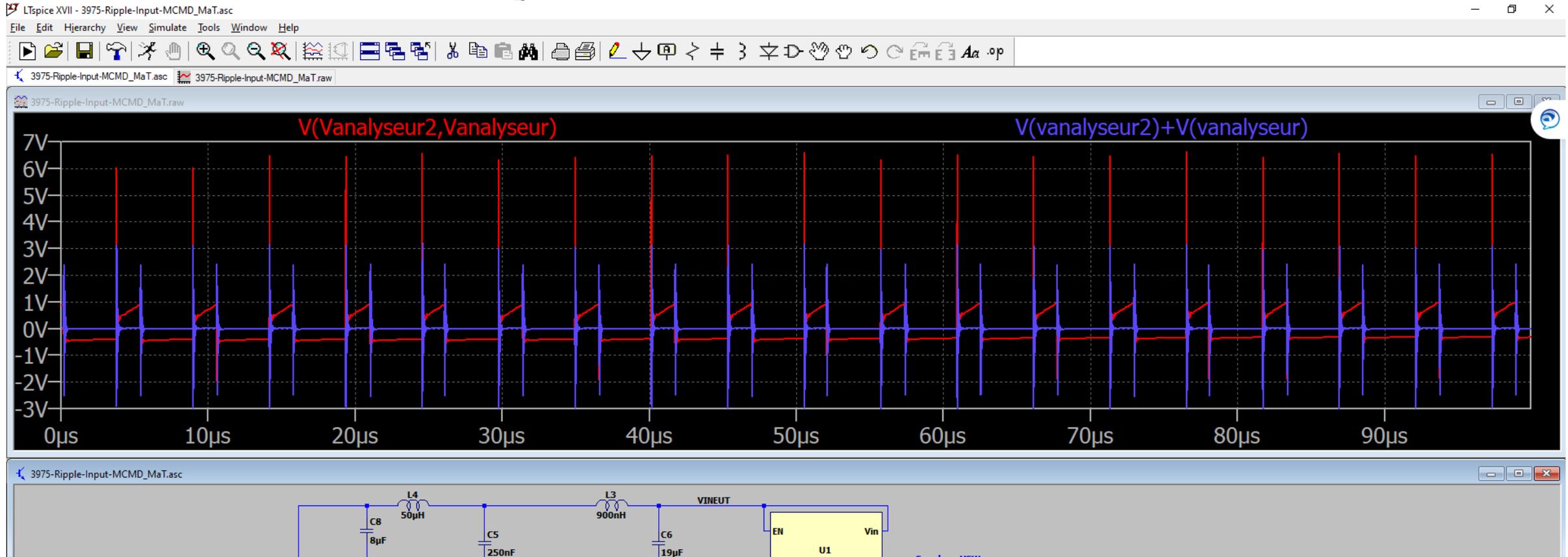
# Going further with simulation

## Splitting CM and DM

```
V(vanalyseur,vanalyseur2)
V(vanalyseur2)+V(vanalyseur)
```

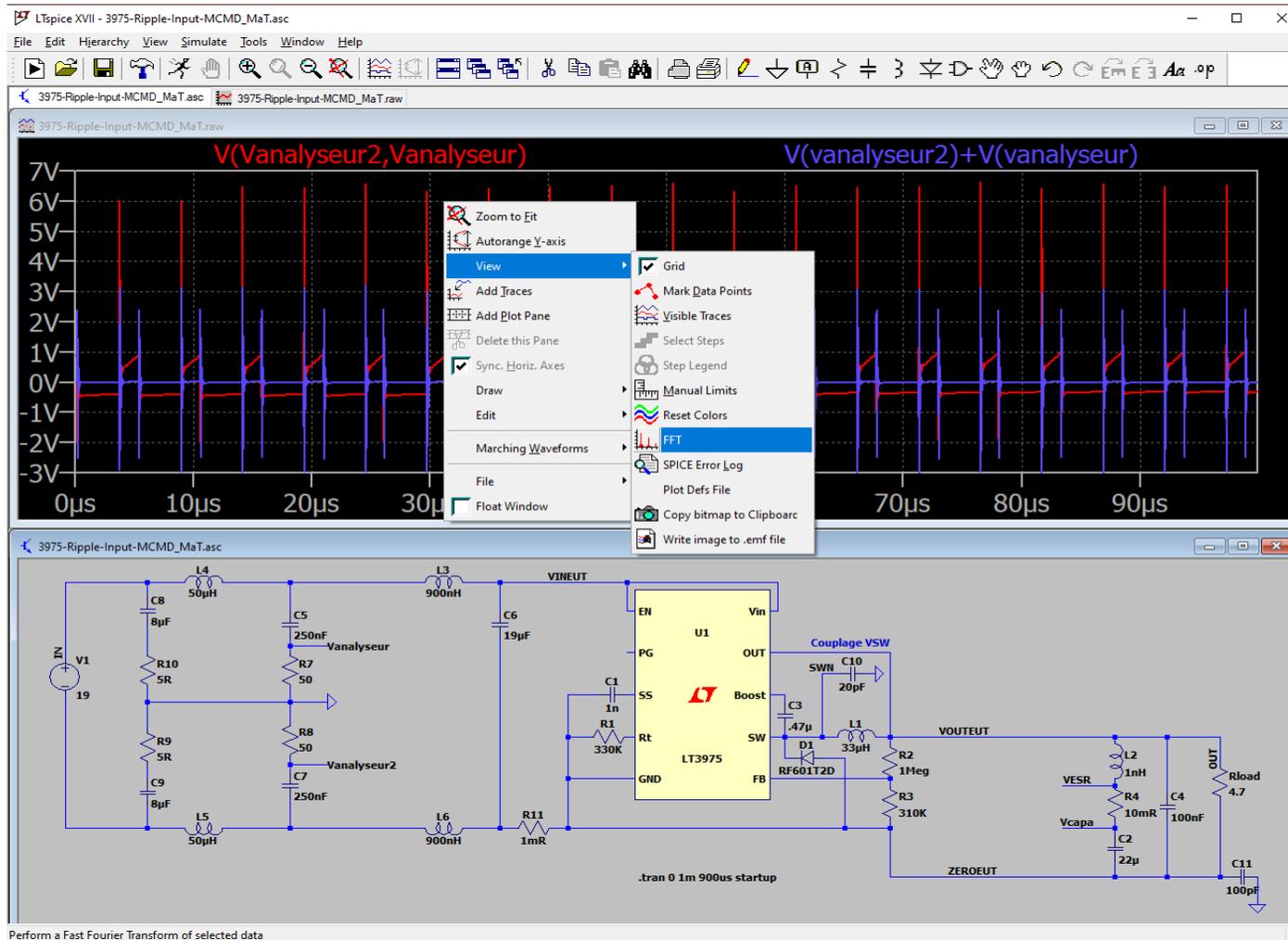
2 \* DM noise

2 \* CM noise



# Going further with simulation

## Splitting CM and DM

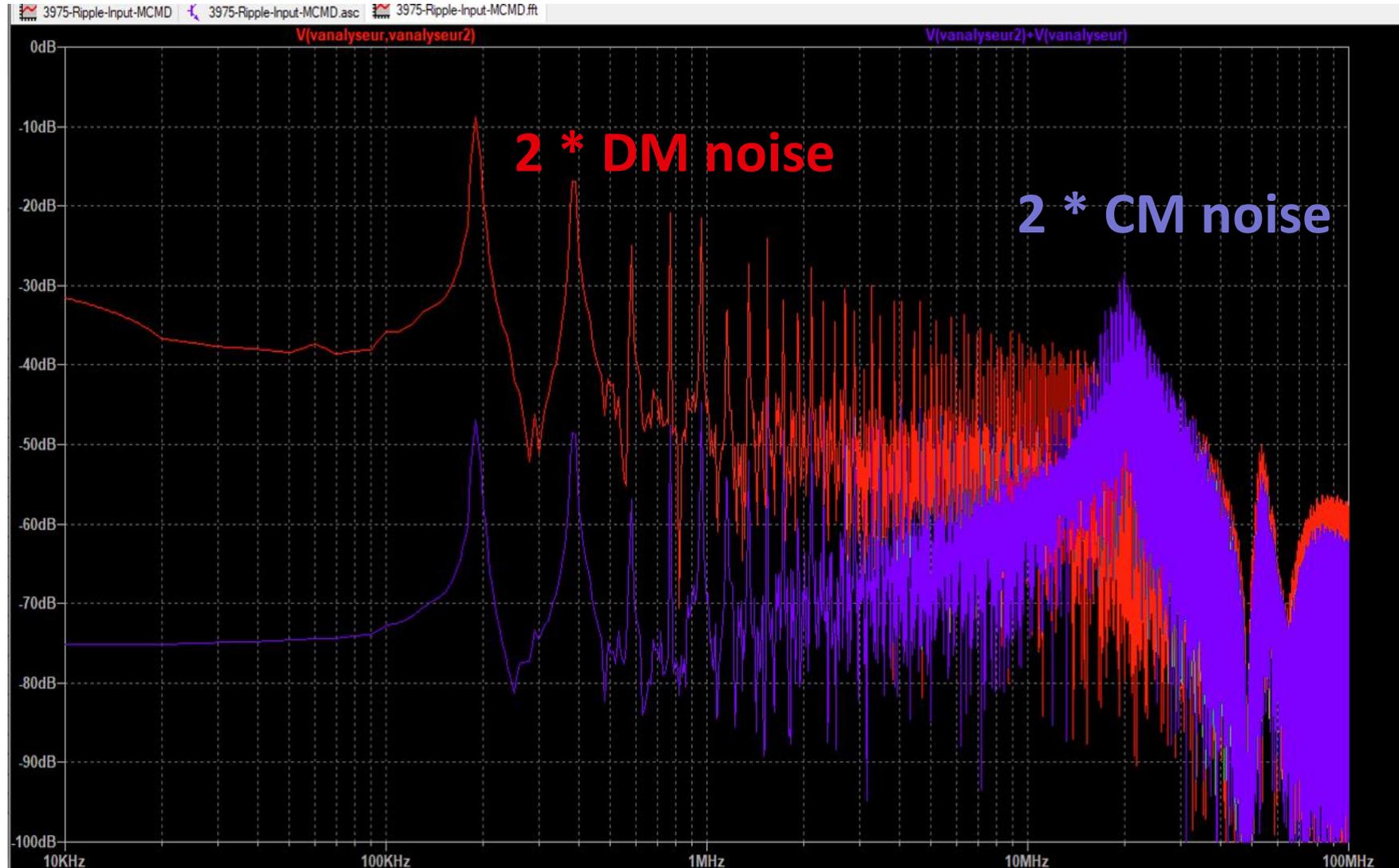


The figure shows the 'Select Visible Waveforms' dialog box in LTspice. The dialog has a checkbox for 'Only list traces matching' and another for 'Asterisks match colons'. Below these are two buttons: 'OK' and 'Cancel'. The 'Select Waveforms to Plot:' section contains a list of waveforms. The first two waveforms are selected:  $V(vanalyseur2,Vanalyseur2)$  and  $V(vanalyseur2)+V(vanalyseur)$ . Red and blue arrows point to these two waveforms with labels  $2 * DM\ noise$  and  $2 * CM\ noise$  respectively. At the bottom of the dialog, there is a checkbox for 'Auto Range'.



# Going further with simulation

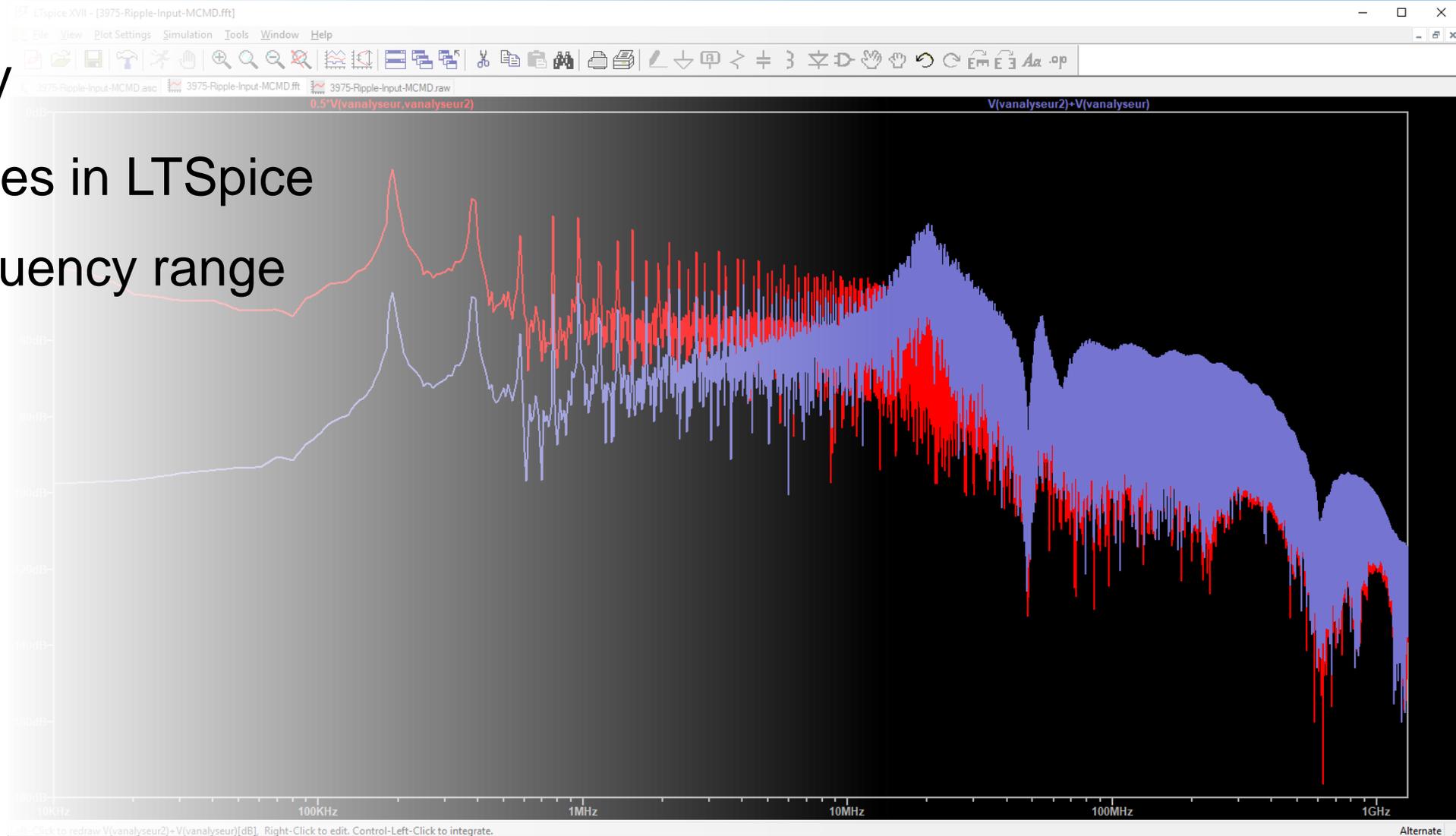
## Splitting CM and DM



# Going further with simulation

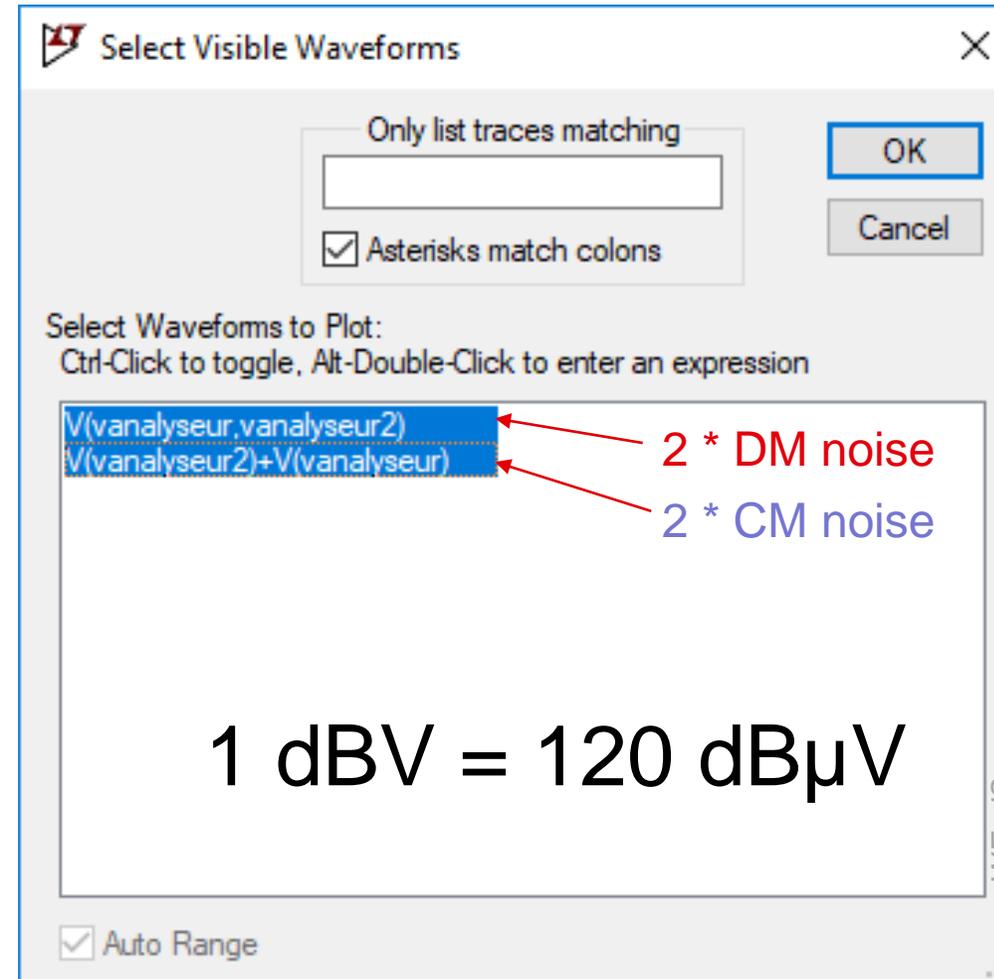
## Making simulation look real

- Scaling to  $\text{dB}\mu\text{V}$
- Loading limit lines in LTSpice
- Defining a Frequency range



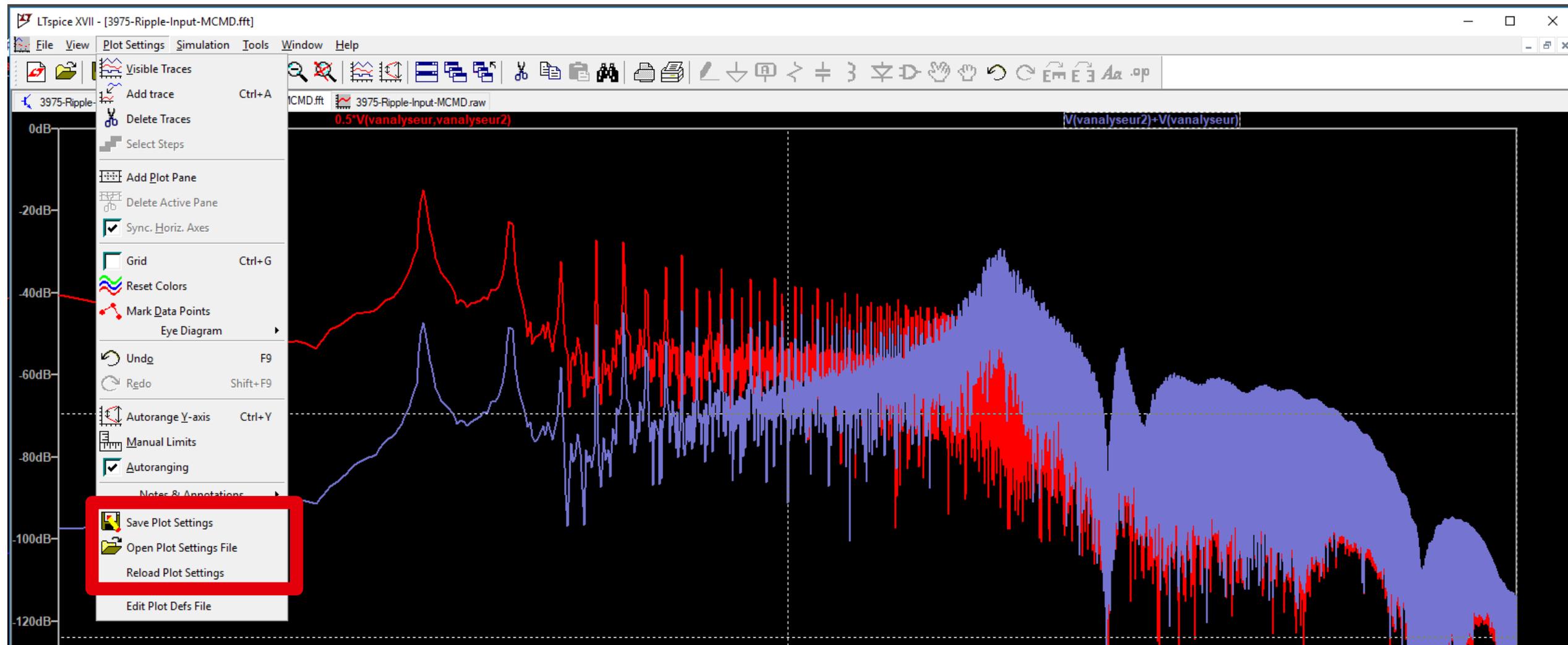
# Going further with simulation

## Making simulation look real



# Going further with simulation

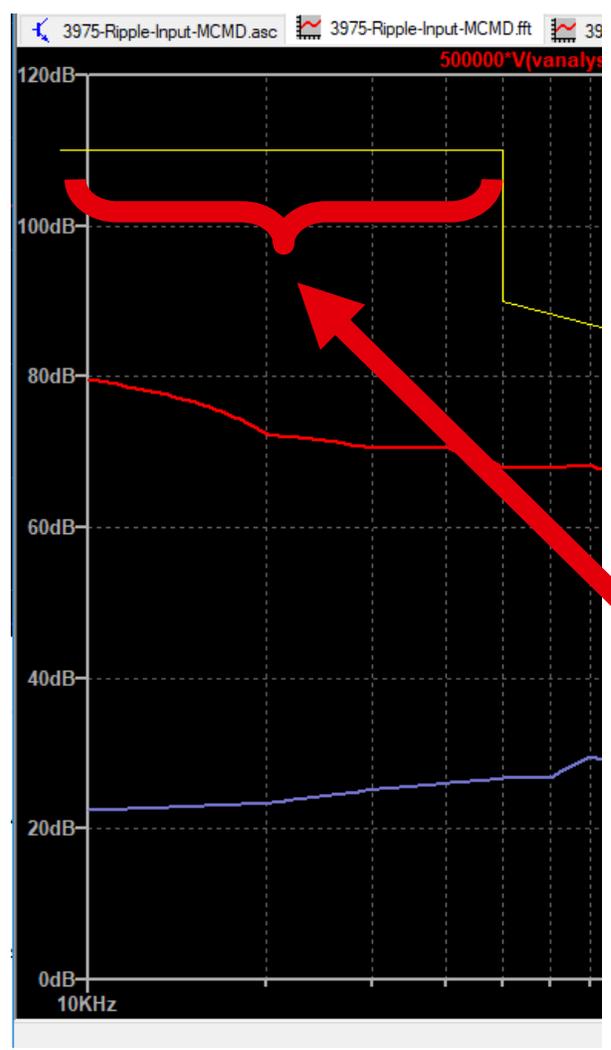
## Making simulation look real





# Going further with simulation

## Making simulation look real – Adding limit lines



Line	Start	End	Amp dBµV start	Amp dBµV stop	Line def for LTSPICE
Line 1	9000	50000	110	110	(9000,0.316227766016838) (50000,0.316227766016838)
Line 2	50000	150000	90	80	(50000,0.0316227766016838) (150000,0.01)
Line 3	150000	500000	66	56	(150000,0.00199526231496888) (500000,0.000630957344480192)
Line 4	500000	5000000	56	56	(500000,0.000630957344480192) (5000000,0.000630957344480192)
Line 5	5000000	30000000	60	60	(5000000,0.001) (30000000,0.001)

```

Flyback-example-2-base - Bloc-notes
Fichier Edition Format Affichage Aide
[FFT of time domain data]
{
  Npanes: 1
  {
    traces: 1 {2,0,"V(vanalyseur2)+V(vanalyseur)"}
    X: ('M',0,9000,0,30000000)
    Y[0]: ('',0,1e-006,10,1)
    Y[1]: ('',0,-200,40,200)
    Log: 1 2 0
    PltMag: 1
    Line: "dB" 4 0 (9000,0.3162277660168) (50000,0.316227766)
    Line: "dB" 4 0 (50049.8435712172,0.0317065818612387) (150407.110289202,0.0100397786508485)
    Line: "dB" 4 0 (150000,0.00199526231496888) (500000,0.000630957344480192)
    Line: "dB" 4 0 (500000,0.000630957344480192) (5000000,0.000630957344480192)
    Line: "dB" 4 0 (5000000,0.001) (30000000,0.001)
  }
}
    
```

Fill according to EMC standards

Copy the result

Paste it here

# Going further with simulation

## Making simulation look real – Defining a range

10kHz to 30 MHz

0 to 120dB $\mu$ V

3975-Ripple-Input-MCMD-dbuV.plt - Bloc-notes

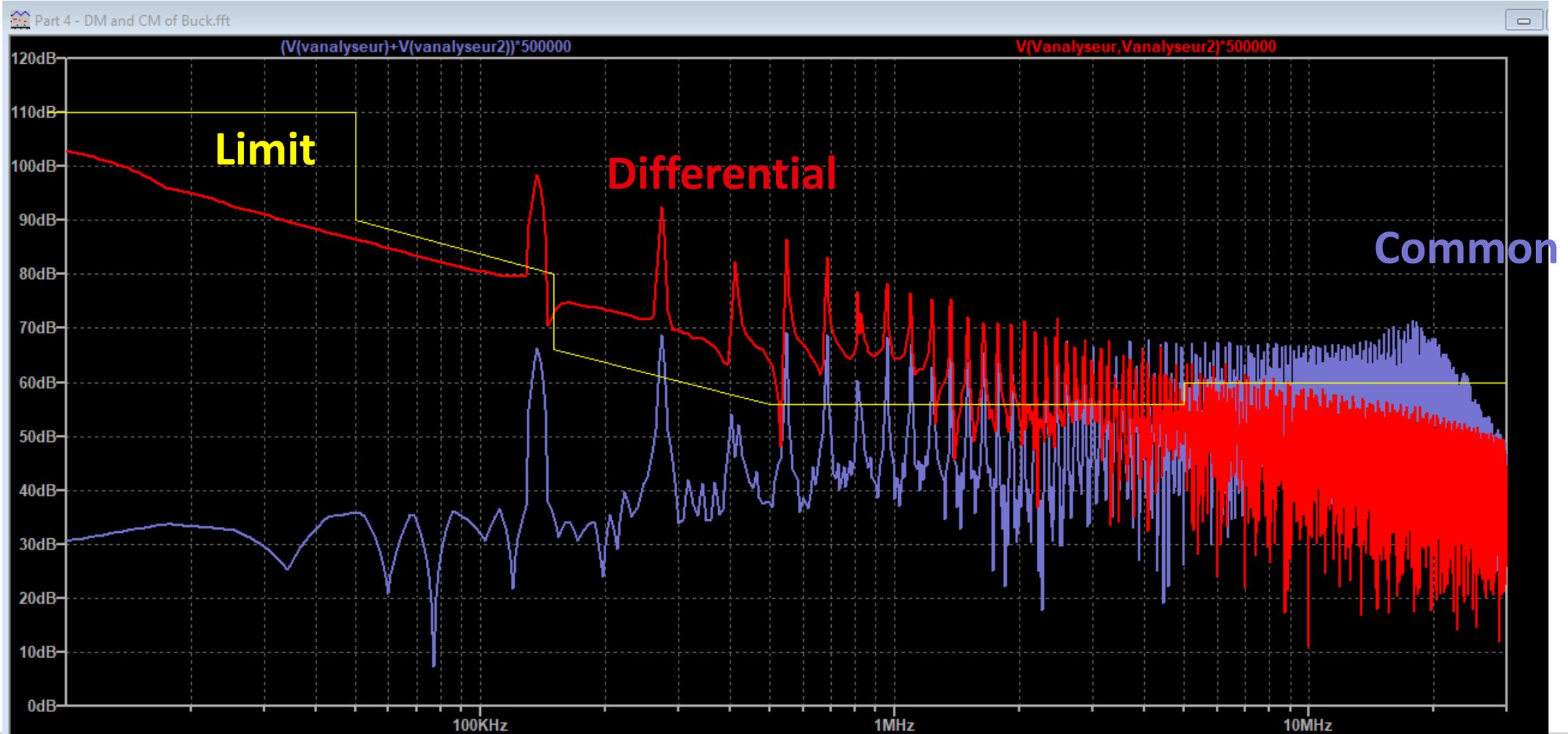
Fichier Edition Format Affichage ?

[FFT of time domain data]

```
{
  Npanes: 1
  {
    traces: 2 {65540,0,"500000*V(vanalyseur,vanalyseur2)"} {65547,0,"1000000*(V(vanalyseur2)+V(vanalyseur))"}
    X: ('M',0,10000,0,3e+007)
    Y[0]: (' ',0,1,20,1e+006)
    Log: 1 2 0
    GridStyle: 1
    PltMag: 1
    Line: "dB" 13 0 (8983.92329505352,319040.747263751) (49889.5367382049,319040.747263751)
    Line: "dB" 13 0 (50000,316227.766016838) (50000,31622.7766016838)
    Line: "dB" 13 0 (50000,31622.7766016838) (150000,10000)
    Line: "dB" 13 0 (150000,10000) (150000,1995.26231496888)
    Line: "dB" 13 0 (150000,1995.26231496888) (500000,630.957344480193)
    Line: "dB" 13 0 (500000,630.957344480193) (5000000,630.957344480193)
    Line: "dB" 13 0 (5000000,630.957344480193) (5000000,1000)
    Line: "dB" 13 0 (5000000,1000) (30000000,1000)
  }
}
```

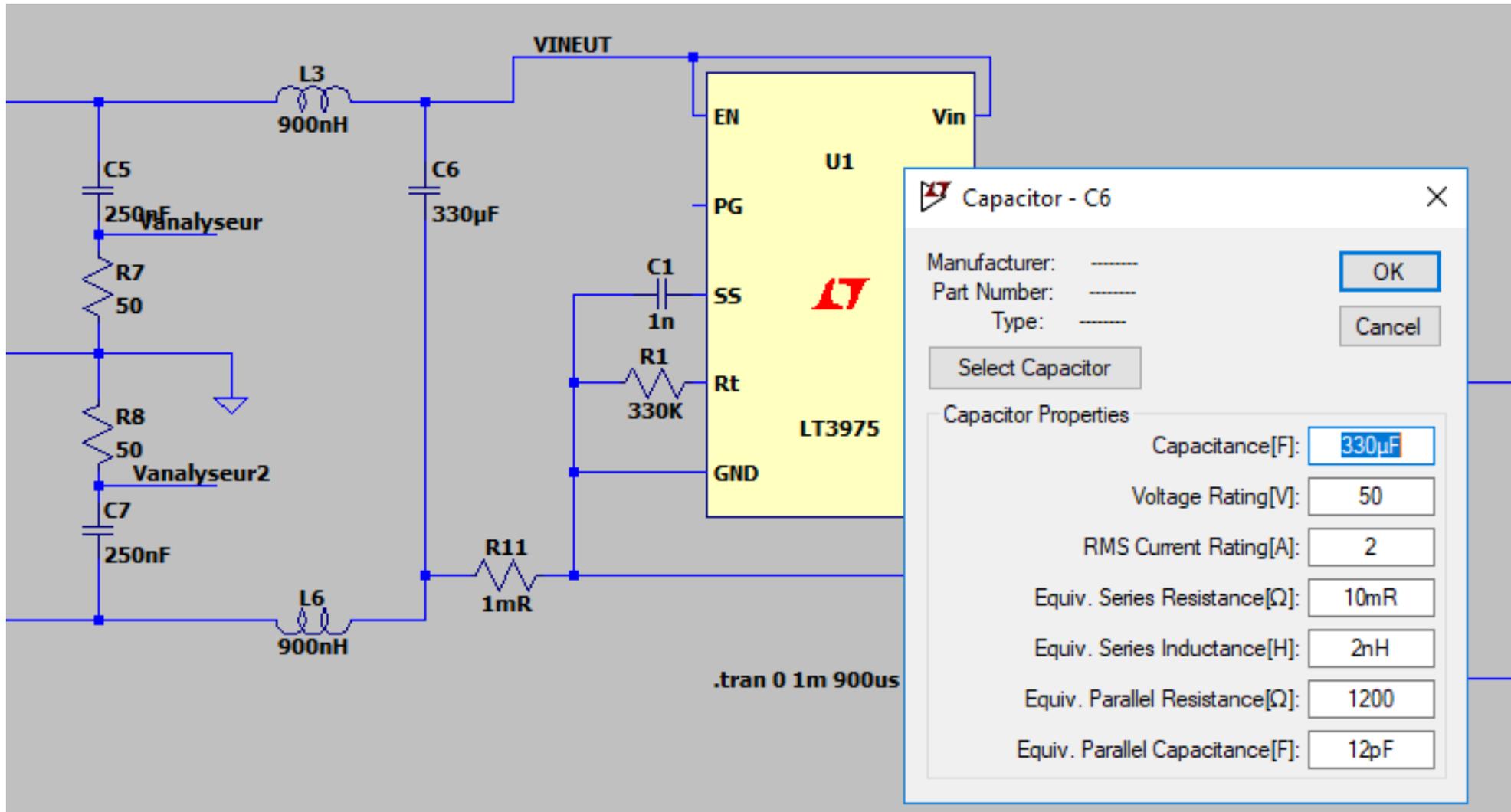
# Going further with simulation

## Making simulation look real – Result 😊



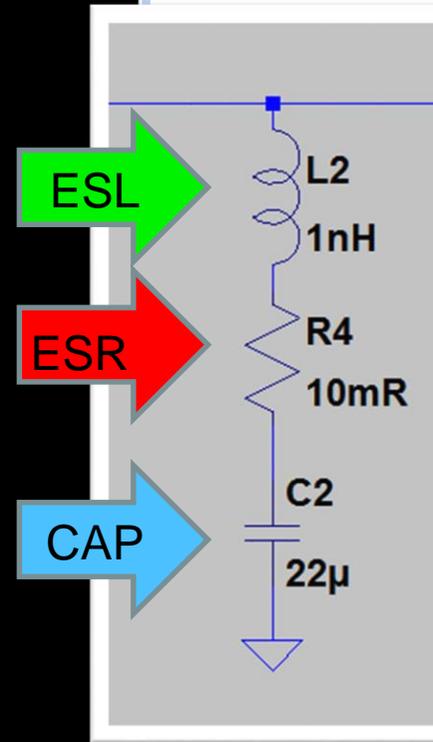
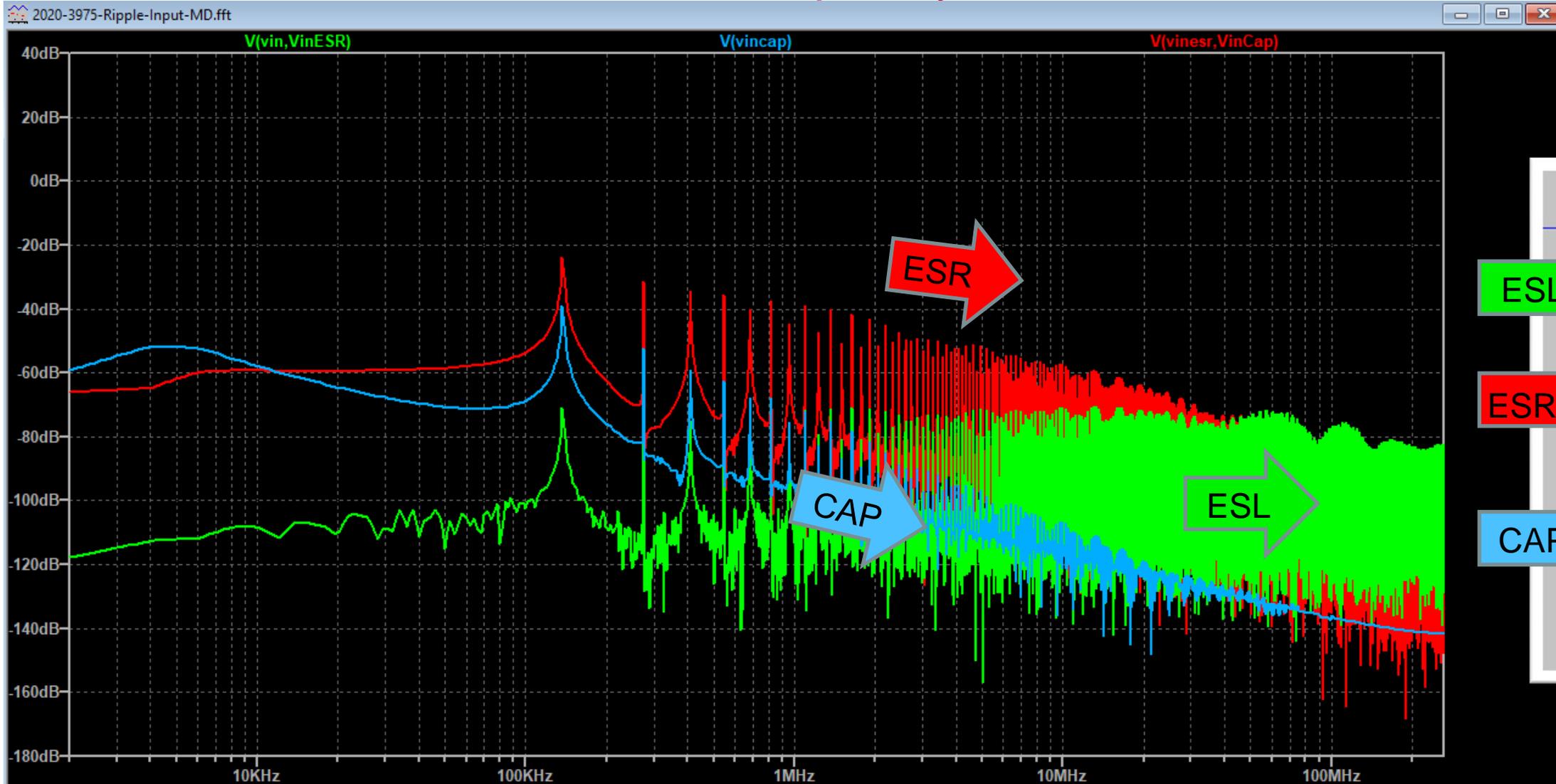
# Going further with simulation

## Fixing that buck in the simulation – Polymer input cap



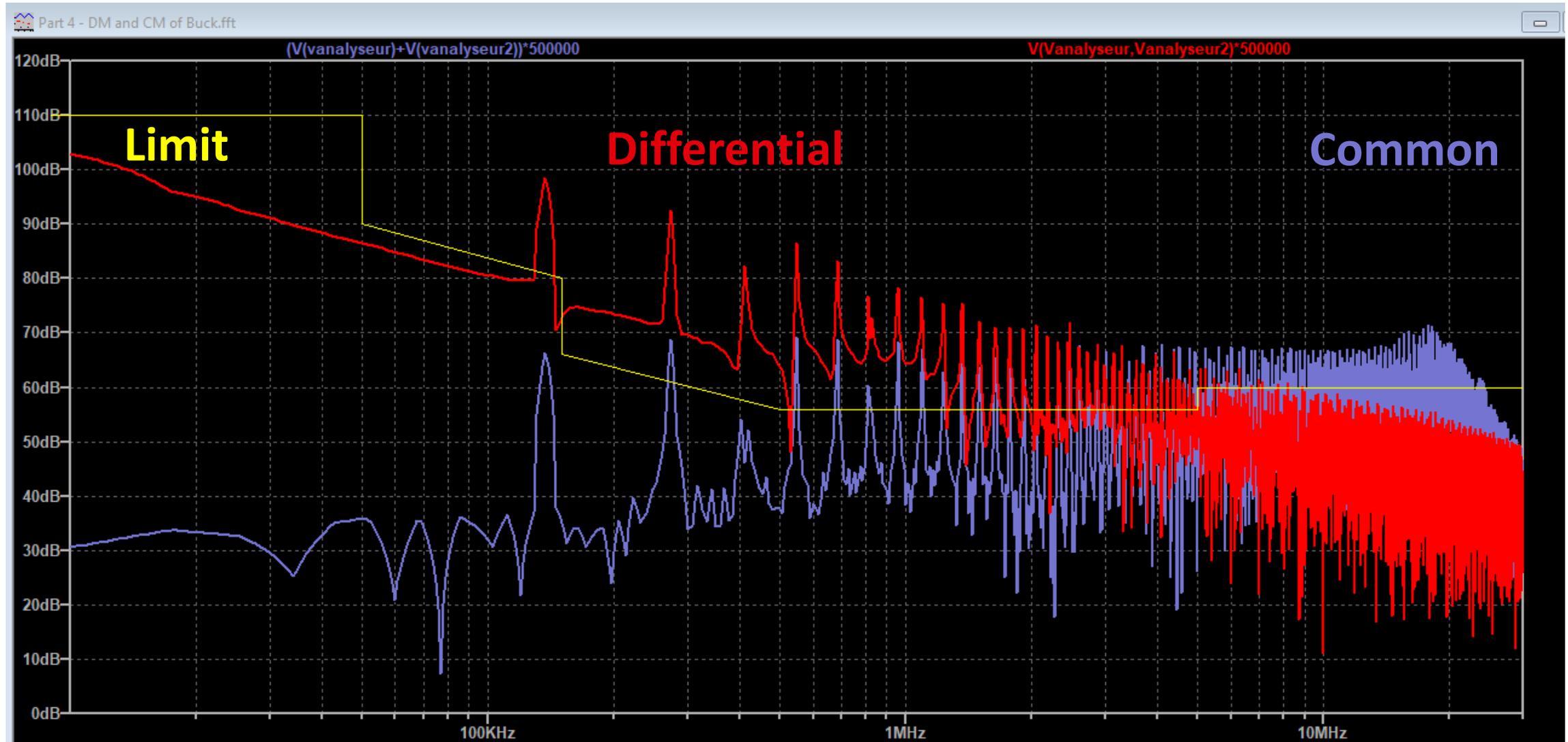
# Reality VS Simulation

## ESR / ESL / CAP breakdown in frequency



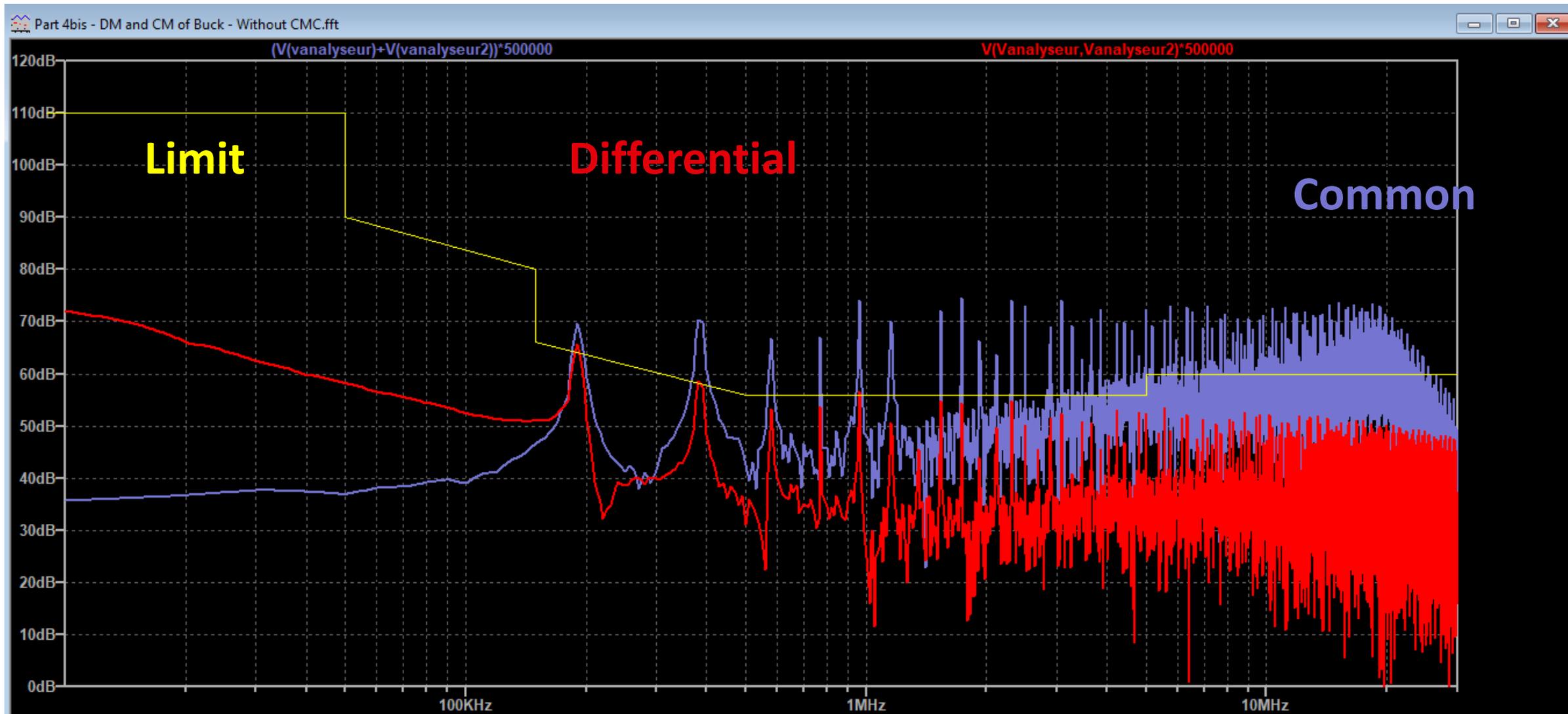
# Going further with simulation

Fixing that buck in the simulation – Before Polymer Cap



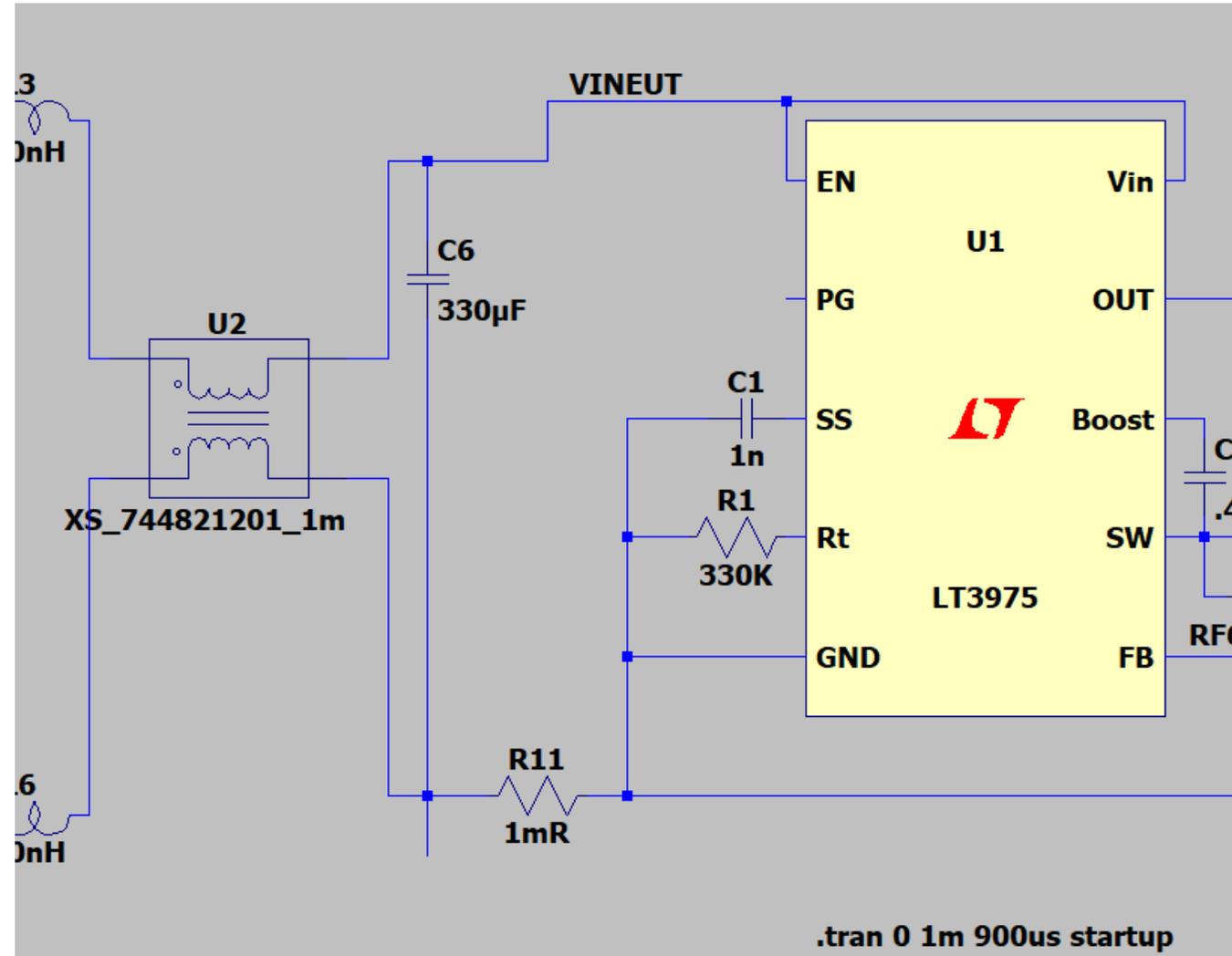
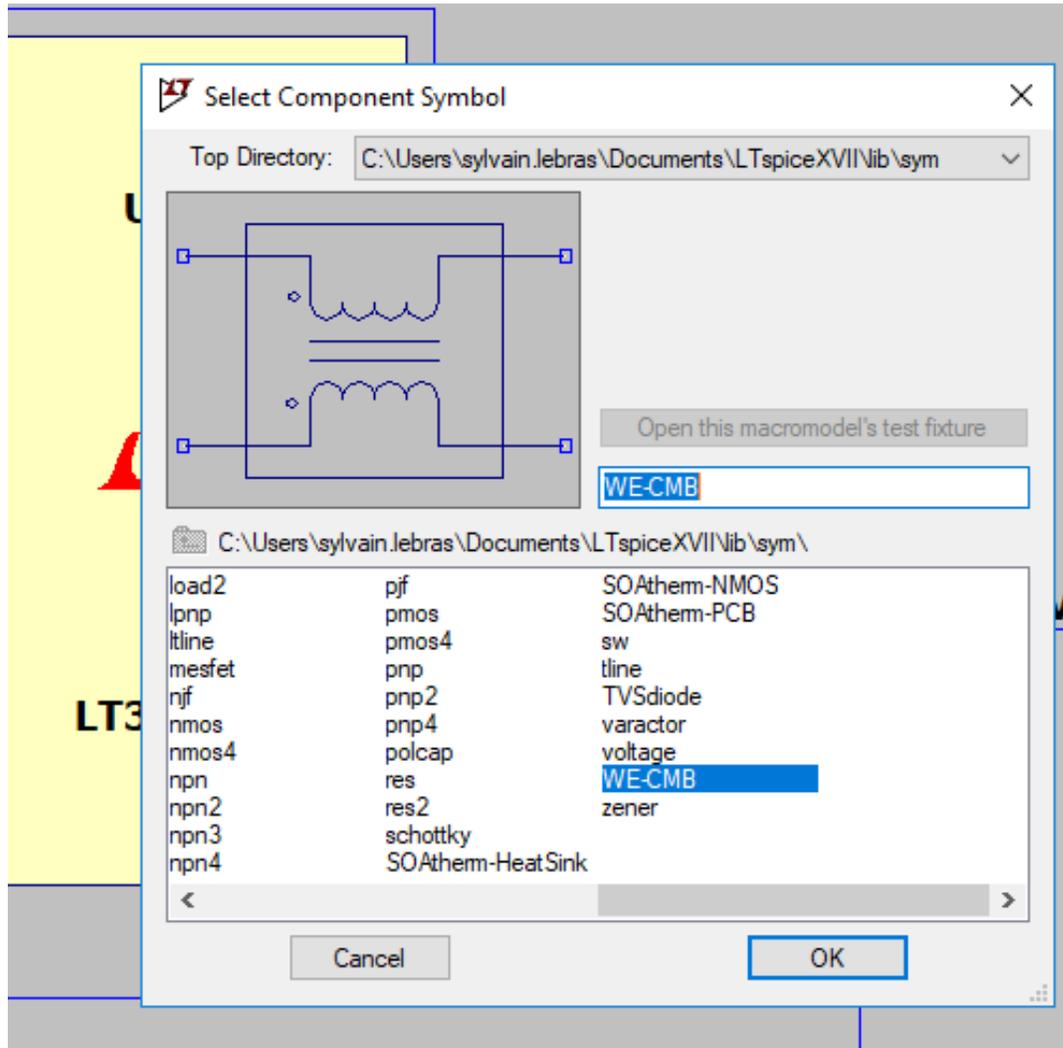
# Going further with simulation

## Fixing that buck in the simulation – After Polymer Cap



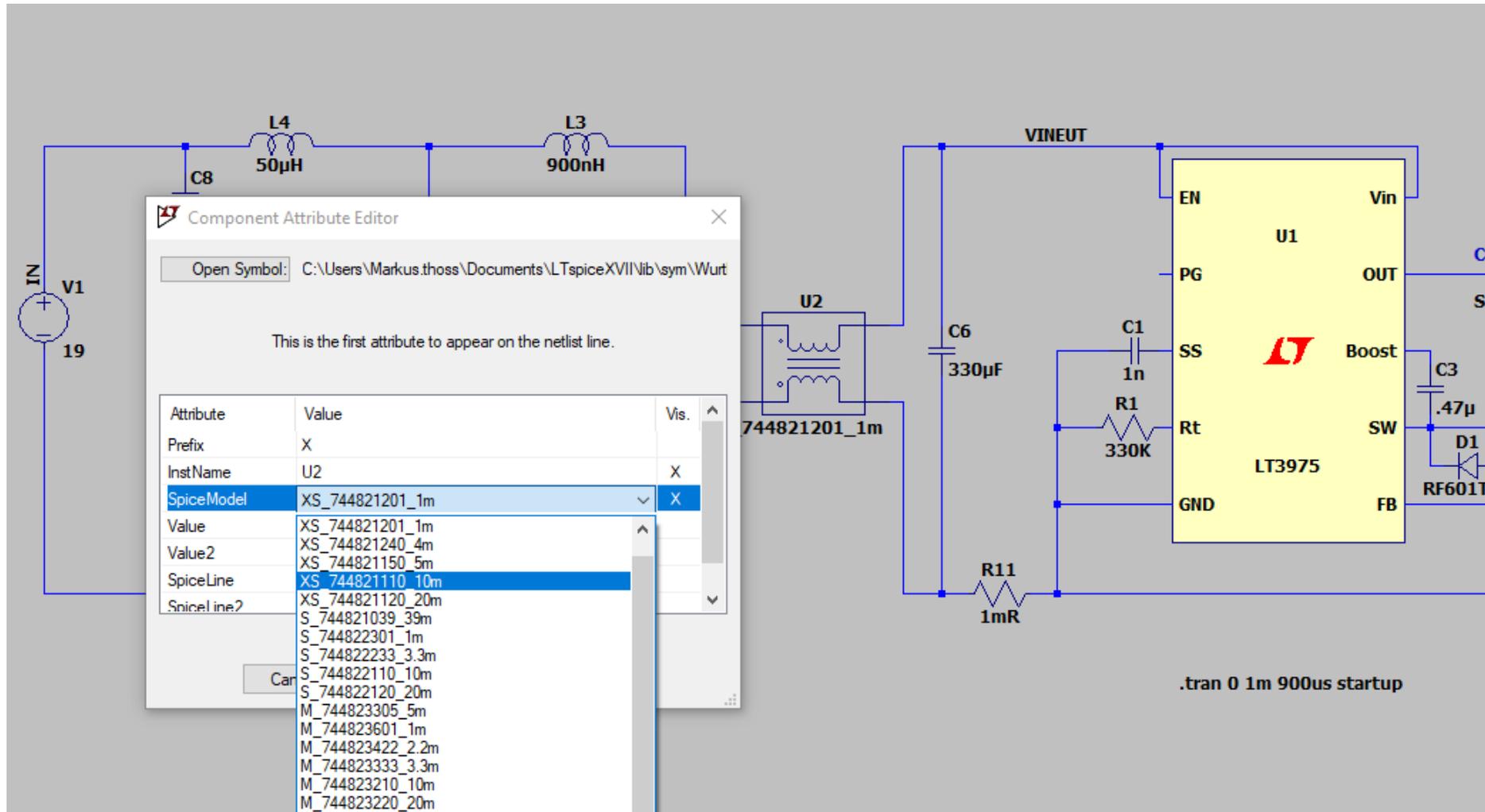
# Going further with simulation

## Fixing that buck in the simulation – Common mode choke



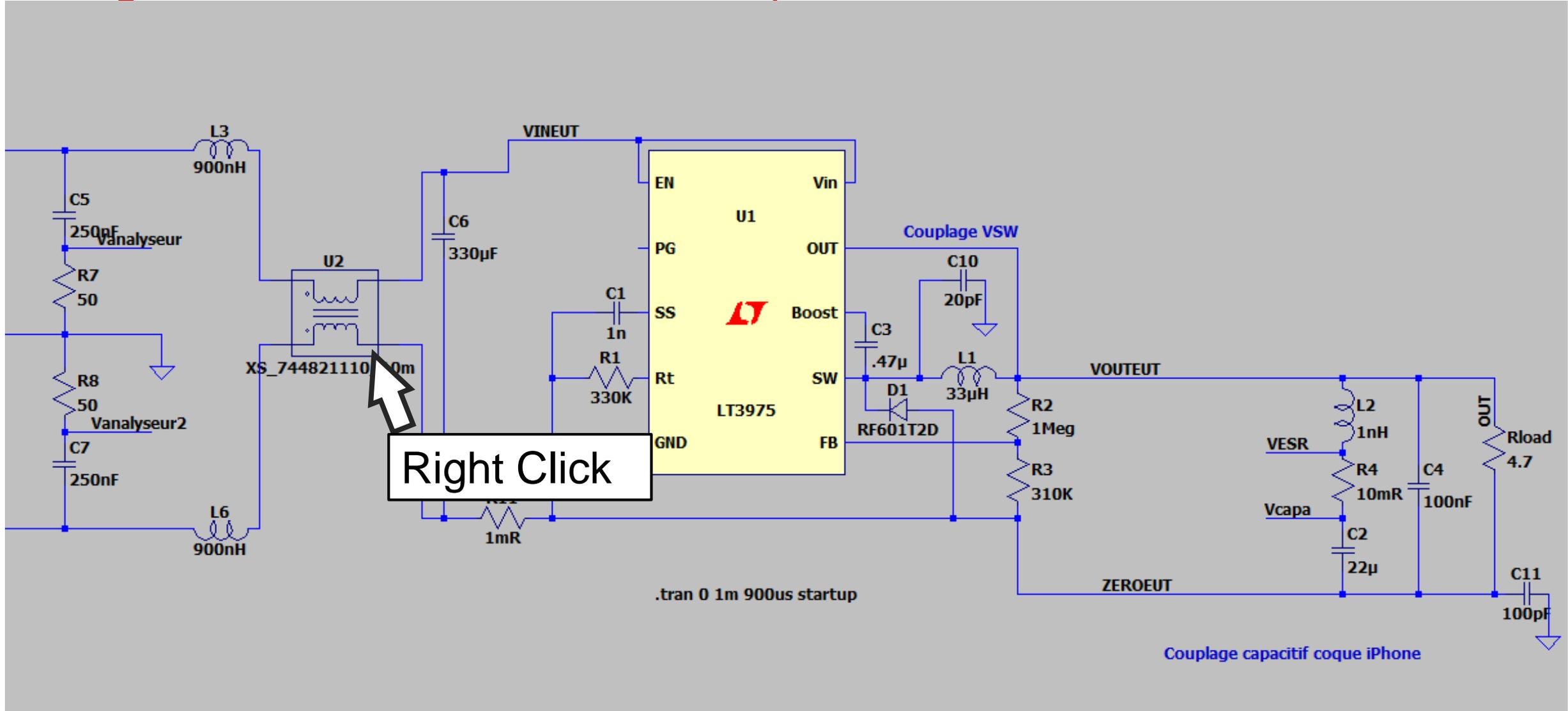
# Going further with simulation

## Fixing that buck in the simulation – Input Common mode choke



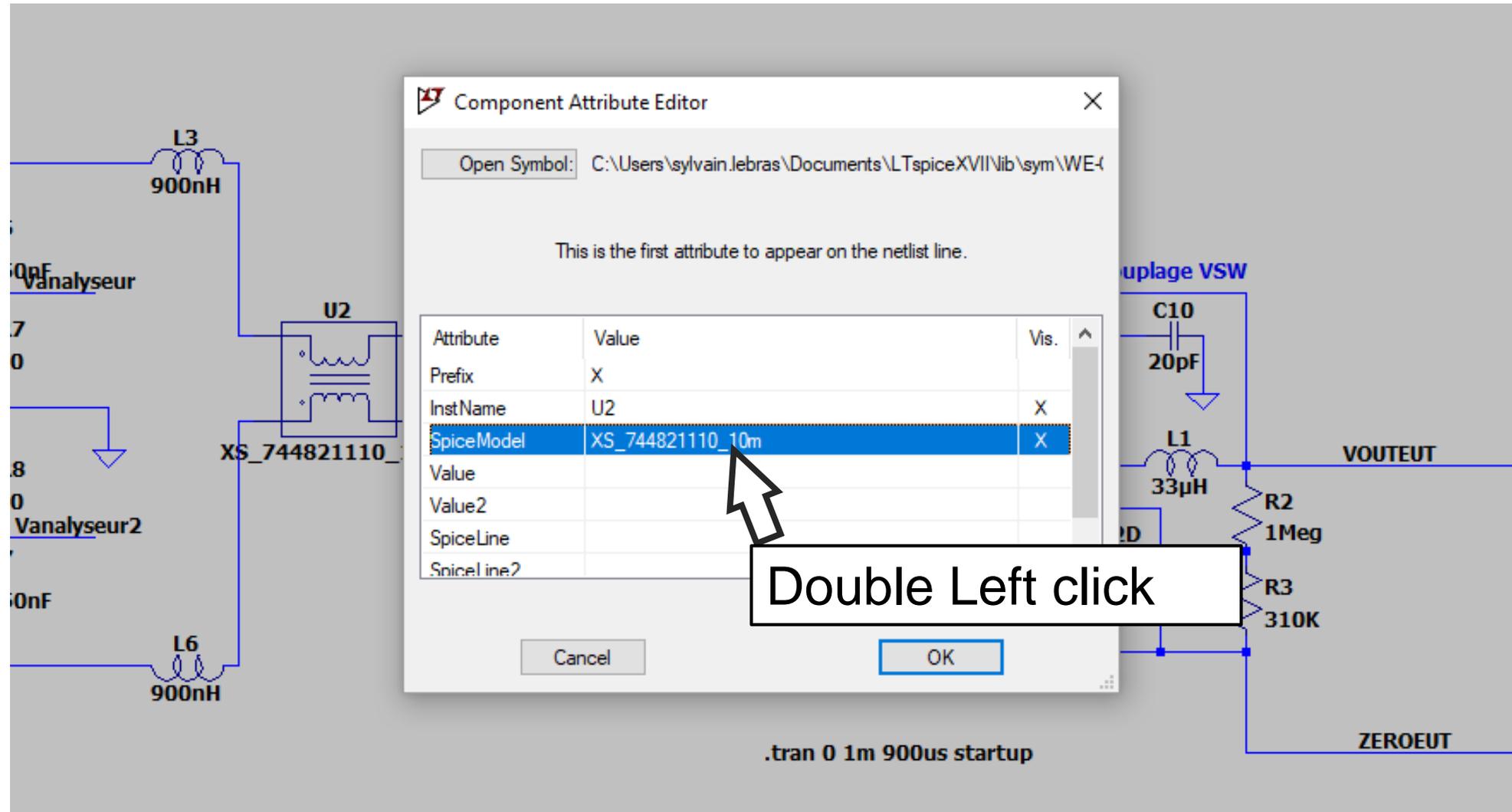
# Going further with simulation

## Fixing that buck in the simulation – Input Common mode choke



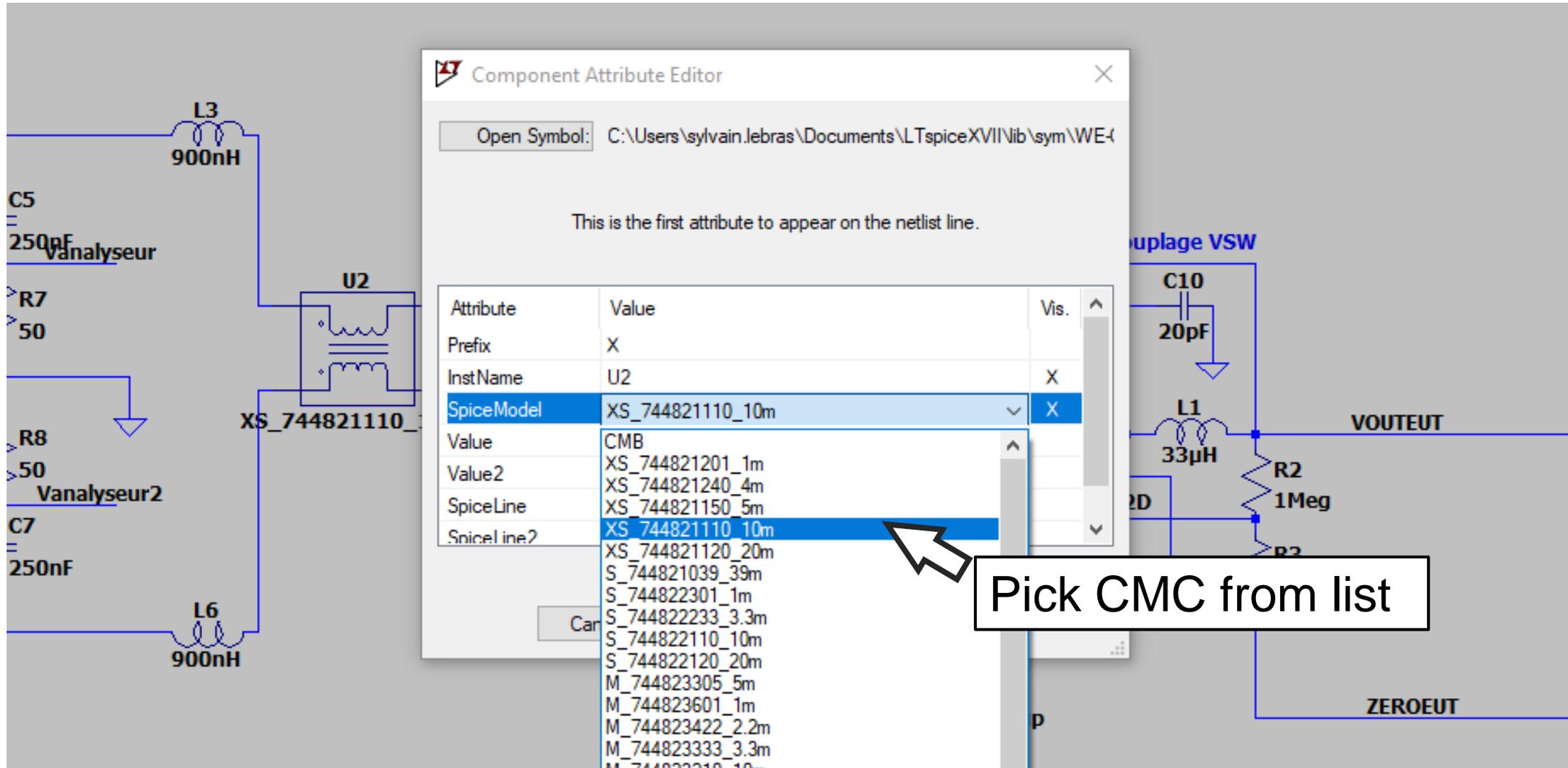
# Going further with simulation

## Fixing that buck in the simulation – Input Common mode choke



# Going further with simulation

## Fixing that buck in the simulation – Input Common mode choke



Component Attribute Editor

Open Symbol: C:\Users\sylvain.lebras\Documents\LTspiceXVII\lib\sym\WE-

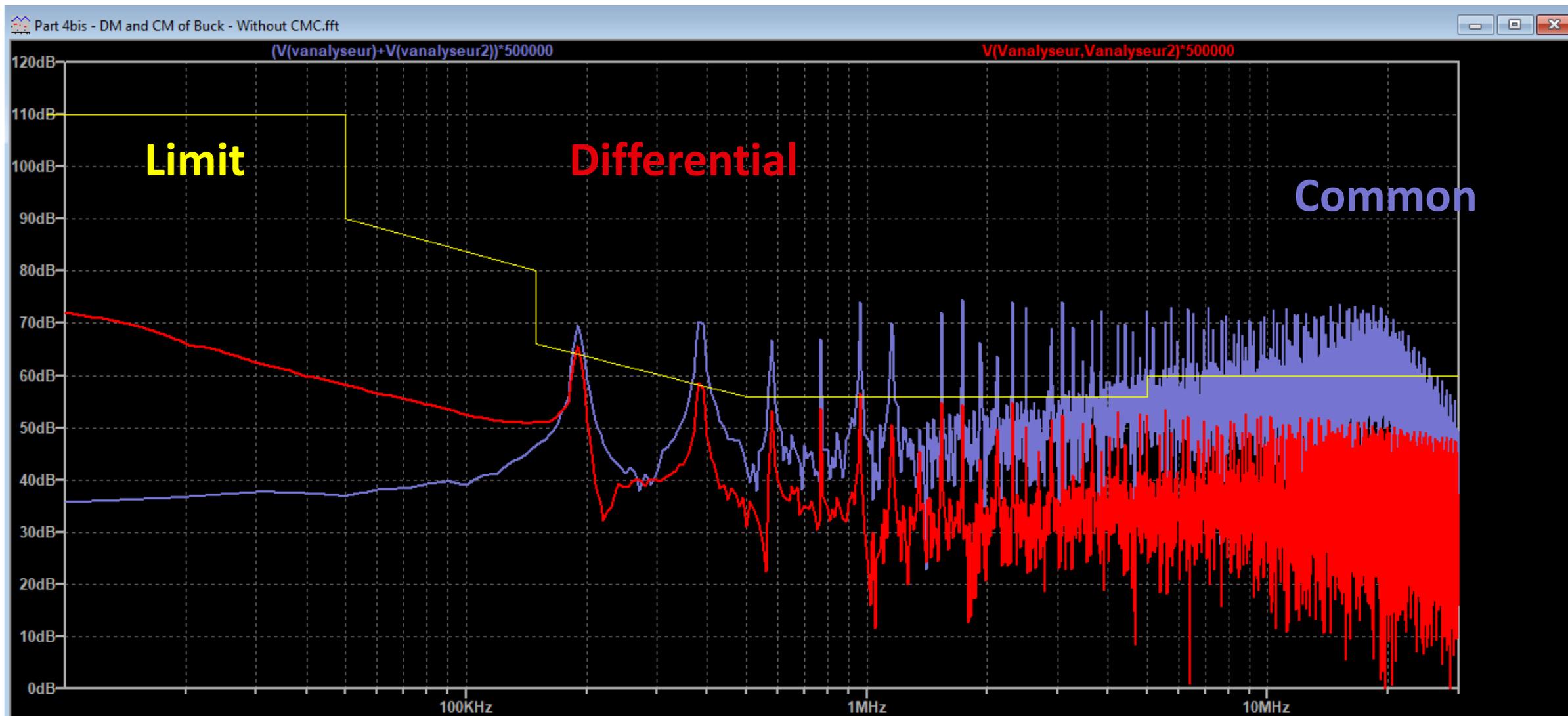
This is the first attribute to appear on the netlist line.

Attribute	Value	Vis.
Prefix	X	
InstName	U2	X
SpiceModel	XS_744821110_10m	X
Value	CMB	
Value2	XS_744821201_1m	
SpiceLine	XS_744821240_4m	
SpiceLine2	XS_744821150_5m	
	XS_744821110_10m	
	XS_744821120_20m	
	S_744821039_39m	
	S_744822301_1m	
	S_744822233_3.3m	
	S_744822110_10m	
	S_744822120_20m	
	M_744823305_5m	
	M_744823601_1m	
	M_744823422_2.2m	
	M_744823333_3.3m	
	M_744822210_10m	

Pick CMC from list

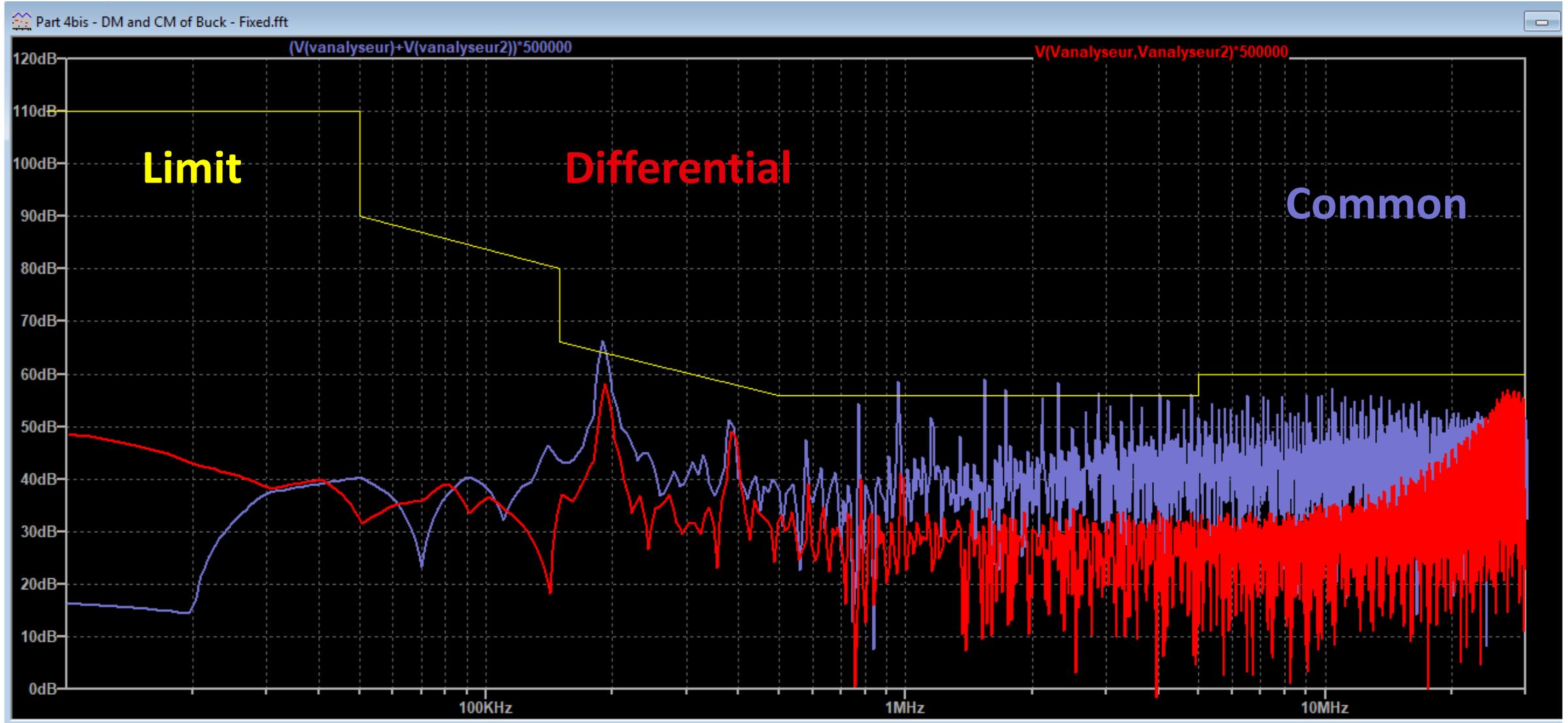
# Going further with simulation

Fixing that buck in the simulation – Without Common mode choke



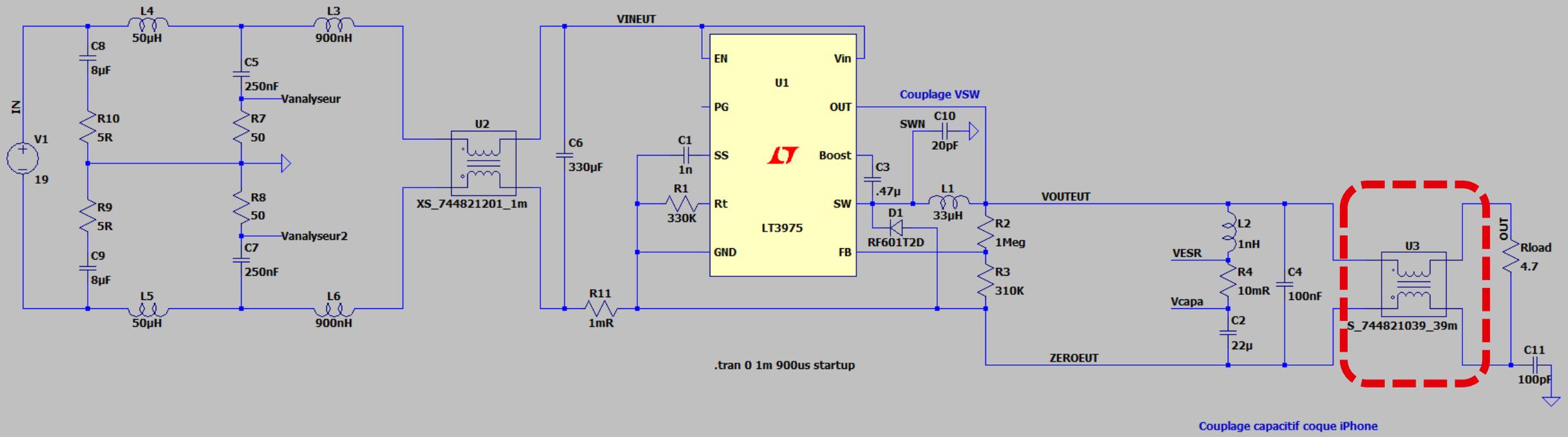
# Going further with simulation

Fixing that buck in the simulation – With input Common mode choke



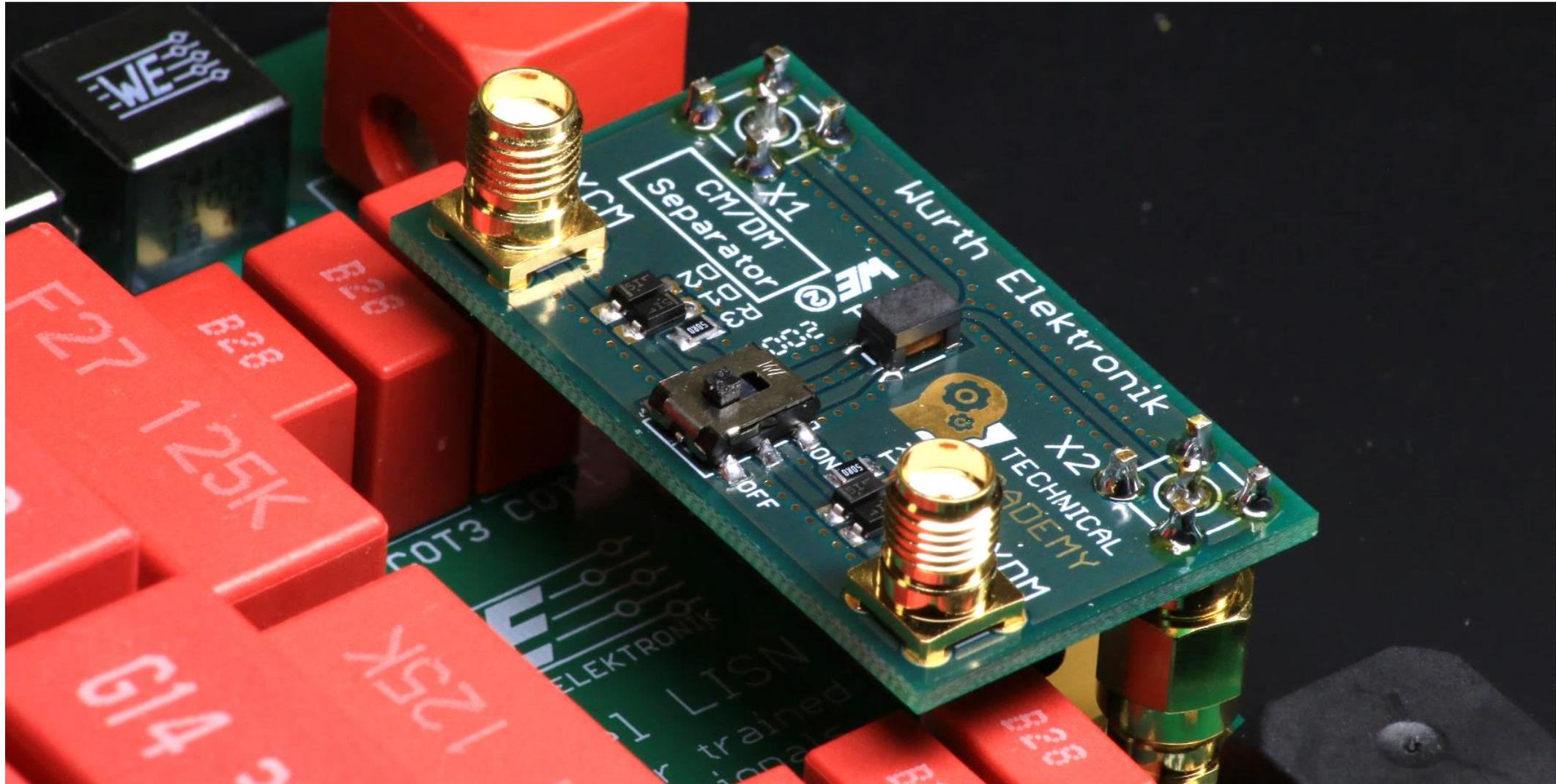
# Going further with simulation

Fixing that buck in the simulation – With output CMC



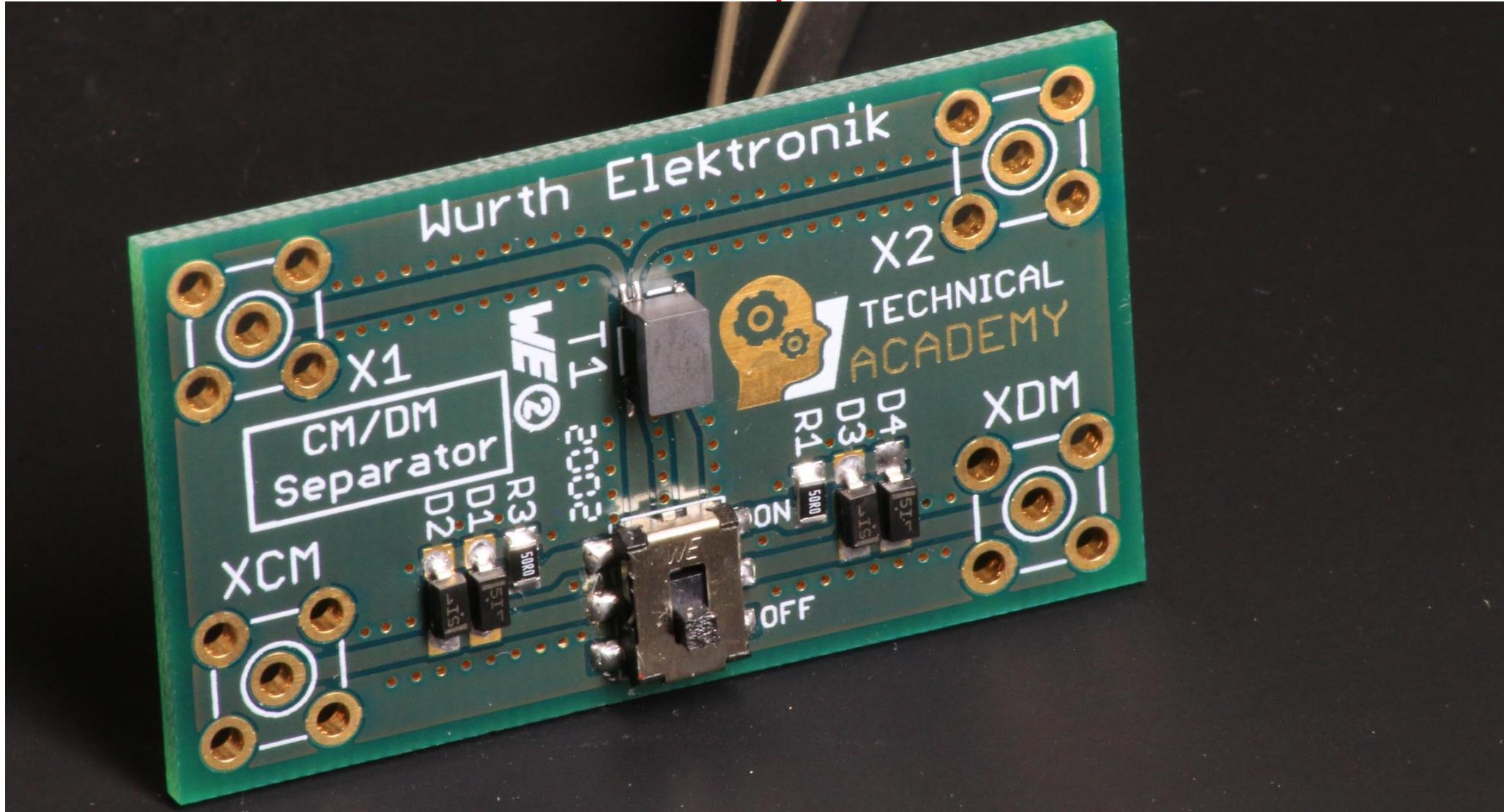
# Going further ?

## Common mode / Differential Mode separator in real life



# Going further ?

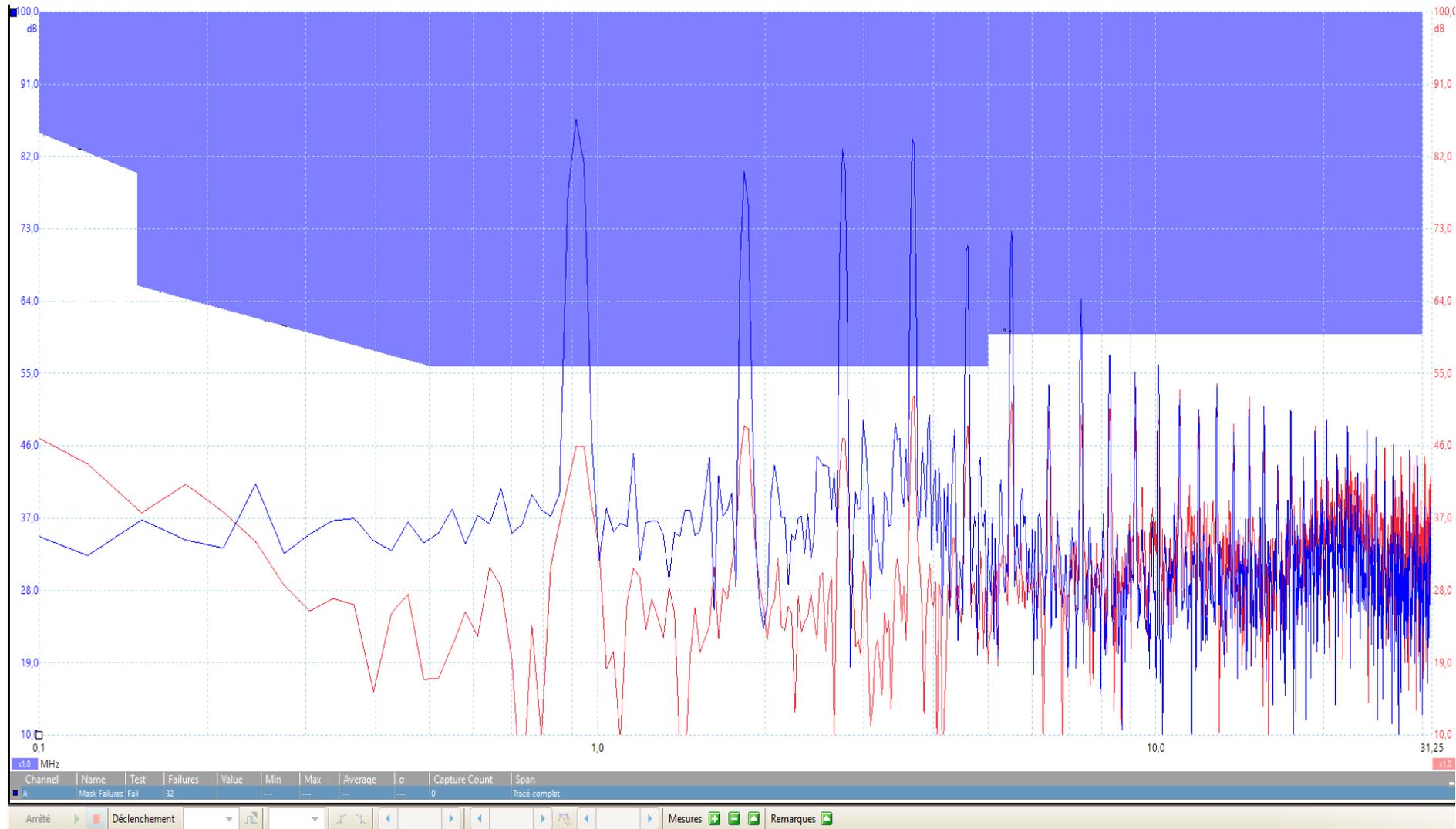
## Common mode / Differential Mode separator in real life





# Going further ?

## Common mode / Differential Mode separator in real life



# Modeling Real life examples

## Flyback converter for lighting applications

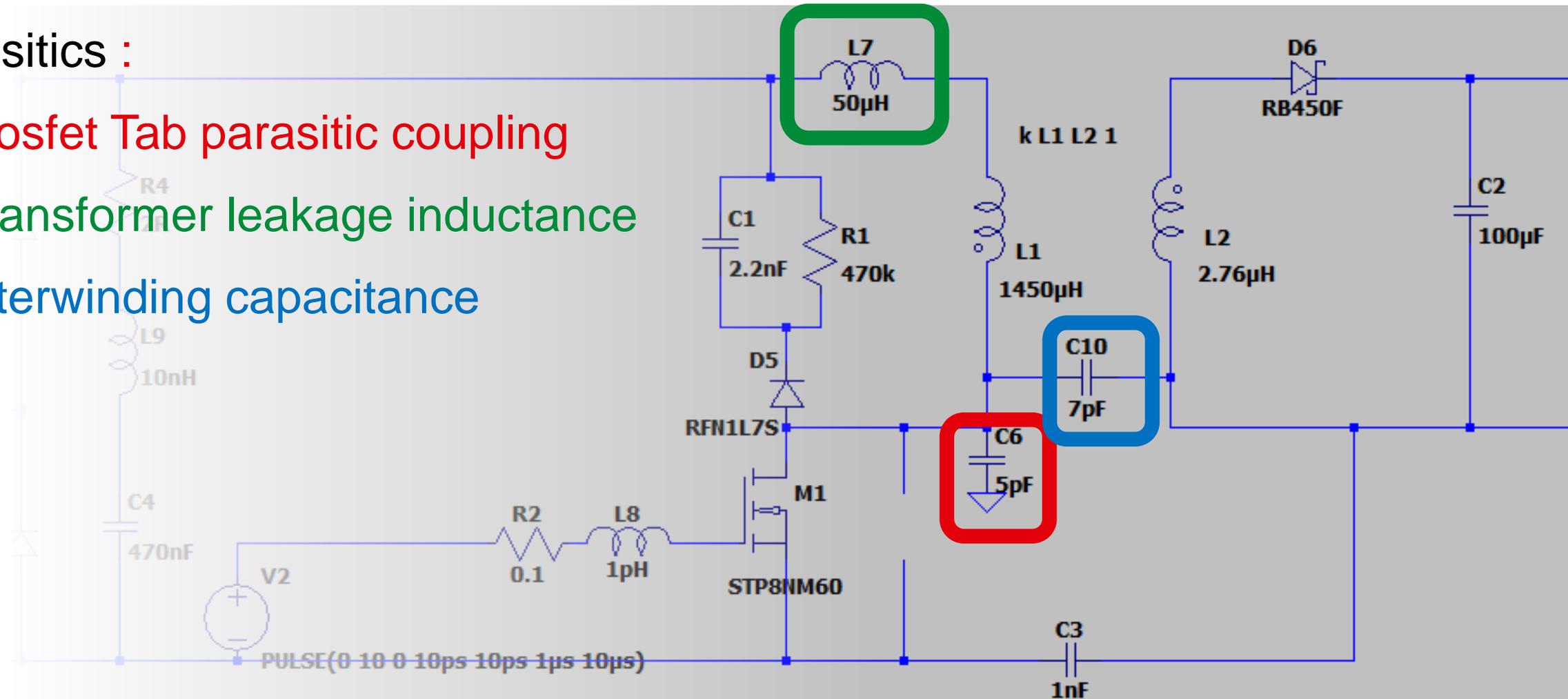


# Modeling Real life examples

## Flyback converter for lighting applications

### Parasitics :

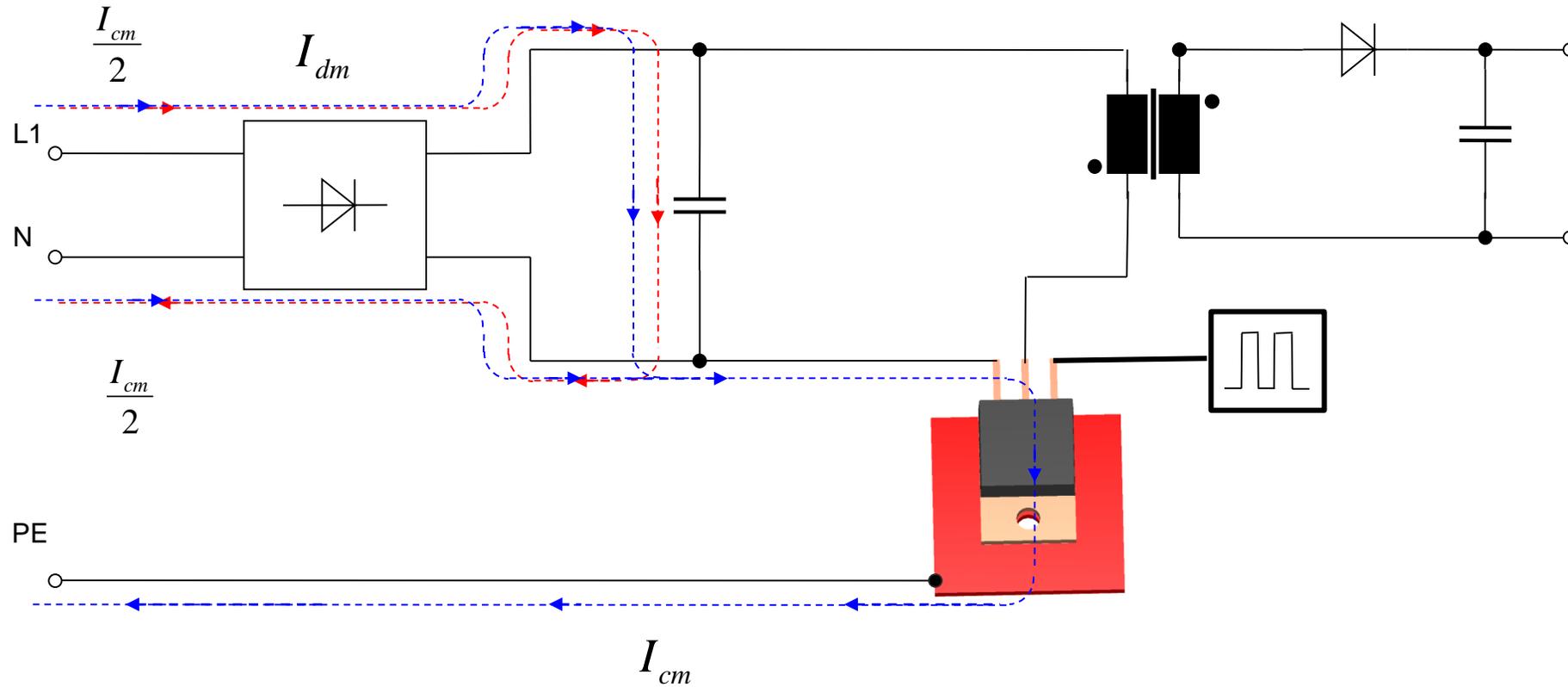
- Mosfet Tab parasitic coupling
- Transformer leakage inductance
- Interwinding capacitance



# Real life examples

## Flyback converter for lighting applications

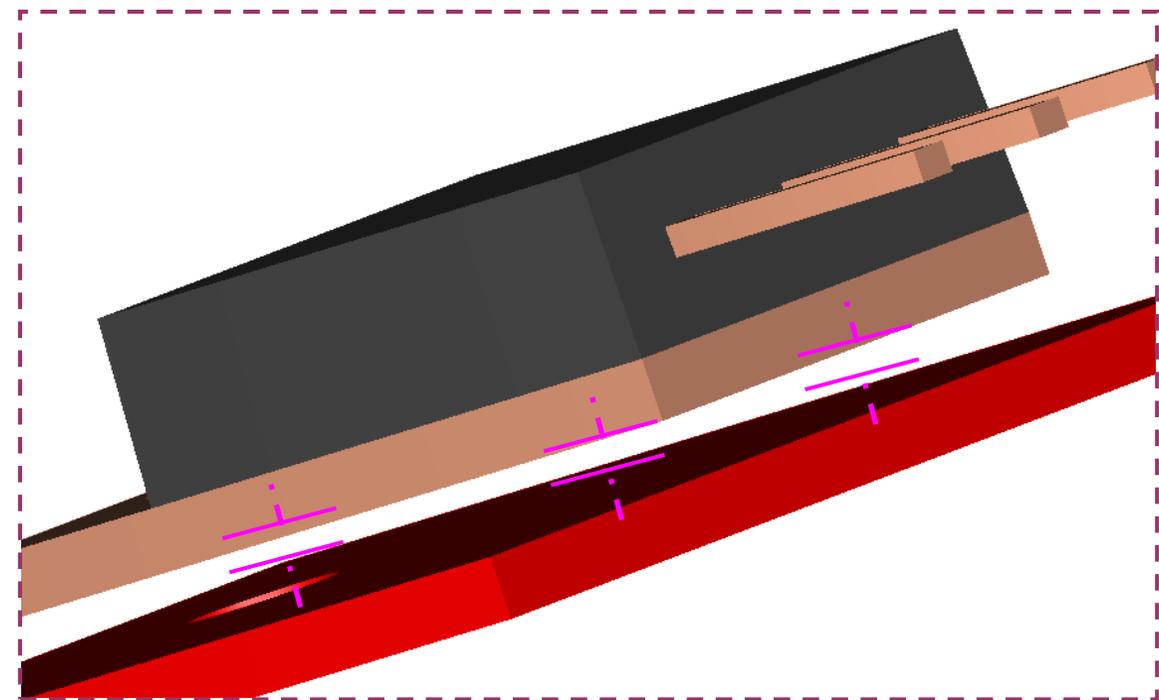
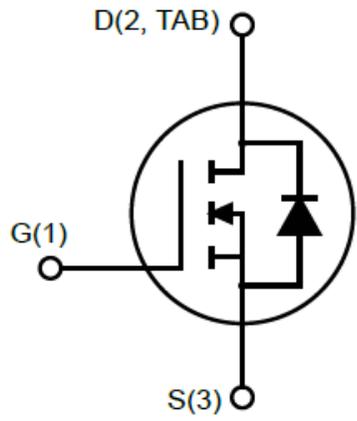
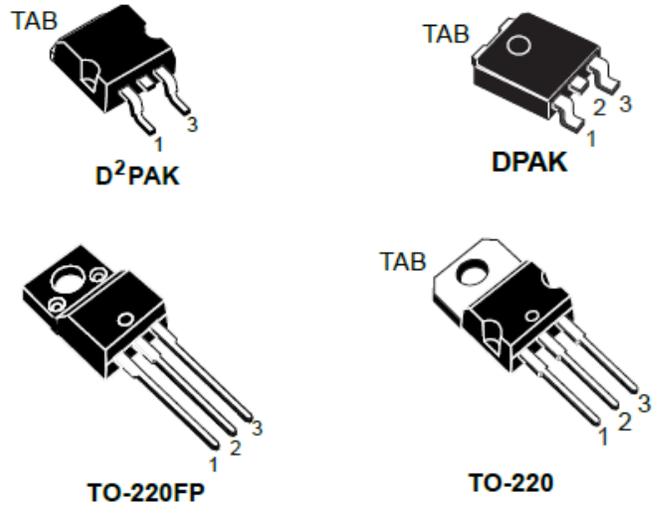
Mosfet Tab parasitic coupling



# Real life examples

## Flyback converter for lighting applications

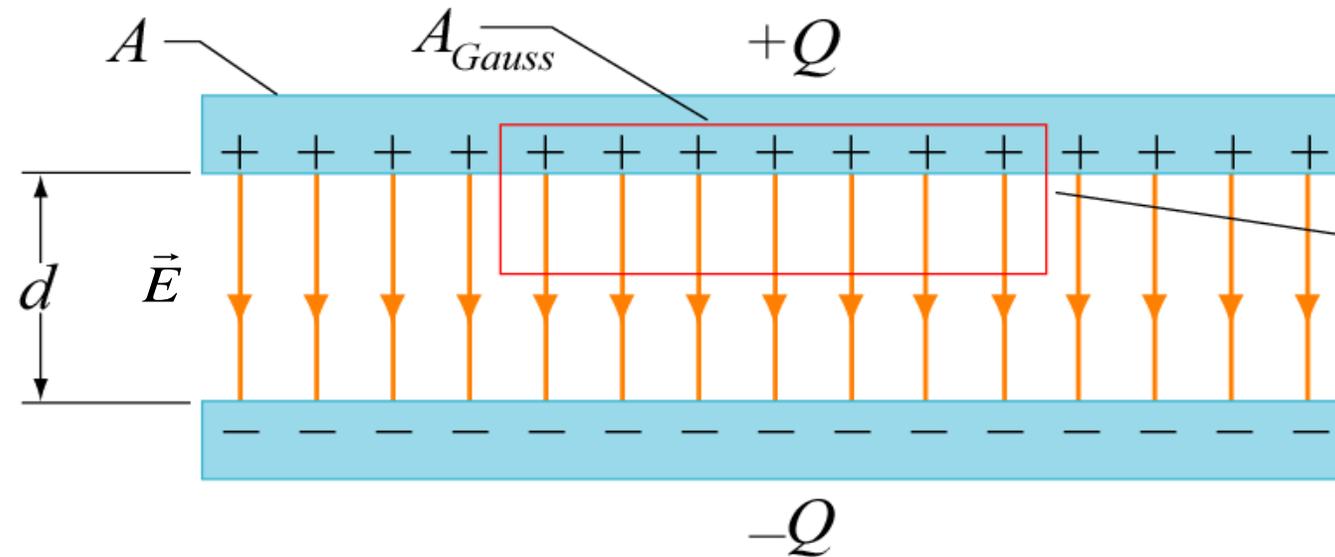
Mosfet Tab parasitic coupling



# Real life examples

## Flyback converter for lighting applications

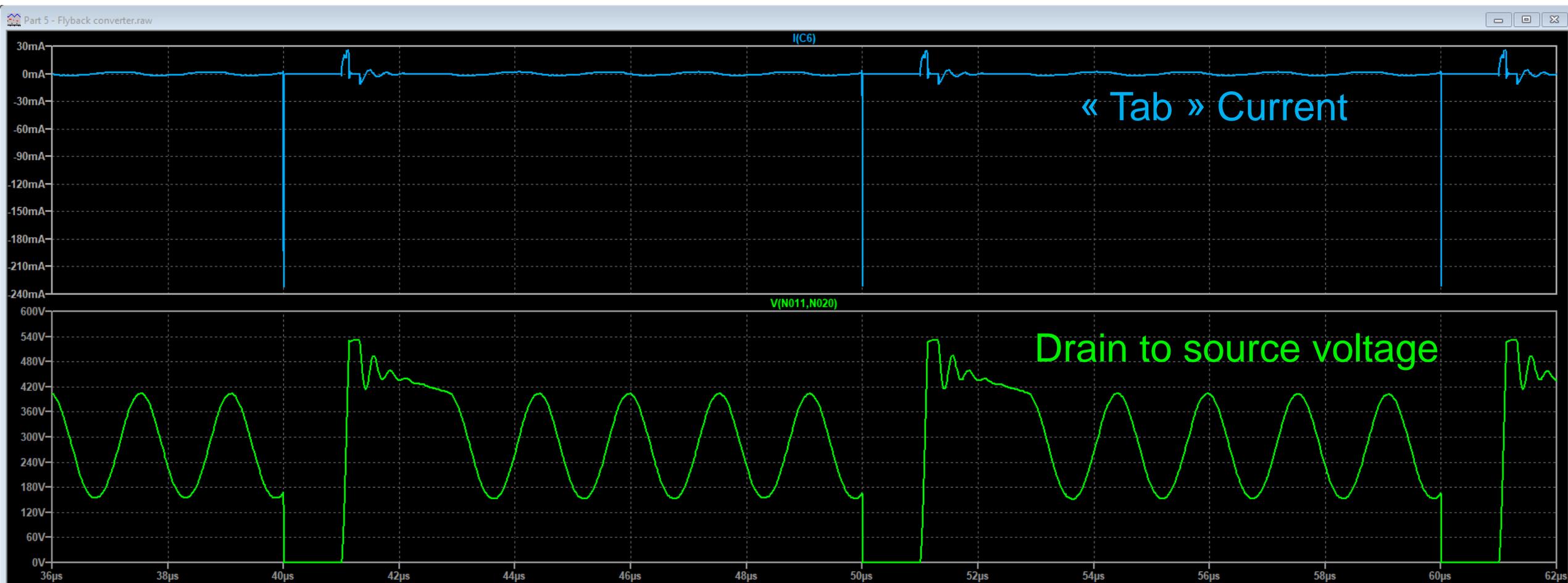
### Mosfet Tab parasitic coupling



$$C = \frac{\epsilon_0 A}{d}$$

# Real life examples

## Flyback converter for lighting applications



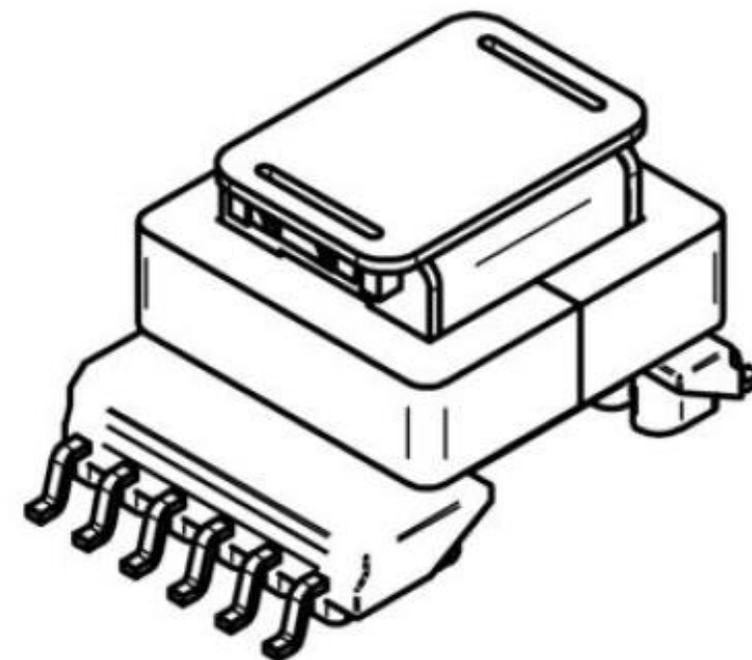
# Real life examples

## Flyback converter for lighting applications

Primary leakage inductance

### D Electrical Properties:

Properties	Test conditions		Value	Unit	Tol.
Inductance	100 kHz/ 100 mV	L	1310	$\mu\text{H}$	$\pm 10\%$
Turns ratio		n	140 : 6 : 6 : 16		$\pm 3\%$
Saturation current	$ \Delta L/L  < 20\%$	$I_{\text{sat}}$	0.8	A	typ.
DC Resistance 1	@ 20°C	$R_{\text{DC1}}$	3000.0	$\text{m}\Omega$	max.
DC Resistance 2	@ 20°C	$R_{\text{DC2}}$	25.0	$\text{m}\Omega$	max.
DC Resistance 3	@ 20°C	$R_{\text{DC3}}$	25.0	$\text{m}\Omega$	max.
DC Resistance 4	@ 20°C	$R_{\text{DC4}}$	450.0	$\text{m}\Omega$	max.
Leakage inductance	100 kHz/ 100 mV	$L_{\text{S}}$	40.0	$\mu\text{H}$	max.
Insulation test voltage	W1,4 => W2,3	$U_{\text{T}}$	4000	V (AC)	



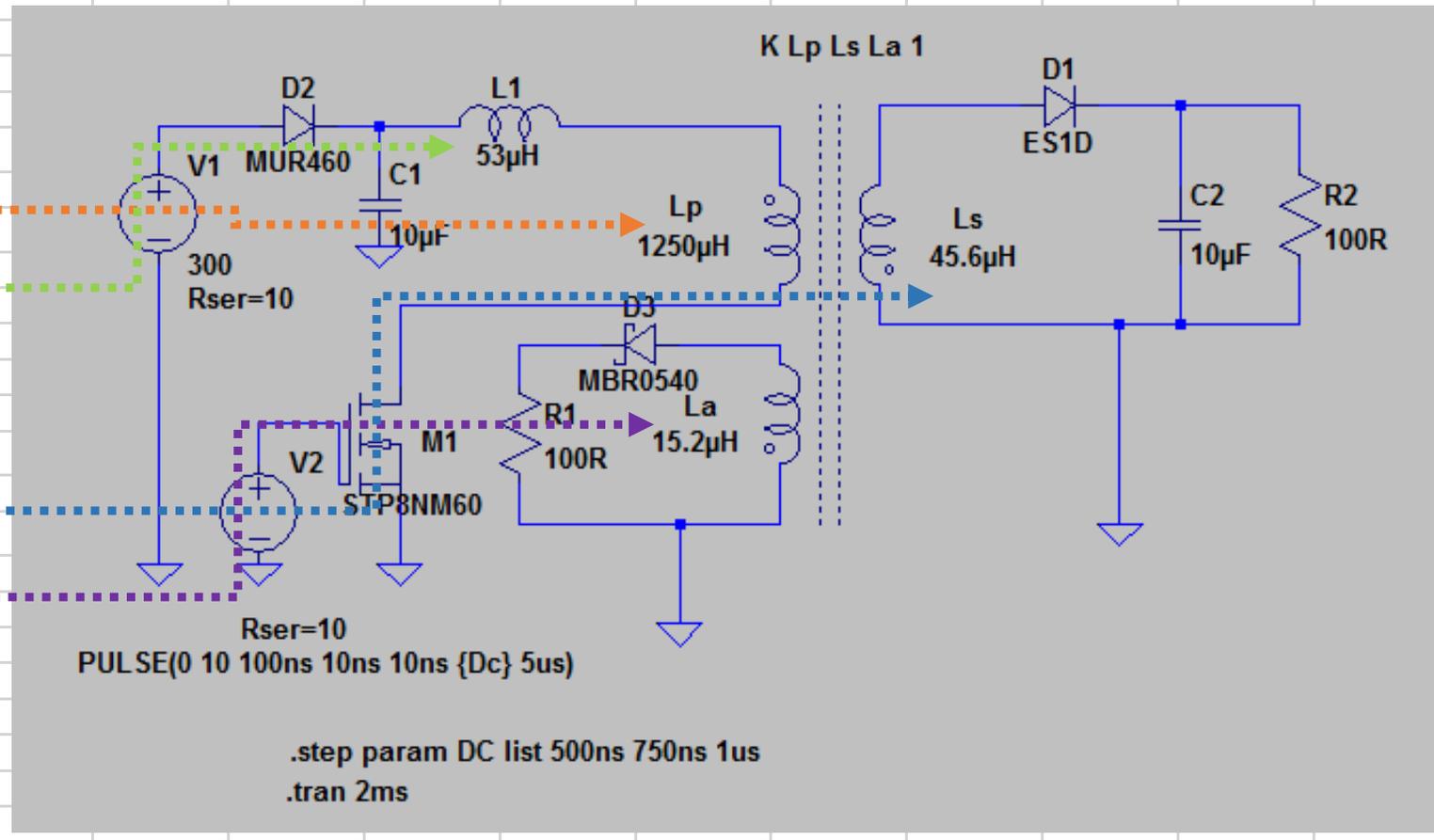
**WE-UOST**

# Real life examples

## Turn ratio to inductance ?

Transformers : from datasheet to LTSpice model

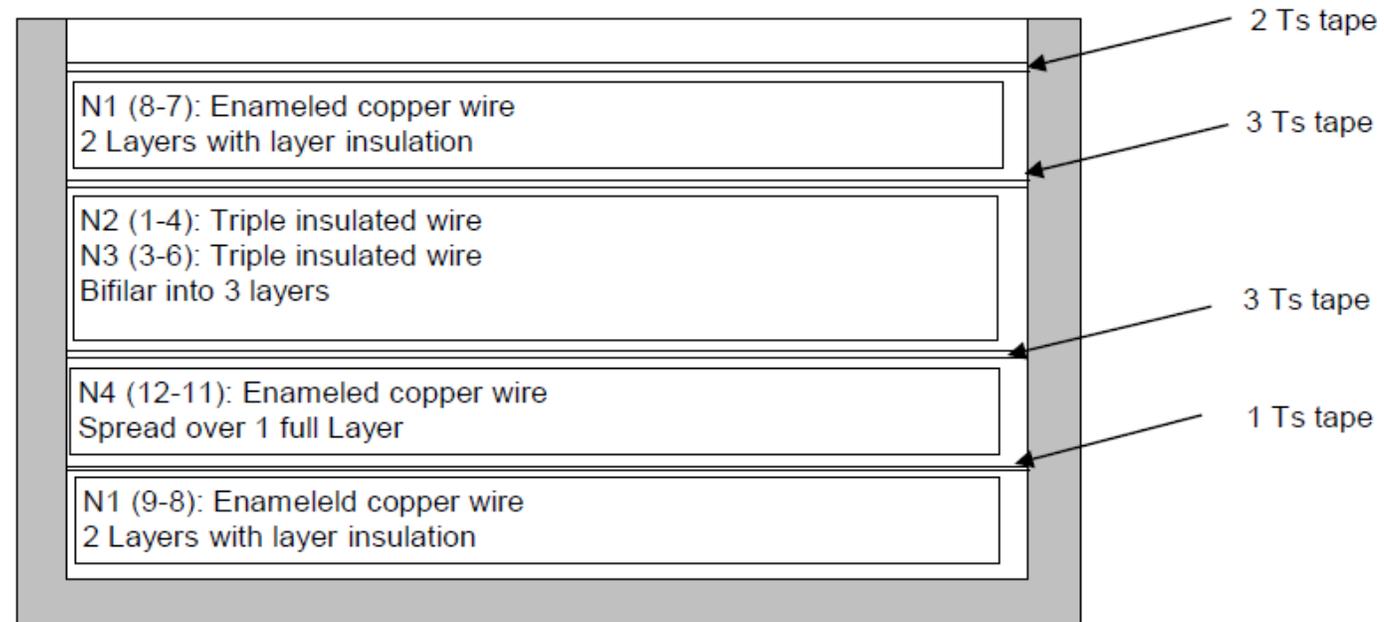
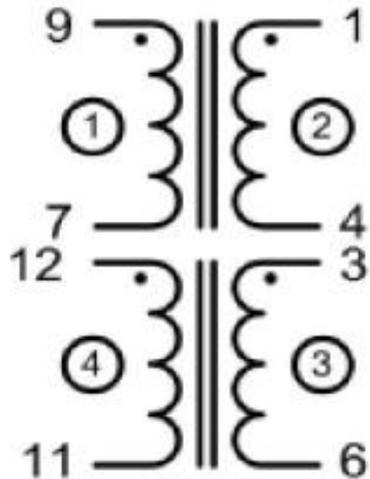
Primary inductance			
			1310 $\mu\text{H}$
Leakage inductance			
			50 $\mu\text{H}$
Ratio	Primary	Secondary	Aux
	130	6	16
Secondary inductance			
			2.79 $\mu\text{H}$
Auxiliary inductance			
			19.84 $\mu\text{H}$



# Real life examples

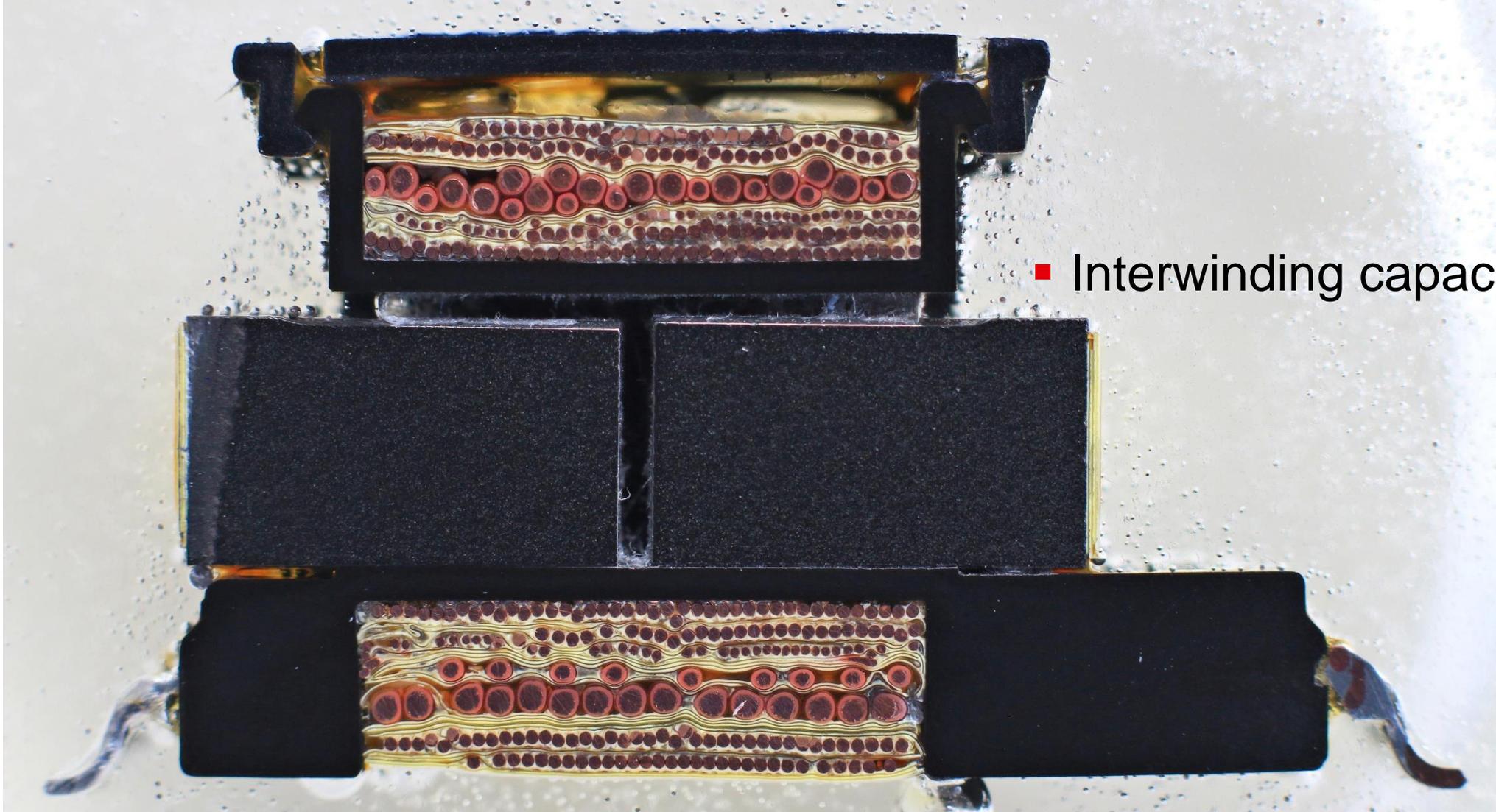
## Flyback converter for lighting applications

- Interwinding capacitance ?



# Real life examples

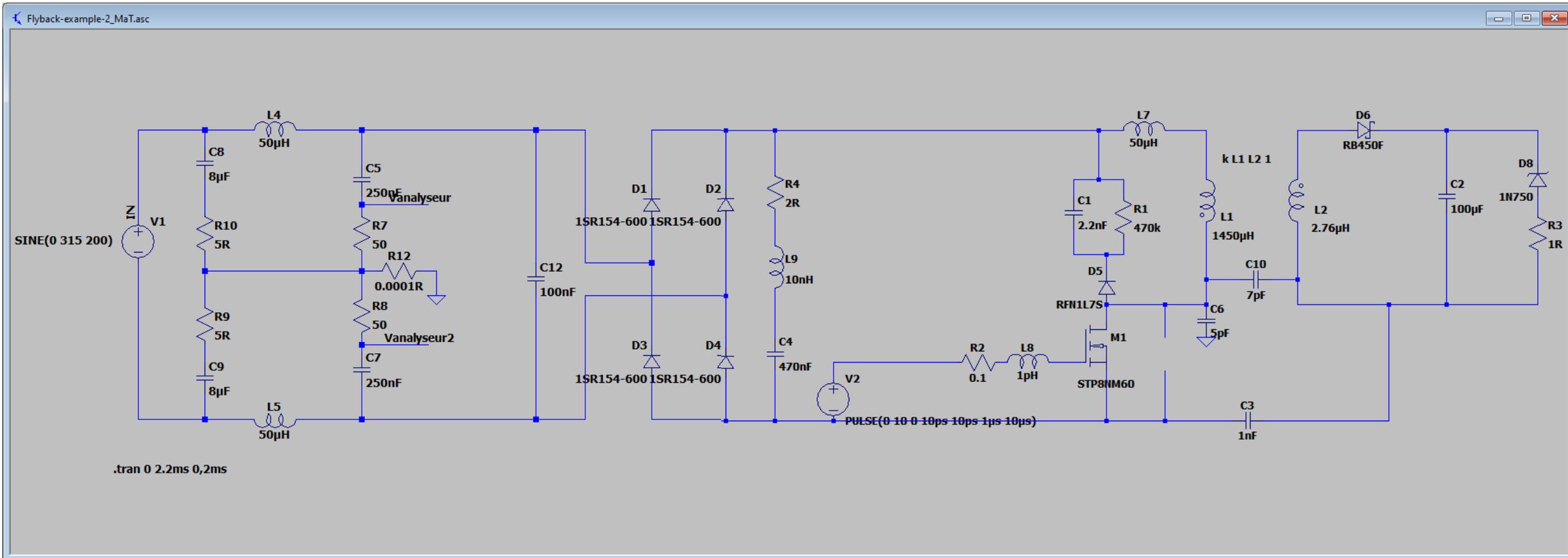
## Flyback converter for lighting applications



- Interwinding capacitance ?

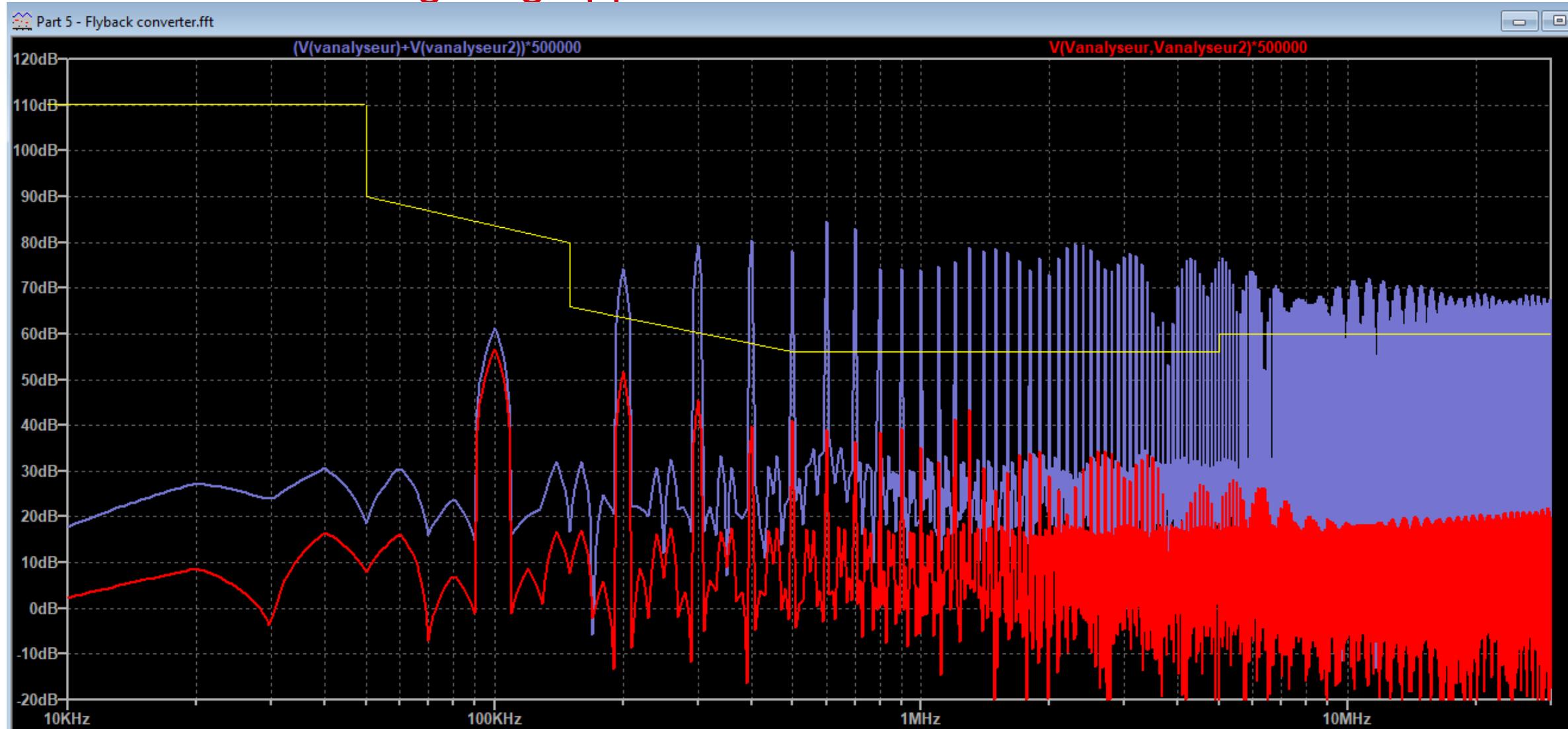
# Real life examples

## Flyback converter for lighting applications



# Real life examples

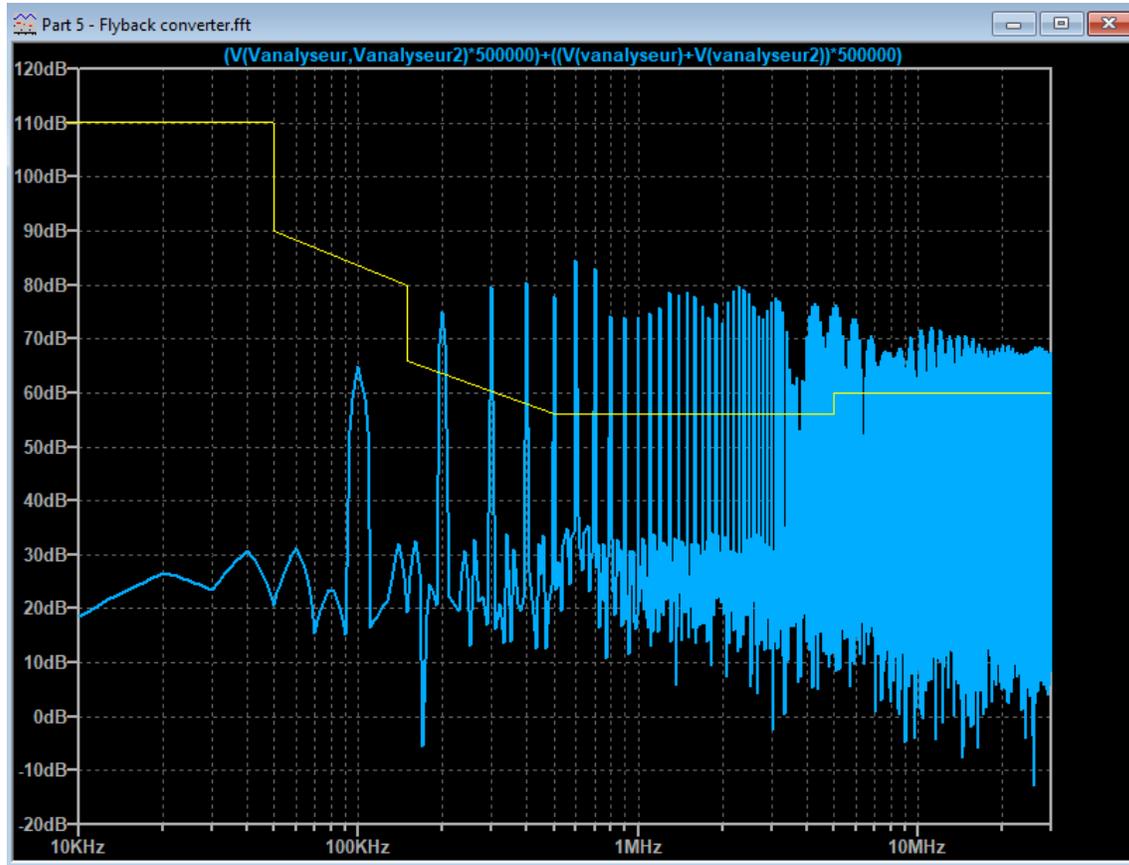
## Flyback converter for lighting applications



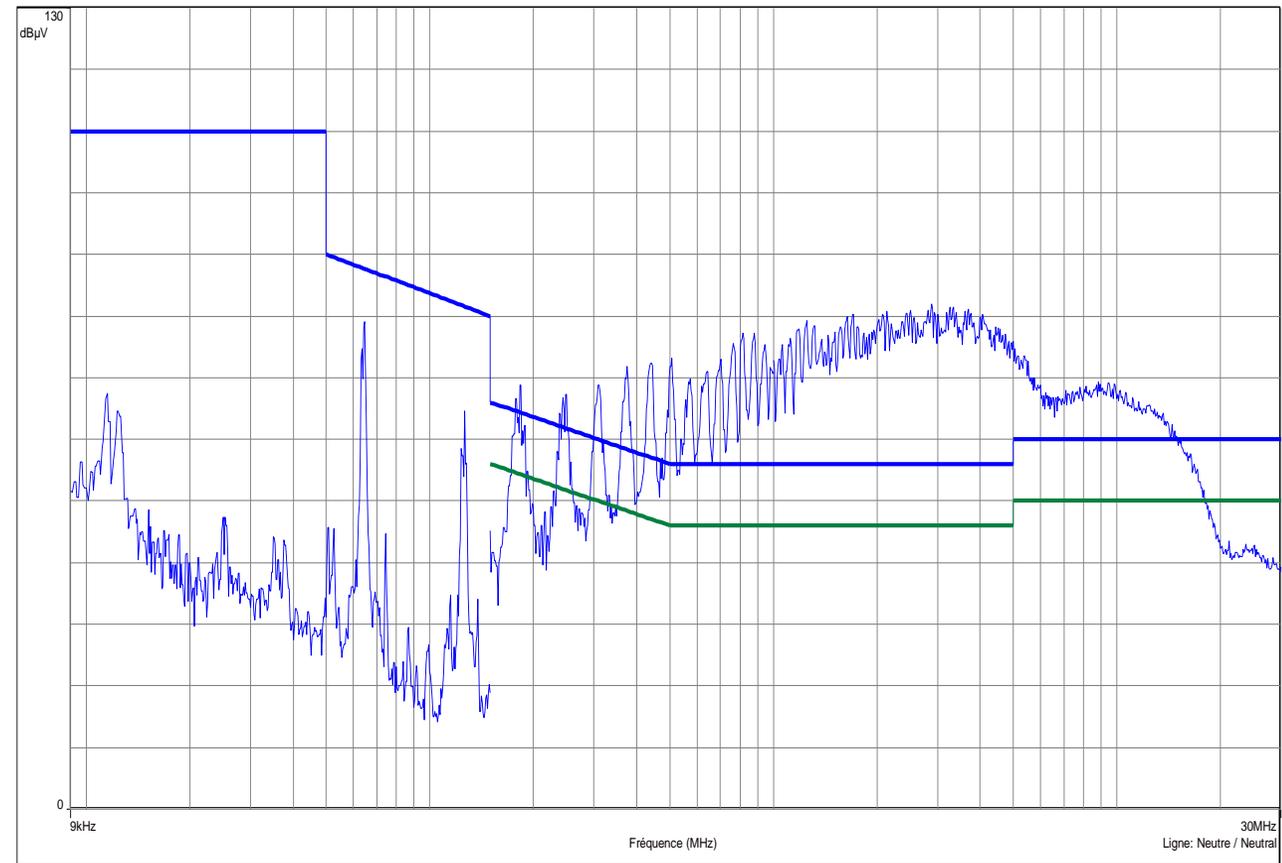
# Real life examples

## Flyback converter for lighting applications

### Simulation



### Example of actual measurement



# Real life examples

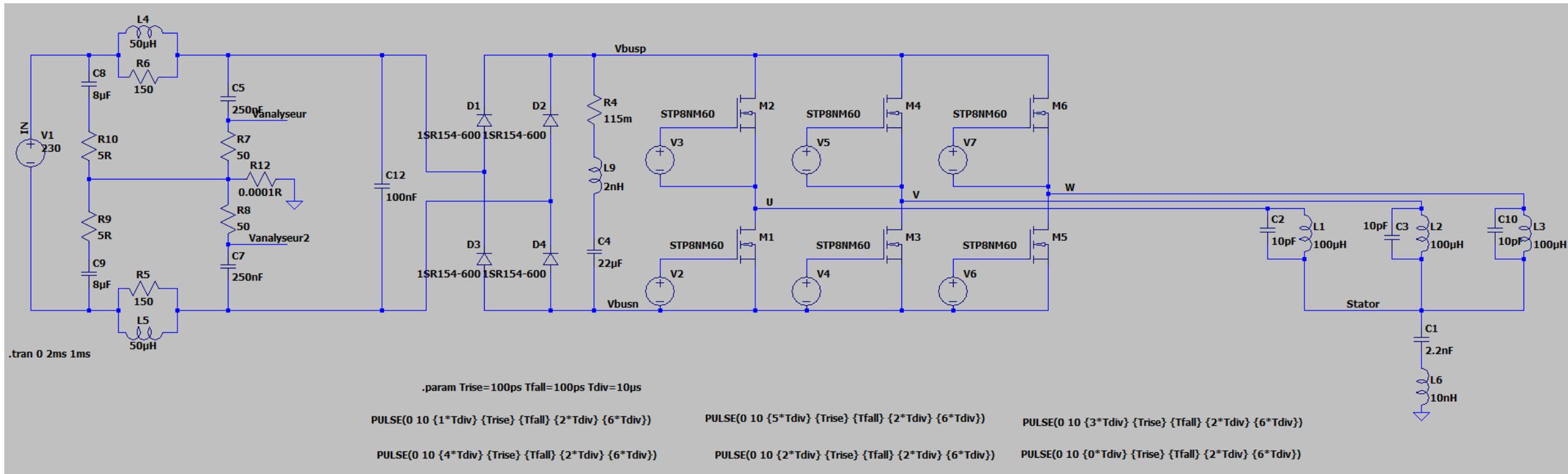
## Mains voltage BLDC driver + motor



# Real life examples

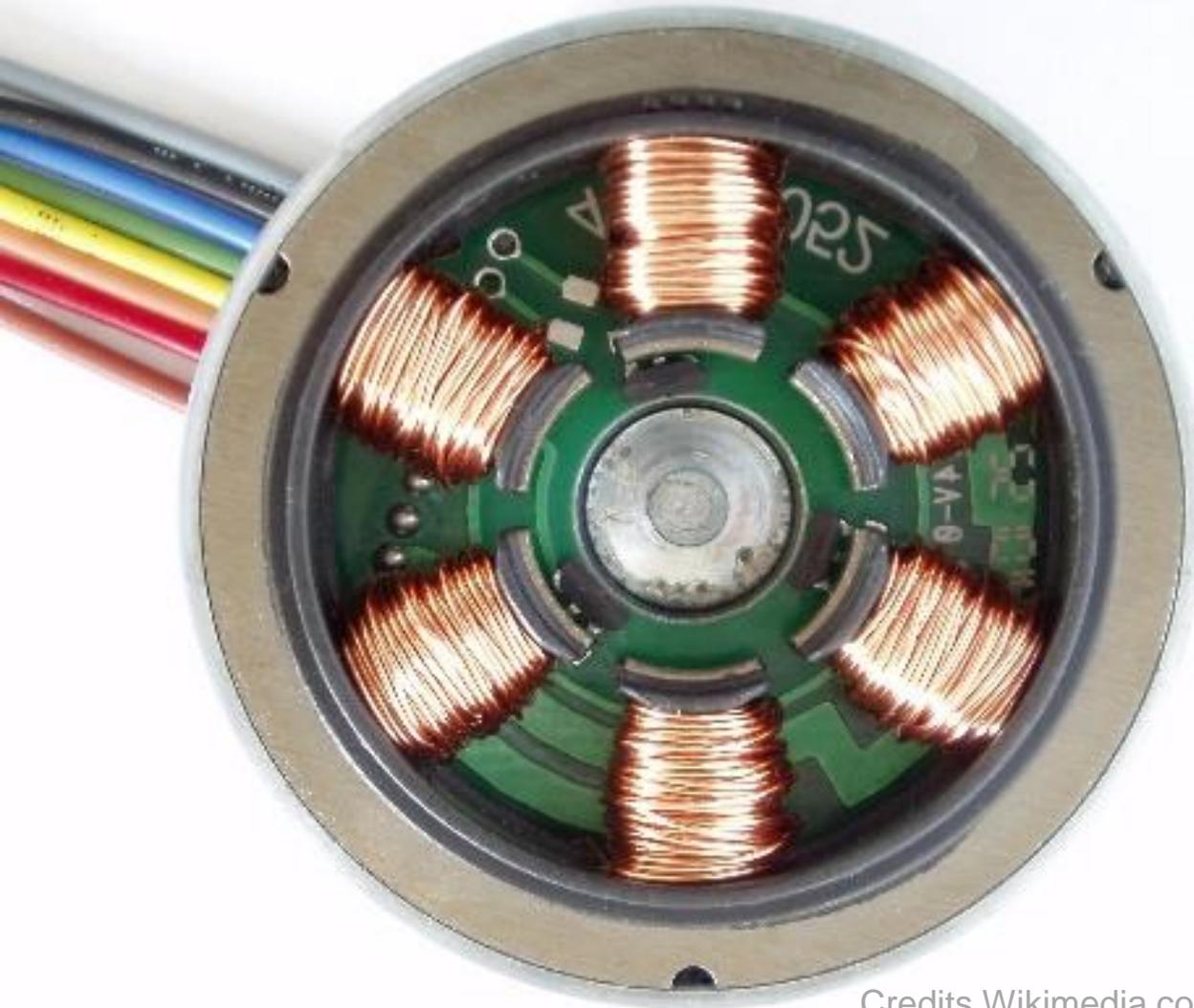
## Mains voltage BLDC driver + motor

- Parasitic coupling to and through stator
- Influence of grounding
- Slew rate of driver
- Dead time impact



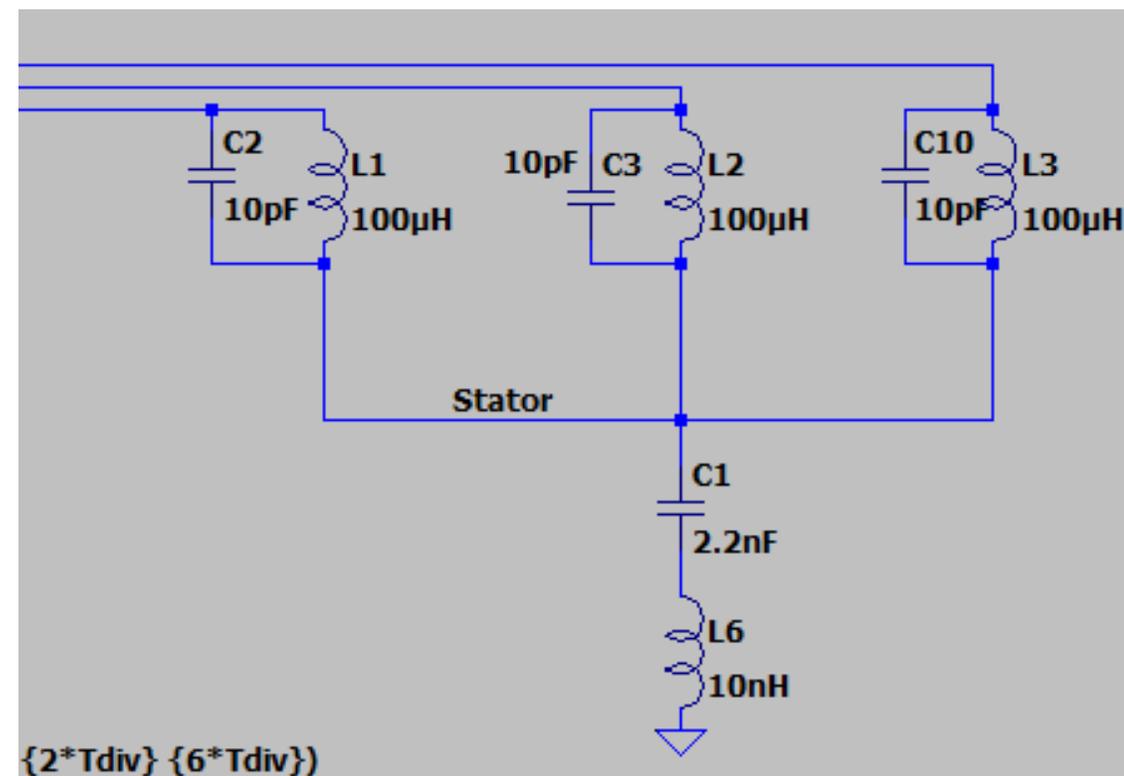
# Real life examples

## Mains voltage BLDC driver + motor



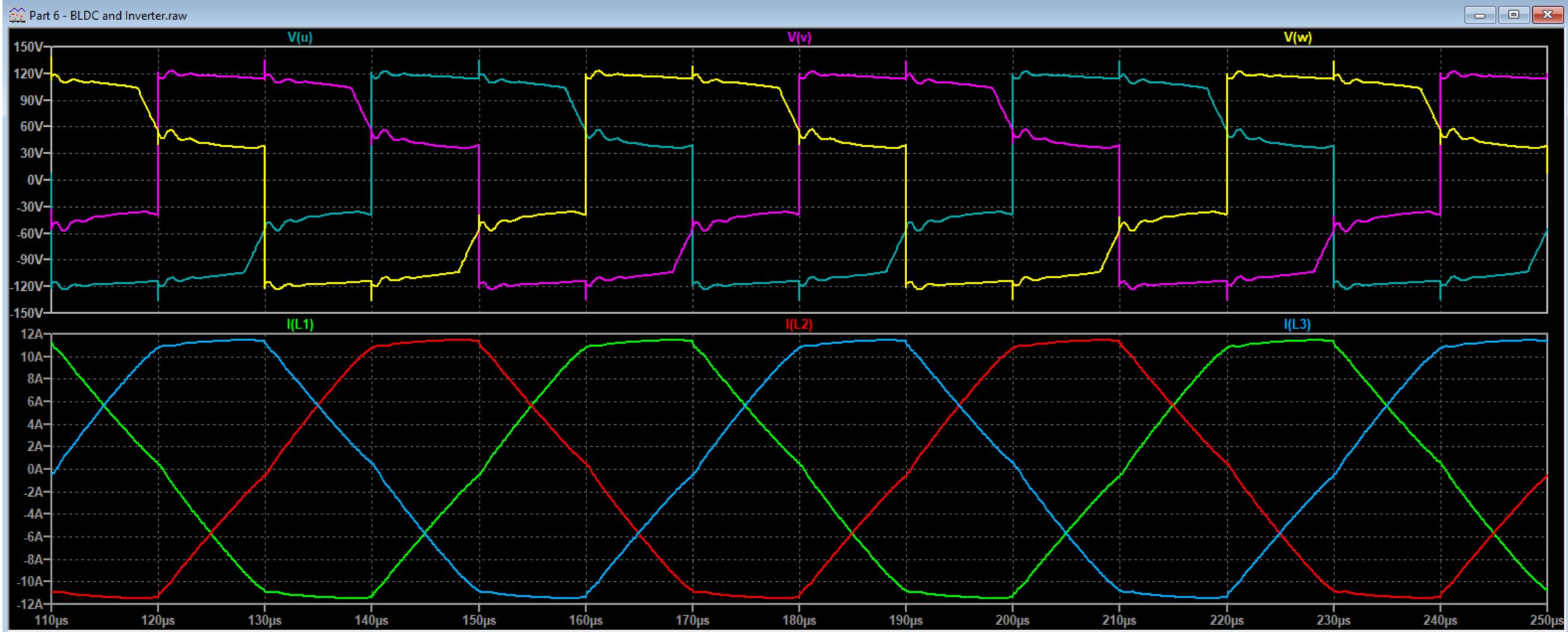
Credits Wikimedia commons {2\*Tdiv} {6\*Tdiv}

- Parasitic coupling to and through stator
- Influence of grounding (of stator)



# Real life examples

## Mains voltage BLDC driver + motor



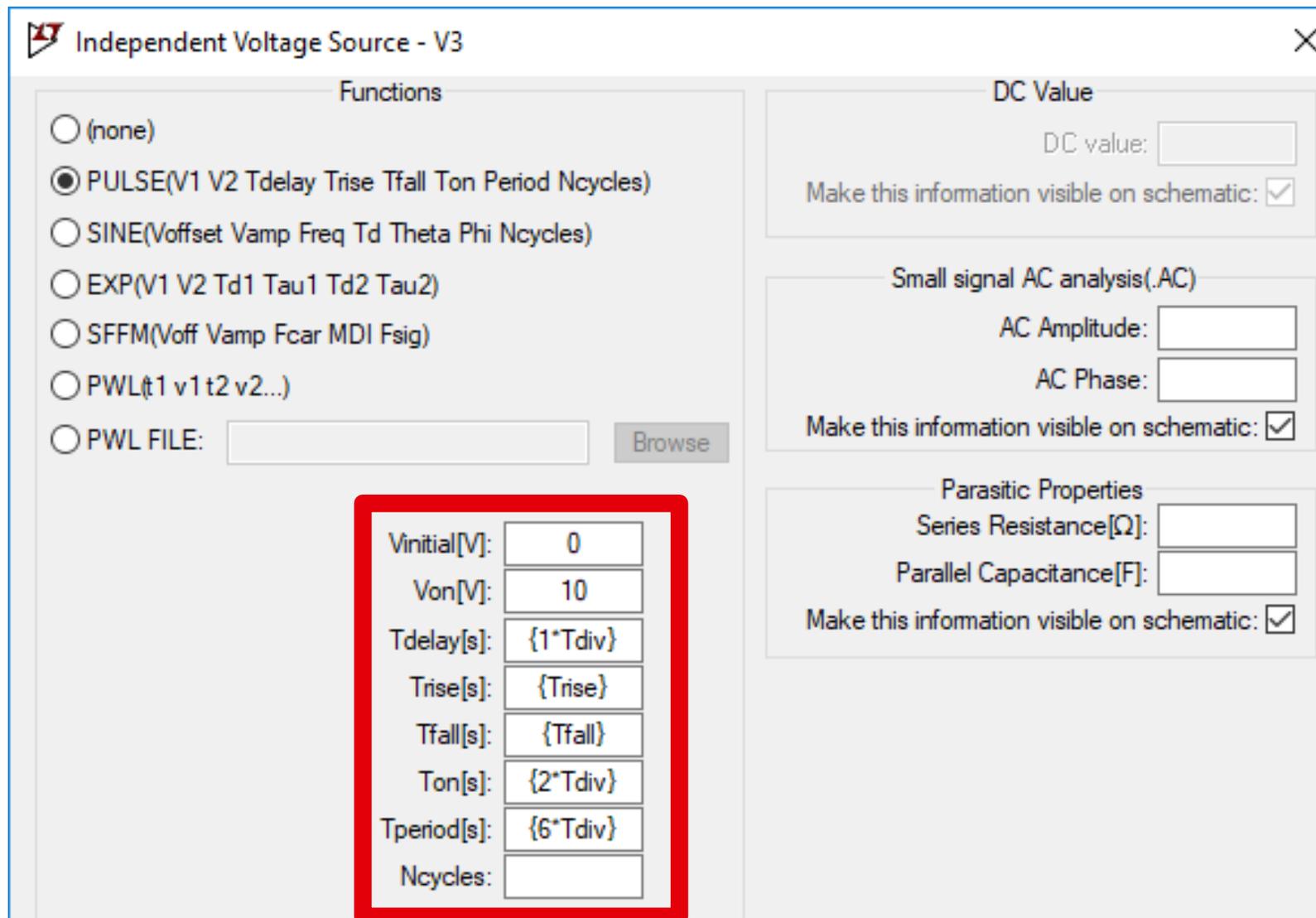
# Real life examples

## Mains voltage BLDC driver + motor

- Parametric simulation

`.param Trise=100ps Tfall=100ps Tdiv=10µs`

- .STEP is possible to see impact of slew rate and dead time on EMC signature



Independent Voltage Source - V3

Functions

(none)

PULSE(V1 V2 Tdelay Trise Tfall Ton Period Ncycles)

SINE(Voffset Vamp Freq Td Theta Phi Ncycles)

EXP(V1 V2 Td1 Tau1 Td2 Tau2)

SFFM(Voff Vamp Fcar MDI Fsig)

PWL(t1 v1 t2 v2...)

PWL FILE:  Browse

DC Value

DC value:

Make this information visible on schematic:

Small signal AC analysis(.AC)

AC Amplitude:

AC Phase:

Make this information visible on schematic:

Parasitic Properties

Series Resistance[Ω]:

Parallel Capacitance[F]:

Make this information visible on schematic:

Vinitial[V]:

Von[V]:

Tdelay[s]:

Trise[s]:

Tfall[s]:

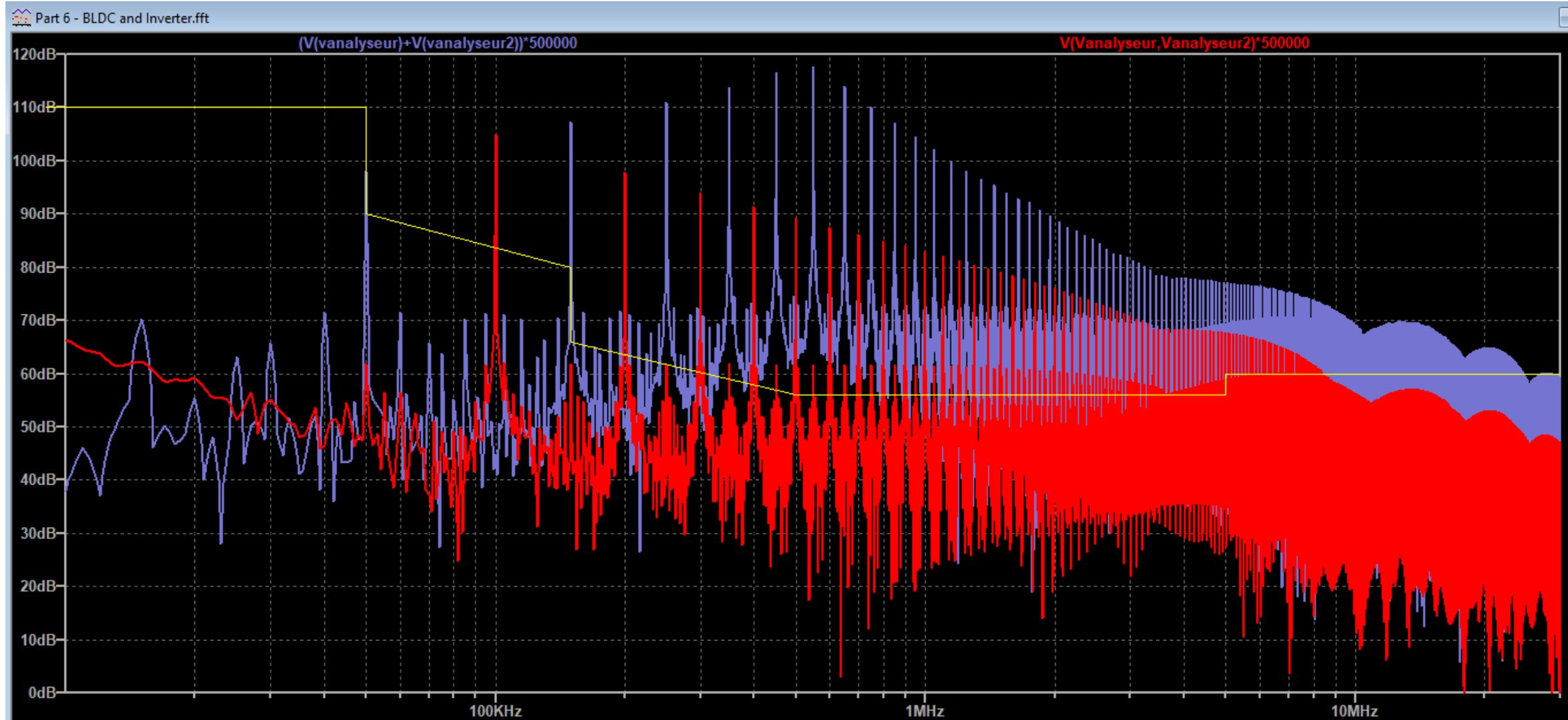
Ton[s]:

Tperiod[s]:

Ncycles:

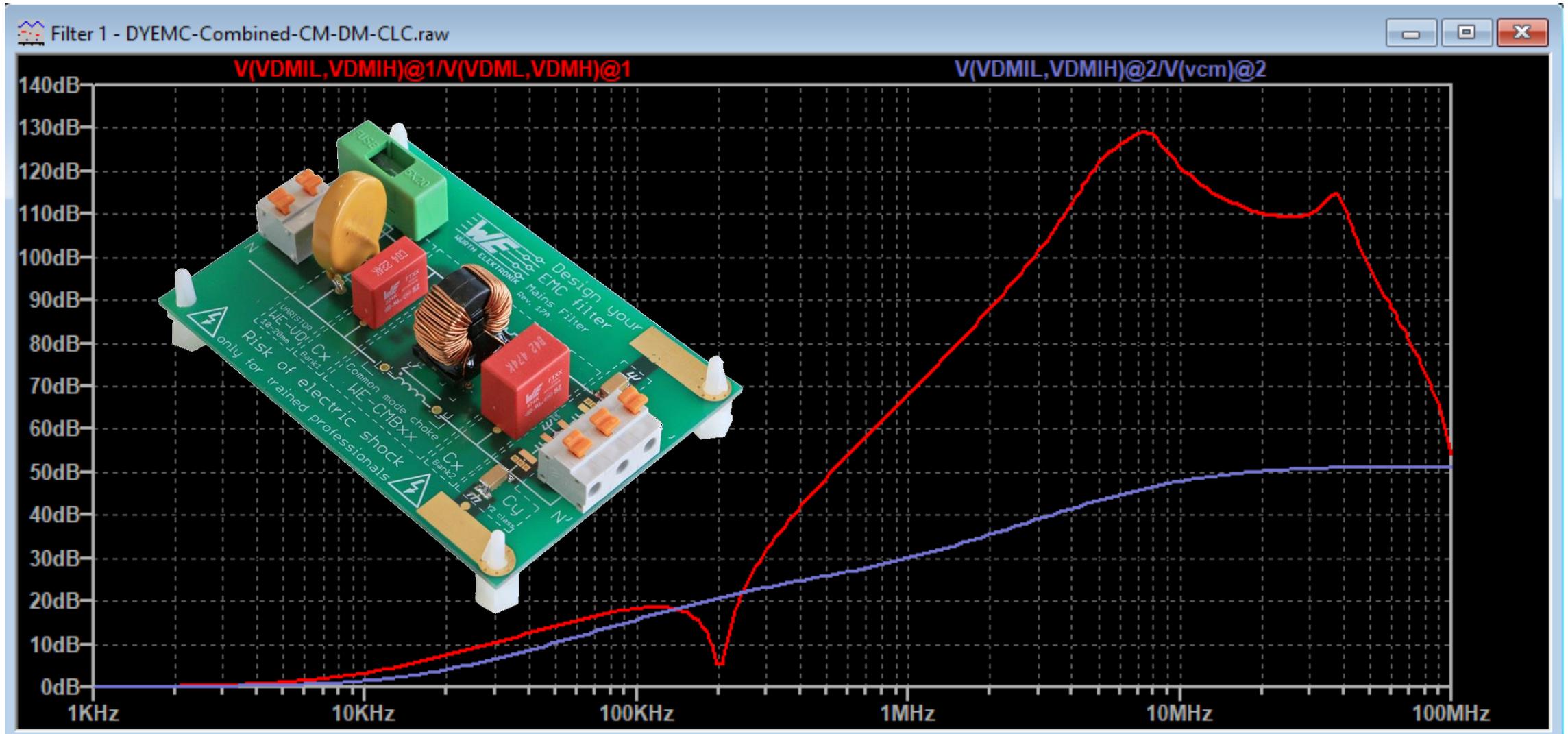
# Real life examples

## Mains voltage BLDC driver + motor



# Evaluation of Filter Insertion losses

## Design your EMC filter in LTspice



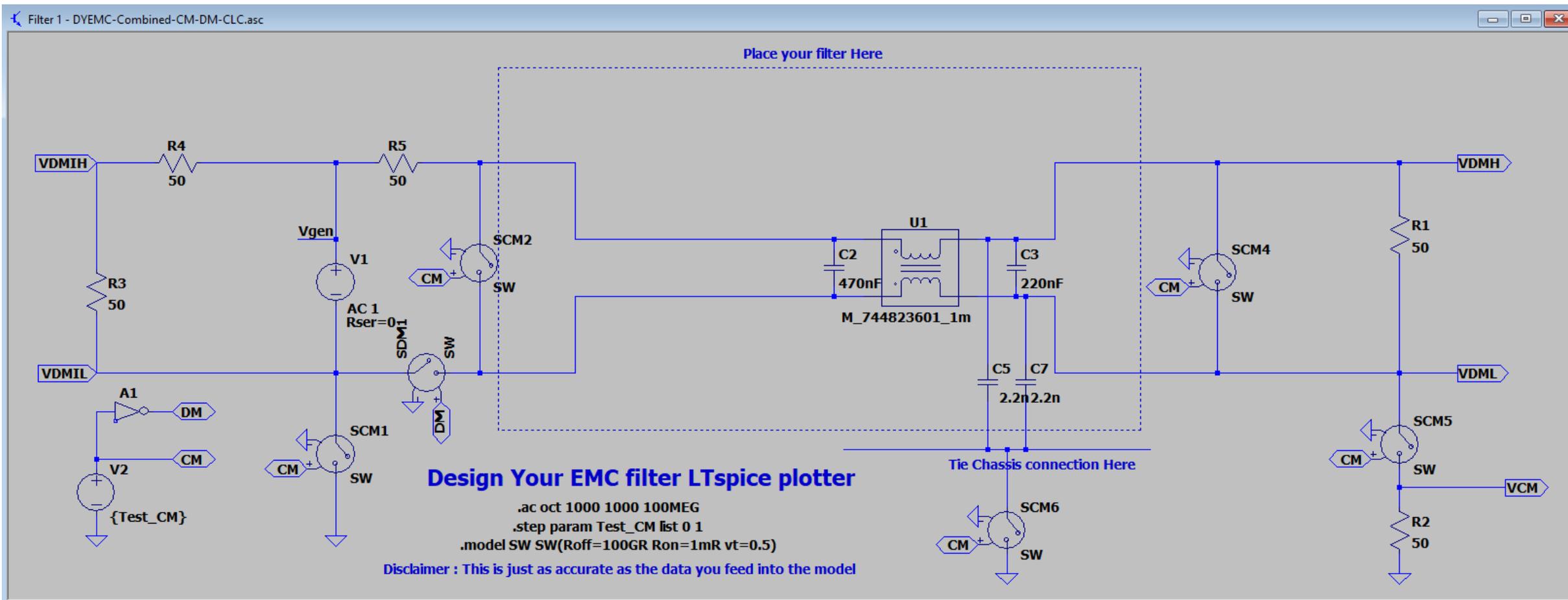
# Evaluation of Filter Insertion losses

## Design your EMC filter in LTspice



V(VDMIL,VDMIH)@1/V(VDML,VDMH)@1

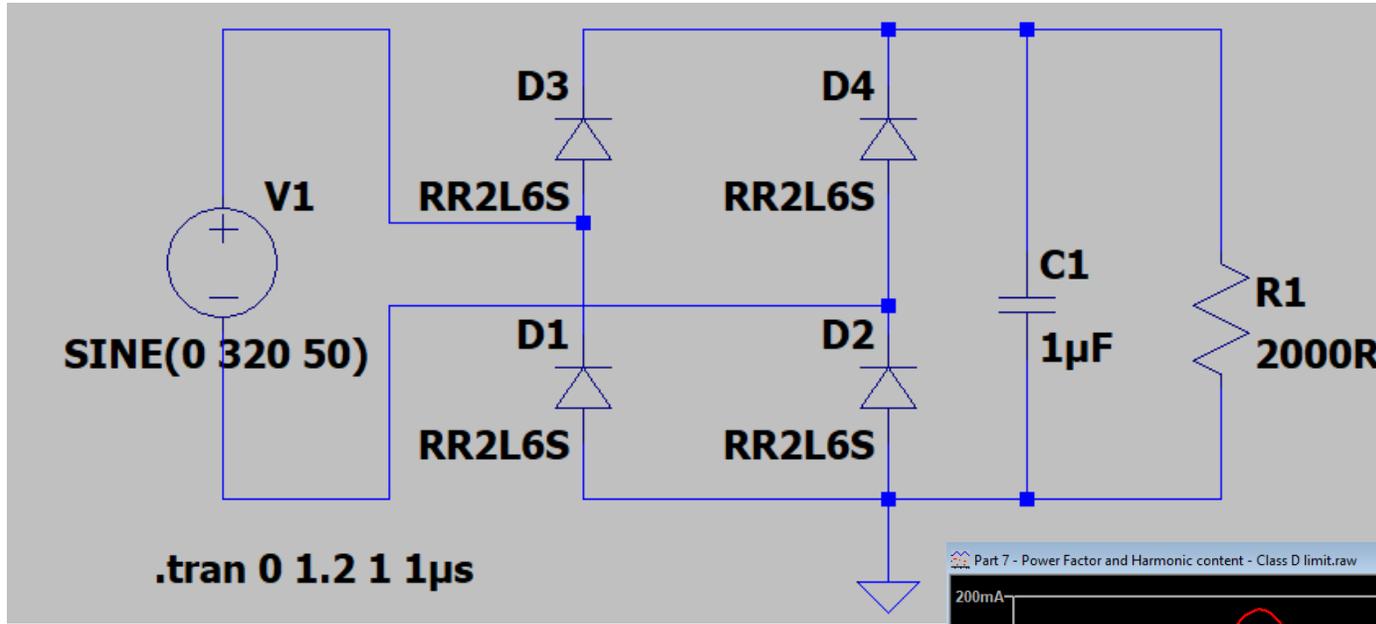
V(VDMIL,VDMIH)@2/V(vcm)@2



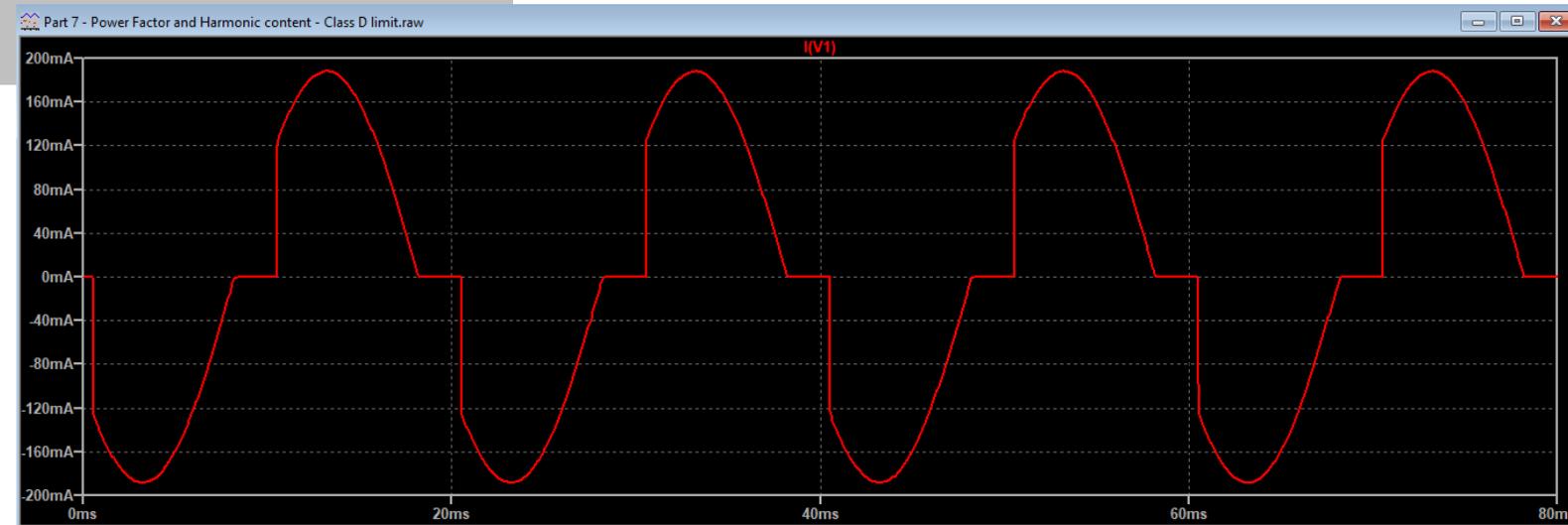


# Power Factor and Harmonic current

Anticipate IEC 61000-3-2

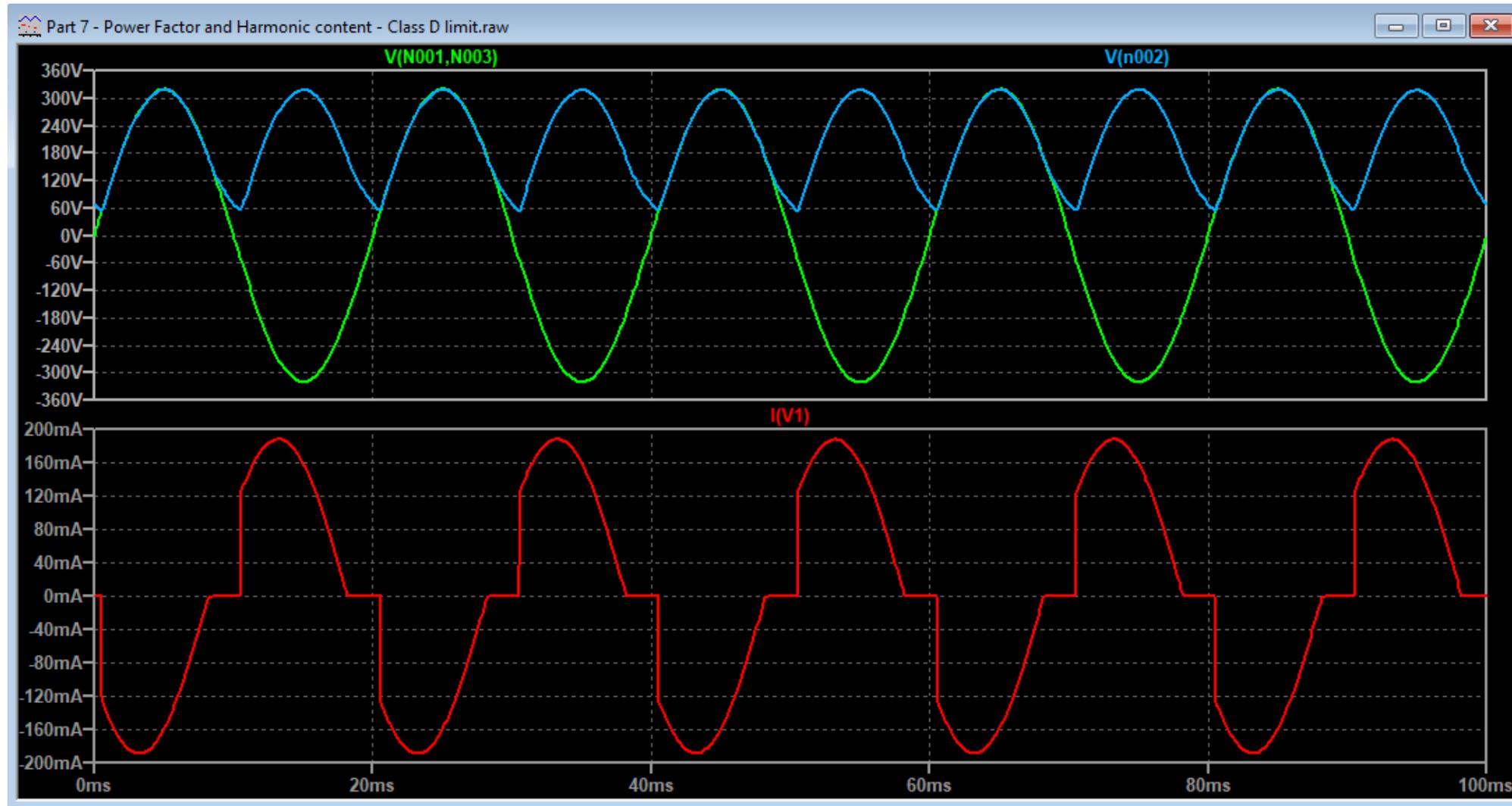


Harmonic order (n)	Maximum permissible harmonic current per watt (mA/W)
3	3.4
5	1.9
7	1.0
9	0.5
11	0.35
13	0.3
$15 \leq n \leq 39$ (odd harmonics only)	$3.85/n$



# Power Factor and Harmonic current

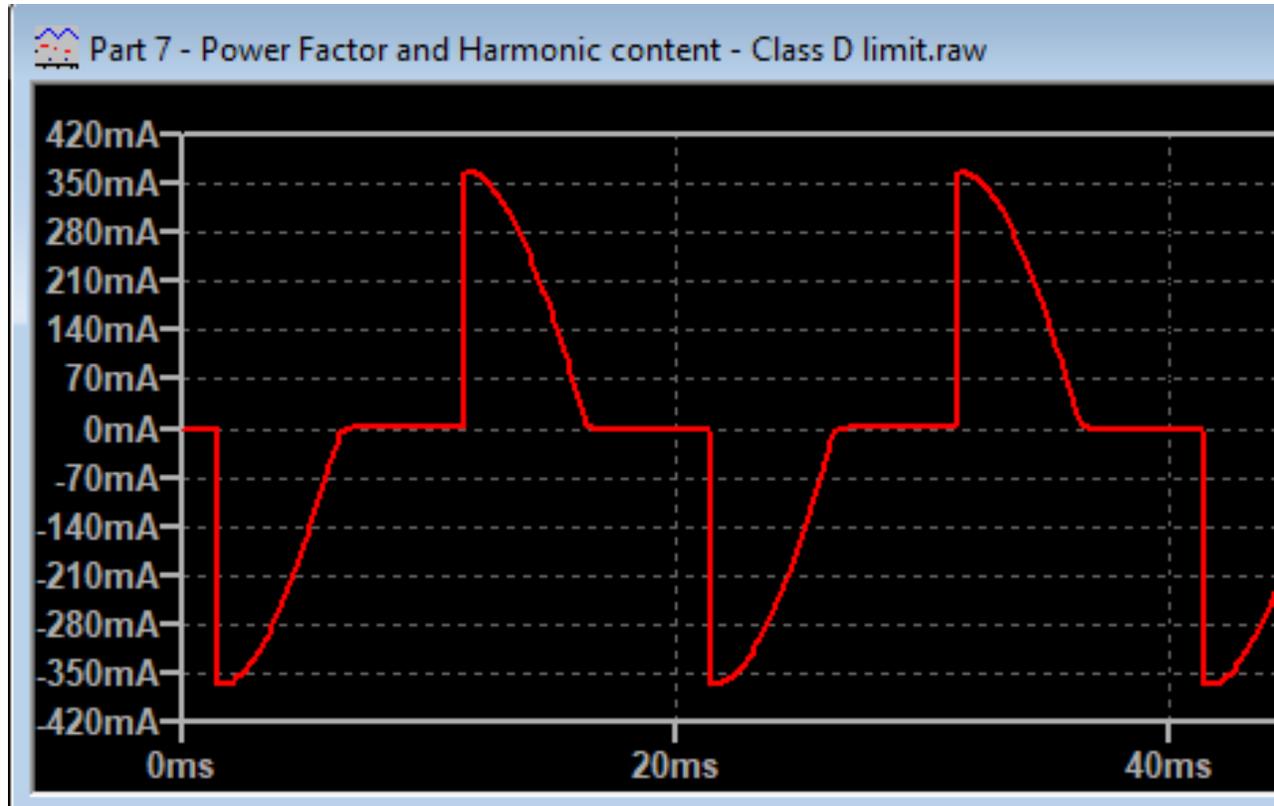
Anticipate IEC 61000-3-2



# Power Factor and Harmonic current

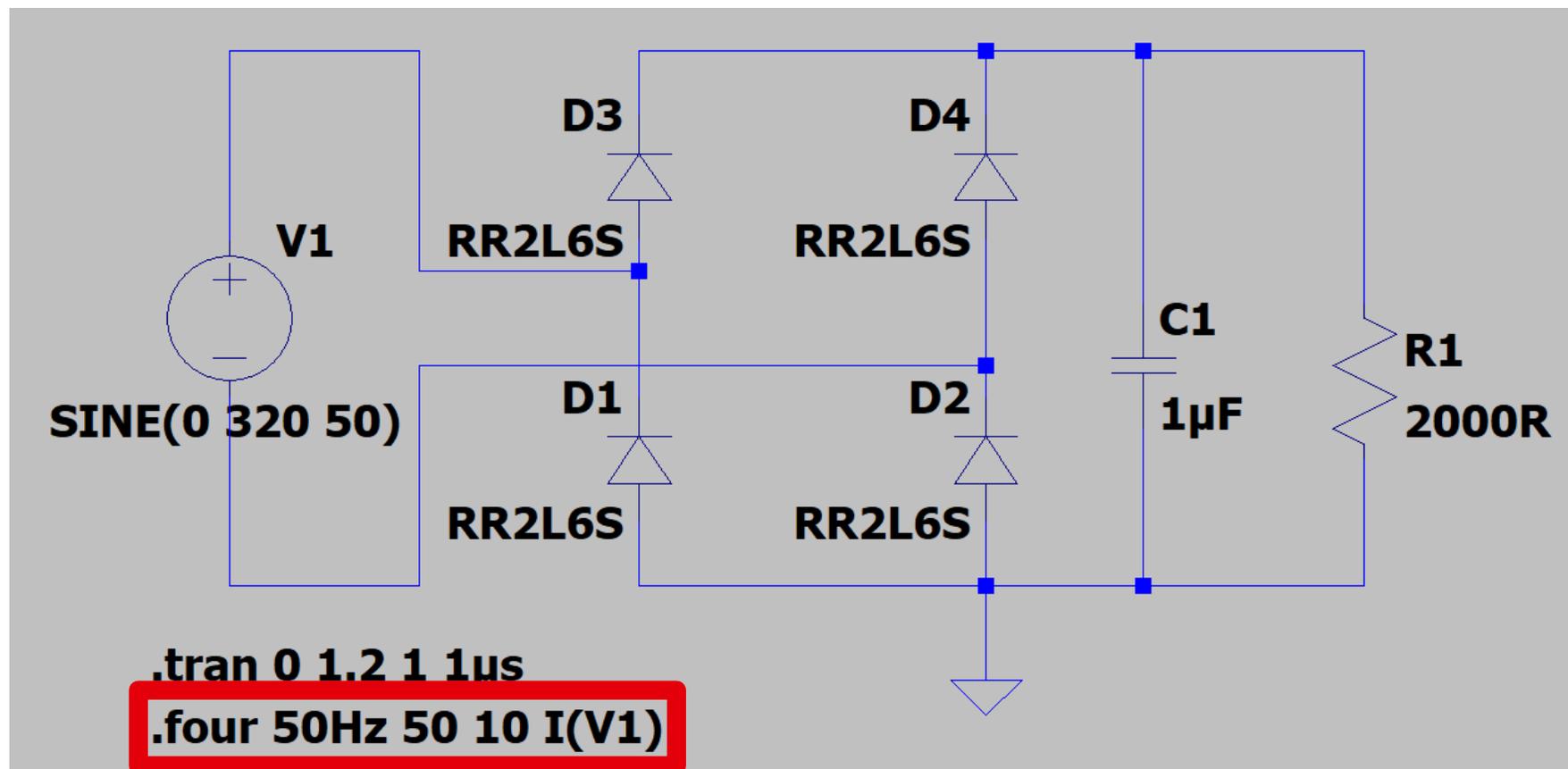
## Anticipate IEC 61000-3-2

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.FOUR directive to Anticipate IEC 61000-3-2





# Power Factor and Harmonic current

.FOUR directive to Anticipate IEC 61000-3-2

LTspice XVII - Part 7 - Power Factor and Harmonic conten

File Edit Hierarchy View Simulate Tools Window

Zoom Area Ctrl+Z  
Zoom Back Ctrl+B  
Zoom to Fit  
Pan

Show Grid Ctrl+G  
Mark Unconn. Pins 'U'  
Mark Anchors 'A'

Bill of Materials  
Efficiency Report

SPICE Netlist  
SPICE Error Log

Visible Traces  
Autorange Y-axis  
Marching Waves  
Set Probe Reference

SPICE Error Log: C:\Users\sylvain.lebras\Docur

Fourier components of I(v1)  
DC component: 5.23172e-007

Harmonic Number	Frequency [Hz]
1	5.000e+01
2	1.000e+02
3	1.500e+02
4	2.000e+02
5	2.500e+02
6	3.000e+02
7	3.500e+02
8	4.000e+02
9	4.500e+02
10	5.000e+02
11	5.500e+02
12	6.000e+02
13	6.500e+02
14	7.000e+02
15	7.500e+02
16	8.000e+02
17	8.500e+02
18	9.000e+02
19	9.500e+02
20	1.000e+03
21	1.050e+03

Ampera Fraction of fundamental

Fourier Component	Normalized Component
1.760e-01	1.000e+00
3.265e-07	1.855e-06
2.687e-02	1.526e-01
1.123e-06	6.379e-06
2.074e-02	1.178e-01
2.040e-07	1.159e-06
1.391e-02	7.904e-02
9.960e-07	5.658e-06
8.532e-03	4.847e-02
9.480e-07	5.386e-06
6.452e-03	3.665e-02
7.110e-07	4.039e-06
6.362e-03	3.614e-02
1.526e-06	8.671e-06
5.865e-03	3.332e-02
4.225e-07	2.401e-06
4.761e-03	2.705e-02
1.168e-06	6.634e-06
3.923e-03	2.229e-02
8.830e-07	5.016e-06
3.752e-03	2.131e-02

nonic content - Class D limit.log

Phase [degree]	Normalized Phase [deg]
-156.56°	0.00°
57.75°	214.31°
102.46°	259.01°
2.94°	159.50°
108.42°	264.98°
-164.89°	-8.33°
108.04°	264.59°
-63.52°	93.04°
93.80°	250.36°
125.74°	282.30°
64.05°	220.61°
-101.44°	55.12°
41.96°	198.52°
51.93°	208.48°
29.38°	185.94°
-89.14°	67.42°
14.64°	171.20°
-50.15°	106.41°
-8.40°	148.16°
-105.51°	51.05°
-31.96°	124.60°

45	2.250e+03	1.732e-03	9.838e-03	98.91°	255.46°
46	2.300e+03	7.944e-07	4.513e-06	-44.86°	111.70°
47	2.350e+03	1.685e-03	9.573e-03	77.95°	234.51°
48	2.400e+03	1.657e-07	9.416e-07	-81.86°	74.69°
49	2.450e+03	1.657e-03	9.412e-03	59.24°	215.79°
50	2.500e+03	7.697e-07	4.373e-06	-107.70°	48.86°

Total Harmonic Distortion: 23.211629% (23.614123%) PF=0.893698 (0.8929)

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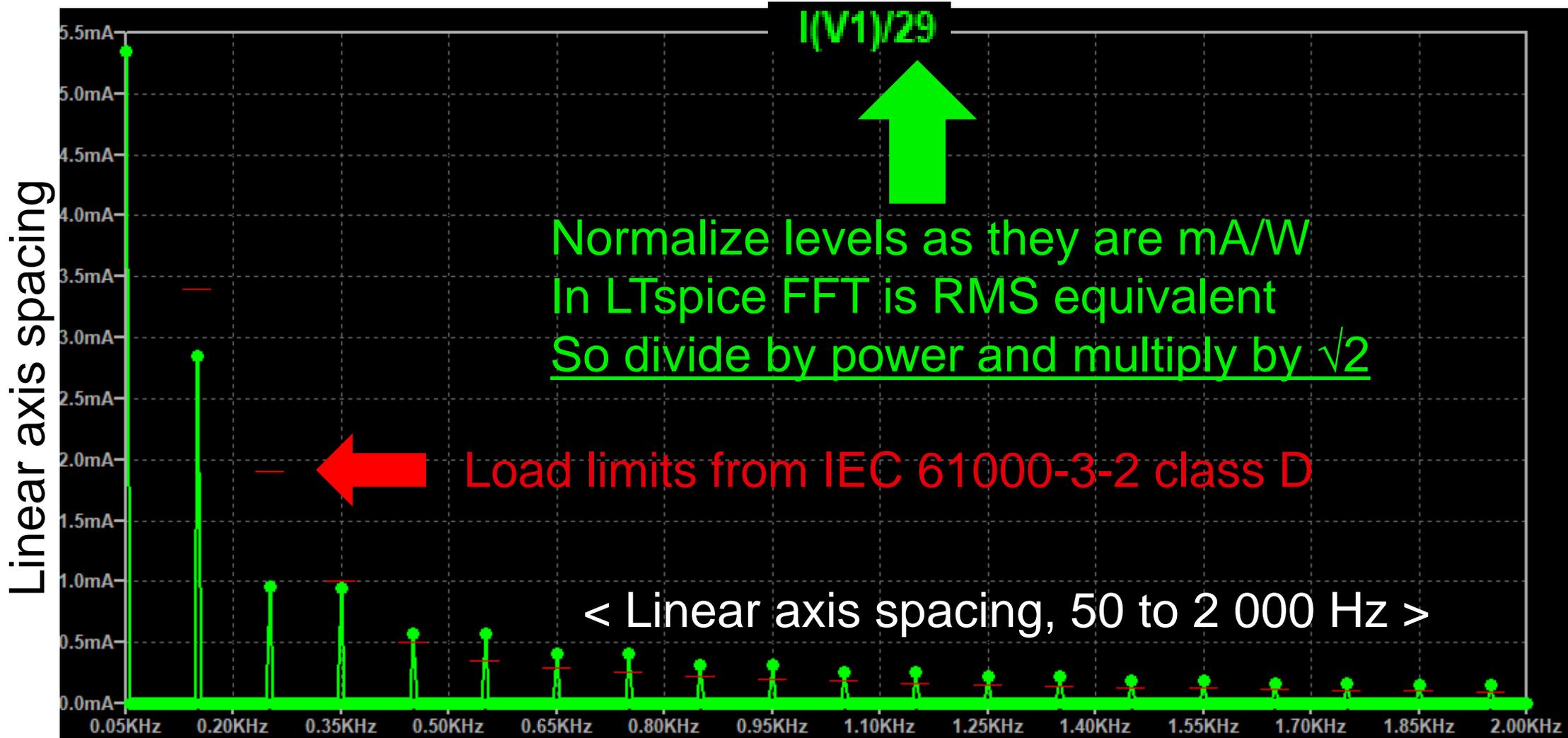
## Graphical method to anticipate IEC 61000-3-2



IEC 61000-3-2 Class D - LTSpice limit line calculator						
in 50Hz base		Start Freq	End Freq	mA/W start	Line def for LTSPICE plot settings file	
Line	3	130	170	3.4	Line: "A" 4 0	(130,0.0034) (170,0.0034)
Line	5	230	270	1.9	Line: "A" 4 0	(230,0.0019) (270,0.0019)
Line	7	330	370	1	Line: "A" 4 0	(330,0.001) (370,0.001)
Line	9	430	470	0.5	Line: "A" 4 0	(430,0.0005) (470,0.0005)
Line	11	530	570	0.35	Line: "A" 4 0	(530,0.00035) (570,0.00035)
Line	13	630	670	0.296153846	Line: "A" 4 0	(630,0.000296153846153846) (670,0.000296153846153846)
Line	15	730	770	0.256666667	Line: "A" 4 0	(730,0.000256666666666667) (770,0.000256666666666667)
Line	17	830	870	0.226470588	Line: "A" 4 0	(830,0.000226470588235294) (870,0.000226470588235294)
Line	19	930	970	0.202631579	Line: "A" 4 0	(930,0.000202631578947368) (970,0.000202631578947368)
Line	21	1030	1070	0.183333333	Line: "A" 4 0	(1030,0.000183333333333333) (1070,0.000183333333333333)
Line	23	1130	1170	0.167391304	Line: "A" 4 0	(1130,0.000167391304347826) (1170,0.000167391304347826)
Line	25	1230	1270	0.154	Line: "A" 4 0	(1230,0.000154) (1270,0.000154)
Line	27	1330	1370	0.142592593	Line: "A" 4 0	(1330,0.000142592592592593) (1370,0.000142592592592593)
Line	29	1430	1470	0.132758621	Line: "A" 4 0	(1430,0.000132758620689655) (1470,0.000132758620689655)
Line	31	1530	1570	0.124193548	Line: "A" 4 0	(1530,0.000124193548387097) (1570,0.000124193548387097)
Line	33	1630	1670	0.116666667	Line: "A" 4 0	(1630,0.000116666666666667) (1670,0.000116666666666667)
Line	35	1730	1770	0.11	Line: "A" 4 0	(1730,0.00011) (1770,0.00011)
Line	37	1830	1870	0.104054054	Line: "A" 4 0	(1830,0.000104054054054054) (1870,0.000104054054054054)
Line	39	1930	1970	0.098717949	Line: "A" 4 0	(1930,9.87179487179487E-05) (1970,9.87179487179487E-05)

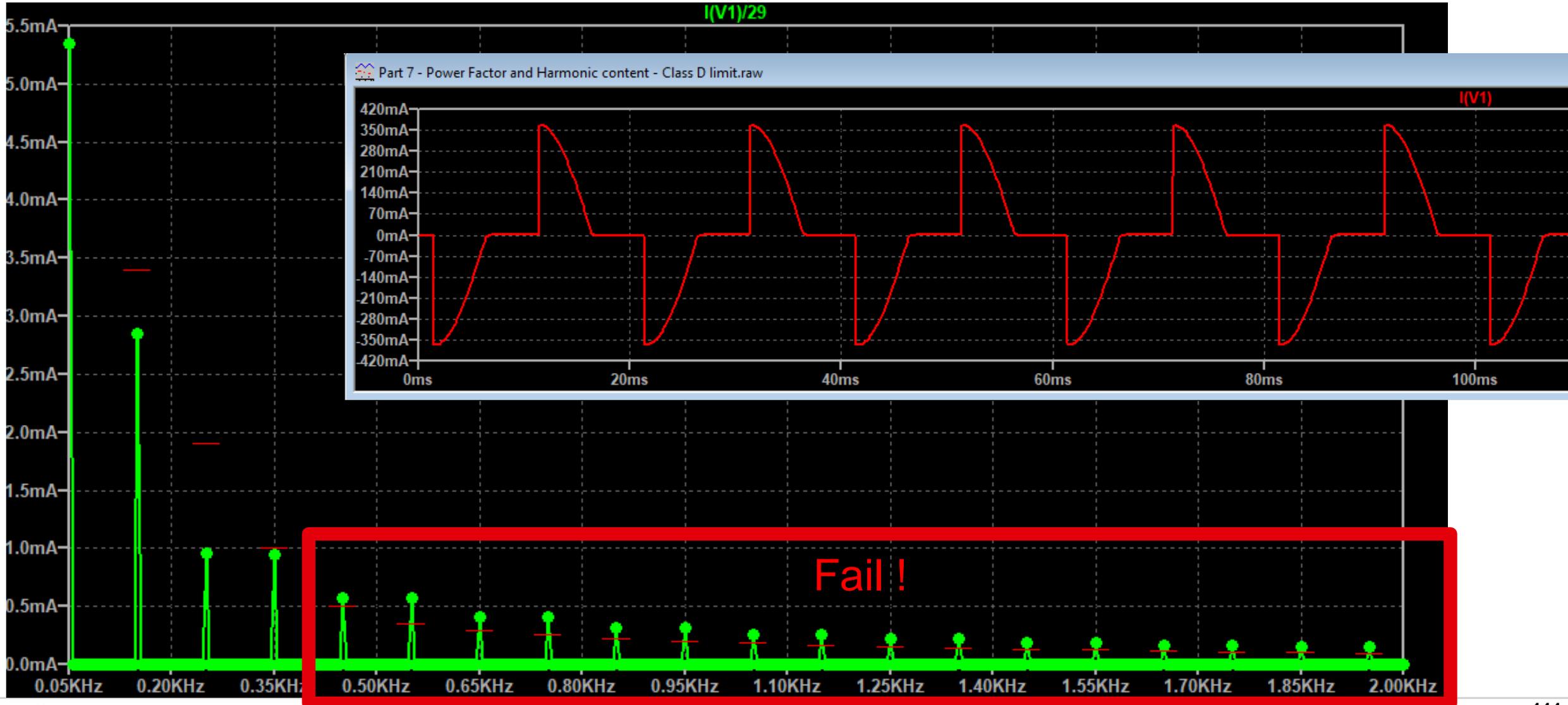
# Power Factor and Harmonic current

## Graphical method to anticipate IEC 61000-3-2



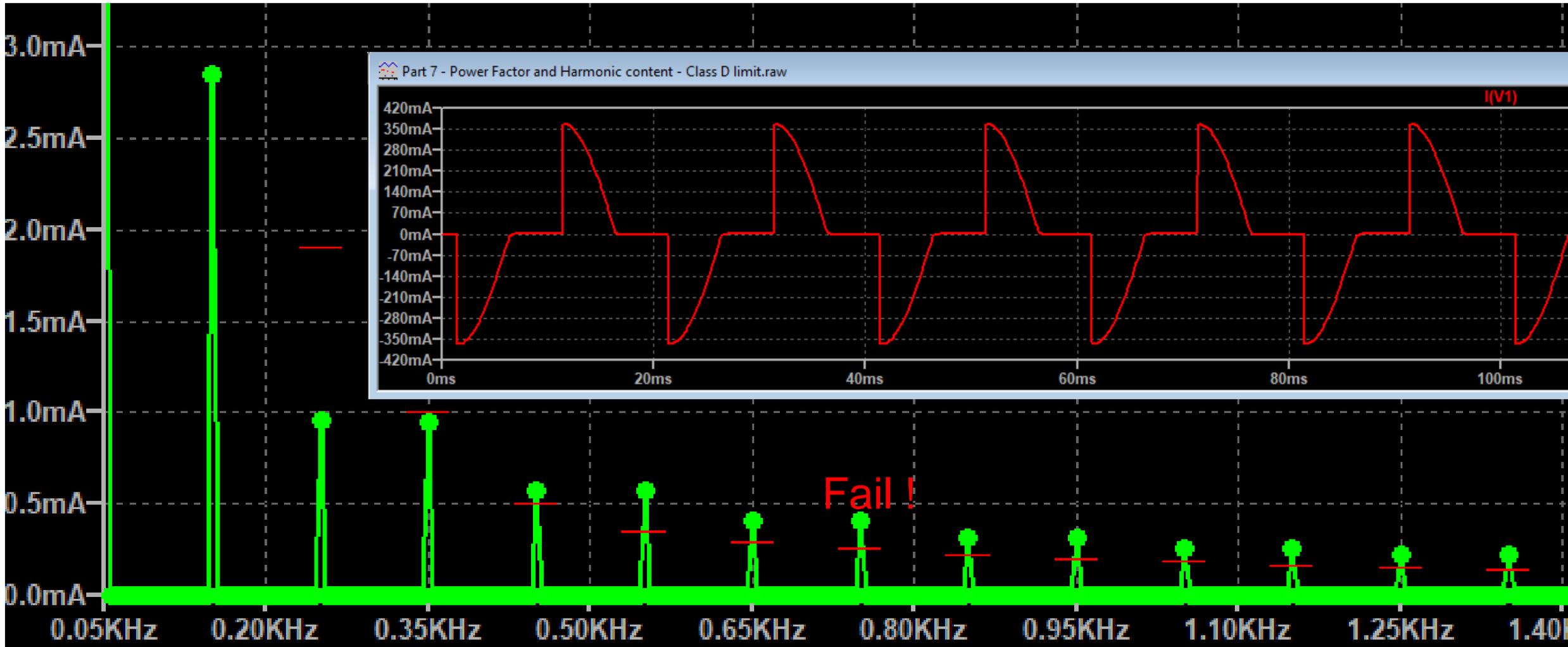
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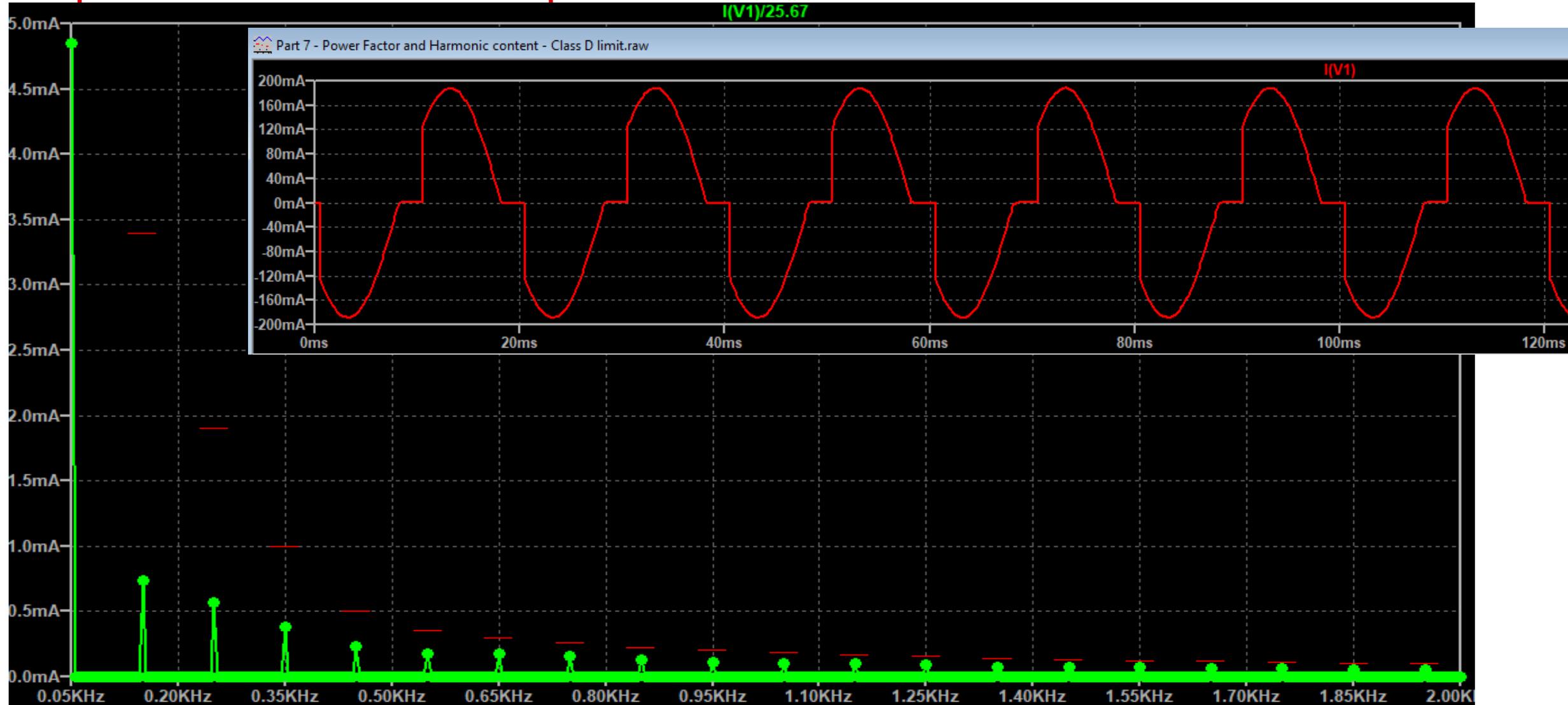
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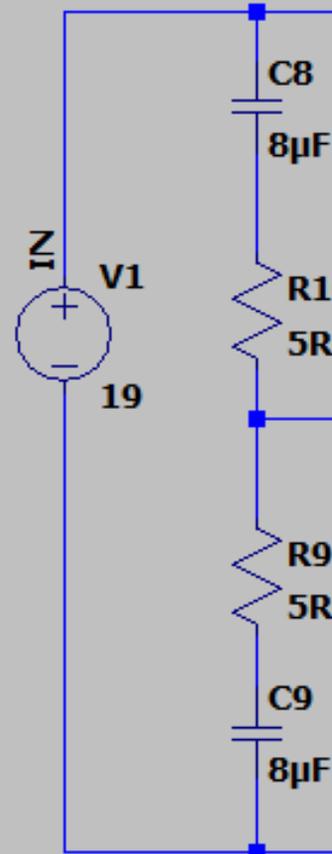
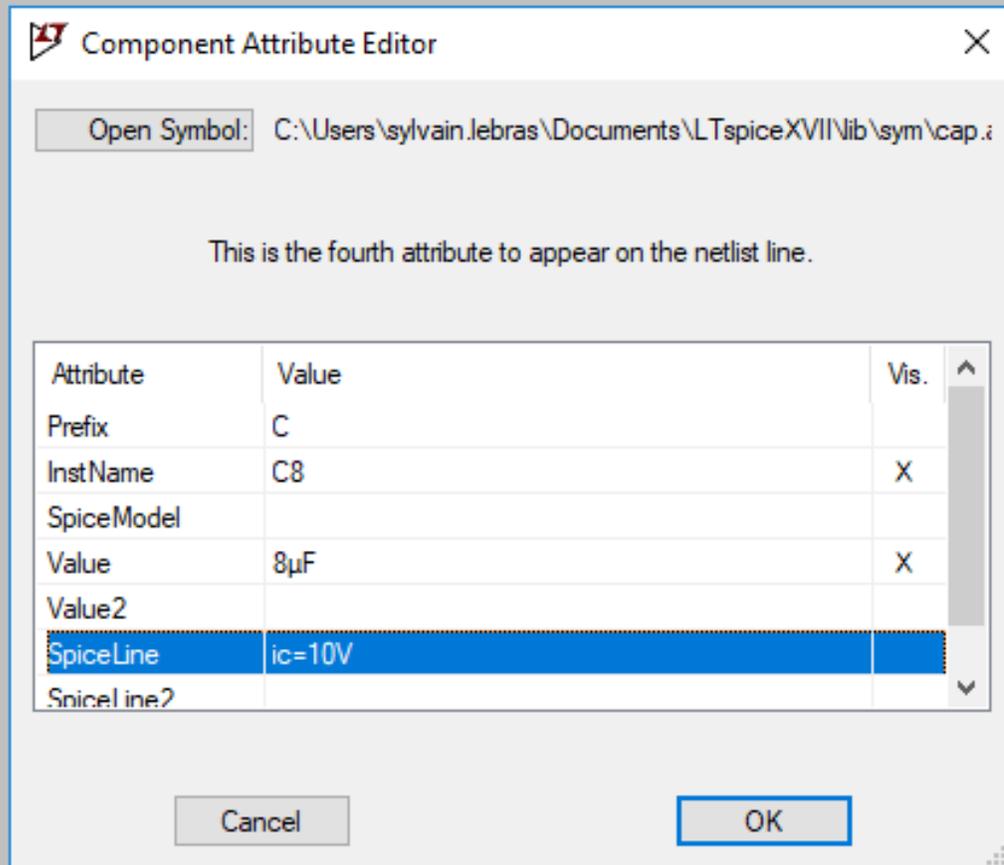
# Power Factor and Harmonic current

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# Good to know

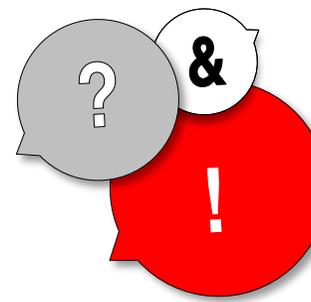
## Speed up simulations



## Setting initial condition

- Ctrl + Right Click
- SpiceLine
  - ic=10V

# Questions & Answers



Slides and Simulation files are available here :

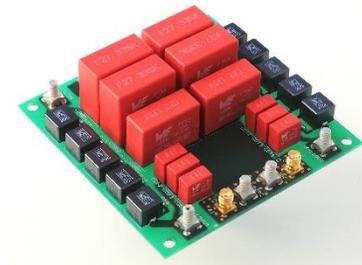
<https://github.com/sylvainlebras/anticipate-emc-with-ltspice>

Schematic, Layouts, Bill of material, are released as open source :

<https://github.com/sylvainlebras/EMC-Tools>

If you have questions:

[Sylvain.LeBras@we-online.com](mailto:Sylvain.LeBras@we-online.com)



**Vous recevrez un lien avec les fichiers utilisés pendant cette présentation**

-  Part 1 - Testfixture.asc
-  Part 1 - Testfixture.plt
-  Part 2 - Modified Testfixture - 1 output voltage.plt
-  Part 2 - Modified Testfixture - 2 Breakdown.plt
-  Part 2 - Modified Testfixture.asc
-  Part 2 - Modified Testfixture.plt
-  Part 3 - Ripple-Input-MD.asc
-  Part 3 - Ripple-Input-MD-1 Time based display.plt
-  Part 3 - Ripple-Input-MD-2 Frequency based display.plt
-  Part 3 - Ripple-Input-MD-4 Frequency based display Breakdown.plt
-  Part 4 - DM and CM of Buck - 1 FFT analysis.plt
-  Part 4 - DM and CM of Buck - 2 Time based CMDM split.plt
-  Part 4 - DM and CM of Buck - 3 FFT display of CMDM split.plt
-  Part 4 - DM and CM of Buck.asc
-  Part 4bis - DM and CM of Buck - Fixed.asc
-  Part 5 - Flyback converter - 1 FFT split analysis.plt
-  Part 5 - Flyback converter.asc
-  Part 6 - BLDC and Inverter.asc
-  Part 6 - BLDC and Inverter.log
-  Part 6 - BLDC and Inverter.op.raw
-  Part 7 - Power Factor and Harmonic content - Class D limit.asc
-  Part 7 - Power Factor and Harmonic content - Class D limit.log
-  Part 7 - Power factor and Harmonic content.plt
-  Part 8 - DYEMC-Combined-CM-DM-CLC.asc
-  Part 8 - DYEMC-Combined-CM-DM-CLC.plt