DIGITAL WE DAYS 2024

WE'VE GOT THE POWER, THE POE POWER

WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

AGENDA

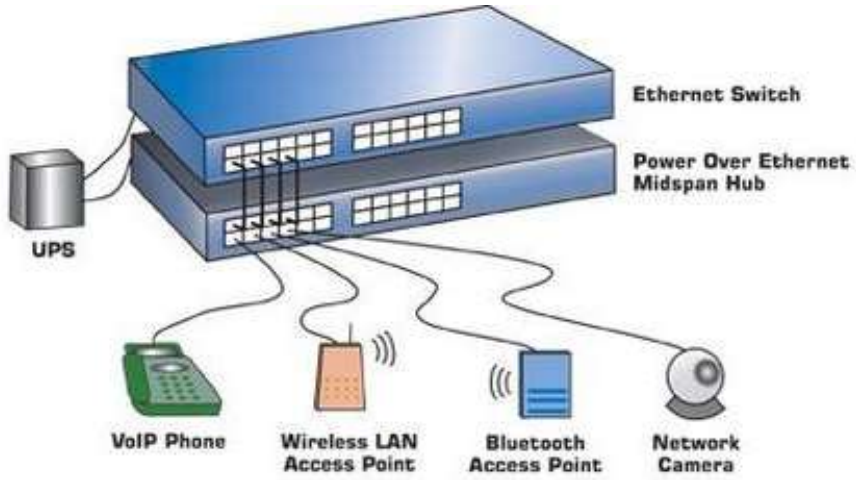
- Concept and Architecture
  - Concept
  - Architecture
    - Signal and Power Flow
- PoE Options and Solutions
- Practical Design Example – PoE PD

CONCEPT AND ARCHITECTURE

CONCEPT

Power over Ethernet

Technology for passing electrical power along data lines of wired Ethernet LANs (up to 100m cable)
Applicable Standard IEEE 802.3



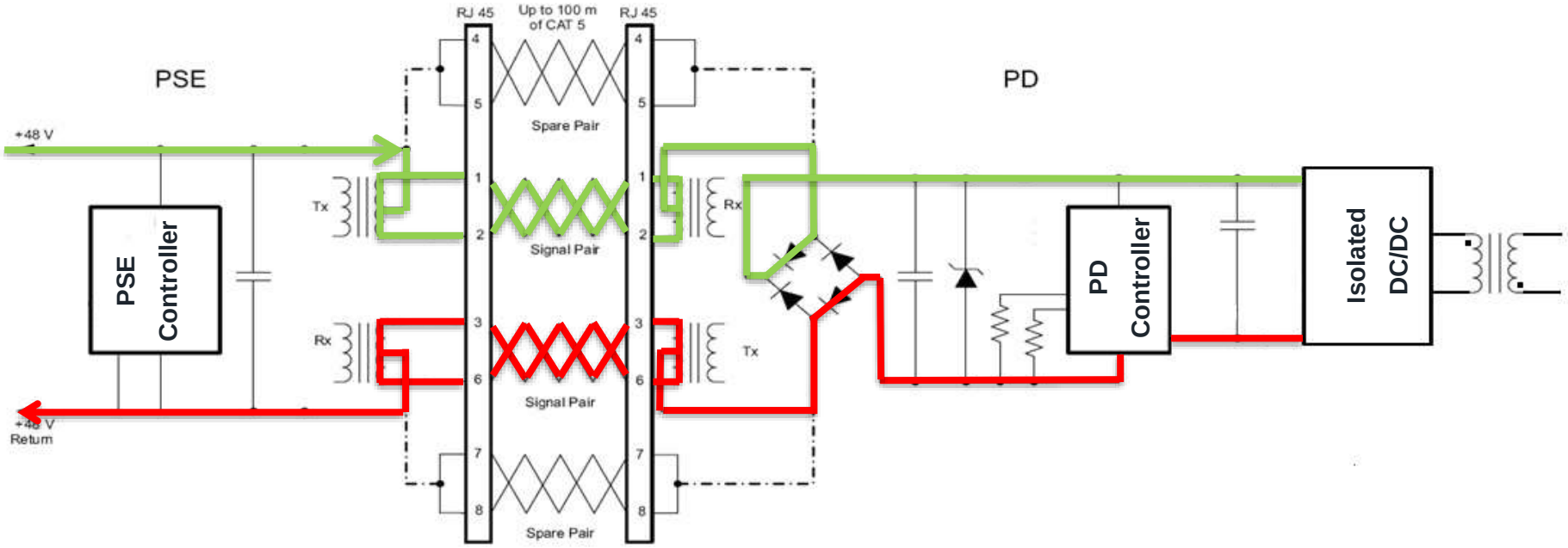
CONCEPT

Types

PoE Standard	IEEE 802.3af Type 1	IEEE 802.3at Type 2	IEEE 802.3bt Type 3	IEEE 802.3bt Type 4
Max Power Delivered by PSE	15.4W	30W	60W	100W
Power Available at PD	12.95W	25.5W	51W	71W
Max Current	350mA	600mA	600mA	960mA
Twisted-pair used	2-Pair	2-Pair	4-Pair	4-Pair

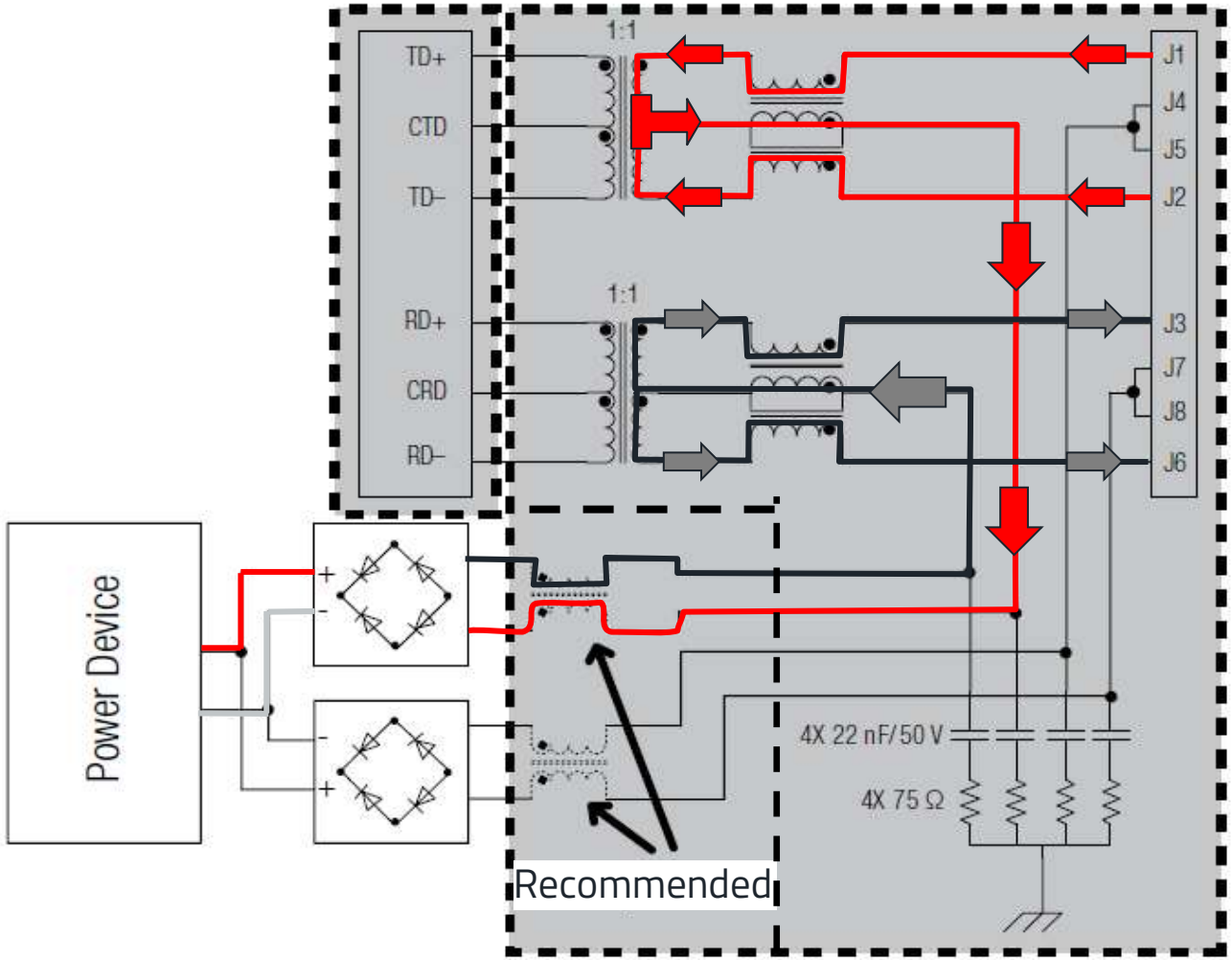
ARCHITECTURE

Power Flow PSE -> PD



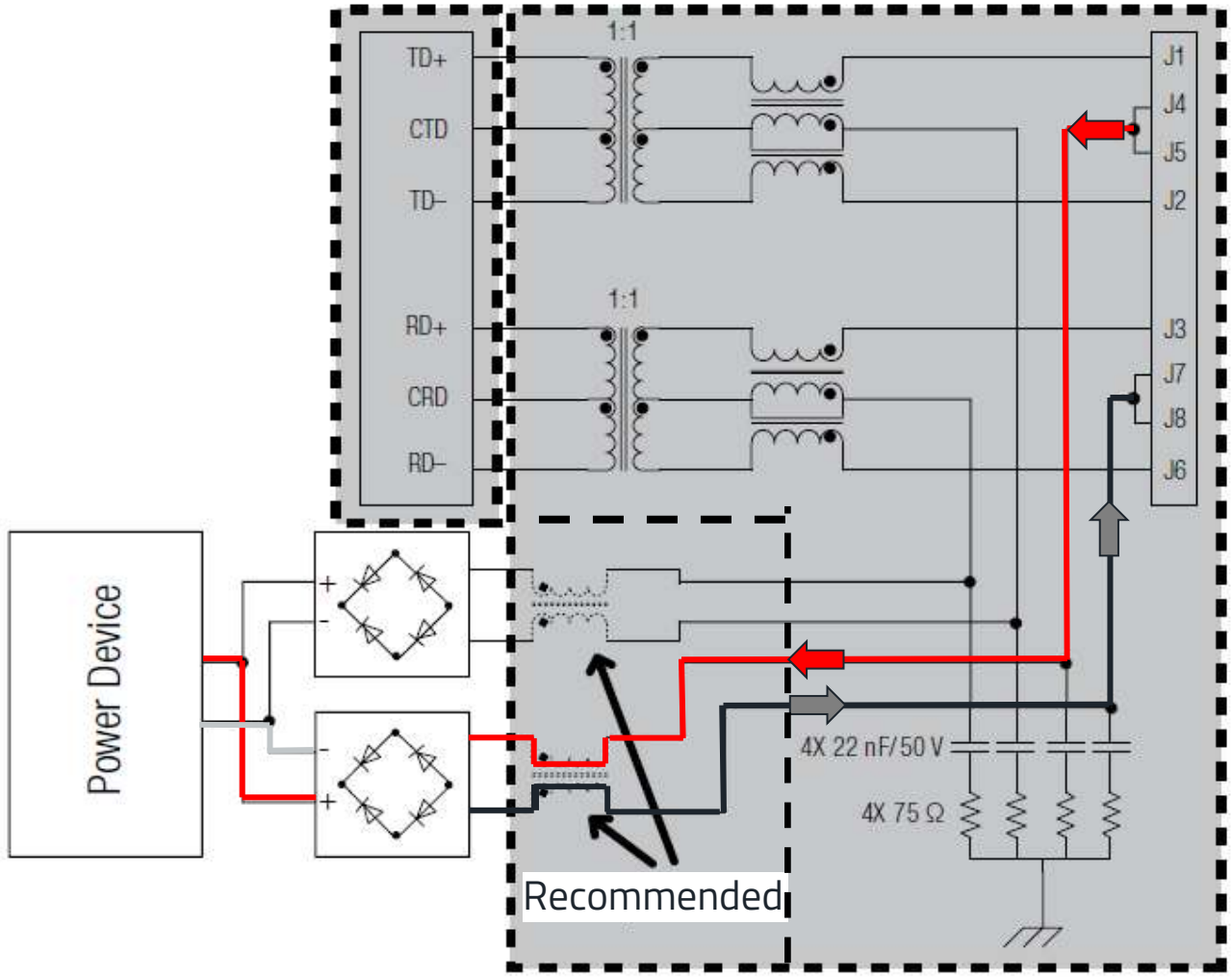
ARCHITECTURE

Power Path 1



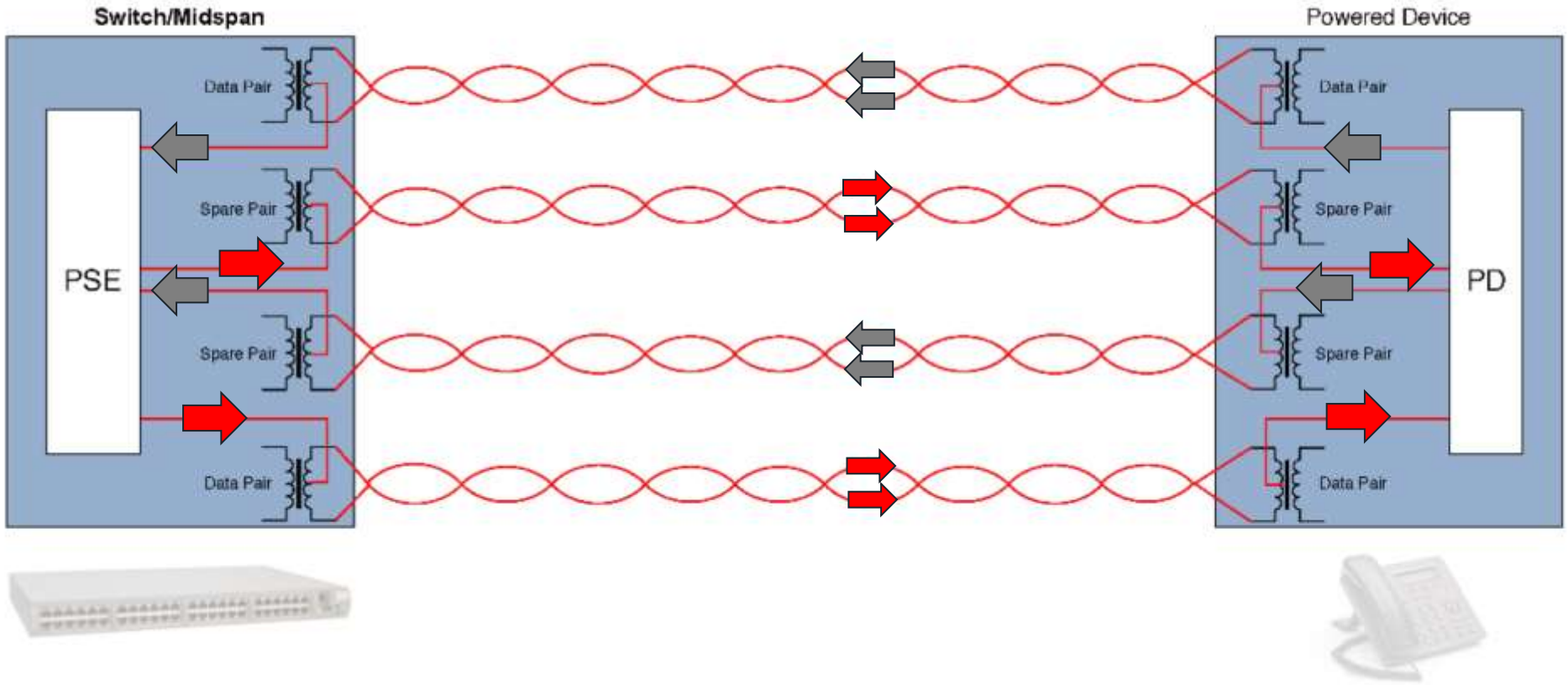
ARCHITECTURE

Power Path 2



ARCHITECTURE IEEE802.3.BT

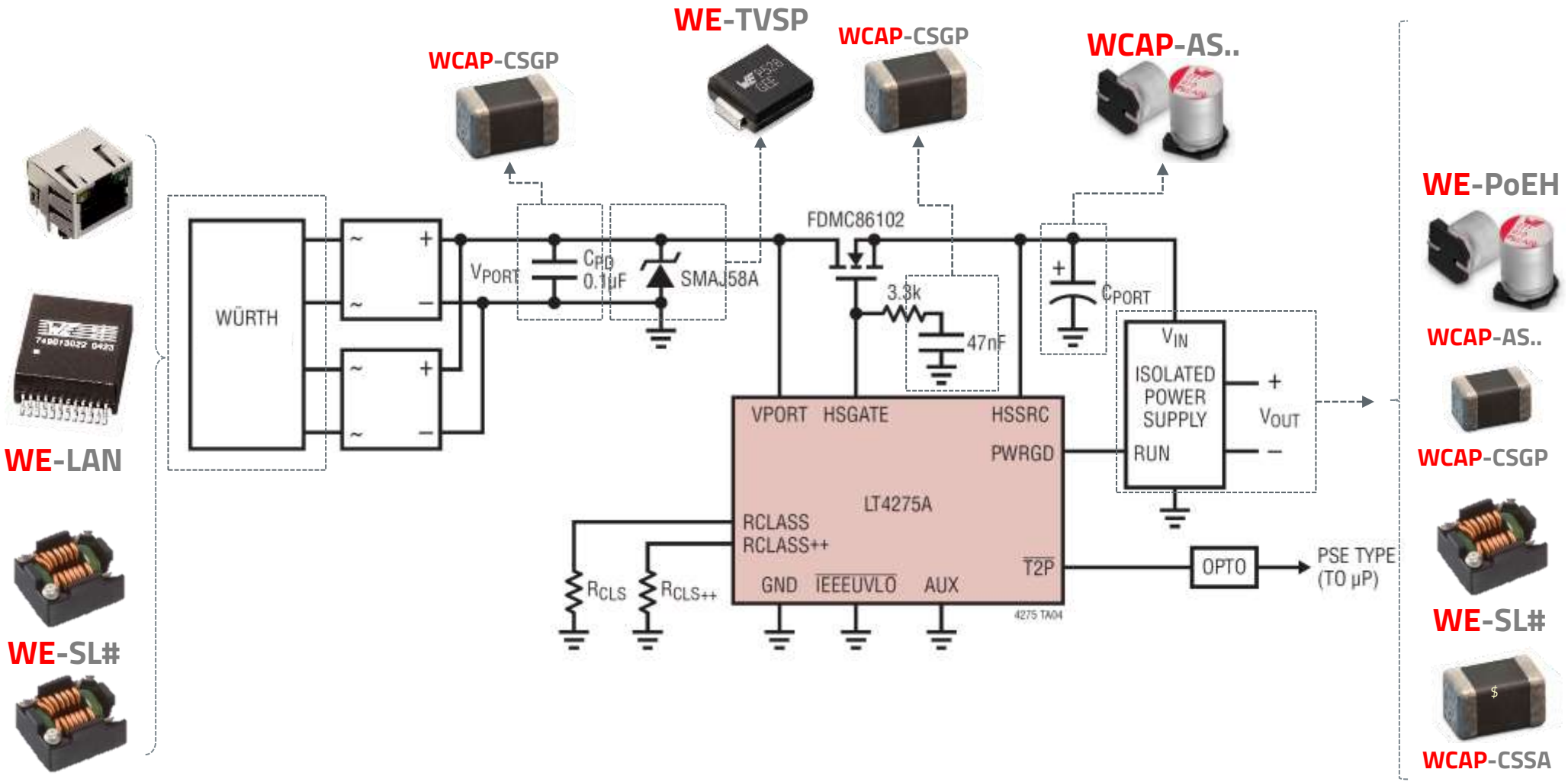
2 Power Paths



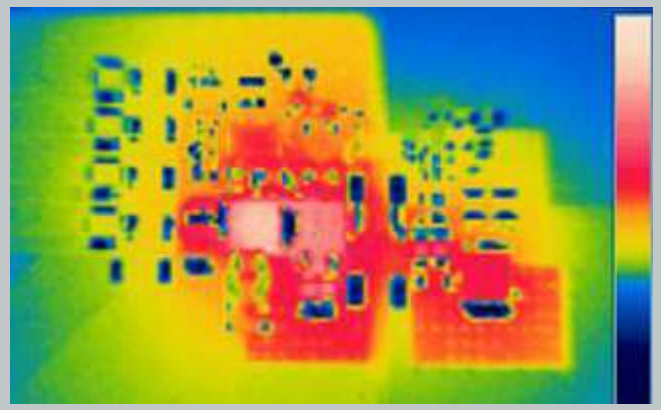
Source Microsemi

ARCHITECTURE

Powered Device



POE
OPTIONS & SOLUTIONS



TYPES AND CLASSIFICATION

Class Number	PSE Output Power [W]	PD Input Power [W]	PD Type	Notes
0	15.4	12.95	1	IEEE802.3af
1	4	3.84	1	
2	7	6.49	1	
3	15.4	12.95	1	
4	30	25.5	2	IEEE802.3at
5	45	40	3	IEEE802.3bt
6	60	51	3	
7	75	62	4	
8	90	73	4	

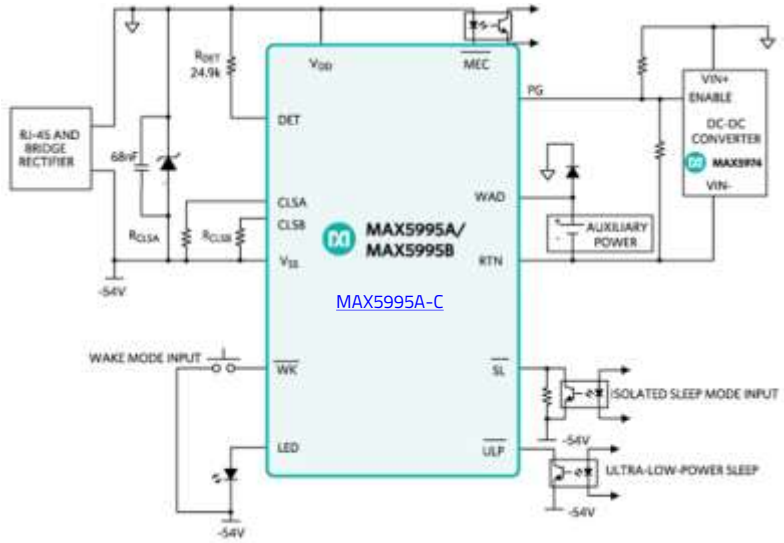
TYPES AND CLASSIFICATION

PD REQUESTED CLASS	PD REQUESTED POWER	PD TYPE	NOMINAL CLASS CURRENT	RESISTOR (1%)	
				R_{CLS}	R_{CLS}++
0	13W	Type 1	2.5mA	1.00kΩ	Open
1	3.84W	Type 1 or 3	10.5mA	150Ω	Open
2	6.49W	Type 1 or 3	18.5mA	80.6Ω	Open
3	13W	Type 1 or 3	28mA	52.3Ω	Open
4	25.5W	Type 2 or 3	40mA	35.7Ω	Open
5	40W	Type 3	40mA/2.5mA	1.00kΩ	37.4Ω
6	51W	Type 3	40mA/10.5mA	150Ω	47.5Ω
7	62W	Type 4	40mA/18.5mA	80.6Ω	64.9Ω
8	71.3W	Type 4	40mA/28mA	52.3Ω	118Ω

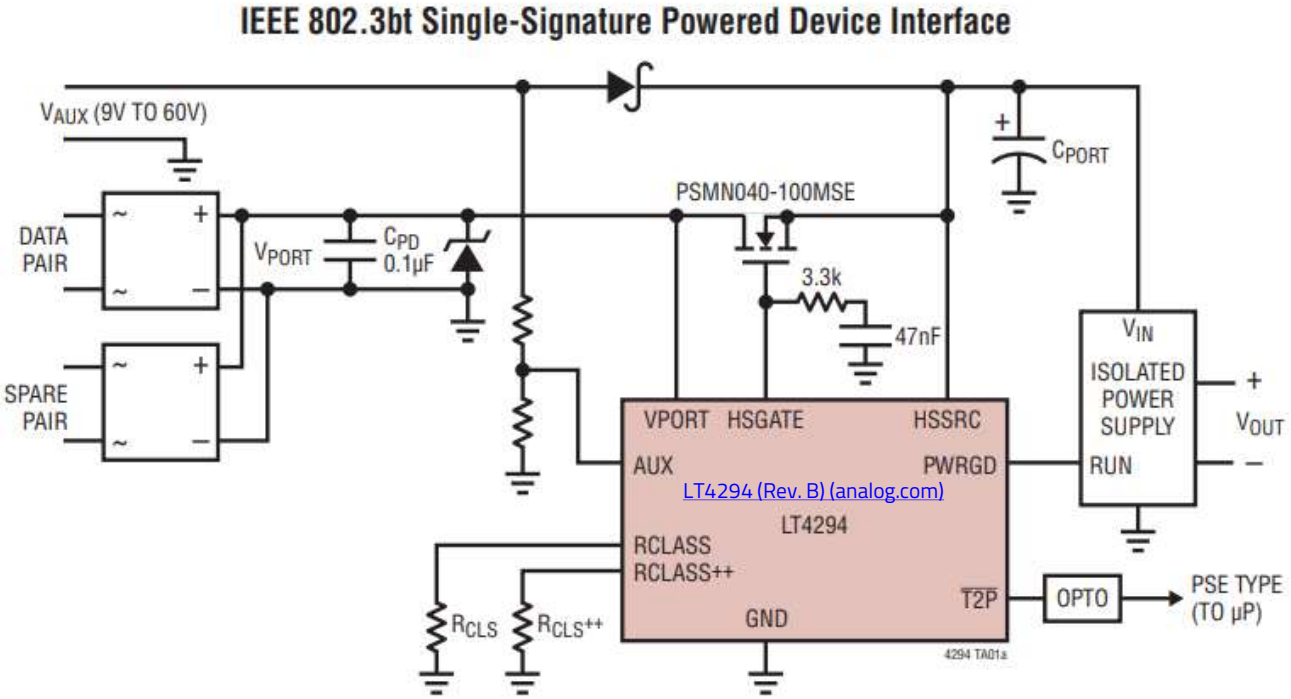
DISCRETE SOLUTION

Example

- Two ICs
  - One for the PSE<->PD hand shake (interface controller)
  - Second for control of isolated DC/DC converter.
- Gives more flexibility for future re-design in case of obsolescence/EoL.
- Gives more options / alternatives for either IC.



MAX5995A-C



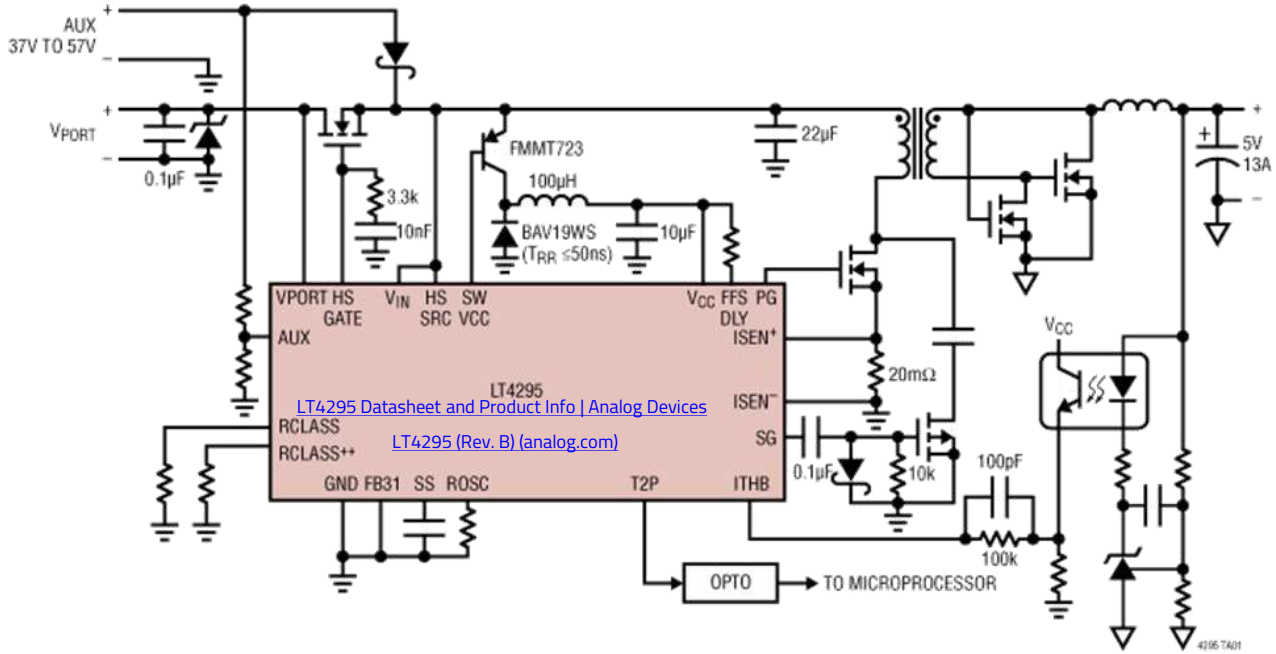
LT4294 (Rev. B) (analog.com)

DC2911A (Rev. 0) (analog.com)

INTEGRATED SOLUTION

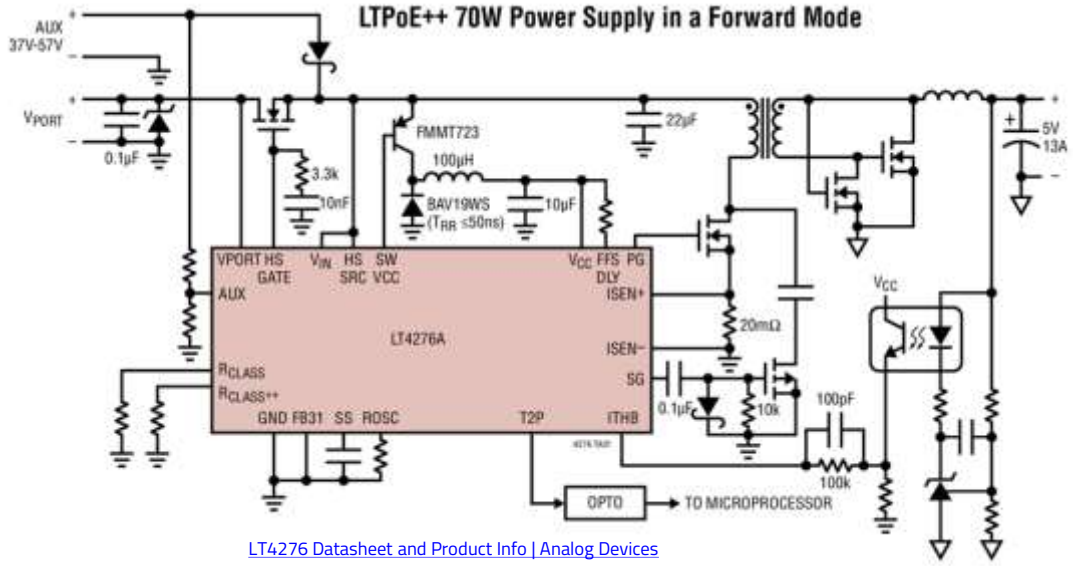
Example

- One IC including both functionality:
  - PSE<->PD hand shake (interface controller)
  - DC/DC converter controller
- Less parts. Smaller pcb area
- Easier/better layout and tracking
- Ability to add extra filtering



LT4295 Datasheet and Product Info | Analog Devices

LT4295 (Rev. B) (analog.com)



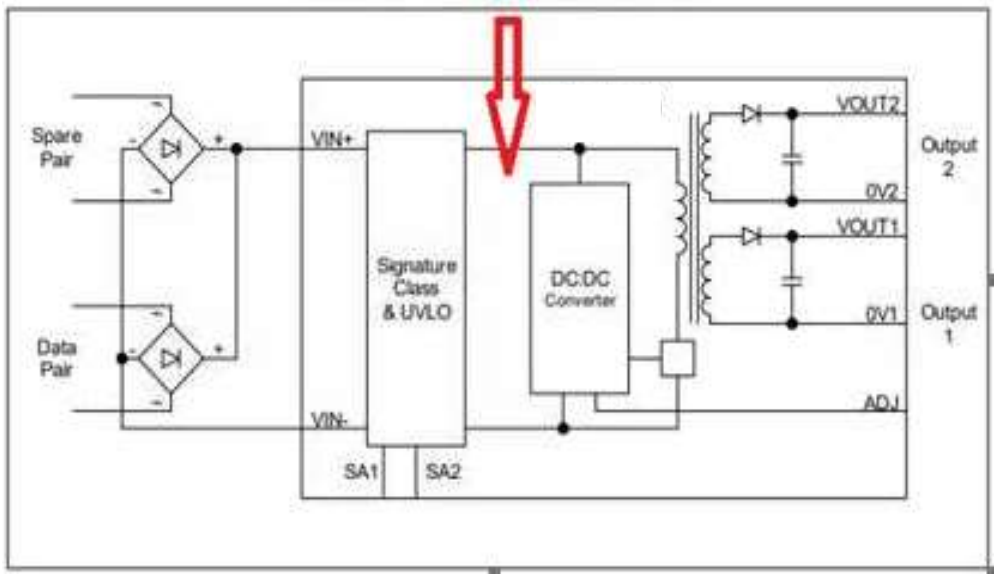
LT4276 Datasheet and Product Info | Analog Devices

DC2047A-A

MODULE SOLUTION

Example

- Module Includes:
  - PSE<->PD hand shake (interface controller)
  - DC/DC converter controller
  - DC/DC isolated converter
- Less parts. Smaller pcb area
- Easier/better layout and tracking
- Faster time to market.
- However:
  - No access to the Power Converter Input to introduce the filtering after the PoE Signature/Class communications.
  - The filter capacitance is the issue here as indicated in the 2012 revision of the IEEE 802.3 standard.
  - This limits C to 150nF.
  - No guarantee of using up to 10uF (may accept or reject). Ref sections 33.2.5.3 & 33.2.5.4 on PD detection and rejection criteria.



PRACTICAL DESIGN EXAMPLE POE PD

POWER CONVERTER DESIGN PROCESS / GUIDELINES

Introduction

- Requirements Capture
  - Steady State (ss) and Dynamic response
  - Power Quality, EMI, Safety, …etc.
  - Abnormal Operating conditions, Fault Tolerance, …etc.
  - Application Specific Requirements (Isolation, Power, Protection, ..etc.)

- Topology Selection
  - Electrical Specifications
  - Other constraints (Size, Cost, …etc.)

1) Full Converter Stage Design
   - Schematic capture, Mathematical analysis and calculations, Simulation, Prototyping and Optimisation.
   - Thermal Analysis and Stress Analysis.
   - Layout and Tracking
   - Functional Testing, Power Quality, Loop Measurements and Stabilisation.
   - FMEA, …etc.

DESIGN PROCESS / GUIDELINES

Introduction

2) Base DC/DC Converter Design On:

- IC Reference Design / Evaluation Board / Kit

CAUTIONs	**MUSTs**
Design Specs do not match your requirements	Maintain Functionality to your Specs
Different ss /dynamic loading requirements	Perform Thermal Management / Analysis to your requirements
No EMI Considerations / Testing	Maintain the reliability / quality to the product's Warrantee / Brand Name
Ref Designs Only Work Under Specific Load, Line and Temperature Conditions	

3) A Power Converter Module

POE PD FLYBACK CONVERTER

Customer Design Requirements Capture

- PoE PD 60W Type 3 / 4
- IEEE802.3.bt
- 1500V Functional Isolation
- Vin= 36V-57V
- Vout = 12V
- Iout = 5A
- Required Efficiency > 90%
- Common and differential EMC filtering
- <5% output ripple
- <65DegC max board/component Temperature (based on an Ambient of 25DegC)

POE PD FLYBACK CONVERTER

Design Architecture

- Discrete Solution
- Synchronous rectified Flyback Topology – (Efficiency and Temperature requirements)
- Use LT3748 Chipset LT3748 (primary side regulation IC)
- Base design on Reference Design (DC1961AF)
- New Power Transformer – (Efficiency and Temperature requirements)
- To maintain efficiency requirement:
  - Use FETs for the input Bridge Rectifier
  - Driver LT4321
- PSE/PD Handshake Chip (LT4294)
- Front end Reference Design (DC2583A)
- Input LC Differential Mode Filter (EMC requirement)
- Input Common Mode Filter (EMC Requirement)
- Output LC Filter (Ripple requirement)

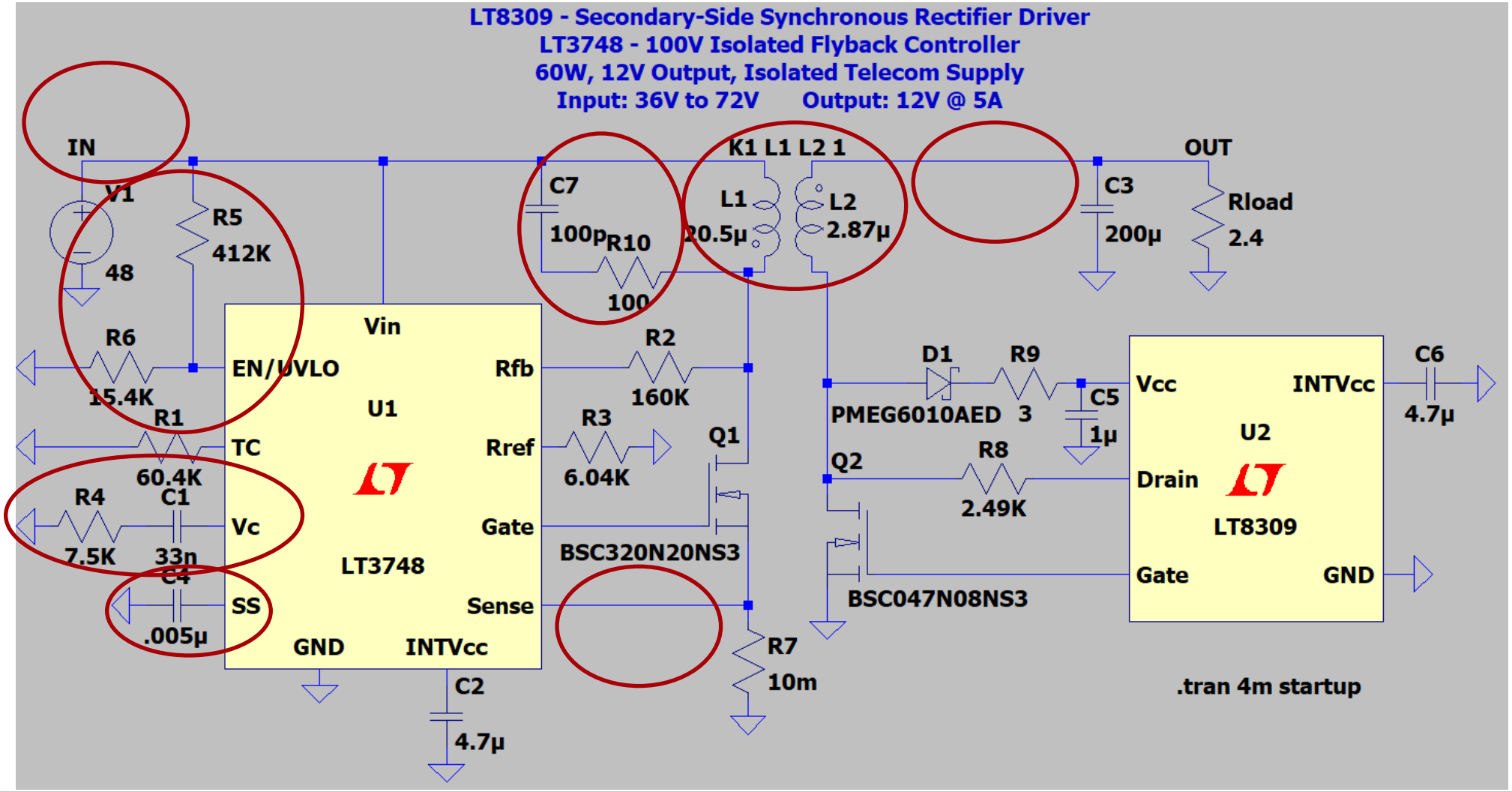
POE PD FLYBACK CONVERTER

Design Verification/Modifications

- LT Spice Simulation of DC1961AF Ref Design
- LT 3748 Datasheet Review and Design modification:
  - New Power Transformer design and calculations
  - Reset UVLO thresholds
  - Dynamic response improvements
  - Output OVP under light load
  - Clamp Snubber re-design
  - Current sense filter design
  - Implementation of input and output LC DM filter
  - Implementation of input CMC Filter.
  - Alternatives to Main and Sync FETs (lower RDS on)
- Modify Evaluation Board and Test
- Create Initial Prototype Hardware Test and Verify

POE PD FLYBACK CONVERTER

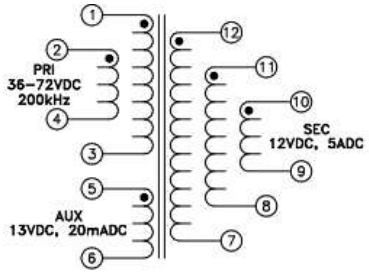
DC1961AF LT SPICE SIMULATION



POE PD FLYBACK CONVERTER

POWER TRANSFORMER

- Ref Design uses EFD20 Transformer [spec similar to 750310644]

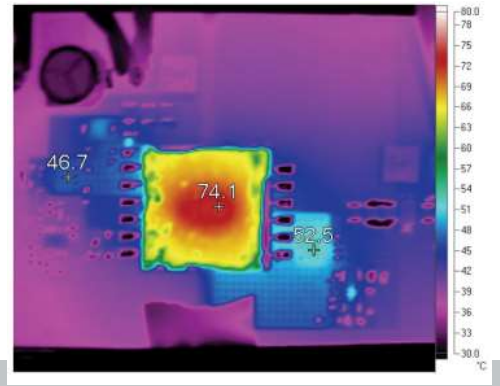


750310644

ELECTRICAL SPECIFICATIONS @ 25°C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	1–4	tie(1+2, 3+4), @20°C	0.039 ohms max.
D.C. RESISTANCE	12–7	tie(7+8+9, 10+11+12), @20°C	0.0085 ohms max.
D.C. RESISTANCE	5–6	@20°C	0.230 ohms max.
INDUCTANCE	1–4	tie(1+2, 3+4), 200kHz, 100mVAC, Ls	20.5uH ±5%
LEAKAGE INDUCTANCE	1–4	tie(1+2, 3+4, 7 thru 12), 200kHz, 100mVAC, Ls	1.0uH max.
DIELECTRIC	1–12	tie(1+2, 10+11+12), 1800VAC, 1 second	-
DIELECTRIC	1–12	tie(1+2+5, 10+11+12), 1800VAC, 1 second	-
TURNS RATIO		(2–4):(12–7) tie(7+8+9, 10+11+12),	2.67:1, ±3%
TURNS RATIO		(1–3):(12–7) tie(7+8+9, 10+11+12),	2.67:1, ±3%
TURNS RATIO		(5–6):(12–7) tie(7+8+9, 10+11+12),	1.17:1, ±3%

- Temperature rise 74.1DegC at 48Vin/12Vout/5Aout

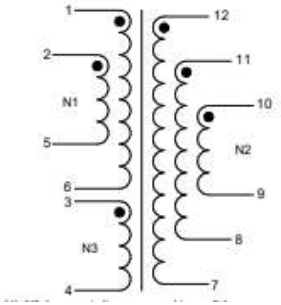


- Decision to go to a bigger EFD25 Core 750319021

Electrical Properties: **750319021**

Properties		Test conditions	Value	Unit	Tol.
Inductance	L	N1/ 10 kHz/ 100 mV	22	µH	±10%
Turns Ratio	n	N1 : N2 : N3	2.4:1:1		
Saturation Current	I_{SAT}	N1/ ΔL/L < 20 %	10.8	A	typ.
DC Resistance 1	$R_{DC\,1}$	N1/ 20 °C	18	mΩ	max.
DC Resistance 2	$R_{DC\,2}$	N2/ 20 °C	8	mΩ	max.
DC Resistance 3	$R_{DC\,3}$	N3/ 20 °C	125	mΩ	±10%
Leakage Inductance	L_S	100 kHz/ 100 mV	0.75	µH	max.
Insulation Test Voltage	V_T	N1,3 => N2	1500	V (AC)	

Schematic:



- **BUT IS IT GOING TO WORK?**

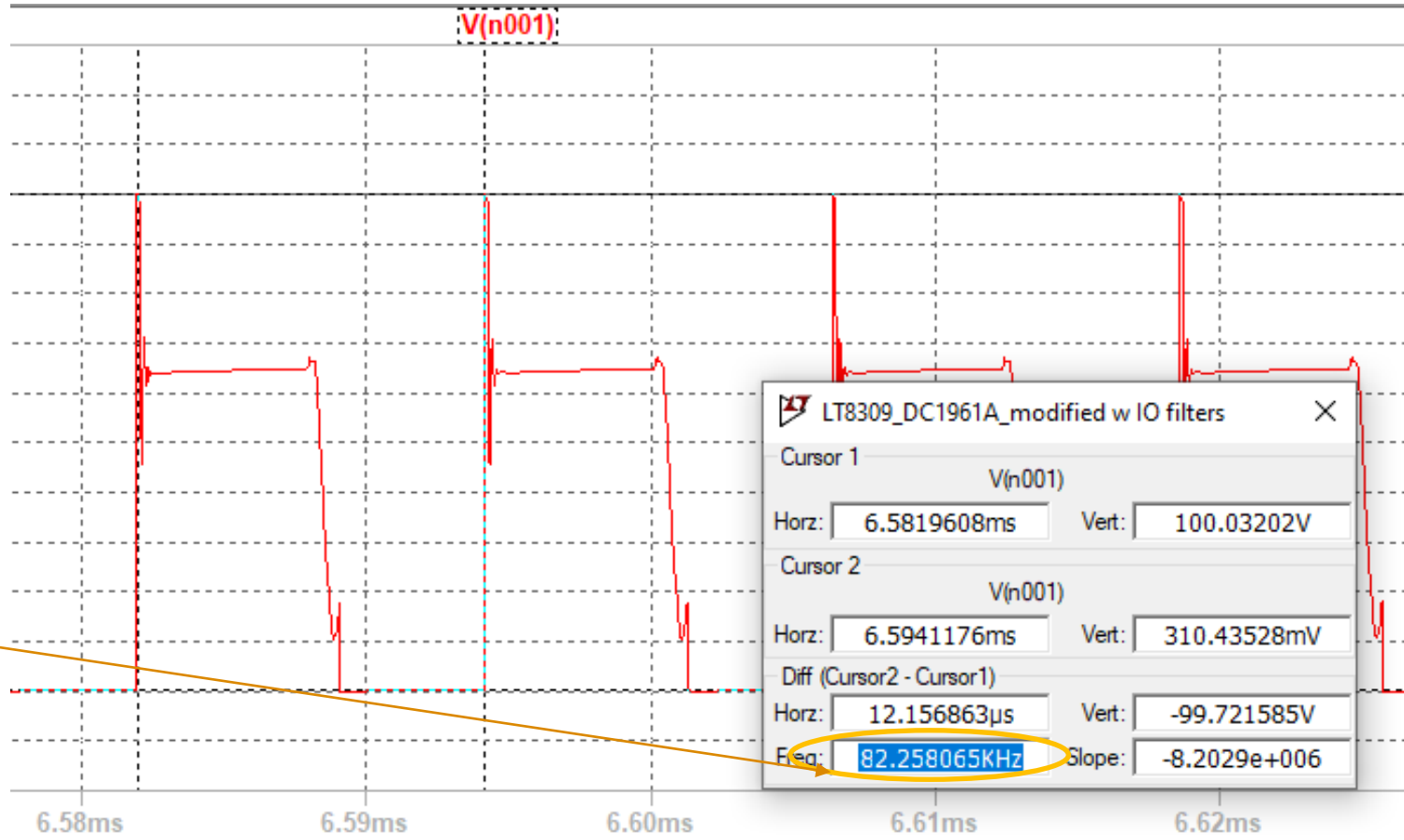
POE PD FLYBACK CONVERTER

POWER TRANSFORMER

- Let's check by doing Transformer Calculations…… DIFFICULT.
- WHY?
  - LT3748 is a Boundary Mode Controller
    - Switching frequency changes with Load/Line conditions
  - Two options:
    - Use datasheet calculation:

$$L_{PRI} \le V_{IN(MIN)} \bullet (V_{OUT} + V_{F(DIODE)}) \bullet N_{PS} / (f_{SW(MIN)} \bullet I_{LIM} \bullet ((V_{OUT} + V_{F(DIODE)}) \bullet N_{PS} + V_{IN(MIN)}))$$

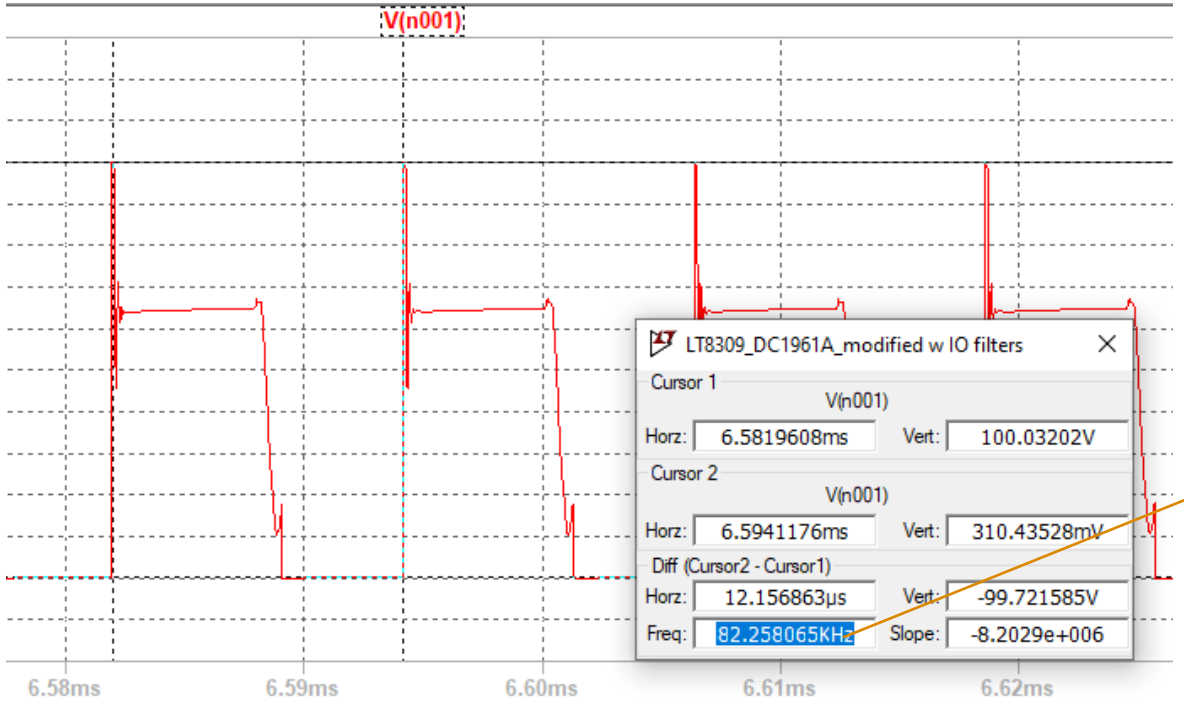
    - Use LT Spice Simulation
      - Better and quicker and more accurate provided good models



POE PD FLYBACK CONVERTER

POWER TRANSFORMER

- Let's check by doing Transformer Calculations……



WE Flyback Transformer Selection

WE Transformer DS Parameters

Part Number	750319021	
Lp	2.20E-05	H
Np	2.4	
Ns	1	
Naux	1	
Vout	12	V
Ip_sat	10.8	A
Io_dc	8	A
Rdc_p	0.018	Ω
Rdc_s	0.008	Ω

Design Requirements

Vin_min	36	V
Vin_nom	48	V
Vin_max	57	V
Pout_max	60	W
Pout_min	10	W
Efficiency	0.85	
Vo	12	V
VF Diode	0.2	V
f	8.20E+04	Hz

Results

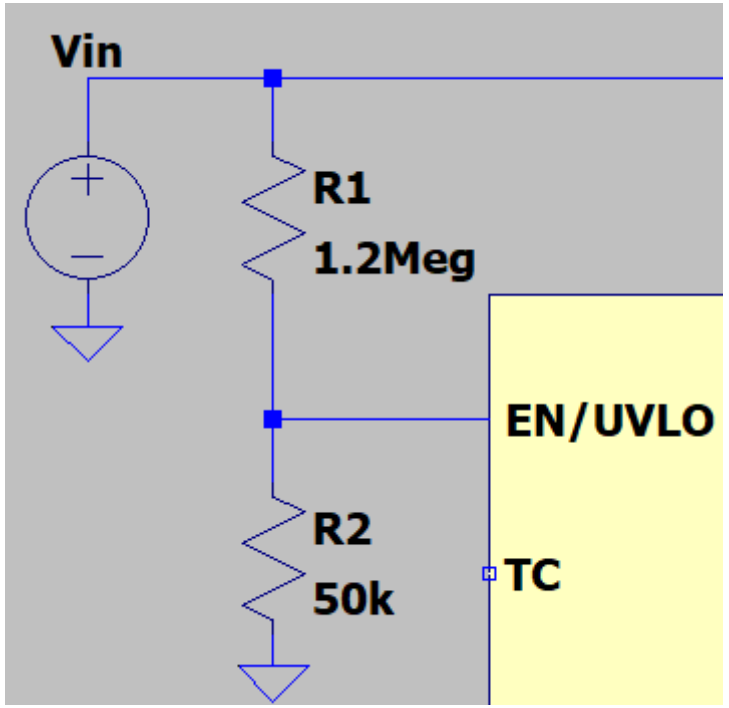
	Pout_max			Pout_min		
	Vin_min	Vin_nom	Vin_max	Vin_min	Vin_nom	Vin_max
Operating Mode:	DCM	DCM	DCM	DCM	DCM	DCM
D	0.4433	0.33247	0.27998	0.18098	0.1357321	0.1143
D2	0.5025	0.5025	0.5025	0.20515	0.2051456	0.20515
D3	0.0542	0.16502	0.21752	0.61388	0.6591223	0.68055
Ip_dc	1.96078	1.47059	1.23839	0.3268	0.245098	0.2064
ΔIp	8.84633	8.84633	8.84633	3.6115	3.6114971	3.6115
Ip_pk	8.84633	8.84633	8.84633	3.6115	3.6114971	3.6115
Ip_rms	3.40056	2.94497	2.70249	0.88703	0.7681887	0.70494
Is_pk	19.5742	19.5742	19.5742	7.99113	7.9911259	7.99113
Is_rms	8.01109	8.01109	8.01109	2.08967	2.0896735	2.08967
Vaux	12			12		
Iout	5			0.83333		
Rdc losses	0.72157					

POE PD FLYBACK CONVERTER

UVLO THRESHOLDS

- VIN(UVLO,FALLING) = 1.223V ▪(R1+R2)/R2
- VIN(UVLO,RISING) = 1.223V ▪[(R1+R2)/R2] + 2.4µA ▪R1

R1/R2	412k / 15.4k	1.2M / 50k	1.2M / 47k
VIN(UVLO, FALLING)	33.94V	30.58V	32.45V
VIN(UVLO, RISING)	34.93V	33.46V	35.33V

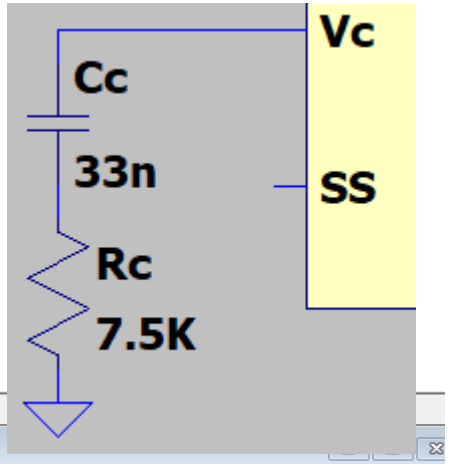


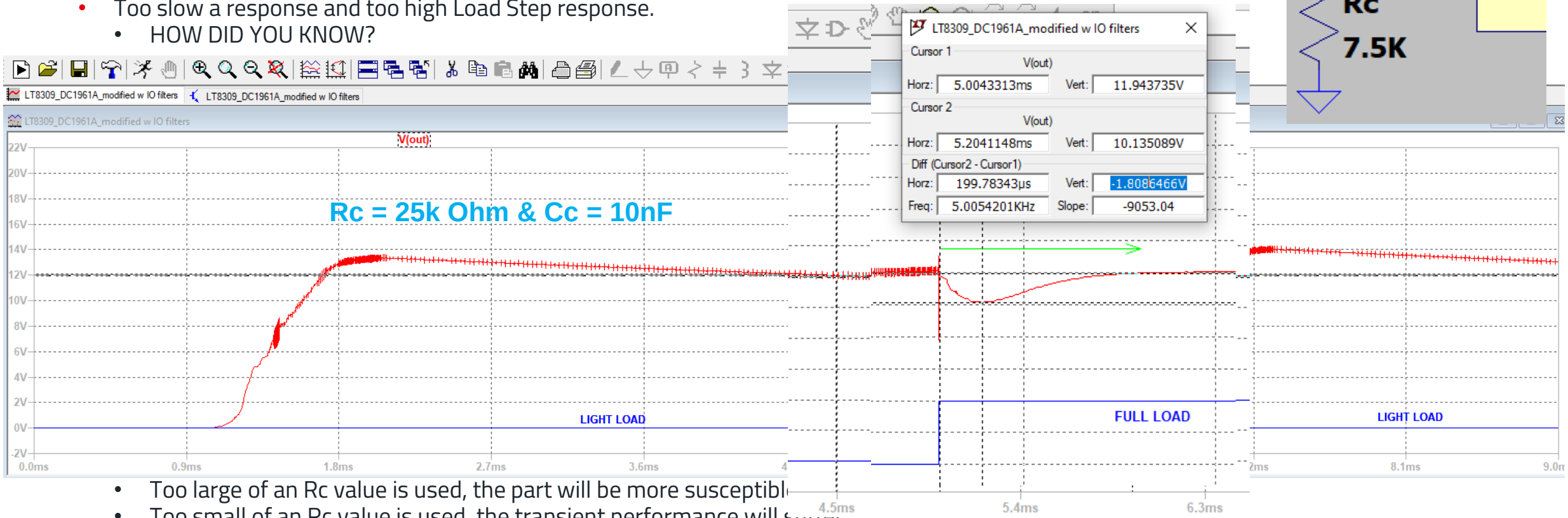
- Consider:
  - Wider hysteresis
  - Voltage Drop across Bridge
  - Min Flyback Operating Input Voltage

POE PD FLYBACK CONVERTER

DYNAMIC RESPONSE IMPROVEMENTS

- Compensation network connected to Vc pin of the LT3748.
- Values used in Ref Design are Rc = 7.5k and Cc = 33nF
- Too slow a response and too high Load Step response.
  - HOW DID YOU KNOW?





- Too large of an Rc value is used, the part will be more susceptibl
- Too small of an Rc value is used, the transient performance will suffer.
- Similarly; Too small a Cc value can result in an unstable loop and with too large a Cc value the transient performance will suffer. (>1nF)

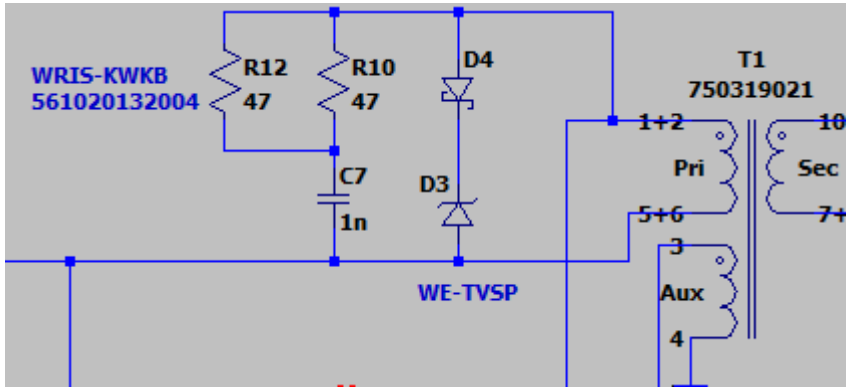
POE PD FLYBACK CONVERTER

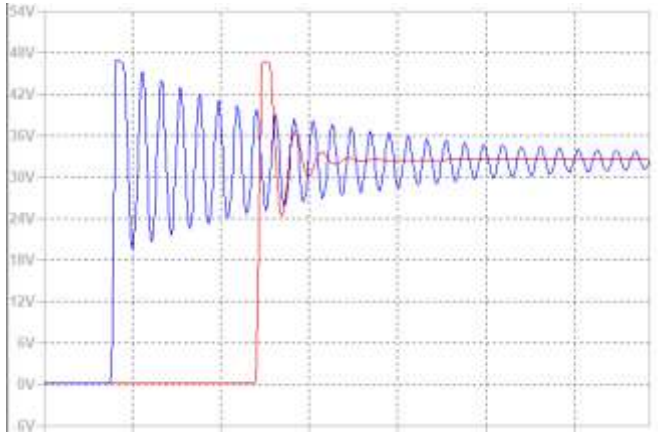
OVP/Snubber Clamp/Current Sense Filter

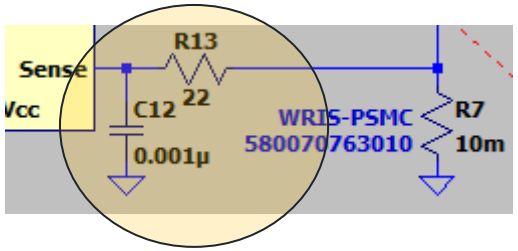
- Output OVP under light load
  - Minimum Load at Light load conditions
  - Clamp the output voltage (OVP connected loads)
  - WE-TVSP

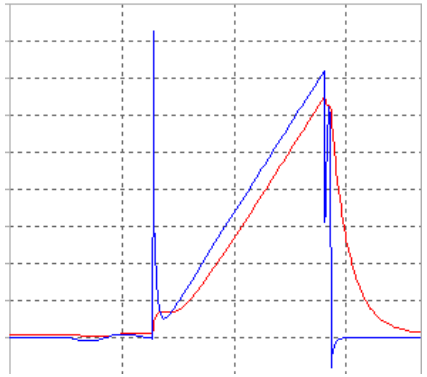
- Clamp Snubber re-design
  - Clamp the Vds Voltage Spike and protect across MOSFET DS junction
  - Damp the ringing of Transformer Llk and Main FET Cds
  - WE-TVSP

- Current sense filter design
  - Implement a LP RC Filter (LEB)





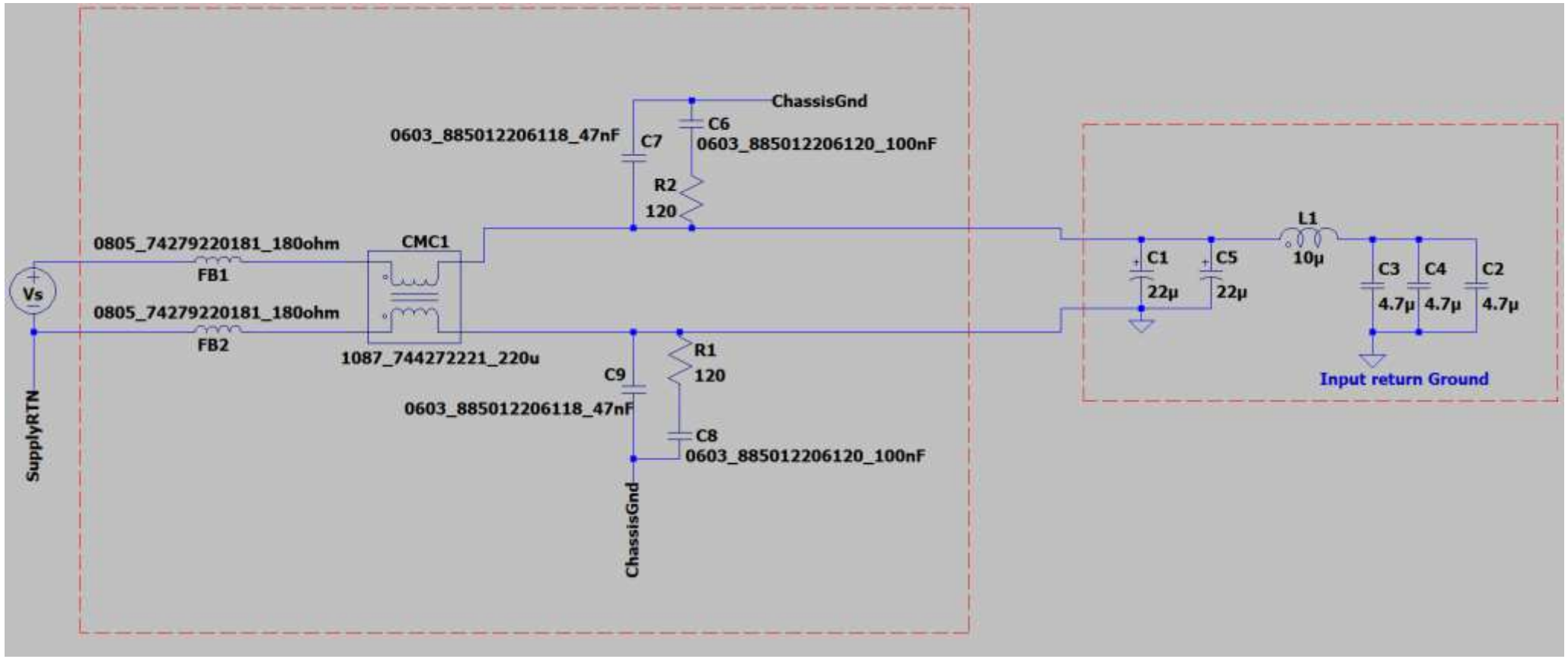




POE PD FLYBACK CONVERTER

Input CM and DM filter

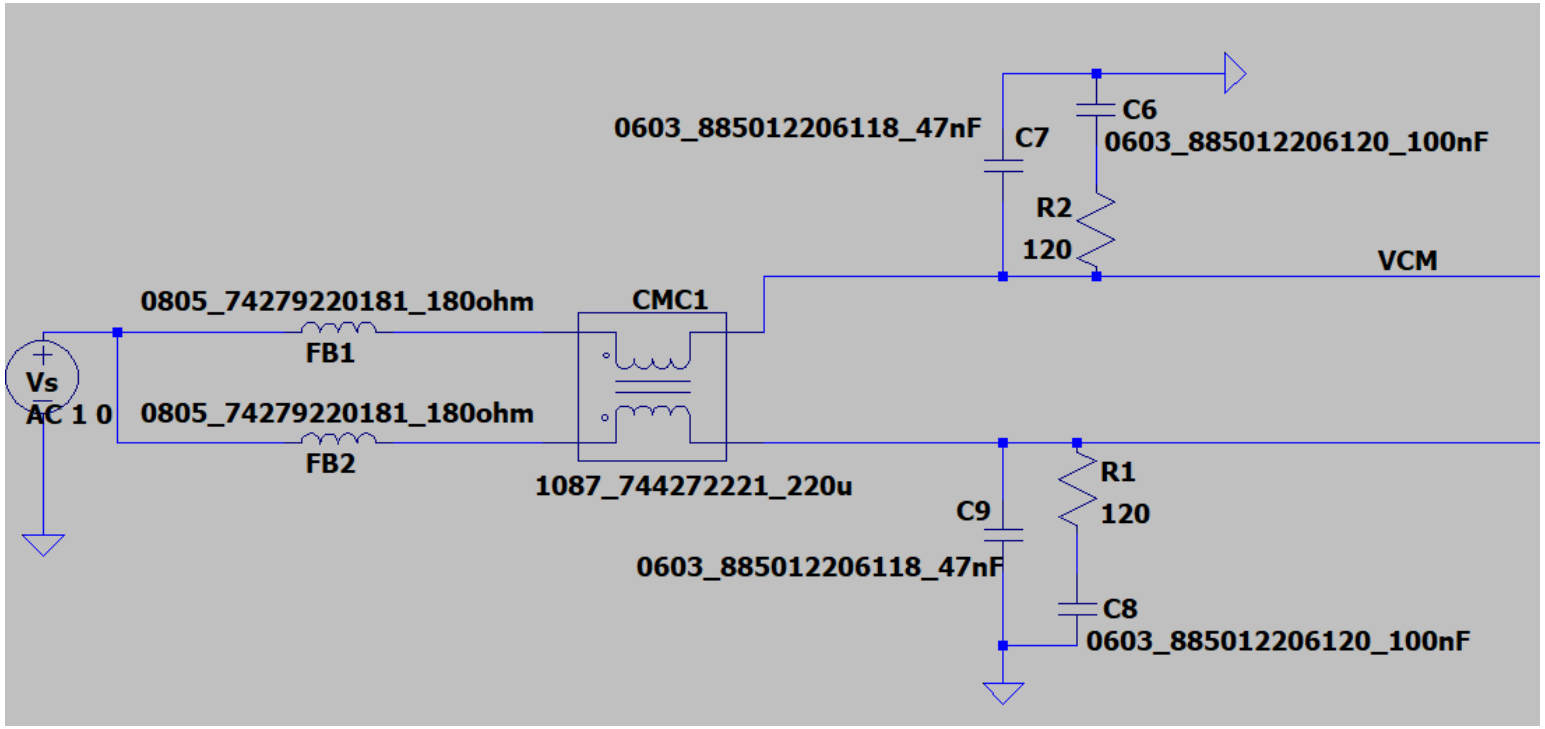
- Conducted and radiated emissions, Common and differential Noise.

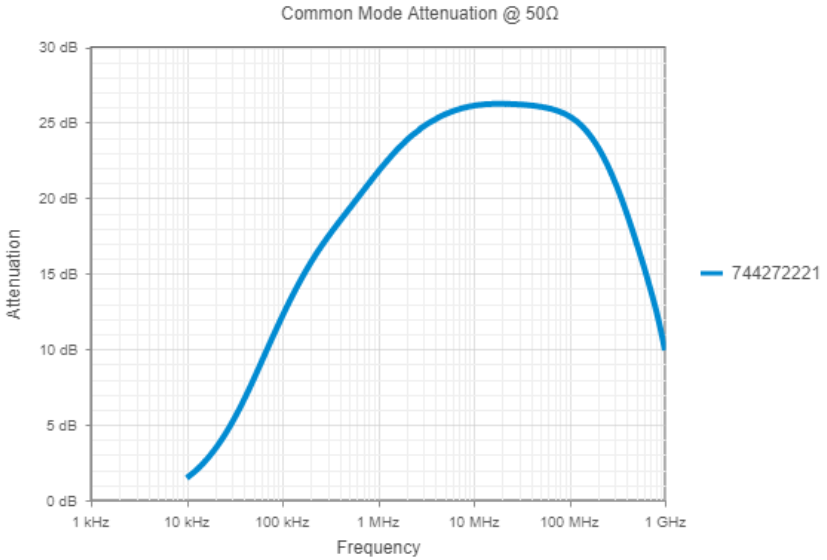


POE PD FLYBACK CONVERTER

Input CM filter

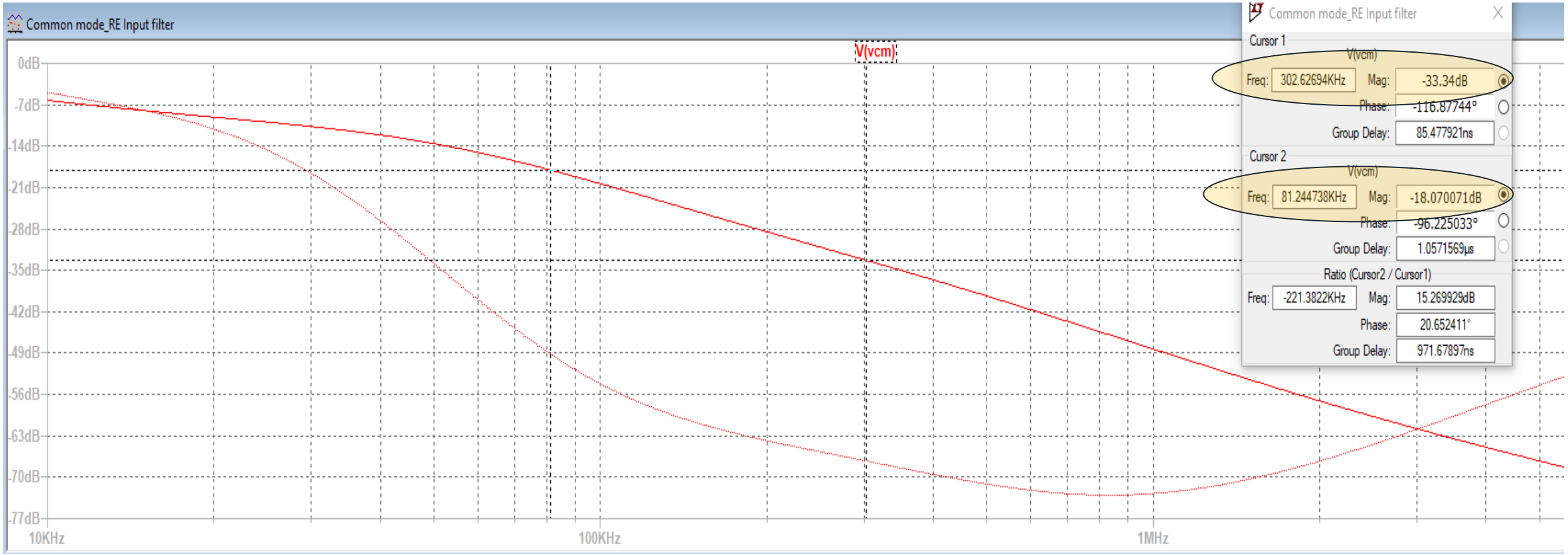
- Common mode Filter design:
  - Input Current = Pout/(ηVin)= 60/(32x0.9) = 2.1A
  - Fs = 80kHz min -> 300kHz max
  - CMC Redexpert selection (Max insertion loss): https://we-online.com/re/5qQVnnIg





POE PD FLYBACK CONVERTER

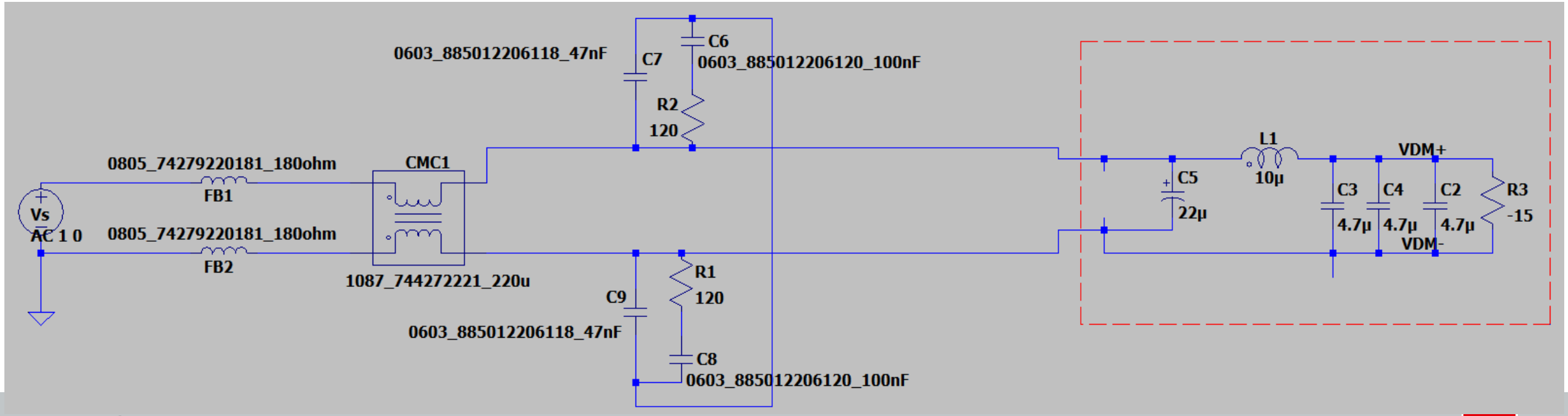
Input CM filter Insertion loss



POE PD FLYBACK CONVERTER

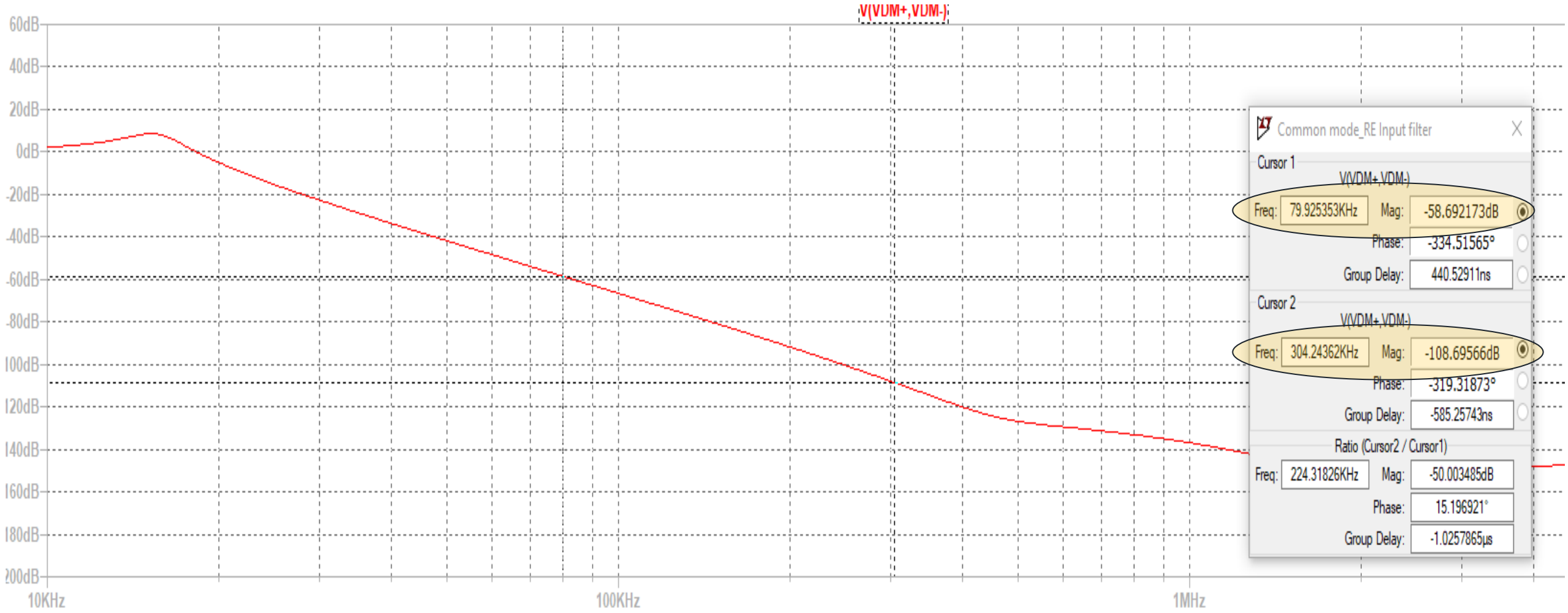
Input DM filter

- Differential mode Filter design:
  - Input Current = Pout/(ηVin)= 60/(32x0.9) = 2.1A
  - Fs = 80kHz min -> 300kHz max
  - Inductor Redexpert selection (Efficiency & Size): https://we-online.com/re/5qQWs8oz
    - WE-XHMI https://www.we-online.com/en/components/products/datasheet/74439358100.pdf
  - Capacitor Selection (Max insertion loss & Size)
    - Low ESR/Profile Aluminum Polymer and MLCCs



POE PD FLYBACK CONVERTER

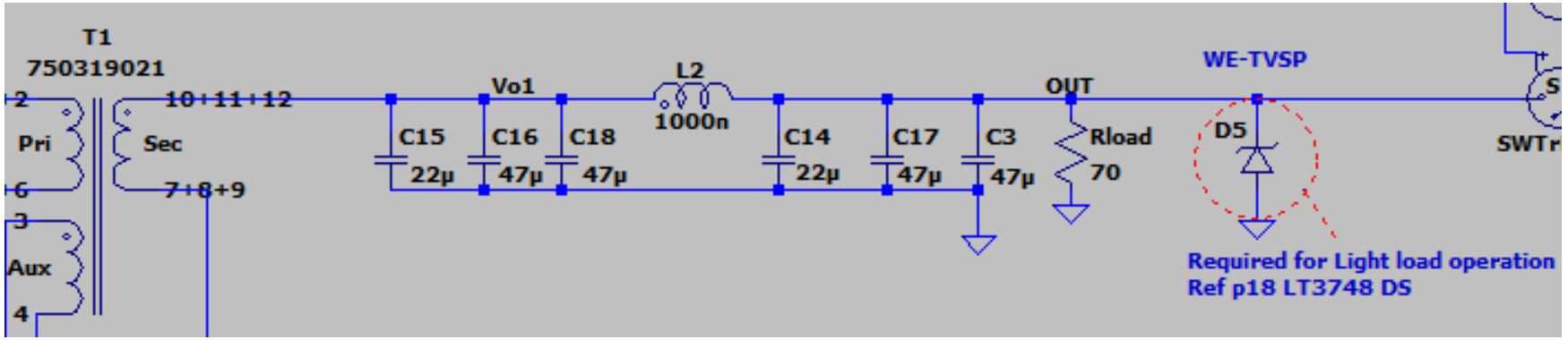
Input DM filter



POE PD FLYBACK CONVERTER

Output LC Filter

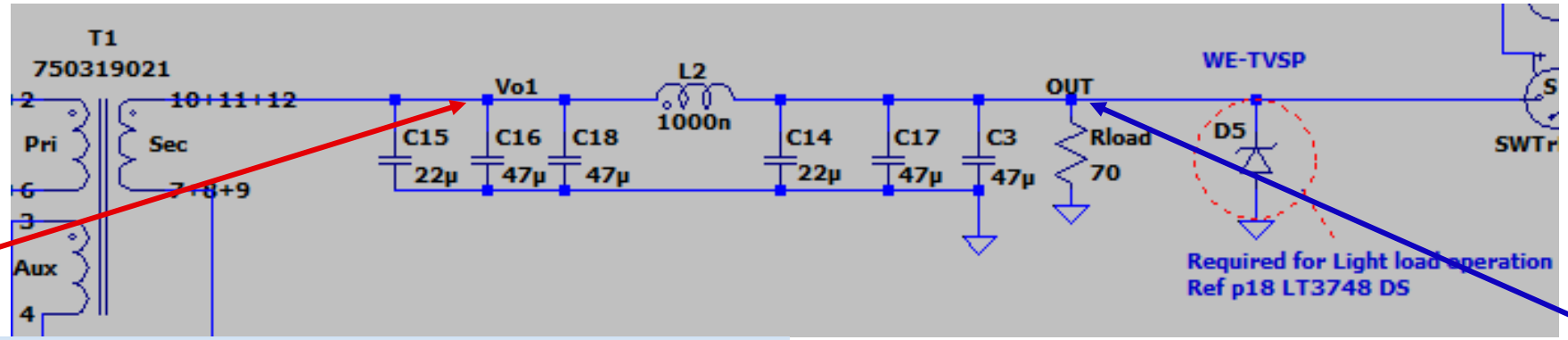
- Differential mode Filter design:
  - Output Current = 5A
  - Fs = 80kHz min -> 300kHz max
  - Ripple rejection
  - Inductor Redexpert selection (Efficiency & Size): https://we-online.com/re/5qQYfWkg
  - WE-LHMI https://www.we-online.com/en/components/products/datasheet/74437349010.pdf
  - Capacitor Selection (Max insertion loss & Size)
    - Low ESR/Profile Aluminum Polymer and MLCCs

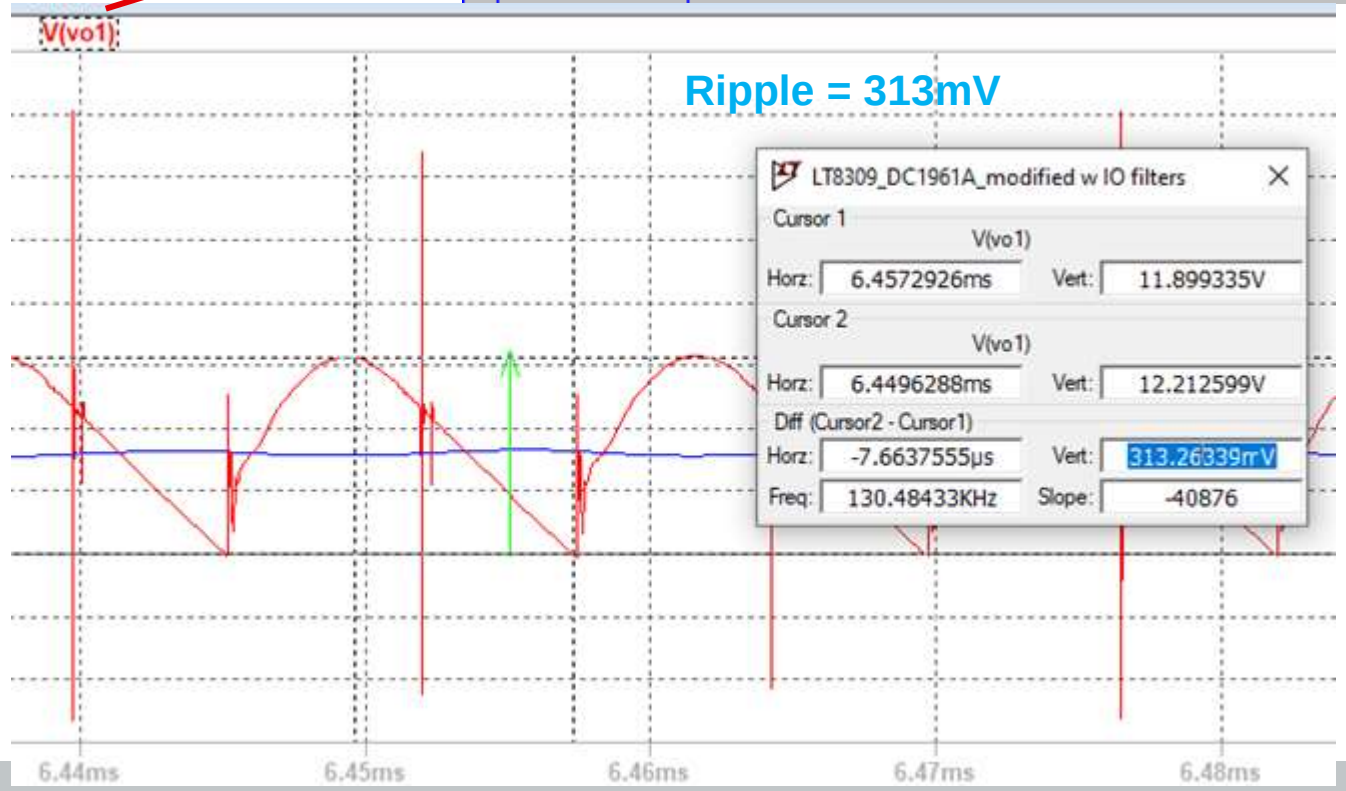


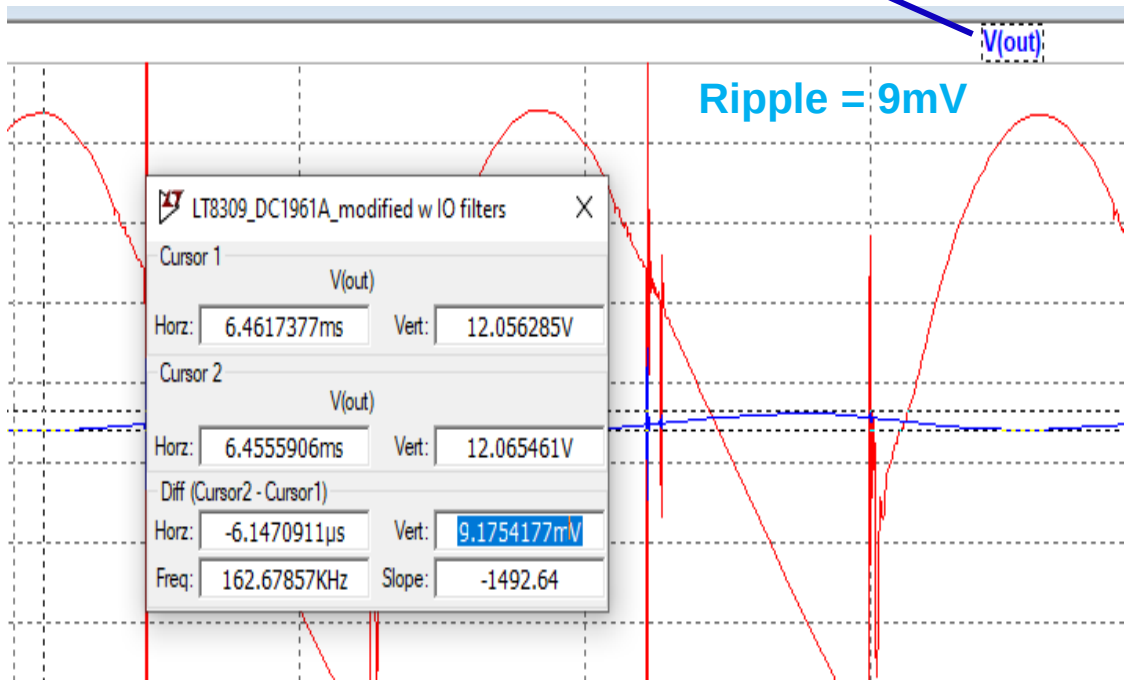
POE PD FLYBACK CONVERTER

Output LC Filter

- Ripple rejection



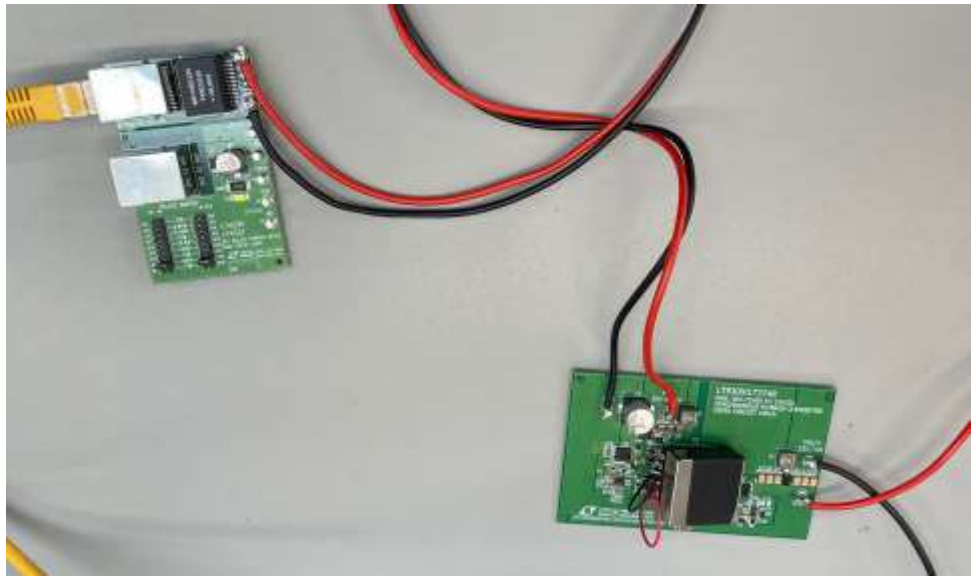


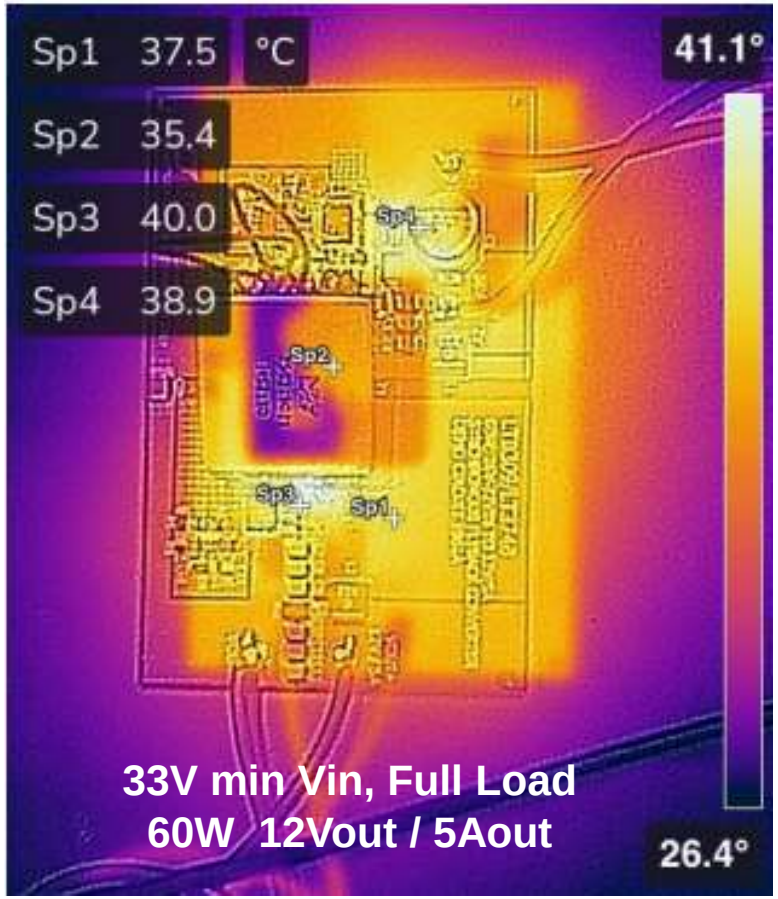


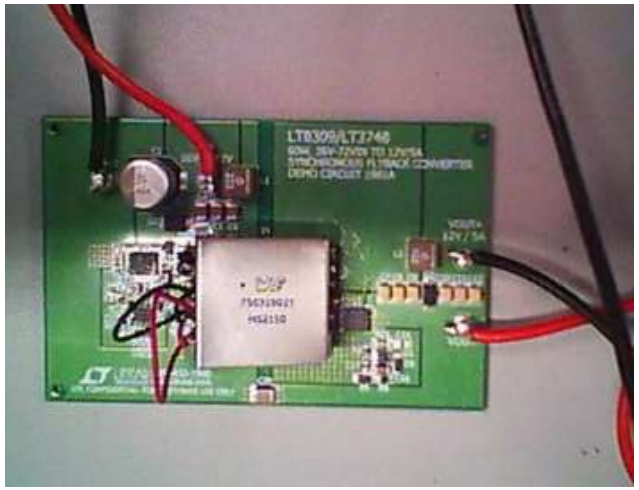
POE PD FLYBACK CONVERTER

Modify Evaluation Board and Test

- Evaluation Boards for both Handshake and Flyback converter.
- Boards Modified as discussed
- Initial Functional testing
  - Load/Line regulation
  - Temperature
  - Dynamic Load Step
  - UVLO Thresholds







POE PD FLYBACK CONVERTER

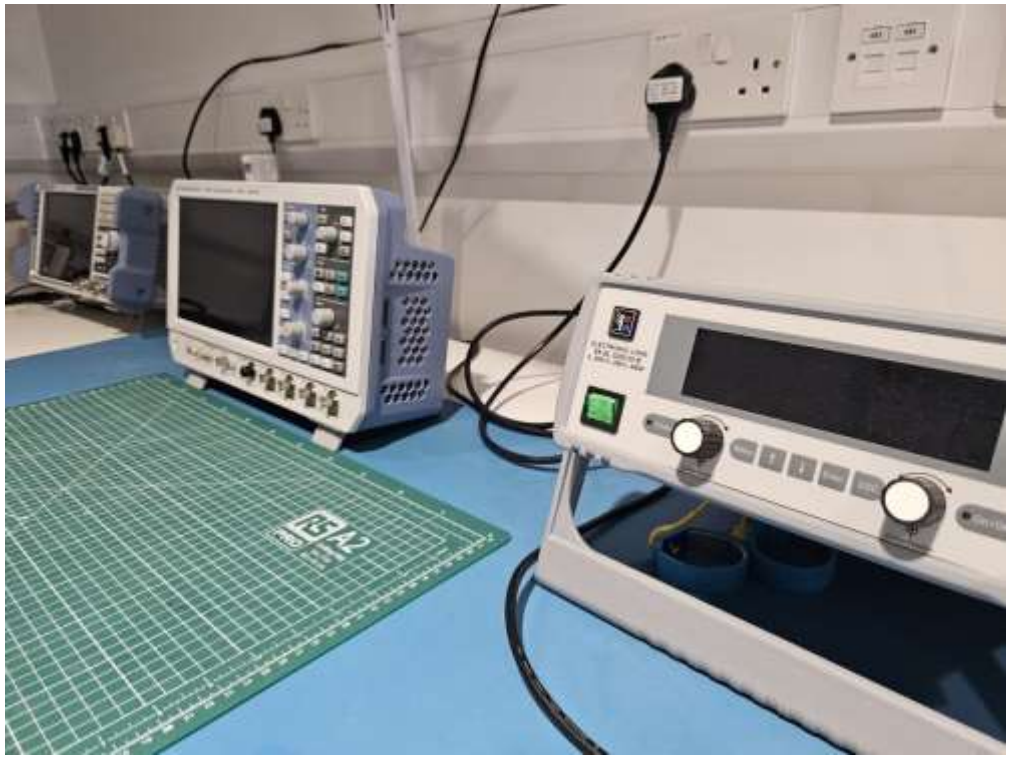
MODIFY EVALUATION BOARD AND TEST SUMMARY

- Regulation is fine across the load and line spec conditions
- Efficiency is 94% at full load (60W) and min Vin.
- Thermal performance is very good (max board temperature 42DegC).
- Load Transient is good. Can be improved further.

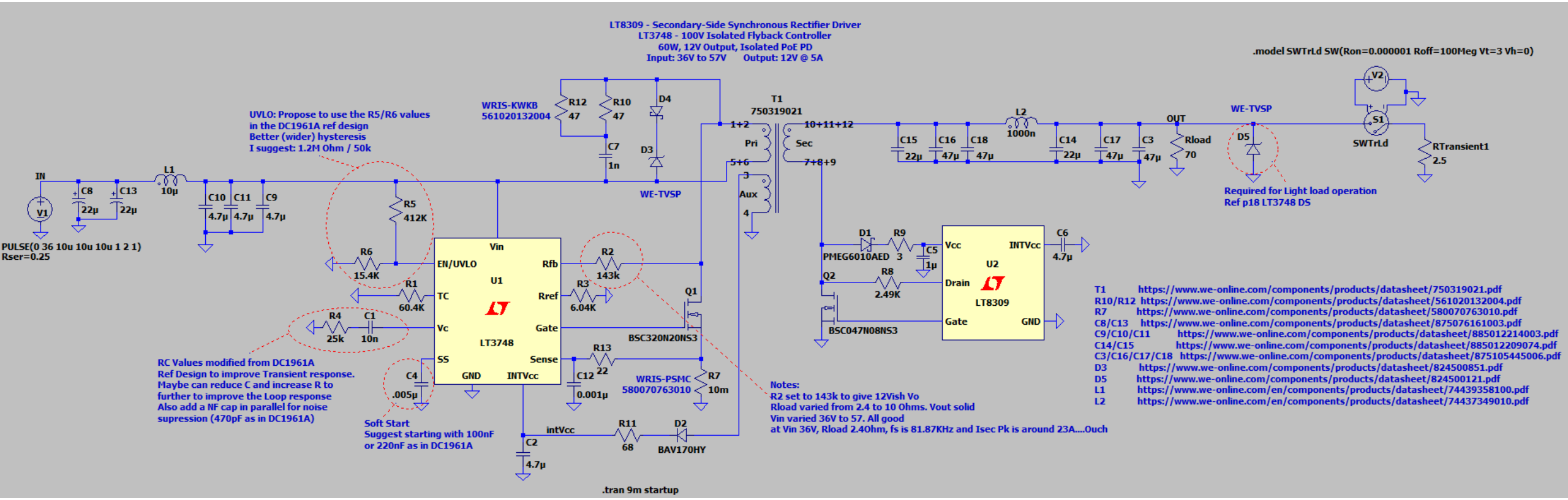
POE PD FLYBACK CONVERTER

Create Initial Prototype Hardware Test and Verify

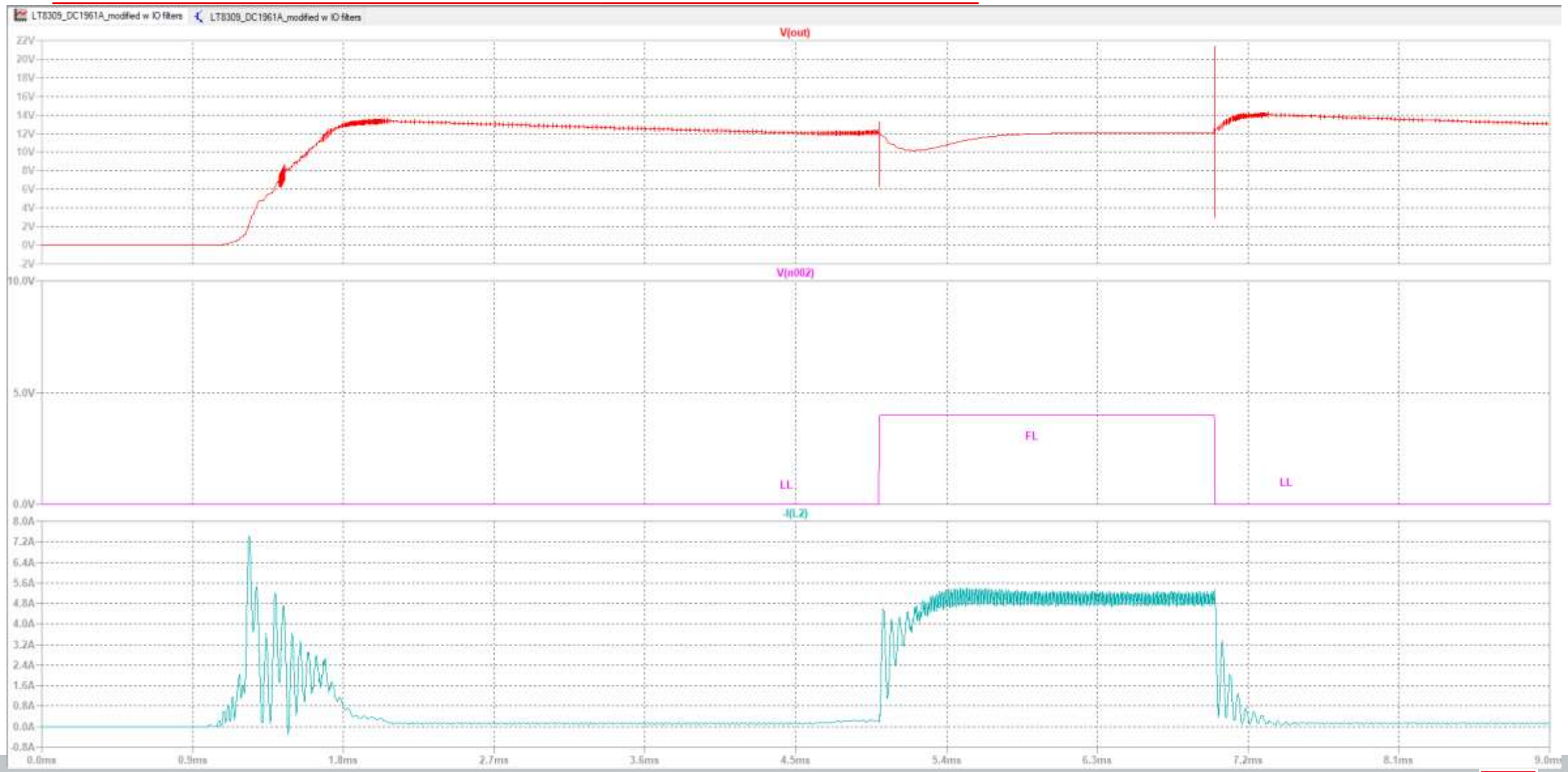
- Ongoing Progress
- Testing at our Manchester Office Lab Facility
- Full Functional Testing:
  - Regulation, Dynamic and Thermal performance
- Signal Integrity and noise immunity:
  - Conducted Emissions debugging
  - Radiated Emissions investigation



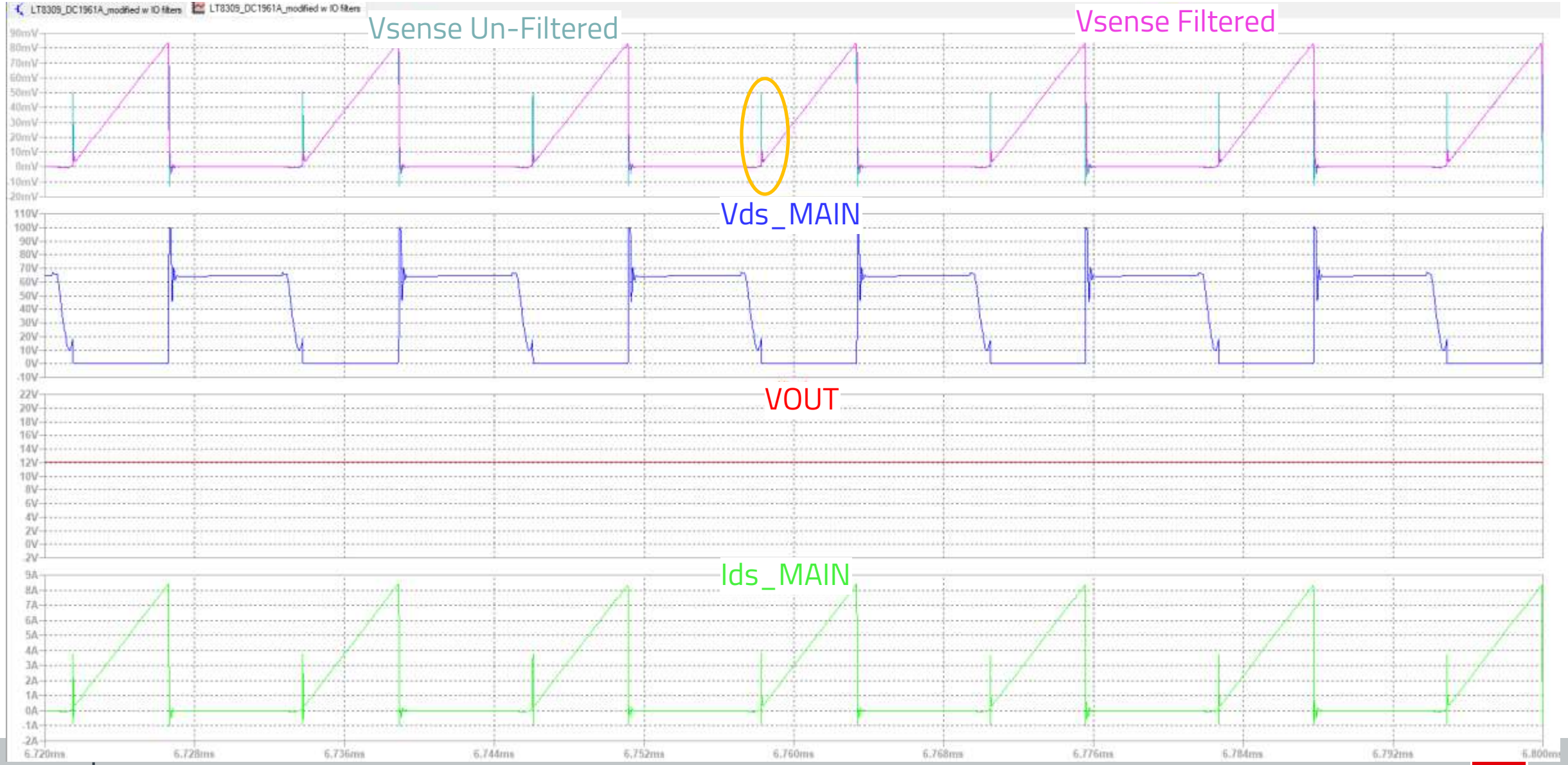
POE PD FLYBACK CONVERTER DESIGN SIMULATION



POE PD FLYBACK CONVERTER DESIGN SIMULATION



POE PD FLYBACK CONVERTER DESIGN SIMULATION



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Signal & Communications | Passive Components | Würth Elektronik Product Catalog (We-online.Com)

Questions

& Answers

We are here for you now!
Ask us directly via our chat or via E-Mail.

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