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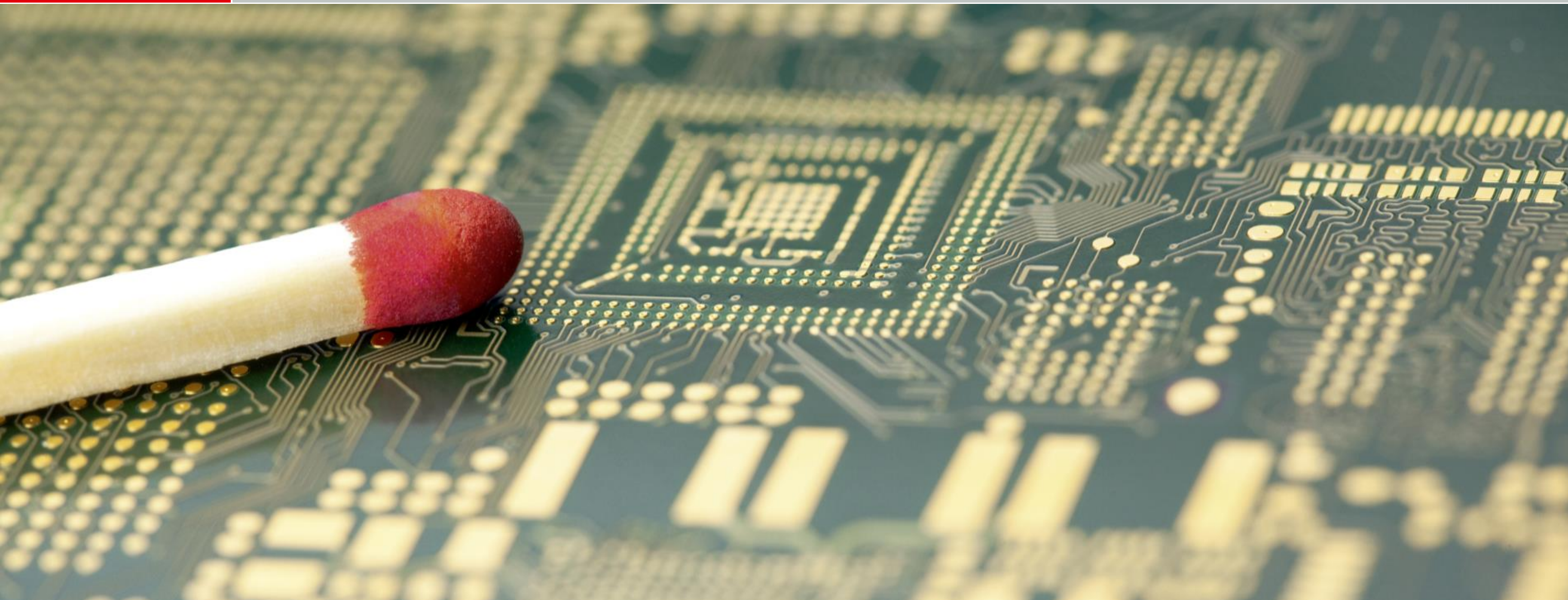
# MINIATURIZATION FOR INDUSTRIAL ELECTRONICS, TAKING COST AND RELIABILITY ASPECTS INTO ACCOUNT



Andreas Dreher

28th September 2022

# AGENDA

Miniaturization – Rigid PCBs

1 Correlations in miniaturization

2 Stack-ups, PCB size, Design Rules HDI (High Density Interconnect)

3 HDI technologie variants & development of costs

4 Reliability – Interconnect Stress Test

5 Case Study Reliability – PCB thickness

6 Case Study Reliability – Type of interconnect

# YOUR SPEAKER

## Andreas Dreher

- Technical Project Management
  - General technology
  - Customer consulting

- With Würth Elektronik CBT since 2003

Here's how to reach me:

- Tel.: +49 7622 397-133
- E-Mail: andreas.dreher@we-online.de

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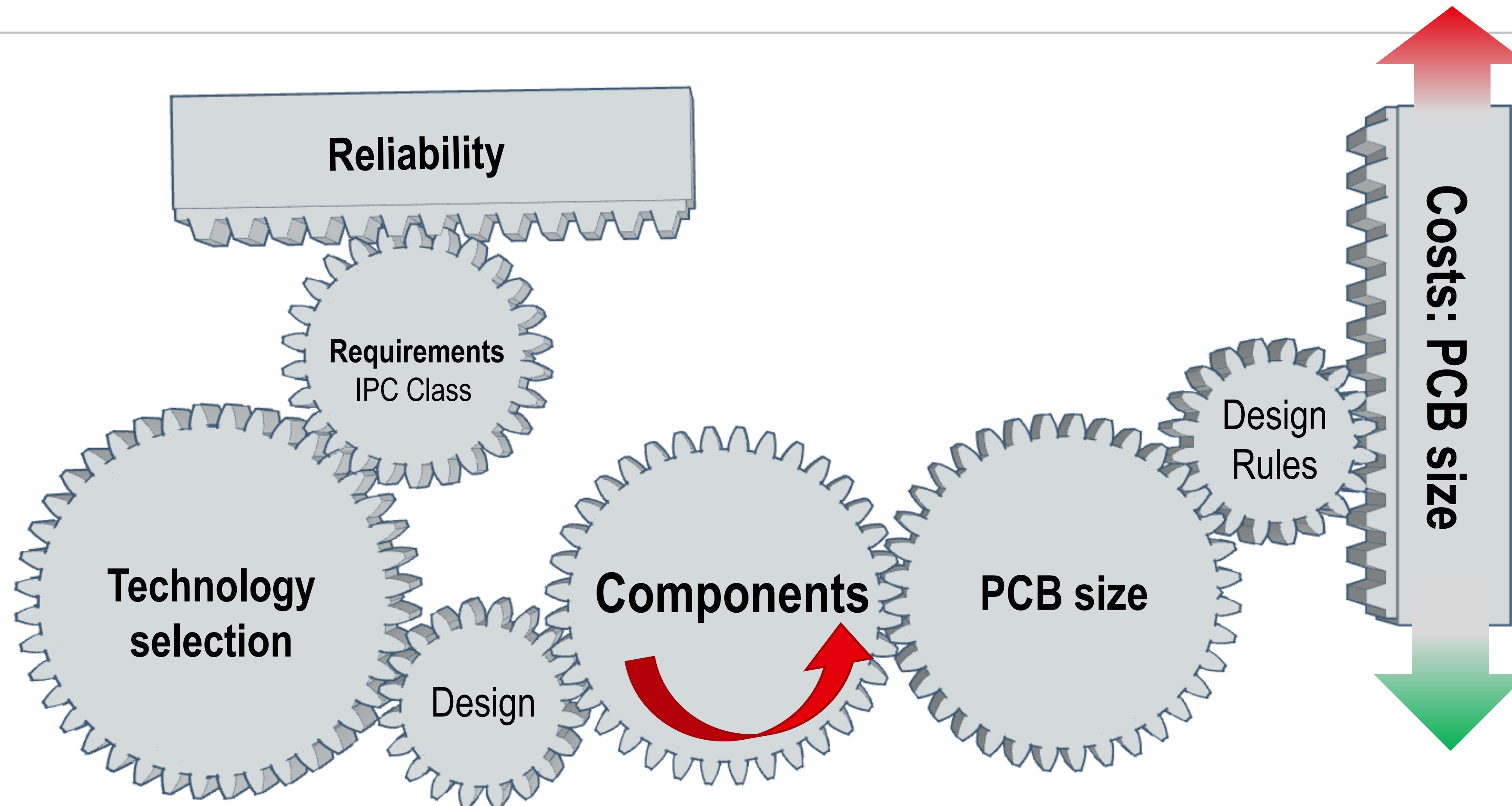
# CORRELATIONS



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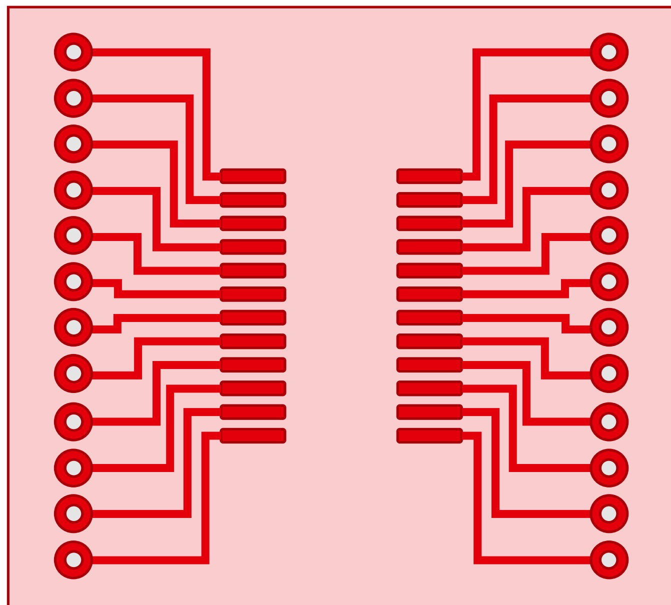
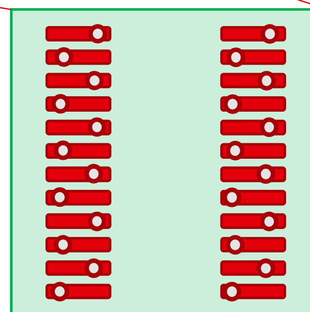
# MINIATURIZATION

## SSOP -24 Component

Plated Trough Hole



HDI - Microvia



# PCB SIZE

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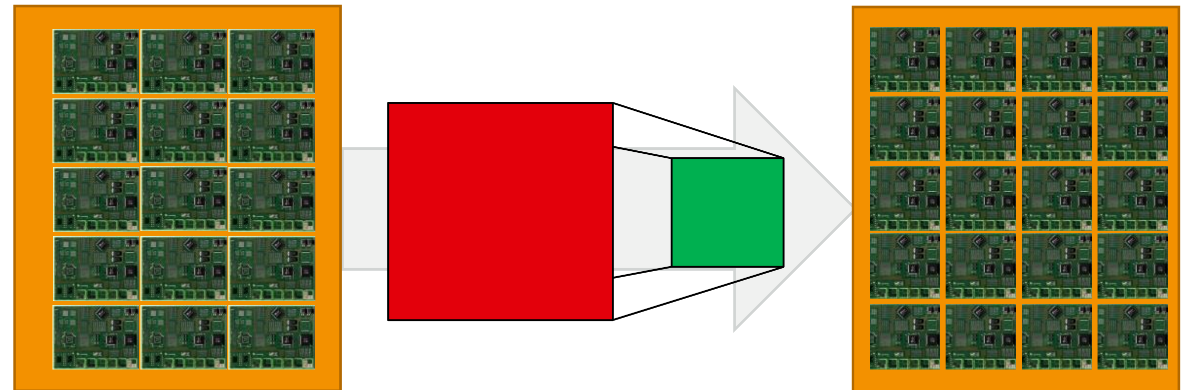
## PCB size

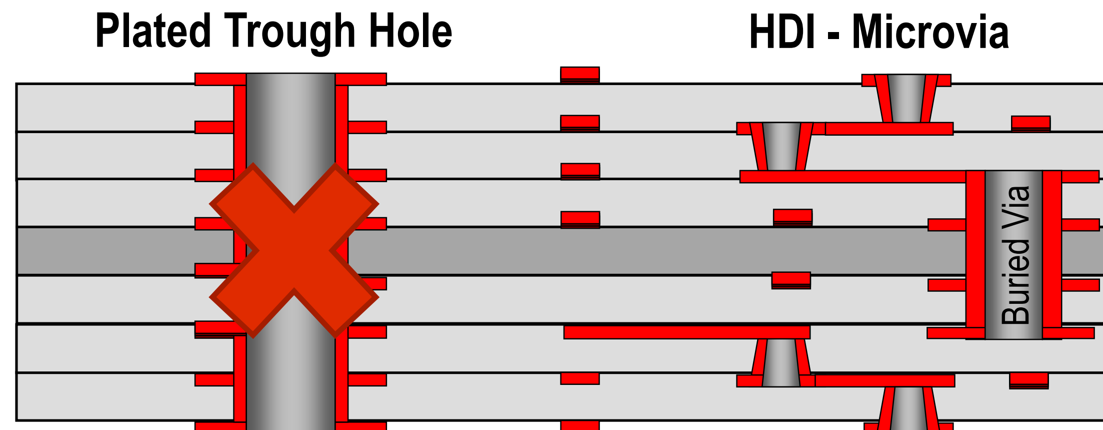
- Is decisive for the size of the device
- Could be essential for a successful product
- Decisively influences the production costs



## Reduction of the required routing area

⇨ HDI Technology with microvias + buried vias

⇨ Instead of through hole vias



# NUMBER OF LAYERS – PCB THICKNESS

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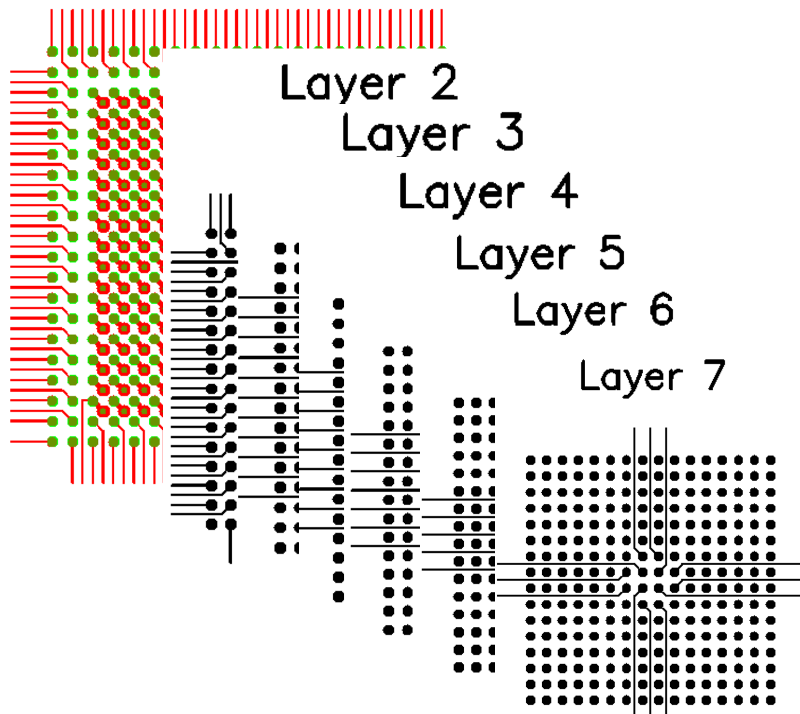
BGA – Pitch 0.80mm
20 x 20 rows

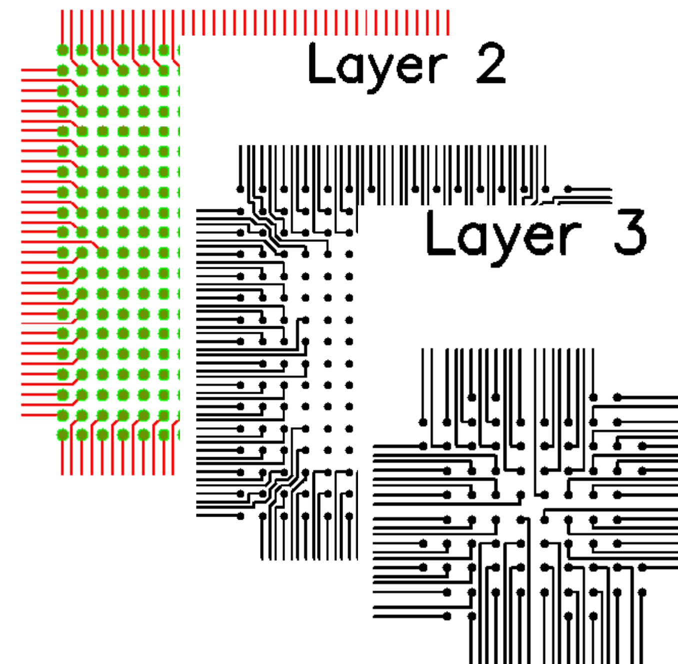
**Design Study**

## Plated Trough Hole




**How many signal layers are needed?**

## HDI - Microvia




**How many signal layers are needed?**

# DESIGN RULES VIAS – IPC SPECIFICATION

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## IPC-2221B Design Recommendation – "general requirements for lands with holes"

- Level A: General Design Producibility
  - Preferred
- Level B: Moderate Design Producibility
  - Standard
- Level C: Least Design Producibility
  - Reduced

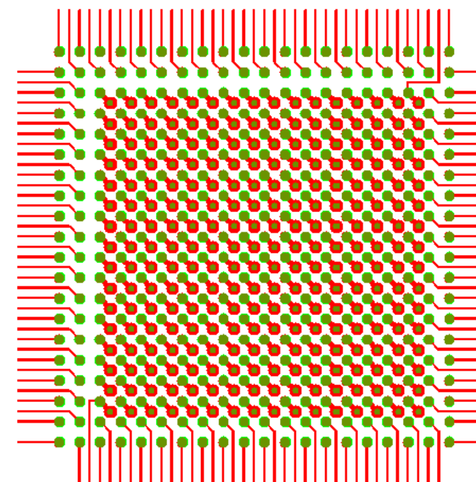
**Minimum via pad size ≈ *0.50mm***

**▶ BGA - Pitch < 0.8mm: HDI Microvia**

Table 9-1 Minimum Standard Fabrication Allowance for Interconnection Lands

| Level A | Level B | Level C |
|---|---|---|
| 0.4 mm [0.016 in] | 0.25 mm [0.0098 in] | 0.2 mm [0.0079 in] |

Note 1. For copper weights greater than 1oz/sq. ft., add 50 µm [1,968 µin] minimum to the fabrication allowance for each additional oz/sq. ft. of copper used.
Note 2. For more than 8 layers add 50 µm [1,968 µin].
Note 3. See IPC-2221 for definition of Levels A, B and C.
Note 4. Refer to IPC-2226 for allowances for HDI and micro-BGA substrates.
Note 5. For hole structures spanning multiple laminations, add 0.05 mm [0.002 in].



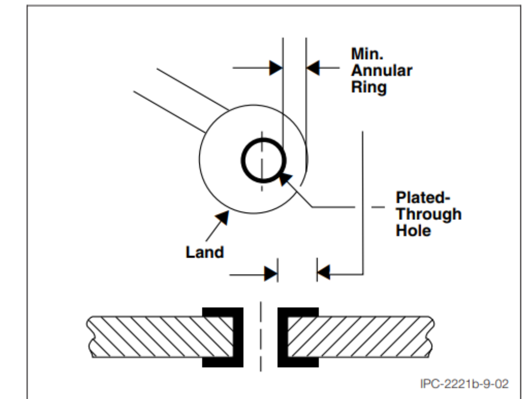



Figure 9-2 External Annular Ring

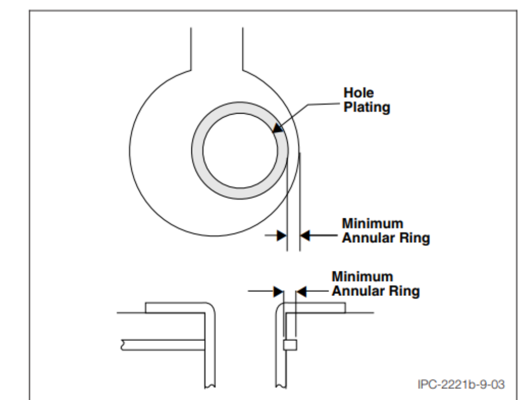



Figure 9-3 Internal Annular Ring

# DESIGN GUIDE – TECHNOLOGY SELECTION

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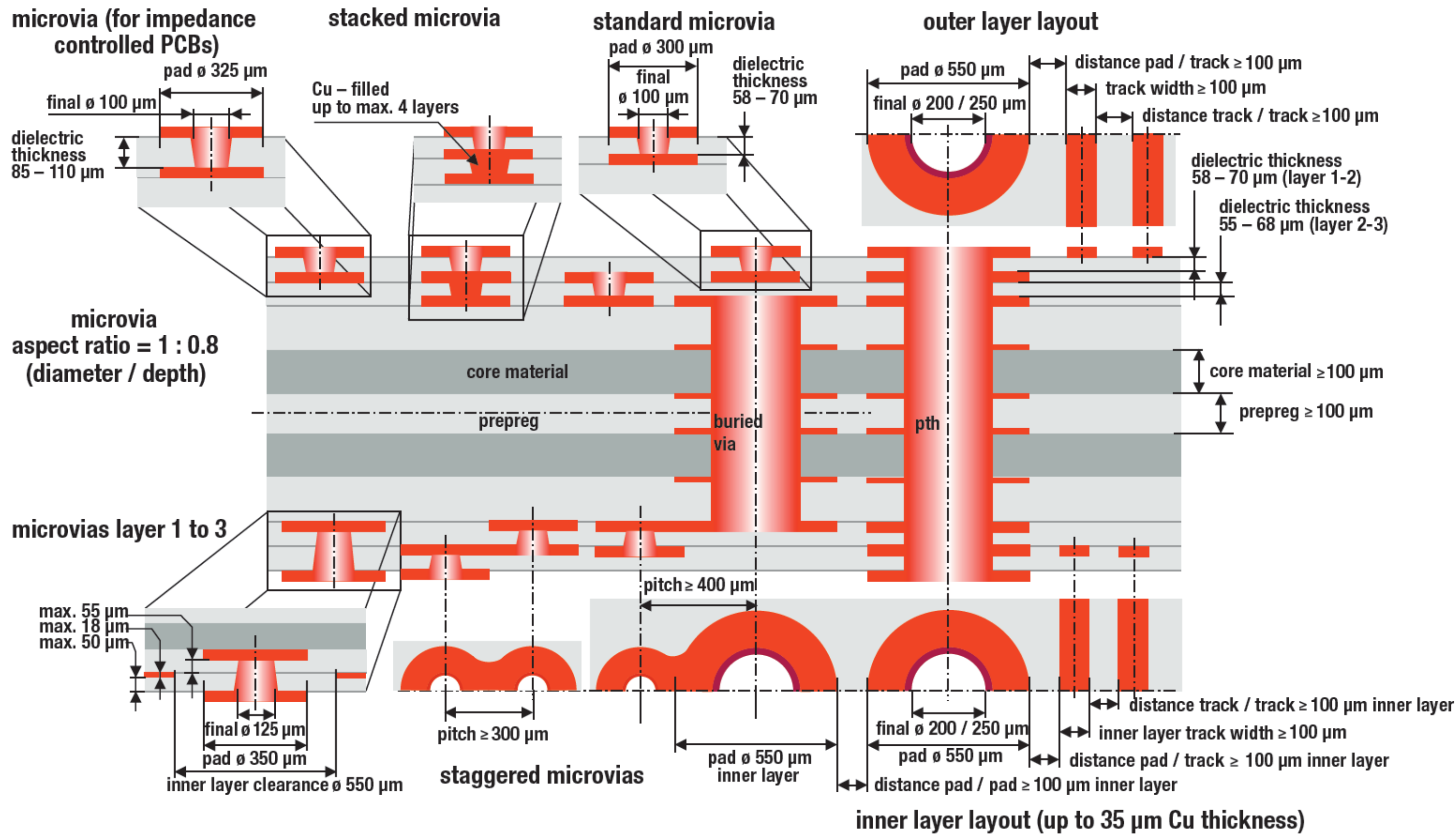


www.we-online.de/microvia

# DESIGN RULES – EXAMPLE 0.50 MM PITCH BGA

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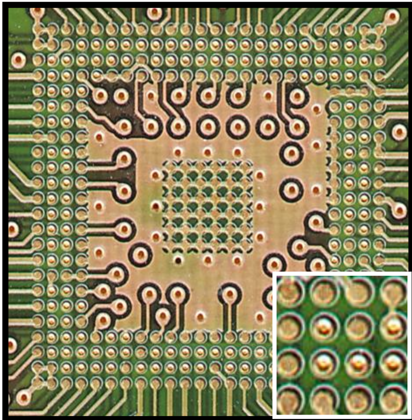
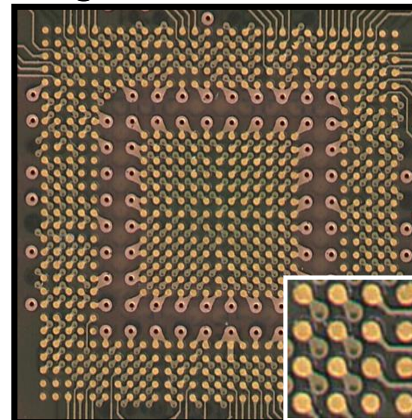
**Via in Pad** Var.1



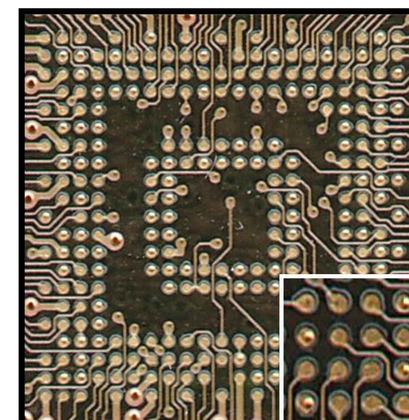
Advantage: large solder pads

**Dog Bone** Var.2

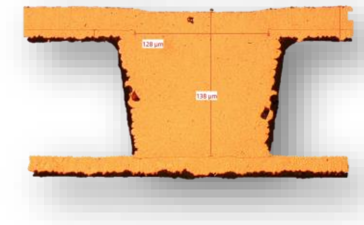


Advantage: filling not necessary

**Via in Pad** Var.3



Advantage: one more routing layer



| Design Rules | Var. 1 | Var. 2 | Var. 3 |
|---|---|---|---|
| BGA solder pad | 300 - 330 µm | 240 / 250 µm | 275 µm |
| Solder mask clearance | 50 µm | 40 µm | 35 µm |
| Microvia pad outer layer | ≥ 300 µm | 275 µm | 275 µm |
| Microvia pad inner layer | 275 µm | 275 µm | 275 µm |
| Track width / spacing outer layer | ≥ 100 µm | 80 - 90 µm | 75 µm |
| Track width / spacing inner layer | 75 µm | 75 µm | 75 µm |

- 75 µm fine line structures
  + copper thickness
  approx. 25 µm max.
- Cu Filling for microvias optional (with via in pad / var.1 and 3)

# TECHNOLOGY SELECTION – STACK-UP

Costs

200 %

100 %

Single lamination

100 %

1 + 6 + 1

Double lamination

115 %

Laser drilling L1 to L3

2 + 4 + 2

120 %

Internal microvias (staggered)

2 + 4 + 2

142 %

Buried vias mechanically drilled

1 + 6b + 1

150 %

Additional internal microvias

2 + 4(6b) + 2

Triple lamination

175 %

2 + 4b + 2

Complexity / Number of process steps

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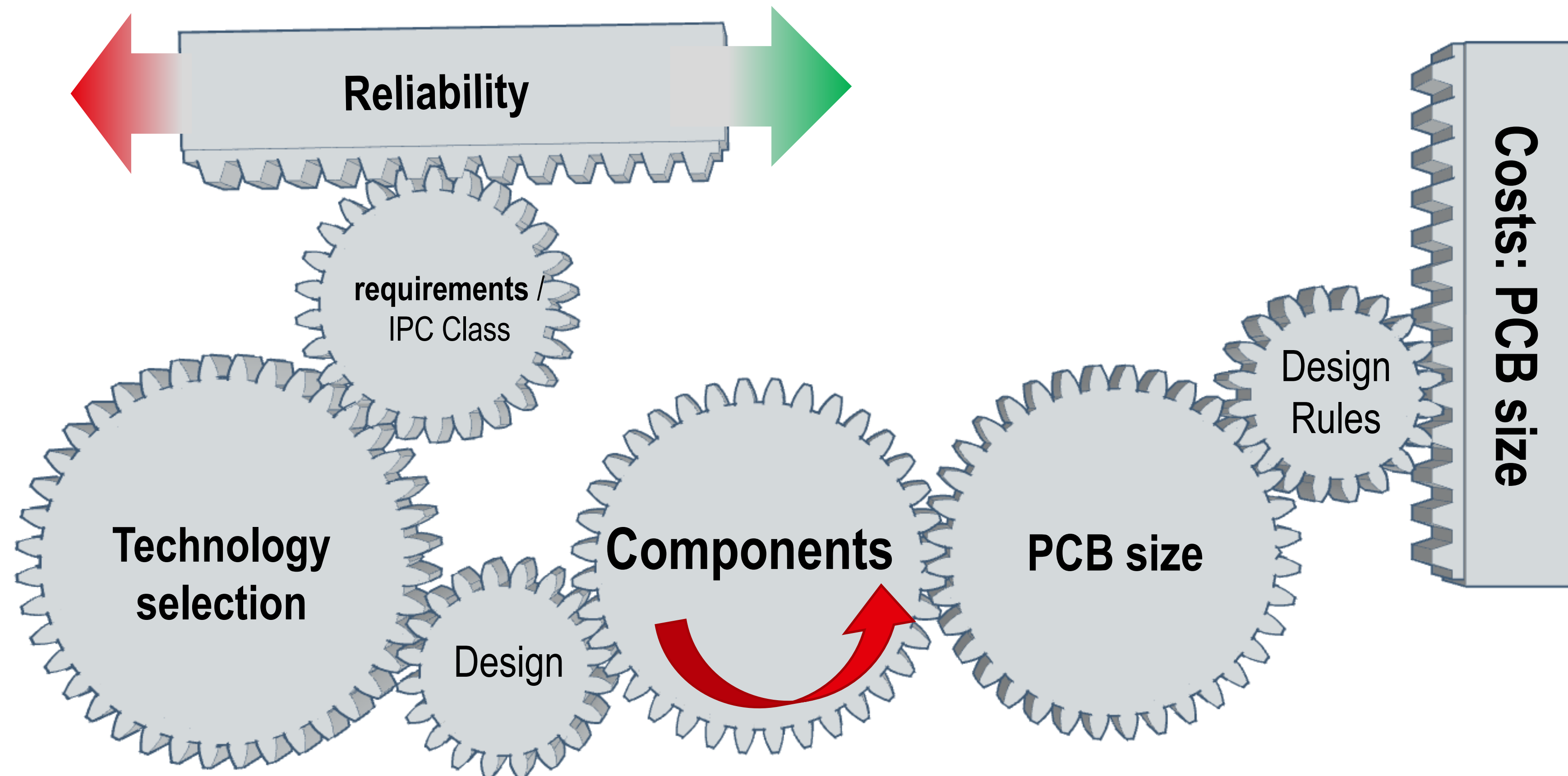
# CORRELATIONS



# RELIABILITY - INTRODUCTION

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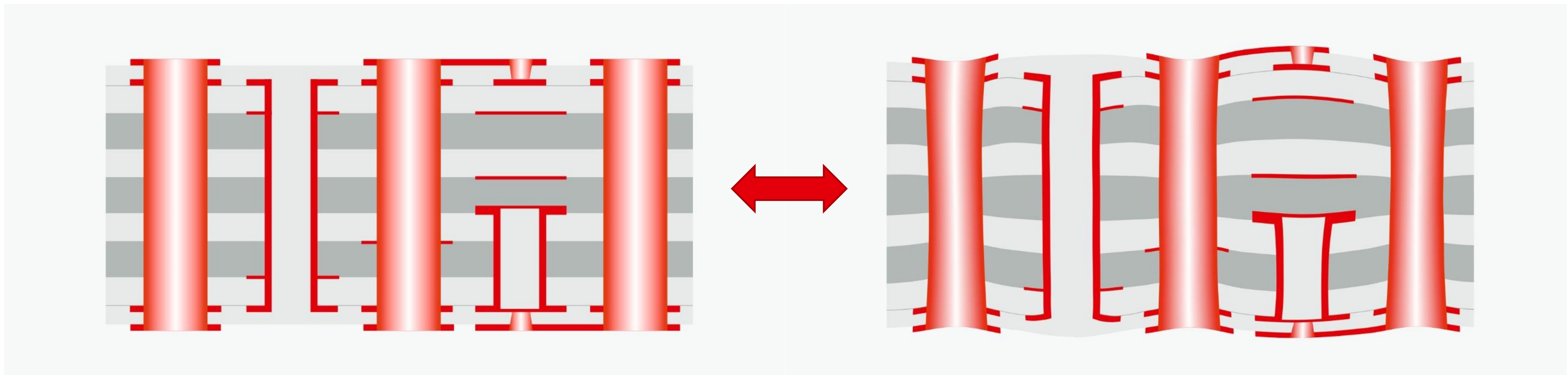
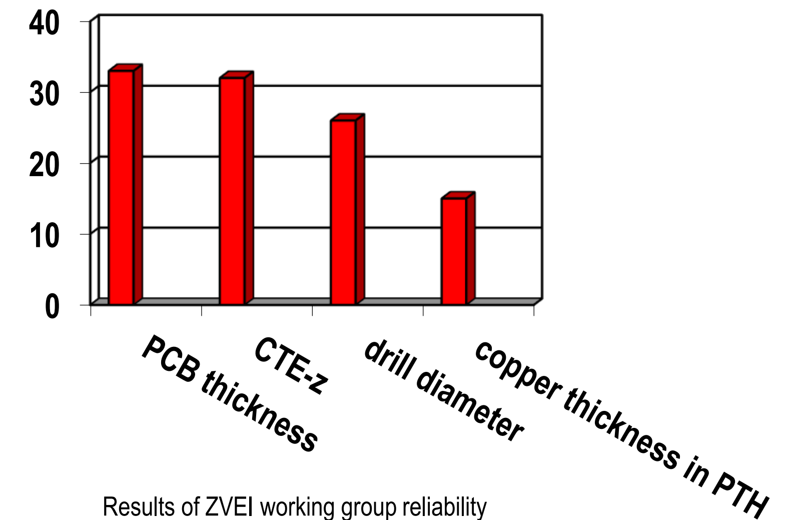
- **What does Reliability means for PCB ?**
  - Ensuring the electrical functions during the entire intended service life.
  - Even flawless circuit boards fail at some point if they are exposed to temperature fluctuations.



# RELIABILITY

## Via Structures

- **Parameters with the most influence to the reliability for plated through holes**
  - Coefficient of thermal expansion ($CTE_Z$) of the used materials
    - Diffenrent $CTE_Z$ values
    - Overall thickness of the PCB!
  - Cross sectional area of the thorugh hole
    - Drill diameter of the hole
    - Copper thickness inside the hole
      Be aware: not allways is a higher thickness better for reliability
  - Conditions in the end application



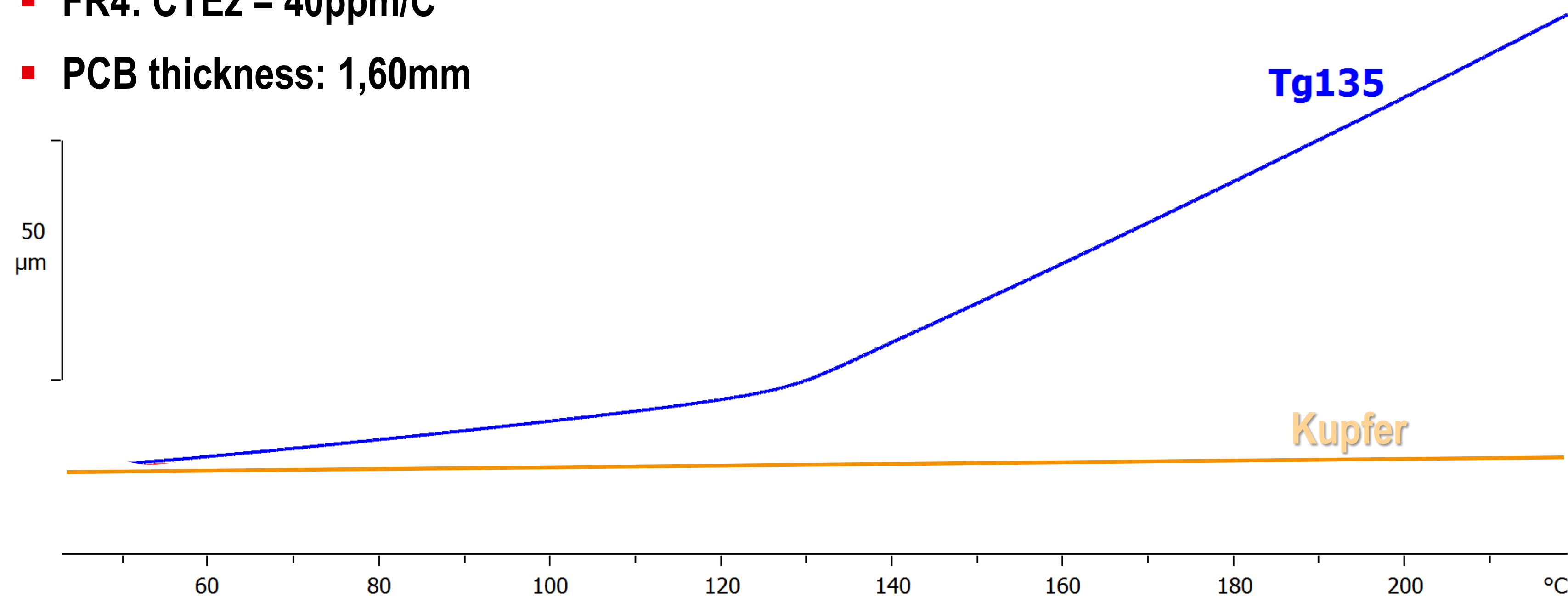

Results of ZVEI working group reliability

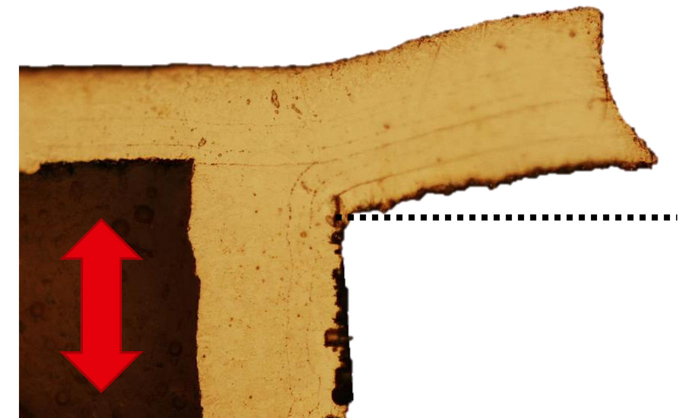
# RELIABILITY

## Coefficient of thermal expansion

**Comparision of the coefficient of thermal expansion in Z-axis**

- **FR4: CTEz = 40ppm/C°**
- **PCB thickness: 1,60mm**



# RELIABILITY – PCB THICKNESS

- **The influence of the printed circuit board thickness is enormous :**

  With only **~ 20 % reduction** of the thickness the reliability can increase up to **3x times**!

Wahrscheinlichkeitsnetz für 2,2mm; 2,0mm; 1,8mm
Weibull - 95%-KI
Vollständige Daten - ML-Schätzwerte

Prozent: 1, 2, 3, 5, 10, 20, 30, 40, 50, 60, 70, 80, 90, 99
Daten: 10, 100, 1000

Variable
2,2mm
2,0mm
1,8mm

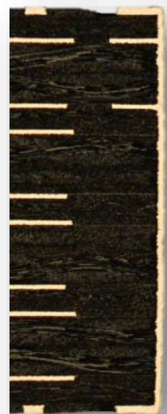
Statistiktabelle

| Form | Skala | AD* | A | Z |
|---|---|---|---|---|
| 3,03964 | 59,973 | 1,080 | 15 | 0 |
| 3,34501 | 86,050 | 1,091 | 15 | 0 |
| 2,58459 | 185,240 | 1,077 | 20 | 0 |

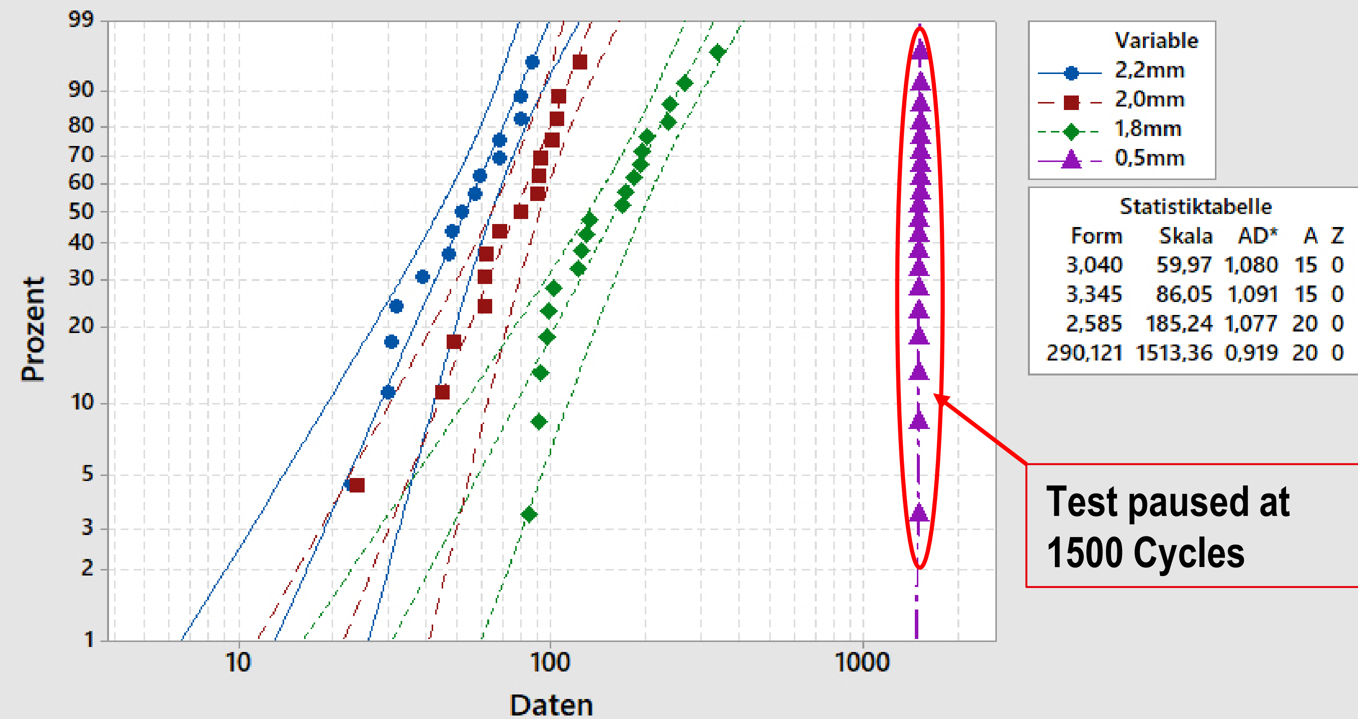
# RELIABILITY
## PCB thickness

- **The influence of the printed circuit board thickness is enormous :**

0,5mm



1,8mm




Test paused at 1500 Cycles

# INTERCONNECT STRESS TEST (IST)

## Procedure and options

- **Coupon design based on your PCB**
  - Material, stack-up and design
  - Via types, drill hole diameters and distances
  - Solder surface
- **Determination of test scope and test parameters in coordination with you**
  - Number of IST test cycles
  - Soldering simulation
  - Test temperature
- **Test preparation and execution (8 test coupons at the same time)**
- **IST Test Report**
  - Microsection analysis of the faults (first, middle and last failure)
  - Statistical analysis
  - Thermomechanical analysis of the stack-up
  - Design recommendations (optional)

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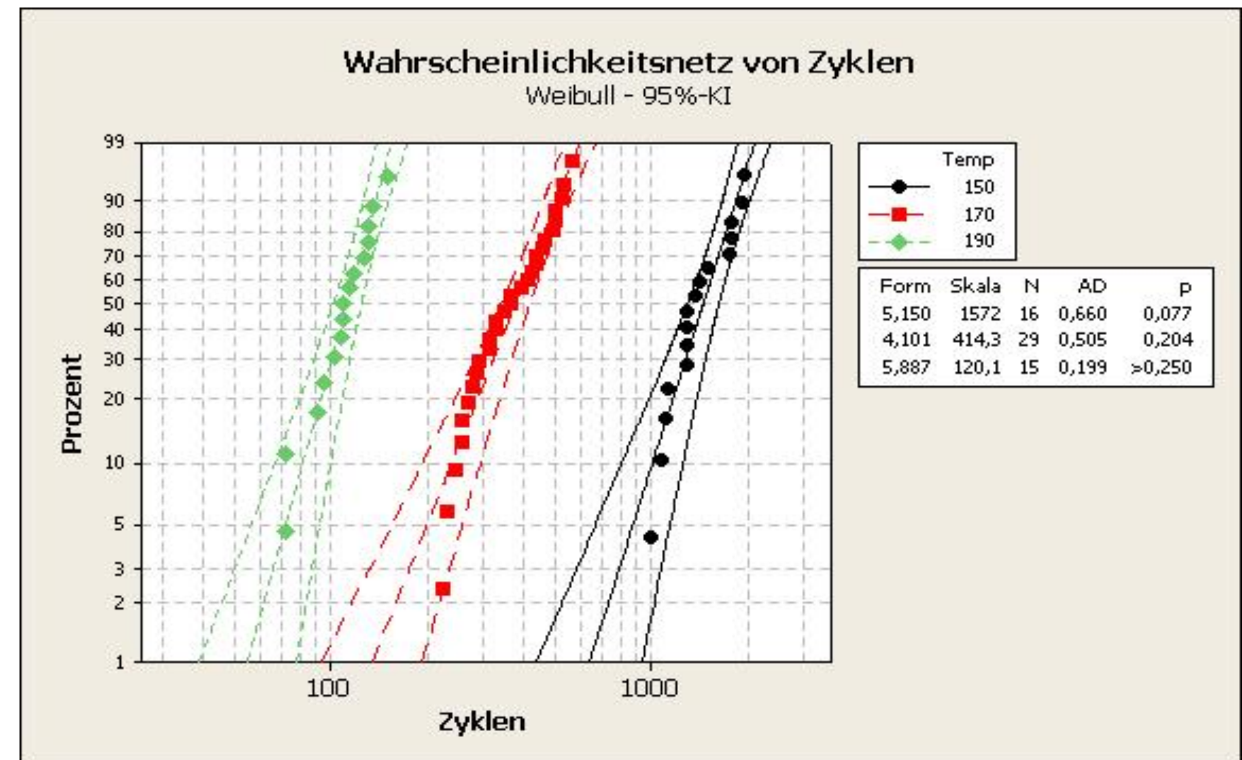
# RELIABILITY - VIA TYPES

## Investigation of plated through hole structures at different test temperatures



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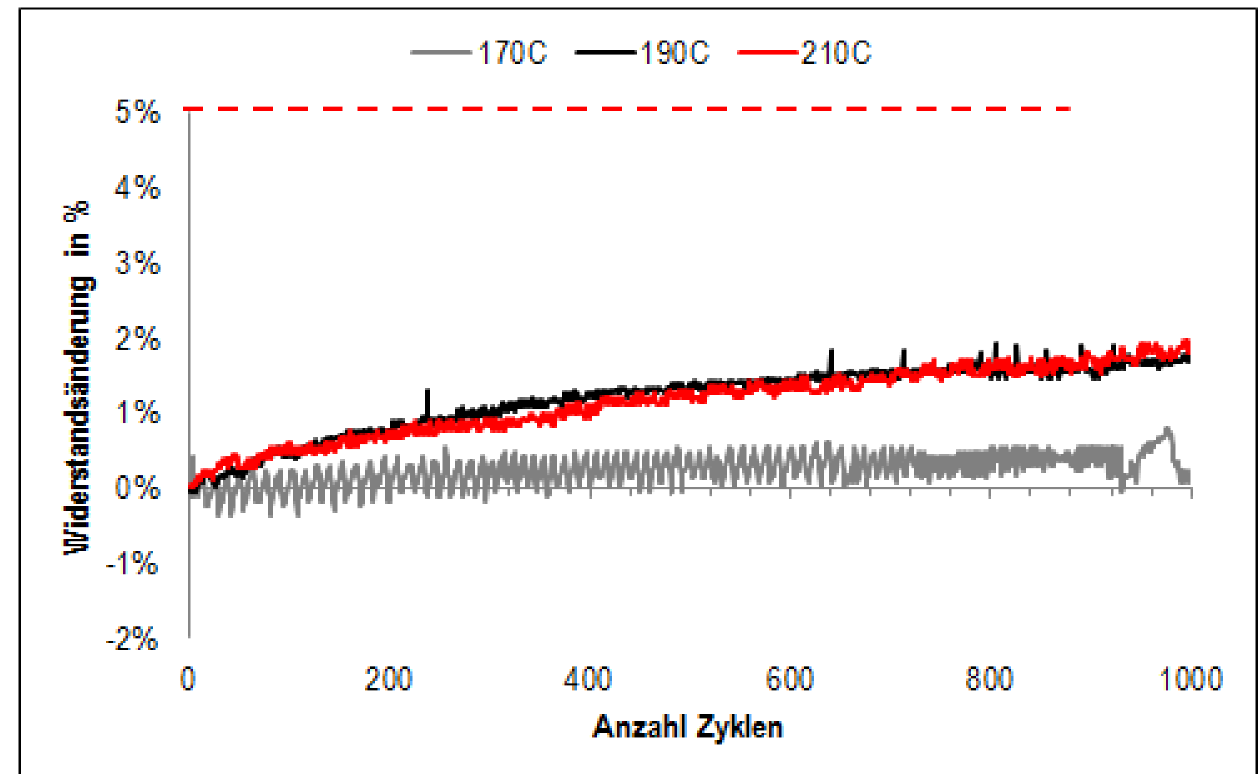
# RELIABILITY - VIA TYPES – IST MICROVIAS

## Investigation of microvia structures at different test temperatures

No defects after 1000 cycles



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# RELIABILITY – STACKED VIAS

**IPC-2226A** Design Standard for HDI Printed Boards

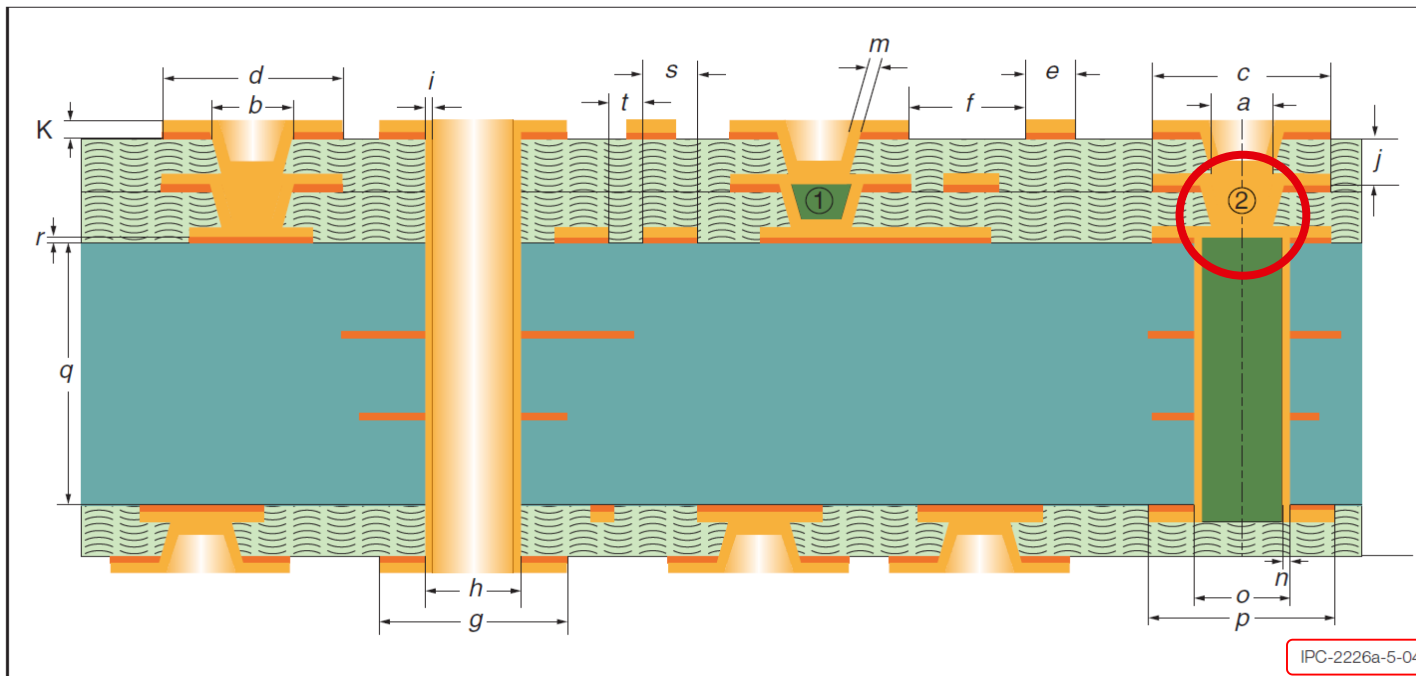



**Figure 5-4 Type III HDI Construction with Stacked Microvias**

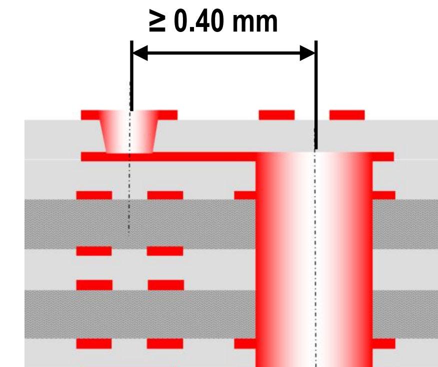
(**Caution:** Unbalanced constructions as shown above may result in excessive bow and twist.)

**Note 1:** Stacking not recommended for resin or conductive/non-conductive filled microvias.

**Note 2:** Stacking not recommended over resin or conductive/non-conductive filled vias due to potential for reduced reliability. The use of staggered structures instead is recommended.

**Caution:** HDI design with microvias stacked on buried vias is not recommended.

**Recommendation by ZVEI Working Group Quality and Würth Elektronik**




**Existing designs should also be changed as soon as possible!**

**WE will support you in this!**

# RELIABILITY – STACKED VIAS

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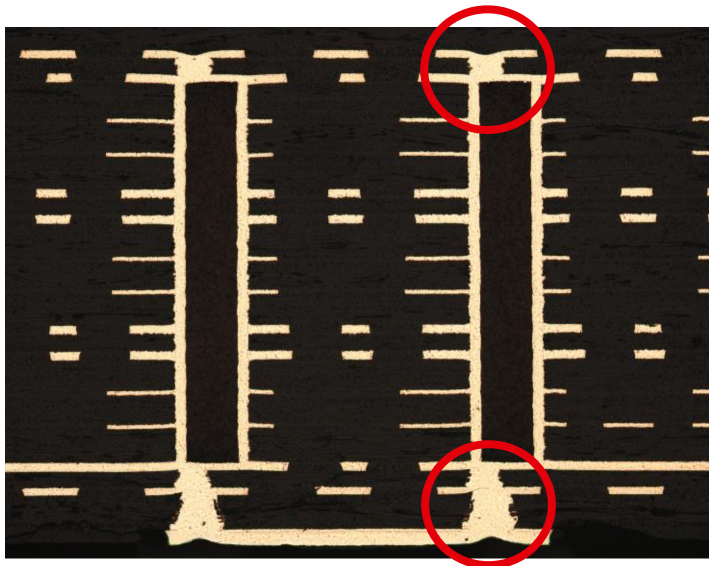

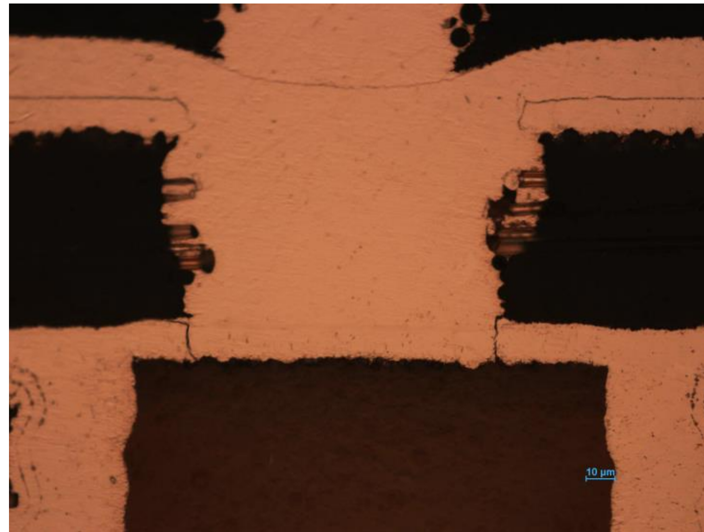


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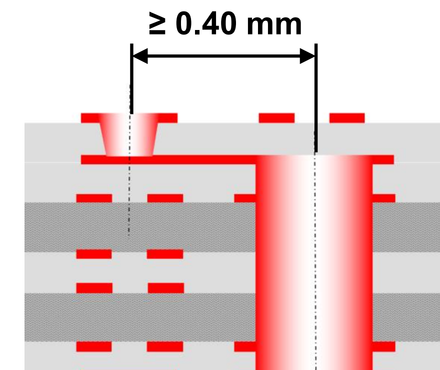


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# CORRELATIONS

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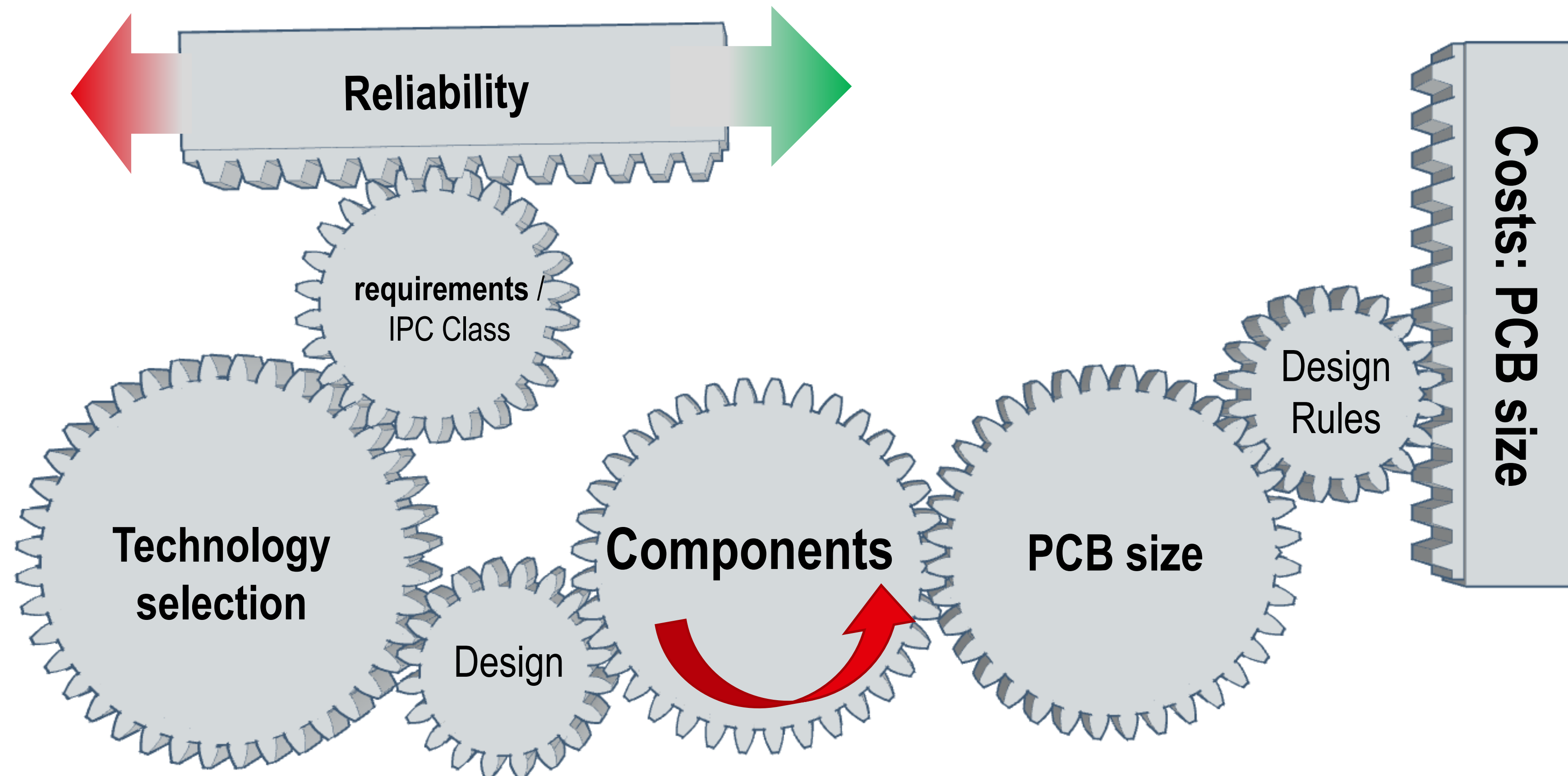

# MANY THANKS FOR YOUR ATTENTION!

What kind of
application
do you have?

How can WE
support you?

# QUESTIONS?