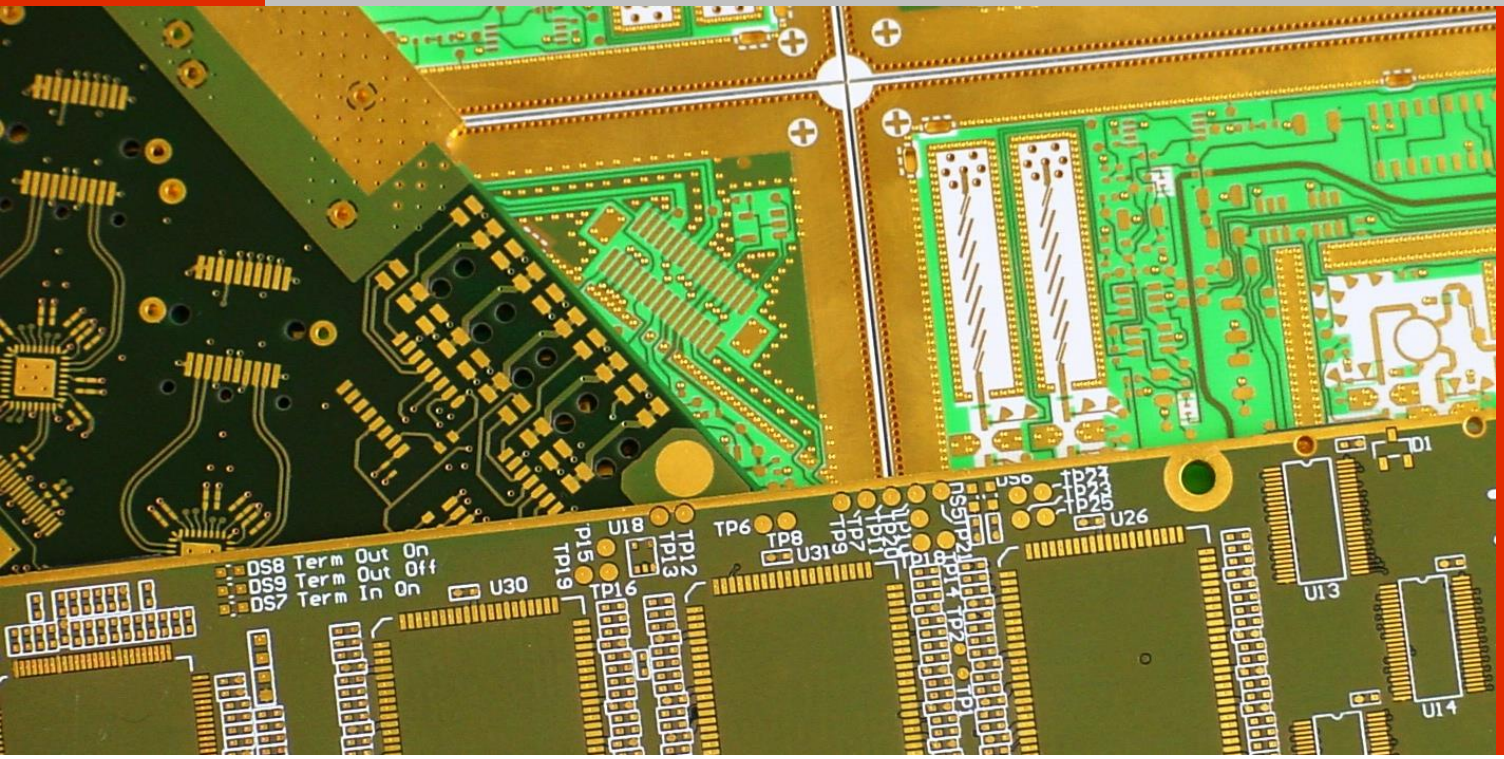
Webinar 2013: Improved signal integrity through impedance matched circuit boards

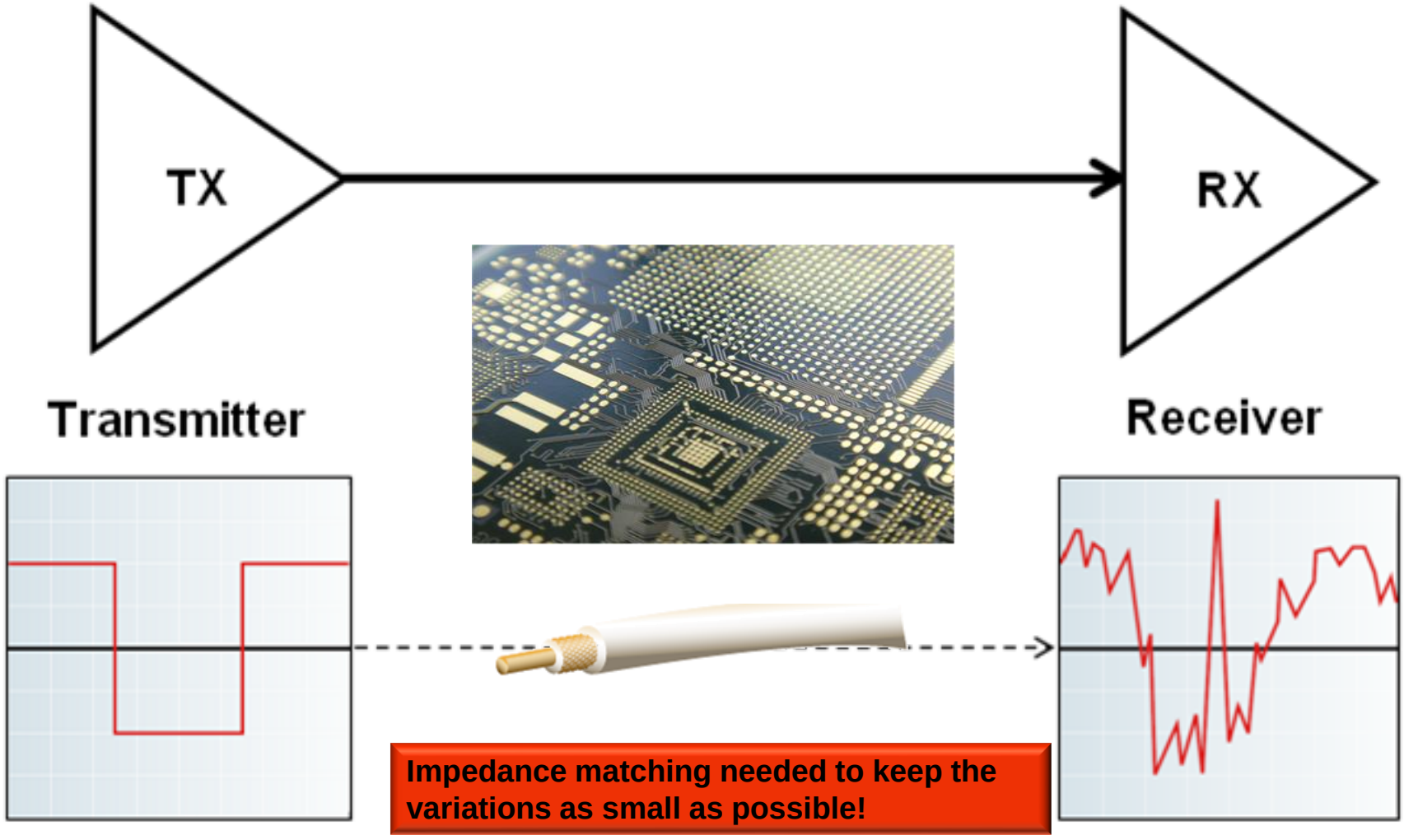
Würth Elektronik Circuit Board Technology



Agenda

- S Impedance and the circuit board
- I Material aspects and parameters
- G Impedance calculation
- N Layer stack-ups
- A Impedance and HDI (EMC)
- L High frequency and mid-performance materials

PCB and impedance



PCB and impedance

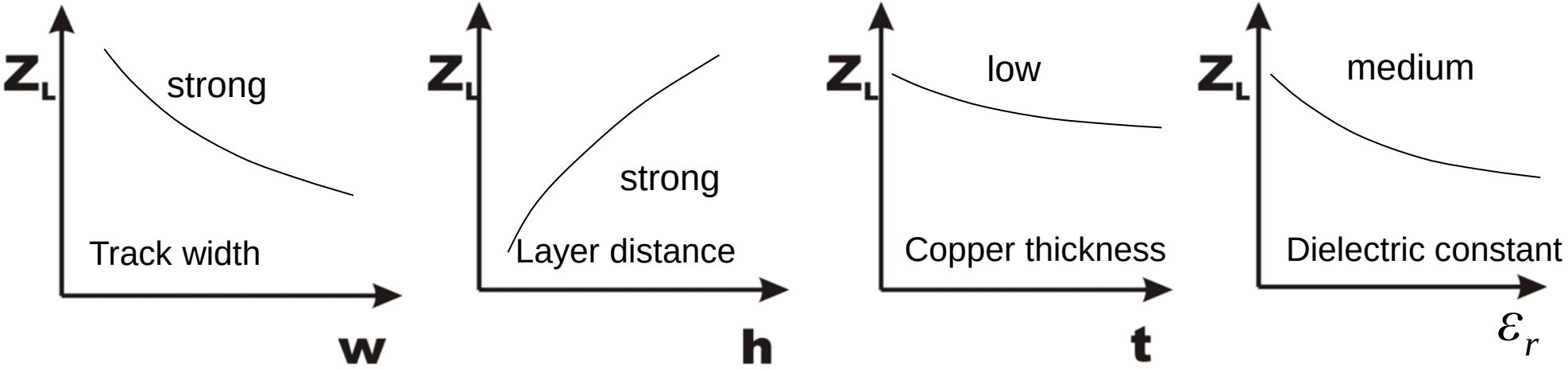
PCB has an ohmic, capacitive and inductive proportion

not an optimal tranfer medium between transmitter and receiver

parameters that influence the signal on a PCB

- Length of conductor
- Raw material loss factor and permittivity
- Reflection due to the PTHs
- Impedance matching
- Crosstalk between conductors
- Noise interference from external sources (EMC shielding)

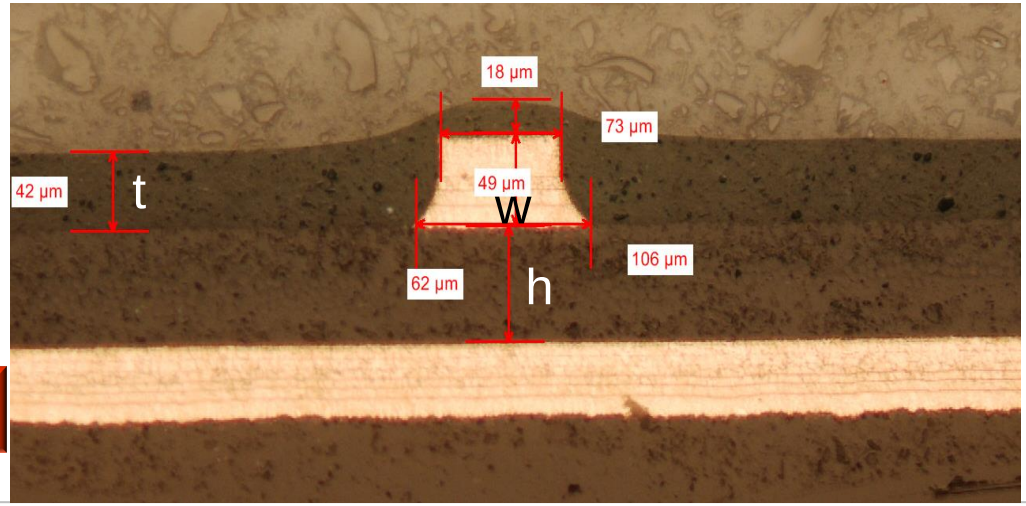
Important parameters



w+h = layouter / developer
+ PCB supplier

t = galvanic process, base copper

ε_r = base material

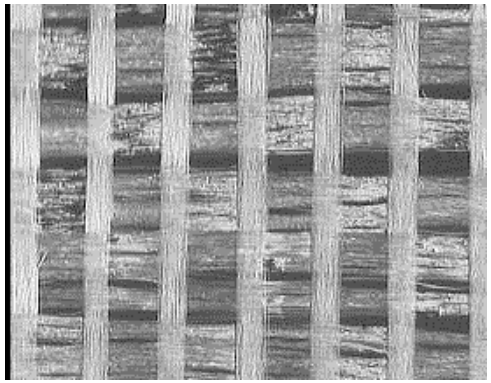


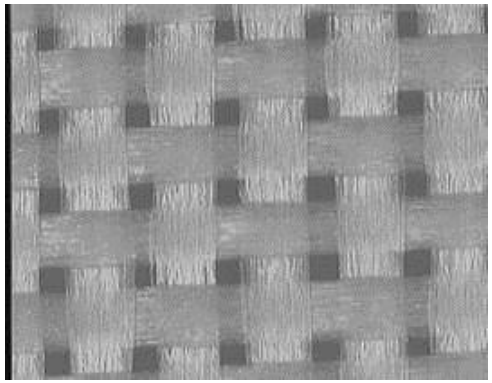
WE offers: advanced partnership!

Material parameters Epsilon R

FR4 Pre-preg **106**

Thickness 50 µm
ε_r = 2,8 – 3,7
Resin content ~70%



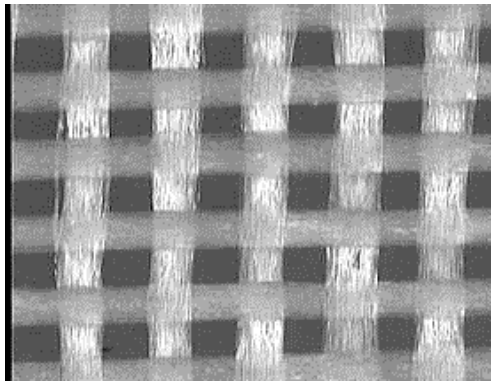


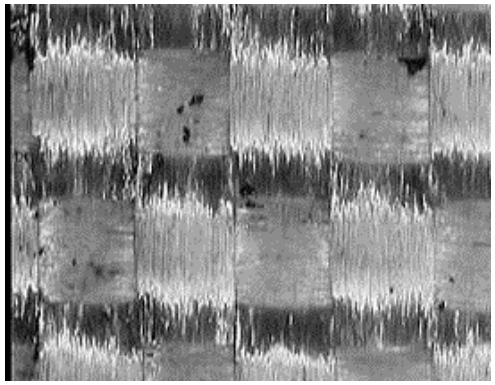
FR4 Pre-preg **2116**

Thickness 90 – 110 µm
ε_r = 3,6 – 3,8
Resin content ~50%

FR4 Pre-preg **1080**

Thickness 60 - 70 µm
ε_r = 3,2 – 3,7
Resin content ~60%





FR4 Pre-preg **7628**

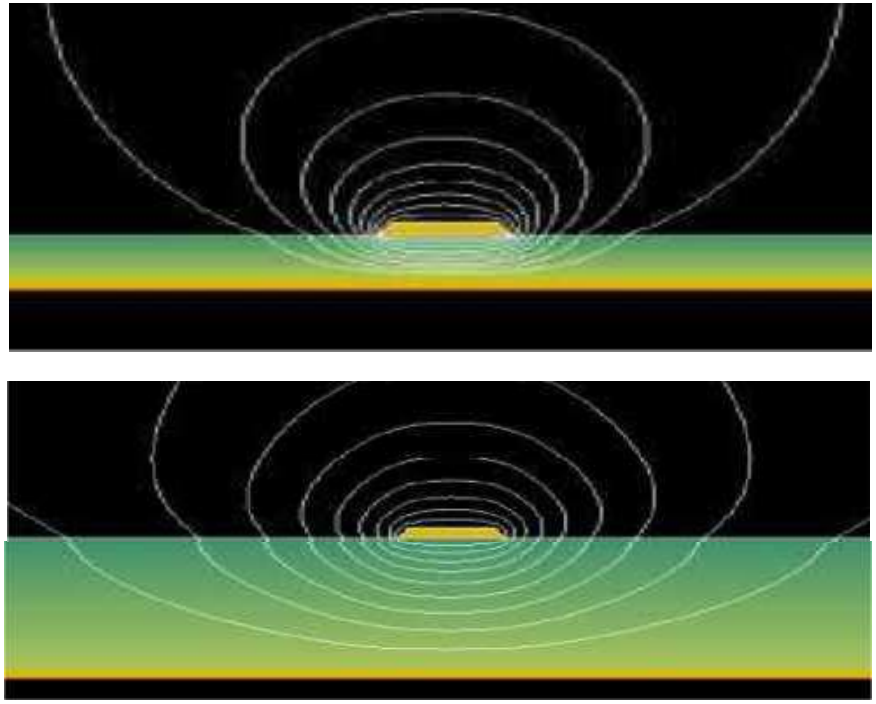
Thickness 170 – 190 µm
ε_r = 4,1 – 4,6
Resin content ~45%

glass εr ~6,1 / resin εr ~3,2

Cores are laminated pre-pregs

Epsilon R

dielectric losses



Influence:
- layer distance
- frequency ….

Influence on characteristic wave impedance

ε_r values in relation to the layer distance FR4

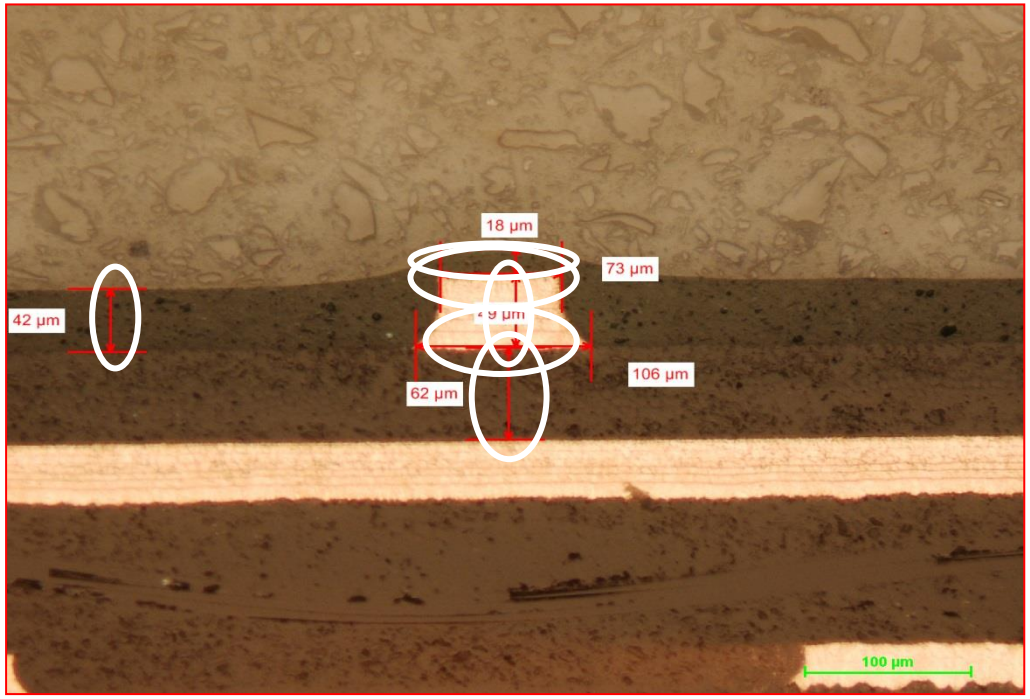
(lossy ε_r)

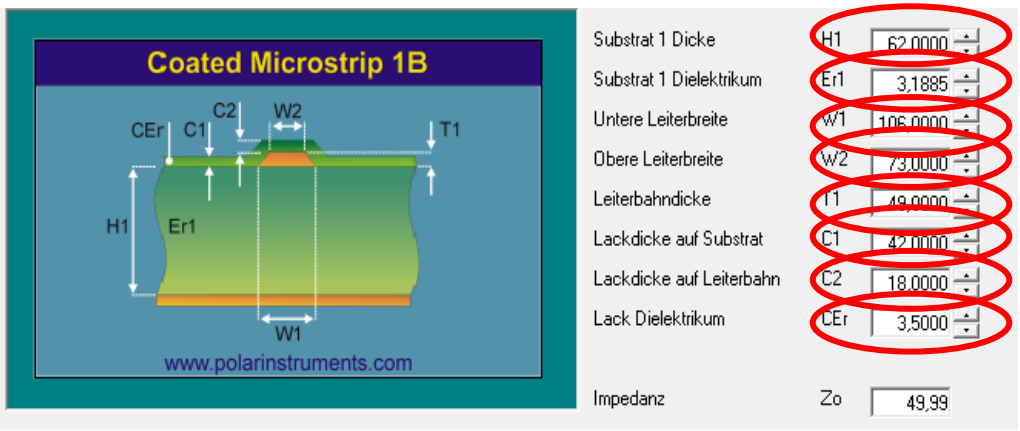
Pre-preg	1080	2 x 1080	3 x 1080	2116	2 x 2116	3 x 2116
Tg 135	3.2	3.5	3.6	3.6	3.9	4.7
Tg 150 hf	3.5	3.7	3.9	3.8	4.3	4.6

Cores	60 µm	100 µm	150 µm	250 µm	510 µm	710 µm
Tg 135	3.2	3.5	3.6	3.6	3.9	4.7
Tg 150 hf	3.5	3.7	3.9	3.8	4.3	4.6

effective ε_r

determination of $\varepsilon_{r\ effectiv}$





Calculation of the Er value according to microsection picture with the help of Polar

H1	**layer distance**
W1	**lower track width**
W2	**upper track width**
T1	**copper thickness**
C1	**solder resist on substrate (FR4)**
C2	**solder resist on track**
CEr	**Er solder resist (supplier)**

Er **dielectric constant**

Layer distances

layout against plane or foil

Pre-preg	17 µm copper	35 µm copper
1 x 1080	65 µm	60 µm
2 x 1080	134 µm	128 µm

layout against layout

Pre-preg	17 µm copper	35 µm copper
2 x 1080	128 µm	120 µm

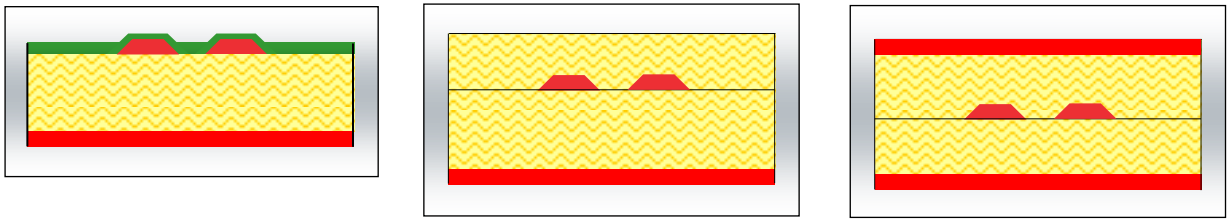
plane against plane or foil

Pre-preg	17 µm copper	35 µm copper
1 x 1080	70 µm	68 µm
2 x 1080	140 µm	136 µm

Models

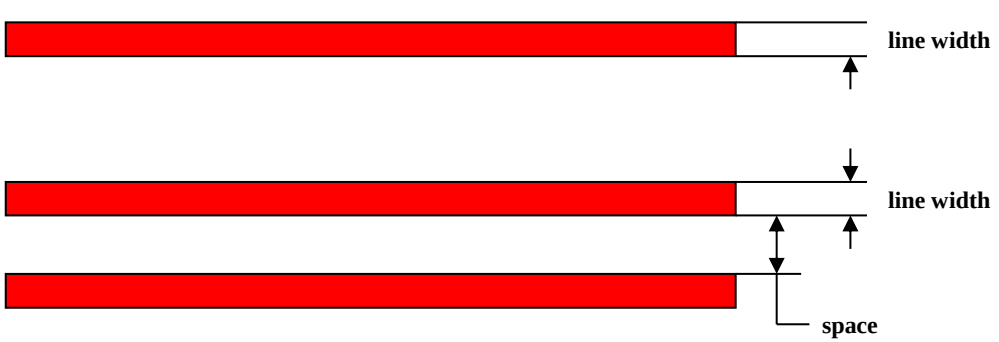
layer / track configuration

layer configuration:



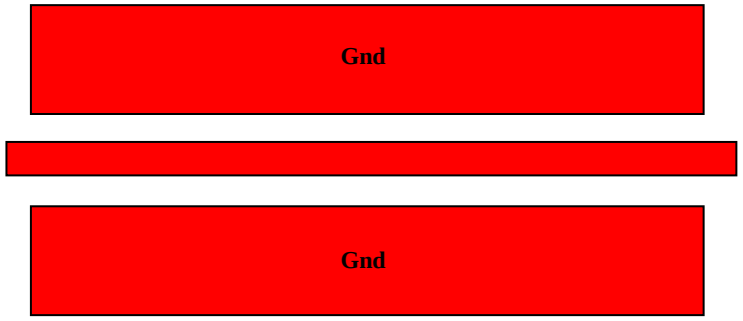
Surface Microstrip | Embedded Microstrip | Stripline

track configuration:



Single

Differential



Coplanar

Which parameters have the biggest influence on the impedance of a track?

Parameters for impedance calculations

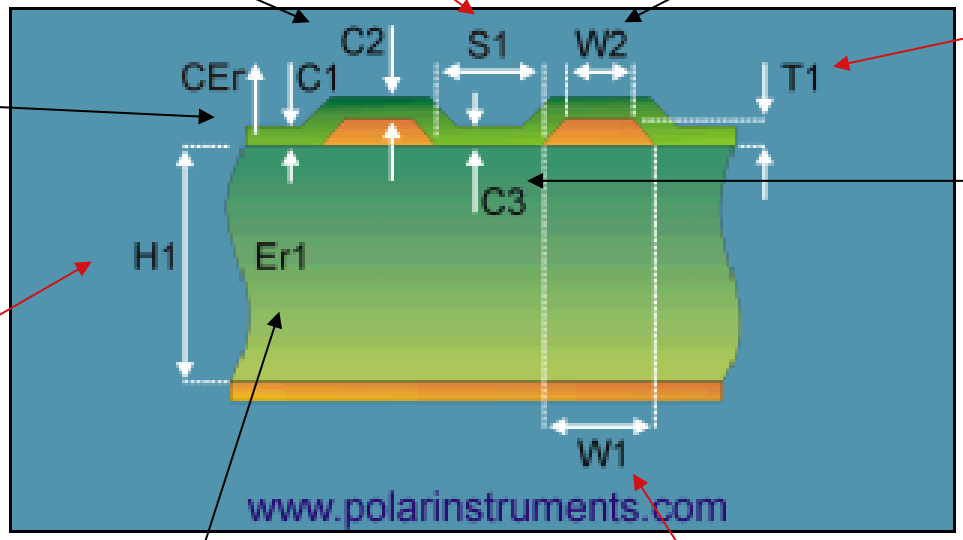
C2
thickness solder resist over track [15 µm]

S1
gap layout

W2
upper track width (head)

T1
copper thickness

ε_r
dielectric constant solder resist [typ. 3,5]

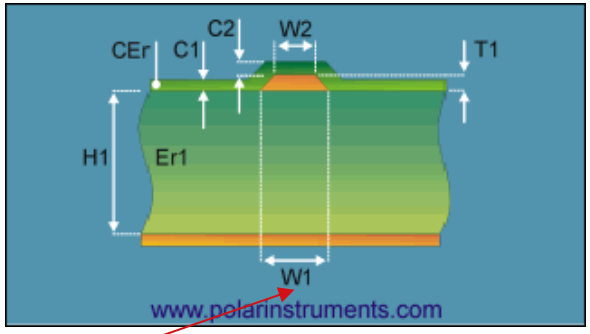


C1=C3
thickness solder resist over FR4 [42 µm]

H1
layer distance Signal > Reference

ε_r
dielectric constant FR4

W1
lower track width (foot) = layout



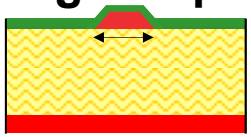
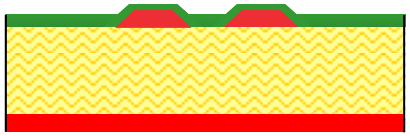
Service “impedance defined stack-ups“
Information required:

- **type of stack-up: Standard <>HDI / via types**
- **Number of layers**
- **PCB – thickness**
- **Copper thickness** (especially inner layers)
- **layer order: position of signal layer plus corresponding reference layers**
- **Number of signal layers and number of reference layers** (Gnd, Power, VCC)
- **Impedance requirements** (Single e.g. 50 Ohm) (Differential e.g. 90 und 100 Ohm)
- ***Which track widths and gaps are preferred or possible?***

Impedance values for different pre-pregs

Microstrip Outer Layers

Pre-pregs: TG 150°, filled, halogen free

Prepreg (each one ply)	**1080**	**2113**	**2116**
Layer spacing above plane layer (pressed thickness , 1 oz copper L2)	**68 µm** $\varepsilon_{r\ effective}$ 3.5	**92 µm** $\varepsilon_{r\ effective}$ 3.6	**108 µm** $\varepsilon_{r\ effective}$ 3.8
Track Width 50 Ω Single Impedance 	**109 µm** (with $\varepsilon_{r\ 4.2}$: 94 µm)	**154 µm** (with $\varepsilon_{r\ 4.2}$: 136 µm)	**179 µm** (with $\varepsilon_{r\ 4.2}$: 165 µm)
Track Width Track Separation 100 Ω diff. Impedance 	**100 µm** **305 µm**	**100 µm** **137 µm**	**100 µm** **122 µm**

Example stack-up

LAGENAUFBAU

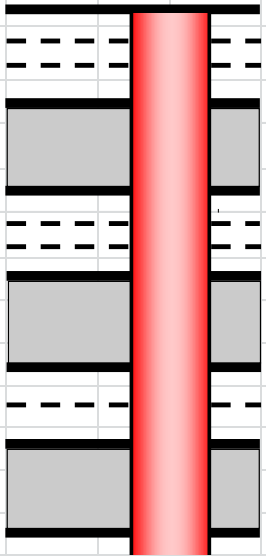
12 - Lagen

WE-Artikel Nr.: ML12

Kunde:

CBT SH

LAGENBEZEICHNUNG		AUFBAU			BASIS-Material	CU	PREPREG ANZAHL/TYP	Dielektrizitäts-konstante	ENDDICKE	KUNDEN-FORDERUNG
KUNDE	WE							[εr]	[µm]	[µm]
	TOP/VS	S1	S3		Foil	17,5 µm	1)		16	
							1 x 1080			
							1 x 2116	4.25	175	
	2	REF				35 µm			33	
					0,100 mm			3.8	100	
	3	REF				35 µm			33	
							2 x 1080	3.7	134	
	4	S2				17,5 µm			16	
					0,100 mm			3.8	100	
	5	REF	REF			17,5 µm			16	
							1 x 2113	3.6	87	
	6	S				17,5 µm			16	
					0,100 mm			3.8	100	
	7	S				17,5 µm			16	



Impedanzberechnung:

S1 Zdiff 100 Ohm @ 180 / 185 / 180 µm

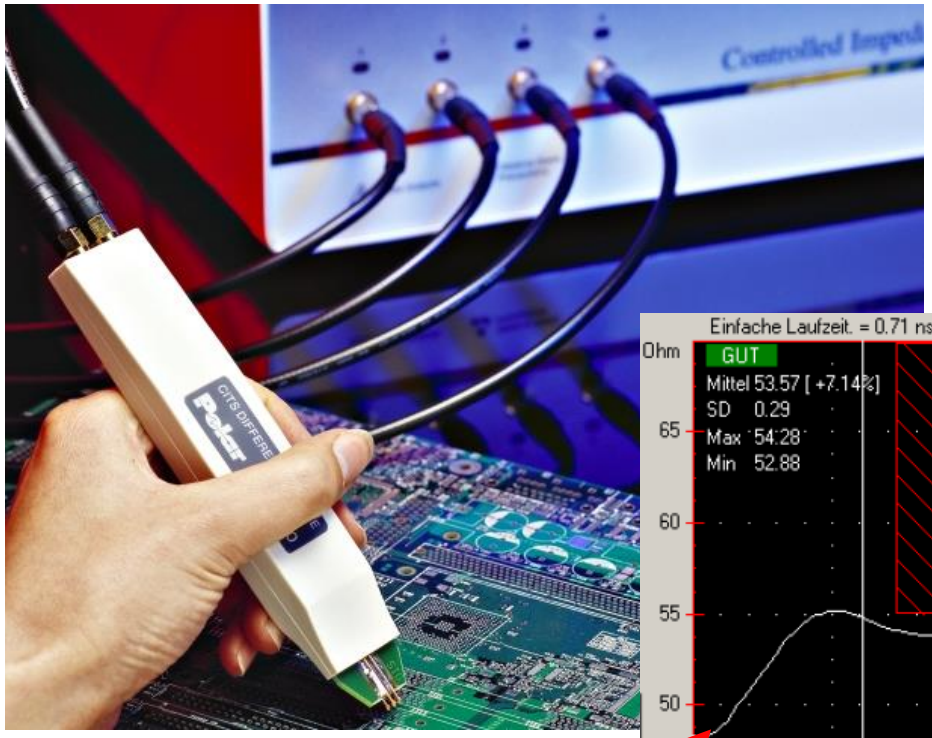
S1 Zdiff 110 Ohm @ 170 / 270 / 170 µm

S2 Zdiff 100 Ohm @ 94 / 186 / 94 µm

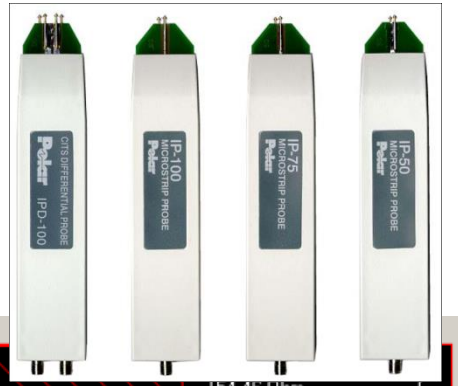
S2 Zdiff 108 Ohm @ 80 / 200 / 80 µm

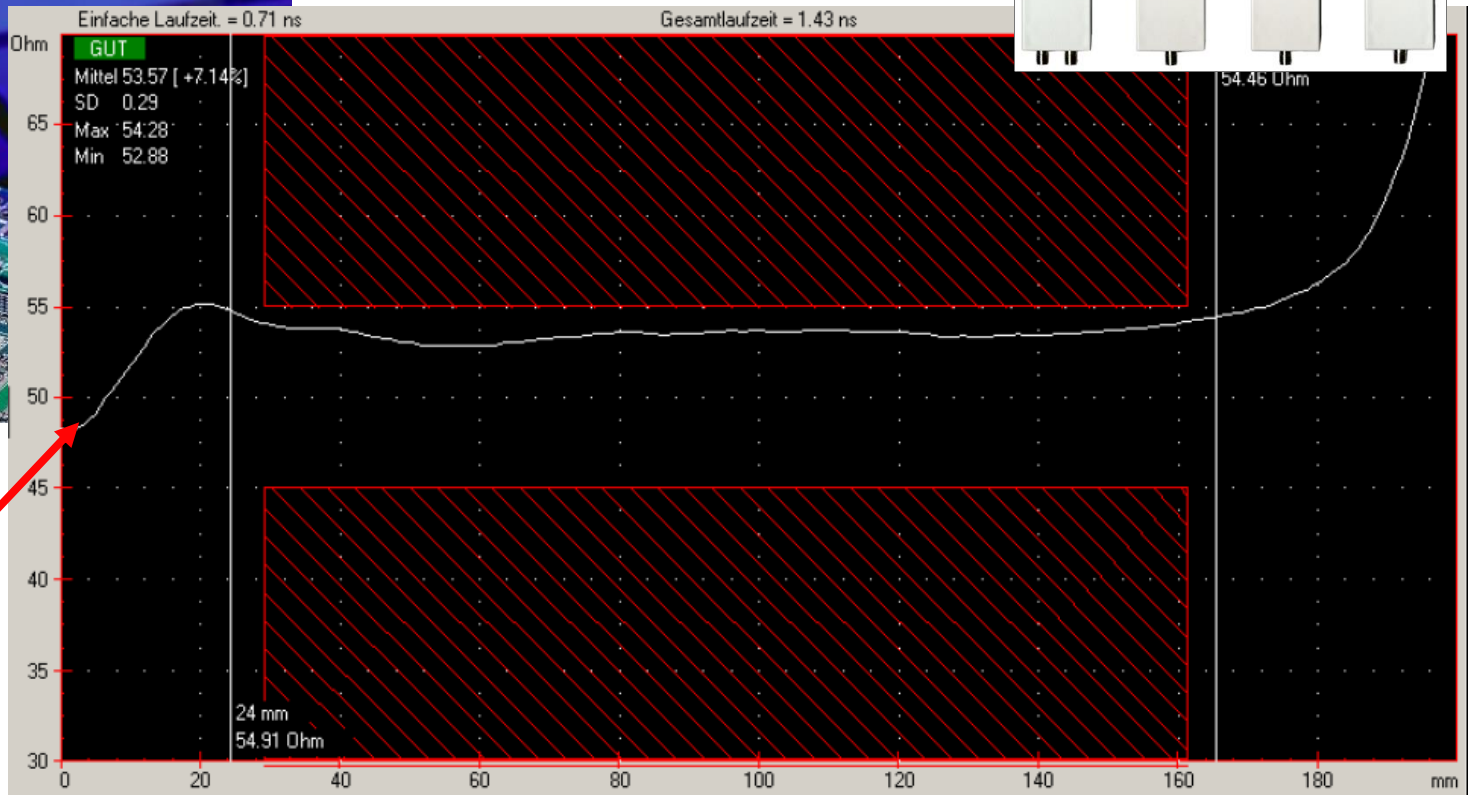
S3 Zo 75 Ohm @ 385 µm LB-Breite

Impedance measuremant Polar



Technology TDR
(Polar Instruments)





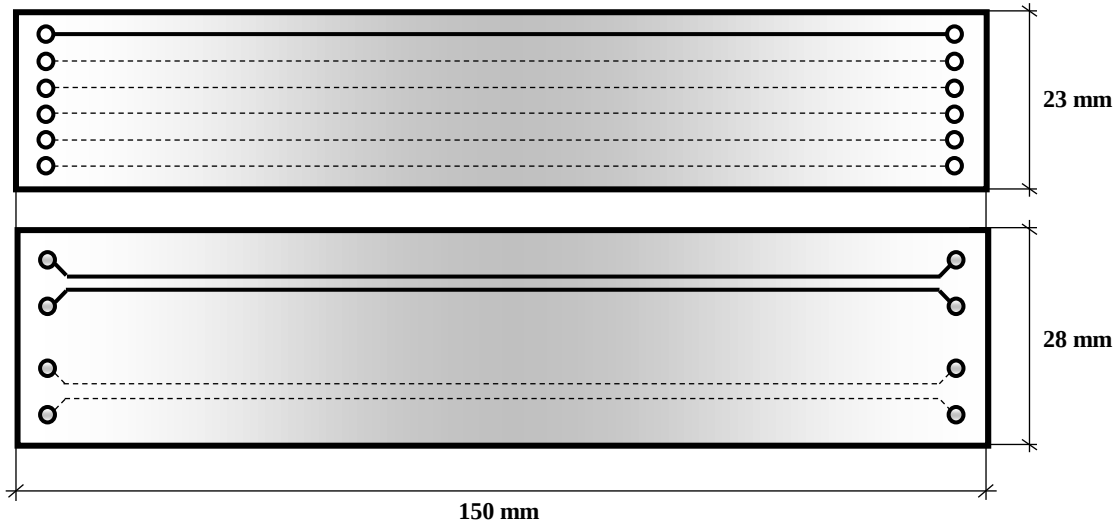
Transition TC -> PCB

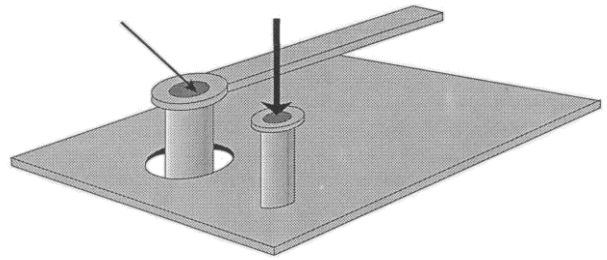
Impedance measurement test coupons

with TC

Single
150 x 23 mm
max. 6 structures

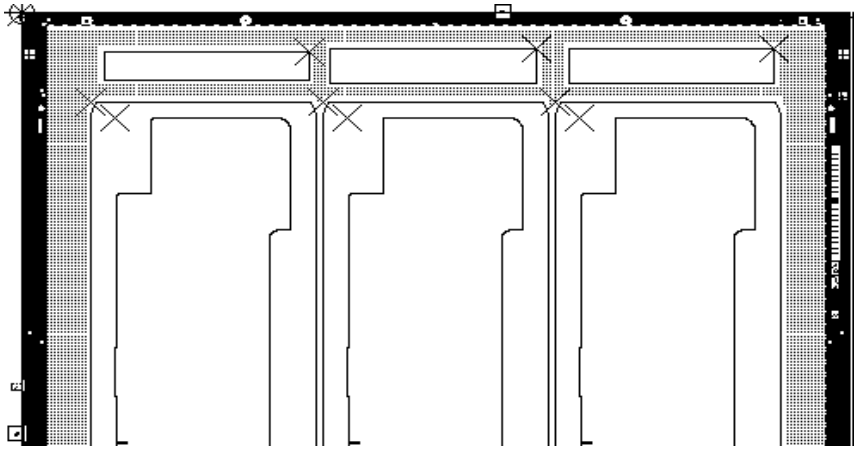
Differentiell
150 x 28 mm
max. 2 structures





TC‘s needed because:

- clear contacting of test adapters
- defined measuring length



PCB‘s per production panel?

Must be considered in the panelisation!

In worst case maybe less PCBs on production panel!

Impedance report

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Web: www.we-online.de

Impedanzreport

Test Summary

TDR Type:	Unknown	DTS Serial Number:	15980
Customer:	Geyers	Job Number:	3#9484 S42440
Board Type:	ML 4	Operator:	Rondak
Part Number:	61501450	Date Code:	1322
Revision:		Test Start:	03/06/13 at 13:24
Station ID:	_TEST STATION 1_	Test End:	03/06/13 at 13:28

Result Summary

Boards Logged:	20
Boards Tested:	20
Boards Passed:	20
Boards Failed:	0

contents

- **customer and job information**
- **requirements for measurements**
- **results of measurement**
- **kleinst mögliche Toleranz +/- 10%**

impedance inseide tolerance:

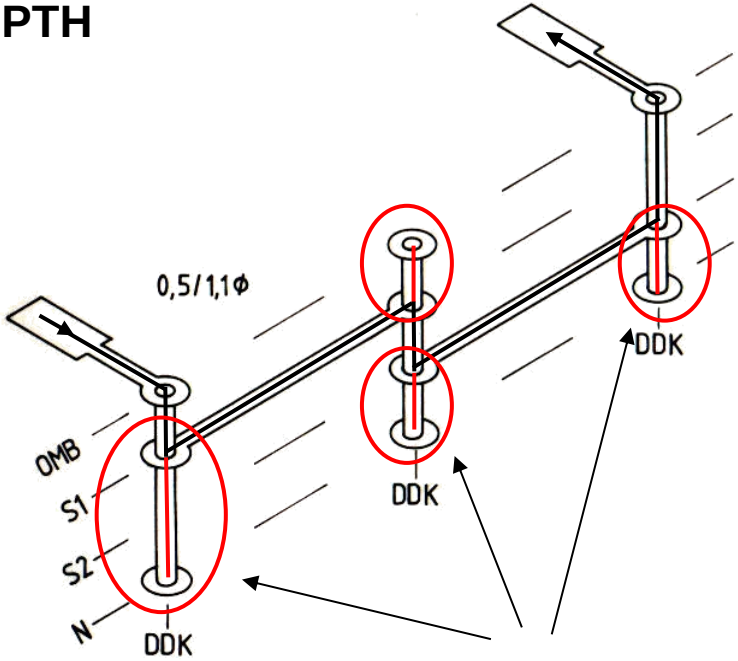
- **PCB‘S + testreport will be sended out to customer**

Why did Würth Elektronik qualified the prepreg type 2113?

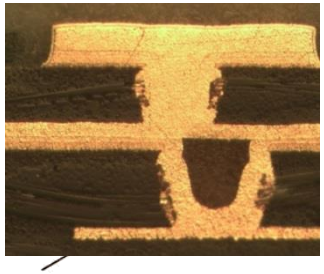
Signal Integrity HDI

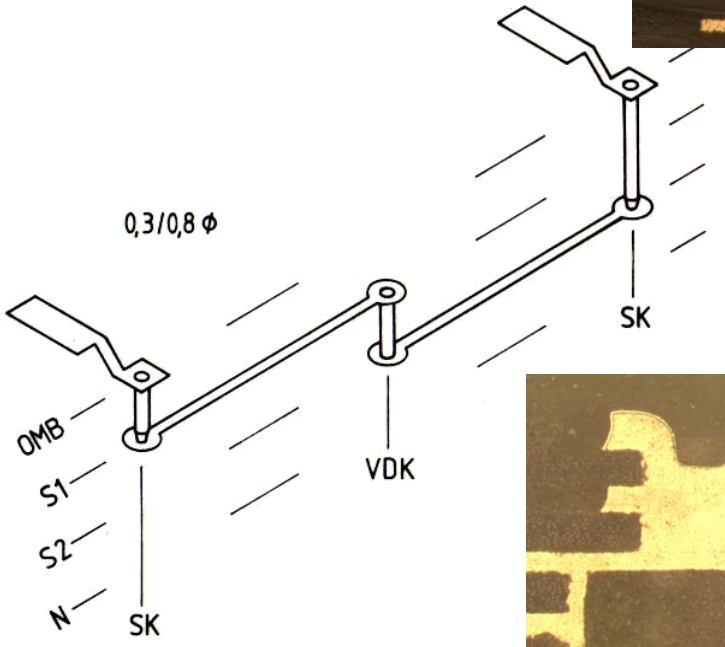
Discontinuities in possible wiring schemes

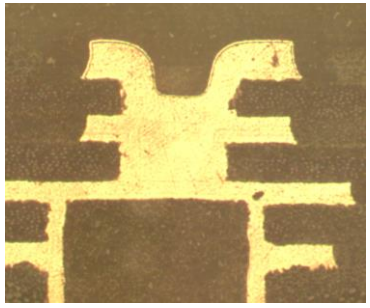
Version 1:
PTH



Version 2:
Microvia / Buried Via



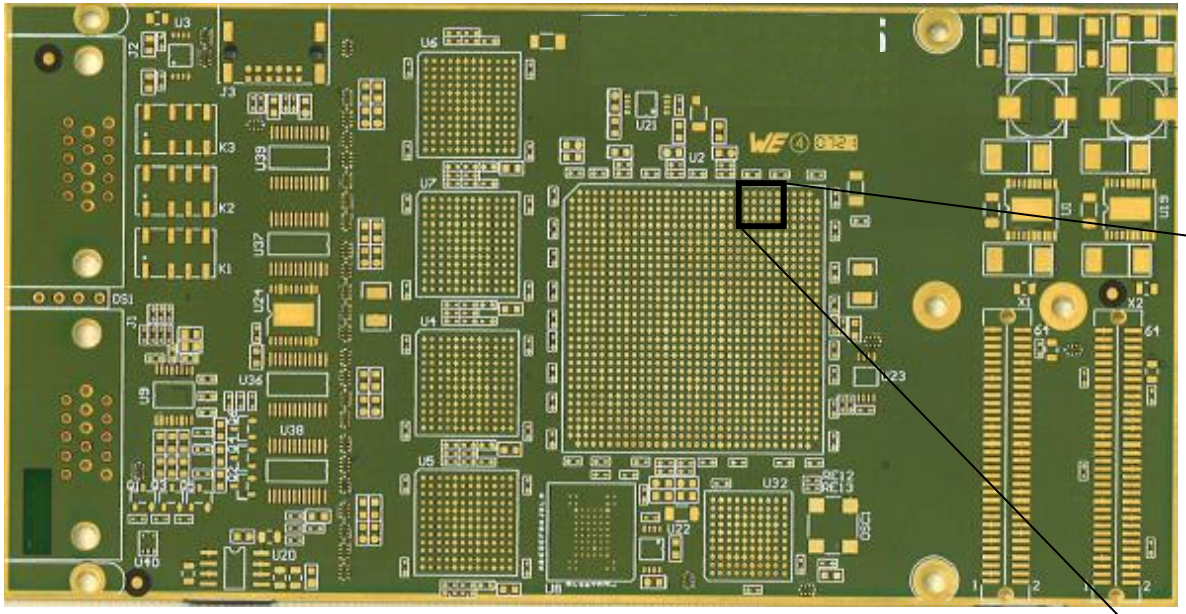


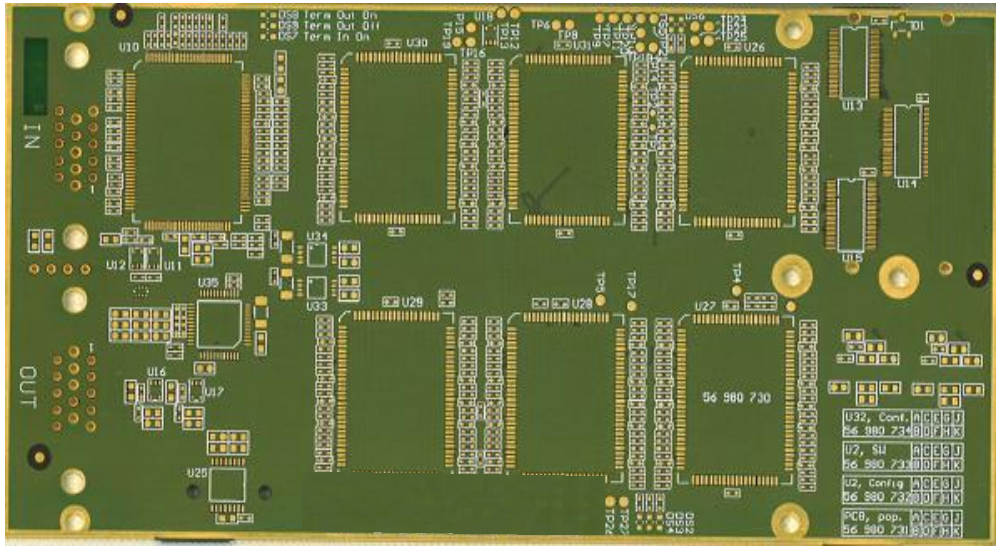


open ends
antenna

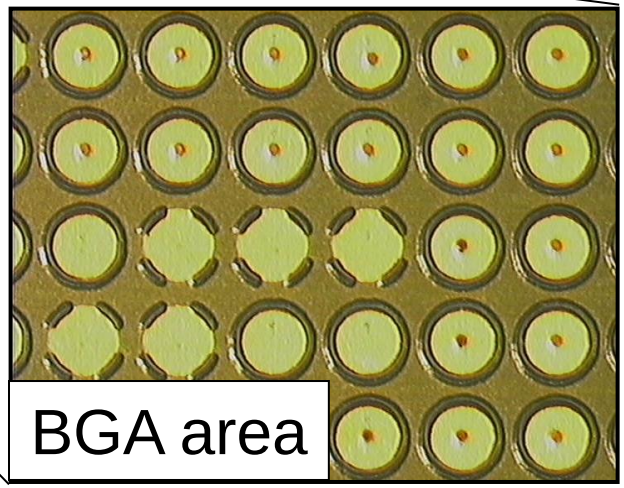
Blind and Buried Vias
result in reduced discontinuities!

Signal Integrity HDI





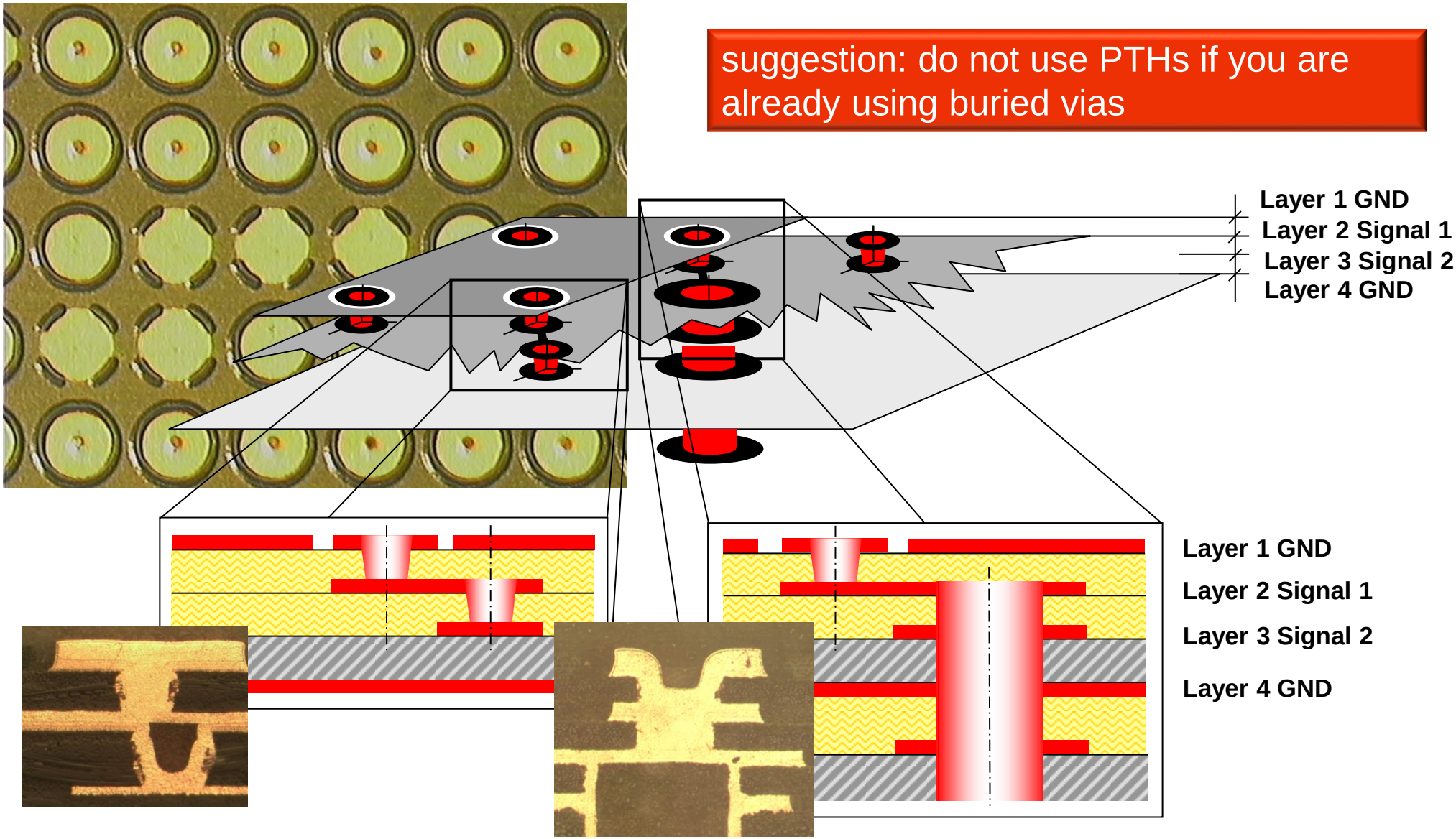
Via in Pad Technology



completely copper on outer layers (no tracks on the outer layers)

signals on outer layers protected from external sources

Design example HDI GND on outer layers



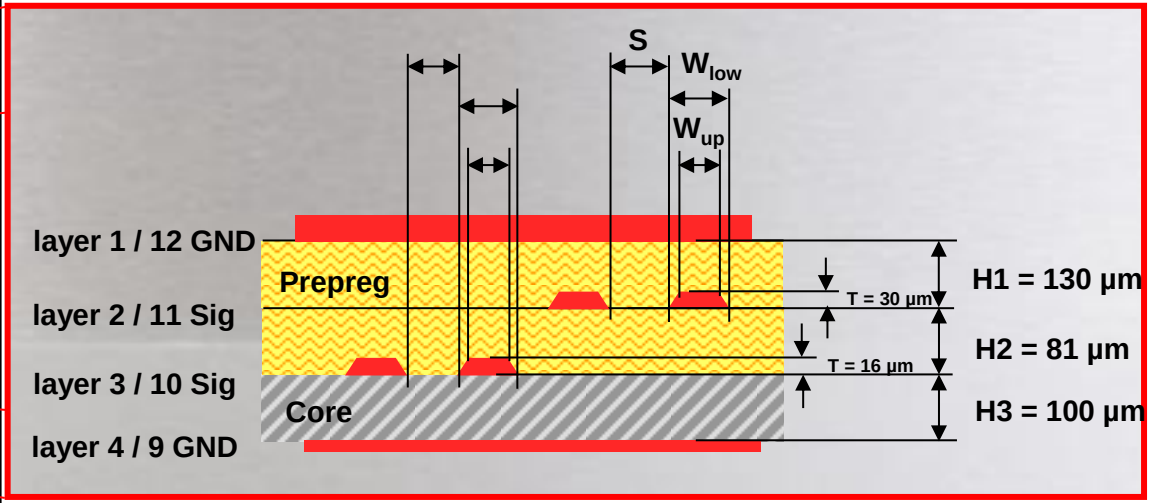
Design example HDI GND on outer layers

BUILD UP HDI
12 - layer

WE-Art No.: 2 + 8(10B) + 2 (staggered)

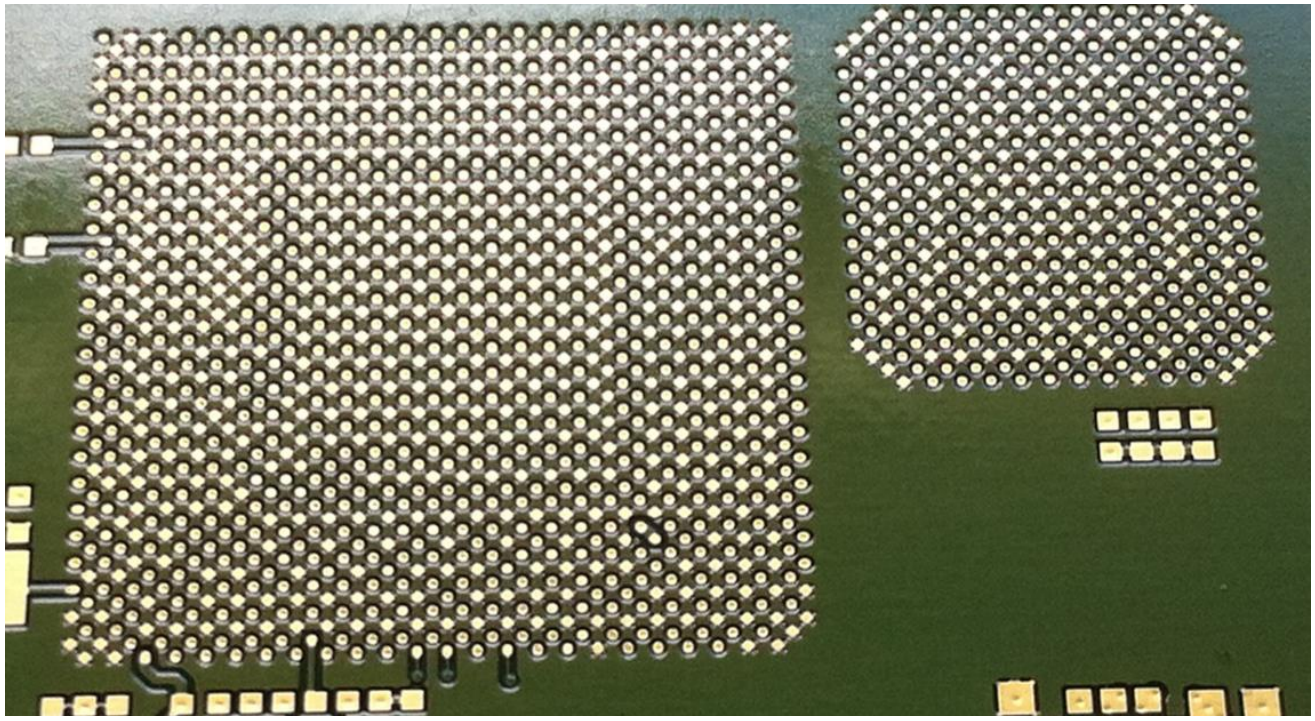
Customer:

layer description		configuration	Raw-Material	CU	PREPREG	Final Thickness	Customer requirements
Customer	WE					[µm]	[µm]
1	TOP/VS	Gnd	foil	12 µm	t)	12	
					1 x 2116	100	
2		Sig	foil	9 µm		30	
					1 x 1080	66	
3		Sig		17.5 µm		16	
			0,100 mm			100	
4		Gnd		17.5 µm		16	
					1 x 2116	110	
5		VCC		17.5 µm		16	
			0,100 mm			100	
6		Sig		17.5 µm		16	
					1 x 1080	66	
7		Sig		17.5 µm		16	
			0,100 mm			100	
8		Gnd		17.5 µm		16	
					1 x 2116	110	
9		Gnd		17.5 µm		16	
			0,100 mm			100	
10		Sig		17.5 µm		16	
					1 x 1080	66	
11		Sig		9 µm		30	
					1 x 2116	100	
12	BOT/RS	Gnd	foil	12 µm	t)	12	



	Layer 2 / 11	Layer 3 / 10
Type	Edge Coupled Offset strip line	Edge Coupled Offset strip line
Distance layer 1 / 12 GND	130 µm	211 µm
Distance layer 4 / 9 GND	181 µm	100 µm
Cu Thickness T	30 µm	16 µm
Upper trace width W_{up}	82 µm	95 µm
Lower trace width W_{low}	100 µm	100 µm
Separation S	214 µm	152 µm
Substrate Dielectric ε_r	3.8 / 3.5 / 3.8	3.8 / 3.5 / 3.8
Impedance	100,0 Ω	100,0 Ω

Signal integrity HDI



Example:

INTEL Atom
Pitch 0.593 mm diagonal

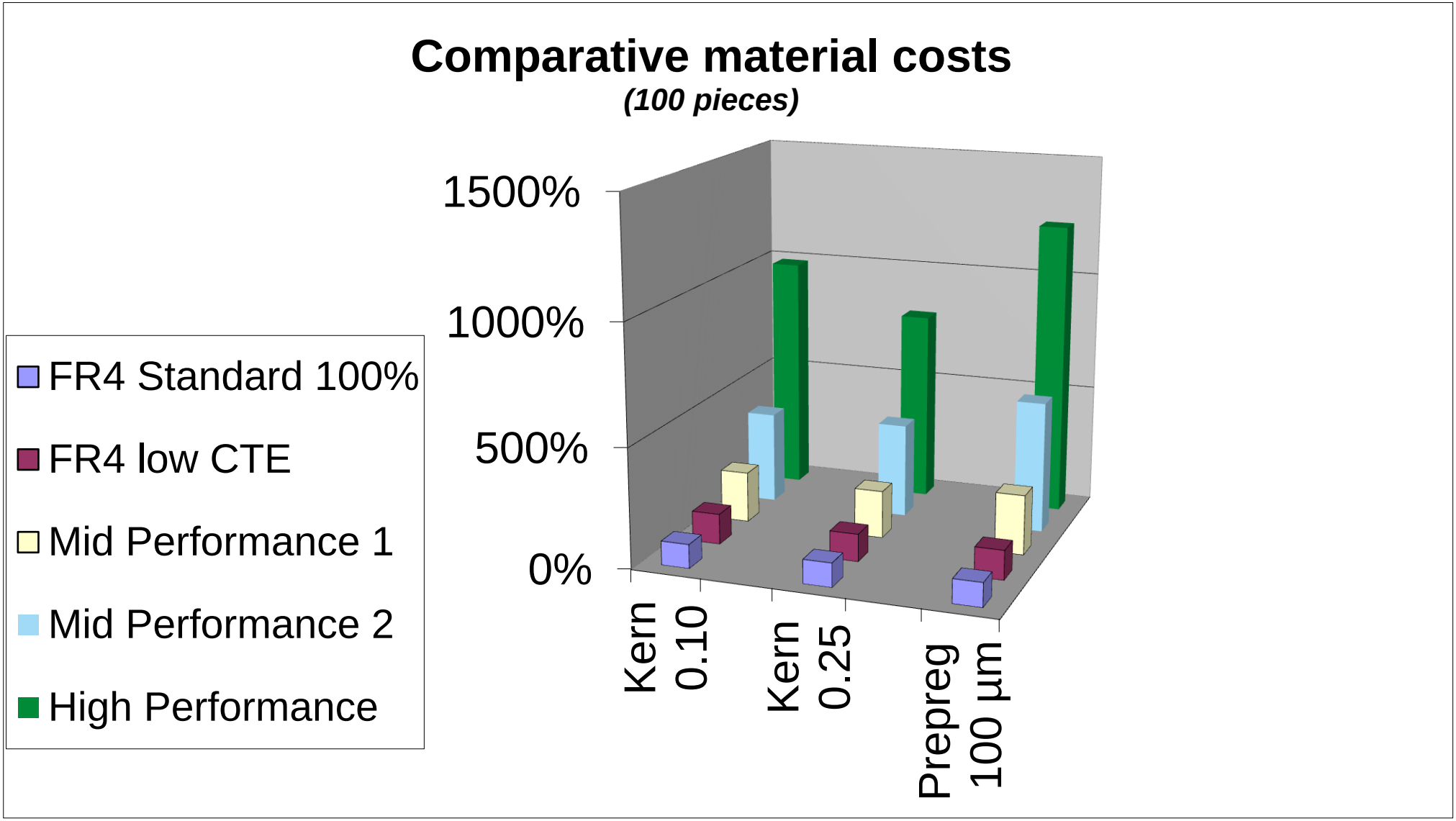
Nearly without any restriction for impedances
layer distances up to ca. 100 µm
track width 90 µm up to pitch 0,6 mm

For smaller pitches e.g. 0,4 mm and 0,5 mm µVia layer distances max. 60-70 µm

summery: Design example HDI GND on outer layers

- using the outer layer as GND, gives:
- direct connection from the solder pad to the first and second inner layer by staggered mircovias
- optimal x – y routing avoids crosstalk between the lines
- a very good shielding avoiding EMC problems
- using 100 µm dielectric thickness for µVias, gives:
- Nearly no restrictions for impedance defined structures

Material costs of high frequency materials



Signal integrity forecast materials

- next steps
- Looking for project partners
- Qualification of mid-performance materials for production
- Materials for frequencies from 2,5 GHz - ca. 10 GHz or 15 GHz
- Lower material costs compared to high performance materials
- e.g. EMC Elite EM888, Isola FR408 HR, Megtron2, Megtron6

If needed please contact Würth Elektronik

Summary

- **Signal Integrity:**

Higher transmission rates and frequencies increasingly more often require impedance matching.

Due to this, we offer our service to you!

For higher transmission rates it can often be the case that high frequency materials are necessary.

In the future cost effective high frequency materials will also be necessary.

We are well prepared!

Understanding the connections is the secret to success!

Many thanks for your interest!

more than you expect

Philipp Reeb
WÜRTH ELEKTRONIK GmbH & Co. KG
Produkt Management
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