Webinar 2013: Improved signal integrity through impedance matched circuit boards

Würth Elektronik Circuit Board Technology
Agenda

S Impedance and the circuit board
I Material aspects and parameters
G Impedance calculation
N Layer stack-ups
A Impedance and HDI (EMC)
L High frequency and mid-performance materials
Impedance matching needed to keep the variations as small as possible!
PCB and impedance

PCB has an ohmic, capacitive and inductive proportion

not an optimal transfer medium between transmitter and receiver

parameters that influence the signal on a PCB

- Length of conductor
- Raw material loss factor and permittivity
- Reflection due to the PTHs
- Impedance matching
- Crosstalk between conductors
- Noise interference from external sources (EMC shielding)
Important parameters

\[ w + h = \text{layouter/developer} + \text{PCB supplier} \]
\[ t = \text{galvanic process, base copper} \]
\[ \varepsilon_r = \text{base material} \]

WE offers: advanced partnership!
Material parameters Epsilon R

FR4 Pre-preg 106
Thickness 50 µm
$\varepsilon_r = 2.8 - 3.7$
Resin content ~70%

FR4 Pre-preg 2116
Thickness 90 – 110 µm
$\varepsilon_r = 3.6 - 3.8$
Resin content ~50%

FR4 Pre-preg 1080
Thickness 60 - 70 µm
$\varepsilon_r = 3.2 - 3.7$
Resin content ~60%

FR4 Pre-preg 7628
Thickness 170 – 190 µm
$\varepsilon_r = 4.1 - 4.6$
Resin content ~45%

glass $\varepsilon_r \sim 6.1$ / resin $\varepsilon_r \sim 3.2$

Cores are laminated pre-pregs
**Epsilon R**

**dielectric losses**

**ε_r values in relation to the layer distance FR4**

(lossy ε_r)

<table>
<thead>
<tr>
<th>Pre-preg</th>
<th>1080</th>
<th>2 x 1080</th>
<th>3 x 1080</th>
<th>2116</th>
<th>2 x 2116</th>
<th>3 x 2116</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tg 135</td>
<td>3.2</td>
<td>3.5</td>
<td>3.6</td>
<td>3.6</td>
<td>3.9</td>
<td>4.7</td>
</tr>
<tr>
<td>Tg 150 hf</td>
<td>3.5</td>
<td>3.7</td>
<td>3.9</td>
<td>3.8</td>
<td>4.3</td>
<td>4.6</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Cores</th>
<th>60 µm</th>
<th>100 µm</th>
<th>150 µm</th>
<th>250 µm</th>
<th>510 µm</th>
<th>710 µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tg 135</td>
<td>3.2</td>
<td>3.5</td>
<td>3.6</td>
<td>3.6</td>
<td>3.9</td>
<td>4.7</td>
</tr>
<tr>
<td>Tg 150 hf</td>
<td>3.5</td>
<td>3.7</td>
<td>3.9</td>
<td>3.8</td>
<td>4.3</td>
<td>4.6</td>
</tr>
</tbody>
</table>

Influence:
- layer distance
- frequency ....

Influence on characteristic wave impedance

**effective ε_r**
determination of $\varepsilon_r^{\text{effective}}$

Calculation of the $\varepsilon_r$ value according to microsection picture with the help of Polar

<table>
<thead>
<tr>
<th>H1</th>
<th>layer distance</th>
</tr>
</thead>
<tbody>
<tr>
<td>W1</td>
<td>lower track width</td>
</tr>
<tr>
<td>W2</td>
<td>upper track width</td>
</tr>
<tr>
<td>T1</td>
<td>copper thickness</td>
</tr>
<tr>
<td>C1</td>
<td>solder resist on substrate (FR4)</td>
</tr>
<tr>
<td>C2</td>
<td>solder resist on track</td>
</tr>
<tr>
<td>CEr</td>
<td>$\varepsilon_r$ solder resist (supplier)</td>
</tr>
</tbody>
</table>

Er  dielectric constant
## Layer distances

<table>
<thead>
<tr>
<th>Layout Type</th>
<th>Pre-preg</th>
<th>17 µm copper</th>
<th>35 µm copper</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre-preg against plane or foil</td>
<td>1 x 1080</td>
<td>65 µm</td>
<td>60 µm</td>
</tr>
<tr>
<td></td>
<td>2 x 1080</td>
<td>134 µm</td>
<td>128 µm</td>
</tr>
<tr>
<td>Pre-preg against layout</td>
<td>2 x 1080</td>
<td>128 µm</td>
<td>120 µm</td>
</tr>
<tr>
<td>Plane against plane or foil</td>
<td>1 x 1080</td>
<td>70 µm</td>
<td>68 µm</td>
</tr>
<tr>
<td></td>
<td>2 x 1080</td>
<td>140 µm</td>
<td>136 µm</td>
</tr>
</tbody>
</table>
Models

layer / track configuration

layer configuration:

track configuration:

Single
Differential
Coplanar
Which parameters have the biggest influence on the impedance of a track?
Parameters for impedance calculations

- **C2**: Thickness solder resist over track [15 µm]
- **S1**: Gap layout
- **W2**: Upper track width (head)
- **T1**: Copper thickness
- **C1 = C3**: Thickness solder resist over FR4 [42 µm]
- **H1**: Layer distance
  - Signal > Reference
- **εr**: Dielectric constant solder resist [typ. 3.5]
- **εr**: Dielectric constant FR4
- **W1**: Lower track width (foot) = layout
**Service “impedance defined stack-ups“**

**Information required:**

- **type of stack-up:** Standard <> HDI / via types
- **Number of layers**
- **PCB – thickness**
- **Copper thickness** (especially inner layers)
- **layer order:** position of signal layer plus corresponding reference layers
  - **Number of signal layers and number of reference layers** (Gnd, Power, VCC)
- **Impedance requirements** (Single e.g. 50 Ohm) (Differential e.g. 90 und 100 Ohm)
- **Which track widths and gaps are preferred or possible?**
## Impedance values for different pre-pregs

### Microstrip Outer Layers

<table>
<thead>
<tr>
<th>Prepreg (each one ply)</th>
<th>1080</th>
<th>2113</th>
<th>2116</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer spacing above plane layer (pressed thickness, 1 oz copper L2)</td>
<td>68 µm, $\varepsilon_r$ effective 3.5</td>
<td>92 µm, $\varepsilon_r$ effective 3.6</td>
<td>108 µm, $\varepsilon_r$ effective 3.8</td>
</tr>
<tr>
<td>Track Width 50 Ω Single Impedance</td>
<td>109 µm (with $\varepsilon_r$ 4.2: 94 µm)</td>
<td>154 µm (with $\varepsilon_r$ 4.2: 136 µm)</td>
<td>179 µm (with $\varepsilon_r$ 4.2: 165 µm)</td>
</tr>
<tr>
<td>Track Width Track Separation 100 Ω diff. Impedance</td>
<td>100 µm 305 µm</td>
<td>100 µm 137 µm</td>
<td>100 µm 122 µm</td>
</tr>
</tbody>
</table>
Example stack-up

<table>
<thead>
<tr>
<th>LAGENBEZEICHNUNG</th>
<th>AUFBAU</th>
<th>BASIS-Material</th>
<th>CU</th>
<th>PREPREG ANZAHL/TYP</th>
<th>Dielektrizitäts-konstante</th>
<th>ENDICKE</th>
<th>KUNDEN-FORDERUNG</th>
</tr>
</thead>
<tbody>
<tr>
<td>KUNDE WE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TOP/VS S1 S3</td>
<td></td>
<td>Foil 17.5 µm</td>
<td>1</td>
<td>1 x 1080</td>
<td>4.25</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 x 2116</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 REF</td>
<td></td>
<td>35 µm</td>
<td></td>
<td></td>
<td></td>
<td>33</td>
<td></td>
</tr>
<tr>
<td>3 REF</td>
<td></td>
<td>0.100 mm</td>
<td></td>
<td></td>
<td></td>
<td>3.8</td>
<td>100</td>
</tr>
<tr>
<td>4 S2</td>
<td></td>
<td>17.5 µm</td>
<td></td>
<td></td>
<td></td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>5 REF REF</td>
<td></td>
<td>0.100 mm</td>
<td></td>
<td></td>
<td></td>
<td>3.8</td>
<td>100</td>
</tr>
<tr>
<td>6 S</td>
<td></td>
<td>17.5 µm</td>
<td></td>
<td></td>
<td></td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>7 S</td>
<td></td>
<td>0.100 mm</td>
<td></td>
<td></td>
<td></td>
<td>3.8</td>
<td>100</td>
</tr>
</tbody>
</table>

Impedanzberechnung:
- S1 Zdiff 100 Ohm @ 180 / 185 / 180 µm
- S1 Zdiff 110 Ohm @ 170 / 270 / 170 µm
- S2 Zdiff 100 Ohm @ 94 / 186 / 94 µm
- S2 Zdiff 108 Ohm @ 80 / 200 / 80 µm
- S3 Zo 75 Ohm @ 385 µm LB-Breite
Impedance measurement Polar

Technology TDR (Polar Instruments)

Transition TC -> PCB
Impedance measurement test coupons

Single
150 x 23 mm
max. 6 structures

Differentiell
150 x 28 mm
max. 2 structures

TC’s needed because:
- clear contacting of test adapters
- defined measuring length

PCB’s per production panel?

Must be considered in the panelisation!

In worst case maybe less PCBs on production panel!
# Impedance report

## Contents

- Customer and job information
- Requirements for measurements
- Results of measurement
- Kleinst mögliche Toleranz +/- 10%

## Impedance inside tolerance:

- PCB'S + test report will be sented out to customer

## Test Summary

<table>
<thead>
<tr>
<th>Test Summary</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Station</td>
<td>TEST STATION 1, 2</td>
</tr>
</tbody>
</table>

## Result Summary

- Boarst Logged: 20
- Boarst Tested: 20
- Boarst Passed: 20
- Boarst Failed: 0
Why did Würth Elektronik qualified the prepreg type 2113?
Discontinuities in possible wiring schemes

Version 1: PTH

Version 2: Microvia / Buried Via

Blind and Buried Vias result in reduced discontinuities!
Via in Pad Technology

BGA area

completely copper on outer layers (no tracks on the outer layers)
signals on outer layers protected from external sources
Design example HDI GND on outer layers

suggestion: do not use PTHs if you are already using buried vias
Design example HDI GND on outer layers

<table>
<thead>
<tr>
<th>Layer description</th>
<th>T</th>
<th>Cu Thickness</th>
<th>Upper trace width</th>
<th>Lower trace width</th>
<th>Substrate Dielectric</th>
<th>Impedance</th>
</tr>
</thead>
<tbody>
<tr>
<td>layer 1 / 12 GND</td>
<td></td>
<td>12 µm</td>
<td>82 µm</td>
<td>100 µm</td>
<td>3.8 / 3.5 / 3.8</td>
<td>100,0 Ω</td>
</tr>
<tr>
<td>layer 2 / 11 Sig</td>
<td></td>
<td>30 µm</td>
<td>95 µm</td>
<td>100 µm</td>
<td>3.8 / 3.5 / 3.8</td>
<td>100,0 Ω</td>
</tr>
<tr>
<td>layer 3 / 10 Sig</td>
<td></td>
<td>16 µm</td>
<td>100 µm</td>
<td>100 µm</td>
<td>3.8 / 3.5 / 3.8</td>
<td>100,0 Ω</td>
</tr>
<tr>
<td>layer 4 / 9 GND</td>
<td></td>
<td>181 µm</td>
<td>100 µm</td>
<td>100 µm</td>
<td>3.8 / 3.5 / 3.8</td>
<td>100,0 Ω</td>
</tr>
</tbody>
</table>
Signal integrity

HDI

Example:
INTEL Atom
Pitch 0.593 mm diagonal

Nearly without any restriction for impedances
layer distances up to ca. 100 µm
track width 90 µm up to pitch 0.6 mm

For smaller pitches e.g. 0.4 mm and 0.5 mm µVia layer distances max. 60-70 µm
**Summary: Design example HDI GND on outer layers**

- Using the outer layer as GND, gives:
  - Direct connection from the solder pad to the first and second inner layer by staggered microvias
  - Optimal x–y routing avoids crosstalk between the lines
  - A very good shielding avoiding EMC problems

- Using 100 µm dielectric thickness for µVias, gives:
  - Nearly no restrictions for impedance defined structures
Material costs of high frequency materials

Comparative material costs
(100 pieces)

- FR4 Standard 100%
- FR4 low CTE
- Mid Performance 1
- Mid Performance 2
- High Performance

FR4 Standard 100%
FR4 low CTE
Mid Performance 1
Mid Performance 2
High Performance
Signal integrity forecast materials

next steps

Looking for project partners

Qualification of mid-performance materials for production

Materials for frequencies from 2,5 GHz - ca. 10 GHz or 15 GHz

Lower material costs compared to high performance materials

e.g. EMC Elite EM888, Isola FR408 HR, Megtron2, Megtron6

If needed please contact Würth Elektronik
Summary

- **Signal Integrity:**

  Higher transmission rates and frequencies increasingly more often require impedance matching.

  Due to this, we offer our service to you!

  For higher transmission rates it can often be the case that high frequency materials are necessary.

  In the future cost effective high frequency materials will also be necessary.

  We are well prepared!
Understanding the connections is the secret to success!

Many thanks for your interest!

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