

MORE POWERFUL THAN EVER – THE NEW SLIM.flex TECHNOLOGY



Webinar

Michael Kress October 13th 2020

AGENDA



Basics Design rules Build up Applications SLIM.flex = robust



Michael Kress Head of Product and Process Development

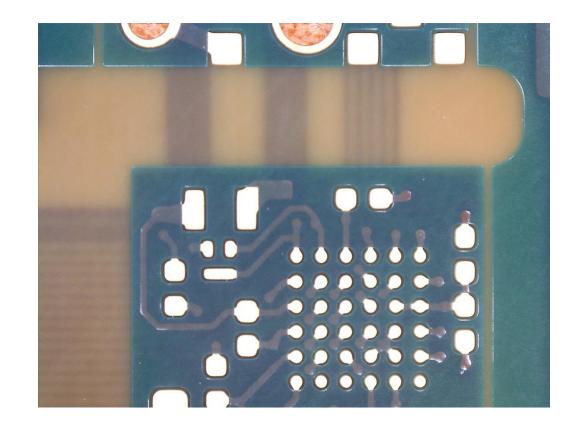


SLIM.flex BASICS

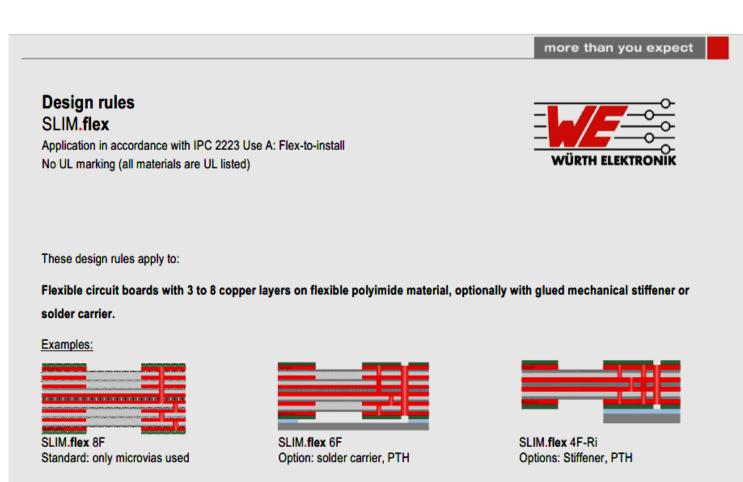
Flex / Rigid-flex buildup possibilities

- 4F 4 layer flex: 0.23mm thick
- 6F 6 layer flex: 0.30mm thick
- 8F 8 layer flex: 0.38mm thick

- Suitable for BGA Pitch 0.3mm
- Solderable several times leadfree
- Very robust and reliable
- Very flexible flex areas possible
- Possible with all common solder surfaces



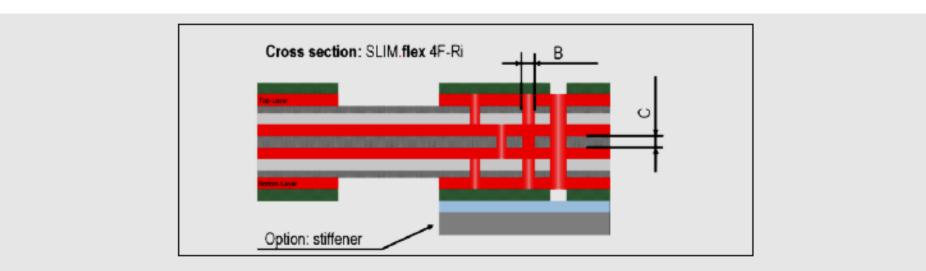
SLIM.flex BASICS



Nomenclature: F = Flex, Ri = Rigid (starr)



SLIM.flex DESIGN RULES

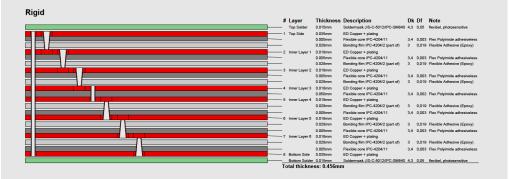


Symbol	Description	Technical Standard Advanced requirements		
Line widths and spacing		75µm/75µm, only Microvias	75µm/100µm with PTH	
	Minimum pad diameter for microvia	225µm	200µm	
	Minimum pad diameter for PTH		450 µm	
В	Finished Hole diameter lasered microvia	70µm	70µm	
-	Distance copper to outline	≥ 300µm	≥ 100µm (Lasercut)	
-	Number x of copper layers (xF)	3-8		
С	Thickness of flexible material polyimide	50µm	75 / 100µm	
-	Thickness of cold-bonded stiffener made of FR4 material	0,1 – 0,5mm	0,5 – 0,8mm	
-	Thickness of cold-bonded solder carrier made of FR4 material	0,80mm		
-	Thickness of glue for stiffener	50 µm		

SLIM.flex Build up



Available as a PDF-document







	notes:	FLEX8_8F_0,46_12				
Circul 4	al copper thickness according to IPC-6012	PCB Thickness Tolerance: rigid ± 10% / flex ± 0,05mm				
	Final copper thickness according to IPC-6012			created		
	IPC 2223 use A "Flex to install"	pcb name		approved		
	IPC 2223 USE A FIEX to Install	engineer		format	A4, landscape	
	Please regard to our sectional design rules:	date				
	www.we-online.com	Template Revision: 07/2020 by Andreas Schilpp / Michael Kress / Werner Öchslen				

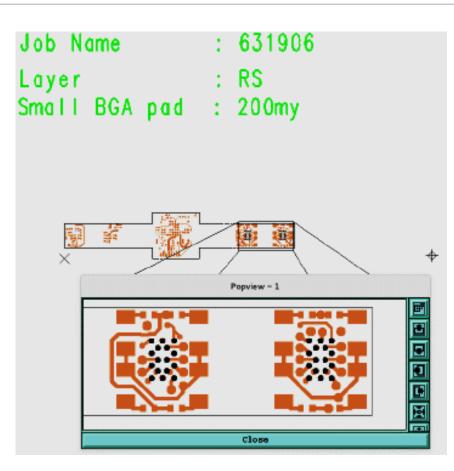
Also available digitally for AltiumDesigner20

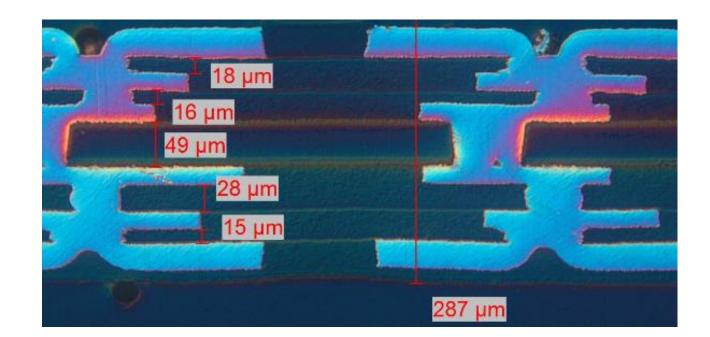






SLIM.flex APPLICATIONS

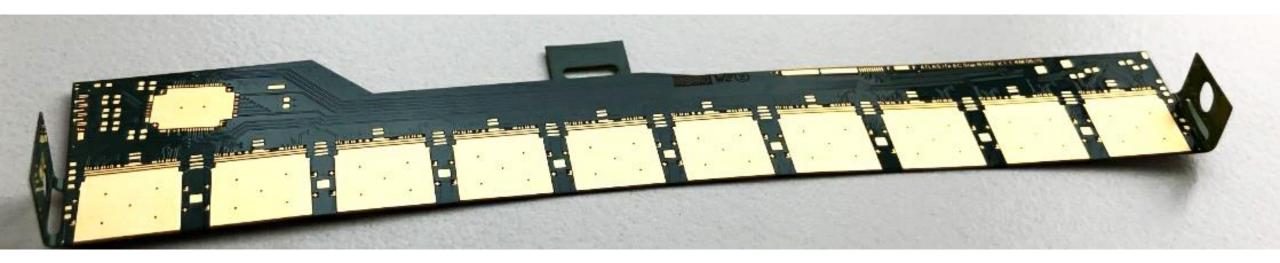




SLIM.flex APPLICATIONS

Particle sensor in the LHC, Cern





Highlights

- Build up 4-layer HDI 1-2b-1, 0,25mm thick
- HDI-Design for FlipChip technology
- Bare chip assembly with wire bonding
- Impedance specified build up
- 75µm fineline layout

- Eliminating of the acrylic improves the detectin and measurement of the collision reaction
- Small thickness with very low tolerances is advantageous for the assembly of the flipchip components

SLIM.flex APPLICATIONS

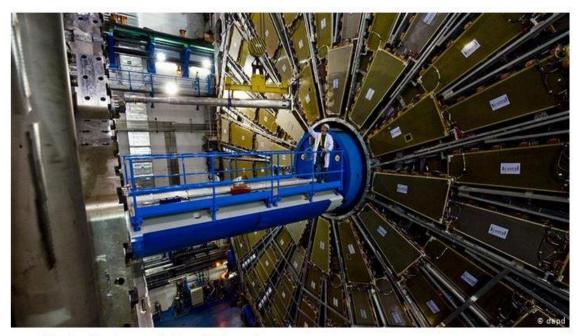
Particle sensor in the LHC, Cern



Progess for research

- Build-up SLIM.flex 4F, thickness 0,25mm
- Impedance matched
 - Zdiff = 100Ω on inner layers
 - Zdiff = 110Ω on outer layers
 - Zo = 50Ω on inner layers
- 75µm fineline layout
- Components: FC soldered, bare chips wirebonded

- Elimination of acrylic improves detection and measurement of collision reactions
- Small thickness with very low tolerances is advantageous for the assambly of the FC components
- Larger process window in the soldering process

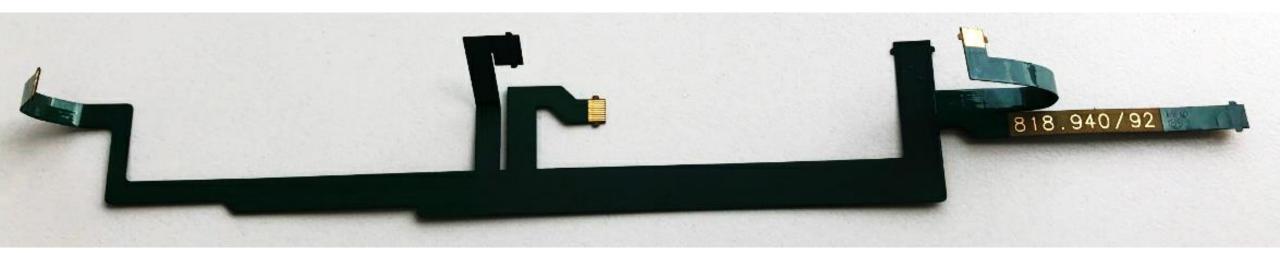


Der Teilchenbeschleuniger LHC ist der größte der Welt

SLIM.flex APPLICATIONS

HighTech Wiring harness





Highlights

- Cable construction ultra flat
- Build-up 6 Layer thickness 0.30mm
- Shielding for inner layers
- ZIF-contacts with locking hook

- Alternative to cabel constructions
- Less space needed for many connections
- Super fast installation thanks to the precurved shape







Qualification (Extract)

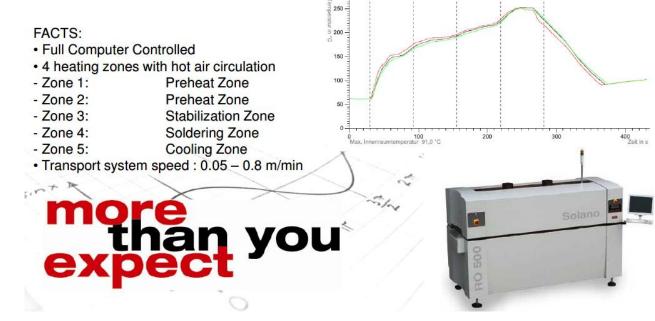


- Reflow testing
 - Drying before reflow process
 - 6 times reflow process with a peak temperature of 260°C

Reflow

TESTS:

- Resistance to Soldering Heat acc. AEC-Q200 / MIL-Std 202 Method 210
- Solderability acc. AEC-Q200 / J-Std 002
- 5-times Reflow WE internal Standard



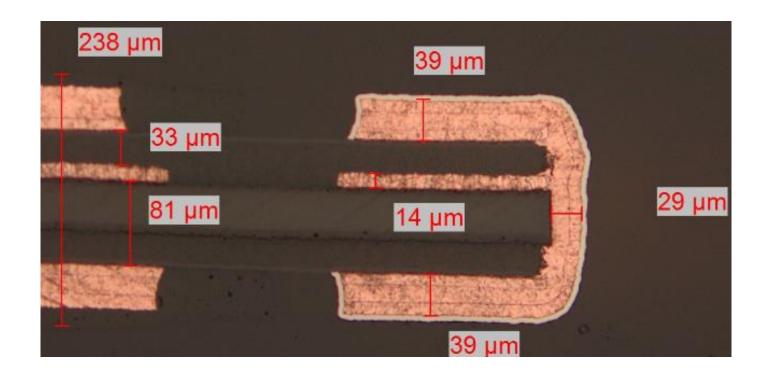


Zanal

Qualification (Extract)



- Reflow testing
 - Drying before reflow process
 - 10 times reflow process with a peak temperature of 260°C
 - ⇒ NO defects



Qualification (Extract)



- Thermal shock test (-55°C / + 125°C)
 - Drying before soldering process
 - 6 times reflow prozess with a peak temperatur of 245°C

Temperature Test System VT7012-S2



TESTS:

- High Temperature Exposure acc. AEC-Q200 / MIL-Std 202 Method 108
- Thermal Shock acc. AEC-Q200 / JESD22 Method JA-104



- Cabinet volume of 120 I
- Dimensions: W470 x H410 x D650 mm
- Max. temperature change rate 11 K/min
- 2 chambers
- Cold chamber ->Temperature range -80 ℃ to +70 ℃
- Warm chamber -> Temperature range -50 ℃ to +220 ℃





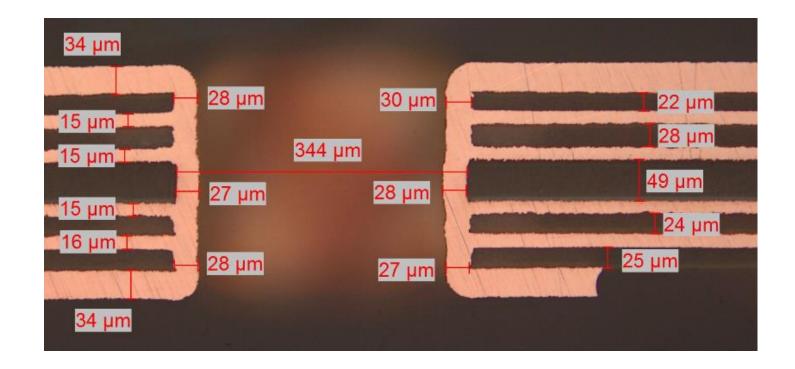
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Qualification (Extract)



- Thermal shock test (-55°C / + 125°C)
 - Drying before soldering process
 - 5 times reflow prozess with a peak temperatur of 245°C
 - → 500 testcycles without defects



SUMMARY

Suitable for

- BGA Pitch 0.35mm with soldermask
- BGA Pitch 0.30mm with soldermask excempted in a block
- Fine line layout on all layers
- Microvias between all layers possible
 - Microvias filled with copper

Excellent thermal stability

- Risk of delamination in the soldering process is reduced significantly
- Capable of multiple reflows (10 times JEDEC reflow tested without failures)



WÜRTH ELEKTRONIK

THANK YOU FOR YOUR ATTENTION! Questions?