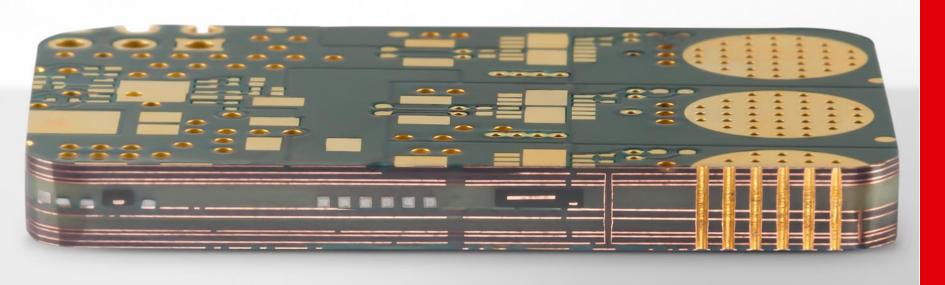


The World of Embedded Components in Printed Circuit Boards Part 2 – Layout and Applications



Jürgen Wolf Würth Elektronik GmbH & Co. KG Circuit Board Technology Advanced Solution Center

YOUR SPEAKER TODAY



Jürgen Wolf Dipl.-Ing. Microsystems Technology

Head of Advanced Solution Center

- Responsible for the technology for embedding components/functions into printed circuit boards and for stretchable printed circuit boards (STRETCH.flex)
- Support of sales for embedding technology and new technologies
- Qualification, planning and further development of these technologies
- With Würth Elektronik Circuit Board Technology since 2008

Save my contact details directly in your address book!





AGENDA

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- **2** Overview of EDA tools and their capabilities
 - How to Design a PCB Layout with Embedded Components
 - Application Examples

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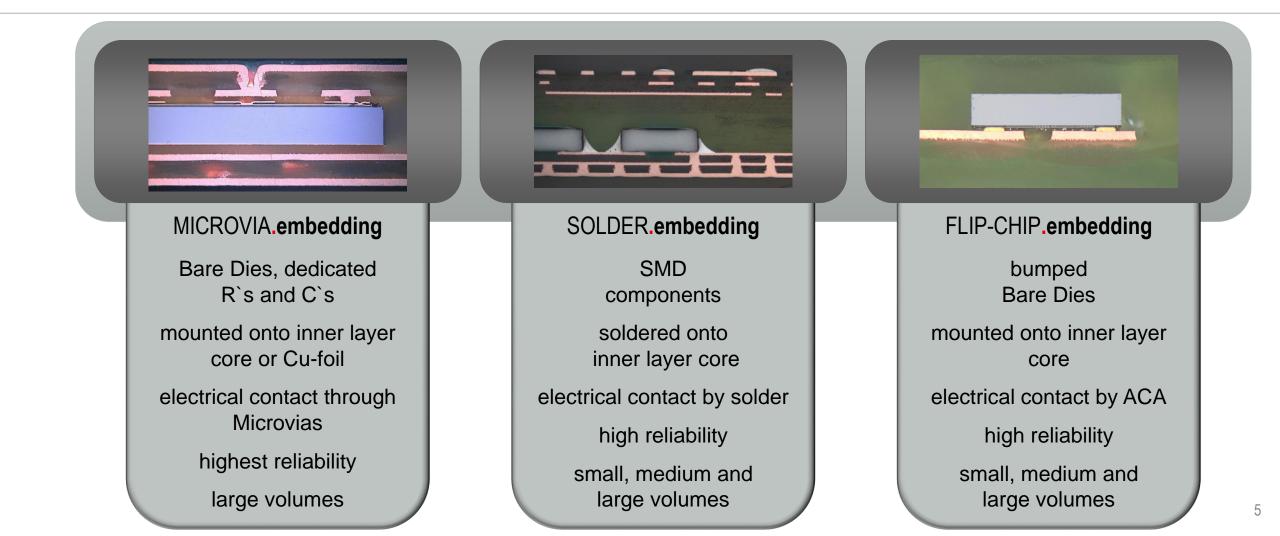
Short Summary of Part 1

- **2** Overview of EDA tools and their capabilities
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- 4 Application Examples

EMBEDDING TECHNOLOGY – THE BASICS

From Part 1: Variants of the Embedding Technology





EMBEDDING TECHNOLOGY – THE BASICS

From Part 1: Advantages and Benefits of Embedded Components



	Miniaturisation	 Package replacement Space savings of assembly area on the outer layers
	Performance/ Function	 Integrated shielding Short signal paths Protection against plagiarism
e c	Reliability	 Protection against environmental influences Secure and full-surface fixing Thermal management

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Short Summary of Part 1

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Short Question



POLL

Which EDA software do you use? (Multiple answers possible)

Please insert the answers in the question-section of GoToWebinar!

Small list of tools to select from (sorted alphabetically - without rating and not complete!)

Allegro PCB Designer (cadence) Altium 365 **Altium Designer** Cadstar (Zuken) CircuitMaker (Altium) **CircuitStudio (Altium) CR-8000 (Zuken)** DesignSpark Eagle gEDA **KiCAD NEXUS** (Altium) **OrCAD PCB Editor (Cadence)** Pads (Siemens EDA/Mentor) Pulsonix **Sprint Layout Target 3001! Ultiboard (NI) Xpedition (Siemens EDA/Mentor)**

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Übersicht EDA-Tools



EDA Tools for Embedding Technology - The current versions of these software tools:



cādence[®] Allegro PCB Design Solution

Miniaturization Option

SIEMENS EDA

(Mentor Graphics®) Xpedition Enterprise





Further tools possible, but with strong limitations

Capabilities of the EDA tools - using the example of cadence[®] Allegro⁼



Normal Multilayer-PCB

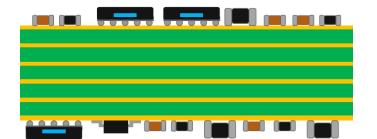
Components on Top and Bottom

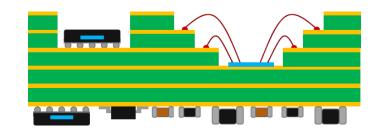
PCB with Cavities

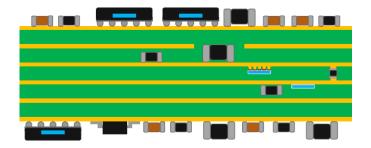
Components in the defined cavities on defined layers and assembly from "outside".

PCB with Embedded Components

Components on the defined inner layers with layer connection and orientation (up/down)









Capabilities of the EDA tools – using the example of cadence[®] Allegro $\overline{-}$

Layer setup of PCBs with Embedded Components

- Orientation of components
- Allow protruding of adjacent layer
- Contacting methods
 "Direct Attach" corresponds to MICROVIA.embedding
 "Indirect Attach" corresponds to SOLDER.embedding

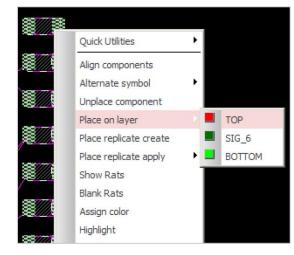
Em	bedded Layer Se	tup					
ID	Layer Name	Туре	Thickness	Embedded Statu	s	Attach Method	
1		SURFACE	0.0010				Тор
2		DIELECTRIC	0.0240				
3	TOP	CONDUCTOR	0.0350	Not Embedded	-		
4		DIELECTRIC	0.0700				
5	LAYER_2	CONDUCTOR	0.0350	Not Embedded	-	•	
6		DIELECTRIC	0.0700				
- 7	LAYER_3	CONDUCTOR	0.0350	Not Embedded	-	-	
8		DIELECTRIC	0.0700				
9	LAYER_4	CONDUCTOR	0.0170	Not Embedded	-	•	
10		DIELECTRIC	0.1000				11
11	LAYER_5	CONDUCTOR	0.0170	Body Down		Direct Attach	
12		DIELECTRIC	0.1270				
13	LAYER_6	CONDUCTOR	0.0170	Protruding Allowed	-		13
14		DIELECTRIC	0.1000				
15	LAYER_7	CONDUCTOR	0.0170	Protruding Allowed	-		
16		DIELECTRIC	0.1270			•	15
						Þ	
	edded Global Parar					2 24	17
1. Pa	ackage height buffe	r:	0.3300	?	у	2 3.4 H H	
2. Minimum cavity gap for merging:		0.2500	?	-			
3. Placebound to via keepout expansion:		0.0000	?	3.4 ⊨			
4. Package to cavity spacing:		0.2000	?	Two	Comps Top View		
5. Via connect height:		0.0000	?	z	L2		
6. Default via connect padstack:				1			
		0.0000		5⊏	L3,		
7. Cavity to route keepout expansion:		0.0000	?		e Comp Side View	Bottom	

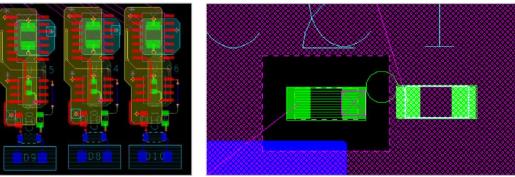


Capabilities of the EDA tools – using the example of cadence[®] Allegro -

Placement of the components

- Onto allowed layers
- DFA-Support with complex rules for distances





Source: Rolf Nick (Fa. FlowCAD) – "Mit Embedded Components Leiterplatten kostengünstig miniaturisieren"

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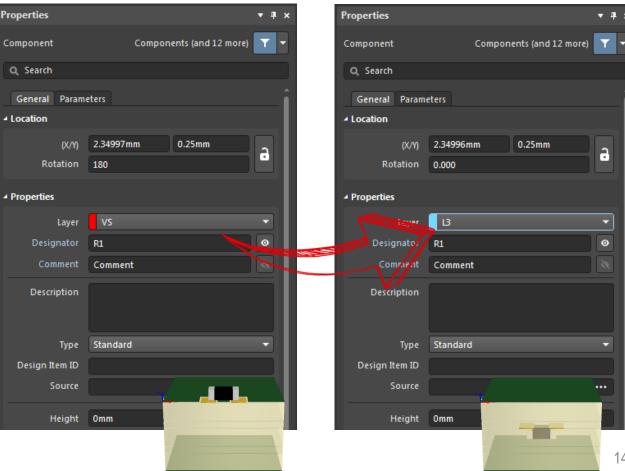
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How to Design a PCB Layout with Embedded Components



Library of components

- Components are created in the library like any other component
- Recommendation: Copy "normal" SMD component and use it only as embedded component afterwards
- Additional information may be required in the component library:
 - Solder mask for inner layers
 - Solder paste for inner layers
 - specific component outline
 - Height of the component as separate parameter
- It becomes an embedded component only when it is moved to an inner layer in the layout



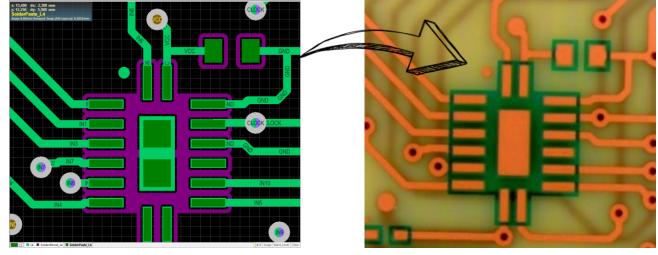
How to Design a PCB Layout with Embedded Components



Library of components – additional information

 Some tools are not capable of providing solder resist and paste data for inner layers.

Workaround: Create additional mechanical layers for solder mask and solder paste data on inner layers



QFN-Footprint in Layout

QFN-Footprint with solder resist before assembly

Side note and reminder of part 1:

Either the solder stop frames can be designed positively - or the clearances as a negative, which we will then convert into frames. Please document accordingly!

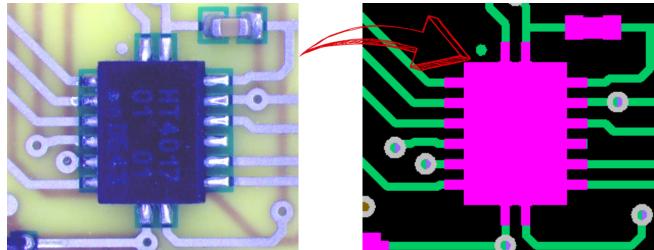
How to Design a PCB Layout with Embedded Components



Library of components – additional information

- Component outline (X/Y) in the data
 - Serve on the one hand the PCB manufacturer for the definition of the "pockets/internal cavities/cut-outs" for the components (see part 1).
 - But are also used for DRC, e.g. to avoid accidental vias through components.
 ⇒ Define outline not only as contour

but as filled area



Assembled QFN for embedding

QFN-Footprint with filled areas for the component outline

How to Design a PCB Layout with Embedded Components

Library of components – additional information

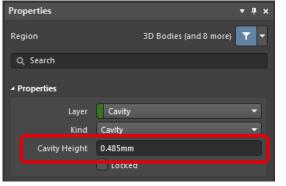
"Pocket/cavity/cut-out" for components

Depending on the technology - e.g. with SOLDER.embedding the height of the cut-out is composed as follows:

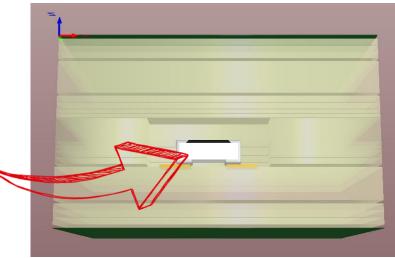
- Height max. tolerance – see data sheet
- Solder stand-off approx. 25..50µm
- Space above component typ. approx. min. 70..100µm
- Can be used by the PCB manufacturer and the layouter to check whether the desired component fits the layer stack-up

Layer	Name	Material	Thickness	Constant	Board Layer Stack	StackC
1	Top Overlay					/////
2	Top Solder	Solder Resist	0,015mm	3,5		
3	VS	Copper	0,040mm			
4	PP2116	FR4 TG150	0,102mm	4,2		
5	PP2116	FR4 TG150	0,102mm	4,2		
6	PP2116	FR4 TG150	0,102mm	4,2		V////
7	L2	Copper	0,035mm			
8	0.50mm-035+035	FR4 TG150	0,500mm	4,2		$\langle $
9	L3	Copper	0,035mm			$\langle $
10	PP2116	FR4 TG150	0,102mm	4,2		$\langle $
11	PP2116	FR4 TG150	0,102mm	4,2		V////
12	PP1080	FR4 TG150	0,062mm	4,2		V
13	PP1080	FR4 TG150	0,062mm	4,2		
14	0.36mm-018+018	FR4 TG150	0,360mm	4,2		
15	PP1080	FR4 TG150	0,062mm	4,2		
16	PP1080	FR4 TG150	0,062mm	4,2		
17	PP2116	FR4 TG150	0,102mm	4,2		
18	PP2116	FR4 TG150	0,102mm	4,2		
19	L4	Copper	0,035mm			$\langle $
20	0.50mm-018+018	FR4 TG150	0,500mm	4,2		$\langle $
21	L5	Copper	0,035mm			V
22	PP2116	FR4 TG150	0,102mm	4,2		$\langle $
23	PP2116	FR4 TG150	0,102mm	4,2		V
24	PP2116	FR4 TG150	0,102mm	4,2		
25	RS	Copper	0,040mm			
26	Bottom Solder	Solder Resist	0,015mm	3,5		
27	Bottom Overlay					

Stack-up from Altium



Definition of the internal cavity



Altium 3D view

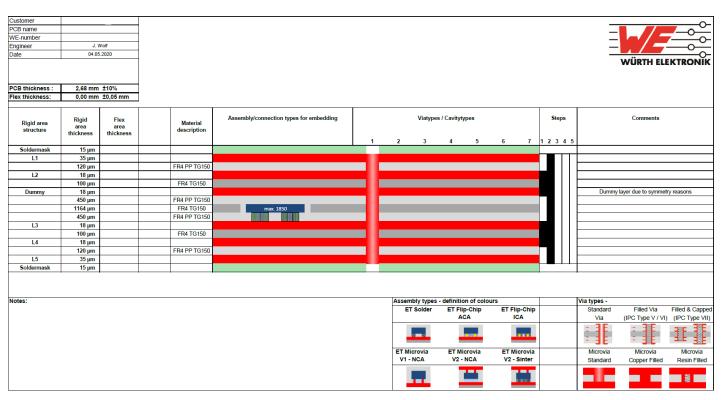


How to Design a PCB Layout with Embedded Components



Layer stack-up

- After analysing the BOM and defining the components to be embedded, a layer stack is provided by the LP manufacturer, which has to be implemented in the EDA tool
- In the layer stack-up, the component location/orientation, max. component heights and possible layer relationships (vias and impedances) are specified



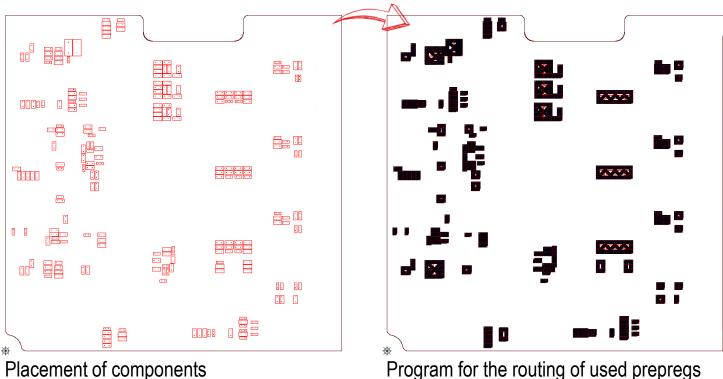
Layer stack-up – created after BOM analysis

How to Design a PCB Layout with Embedded Components



Placement of components

- Brief reminder of part 1: Components are embedded by the resin of the prepregs used in the stack-up
 - \Rightarrow Not the entire area on the inner layer can/may be equipped with components.
 - ⇒ Components should be arranged in groups if possible



Placement of components

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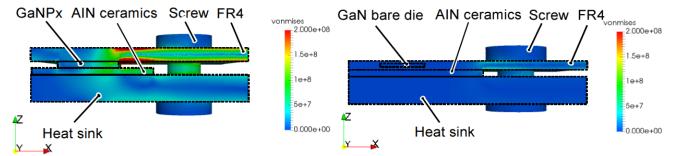


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Application Examples

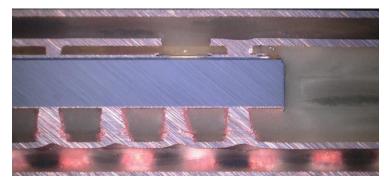


Automotive: Embedded GaN Half Bridge Switching Cell

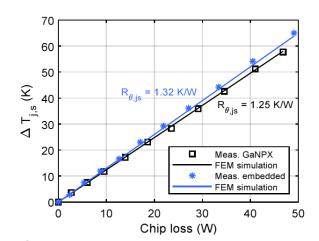


Source: Dechant et. al., »Performance of an Ultra Low Inductance GaN Half Bridge Switching Cell with Substrate Integrated Bare Dies", PCIM 2019

Build-up and comparison of mechanical stress Primary package vs. Embedding



Microsection of the printed circuit board



For even better performance, the number of µVias can be doubled.

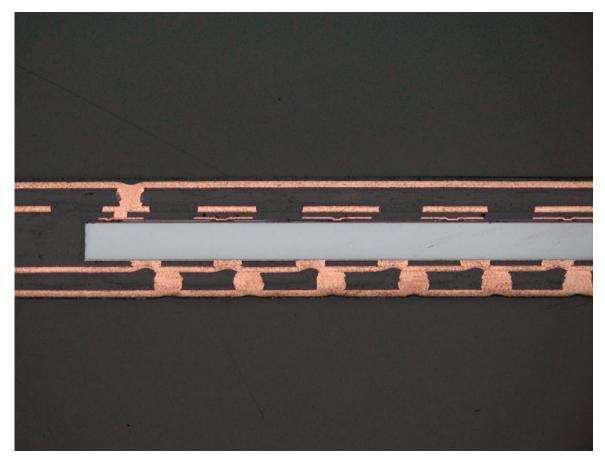
Simulated and measured Junction-Temperature

Application Examples



Automotive: Embedded GaN Half Bridge Switching Cell

- GaN IC embedded in 4-layer HDI multilayer
- Contacted by Microvias on all layers



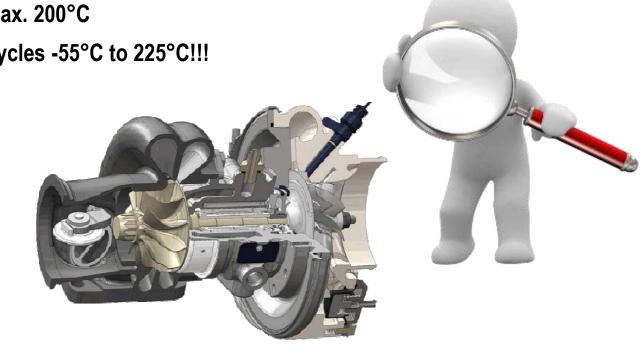
Microsection - optimised layer stacking for improved back side connection

Application Examples: Highest Reliability Requirements



Automotive: embedded silicon components – sensor in the engine compartment

- Operating temperature max. 200°C
- Cycle-proof: TCT 1.000 cycles -55°C to 225°C!!!
- As small as possible
- Injection moulding-proof

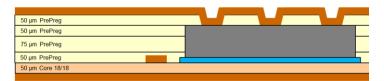


Application Examples: Highest Reliability Requirements



Automotive: embedded silicon components – sensor in the engine compartment

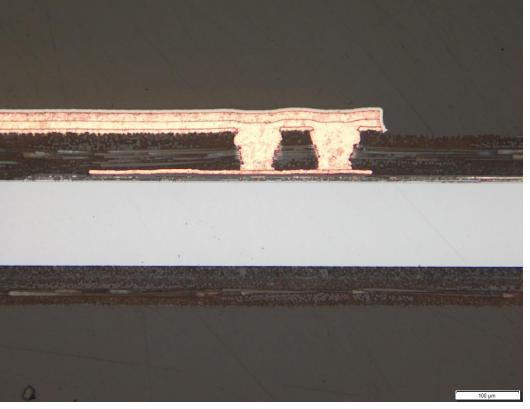
- Operating temperature max. 200°C
- Cycle-proof: TCT 1.000 cycles -55°C to 225°C!!!
- As small as possible
- Injection moulding-proof



Stack-up: <= 300µm overall thickness



Module with embedded ASIC and 2x Si-C's



Microsection after 1000 cycles TCT -55°C to 225°C

Application Examples: Highest Reliability Requirements



Medical Technology: embedded ASIC – radio module for implants

\sub Microsemi. ZL70323

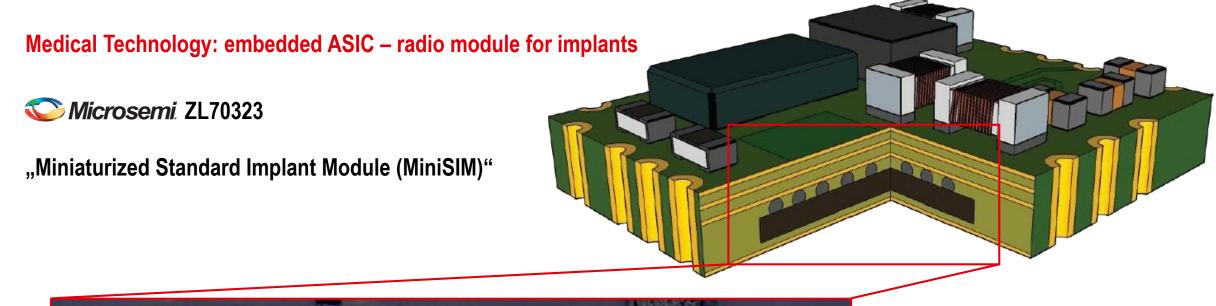
"Miniaturized Standard Implant Module (MiniSIM)" Complete radio solution for implant based on the MICS-Band (Medical Implant Communication Service)

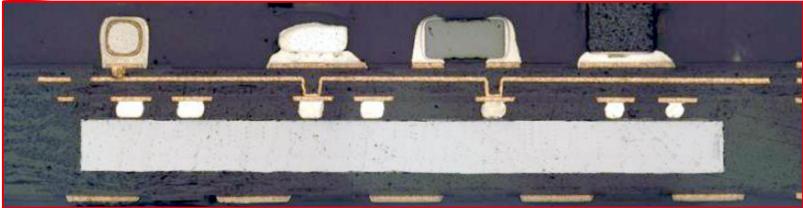


Source: Microsemi

Application Examples: Highest Reliability Requirements







Source: Microsemi

Application Examples: Highest Reliability Requirements



Medical Technology: embedded ASIC Microsemi, ZL70323 "Miniaturized Standard Implant Module (MiniSIM)" Size comparison

Source: Microsemi

Short Question



Poll

When you look back at the two parts, what do you think about our embedding technology?

Thank you for your attention!

JÜRGEN WOLF

Head of Advanced Solution Center



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