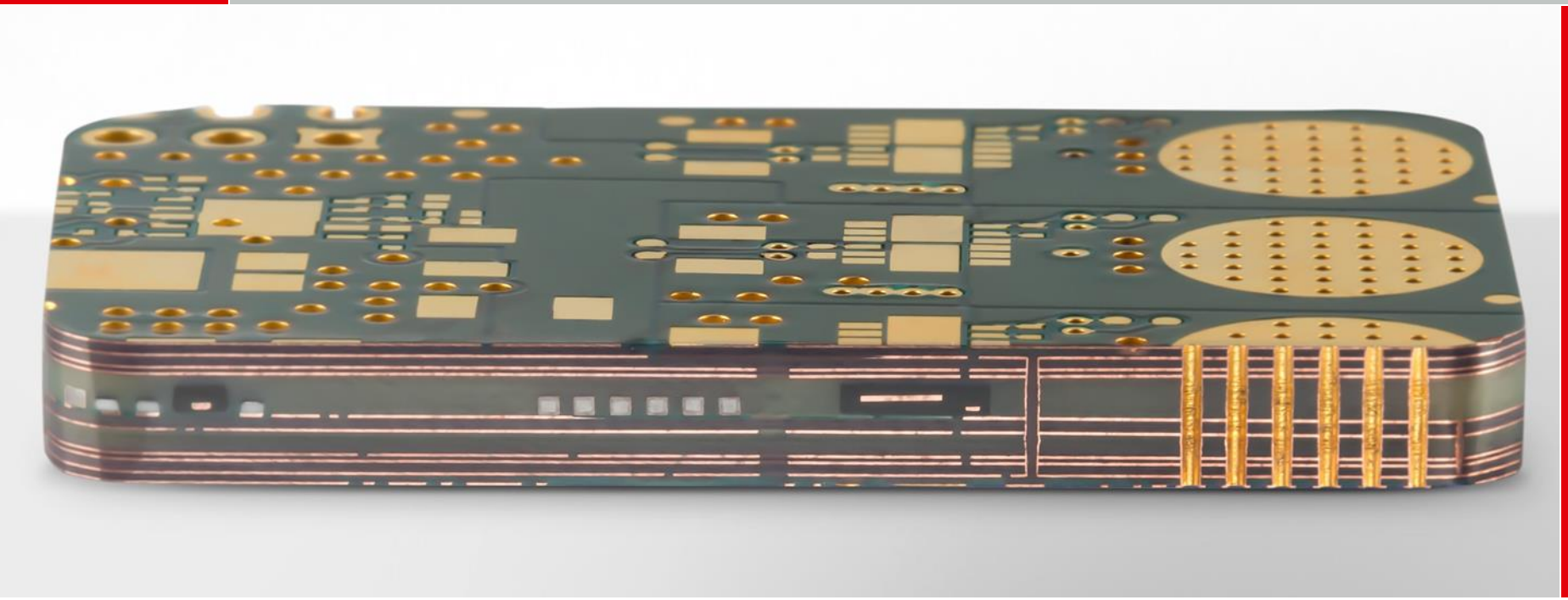
The World of Embedded Components in Printed Circuit Boards

Part 1 – The Basics



Jürgen Wolf
Würth Elektronik GmbH & Co. KG
Circuit Board Technology
Advanced Solution Center

YOUR SPEAKER TODAY

- **Jürgen Wolf**
  Dipl.-Ing. Microsystems Technology

- **Head of Advanced Solution Center**
  - Responsible for the technology for embedding components/functions into printed circuit boards and for stretchable printed circuit boards (STRETCH.**flex**)
  - Support of sales for embedding technology and new technologies
  - Qualification, planning and further development of these technologies

- **With Würth Elektronik Circuit Board Technology since 2008**

Save my contact details directly in your address book!

AGENDA

1. Variants of the Embedding Technology
2. Process flows
3. Criteria for selecting the appropriate embedding variant
4. Design rules
5. Workflow of an ET project

EMBEDDING TECHNOLOGY – THE BASICS

Short Question

WÜRTH ELEKTRONIK

POLL

Have you ever planned or executed a project with embedded components?

AGENDA

1 **Variants of the Embedding Technology**

2 Process flows

3 Criteria for selecting the appropriate embedding variant

4 Design rules

5 Workflow of an ET project

EMBEDDING TECHNOLOGY – THE BASICS

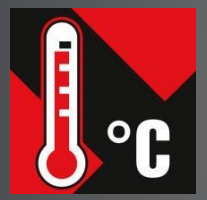
Advantages and Benefits of Embedded Components

Miniaturisation

- Package replacement
- Space savings of assembly area on the outer layers

Performance/ Function

- Integrated shielding
- Short signal paths
- Protection against plagiarism

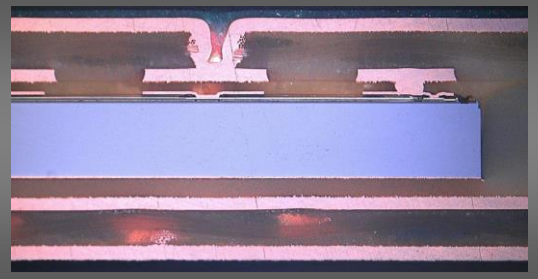


Reliability

- Protection against environmental influences
- Secure and full-surface fixing
- Thermal management

EMBEDDING TECHNOLOGY – THE BASICS

Variants of the Embedding Technology



MICROVIA.**embedding**

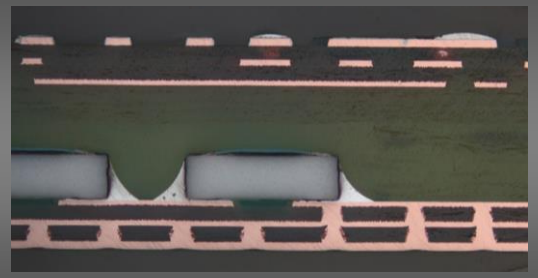
Bare Dies, dedicated R`s and C`s

mounted onto inner layer core or Cu-foil

electrical contact through Microvias

highest reliability

large volumes



SOLDER.**embedding**

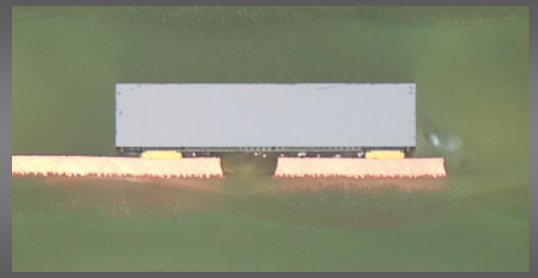
SMD components

soldered onto inner layer core

electrical contact by solder

high reliability

small, medium and large volumes



FLIP-CHIP.**embedding**

bumped Bare Dies

mounted onto inner layer core

electrical contact by ACA

high reliability

small, medium and large volumes

AGENDA

1 Variants of the Embedding Technology

2 **Process flows**

3 Criteria for selecting the appropriate embedding variant

4 Design rules

5 Workflow of an ET project

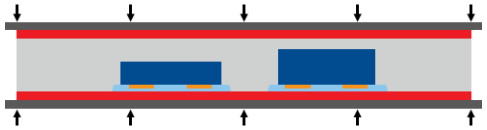
EMBEDDING TECHNOLOGY – THE BASICS

Process flows – MICROVIA.**embedding** – Version 1

1 **Face-down assembly onto Cu-foil and into non-conductive epoxy adhesive**

2 **Multilayer lay-up incl. cavities for components**

3 **Multilayer lamination - cavities will be filled**



4 **Laser drilling onto metal pads of the components**

5 **Electroplating and remaining process steps of the PCB**

EMBEDDING TECHNOLOGY – THE BASICS

Process flows – MICROVIA.**embedding** – Version 2

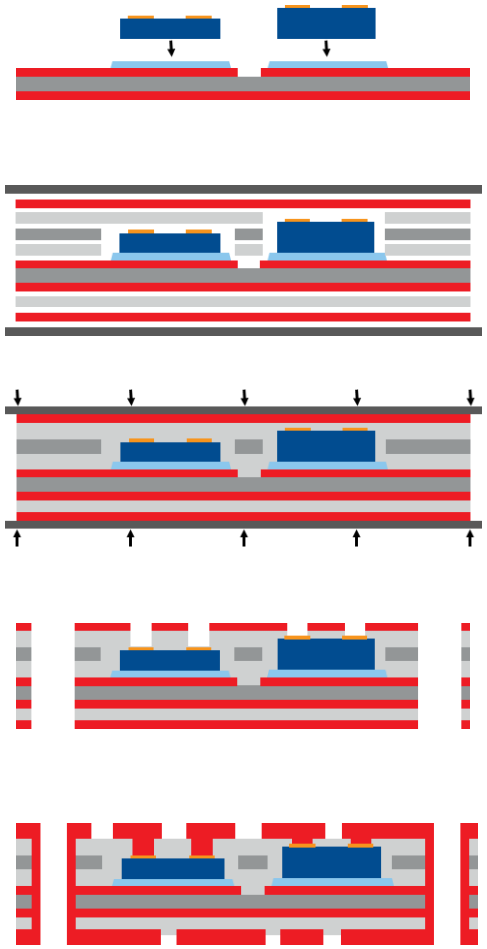
1 **Face-up assembly onto core and into (non-)conductive adhesive**

2 **Multilayer lay-up incl. cavities for components**

3 **Multilayer lamination - cavities will be filled**

4 **Laser drilling onto metal pads of the components**

5 **Electroplating and remaining process steps of the PCB**



EMBEDDING TECHNOLOGY – THE BASICS

Process flows – FLIP-CHIP.**embedding**

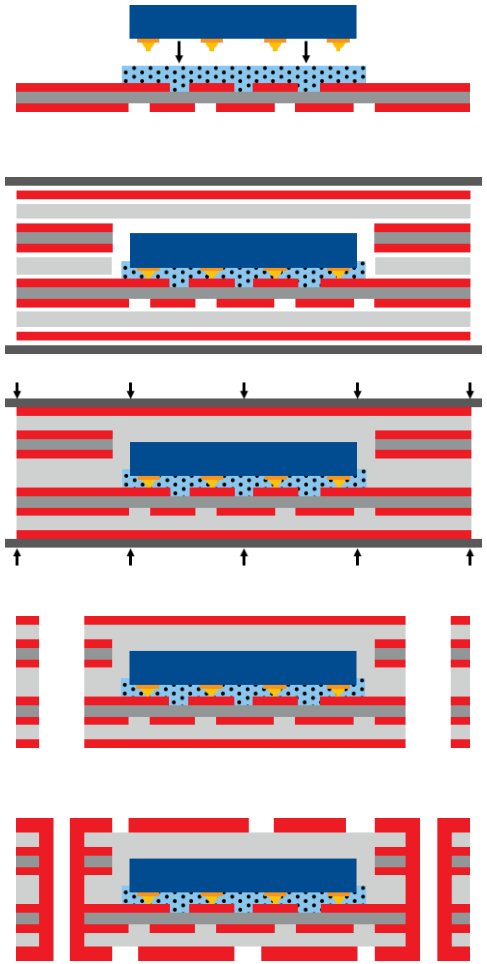
1 **Face-down assembly onto core and into anisotropic-conductive adhesive**

2 **Multilayer lay-up incl. cavities for components**

3 **Multilayer lamination - cavities will be filled**

4 **Further PCB processes such as mechanical drilling**

5 **Electroplating and remaining process steps of the PCB**



EMBEDDING TECHNOLOGY – THE BASICS

Process flows – SOLDER.**embedding**

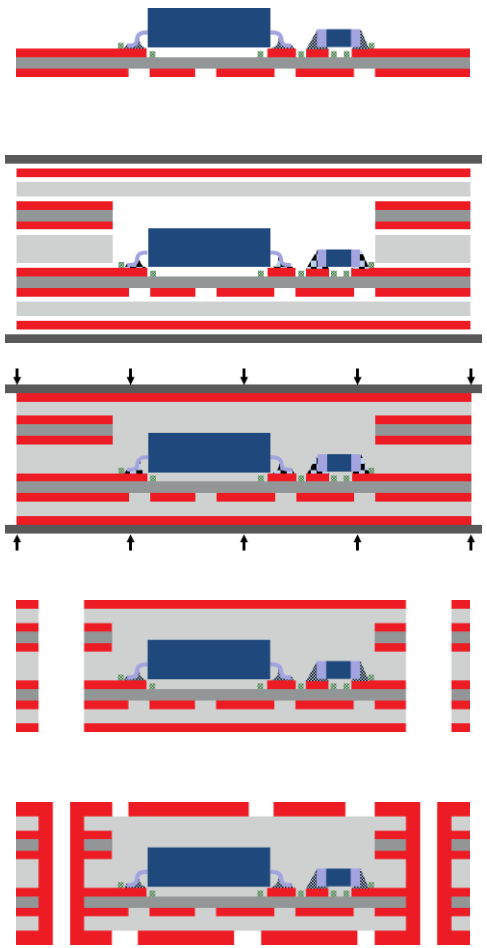
1 **Solder assembly – SAC305-paste or high-temperature paste**

2 **Multilayer lay-up incl. cavities for components**

3 **Multilayer lamination - cavities will be filled**

4 **Further PCB processes such as mechanical drilling**

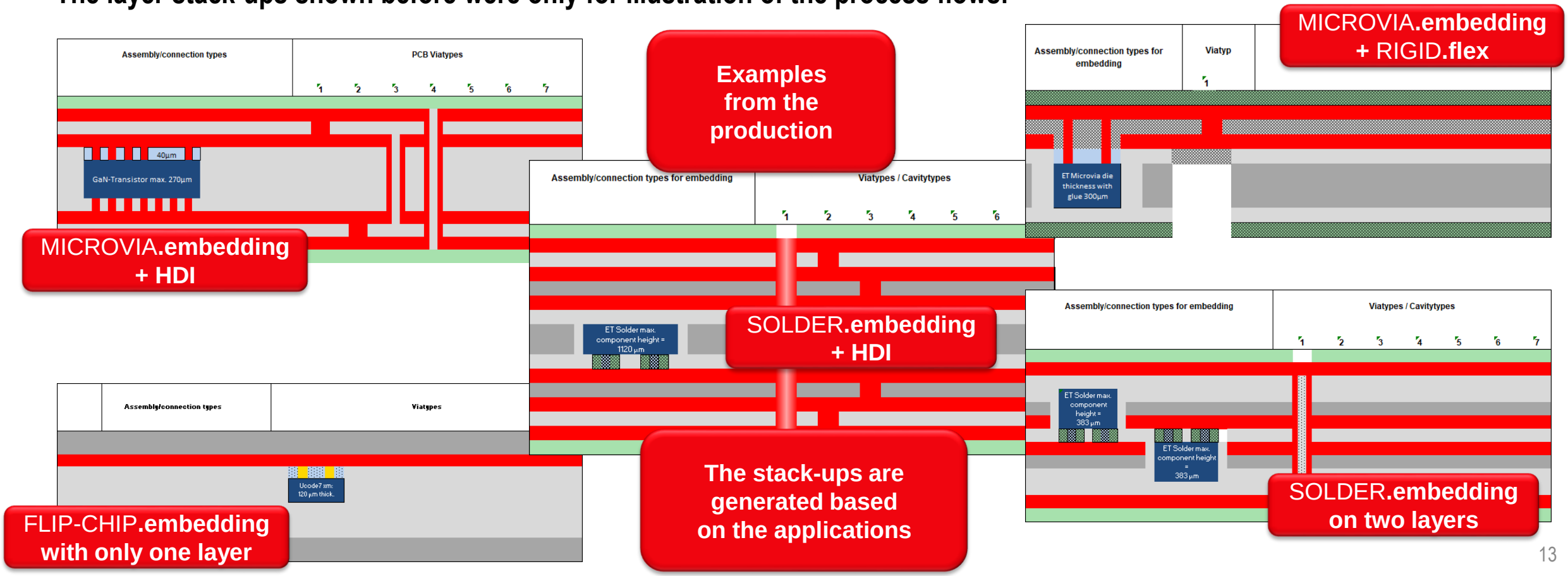
5 **Electroplating and remaining process steps of the PCB**



EMBEDDING TECHNOLOGY – THE BASICS

Process flows – Layer Stack-Ups

The layer stack-ups shown before were only for illustration of the process flows!



EMBEDDING TECHNOLOGY – THE BASICS

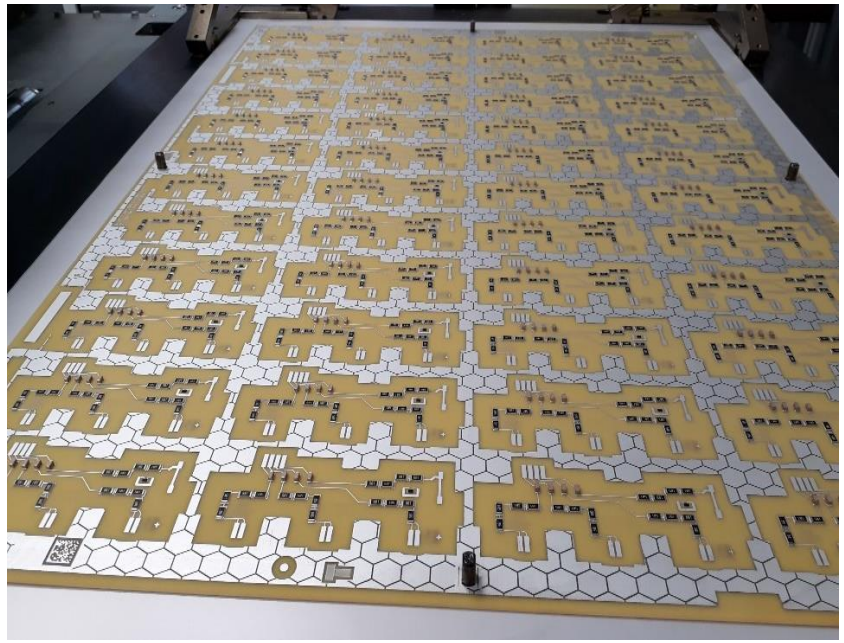
Process flows – Special Assembly Processes

- **No in-house assembly line at WE**
- **Fully qualified and audited partner in use**
- **2nd source partner is currently being built up**

Assembly Challenges for Embedding

- **Assembly formats of WE:**
  - 460 mm x 305 mm
  - 610 mm x 460 mm
- **Min. substrate thicknesses**
  - 70 µm Cu-foils
  - 100 µm FR4-cores

View of the assembly lines of our partner



Assembled inner layer core (610 x 460 mm²)

Own logistics concept

Qualification and audit according to VDA 6.3

AGENDA

EMBEDDING TECHNOLOGY – THE BASICS

Which embedding variant should be used?

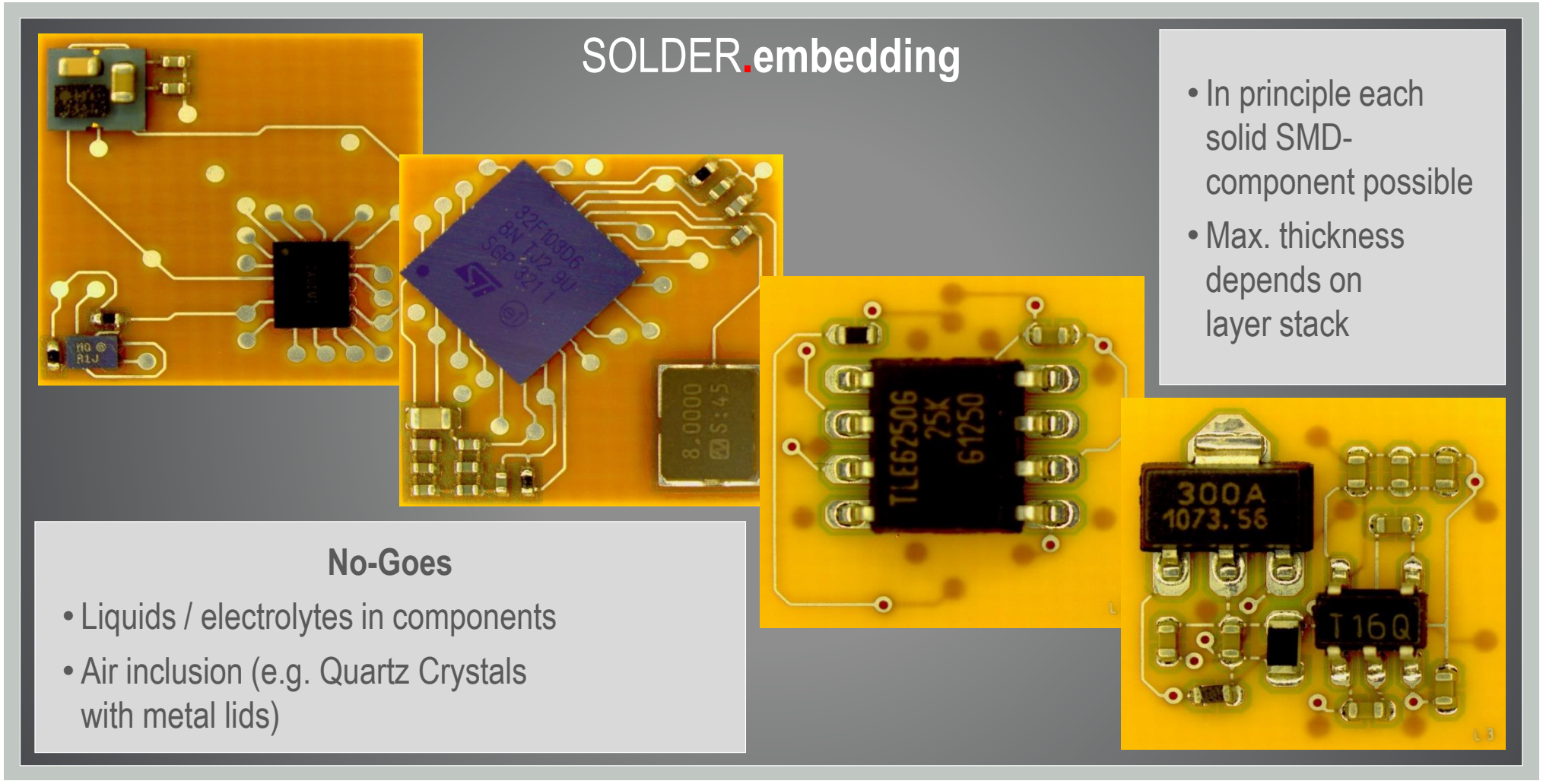
In 95% of the cases, this is being decided by the application or the components themselves ☺

Questions to be asked:

- **In which form are the components available?**
  - SMD components ⇨ SOLDER.**embedding**
  - Bare Dies or components offering pads to be connected with Cu ⇨ MICROVIA.**embedding**
  - Bare Dies with Au-Bumps ⇨ FLIP-CHIP.**embedding**
- **If you might want to use a different technology:**
  - Can the component be sourced or manufactured in the required configuration, e.g. an IC with copper pads instead of AlSiCu (common for wire bonding)?
- **Or do I have to mix the technologies?**
  - unfavourable but doable

EMBEDDING TECHNOLOGY – THE BASICS

Which components are suitable for which variant?

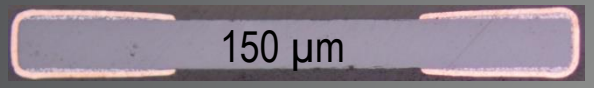


EMBEDDING TECHNOLOGY – THE BASICS

Which components are suitable for which variant?

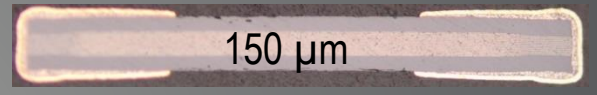
MICROVIA.embedding

resistors



Passive components with Cu-termination

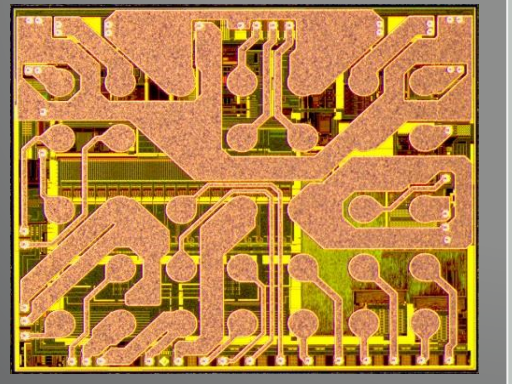
capacitors



Bare die ICs

IC pad metallization

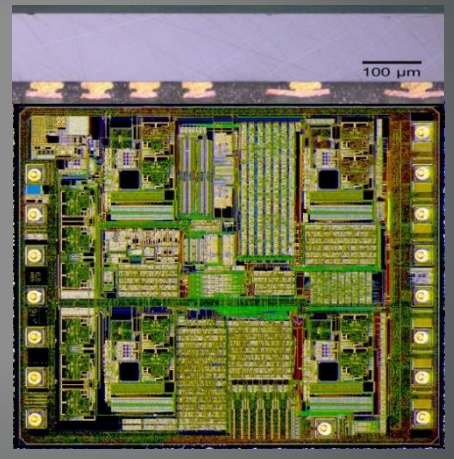
- Copper
- Nickel-Palladium



FLIP-CHIP.embedding

IC pad configuration

- Wire bonded Au stud bumps
- Wafer-level Au bumps



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1 Variants of the Embedding Technology

2 Process flows

3 Criteria for selecting the appropriate embedding variant

4 **Design rules**

5 Workflow of an ET project

EMBEDDING TECHNOLOGY – THE BASICS

Design rules

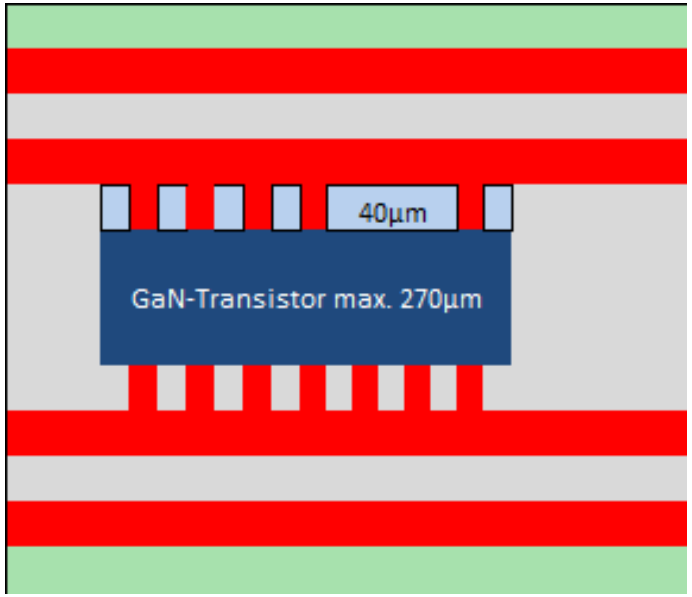
- Design Guide with description, hints and rules available, either printed or online
- All PCBs with embedded components are based on these Design Guides:
  - Basic Design Guide,
  - HDI Design Guide,
  - Flex-Rigid Design Guide and
  - Thermal Management Design Guide

  depending on the used technologies
- Available from your trusted manufacturer

EMBEDDING TECHNOLOGY – THE BASICS

Design rules

Specific features that are NOT included in the Design Guide so far:



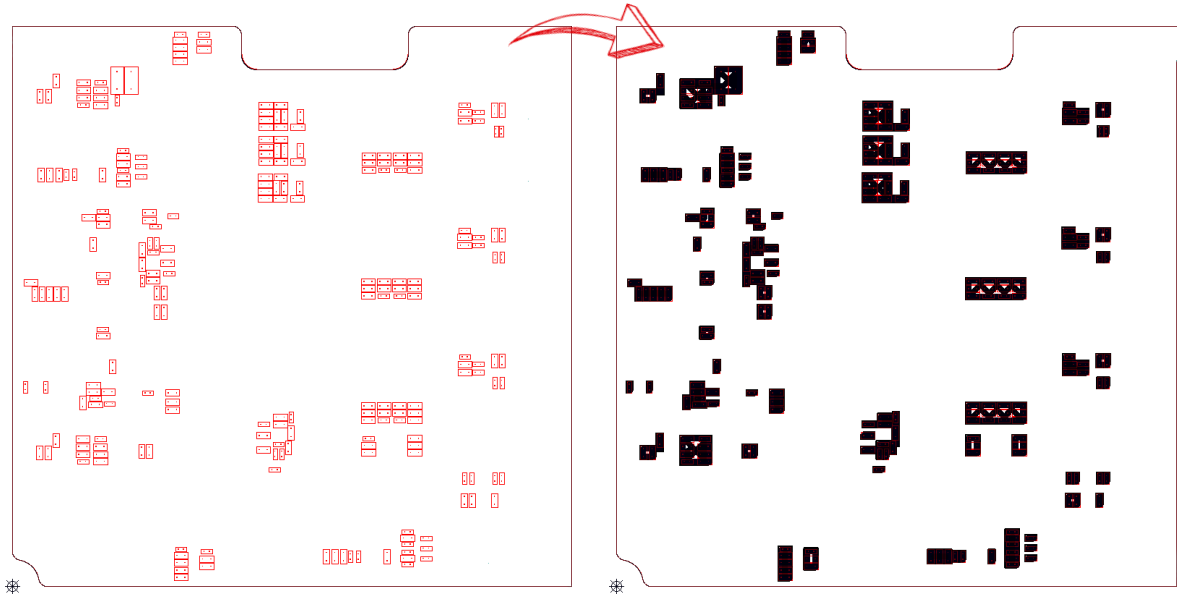
- **PCB thickness - according to our general PCB specification**
  - Default thickness: 2,4 mm
  - Upon Request: 3,2 mm
  - In special cases: >3,2 mm (needs to be evaluated for specific applications)
- **Layer stack-up**
  - At least one layer of prepreg should always be inserted between the component and the copper layer above
  - Based on assembly technology and layer stack, the max. thickness of the components is calculated
  - The WE stack-up proposal specifies the maximum component height - or references the maximum component height
- **Component height**
  - All components must fit into the stack-up
  - No component may protrude in the z-axis

EMBEDDING TECHNOLOGY – THE BASICS

Design rules

Specific features that are NOT included in the Design Guide so far:

- **Occupation of an inner layer with components**
  - Max. 40% of the available area
  - Individual clarification necessary with >40% occupancy
- **Components should be grouped**
- **Distance group to group or component to group:**
  - Min. 1.000 µm
  - 700 µm available upon request and after clarification



Placement of components

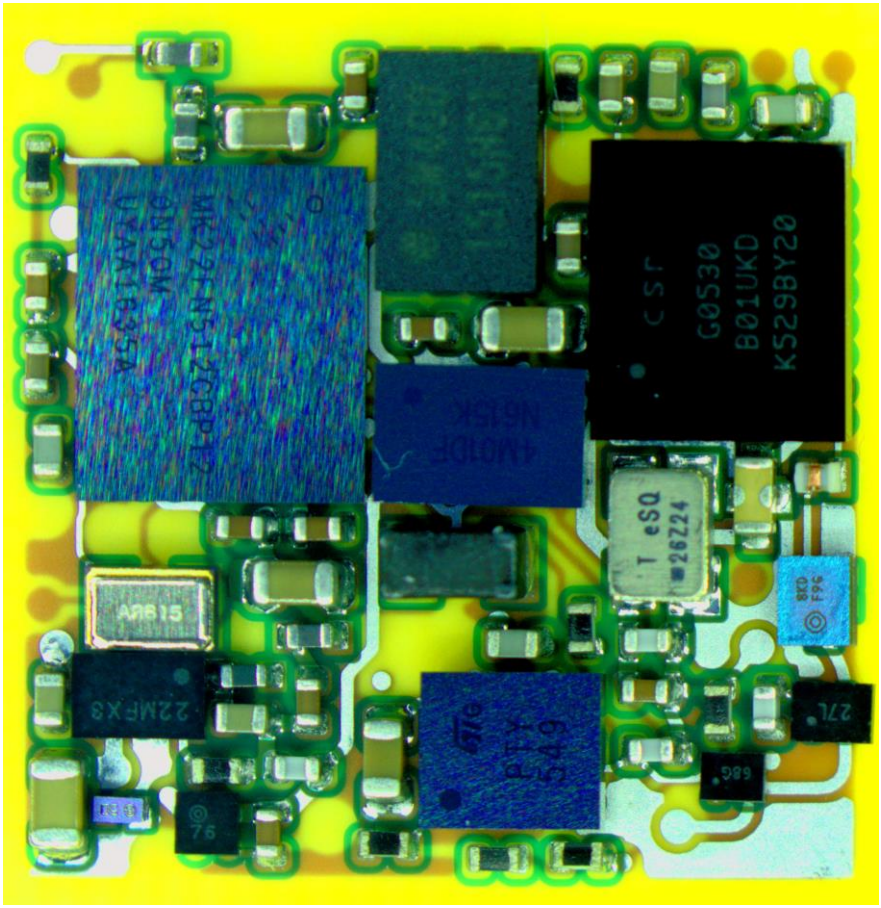
Routing program of prepreg

EMBEDDING TECHNOLOGY – THE BASICS

Design rules

Specific features that are NOT included in the Design Guide so far:

- **Distance component to PCB outline**
  - ≥ 500 µm (less possible upon request and after clarification)
- **Distance via to component outline**
  - ≥ 500 µm (less possible upon request and after clarification)
- **Distance component to component**
  - Pad of the footprint extends beyond the component:
    ≥ 300 µm between the pads
  - Component extends beyond pads:
    ≥ 200 µm between component outlines
  - Smaller distances upon request and after clarification



Tightly packed component group

EMBEDDING TECHNOLOGY – THE BASICS

Short Question

POLL

Which of the three technologies presented is/are of interest to you?

AGENDA

1 Variants of the Embedding Technology

2 Process flows

3 Criteria for selecting the appropriate embedding variant

4 Design rules

5 **Workflow of an ET project**

EMBEDDING TECHNOLOGY – THE BASICS

Procedure for new projects

Required documents and data for initial implementation planning

- **Bill-of-Materials (BOM) of the components to be embedded**
  - incl. all mechanical MAXIMUM dimensions
  - or dimensions incl. all tolerances

Max. dimensions (Z)	Max. Dimensions (X, Y)
0,60 mm	3,00 mm x 3,00 mm
1,20 mm	6,60 mm x 3,10 mm
0,55 mm	1,05 mm x 0,55 mm

Bill-of-Materials

Project / Würth Elektronik Number	WE434797
Index	A
Contact Person	L. Haase
Report Date	31.01.2017
Print Date	24.09.2018
Production Quantity	1.500

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#	Designator (*Reference to P&P)	Description	Quantity	Manufacturer	Manufacturer Part Number	Package/Case	Value	Tolerance	Power Rating	Voltage Rating	Voltage Rating DC	Dielectric	Place Yes/No	Max. dimensions (Z)	Max. Dimensions (X, Y)	Supplied by Customer Yes/No	Comment
0	U3, U4, U5, U6	Gate Drivers 7 Darlington Array 500mA 50V High Volt	4	Diodes Incorporated	ULN2003F12FN-7	UDFN3030-16							Yes	0,60 mm	3,00 mm x 3,00 mm	No	ULN2003 Gate Treiber
1	U1	Timers & Support Products Sgl Prec Timer	1	Texas Instruments	NE555PWR	TSSOP-8							Yes	1,20 mm	6,60 mm x 3,10 mm	No	NE555 Timer
2	C2	Multilayer Ceramic Capacitors MLCC - SMD/SMT 0402 2.2uF 16volts X6S 10%	1	TDK	C1005X6S1C225K050BC		2,2uF	10%		16V		X6S	Yes	0,55 mm	1,05 mm x 0,55 mm	No	CAP 2,2uF
3	D1	TVS Diodes - Transient Voltage Suppressors SOD-923 ESD PROT	1	ON Semiconductor	ESD9X5.0ST5G	SOD-923							Yes	0,43 mm	1,05 mm x 0,65 mm	No	TVS Diode
4	R1	Thick Film Resistors - SMD 0402 64.9Kohms 1% 0.1W AEC-Q200	1	Panasonic	ERJ-2RKF6492X	0402 (1005 metric)	64K9	1%	100mW	50V			Yes	0,40 mm	1,05 mm x 0,55 mm	No	RES 64K9
5	R2	Thick Film Resistors - SMD 0402 40.2ohms 1% AEC-Q200	1	Panasonic	ERJ-2RKF40R2X	0402 (1005 metric)	40R2	1 %	100 mW	50 V			Yes	0,40 mm	1,05 mm x 0,55 mm	No	RES 40R2
6	R3	Thick Film Resistors - SMD 0402 120ohms 1% AEC-Q200	1	Panasonic	ERJ-2RKF1200X	0402 (1005 metric)	120	1 %	100 mW	50 V			Yes	0,40 mm	1,05 mm x 0,55 mm	No	RES 120R
7	C1, C3	Multilayer Ceramic Capacitors MLCC - SMD/SMT 0402 0.1uF 10volts X7R 20%	2	Yageo	CC0402KRX7R6BB104	0402 (1005 metric)	100nF	10%		10V		X7R	Yes	0,55 mm	1,05 mm x 0,55 mm	No	CAP 100nF
8	LED1, LED2, LED3, LED4, LED5, LED6,	Standard LEDs - SMD	24	OSRAM Opto	LS Q976-NR-1	0603 (1608							Yes	0,90 mm	1,70 mm x 0,90 mm	No	LED Rot

EMBEDDING TECHNOLOGY – THE BASICS

Procedure for new projects

Required documents and data for initial implementation planning

- **The BOM is analyzed by WE regarding the "embeddability" of the components:**

Quantity	Designator	Comment	Description	Footprint	manufacturer_pn	Tolerance	voltage	Length	Width	Height	Max. Height
6	C1,C3, C8, C11, C13, C16	10µ	10µF, 16V, AEC-Q200, Flexterm, X7S	C0805	CGA4J1X7S1C106M125 AE	20%	16V	2,000 mm ± 0,450 mm	1,250 mm ± 0,250 mm	1,250 mm ± 0,250 mm	1,500 mm
8	C2,C4, C9, C14, C15, C17, C18, C21	100n	AEC-Q200 FlexTerm	C0603	CGA3E3X8R1H104K080 AE	10%	50V	1,600 mm ± 0,200 mm	0,800 mm ± 0,150 mm	0,800 mm ± 0,150 mm	0,950 mm
3	C5,C19, C20	1u	AEC-Q200 FlexTerm	C0805	08055C105K4Z2A	10%	50V	2,010 mm ± 0,200 mm	1,250 mm ± 0,200 mm	1,400 mm ± 0,000 mm	1,400 mm
2	C6,C7	10u	AEC-Q200, FlexTerm	C0805	JMJ212CB7106KGHT	10%	6.3V	2,000 mm ± 0,250 mm	1,250 mm ± 0,250 mm	1,250 mm ± 0,250 mm	1,500 mm
1	C10	100n	SMD C1206, X7R, AEC-Q(200), VPE 10.000	C1206	CL31B104KBP5PNF	±10 %	50 V	3,200 mm ± 0,200 mm	1,600 mm ± 0,200 mm	1,600 mm ± 0,200 mm	1,800 mm
1	C12	33n	33n, 25V, X7R, 0402, AEC-Q200	C0402	CGA2B1X7R1E333M05 0BC	20%	25V	1,000 mm ± 0,050 mm	0,500 mm ± 0,050 mm	0,500 mm ± 0,050 mm	0,550 mm
2	D1, D2	CDSOT23-SM712	TVS Diode 7/12V	SOT-23-3	CDSOT23-SM712			2,900 mm ± 0,100 mm	2,300 mm ± 0,200 mm	1,030 mm ± 0,140 mm	1,170 mm
1	D3	SM15T22CAY	AEC-Q101	SMC_DO-214AB	SM15T22CAY			7,950 mm ± 0,200 mm	5,900 mm ± 0,350 mm	2,300 mm ± 0,350 mm	2,650 mm
1	IC1	LTM8029	36VIN, 600mA Step-Down µModule Converter with 5µA Quiescent Current	BGA-35_6.25x11.25_1.27mm_Linear_05-12-1878				11,250 mm ± 0,000 mm	6,250 mm ± 0,000 mm	3,420 mm ± 0,200 mm	3,620 mm
1	IC2	ISOW7841		SOIC-16W	ISOW7841DWER			10,300 mm ± 0,200 mm	10,300 mm ± 0,330 mm	2,650 mm ± 0,000 mm	2,650 mm
1	IC3	AMC1306M05	High Precision Reinforced Isolated Delta-Sigma Modulator	SOIC-8W_TI-DWV	AMC1306M05DWV			11,500 mm ± 0,250 mm	5,850 mm ± 0,100 mm	2,800 mm ± 0,000 mm	2,800 mm
1	IC4	LP38693QSD-3.3/NOPB	LDO, 2.7V to 10V, 330mV Dropout, 3.3Vout, 0.5Aout, AEC-Q100	WSON-6_NGG0006A_Texas_Instruments	LP38693QSD-3.3/NOPB			3,000 mm ± 0,100 mm	3,000 mm ± 0,100 mm	0,80 mm ± 0,000 mm	0,800 mm
1	IC5	SN65HVD77		VSSOP8_DGK	SN65HVD77DGKR			4,900 mm ± 0,150 mm	3,000 mm ± 0,100 mm	1,100 mm ± 0,000 mm	1,100 mm
3	L1, L2, L3	1k5 @ 100MHz	Chip Ferrit, 1 A, 1.5 kOhm @ 100 MHz	L0805	742792097			2,000 mm ± 0,200 mm	1,200 mm ± 0,200 mm	0,900 mm ± 0,200 mm	1,100 mm
1	L4	10u	SMDL0805, Isat= 200 mA, DCR= 611 mOhm	L0805	MLZ2012M100WT000			2,000 mm ± 0,200 mm	1,250 mm ± 0,200 mm	1,250 mm ± 0,200 mm	1,450 mm
1	R1	154k	AEC-Q200	R0603	CRCW0603154KFKEA	1%	75V	1,550 mm ± 0,10 mm	0,850 mm ± 0,100 mm	0,450 mm ± 0,050 mm	0,500 mm
1	R2	316k	SMD R0603, AEC-Q200	R0603	ERJ-3EKF3163V	±1 %	75 V	1,600 mm ± 0,150 mm	0,850 mm ± 0,10 mm	0,450 mm ± 0,100 mm	0,550 mm
2	R3, R5	ERJ-2RKF43R0X	RES SMD 43 OHM 1% 1/10W 0402	SMD-0402-RES	ERJ-2RKF43R0X	±1%		1,000 mm ± 0,050 mm	0,500 mm ± 0,050 mm	0,350 mm ± 0,050 mm	0,400 mm
4	R6, R8, R9, R10	10R	Anti-Surge, AEC-Q200	R0603	ESR03EZPJ100	5%	150V	1,600 mm ± 0,100 mm	0,800 mm ± 0,100 mm	0,450 mm ± 0,100 mm	0,550 mm
1	R7	100R	AEC-Q200	R1206	CRCW1206100RFKEA	1%	200V	3,150 mm ± 0,150 mm	1,600 mm ± 0,150 mm	0,550 mm ± 0,050 mm	0,600 mm
1	X1	G125-MS10605M1		G125-MS10605m1	G125-MS10605M1						

EMBEDDING TECHNOLOGY – THE BASICS

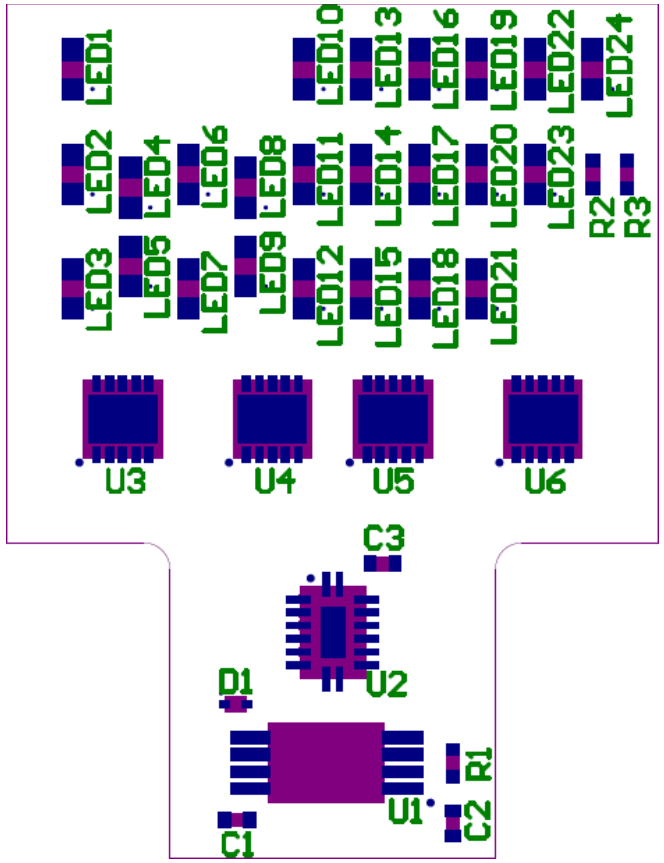
Procedure for new projects

Required documents and data for initial implementation planning

- **Data for the inner layer assembly**
  - Planned/desired assembly drawing of the inner layer
  - incl. outlines of the contacts protruding the body e.g. Gull-Wing- und J-Leads

⇨ Serves the group planning incl. occupancy and distances

⇨ Assembly drawing serves as occupancy drawing as well



Assembly or occupancy drawing

EMBEDDING TECHNOLOGY – THE BASICS

Procedure for new projects

Required documents and data for initial implementation planning

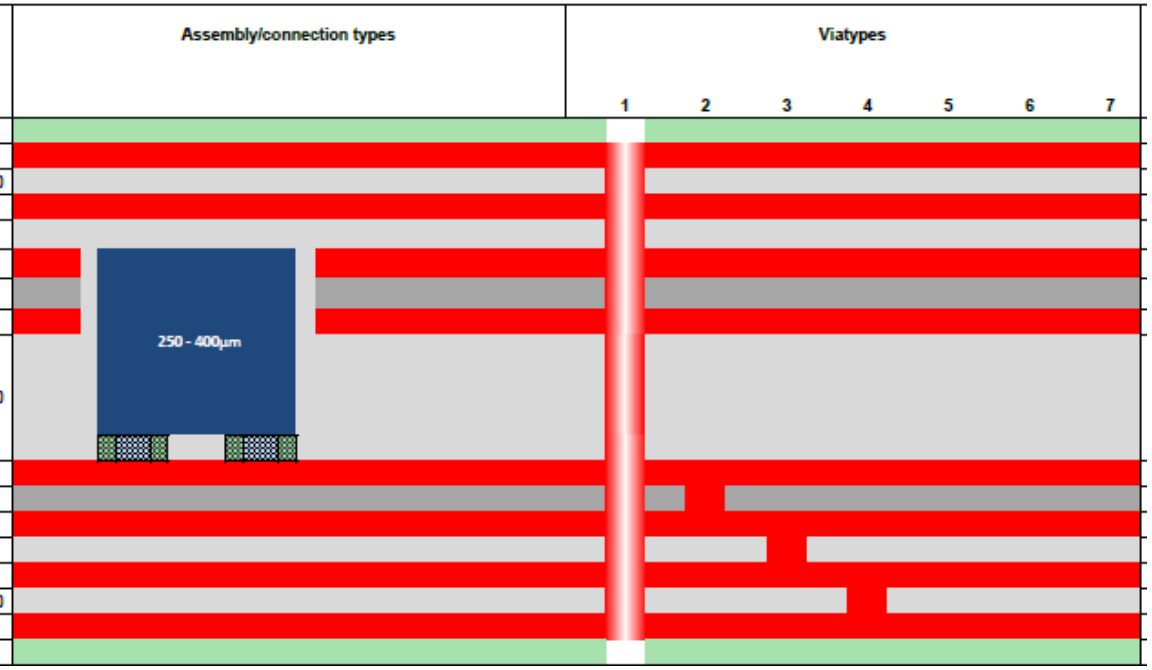
- **Data sets (preferably Extended Gerber or ODB++) and documents with**
  - PCB outline (incl. outline of assembly array if needed)
  - Layout-data (if already available)
  - Required number of layers and the required copper thicknesses
  - Required layer connections/vias
  - Required and predefined layer distances (e.g. for impedances or insulation requirements)
- **Data from the previous board is often helpful**

EMBEDDING TECHNOLOGY – THE BASICS

Procedure for new projects

- **After reviewing and checking all data including components etc., WE creates a layer stack-up according to the required boundary conditions**
- **Based on the stack-up and the agreed components that are ”embeddable”, the layout phase starts**

Rigid area structure	Rigid area thickness	Flex area thickness		Material description	Assembly/connection types	Viatypes 1 2 3 4 5 6 7
Soldermask	15 µm					
L1	35 µm					
	55 µm			FR4 PP TG150		
L2	35 µm					
	55 µm			FR4 TG150		
L3	35 µm					
	100 µm					
L4	35 µm					
	600 µm			FR4 PP TG150		
L5	35 µm					
	100 µm			FR4 TG150		
L6	35 µm					
	55 µm					
L7	35 µm					
	55 µm			FR4 PP TG150		
L8	35 µm					
Soldermask	15 µm					



Example of a layer stack-up with material and via definitions as well as layer distances

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Outlook for Part 2

In the 2nd part of the webinar on March 16, 2021 we will seamlessly continue with the topic “layout”:

- **How to layout printed circuit boards with embedded components?**
- **What do EDA tools already cover today?**
- **How do I create the libraries?**
- **What are the tricks and knacks?**

You will also gain an insight into current applications and projects from the following areas

- **Automotive,**
- **Industrial,**
- **Medical technology,**
- **Aerospace/Sensor Technology and**
- **further application ideas**

Thank you for your attention!

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