PLUGGING – FILLING – TENTING

Andreas Dreher
technical Projectmanagement

WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

TOPIC

Plugging – Filling – Tenting

1. Background for Via Opening in Solder Mask
2. Different Options for protection of Via Structures
3. Description of different options according IPC-4761
4. The correct choice for your PCB

YOUR SPEAKER

Andreas Dreher

Technical Project Management

- HDI-Design
- Signal Integrität & High Speed

Since 2003 at Würth Elektronik CBT

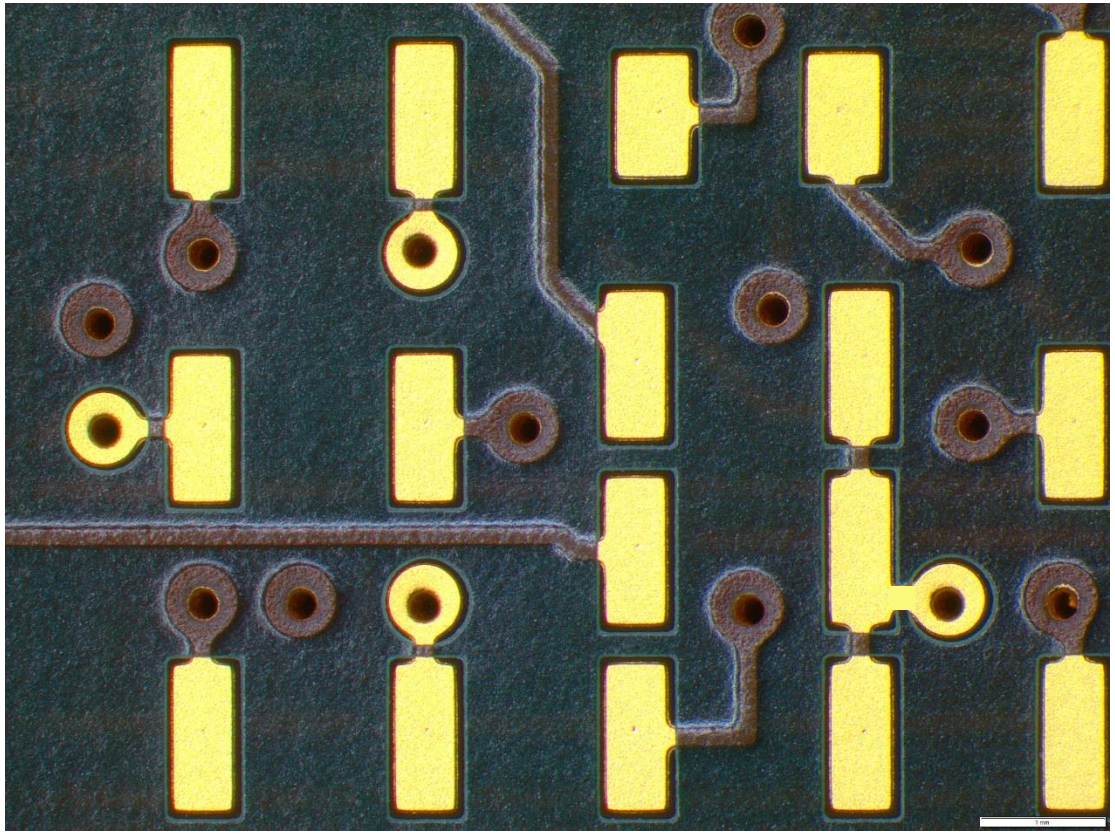
How to reach me :

Phone +49 7622 397-133
Mail andreas.dreher@we-online.com

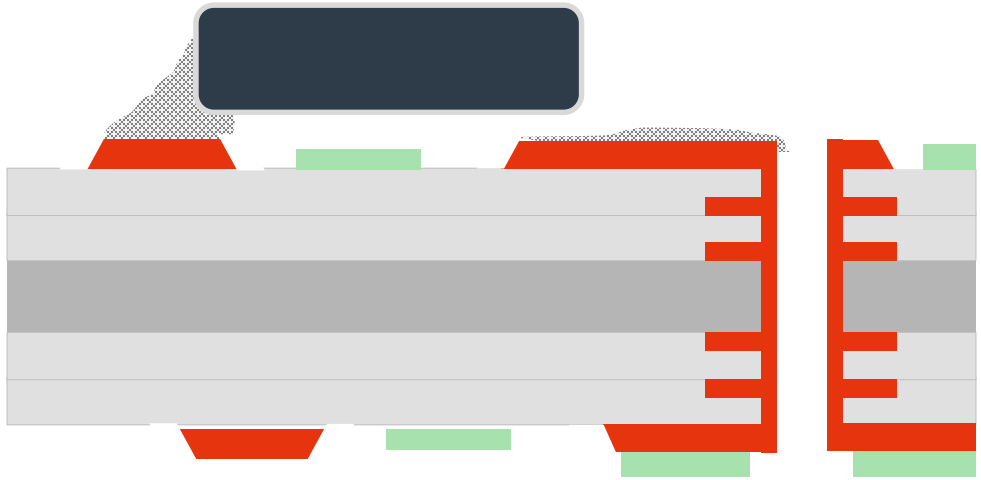
Andreas Dreher
Technisches Projektmanagement

VIA OPENING IN SOLDER MASK

Background



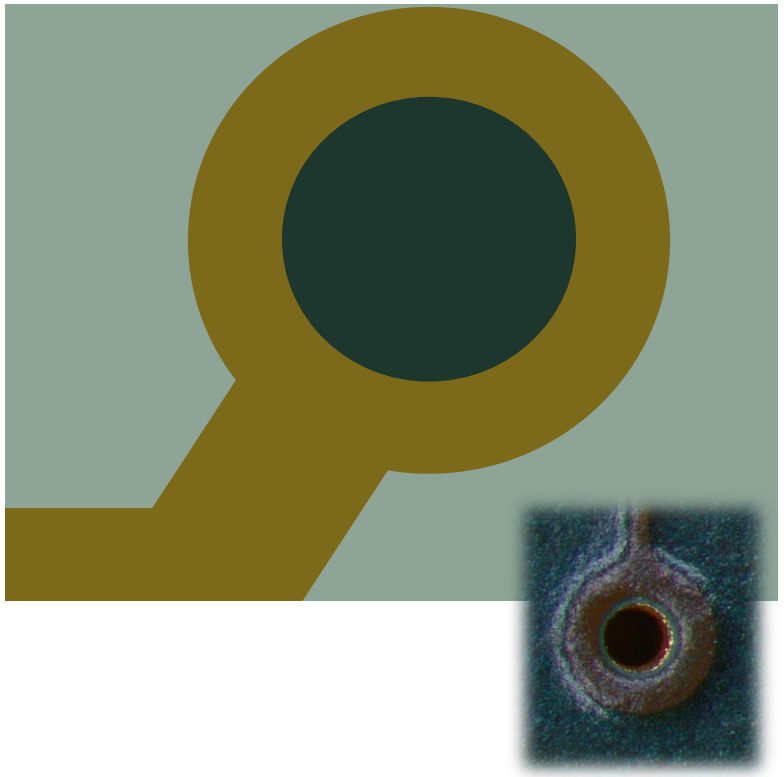
- Prevention of solder from passing through the via
- Creating a defined State of the Via
- Reliable and producable PCB



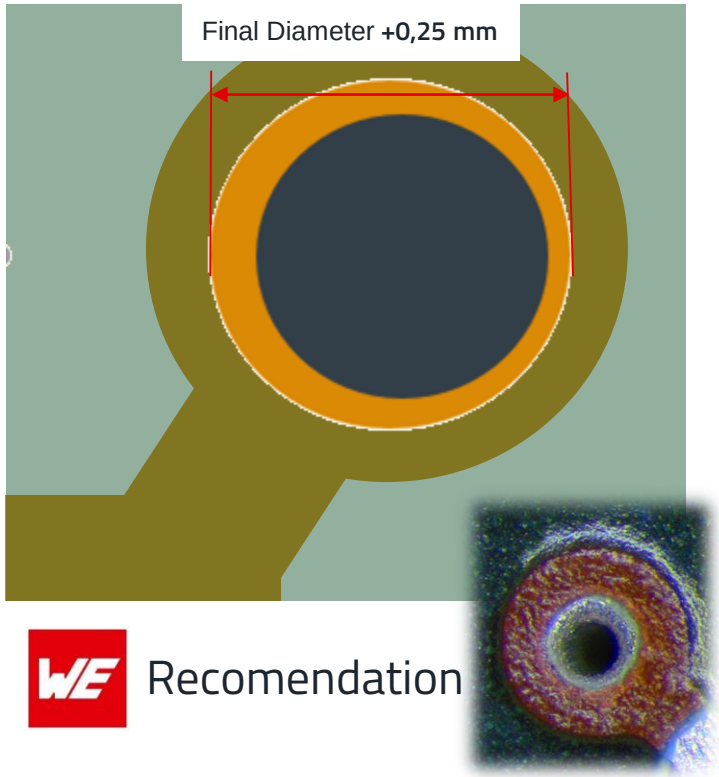
VIA OPENING IN SOLDER MASK

Options

No Clearance

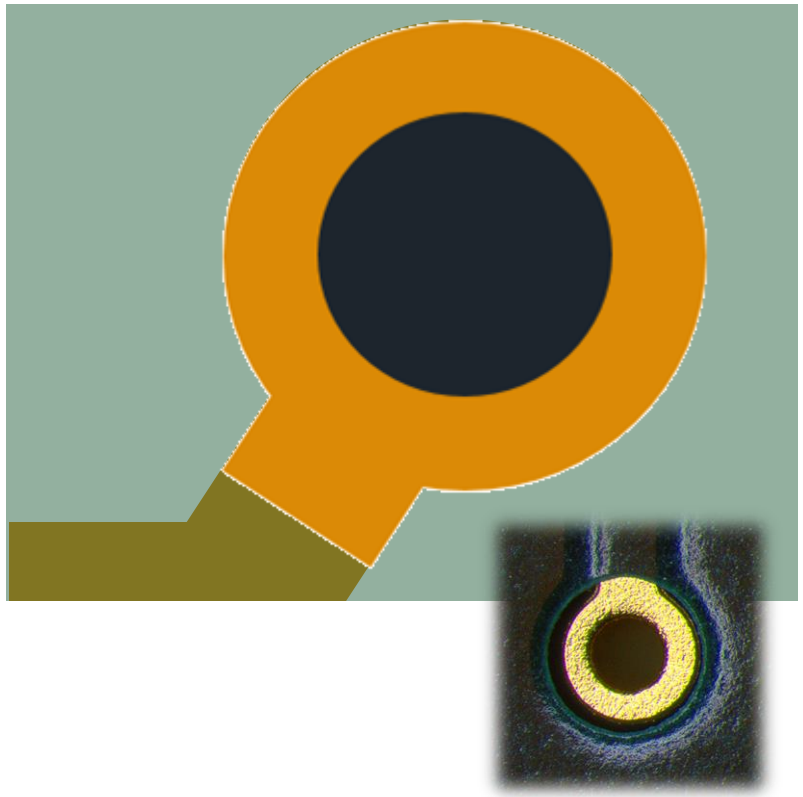


With Center Clearance



Recomendation

Via Land without Solder Mask

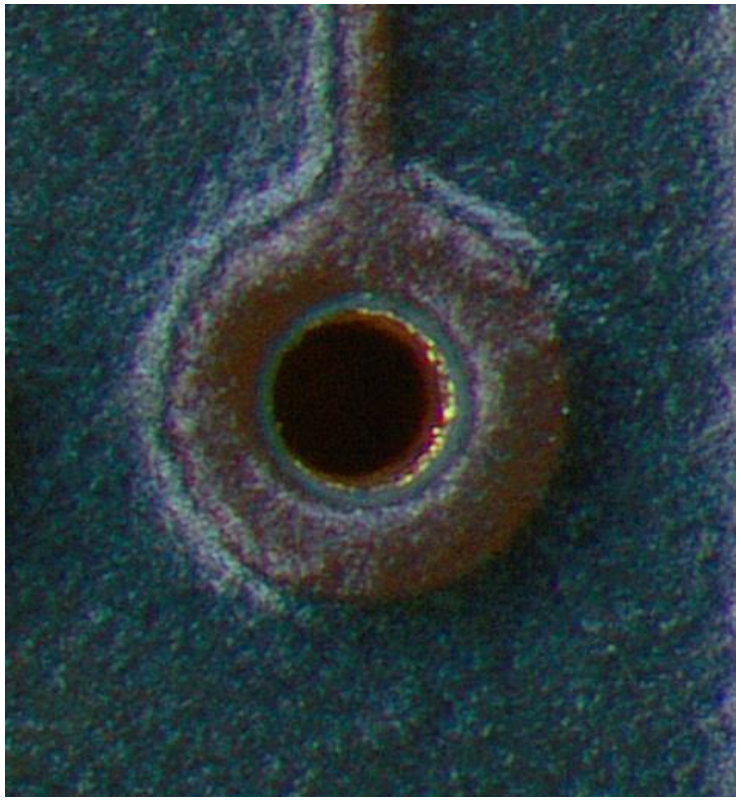


Weitere Details in den Basic Design Rules

VIA OPENING IN SOLDER MASK

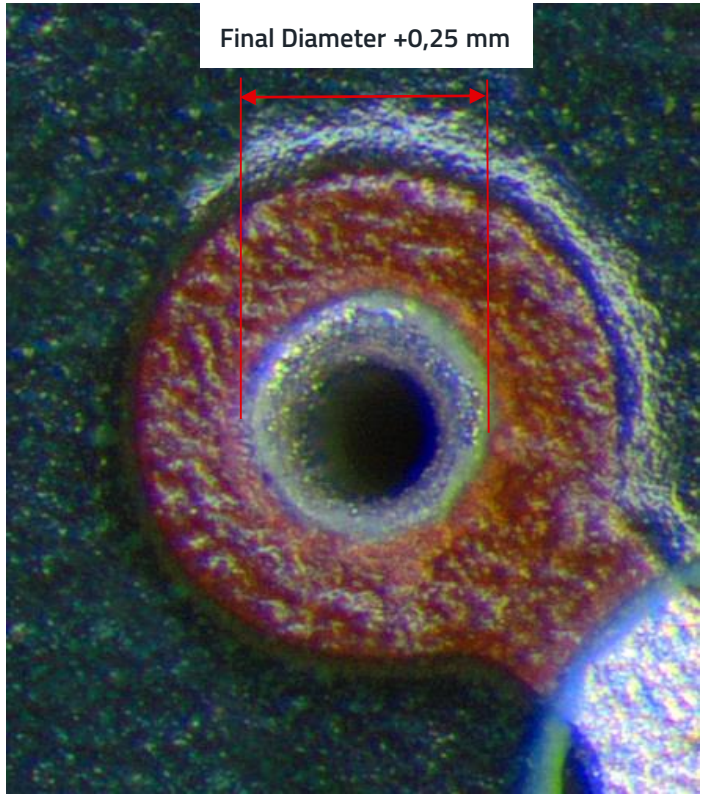
Options

No Clearance



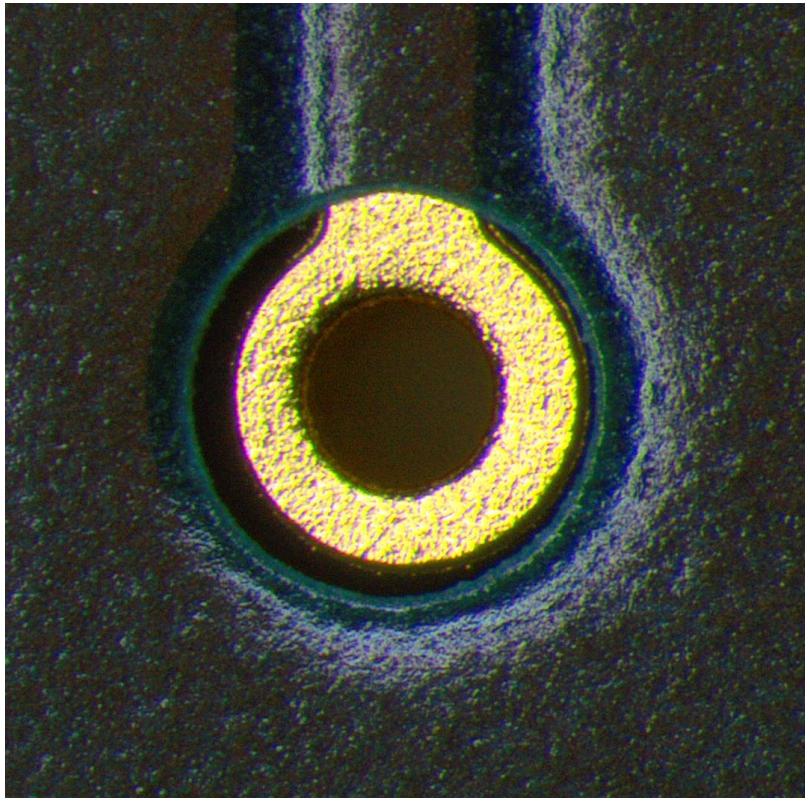
Undefinierter Zustand

With Center Clearance



Empfehlung

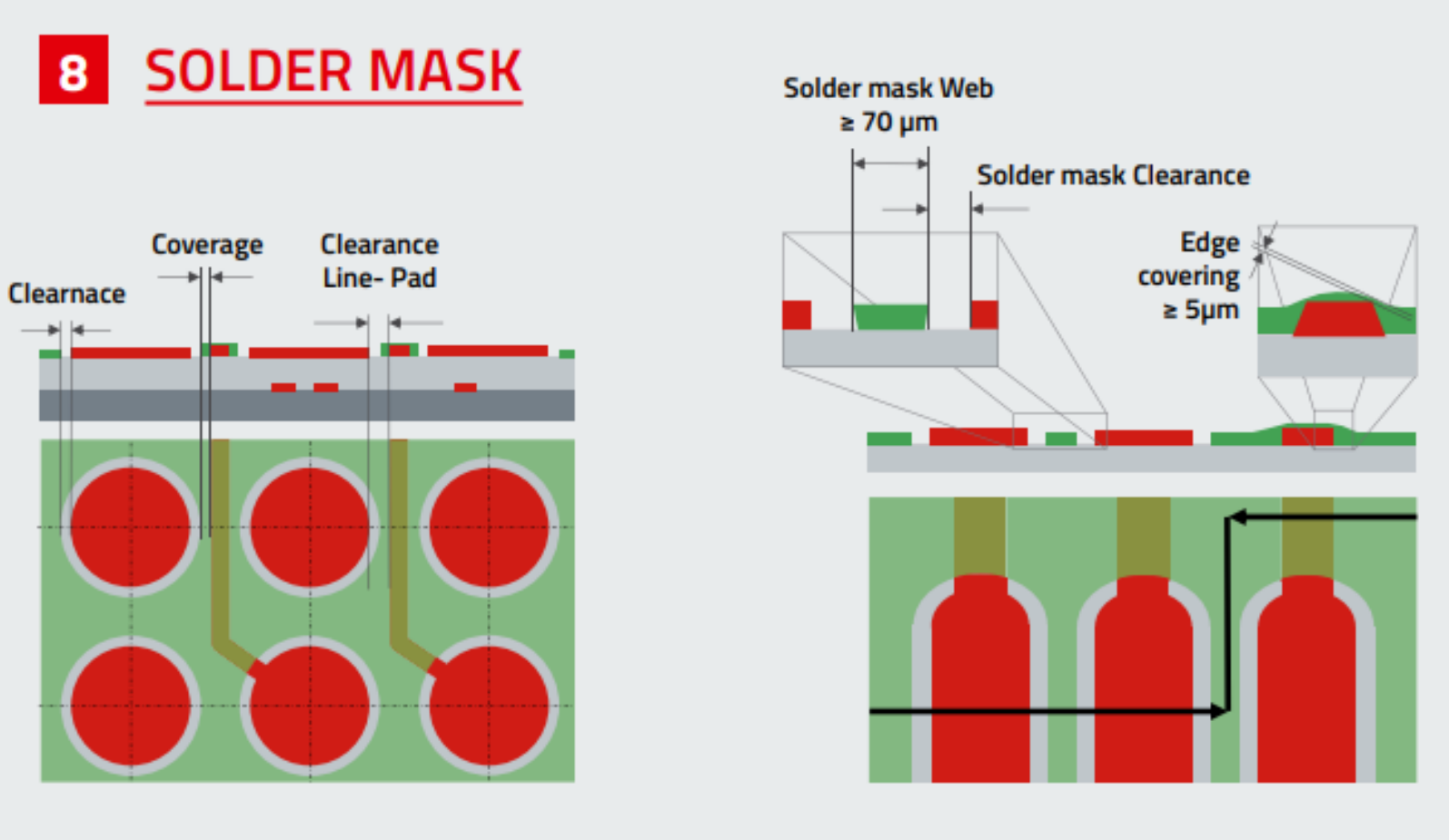
Via Land without Solder Mask



Als Testpunkt nutzbar

SOLDER MASK

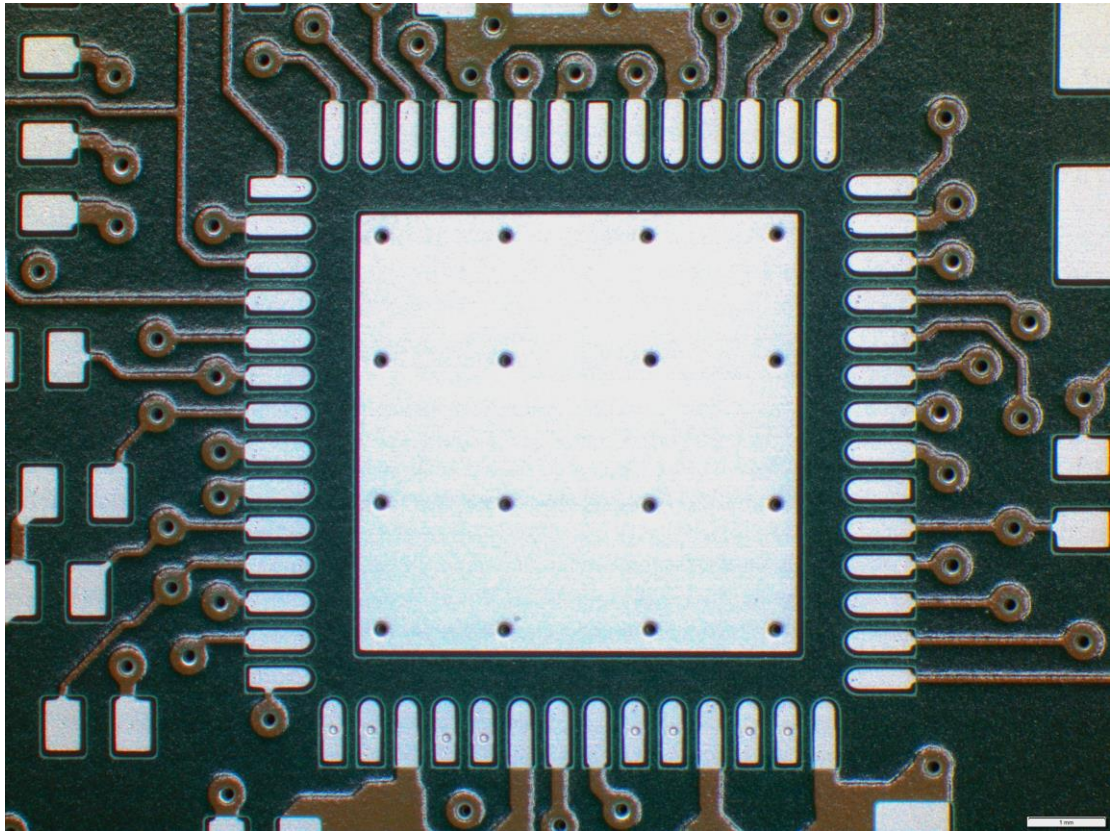
Design Rules



- More Details in the

Basic Design Rules

DIFFERENT OPTIONS FOR PROTECTION OF VIA STRUCTURES



- Prevention of solder from passing through the via
- Creating a defined State of the Via
- Reliable and producable PCB

- Coating or Vakuum-Testing ?

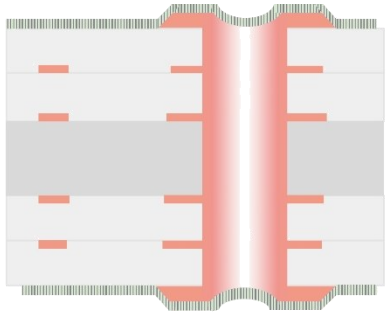
- Via-in-Pad Design ?

- HDI-Designs ?

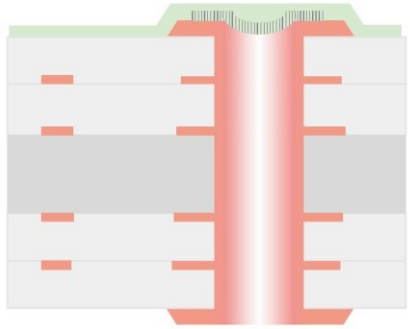
SPECIFIKATION ACCORDING IPC-4761

Design Guide for Protection of Printed Board Via Structures

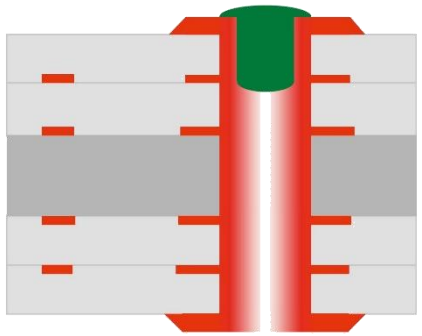
Typ I
Tented Via



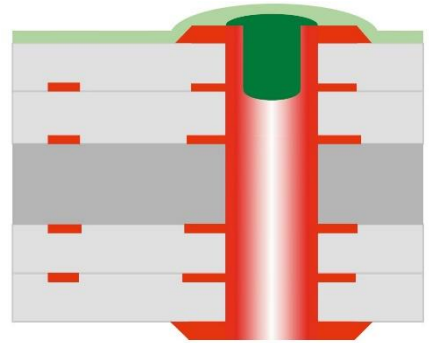
Typ II
Tented & Covered Via



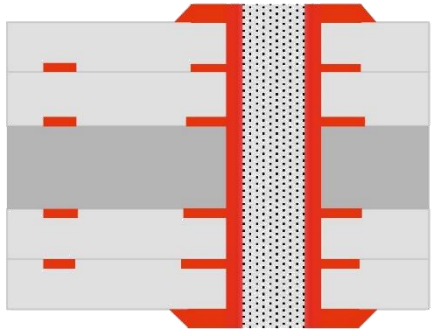
Typ III
Plugged Via



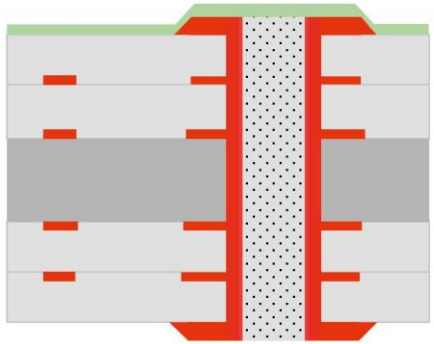
Typ IV
Plugged & Covered Via



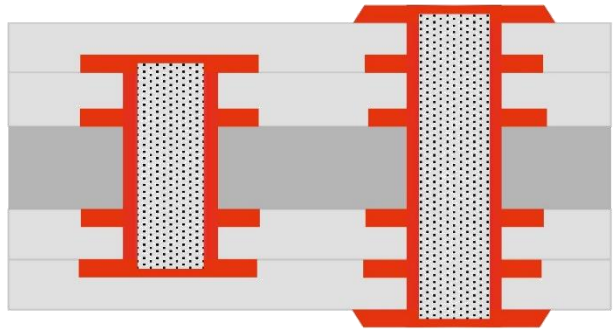
Typ V
Filled Via



Typ VI
Filled & Covered Via

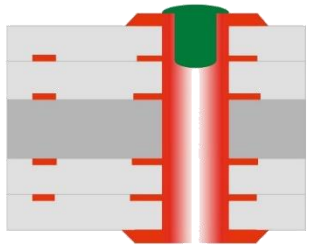


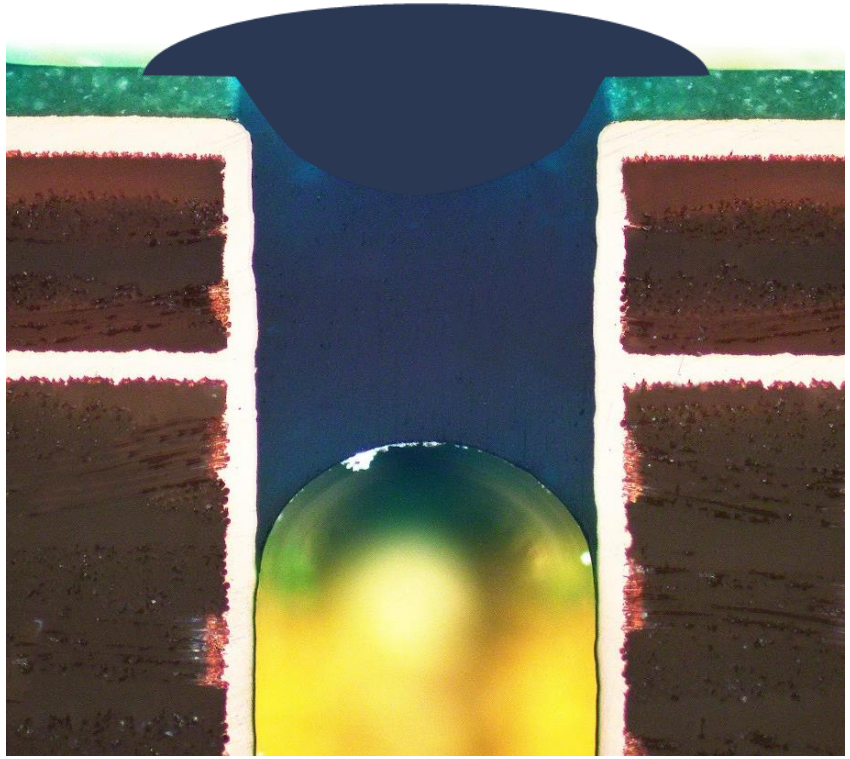
Typ VII
Filled & Capped Via



Typ I-a or Typ I-b describe the usage of single sided or double sided technology

TYP III PLUGGED VIA





A Via with material applied allowing partial penetration into the via

Process	**silc screen printing**
Material	therm. curing ink

Benefit

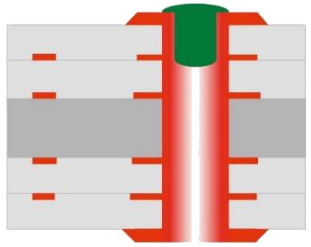
- Vacuum seal for e.g. ICT
- cheap
- Locally selectiv plugging possible

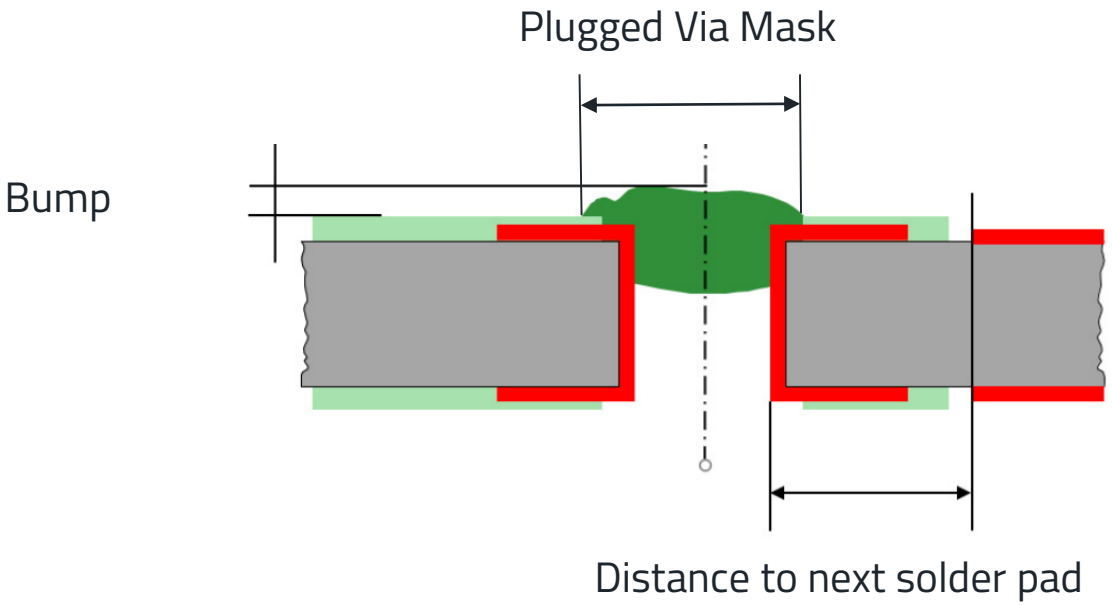
Concern

- Bumps up to 70 µm
- Via-in-Pad technology not possible
- Limited in fine line Designs

TYP III PLUGGED VIA

Design Rules

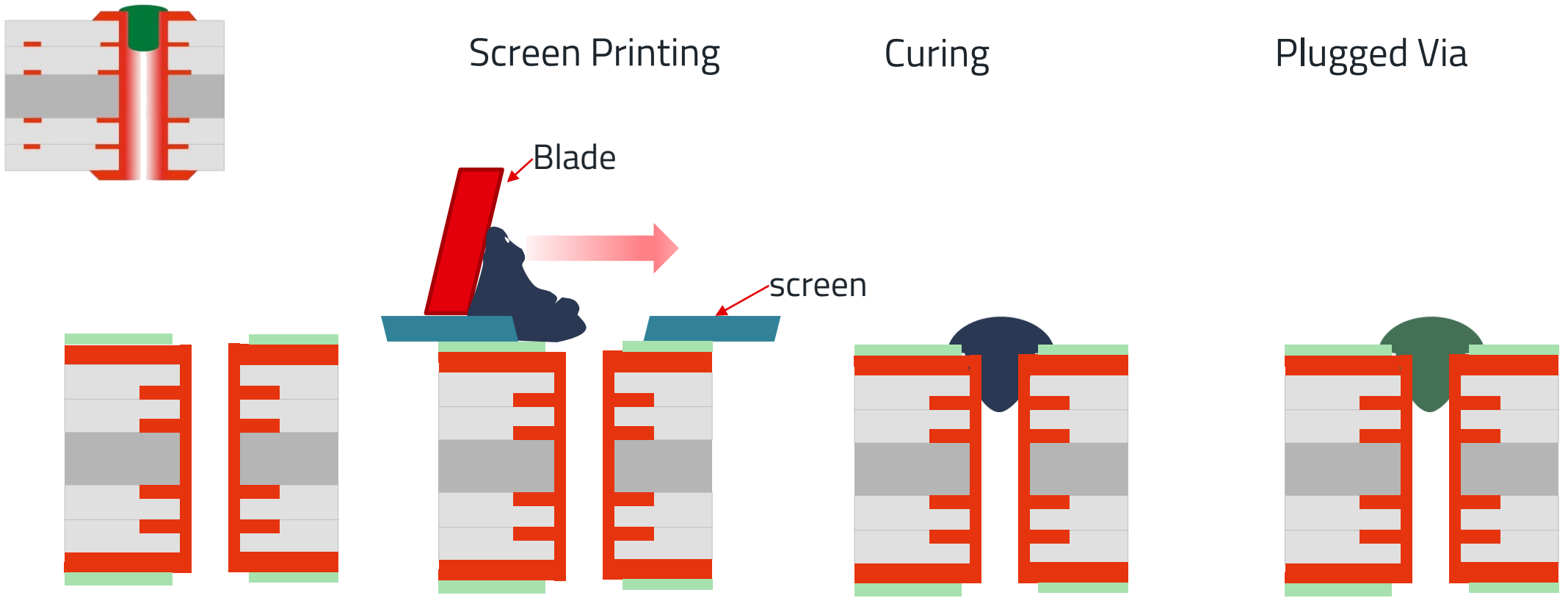




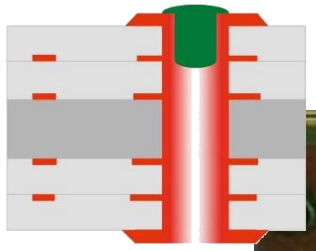
- The Distance to the next solder pad has to be at least 0,15mm on top and botom
- Bumps up to 70 µm over solder mask possible
- For german factory´s:
  double sided plugging is not possible

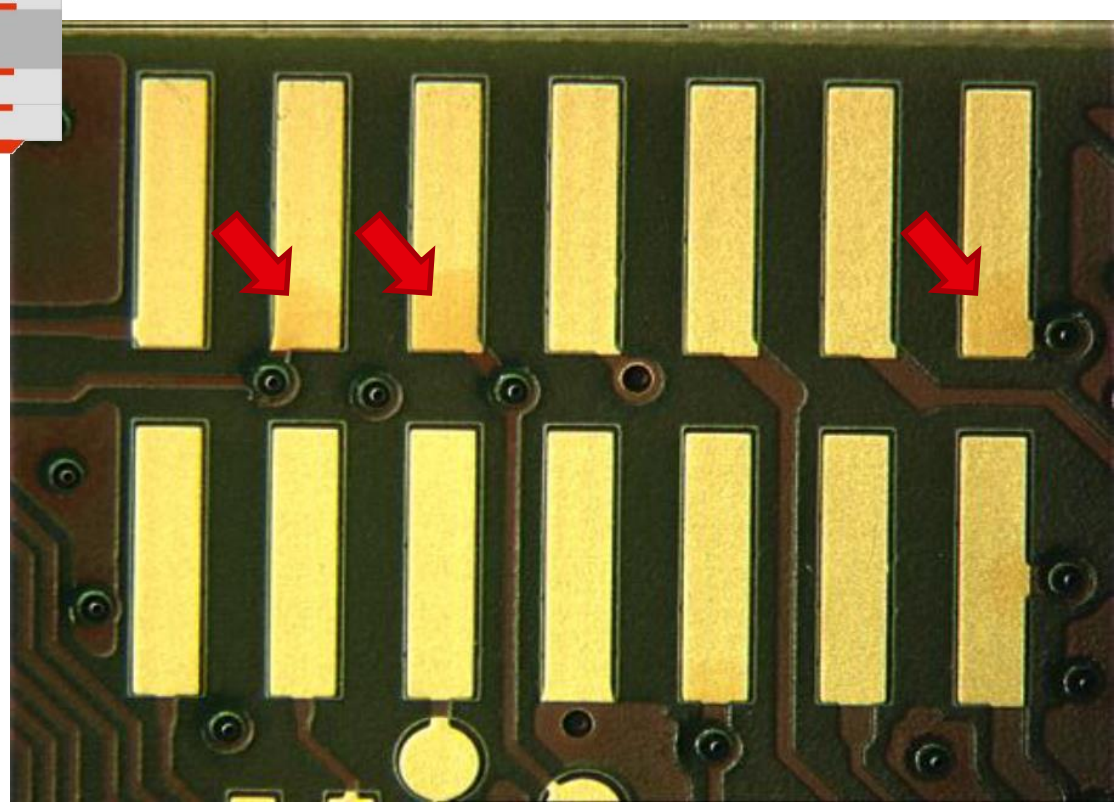
Final Diameter	Size of Plugged Via Mask
≤ 0,30 mm	0,40 mm
≤ 0,40 mm	0,50 mm
0,45 – 0,70 mm	Ø + 0,20 mm
bis 0,80 mm	Ø + 0,30 mm

TYP III-A PLUGGED VIA - PROCESS



DISTANCE TO SMALL TO SOLDER PAD

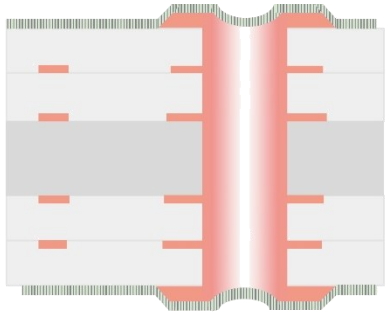




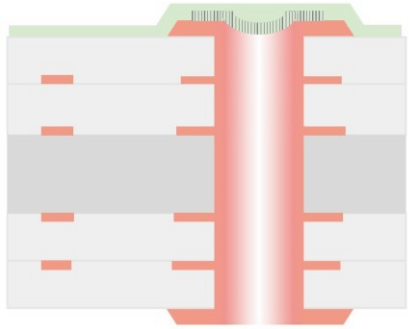
- Risk of Ink contamination to the solder pads
- Discoloration of solder pads possible

SPECIFIKATION ACCORDING IPC-4761

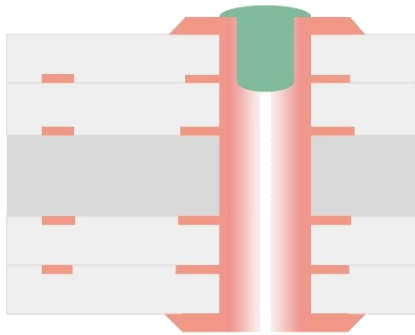
Typ I
Tented Via



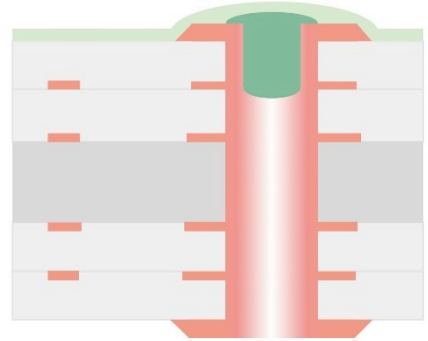
Typ II
Tented & Covered Via



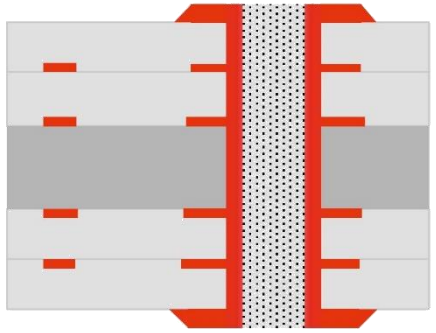
Typ III
Plugged Via



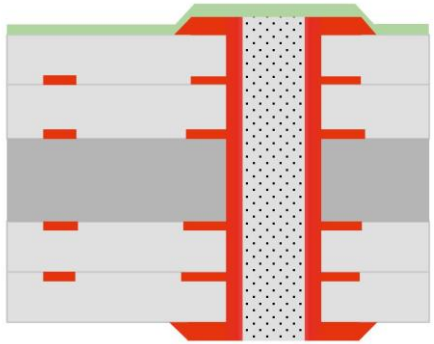
Typ IV
Plugged & Covered Via



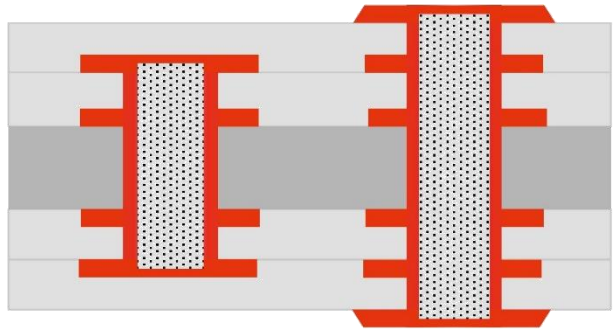
Typ V
Filled Via



Typ VI
Filled & Covered Via

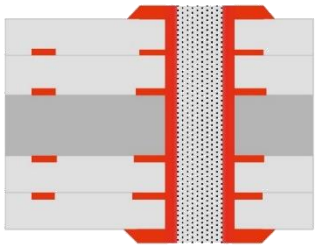


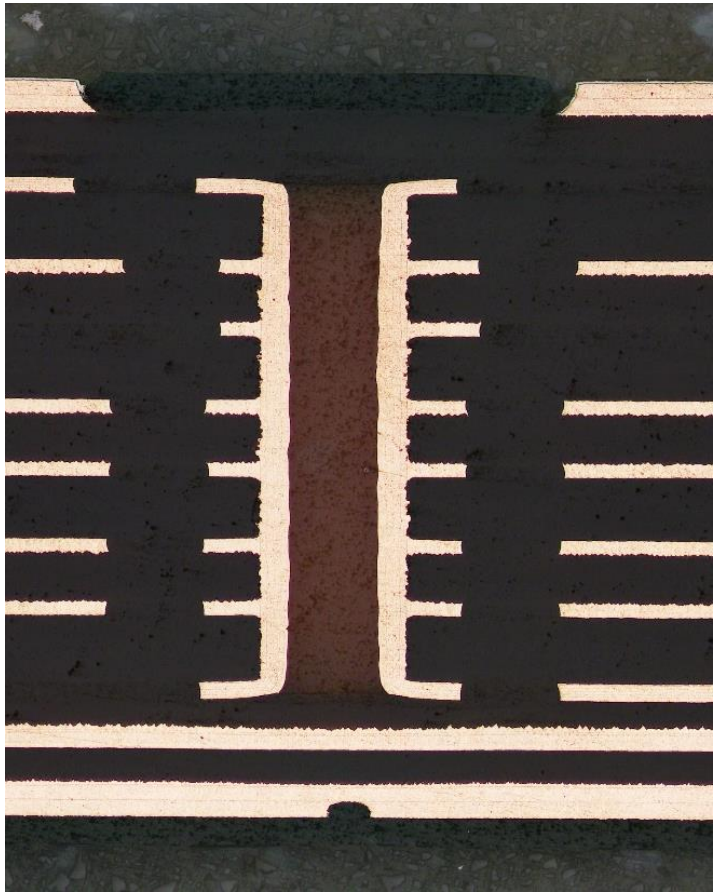
Typ VII
Filled & Capped Via



Typ I-a or Typ I-b describe the usage of single sided or double sided technology

TYP V FILLED VIA





A via with material applied into the via targeting a full penetration and encapsulation of the hole

Process	Vacuum Filling & sanding
Material	filled nonconductiv therm. Curing Epoxyd Resin

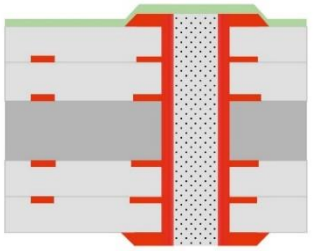
Benefit

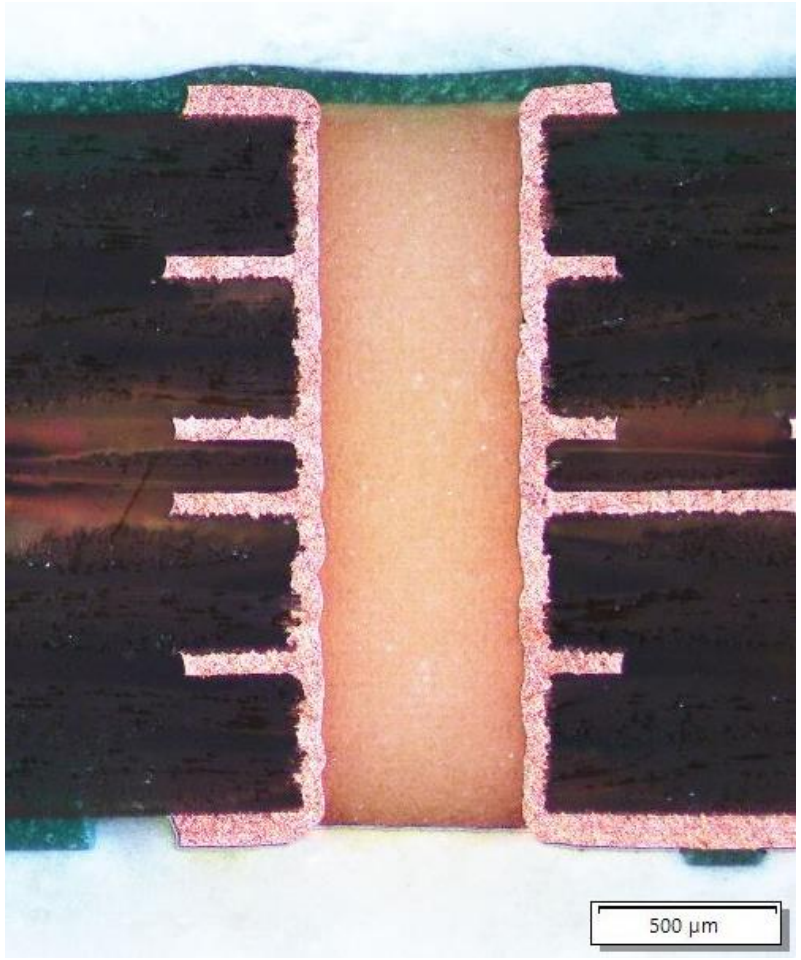
- Vacuum seal
- Homogenios flat surface through sanding process
- Often used on Inner layers to fill buried via

Concern

- With the filling process all through holes are filled
- Expensive

TYP VI-A FILLED VIA





A via with material applied into the via targeting a full penetration and encapsulation of the hole with solder mask

Process	Vacuum Filling & sanding & solder mask
Material	filled nonconductiv therm. Curing Epoxyd Resin

Benefit

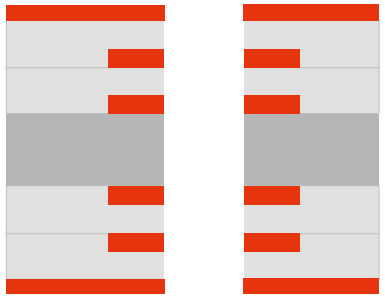
- Vacuum seal
- Homogenios flat surface through sanding process
- Often used on Inner layers to fill buried via

Concern

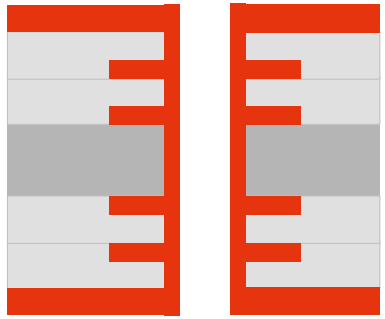
- With the filling process all through holes are filled
- Expensive

FILLED VIA FERTIGUNGSPROZESS

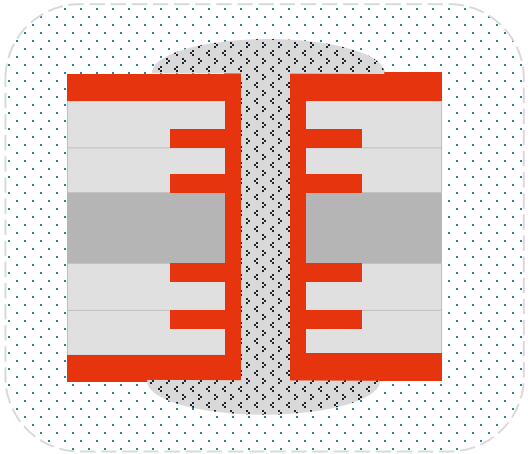
Drilling



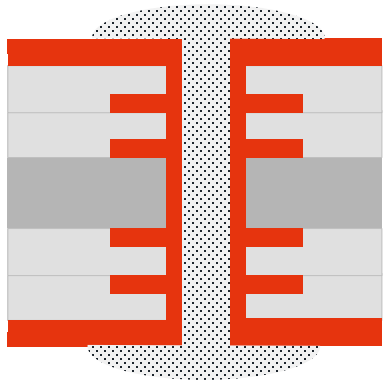
Metallization



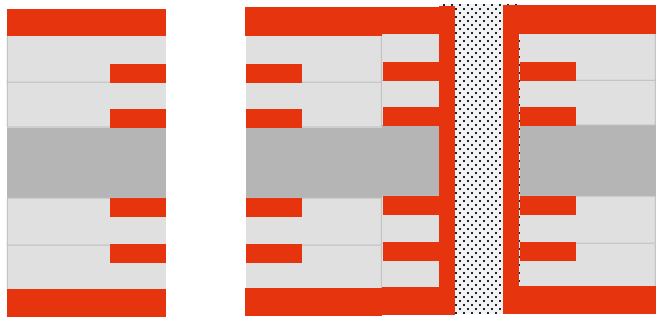
Vakuum Filling



Curing

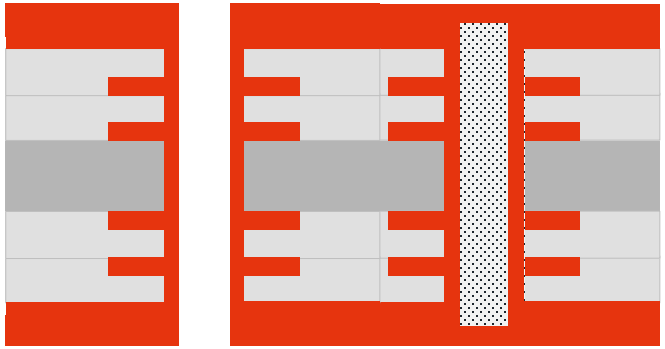


Sanding



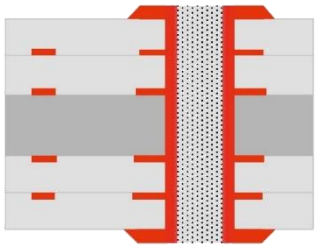
Typ V Filled Via

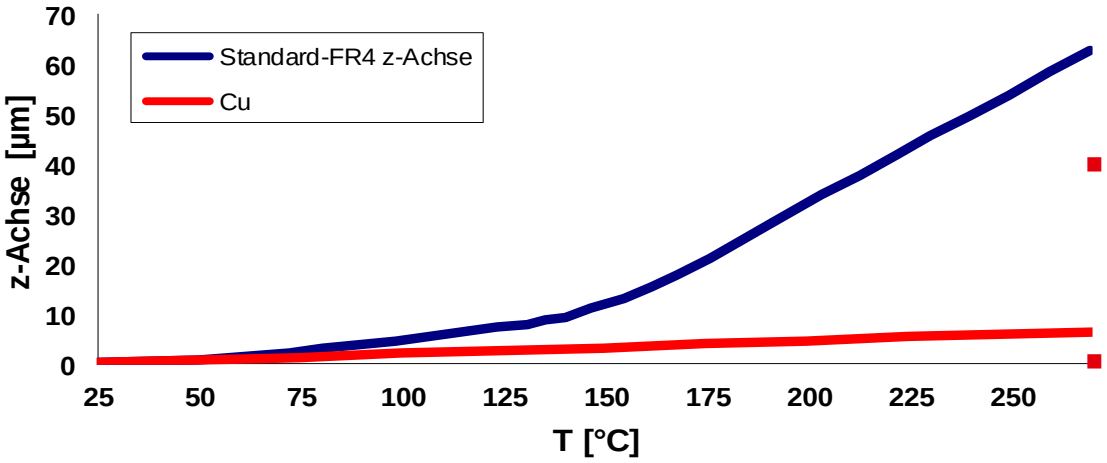
Cap metalization

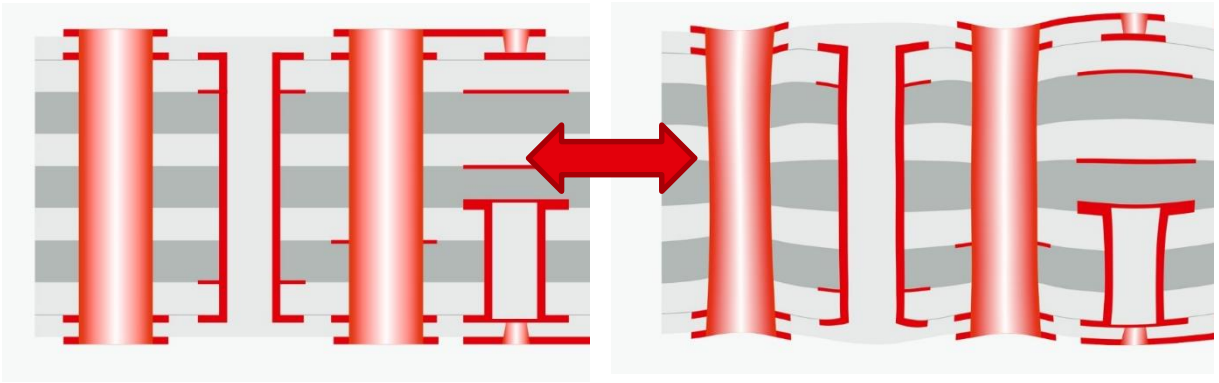


Typ VII Filled Via

FILLED VIA – MATERIAL COMBINATION

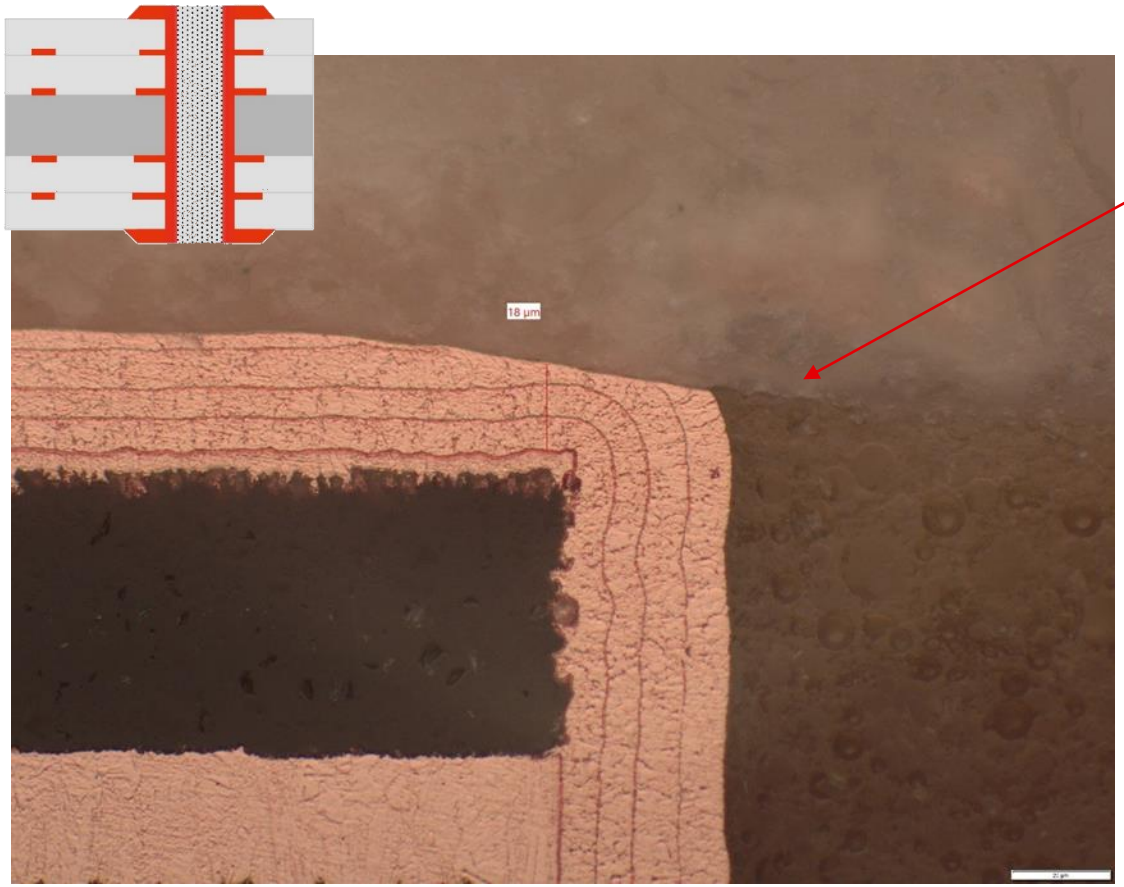






- To avoid a CTE missmatch the resin has to match to the FR-4 Material
- We recommend using filled FR-4 Materials with a TG ≥ 150 °C to achive highest performance

IPC-6012 WRAP COPPER



IPC-6012

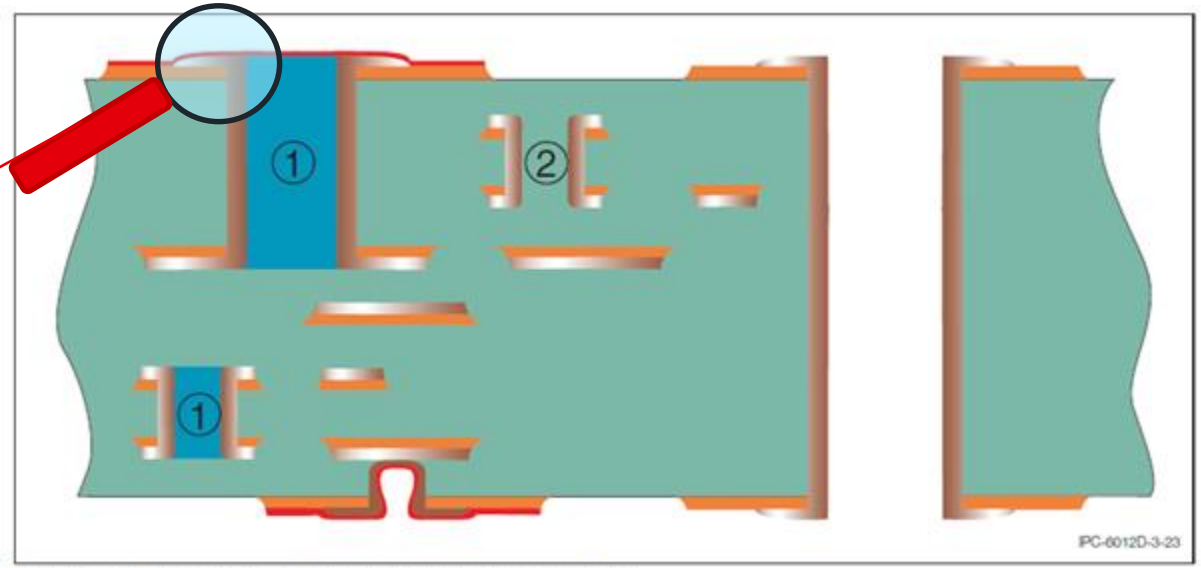


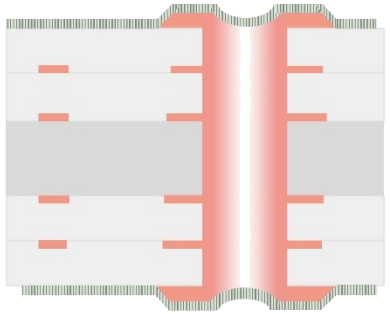
Figure 3-23 Wrap Copper in Type 4 Printed Board (Acceptable)
Note 1. Material Fill.
Note 2. Resin Fill.

Surface and Hole Copper Plating Minimum Requirements for Buried Vias > 2 Layers, Through-Holes, and Blind Vias

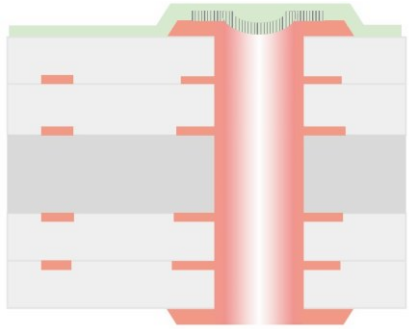
	Class 2	Class 3
Copper – average[2]	20 µm [787 µin]	25 µm [984 µin]
Thin areas	18 µm [709 µin]	20 µm [787 µin]
Wrap	5 µm [197 µin]	12 µm [472 µin]

SPECIFIKATION ACCORDING IPC-4761

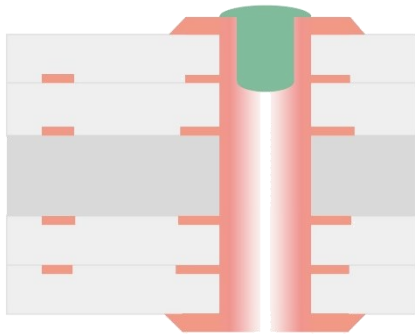
Typ I
Tented Via



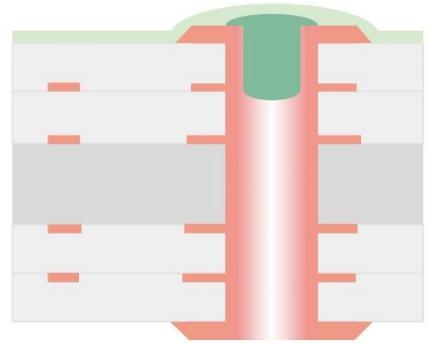
Typ II
Tented & Covered Via



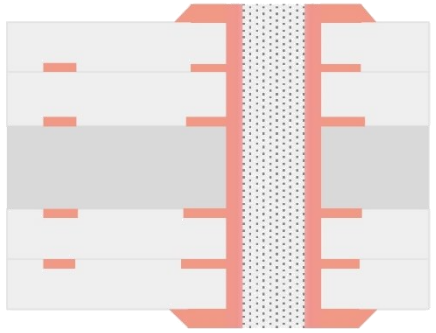
Typ III
Plugged Via



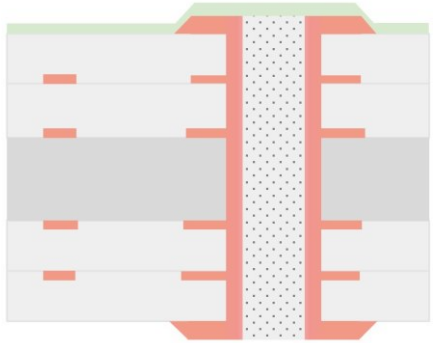
Typ IV
Plugged & Covered Via



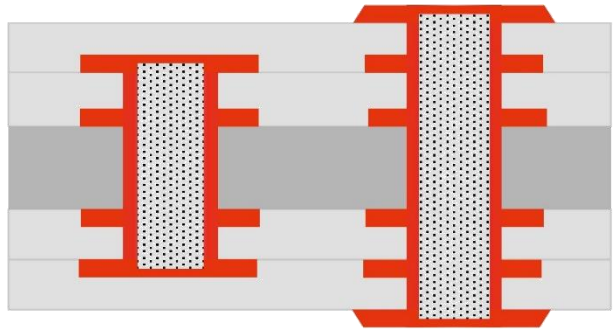
Typ V
Filled Via



Typ VI
Filled & Covered Via

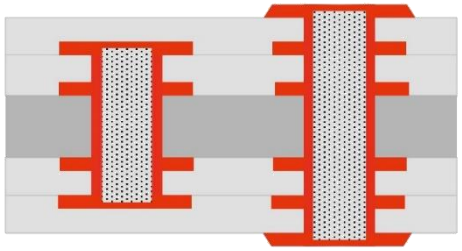


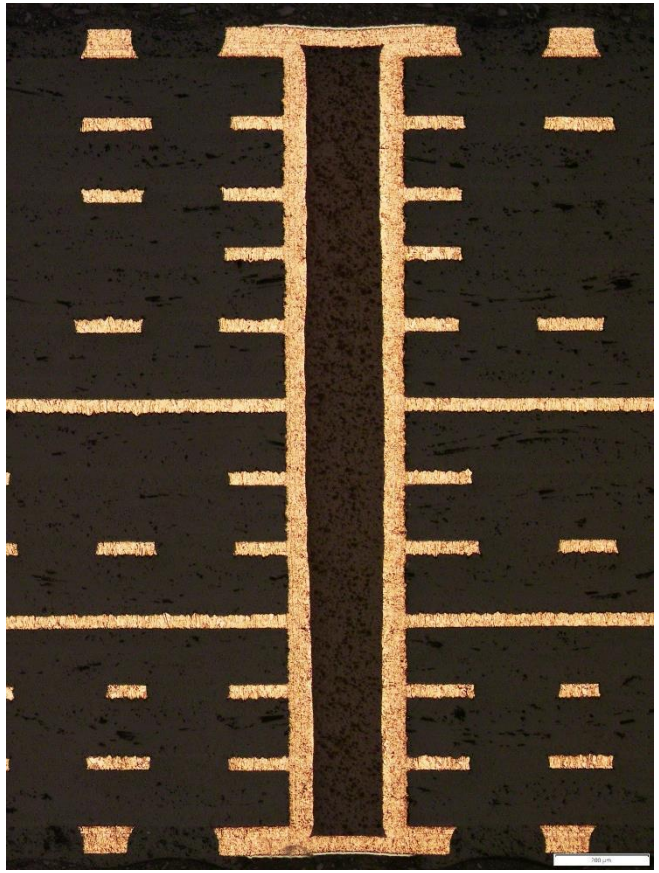
Typ VII
Filled & Capped Via



Typ I-a or Typ I-b describe the usage of single sided or double sided technology

TYP VII FILLED & CAPPED VIA





- A Type V via with a secondary metallized coating covering the via

Process	Vacuum Filling & sanding & cap plating
Material	filled nonconductiv therm. Curing Epoxyd Resin

Benefit

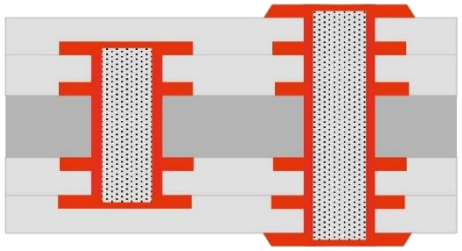
- Vacuum seal
- Homogenios flat surface through sanding process
- Via-in-Pad compatible

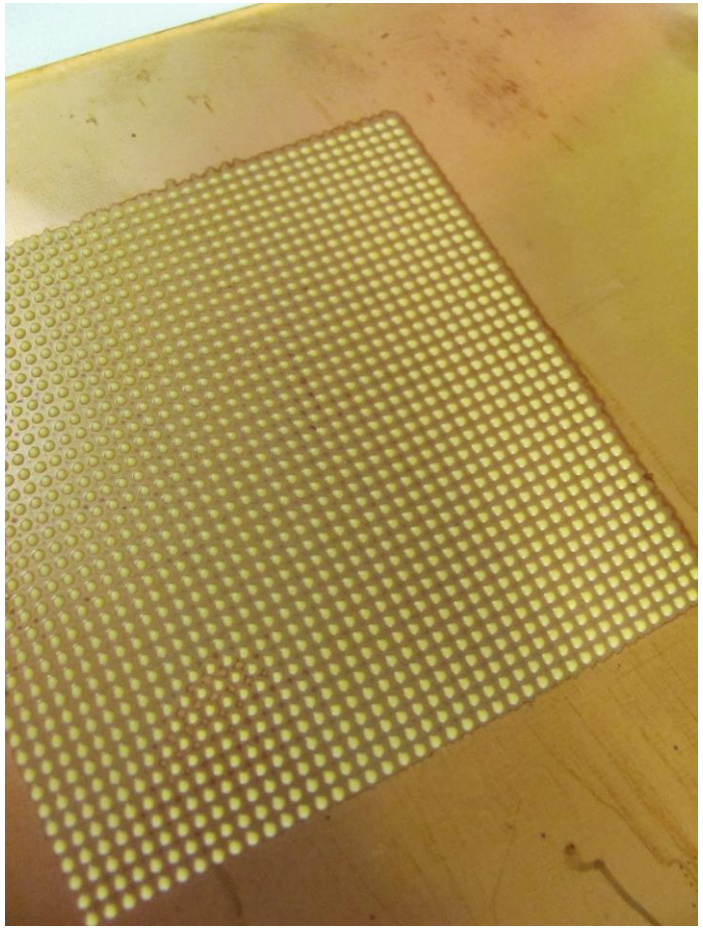
Concern

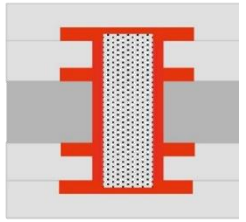
- With the filling process all through holes are filled
- Even more expensive through additional plating
- Reduction of fine line technology possible

TYP VII FILLED & CAPPED VIA

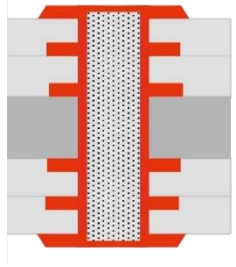
Design Rules







- 0,65 mm -1,60 mm Board thickness
  - Aspect Ratio 1:10
  - Smallest drill tool Ø 0,25 mm (final Ø 0,15 mm)
    Pad 500 µm
  - Max final Ø 0,65 mm
  - Layout Clearance >120 µm



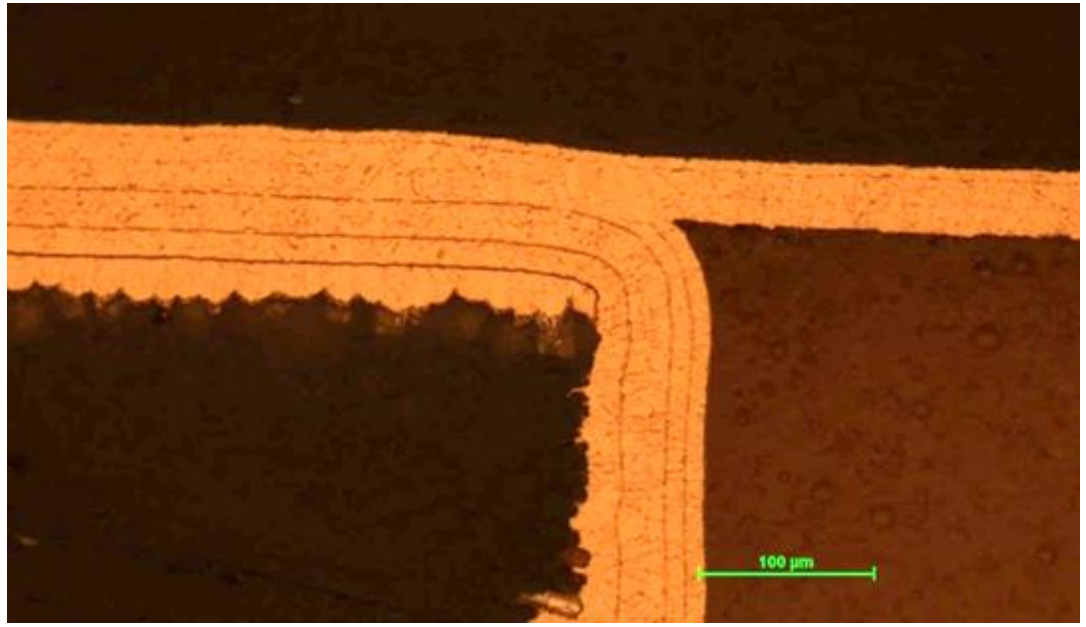
- 1,60 mm - 3,20 mm thickness
  - Aspect Ratio 1:8
  - Max final Ø 0,8 mm
  - Layout Clearance >120 µm

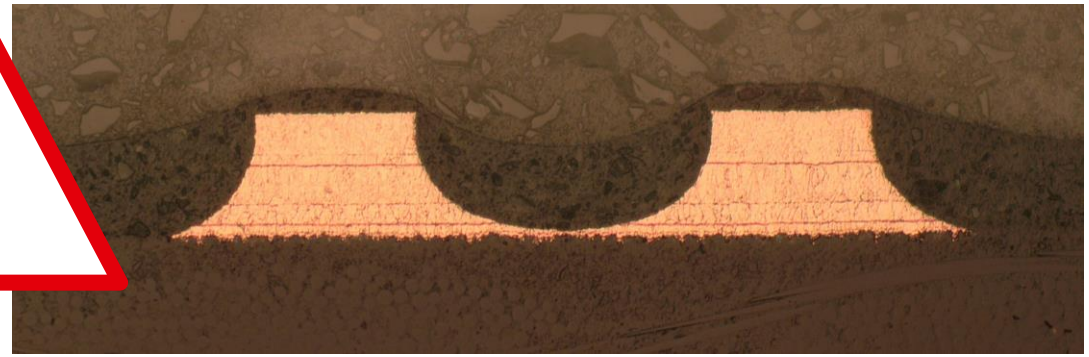
Please contact us early in your Design Phase to find optimal Parameters for your needs

Contact via your local WE partner or
HDI@we-online.de

FILLED VIA – TECHNOLOGY COMBINATION

design restrictions with fine line technology





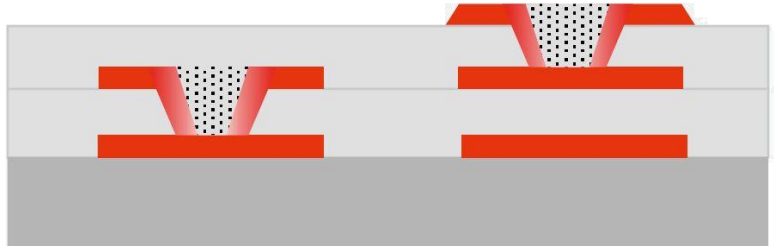
Through the need of several metallization processes the copper thickness on the surface will increase

Therfore compromisses in combination with fine line Technologies are necessary

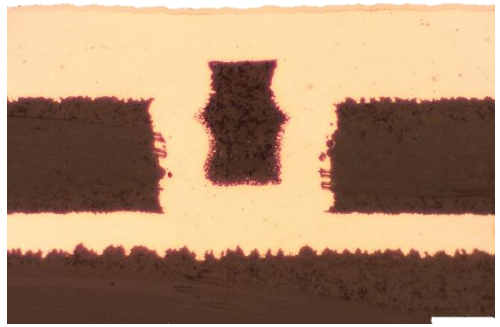
Typical design parameters related to the copper thickness		
Copper Thickness	**Line**	**Space**
~ 30 µm	75 µm	100 µm
~ 40 µm	100 µm	120 µm
~ 50 µm	120 µm	180 µm

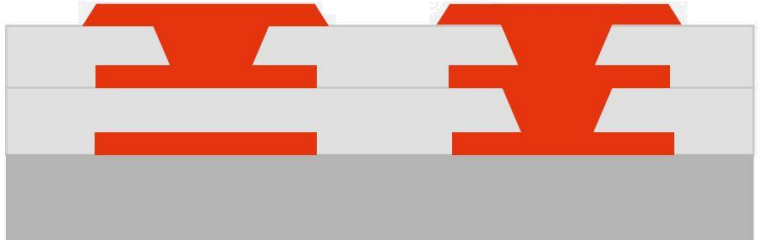
WEITERE ANWENDUNGEN

Micro Via Filling

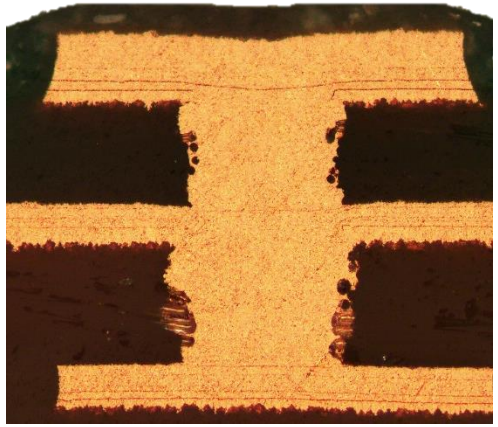


Filled Micro Via





Copper Filled Micro Via



Material filled Epoxy Resin or Copper

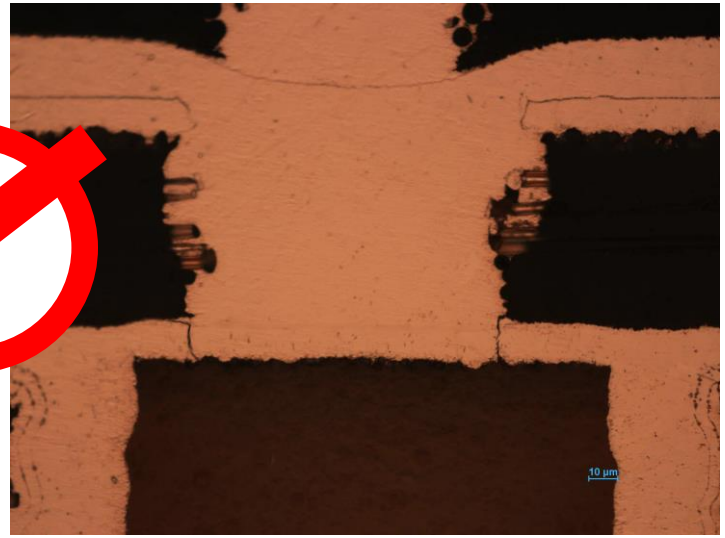
Benefit

- Via-in-Pad compatibel
- small Footprint
- Staggered or Stacked is possible

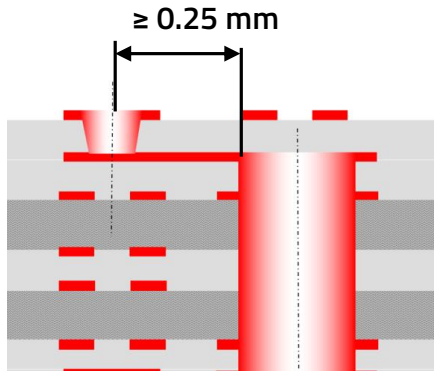
Concern

- With the filling process all through holes are filled
- Copper-Filling has limited compatibility with Through Hole Via
- Expensive

STACKED MIKROVIA ON TOP OF BURIED VIA



Recomendation by IPC & ZVEI-Arbeitskreis Qualität & from Würth Elektronik:

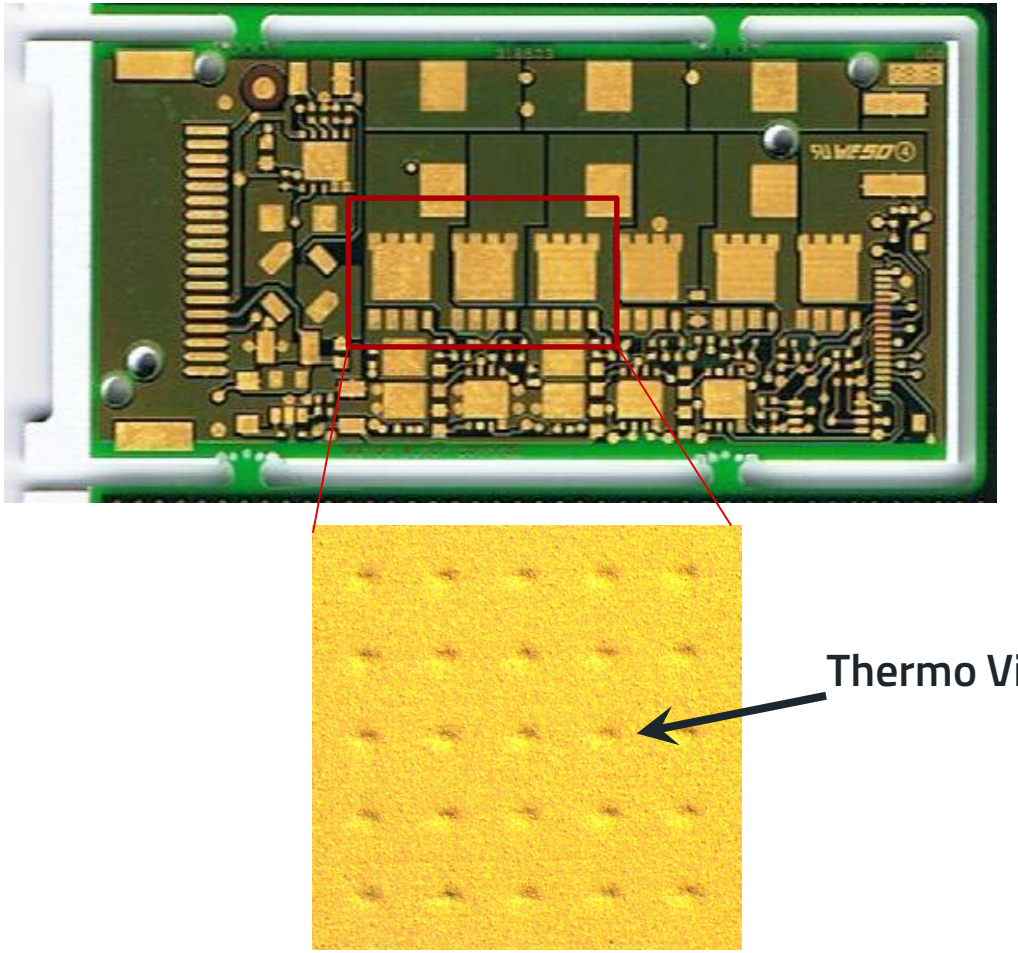


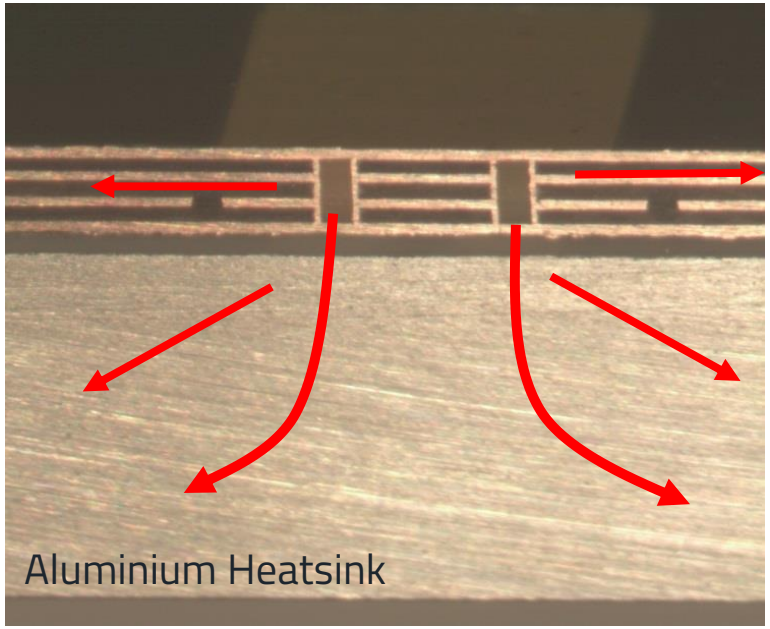
Also existing Layouts with these technology should by chance

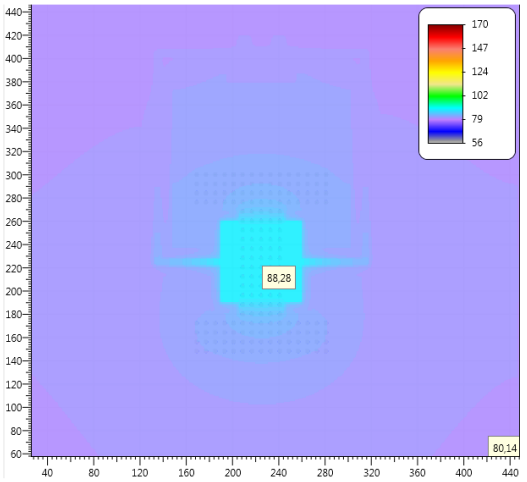
We will assist you !

EXAMPLE & PRATICAL USE

Thermo Vias & Via-in-Pad

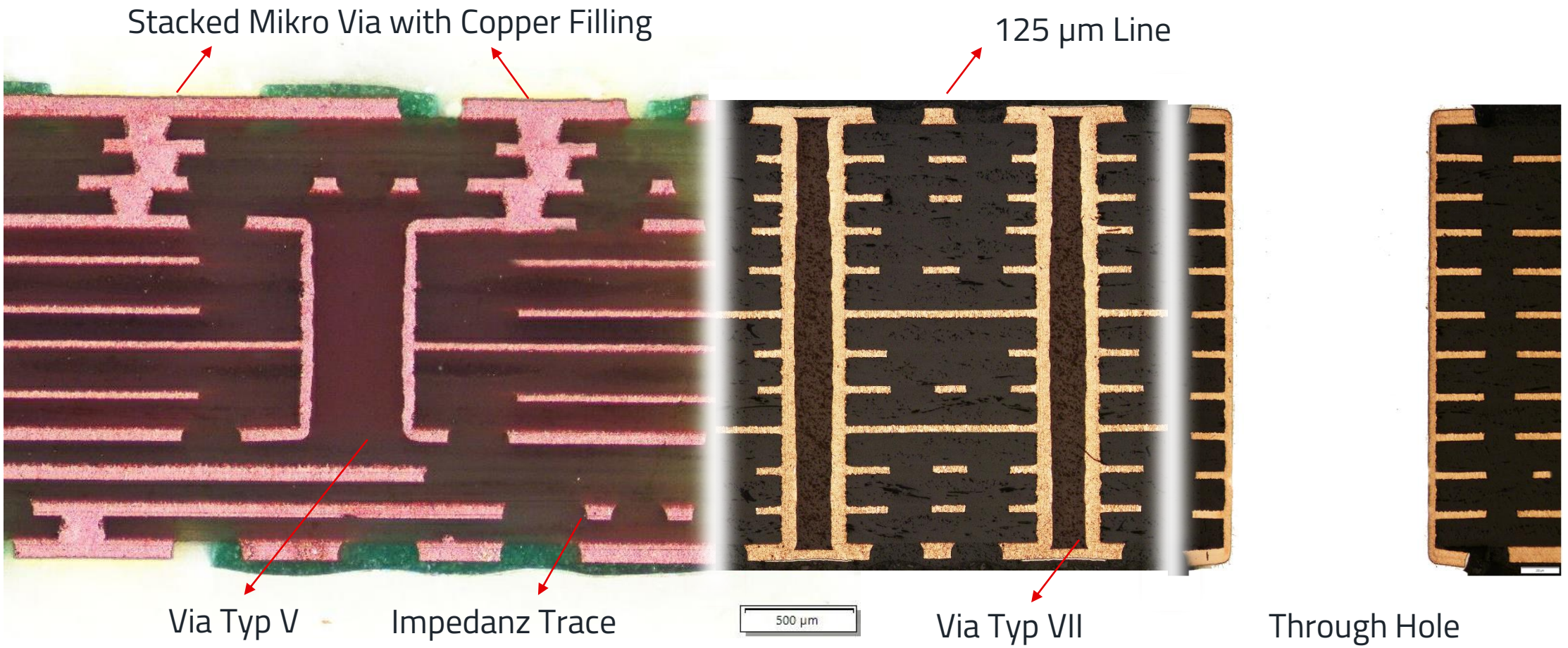






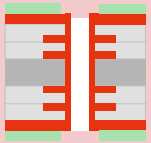
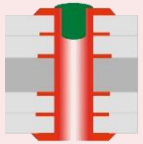
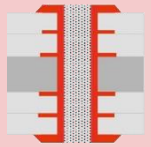
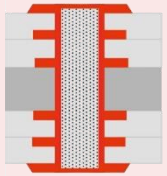
EXAMPLE & PRATICAL USE

HDI – Anwendung



Please contact us early in your Design Phase to find optimal Stack Up for your needs! Contact: HDI@we-online.de

SUMMARY

VIA-TYP	Vacuum Seal	Flat Surface	Possible on inner layer	Effort
 Clearance in Solder Mask	✗	✓	✗	
 Typ III a Plugged Via	✓	✗	✗	
 Typ V Filled Via	✓	✓	✓	
 Typ VII Filled & Ccapped Via	✓	✓	?	
 Micro Via Copper Filling	✓	✓	✓	

THANK YOU FOR YOUR ATTENTION!

Questions?

Contact:
Würth Elektronik GmbH & Co. KG
Circuit Board Technology
+49 7622 397-133
andreas.dreher@we-online.com