TRANSFORMER CHARACTERIZATION IN A FLYBACK CONVERTER

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WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

TABLE OF CONTENT

WBG AND ITS IMPACT ON MAGNETICS

Property	Si	GaN
E_g (eV) – band gap	1.1	3.39
E_c (MV/cm) – critical electric field	0.3	3.33
ε_r – dielectric constant	11.9	9
μ_n (cm^2/Vs) – electron mobility	1350	1700

Figure 1: Material properties of GaN and Si

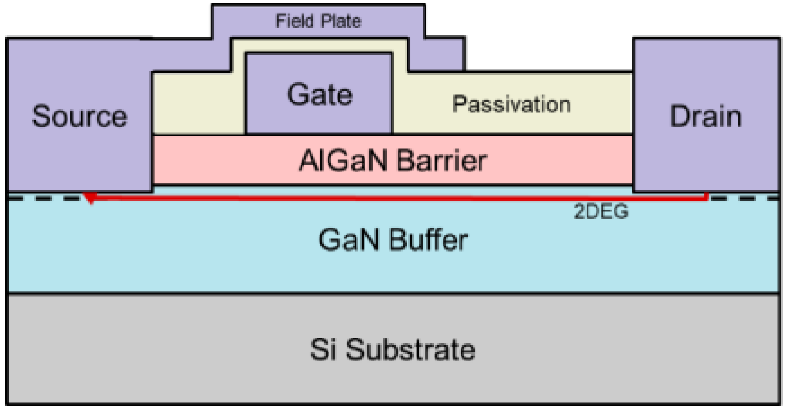
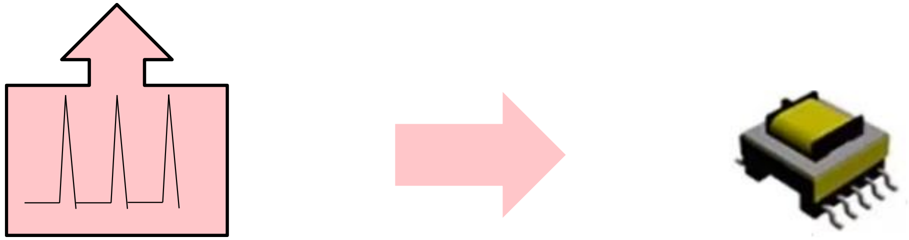


Figure 2: Basic Lateral Structure of GaN FET

The lateral structure of the HEMT (high electrons mobility Transistor) make possible high-speed operation, low capacitance device and low on-resistance which permit high operation frequencies compared to the traditional Si devices

Higher SW Frequency



- Smaller magnetics
- Tougher EMI to mitigate
- Higher parasitic capacitance resulting in ringing and voltage spikes
- Higher parasitic inductance that can lead to higher core losses

TRANSFORMER´S PARASITIC IMPACT ON A FLYBACK CONVERTER

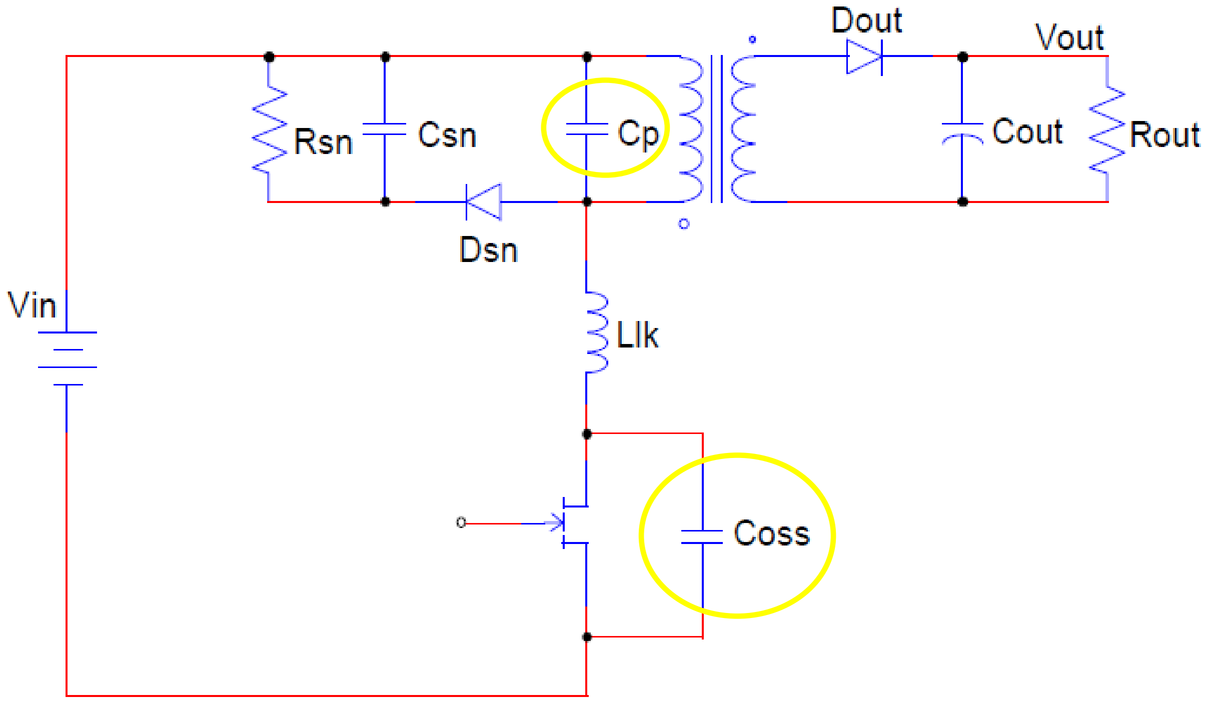


Figure3: Standard Flyback converter (Transformer Model)

The Flyback topology is by far the most common topology for converters <100W this is due primarily to its low component count and its fairly easy design and manufacturing.

The total losses during Turn ON can be resumed in two main parameters:
The first is Coos dependent on Drain to Source voltage:

$$P_{SW-ON(Coss)} = f_{SW} \int_{0}^{V_{DS(OFF)}} C_{OSS}(V_{ds}) V_{ds} dV_{ds}$$

The second contribution which is topology related, is due to the transformer parasitic capacitance Cp. This capacitance is discharged in the GaN switch at Turn ON and is constant:

$$P_{SW-ON(Cp)} = \frac{1}{2} C_P V_{DS(OFF)}^2 f_{SW}$$

TRANSFORMER´S PARASITIC IMPACT ON A FLYBACK CONVERTER

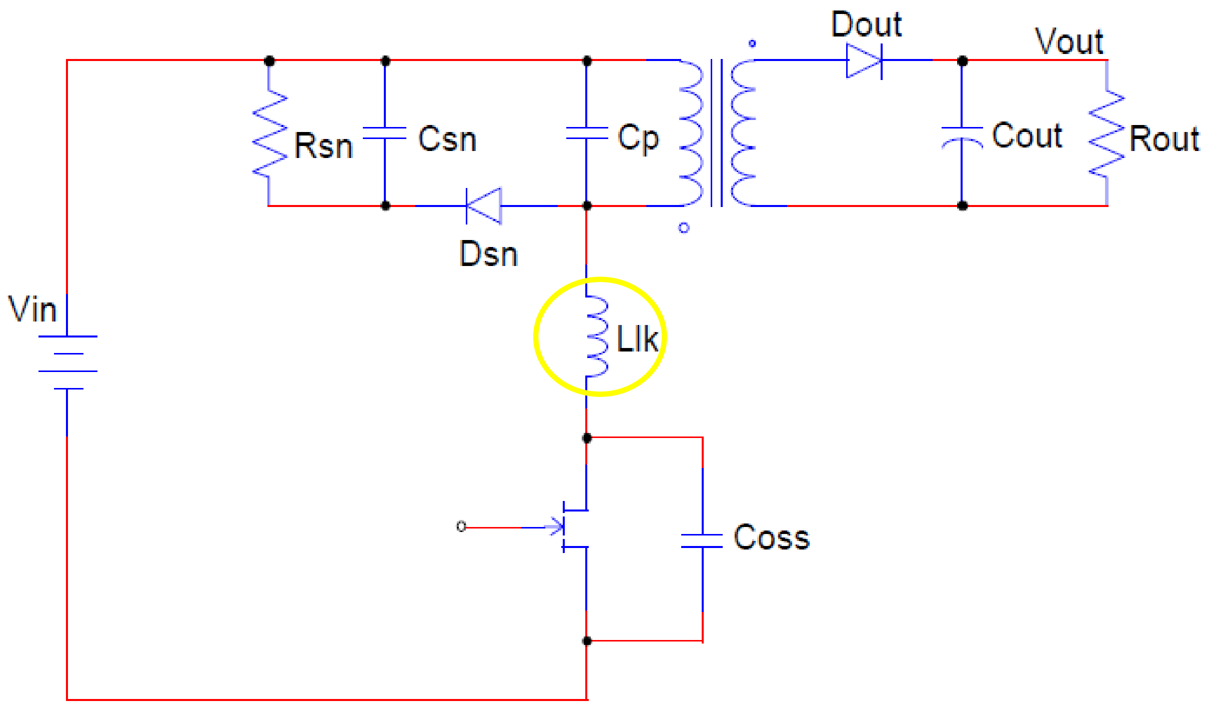


Figure3: Standard Flyback converter (Transformer Model)

Another important source of inefficiency for a traditional Flyback would be the leakage inductance

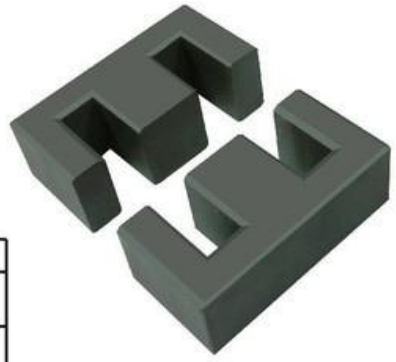
During turn OFF, the energy stored in the leakage inductance is being released onto the Switching device. To avoid any possible damage and the high voltage spikes, this energy can be dissipated via a snubber circuit, in this case an RCD.

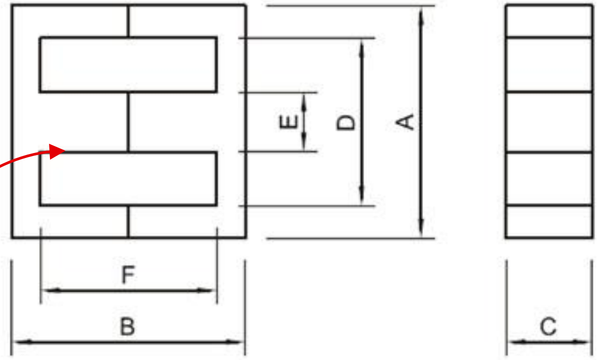
→ The adoption of GaN MOSFET reduces the component that is related to the output capacitance of the device, but there is still power dissipation due to the transformer parasitic that we need to control.

DESIGN REQUIREMENTS FOR A FLYBACK CONVERTER

- A Flyback Transformer isn´t really a transformer but rather a coupled inductor since the energy transfer between the Prim and the Sec isn’t instant. The transformer needs to store energy in the core

$$\text{Energy (store inside core)} = \frac{1}{2}\frac{B^2}{\mu_c}V_c \quad \text{unit J}$$





$$\text{Energy} \propto \frac{V_c}{\mu_c}$$

$$\uparrow \text{Energy} \propto \frac{\uparrow V_c}{\mu_c}$$

$$\uparrow \text{Energy} \propto \frac{V_c}{\downarrow \mu_c}$$

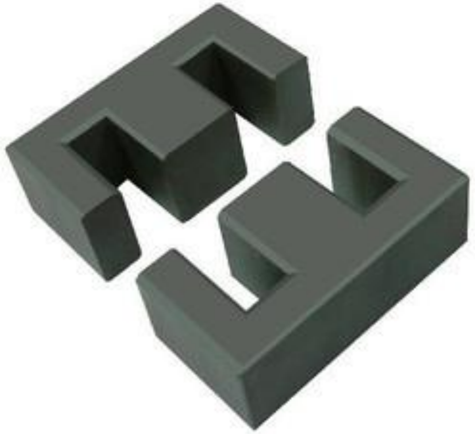
For un-gapped core, μc about 1500 to 6000

DESIGN REQUIREMENTS FOR A FLYBACK CONVERTER

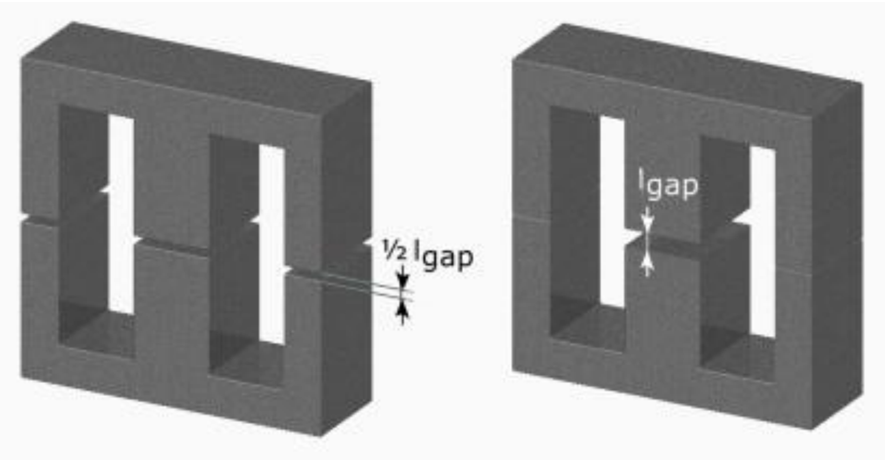
- How can we store more Energy in the core ?

$$\uparrow \text{Energy} \propto \frac{V_c}{\downarrow \mu_c}$$

Add an air gap to core to reduce the equivalent permeability



$$\text{Energy (store in an inductor)} = \frac{1}{2} L_{ind} I_{peak}^{2}$$

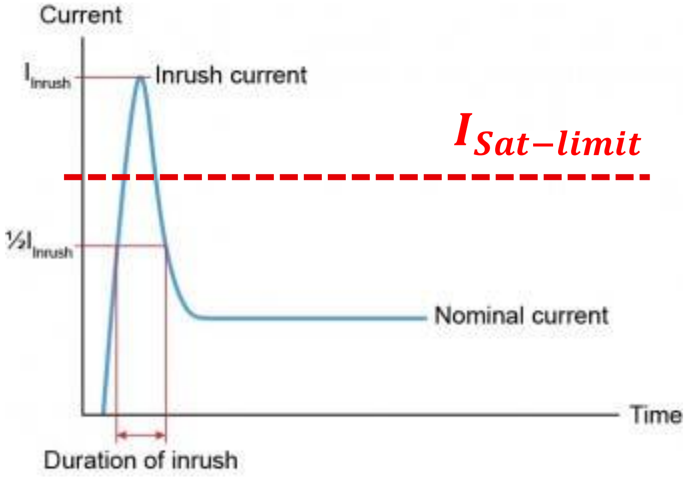


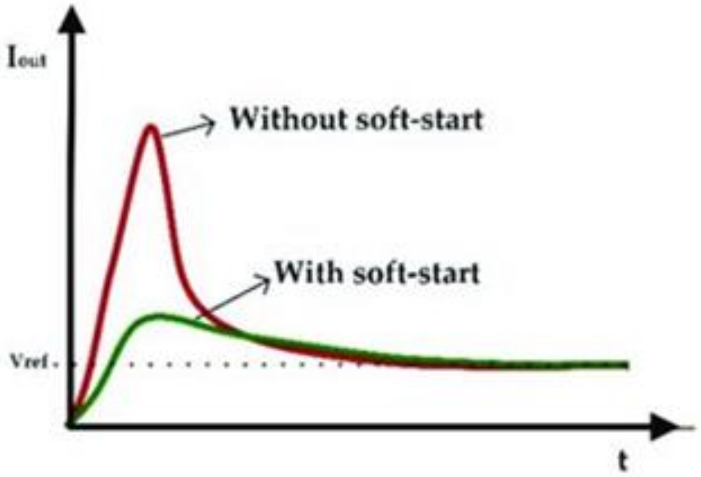
$$I_{sat-prim} \gg I_{Pri\ or\ required\ for\ design}$$

$$\text{Max. Energy (store in an inductor)} \approx \frac{1}{2} L_{ind} I_{sat}^{2}$$

DESIGN REQUIREMENTS FOR A FLYBACK CONVERTER

- The inrush current while starting the flyback converter can saturate the transformer even for a short duration





DESIGN REQUIREMENTS FOR A FLYBACK CONVERTER

$$I_{sat-prim} \gg I_{Pri\ or\ required\ for\ design}$$

Important requirement for Flyback transformer

WÜRTH ELEKTRONIK

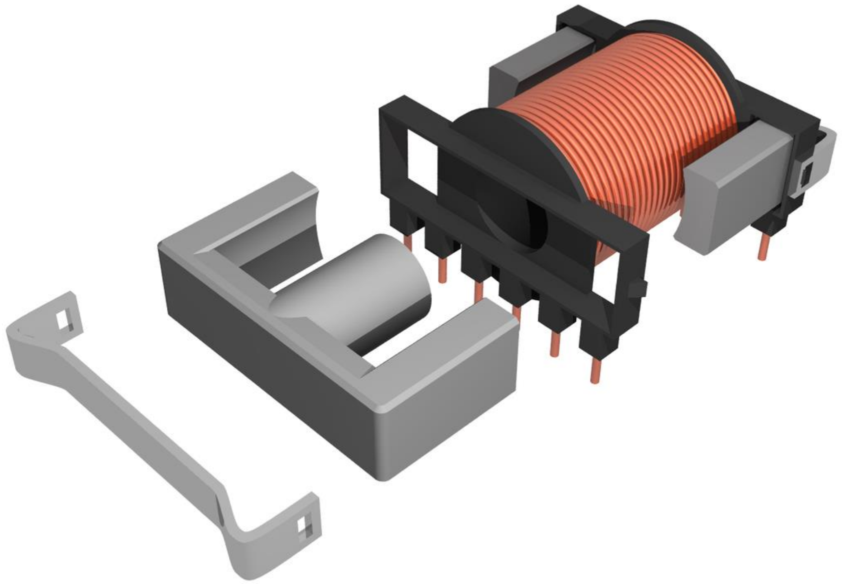
6C ELECTRICAL SPECIFICATIONS @ 25°C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	1–3	@20°C	3.15 ohms ±10%
D.C. RESISTANCE	5–4	@20°C	0.81 ohms ±10%
D.C. RESISTANCE	7–9	tie(6+7, 8+9), @20°C	0.021 ohms ±20%
INDUCTANCE	1–3	10kHz, 100mVAC, Ls	1.59mH ±10%
SATURATION CURRENT		20% rolloff from initial	480mA
LEAKAGE INDUCTANCE	1–3	tie(4+5, 6+7+8+9), 100kHz, 100mVAC, Ls	23uH typ., 34uH max.
6C DIELECTRIC	3–7	tie(3+4, 7+8), 4500VAC, 1 second	3600VAC, 1 minute
TURNS RATIO		(3–1):(7–9), tie(6+7, 8+9)	15:1, ±1%
TURNS RATIO		(3–1):(5–4)	8.571:1, ±1%

DESIGN REQUIREMENTS FOR A FLYBACK CONVERTER

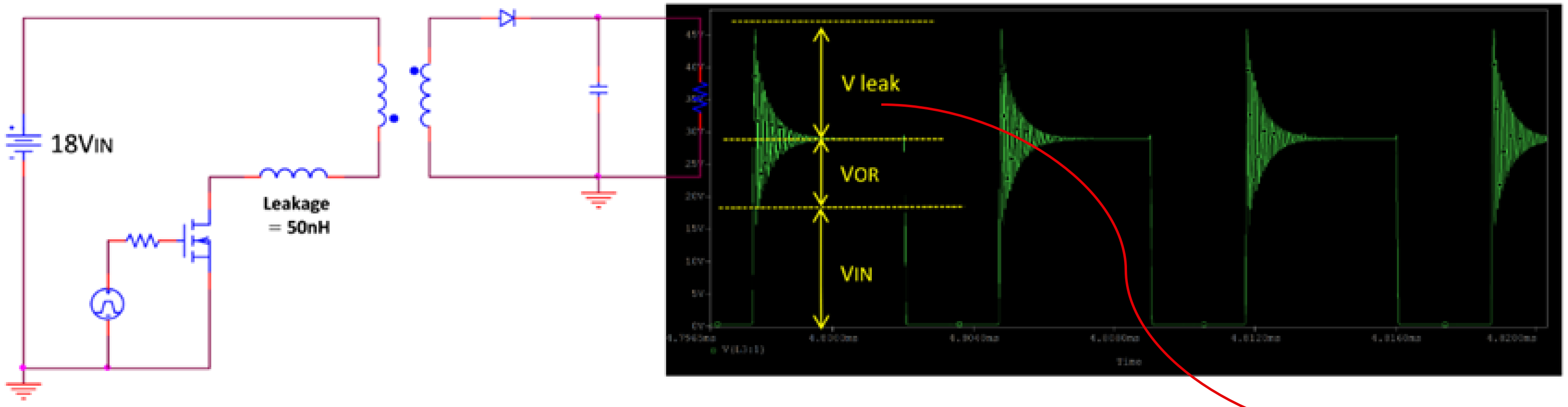
- Unlocking higher operating frequency thanks to the use of GaN Ics led us to take into account the choice of a proper core material

We currently use MnZn core materials that allow good behavior of the transformer up to 1 MHz



DESIGN REQUIREMENTS FOR A FLYBACK CONVERTER

- The leakage inductance is an important parameter we should make sure of supressing in a Flyback transformer. The rule of thumb mostly specify a max value of 5% of the nominal inductance value



Switch Note Waveform with Leakage Inductance

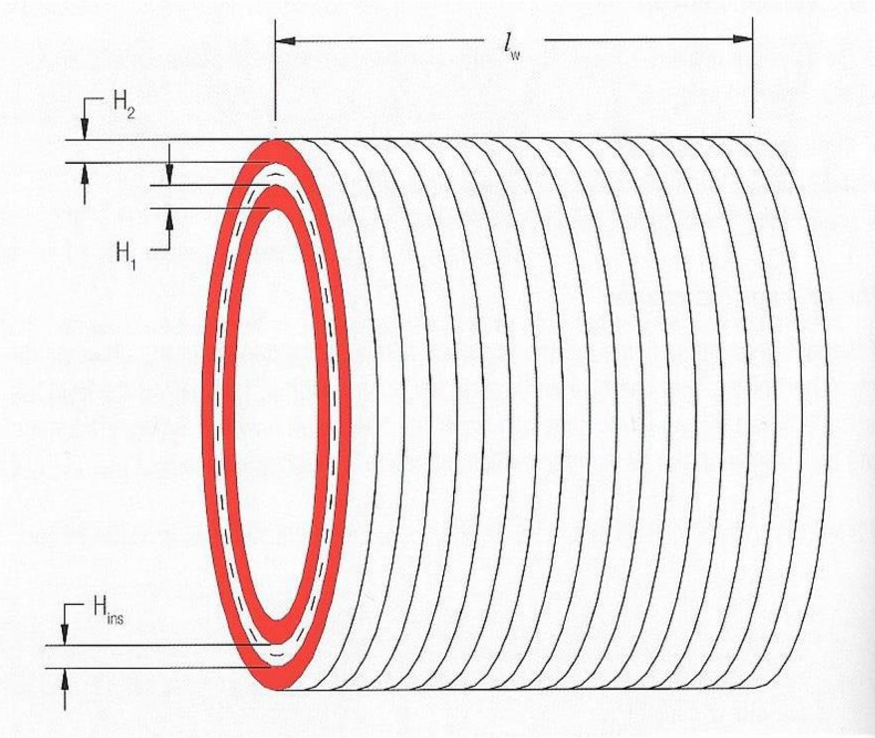
$$V_{leak\ or\ Spike} = I_{Pri-peak}\sqrt{\frac{L_{leakage}}{(C_p + C_{ds})}}$$

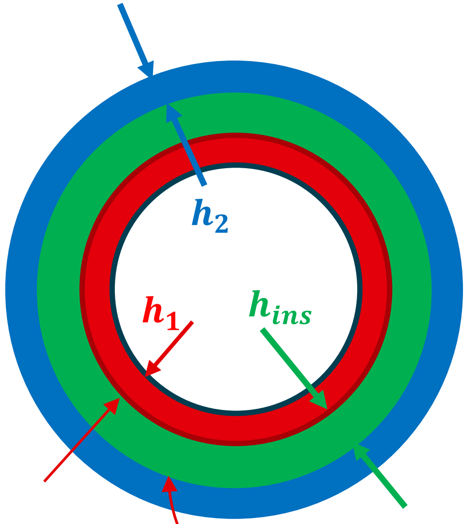
Where:

$L_{leakage}$: Primary leakage inductance
C_p: Transformer primary capacitance
C_{ds}: Mosfet drain-source capacitance

DESIGN REQUIREMENTS FOR A FLYBACK CONVERTER

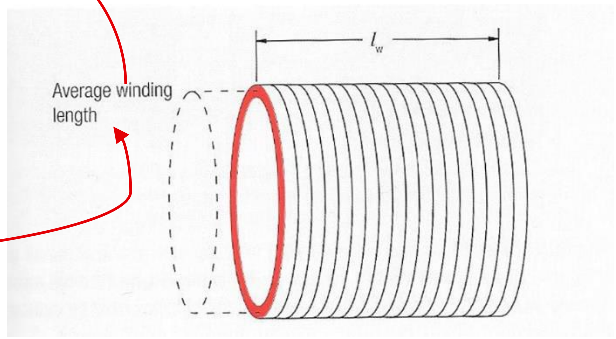
- For a solenoid structure with symmetrical turn ratio,





$$L_{leakage} = \frac{\mu_0 N^2 A_{insulation}}{l_w}$$

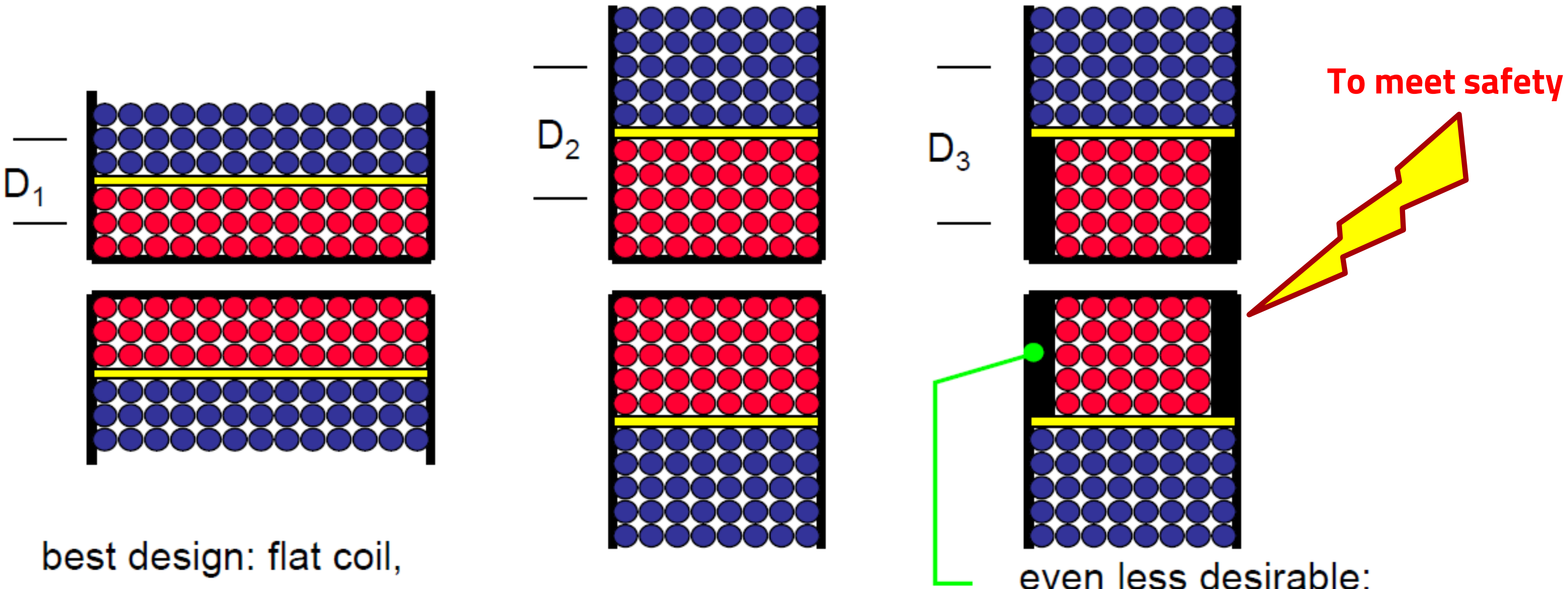
$$A_{insulation} = MLT\left(h_{ins} + \frac{1}{3}h_1 + \frac{1}{3}h_2\right)$$



MLT: Mean length turn or average winding length

DESIGN REQUIREMENTS FOR A FLYBACK CONVERTER

- How does the transfromer structure impact the leakage inductance ?



best design: flat coil, short average distance

less desirable: greater average distance

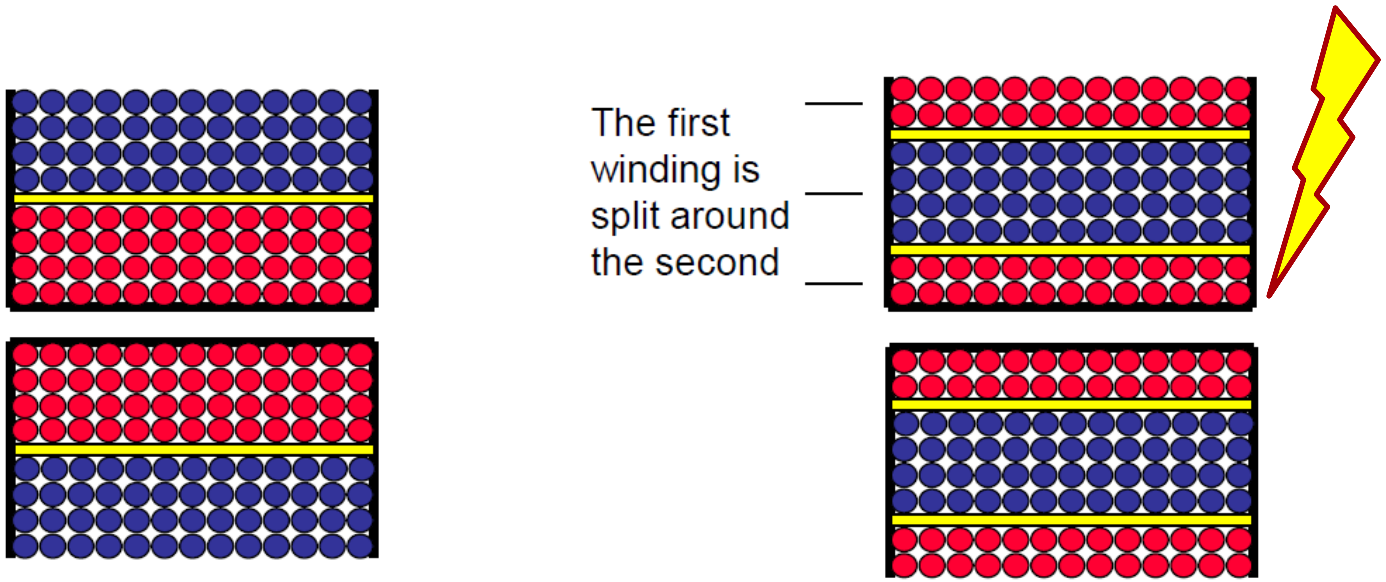
even less desirable: shelves reduce area at interface between coils

Reference: Würth Elektronik eiSos, Trilogy of Magnetics, handbook

DESIGN REQUIREMENTS FOR A FLYBACK CONVERTER

- How does the transfromer structure impact the leakage inductance ?

More winding labor - $$ cost

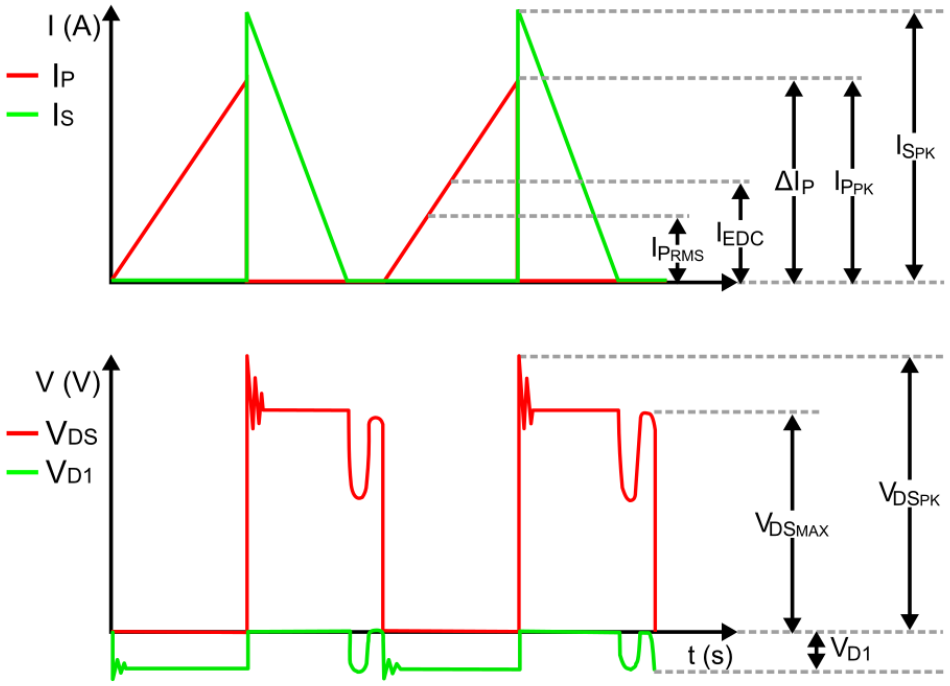


To improve the coupling between the windings we can sandwich the first winding around the second. This reduces the average distance between the windings and results in 1/4th the original value of leakage inductance –

Reference: Würth Elektronik eiSos, Trilogy of Magnetics, handbook

DESIGN REQUIREMENTS FOR A FLYBACK CONVERTER

- AC Resistance:
  - Importance for DCM mode of operation.



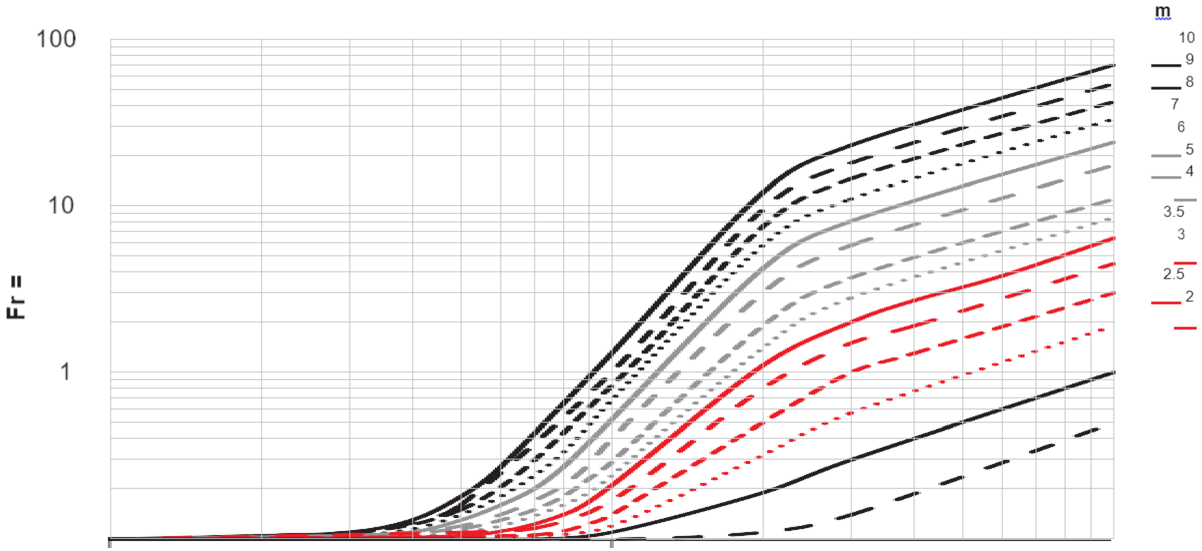
Discontinuous Conduction Mode

- **Sawtooth current waveform on PRI & SEC**
- **FFT of current waveform shows a fundamental @ switching frequency + harmonics**
- **So importance of AC resistance comes to the equation**

DESIGN REQUIREMENTS FOR A FLYBACK CONVERTER

Design Requirements

- AC Resistance:
  - Important of this resistance appears in DCM mode of operation.
  - At higher frequencies (e.g. GaN converters), AC resistance is the dominant for copper losses



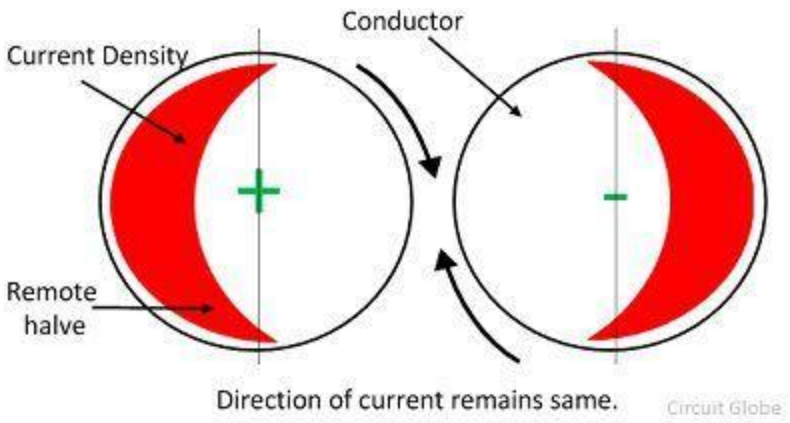
Dowell's curves showing rapid increase in ac resistance factor (Fr) as the wire thickness relative to skin depth (φ) and number of winding layers (m) increase

Reference: Trilogy of Magnetics

DESIGN REQUIREMENTS FOR A FLYBACK CONVERTER

Design Requirements

- AC Resistance:
  - Important of this resistance appears in DCM mode of operation.
  - At higher frequencies, AC resistance is the dominant for copper losses
  - Modeling of AC resistance:
    - Analytical or theoretical model -> **not easy (check text books)**
    - **Need to study the effect of:**
      - **Proximity effect**
      - **Skin depth**
    - **2D or 3D model using FEM:**
      - **Ansys -> Maxwell**



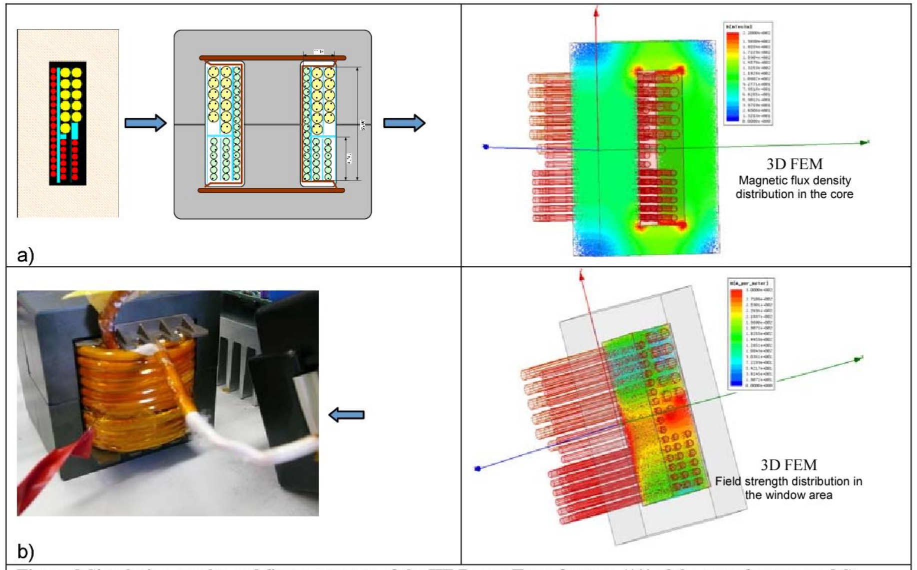


Figure 8 Simulation results and first prototype of the HF Power Transformer, (1/4 of the transformer model)

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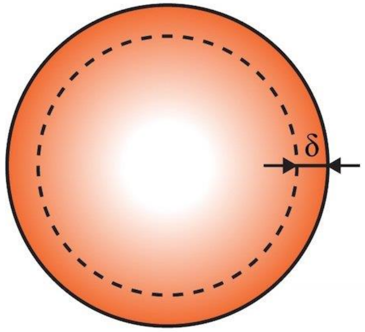


Skin Depth is:

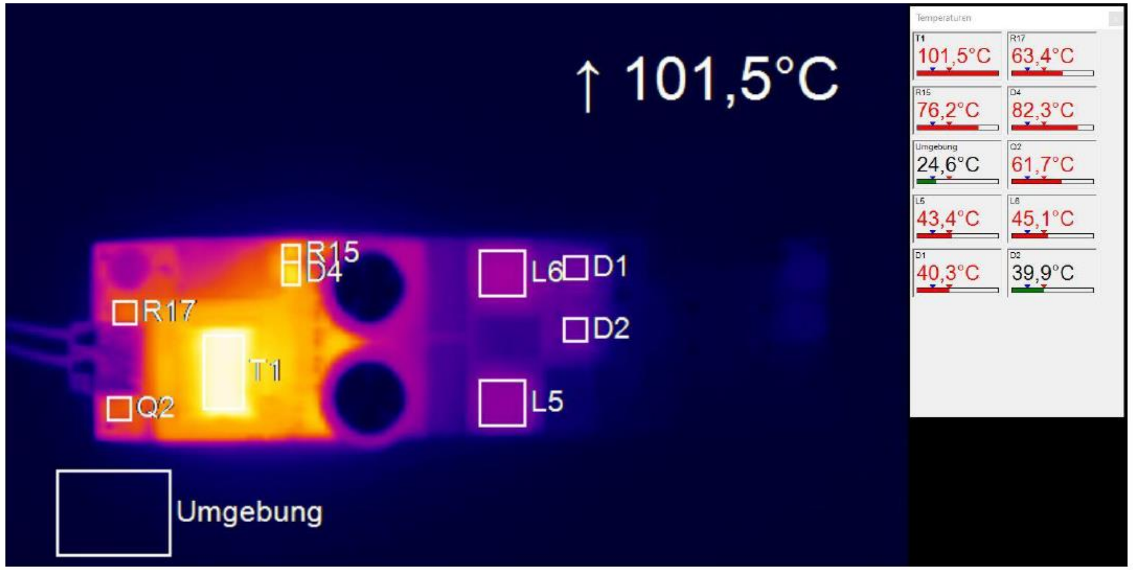
$$\delta = \sqrt{\frac{1}{\pi f \mu_0 \mu_r \sigma_0 \sigma_r}}$$

DESIGN REQUIREMENTS FOR A FLYBACK CONVERTER

Design Requirements

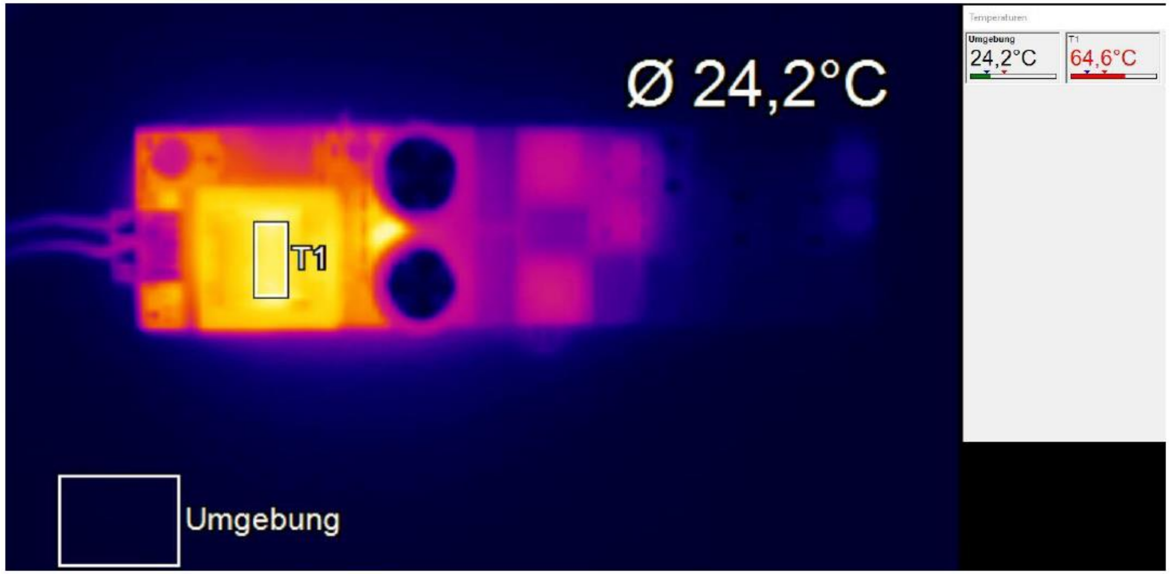
- AC Resistance:
  - Litz wire to optimize AC resistance
  - Example:
    - **Transformer for Offline Flyback DCM topology at 100kHz operating freq.**

Line: 230V / Load: 30W



Transformer with solid wire

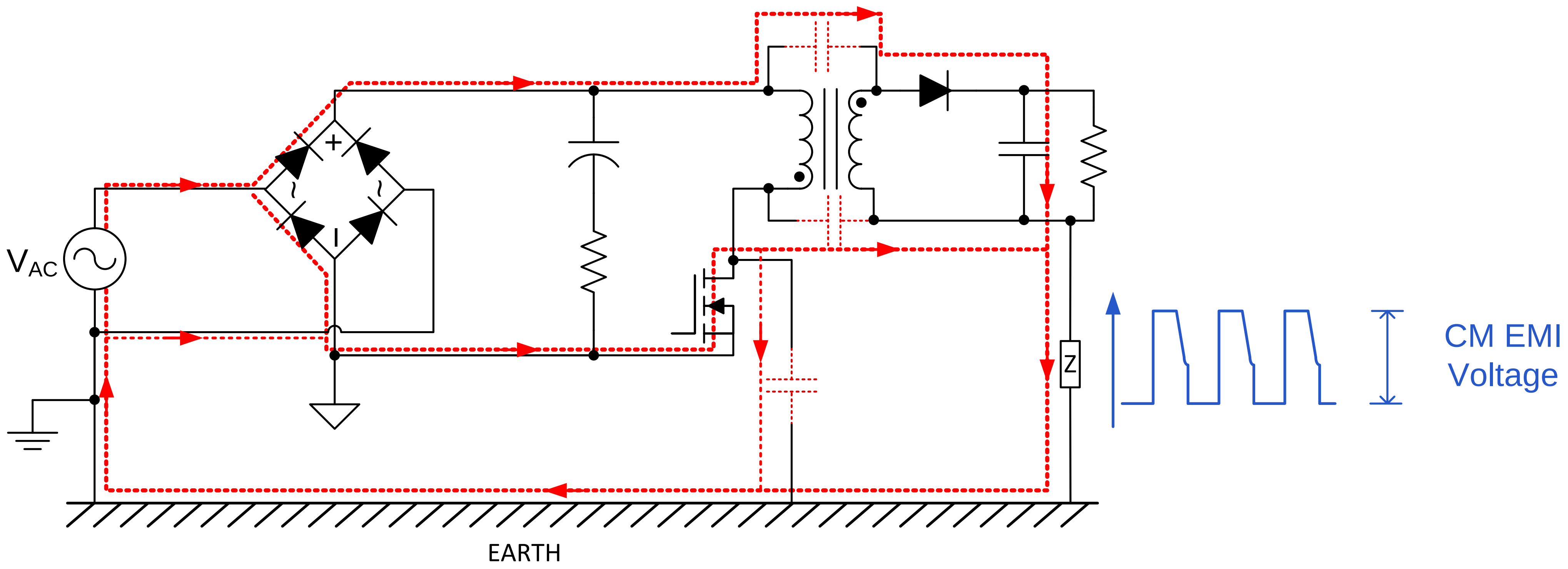
Line: 230V / Load: 30W



Optimized transformer using litz wire

EMC CONSIDERATIONS

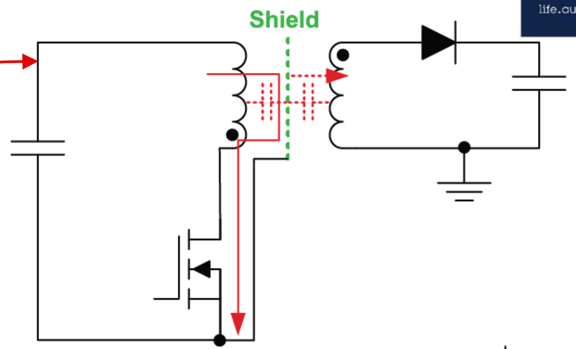
- Switching voltage across parasitic capacitance causes CM current flow to EARTH
- CM noise also radiated to other circuit nodes



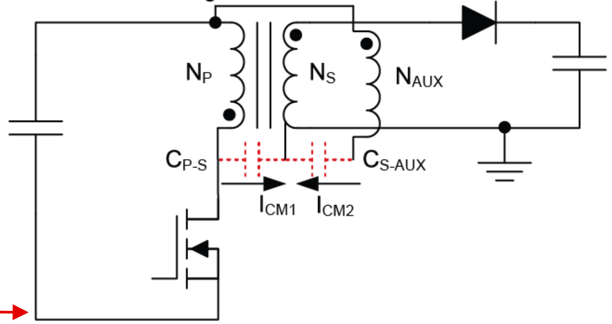
EMC CONSIDERATIONS

- MITIGATION OPTIONS FOR CM NOISE

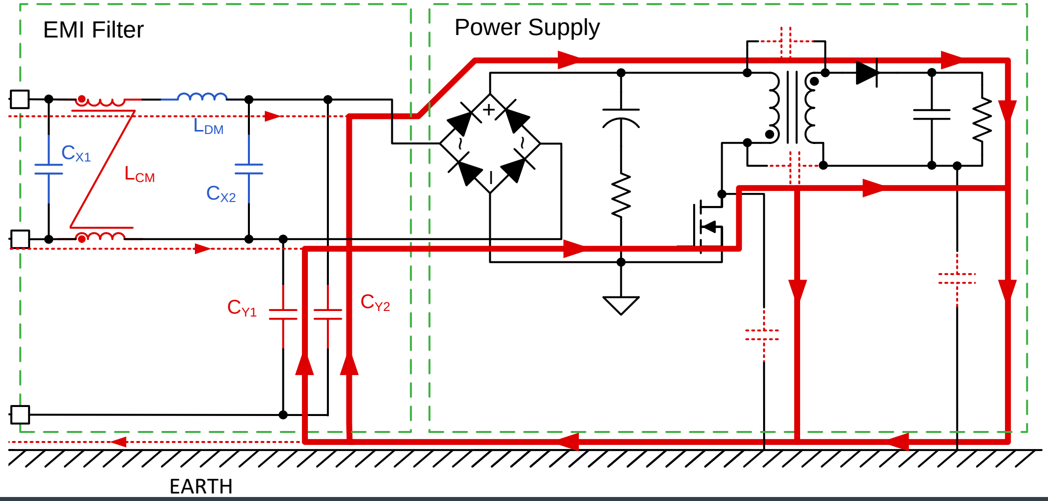
1. **Shielding:**
   - Reduce flow of HF current to EARTH (Internal)
   - GNDed flux-band (external)



2. **Cancellation:**
   - Arrange transformer and power stage for balanced CM



3. **Filtering:**
   - Increase impedance of the EARTH return path
   - Provide alternative routes for the HF current



EMC CONSIDERATIONS

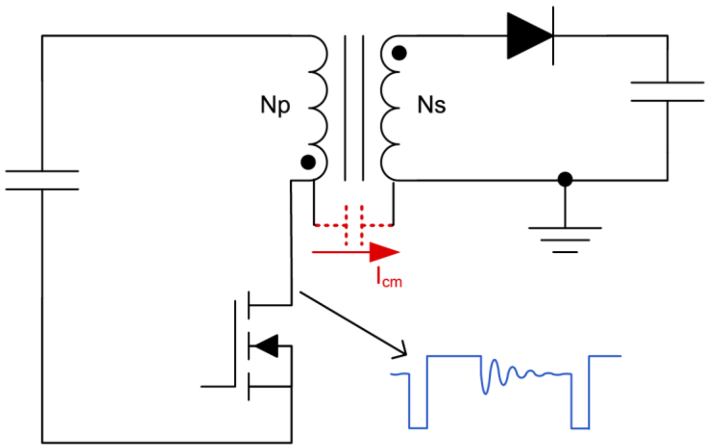
- **COMMON MODE MITIGATION BY TRANSFORMER INTERNAL SHIELDING**

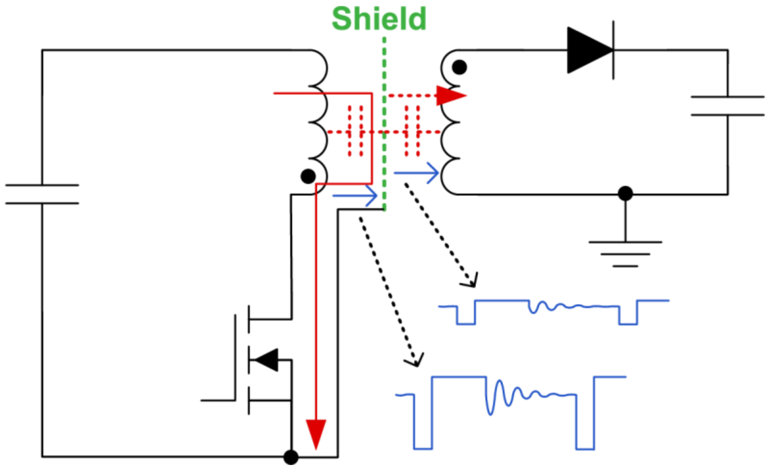
Shield added to keep most of CM current local to primary

Shield is 1-turn winding ⇒ lower induced voltage, less voltage across parasitic capacitance between shield & sec ⇒ less CM current flows

Shield must be thin (< 50 µm) ⇒ minimize induced eddy current loss

Eddy currents get very significant as FSW increases



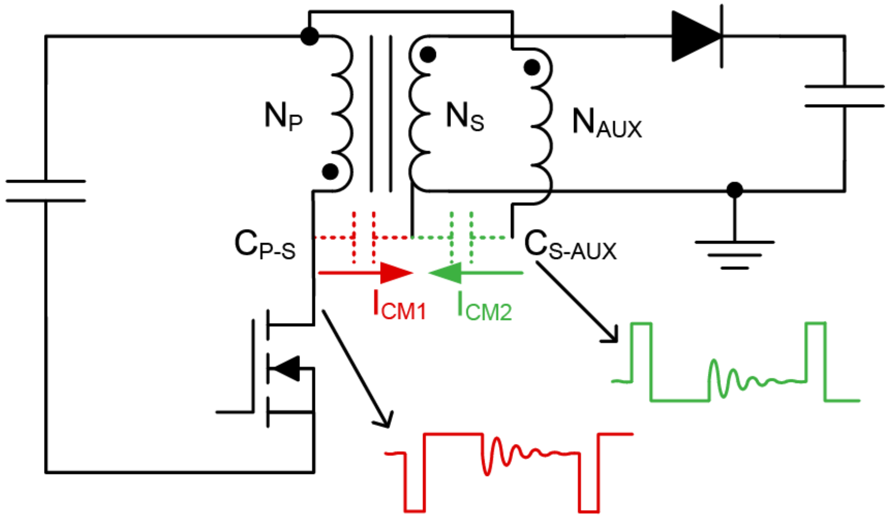


EMC CONSIDERATIONS

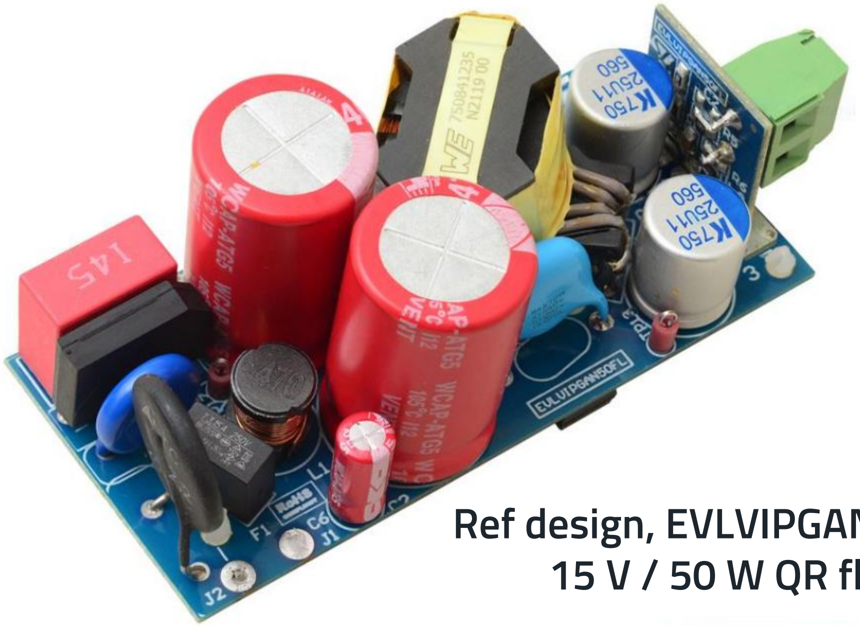
- **CM MITIGATION BY CANCELLATION/BALANCE**

- Single-ended topologies – can add explicit additional cancellation elements
  - Add auxiliary (AUX) transformer winding
  - AUX voltage proportional to CM waveform
  - Arrange AUX polarity for opposite phase

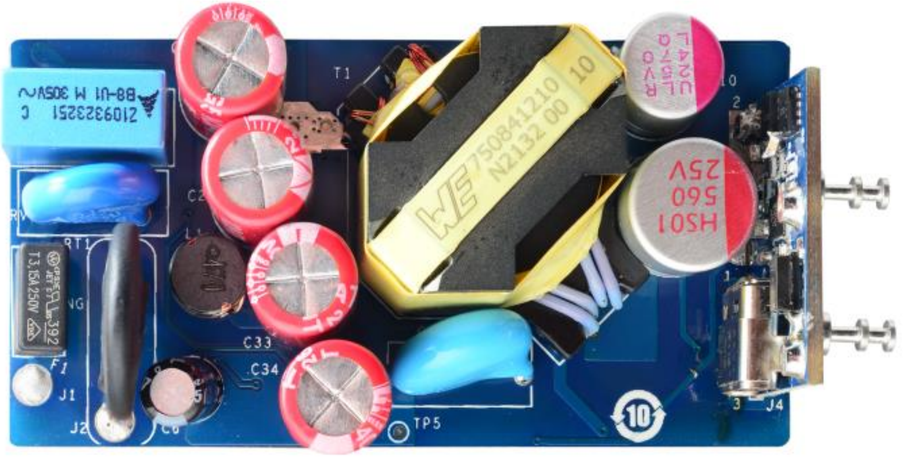
  - Capacitor to inject cancelling current, I_{CM2}, to balance CM current from primary, I_{CM1}
  - Injection capacitor explicit physical component added to design
  - Or can use parasitic capacitance, e.g., $C_{S\text{-}AUX}$, part of transformer structure



DESIGN AND CONCLUSION

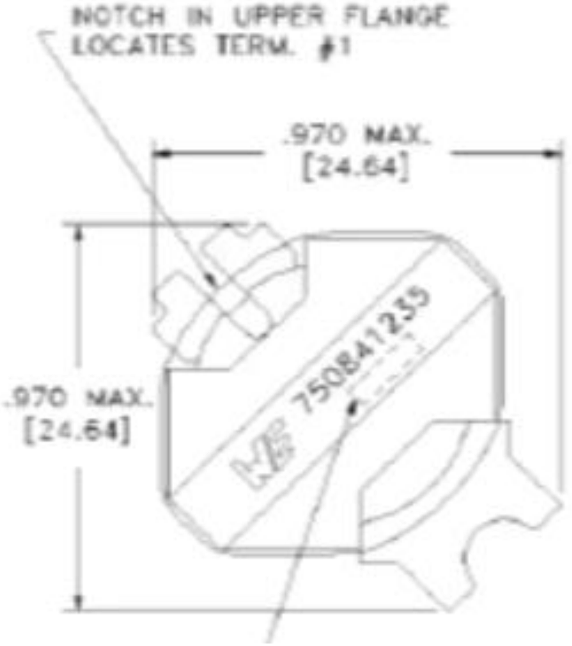


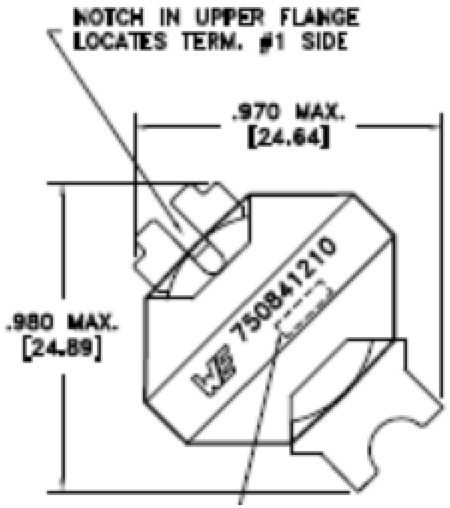
Ref design, EVLVIPGAN50FL
15 V / 50 W QR flyback



Ref design, EVLVIPGAN50PD
45W QR USB PD

Ref design, EVLVIPGAN65PD
65 W USB Type-C PD

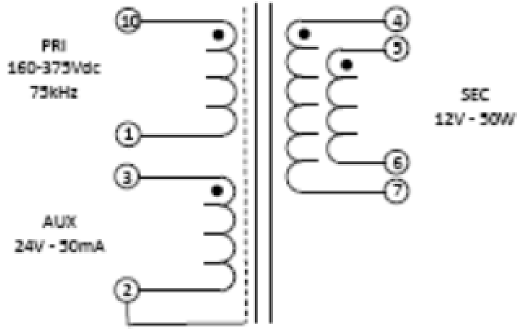




ELECTRICAL SPECIFICATIONS @ 25°C unless otherwise noted:

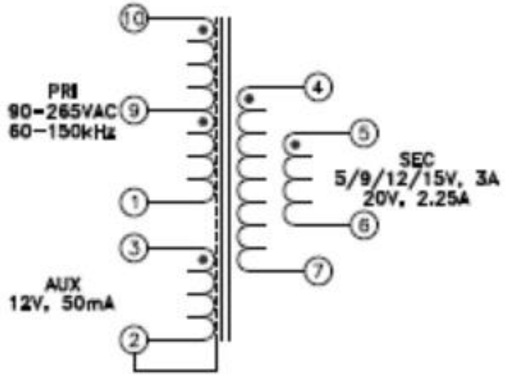
PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	10–1	@20°C	0.31 ohms max.
D.C. RESISTANCE	4–7	tie(4+5, 6+7), @20°C	0.02 ohms max.
D.C. RESISTANCE	3–2	@20°C	0.43 ohms max.
INDUCTANCE	10–1	100kHz, 100mVAC, Ls	400.00uH ±10%
SATURATION CURRENT	10–1	20% rolloff from initial	2A
LEAKAGE INDUCTANCE	10–1	tie(2+3+4+5+6+7), 100kHz, 100mVAC, Ls	8uH max.
DISTRIBUTED CAPACITANCE	10–1	100mVAC, Cs	50pF ref.
DIELECTRIC	10–4	tie(1+2, 4+5), 4000VAC, 1 second	4000VAC, 1 minute
DIELECTRIC	10–3	625VAC, 1 second	–
TURNS RATIO		(10–1):(4–7), tie(4+5, 6+7)	7.5:1
TURNS RATIO		(10–1):(3–2)	3.21:1

2%



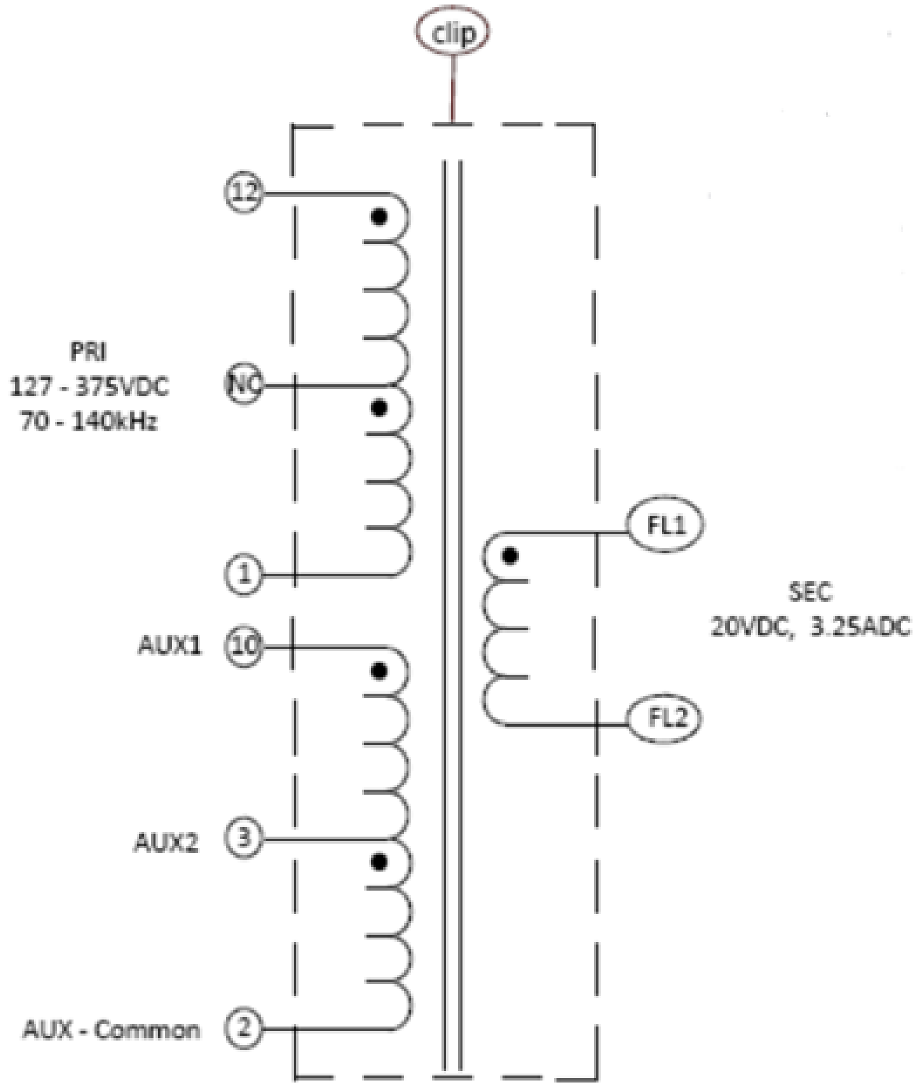
ELECTRICAL SPECIFICATIONS @ 25° C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	10-1	@20°C	0.35 ohms max.
D.C. RESISTANCE	4-7	tie(4+5,6+7), @20°C	0.01 ohms max.
D.C. RESISTANCE	3-2	@20°C	0.26 ohms max.
INDUCTANCE	10-1	100kHz, 100mV, Ls	350.00µH ±10%
SATURATION CURRENT	10-1	20% rolloff from initial	2.3A
LEAKAGE INDUCTANCE	10-1	tie(2+3+4+5+6+7),100kHz, 100mV, Ls	4.5µH typ., 8.0µH max.
DISTRIBUTED CAPACITANCE	10-1	100mVAC, Cs	40pF typ., 70pF Max.
DIELECTRIC	10-4	tie(1+2,4+5), 4000VAC, 1 second	4000VAC, 1 minute
DIELECTRIC	10-3	625VAC, 1 second	
TURNS RATIO		(10-1):(4-7), tie(4+5,6+7)	13.33:1
TURNS RATIO		(10-1):(3-2)	5:1



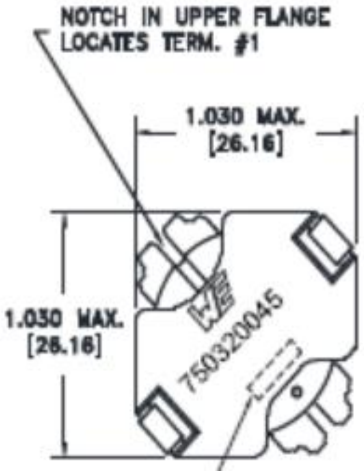
Customer to tie terminals 4+5 and 6+7 on PC board.

Application of the transformer allows for the leadwires between terminals 4&5 and 6&7 to solder bridge.



ELECTRICAL SPECIFICATIONS @ 25° C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	12-1	@20ºC	0.335 ohms ±10%
D.C. RESISTANCE	10-3	@20ºC	0.079 ohms ±10%
D.C. RESISTANCE	3-2	@20ºC	0.220 ohms ±10%
D.C. RESISTANCE	FL1-FL2	@20ºC	0.016 ohms ±20%
INDUCTANCE	12-1	100kHz, 100mV, Ls	500µH ±10%
SATURATION CURRENT	12-1	20% rolloff from initial	3.5A
LEAKAGE INDUCTANCE	12-1	tie(2+3+10,FL1+FL2),100kHz, 100mV, Ls	4.5µH typ., 7.5µH max.
DIELECTRIC	12-FL1	tie(1+10), 3650VAC, 1 second	3650VAC, 1 minute
DIELECTRIC	12-10	625VAC, 1 second	500VAC, 1 minute
TURNS RATIO		(12-1):(10-2)	2.53:1
TURNS RATIO		(12-1):(3-2)	3.43:1
TURNS RATIO		(12-1):(FL1-FL2)	6:1



CONCLUSION

- Flyback Transformers are about storing Energy
- Trasformer structre impacts the leakage inductance
- Saturation current limitations
- Considering AC Resistance in the design of the transformer
- Decreasing EMI issues with increasing switching frequency