Brief Overview - Design of a SPE with PoE – PoDL Interface

Digital Days 2025

Dr.-Ing. Heinz Zenkner, Application Engineering, Technical Marketing
Adrian Stirn, Technical Lead EMC Laboratory

Würth Elektronik eiSos

Agenda

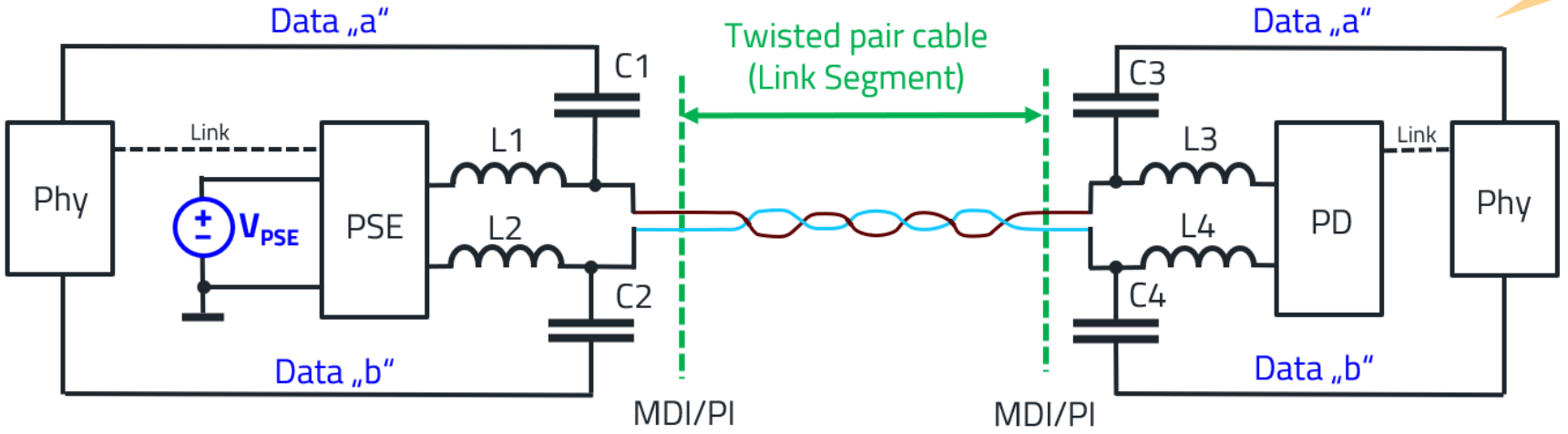
- Introduction and technical background
- Design parameters to consider for a normative- and EMC-compliant application
- Hardware topology of a SPoE – system
- WE – design of the 10 Mbit/s - SPoE – system
  - The Power Sourcing Equipment (PSE)
  - The Powered Device (PD)
- General design information
- The SPoE Interface from an EMC perspective

Introduction and technical background

1. Introduction and Technical Background

- Single Pair Ethernet (SPE) with power over the wires (PoE) = SPoE: Power over 2-wire Ethernet data cables together with the data
  - Different in definition and implementation compared to conventional PoE.
    - Unique power coupling techniques used in a 2-wire system.
    - Simultaneous transmission of power and data over a balanced twisted pair.

Power supply inductively decoupled
Signal capacitively coupled



A technically possible option, not the final concept!

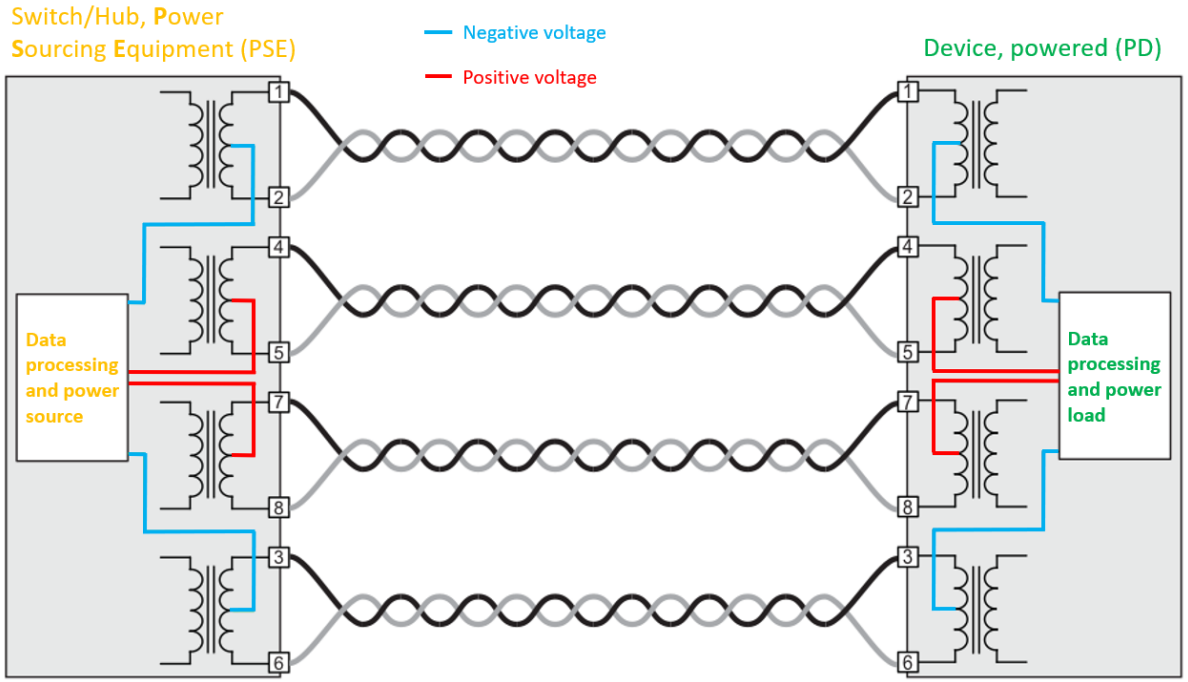
- Data connections via single pair of wires, AC-coupled at each end “to avoid ground loops”.
  - Conventional PoE systems transmit power in common mode to the differential data lines.
  - SPoE systems diplex power **and** data over a **single pair of conductors - both in differential mode**.

MDI: Media Dependant Interface
PI: Port Interface
PD: Powered Device
PSE: Power Source Device
Phy: Physical Layer

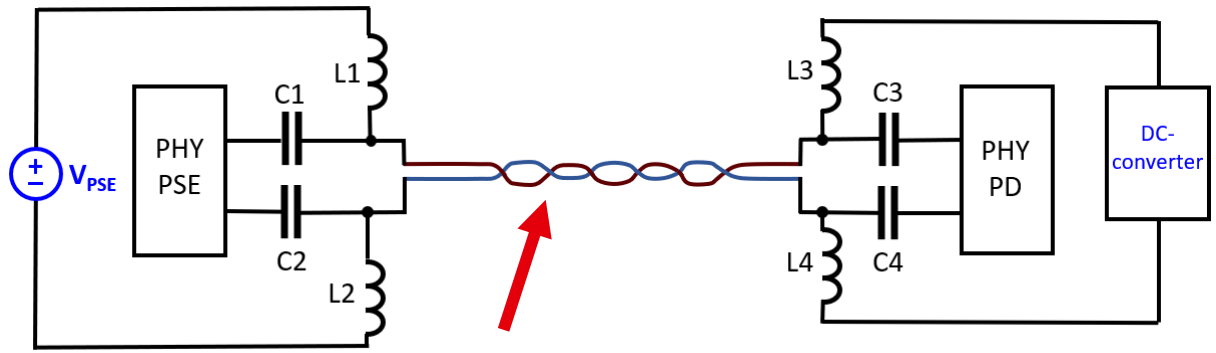
1. Introduction and Technical Background

- SPoE = SPE - PoDL system principle
- **S**ingle **P**air **E**thernet using **P**ower **o**ver **D**ata **L**ine is not the same as Power over Ethernet (PoE)
  - PoE requires a special network switch with one device connected to each port using a CAT 5 cable.
  - PoDL systems feature: Supply: 12 V, 24 V, 48 V / Power: 0,5 W - 50 W / Max. current: 2 A (higher than with PoE)

- Power over Ethernet (PoE), basic principle



- Power over Data Line (PoDL), basic principle



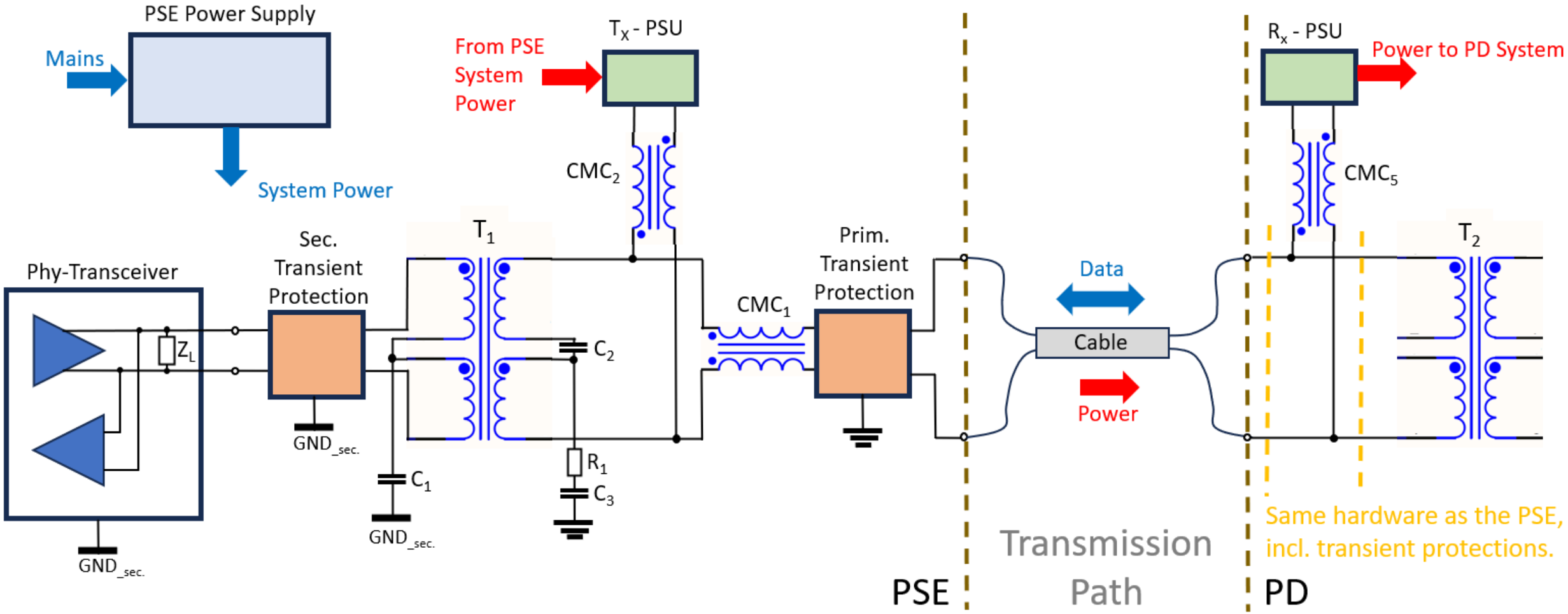
Full data rate over **one** channel!

Data is distributed to **4 channels**!

Hardware Topology of a PoDL - System

2. Hardware Topology

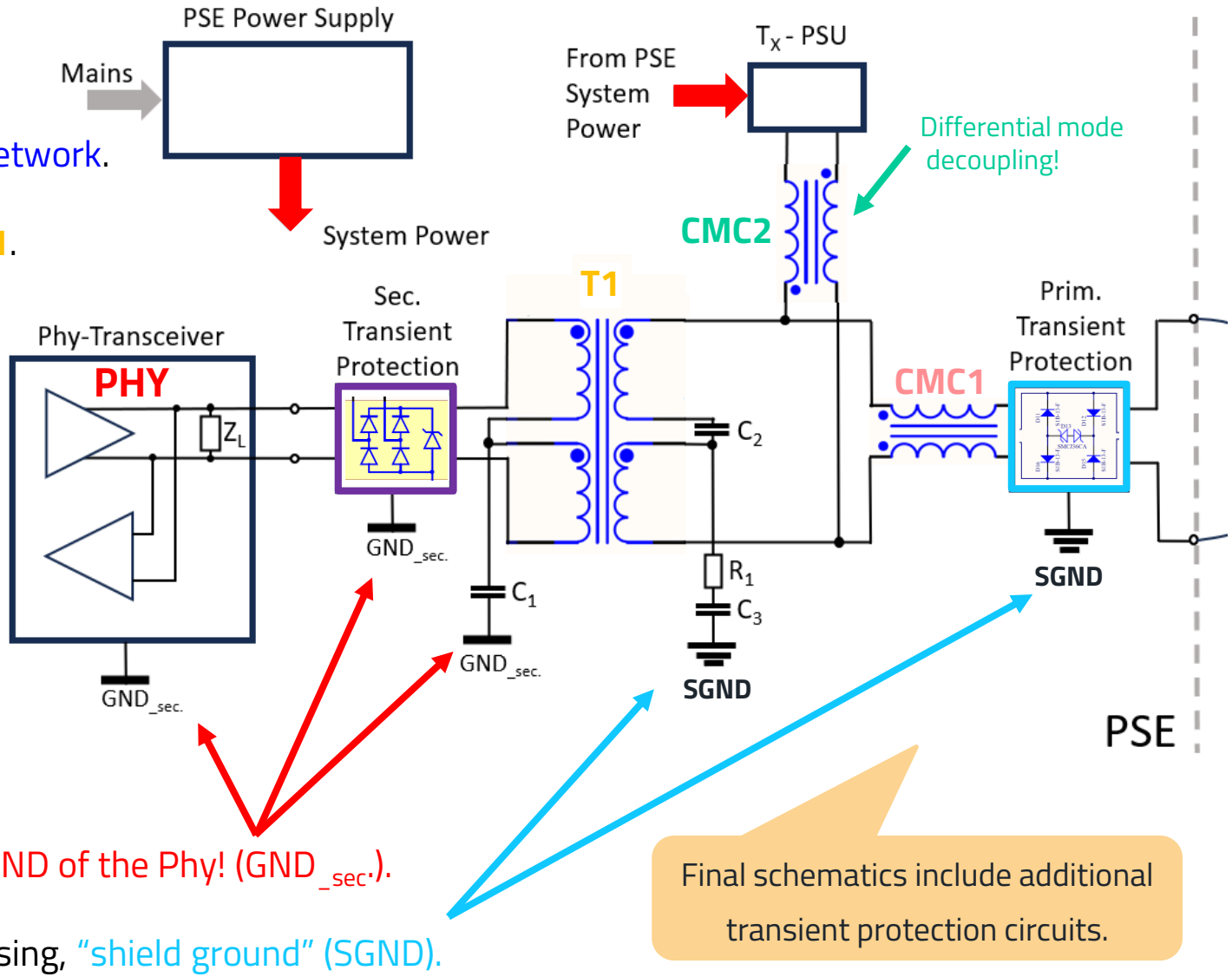
- Interface block diagram



2. Hardware Topology

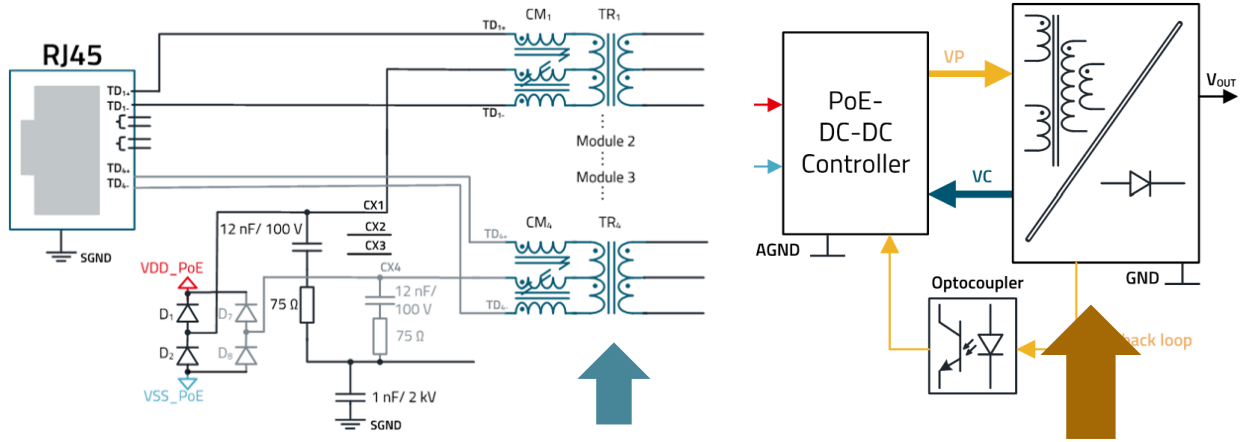
- Interface block diagram, magnetics

- Power and data coupled together by a power coupling network.
  - The **PHY** is AC-coupled by the signal transformer **T1**.
  - **CMC1** attenuates common mode noise from the data line to the Phy and vise versa.
  - The PSE DC power is coupled onto the differential signal lines, the signal is decoupled by **CMC2**.
- The **magnetics** (Tx, CMCx) must be selected to meet the droop, return loss, and mode conversion specifications according to IEEE 802.3cg.
- Transient protection
  - **Secondary side**, on the Phy side: Reference is the GND of the Phy! ($GND_{\_sec.}$).
  - **Primary side**, at the interface: Reference is the housing, "shield ground" (SGND).



2. Hardware topology

- Interface block diagram, galvanic isolation
- In conventional IEEE 802.3 multipair Ethernet (including PoE)
  - Galvanic isolation from the chassis ground is done by a **signal transformer** and an **isolated DC-DC converter**.



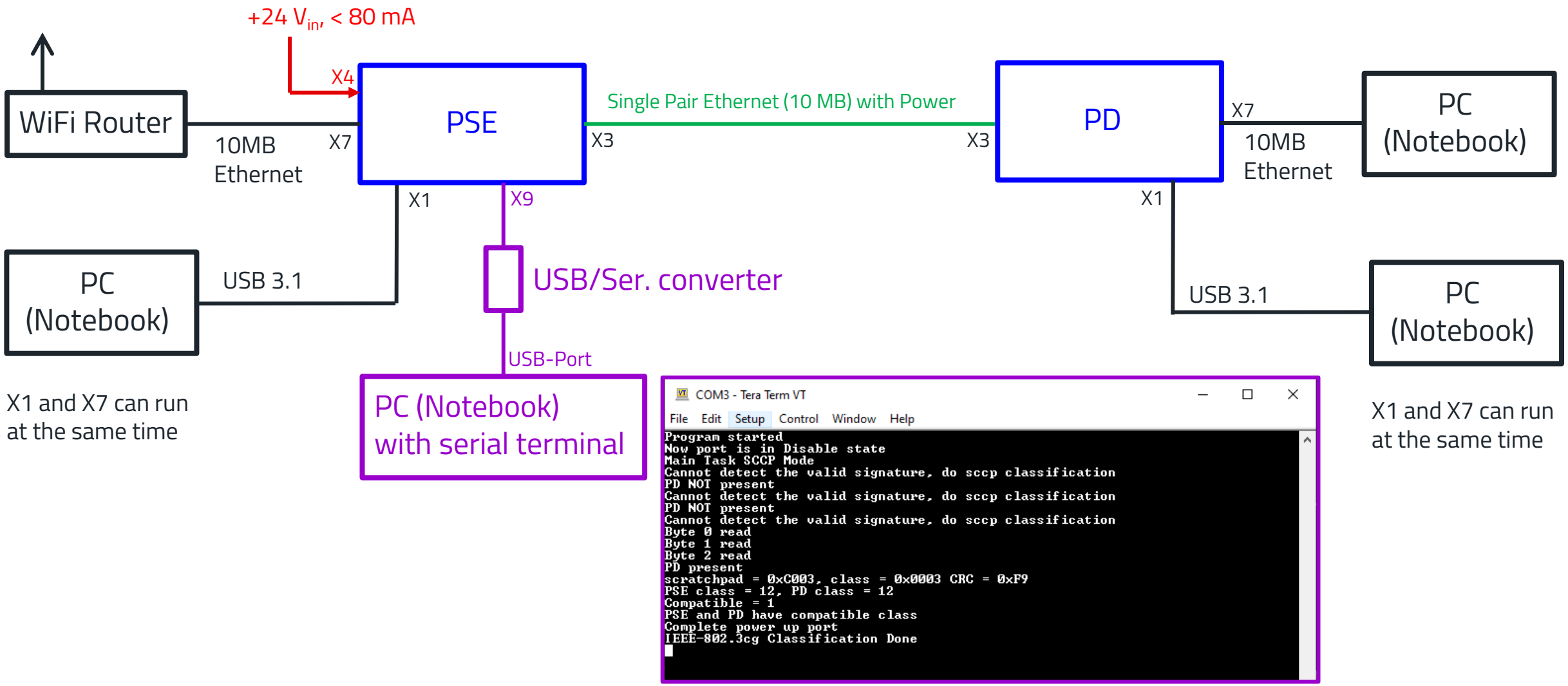
- In SPoE: IEEE 802.3bu (PoDL) and IEEE 802.3cg (SPoE)
  - PDs must provide at least 1 MΩ (@ 5V ± 20%) isolation between all accessible external conductors and the interface (MDI).
  - Although not explicitly required by standard, the PSE should also be galvanically isolated as state of the art.
    - Equipment must comply with relevant product safety standards, e.g. IEC 61010-1, IEC 62368-1, IEC 60601-1.
      - Isolated power supply must be used.
      - Relevant safety standard requirements (clearance and creepage distances, protective distances) must be followed.

WE-Design of a SPoE – System

Block Diagram of the System

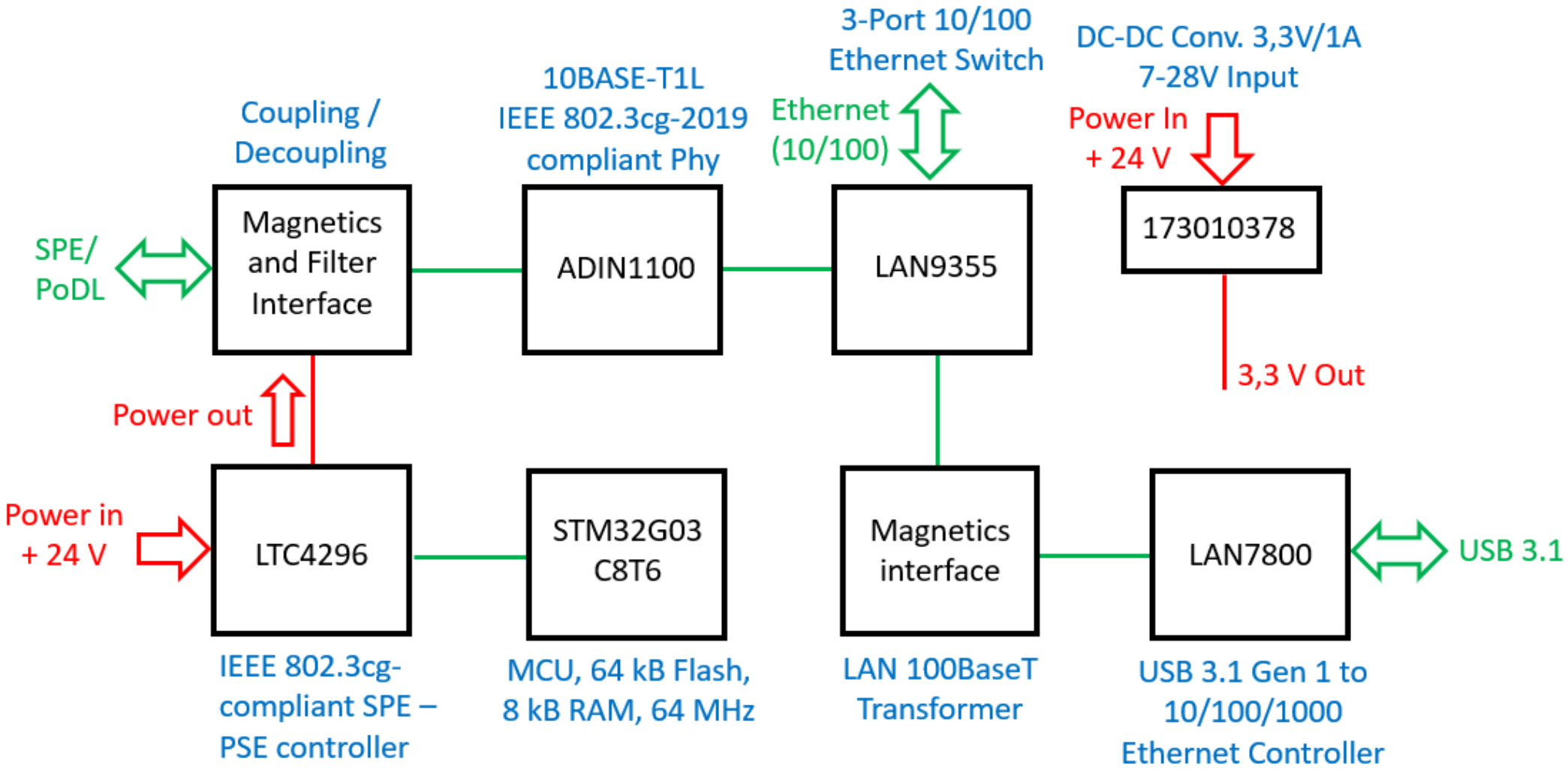
3. WE-Design

- Block diagram WE-System



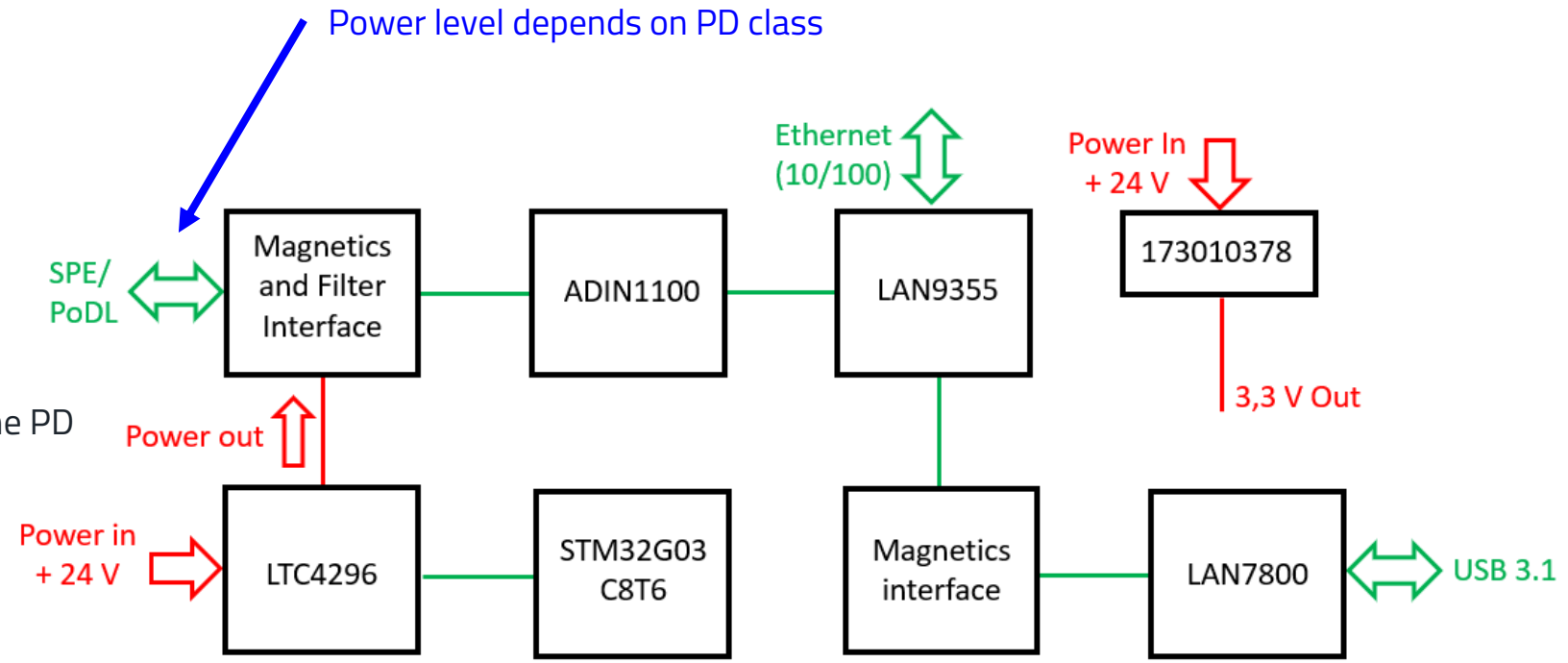
3. WE-Design

- Block diagram WE-System, **PSE** (1/2)



3. WE-Design

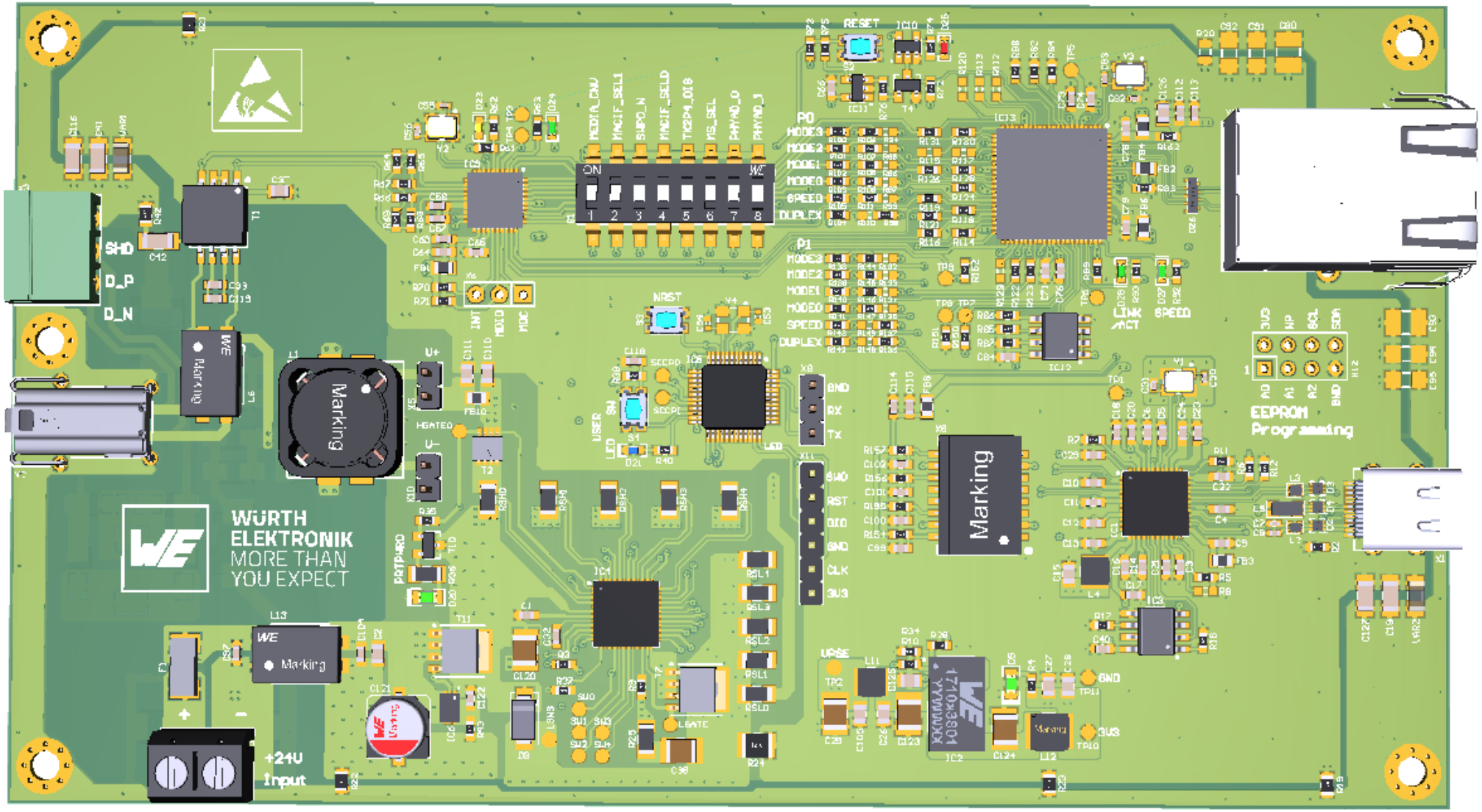
- Block diagram WE-System, **PSE** (2/2)
- Features
  - Supports multiple SPoE power levels
  - Detecting and classifying the PD
  - 10 MB SPE port
    - PoDL class 12 up to 30 V / 8,3 W at the PD
  - USB 3.1 port (no power)
  - 10/100 MB Ethernet port



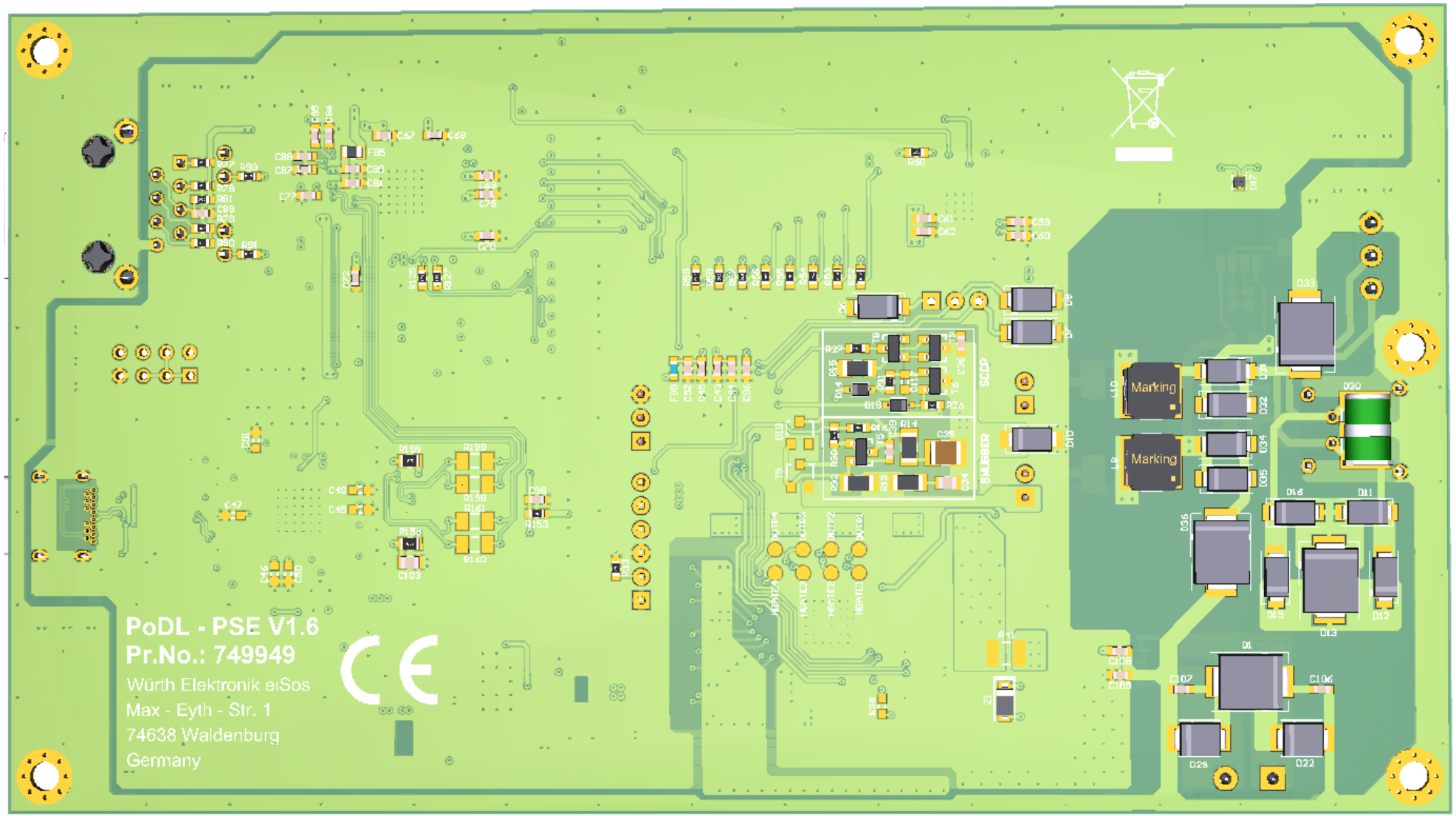
- Data transfer between USB 3.1 and 10/100 MB Ethernet
- Data transfer between USB 3.1 and SPE
- Data transfer between SPE and 10/100 Ethernet

Data transmission across multiple ports

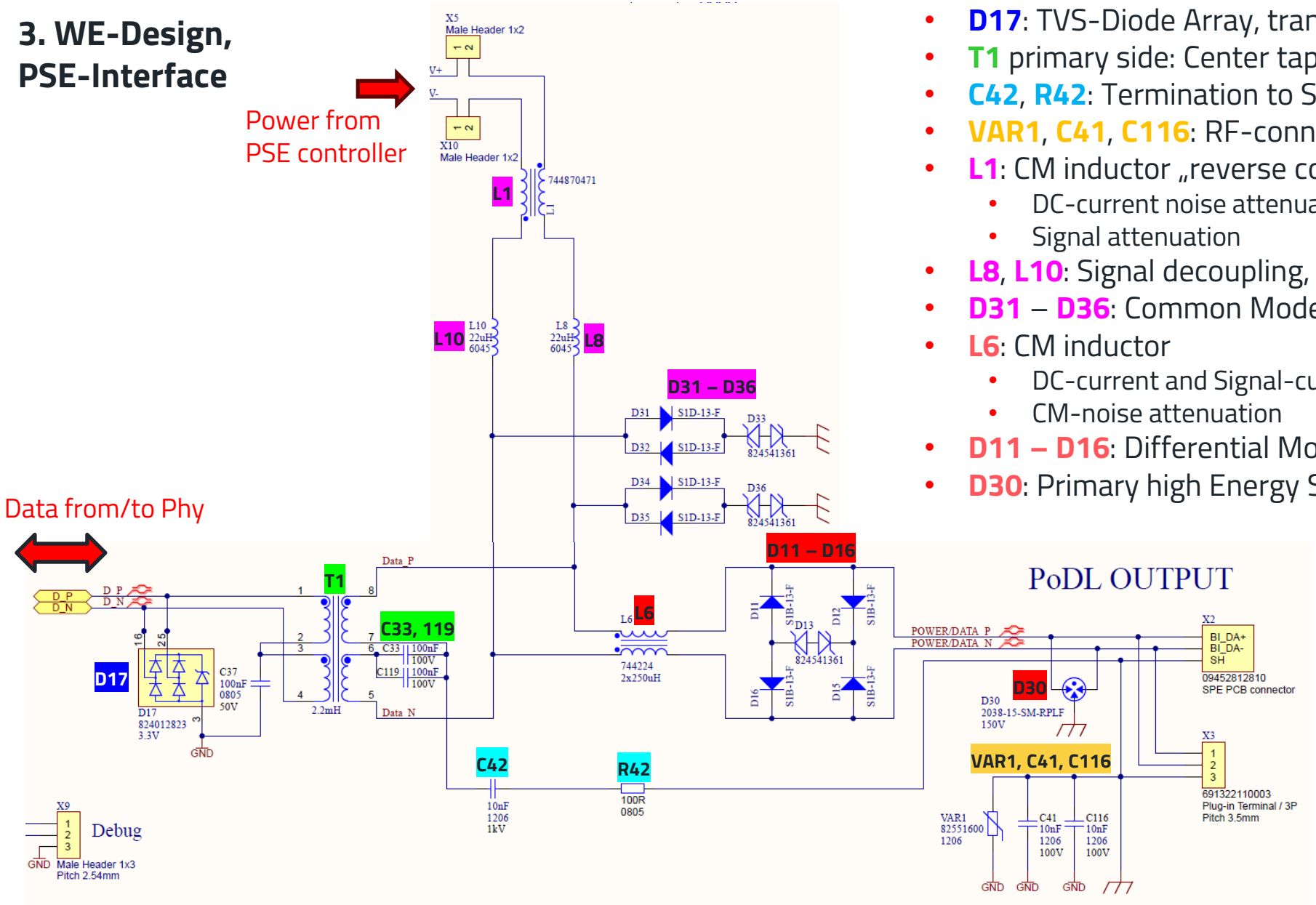
3. WE-Design, The PSE hardware (3D – graphics 1 of 2))



3. WE-Design, The PSE hardware (3D – graphics 2 of 2)



3. WE-Design, PSE-Interface

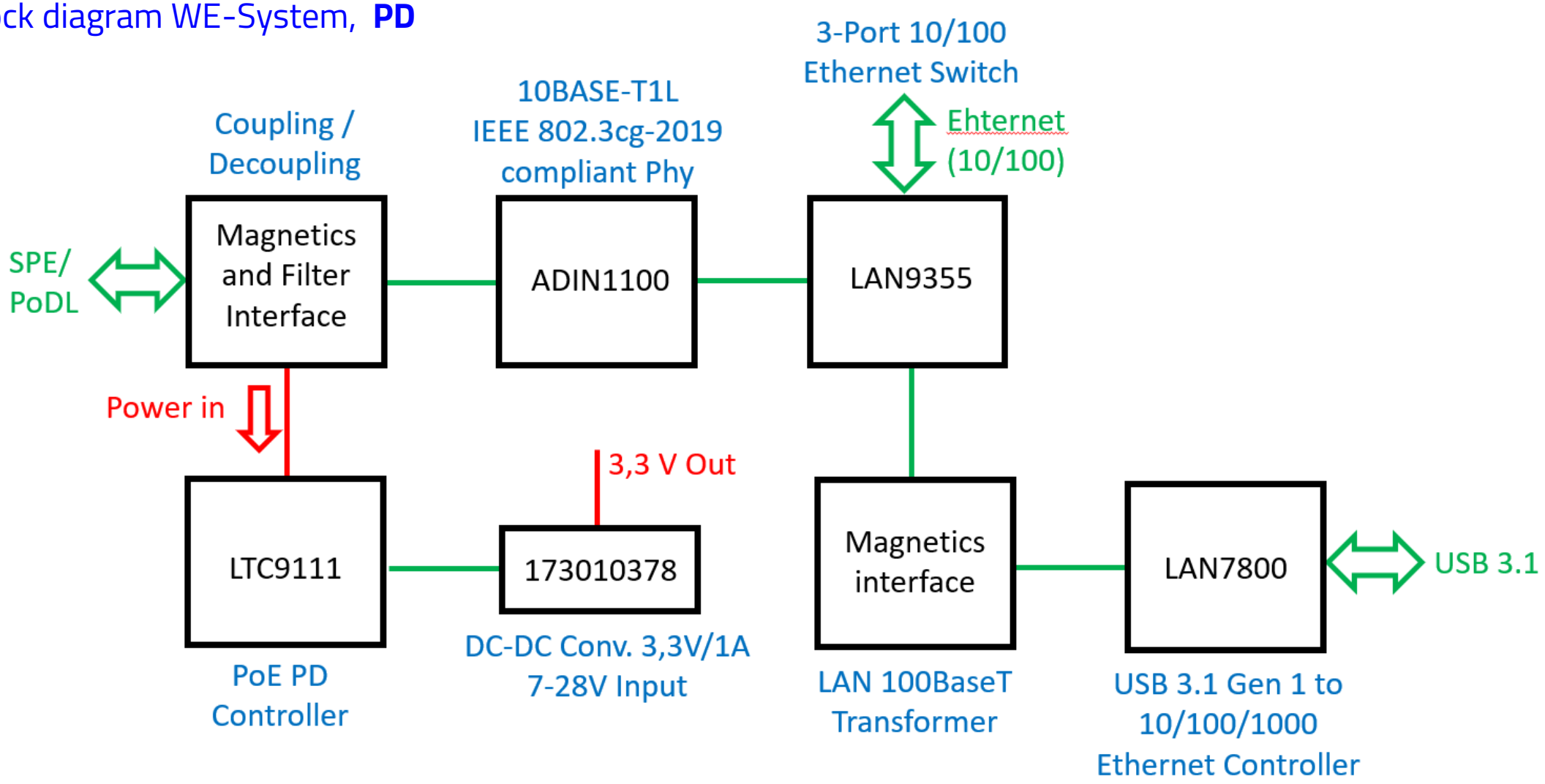


- **D17**: TVS-Diode Array, transient protection towards Phy
- **T1** primary side: Center tapping, **C33**, **C119** galvanic separation
- **C42**, **R42**: Termination to SGND
- **VAR1**, **C41**, **C116**: RF-connection between GND and SGND
- **L1**: CM inductor „reverse connected“ -> differential mode att.
  - DC-current noise attenuation
  - Signal attenuation
- **L8**, **L10**: Signal decoupling, inductors for higher frequency range
- **D31** – **D36**: Common Mode Surge protection
- **L6**: CM inductor
  - DC-current and Signal-current compensation
  - CM-noise attenuation
- **D11 – D16**: Differential Mode transient protection
- **D30**: Primary high Energy Surge protection

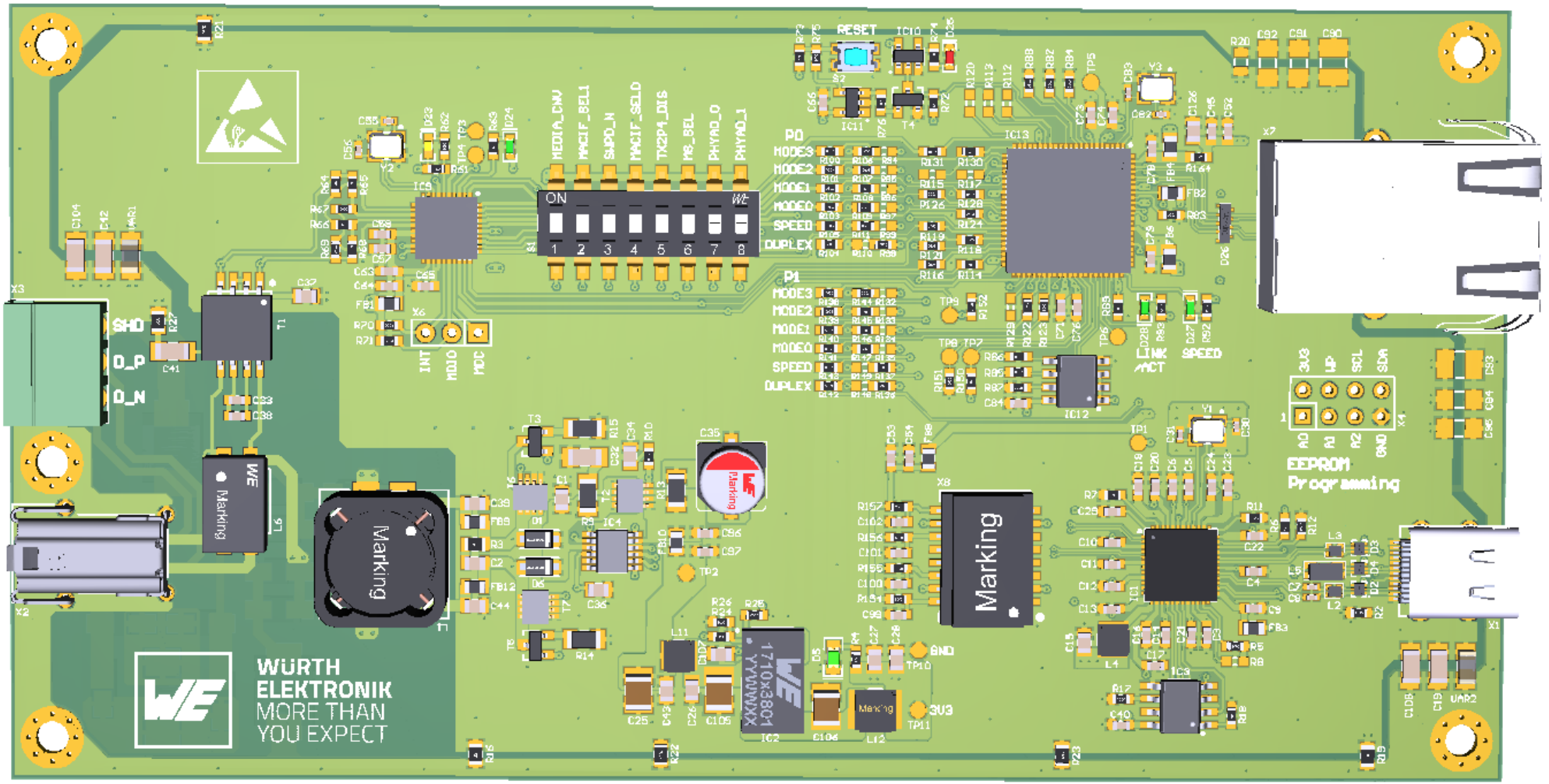
WE-Design of a PoDL – System
Powered Device (PD)

3. WE-Design

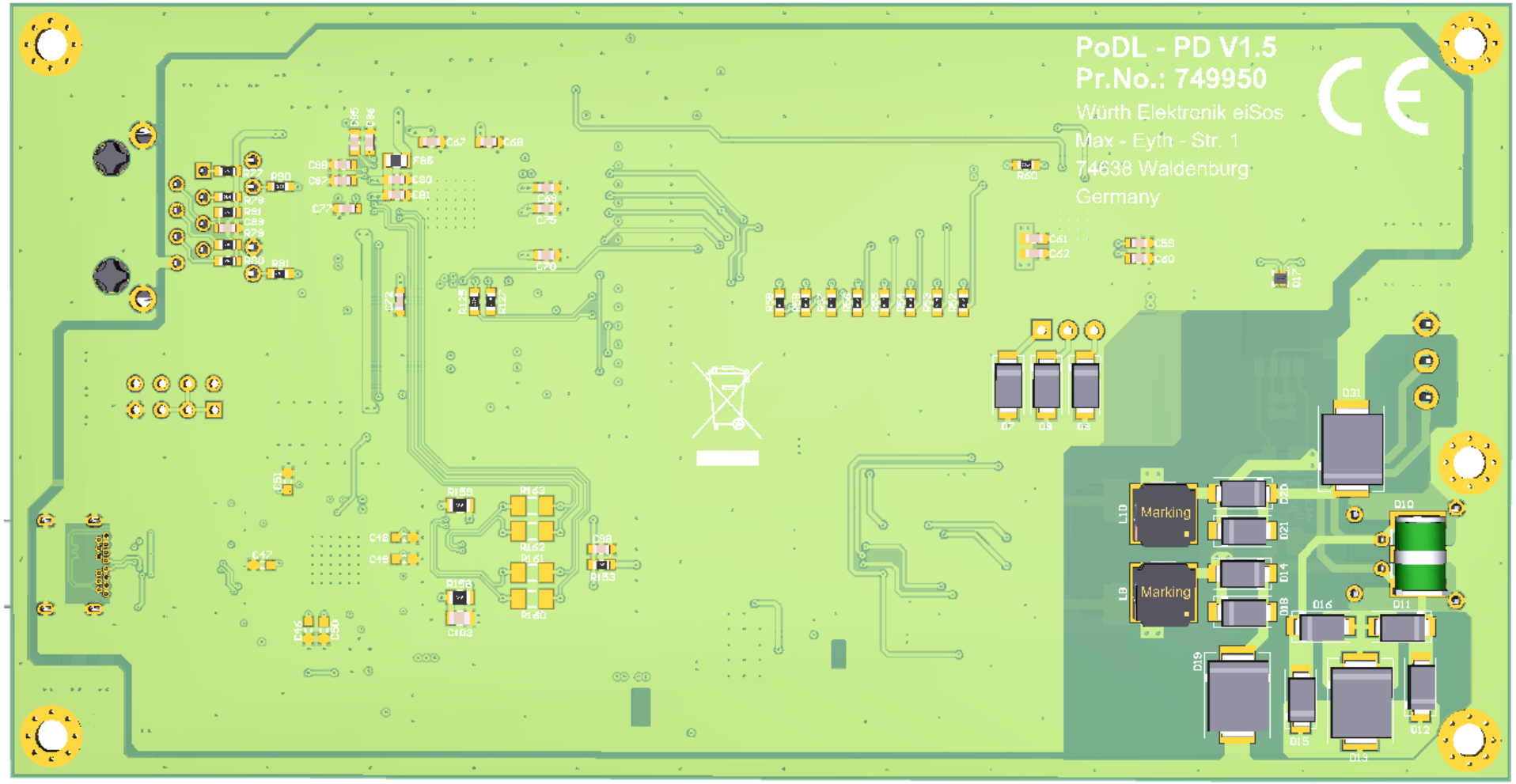
- Block diagram WE-System, **PD**



3. WE-Design, The PD hardware (3D – graphics, 1 of 2)



3. WE-Design, The PD hardware (3D – graphics, 2 of 2)



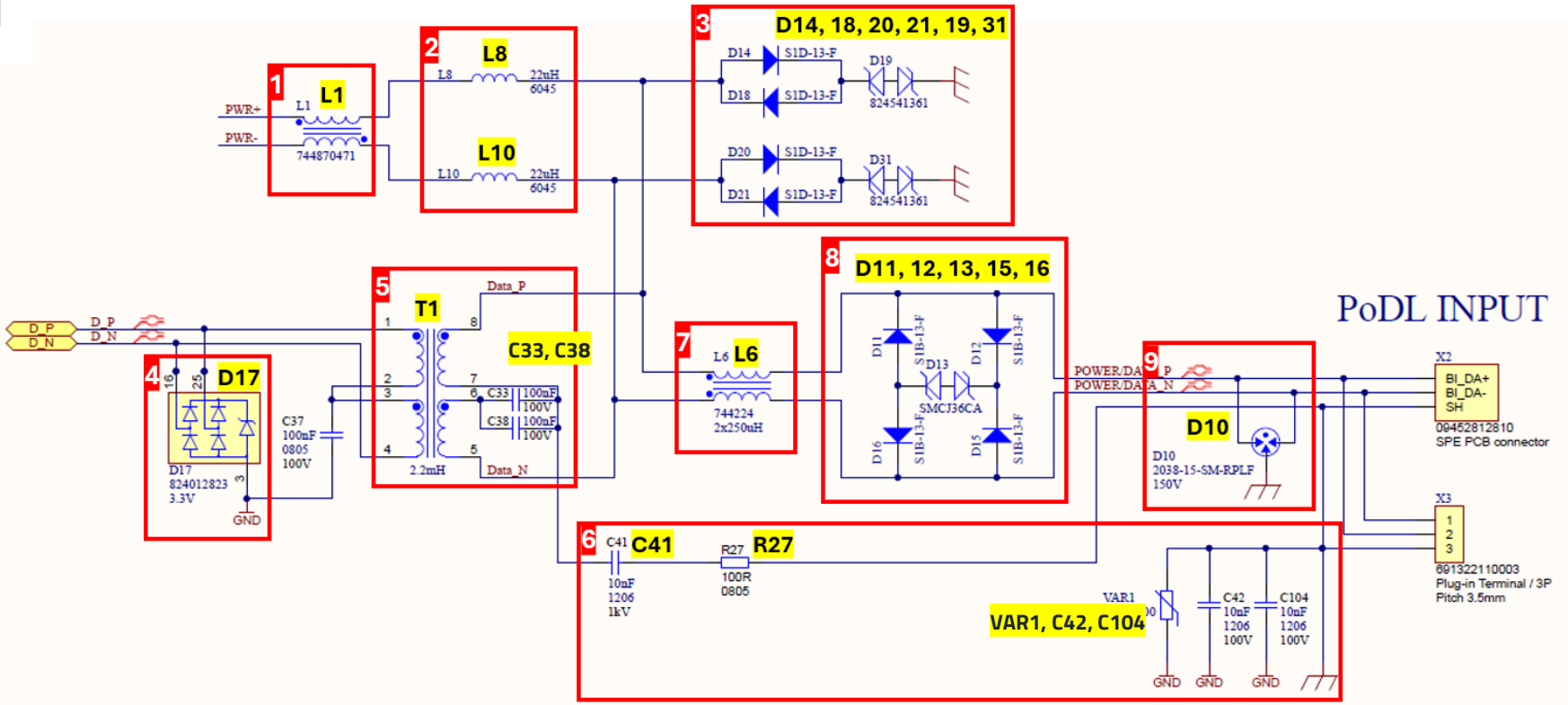
3. WE-Design, schematics in detail

- PD interface

1 CM-Inductor
- No current compensation
- Differential Mode attenuation of
  - SPE-Signal
  - DC-supply noise

2 Inductors for high frequency noise attenuation

3 Common Mode transient protection



4 Common Mode transient protection of Phy inputs (GND reference to Phy)

5 Primary side: Center tapping; C33 and C38 for DC-block

6 Termination circuit to SGND and connection to GND via VAR1/C42 and C104

7 CM-Inductor, „no“ attenuation for signal, compensated against DC-current

8 Differential Mode transient protection by bi-directional TVS-Diode

9 Primary high energy CM / DM transient protection (GAS discharge tube)

Chapter 4
General Design Information

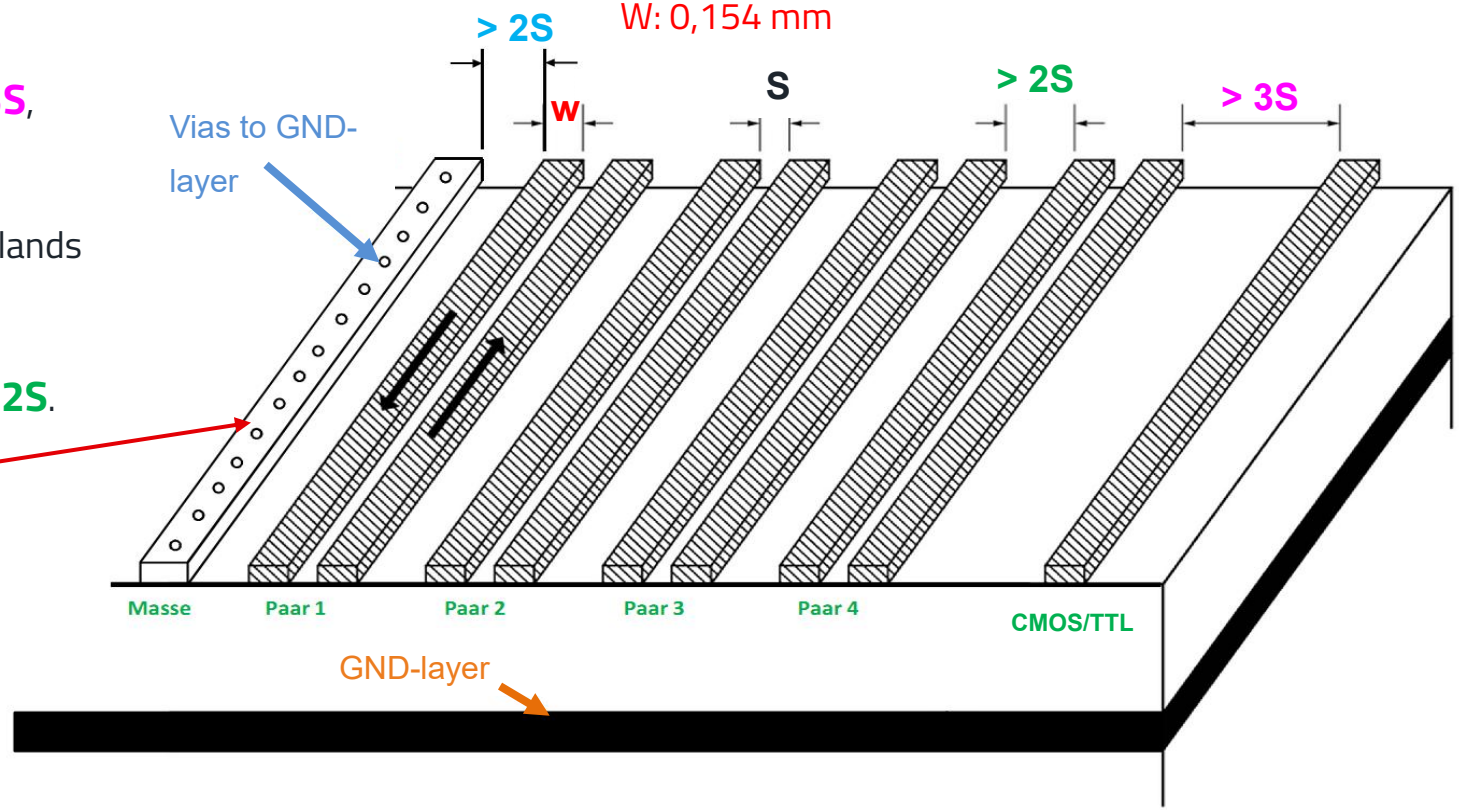
4. General Design Information

Layout considerations

- Use of at least 4-layer PCBs, VCC and GND on the inside.
- Blocking capacitors for the Phy must be placed directly at the IC.
  - 4,7uF/0,1uF/1nF capacitors at each V_{CC}-Pin.
  - Inductance of the traces L < 1,5 nH - 2 nH.
- Distance from other traces to the Ethernet traces **w > 3S**, to avoide cross coupling.
- Distance between the Ethernet traces and the ground islands in the same layer **> 2S**.
- Distance between adjacent Ethernet differential pairs **> 2S**.
- If **ground fill** is too close to differential lines on the same layer, the signal trace topology shifts from a pure edge-coupled pair to a coplanar waveguide with ground or a hybrid microstrip/CPW, depending on spacing. Keep **w > 3S**

- Example: GB Ethernet
  - Maximum length offset between pairs (inter-pair): 50 mm (< 330 ps)
  - Maximum length offset within a pair (intra-pair): 250 um (< 1.6 ps)

Depending on the substrate (here Prepreg: 0,2 mm):
S: 0,125 mm
W: 0,154 mm



4. General Design Information

- PCB and Signal Integrity
- Layer stacking

ε_r

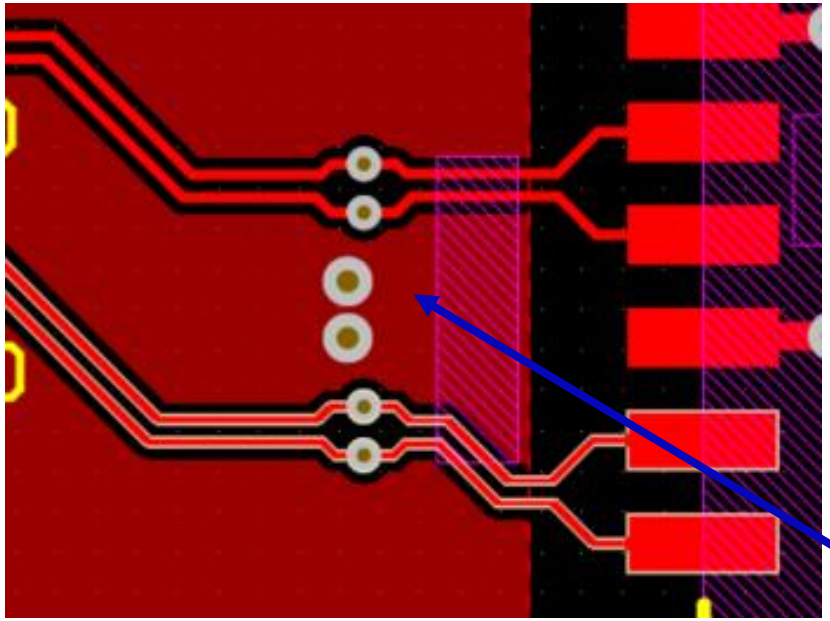
#	Name	Material	Type	Weight	Thickness	Dk
	Top Overlay		Overlay			
	Top Solder	Solder Resist	Solder Mask		0.0127mm	3.8
1	**Top Layer**		Signal	1oz	0.035mm	
	Dielectric 1	7628	Prepreg		0.2mm	4.6
2	**GND**		Plane	1/2oz	0.0175mm	
	Dielectric 2	FR4	Core		1.065mm	4.6
3	**Power plane/GND**		Signal	1/2oz	0.0175mm	
	Dielectric 3	7628	Prepreg		0.2mm	4.6
4	**Bottom Layer**		Signal	1oz	0.035mm	
	Bottom Solder	Solder Resist	Solder Mask		0.0127mm	3.8
	Bottom Overlay		Overlay			

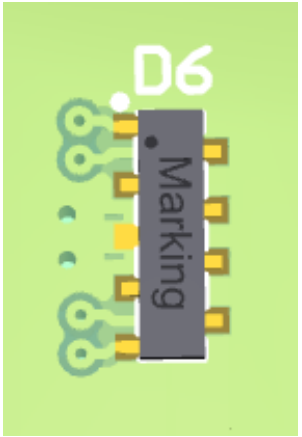
General Design Information
ESD Protection and related grounding

4. General Design Information

- Grounding on PCB, Filter ground, ground to limit transient voltages

- The TVS diode arrays must be connected directly into the signal path and to GND to avoid voltage drop due to parasitic inductances.

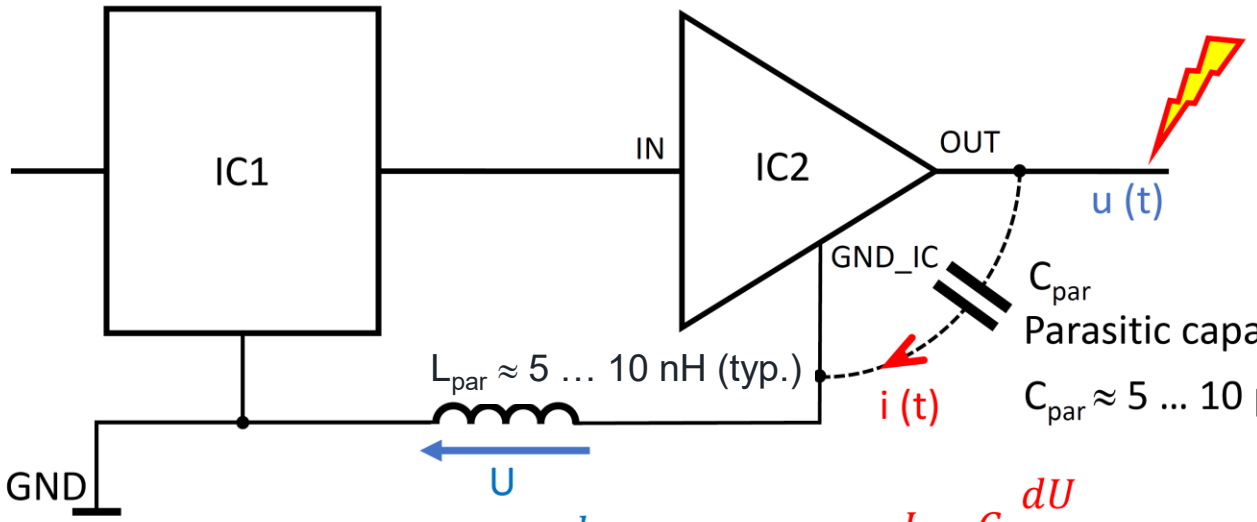




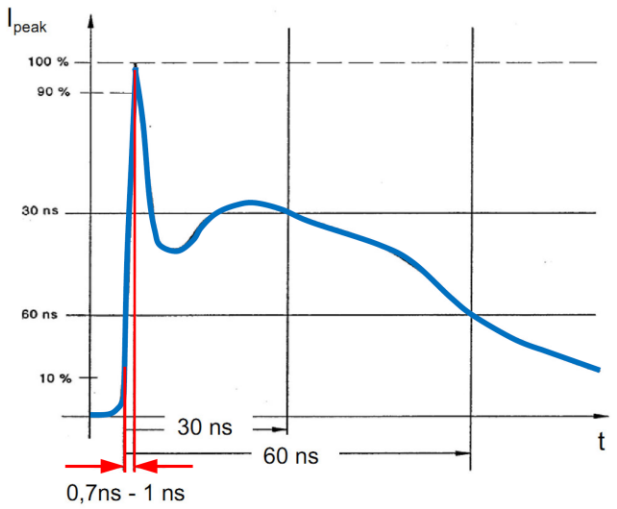
What is „**directly**“, what is a „**parasitic inductance**“?

4. General Design Information

- Grounding on PCB, Filter ground, ground to limit transient voltages
- A simple estimation (1/3)



ESD, e.g. by discharge to shield and capacitive coupling into the wire



$$U = L_{par} \frac{d_i}{d_t}$$

$$I = C \frac{dU}{dt}$$

$$I = C \cdot \frac{dU}{dt} \qquad ESD: \frac{1000V}{1ns}$$

- Different reference grounds
- Different ground potentials

Causes damage of components

- Parasitic capacitance of IC
- Charging current of C_{par}

Causes damage of components

4. General Design Information

- Grounding on PCB, Filter ground, ground to limit transient voltages

- A simple estimation (2/3)

- Parasitic chip-internal capacitance of the controller output causes a current in the event of a discharge.
- The parasitic inductance results from the IC connections, the ground configuration of the assembly and the assembly screw connection. The current flow is high!

- **Charging of the parasitic capacitor**

$$I = C \cdot \frac{dU}{dt} \qquad ESD: \frac{1000\,V}{1ns}$$

  - Here only 1 kV
  - According IEC61000-4-2: 8 kV
  - In practice up to 25 kV

$$I = 5 \cdot 10^{-12}\,pF \cdot \frac{1000\ V}{1\,ns} = \underline{\underline{5A}}$$

- **Influence of the parasitic ground inductance**

1 cm wire: L = 10 nH (typ. value: 10 nH/cm)

Current of ESD impulse: I = 30 A/nS (acc. to standard)

$$U = L \cdot \frac{di}{dt} \qquad \Rightarrow U = 10 \cdot 10^{-9}\ \mathrm{H} \cdot \frac{30\,A}{1ns} = 300\,V$$

→ In both cases the device will be damaged!

4. General Design Information

- Grounding on PCB, Filter ground, ground to limit transient voltages

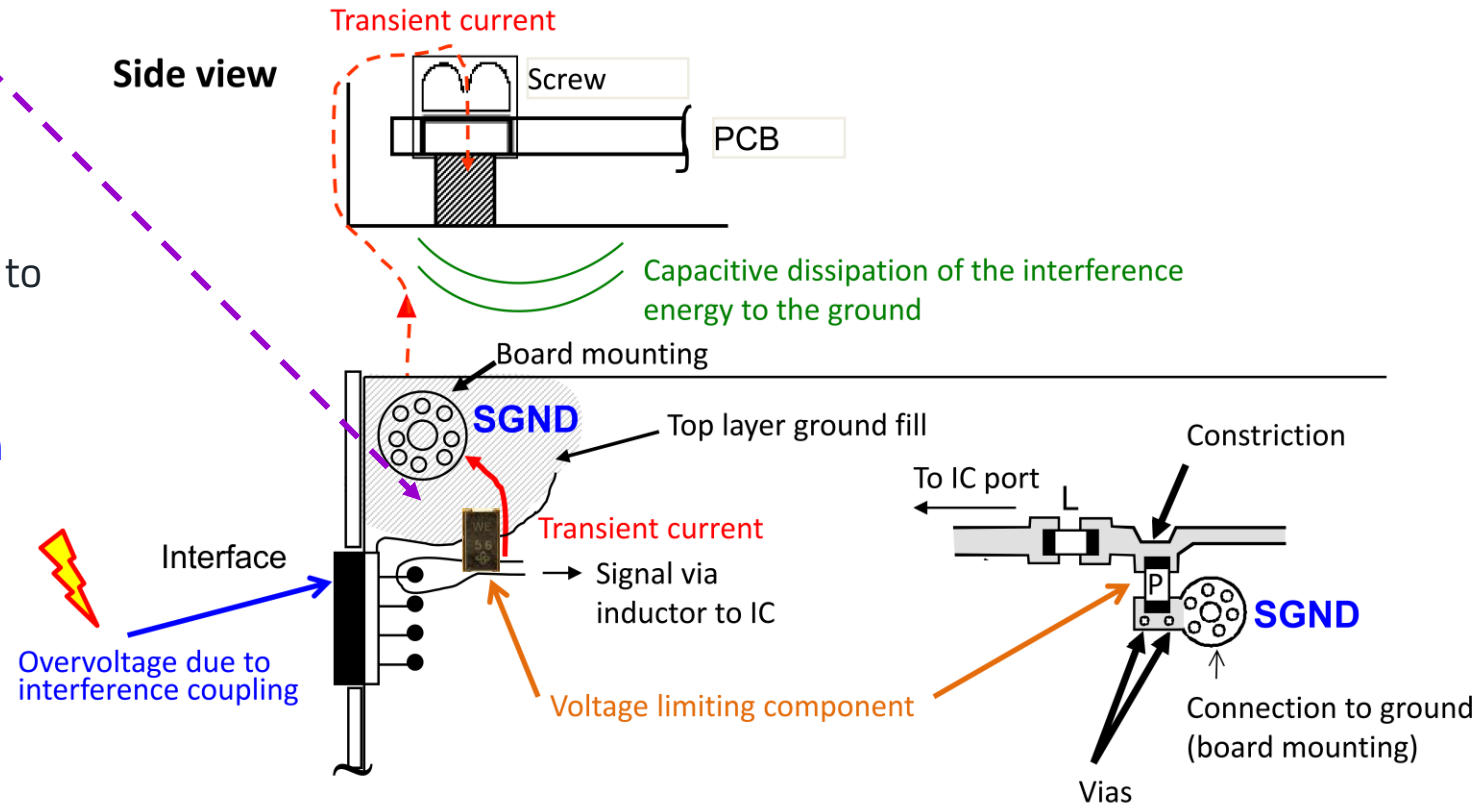
- A simple estimation (3/3)

- Ground connection directly at the clamping point / reference GND → keeping parasitic inductances and contact resistances as low as possible.

- TVS-Diode parameters must be selected according to signal bandwidth and/or interface voltage levels (AC, DC).

- Other traces should be placed at least 4 mm apart to avoid inductive and capacitive coupling.

- The PCB around the components can be filled with ground **and** plated through to the ground layer several times by large VIAs.



4. General Design Information

- The Reference Design Kit

- Content of the kit
  - PSE board compatible with PoDL class 12 providing up to 30 V/8.3 W detecting and classifying the PD to supply the correct power.
  - PD board operating at a voltage of 24 V and using the SCCP protocol for power classification.
  - 1.5 m single pair twisted cable
  - 2 WR-TLB connectors

https://www.we-online.com/en/support/knowledge/application-notes?d=rd041-design-of-a-single-pair-ethernet-system-with-power-over-data-lines

Application Note 141: The SPoE Interface from an EMC Perspective

EN: https://www.youtube.com/watch?v=r5xBqNhQ7X0

DE: https://www.youtube.com/watch?v=6fuJT75ifF0

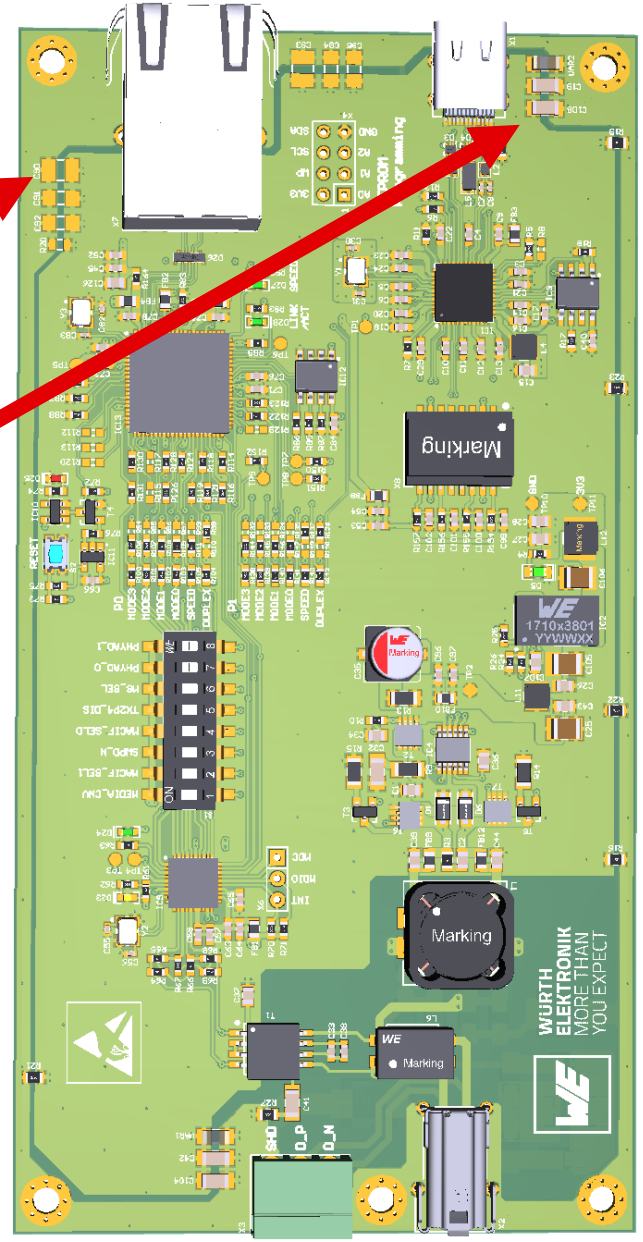
EMC-PERSPECTIVE

of the SPoE-Reference-Design

SHIELD TERMINATION SPOE REV DESIGN AND CABLES

Ethernet and SPE used as a shielded interface

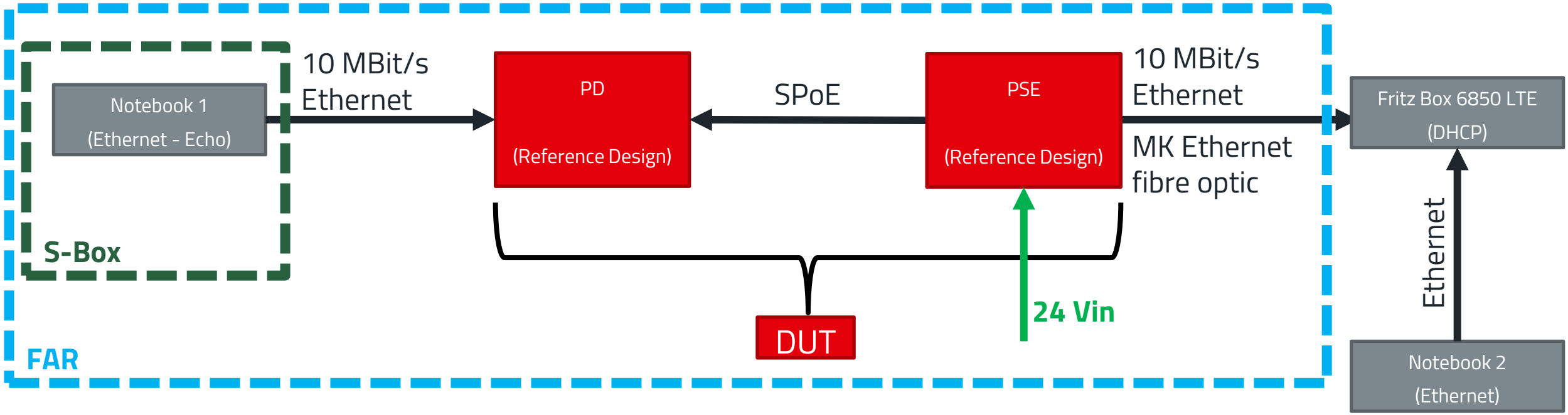
- Ethernet cable always used as shielded cable.
- Capacitive connection of the Ethernet cable shield to the GND plane:
  - 2 x 10 nF X7R 1206 MLCC 100 V (885012208112).
  - SMD Varistor (82551600).
- USB cable shield connected to the GND Plane and connected with Capacitor and Varistor to chassis-GND.
- SPE used as shielded and unshielded cable.



MEASUREMENT AND TEST SETUP

General test setup radiated emissions and immunity testing

- Two notebooks are required to test the function of the reference design.



- Notebook 1: Test-Server sending Error and Speed-Test-Data. Notebook 1 in shielded box.
- The Reference Design, SPE-Cable and 100 Mbit/s Ethernet are the DUT.
- Fritz Box 6850 defining IP-address of Notebooks.

IMMUNITY PERFORMANCE

Monitoring SW

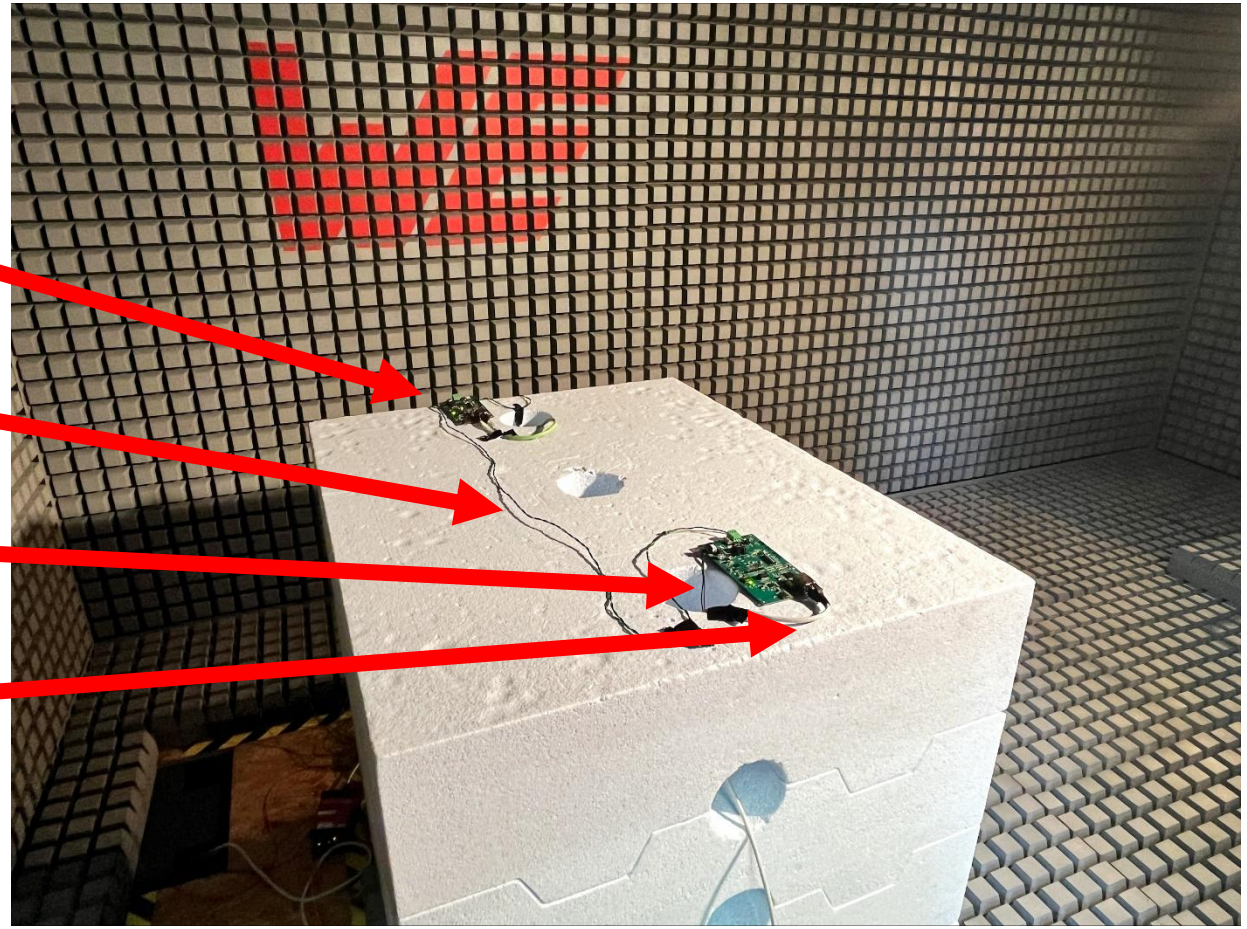
- Monitoring Notebook shows transmission speed and errors in the communication.
- 8,5 payload possible in the setup used for testing the reference design.

- As an alternative you can use iPerf to monitor the network speed between two devices.

RADIATED EMISSIONS AND IMMUNITY

Setup in FAR

- Ethernet cable shielded and only short on PD side (only vertical).
- SPE cable - 5 to 10 m cable:
  1 m horizontal in the field.
- 24 Vin cable 1 m horizontal in the field in cable channel of the table.
- Ethernet cable shielded on PSE horizontal and only short (only vertical).

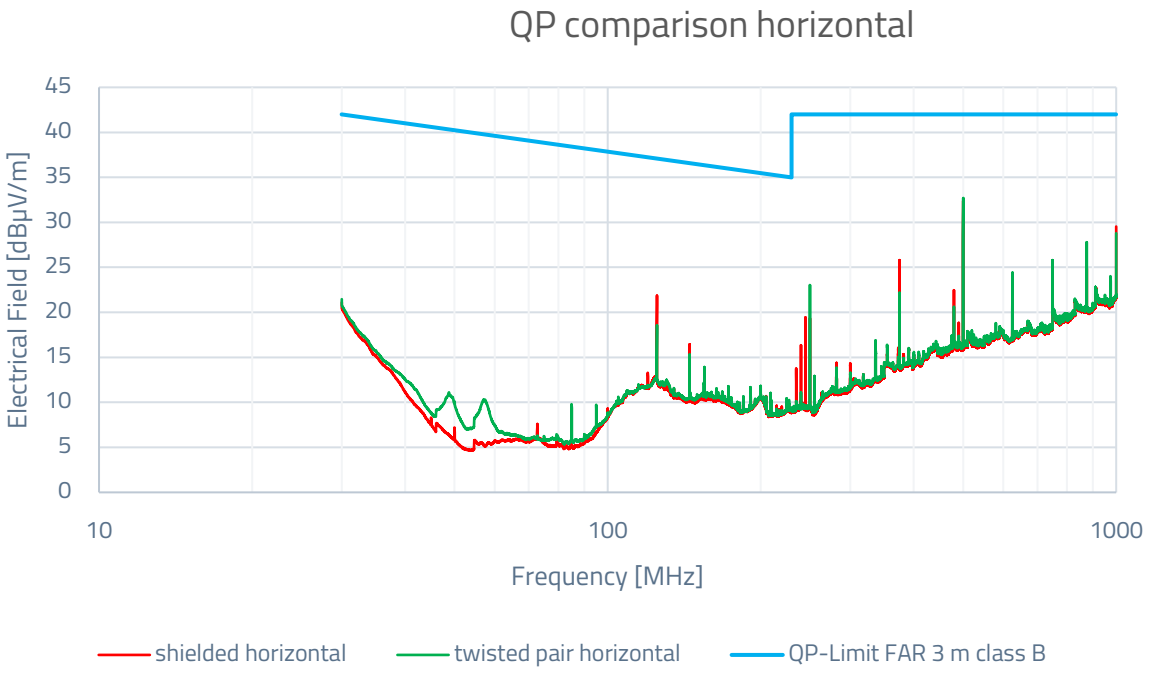


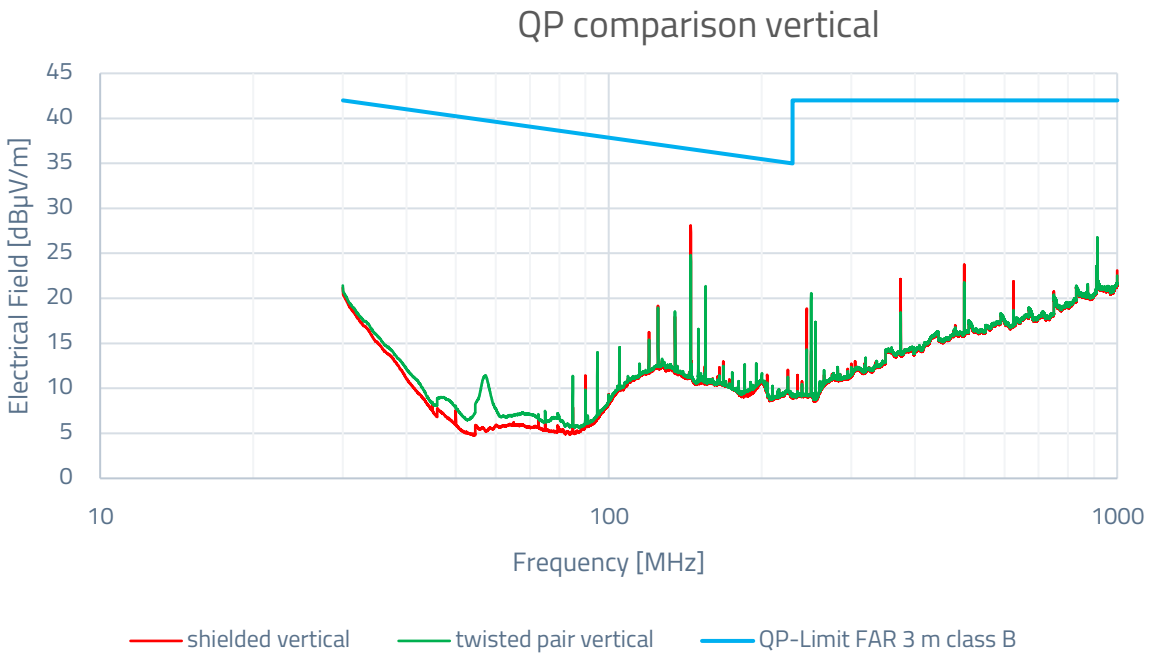
➢ PD and PSE tested together as a system.

RADIATED EMISSIONS

Comparison shielded and unshielded cable at SPoE interface

- 100 Mbit/s Ethernet: cat.5e SF/UTP.





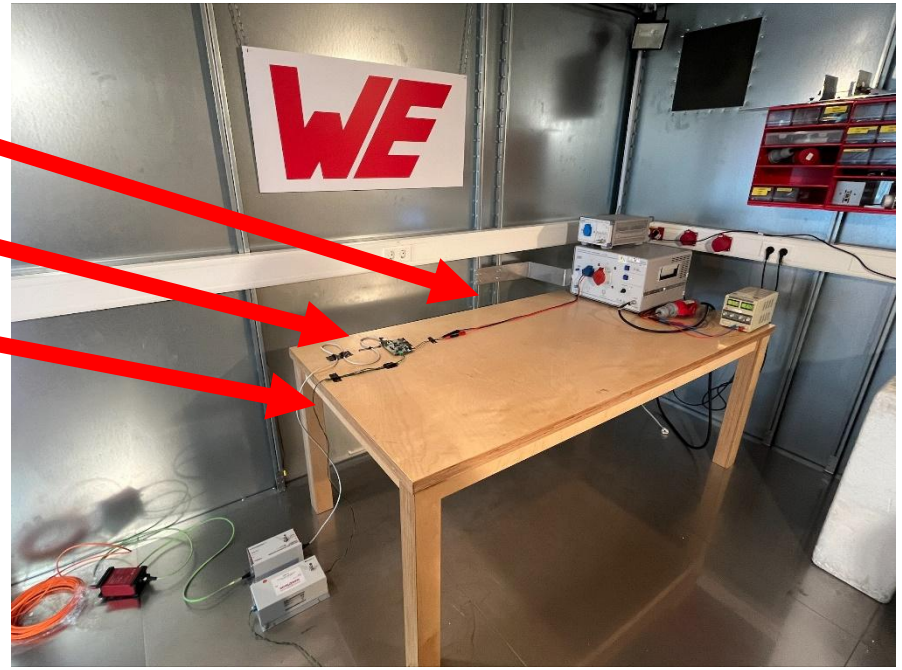
- Results are comparable - pass the radiated emissions test with shielded cable and with twisted pair cable.
- Pass Class B Limits.

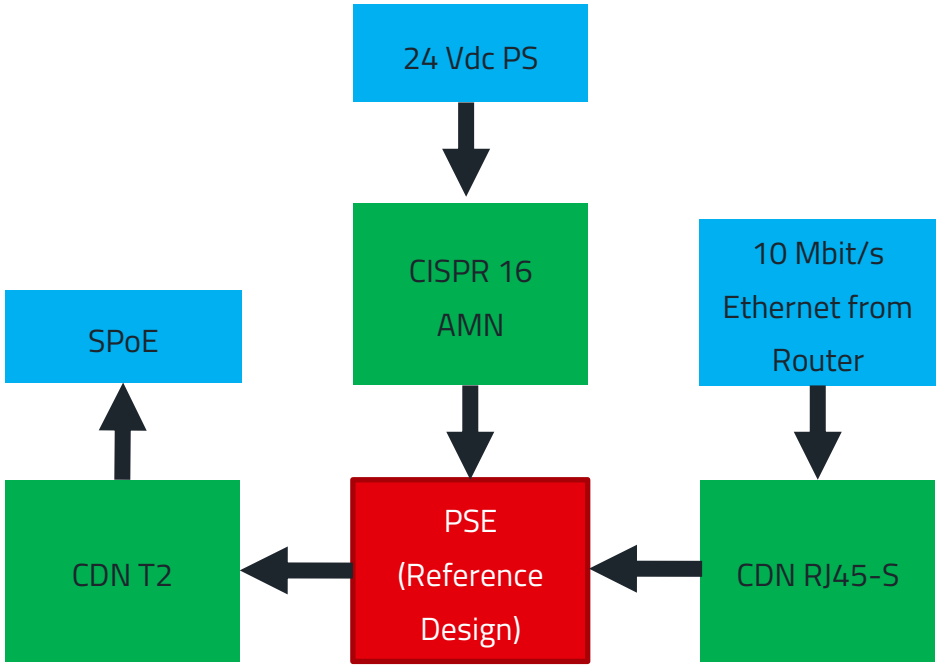
TEST SETUP CONDUCTED EMISSIONS CISPR 32

conducted emissions test setup according to the standard: PSE

- Test setup according to the standard: PSE and PD tested individually.
  - Distance DUT to ref GND (wall): 40 cm.
  - Distance DUT to LISN: 80 cm.
  - AAN (=CDNs) on the floor: 80 cm distance to DUT.

- PSE:
  - 24 Vin DC.
  - Ethernet Interface.
  - SPE Interface.

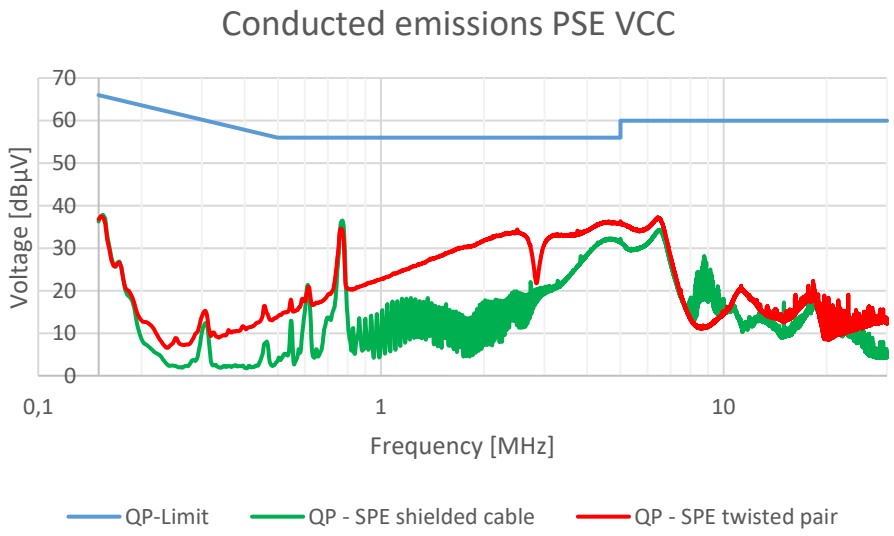


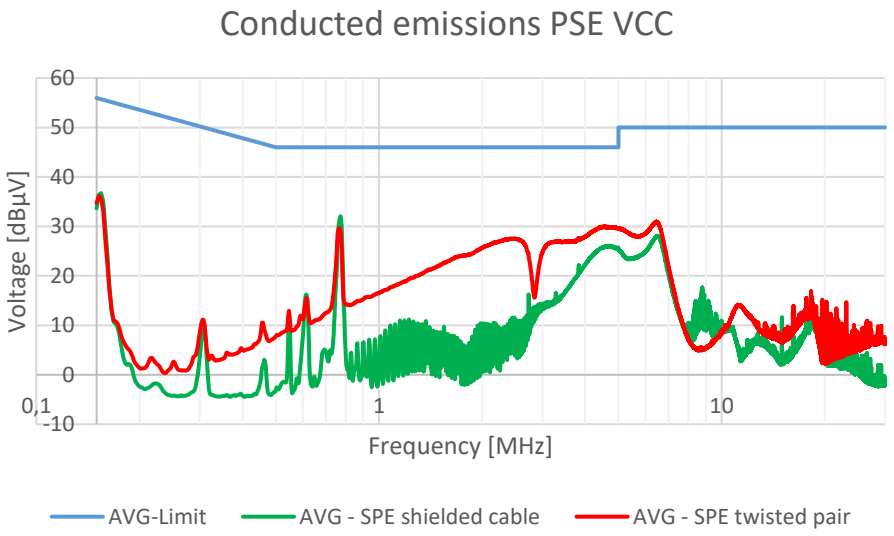


CONDUCTED EMISSIONS

PSE measured on **24 Vin** with CISPR 16 LISN – comparison shielded SPE cable and twisted pair SPE cable

- 100 Mbit/s Ethernet: cat.5e SF/UTP.
- Emissions of Neutral and VCC comparable – only show neutral.



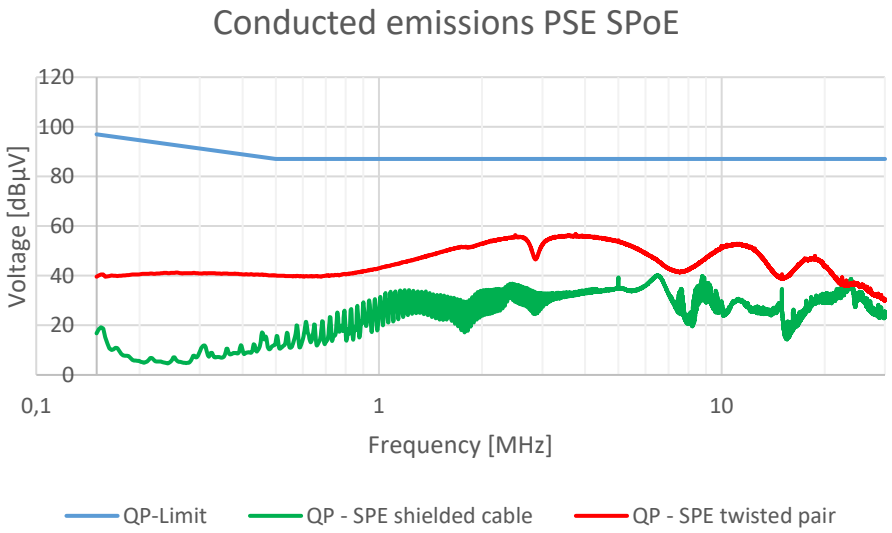


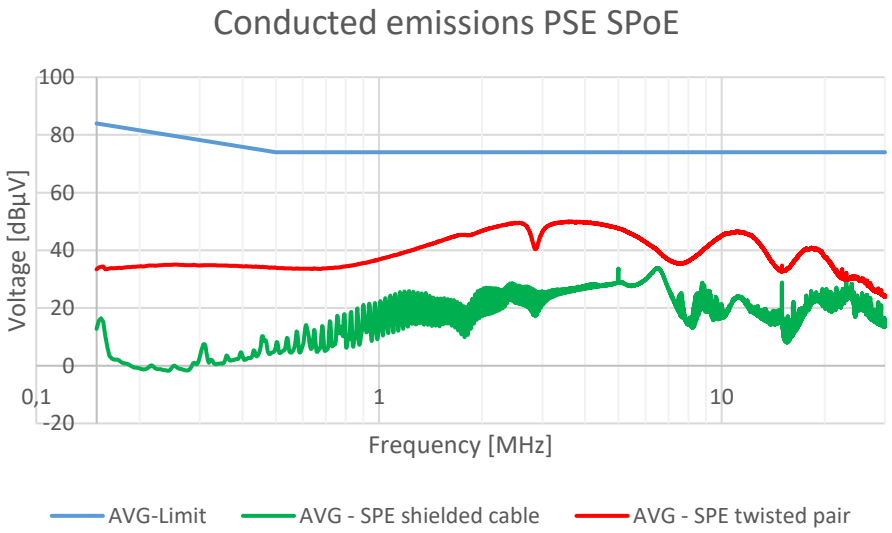
- Pass the test with shielded and unshielded cable on SPoE interface. Class B Limits.
- Reduced noise with shielded cable.

CONDUCTED EMISSIONS

PSE measured on **SPoE interface** – comparison shielded SPE cable and twisted pair SPE cable

- 100 Mbit/s Ethernet: cat.5e SF/UTP.



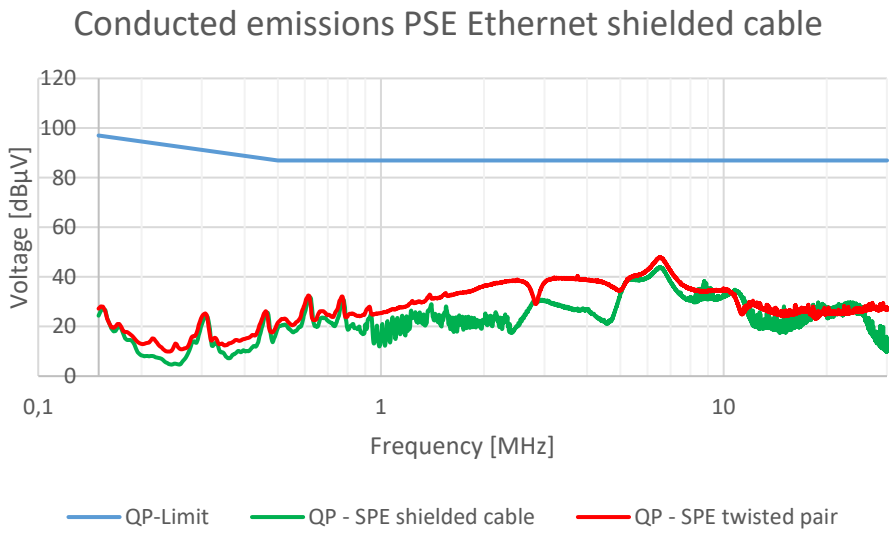


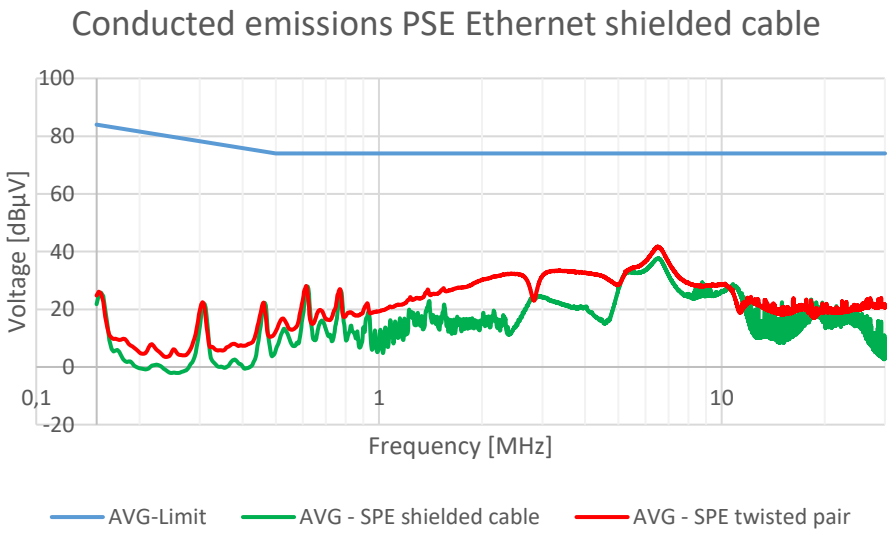
- Pass the test with shielded and unshielded cable on SPoE interface. Class B Limits.
- Reduced noise with shielded cable.

CONDUCTED EMISSIONS

PSE measured on **shielded 100 Mbit/s Ethernet** – comparison shielded SPE cable and twisted pair SPE cable

- 100 Mbit/s Ethernet: cat5e SF/UTP.





- Pass the test with shielded and unshielded cable on SPoE interface. Class B Limits.
- Effect of SPoE cable not relevant for the emission on the cat5e SF/UTP cable shield.
- Common Mode noise coupling from the twisted pair dominant on the VCC-Line.

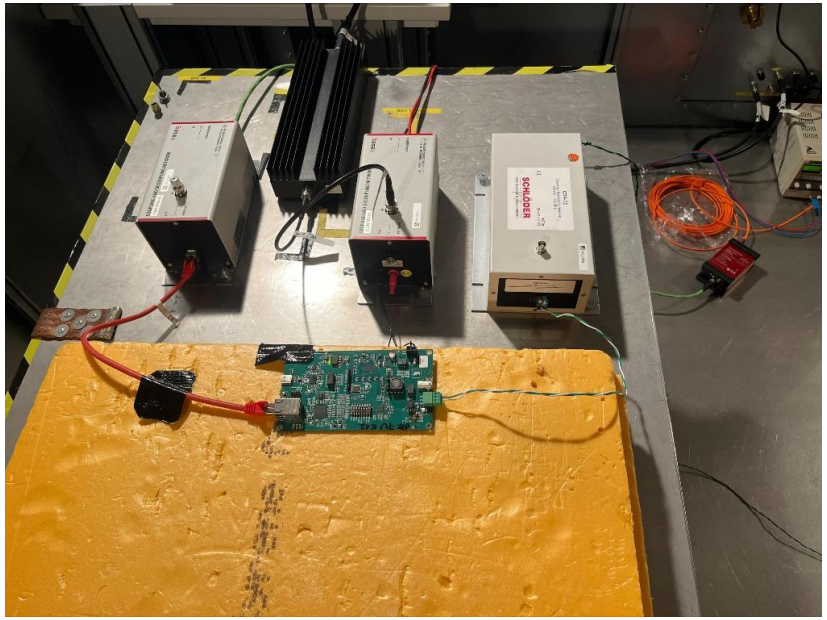
CONDUCTED AND RADIATED IMMUNITY

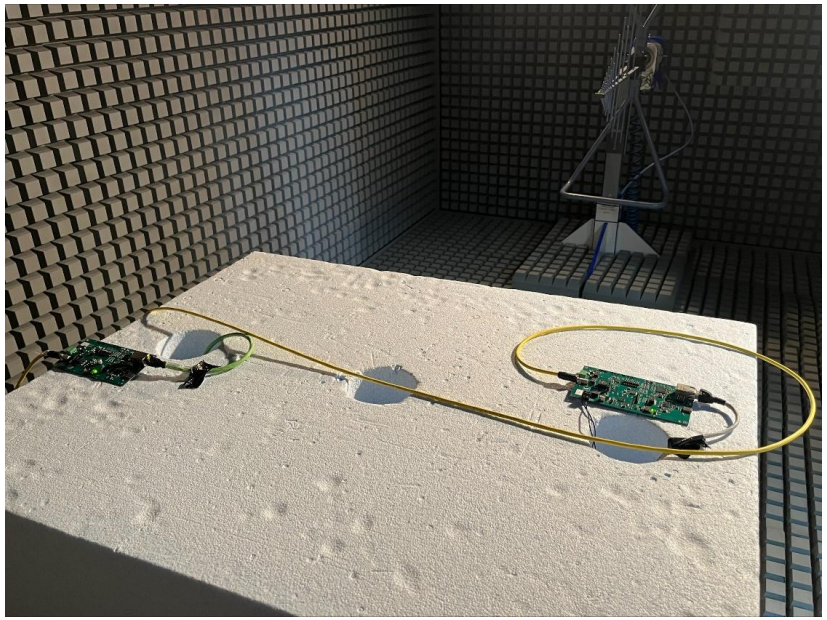
Continuous disturbances

- Conducted immunity IEC 61000-4-6:
  - Pass the test with a level of 20 V.
    - SPE: twisted pair unshielded.
    - SPE: shielded cable.
    - 24 Vdc Input.
    - Shielded Ethernet cable cat.5e SF/UTP.

- Radiated immunity IEC 61000-4-3:
  - Pass with the following test levels:
    - 80 MHz to 1 GHz: 20 V/m.
    - 1 GHz to 6 GHz: 10 V/m.
    - SPE: twisted pair unshielded.
    - SPE: shielded cable.

- Performance Criteria A: no change in payload and error rate 0%.





BURST TEST UNSHIELDED SPE CABLE – DUT EARTHED

SPE cable twisted pair unshielded

- Overvoltage protection at work during burst test on unshielded twisted pair SPE interface.

TRANSIENT IMMUNITY

Insulated setup: PSE insulated power supply, and PD electronic insulated from GND.

- Very good performance with shielded SPoE cable.
- Unshielded twisted pair cable: The DUT passed in criteria B up to Burst test levels of1 kV.

Etherner shielded cat5e SF/UTP cable shield conencted with 2 x 10 nF + Varistor to GND		transient disturbance (DUT floating)														
		61000-4-4 (CCC tested)						61000-4-2			61000-4-2			61000-4-5		
		5 kHz and 100 kHz tested						test level [kV] HCP			test level [kV] Chassis CD			test level [kV]		
DUT	Interface	500 V	1 kV	2 kV	3 kV	4 kV	5 kV	crit. A	crit. B	RESET	crit. A	crit. B	self recover	0,5	1	
PSE (V1.3): SPE unshielded	DC in							+/- 4 kV	+/- 6 kV	+/- 8 kV						
	SPE unshielded							+/- 4 kV	+/- 6 kV	+/- 8 kV	+/- 2 kV	+/- 6 kV	+/- 8 kV			
	Ethernet shielded							+/- 4 kV	+/- 6 kV	+/- 8 kV	+/- 2 kV	+/- 6 kV	+/- 8 kV			
PSE (V1.3): SPE shielded: 2 x 10 nF + Varistor	DC in							+/- 4 kV	+/- 6 kV	+/- 8 kV						
	SPE shielded							+/- 4 kV	+/- 6 kV	+/- 8 kV	+/- 4 kV	+/- 6 kV	+/- 8 kV			
	Ethernet shielded							+/- 4 kV	+/- 6 kV	+/- 8 kV	+/- 4 kV	+/- 6 kV	+/- 8 kV			
PD (V1.2): SPE unshielded	SPE unshielded							+/- 4 kV	+/- 6 kV	+/- 8 kV	+/- 2 kV	+/-4 kV	+/- 8 kV			
	Ethernet shielded							+/- 4 kV	+/- 6 kV	+/- 8 kV	+/- 2 kV	+/-4 kV	+/- 8 kV			
PD (V1.2): SPE shielded: 2 x 10 nF + Varistor	SPE shielded							+/- 4 kV	+/- 6 kV	+/- 8 kV	+/- 4 kV	+/- 6 kV	+/- 8 kV			
	Ethernet shielded							+/- 4 kV	+/- 6 kV	+/- 8 kV	+/- 4 kV	+/- 6 kV	+/- 8 kV			

NOTE: ESD discharge at shield connector also when using unshielded cable. The application needs to be designed to protect the terminals from being touched in operation.

TI OPTION

- Comparable EMC test results.
- Tested as SPE without SPoE in October 2024.

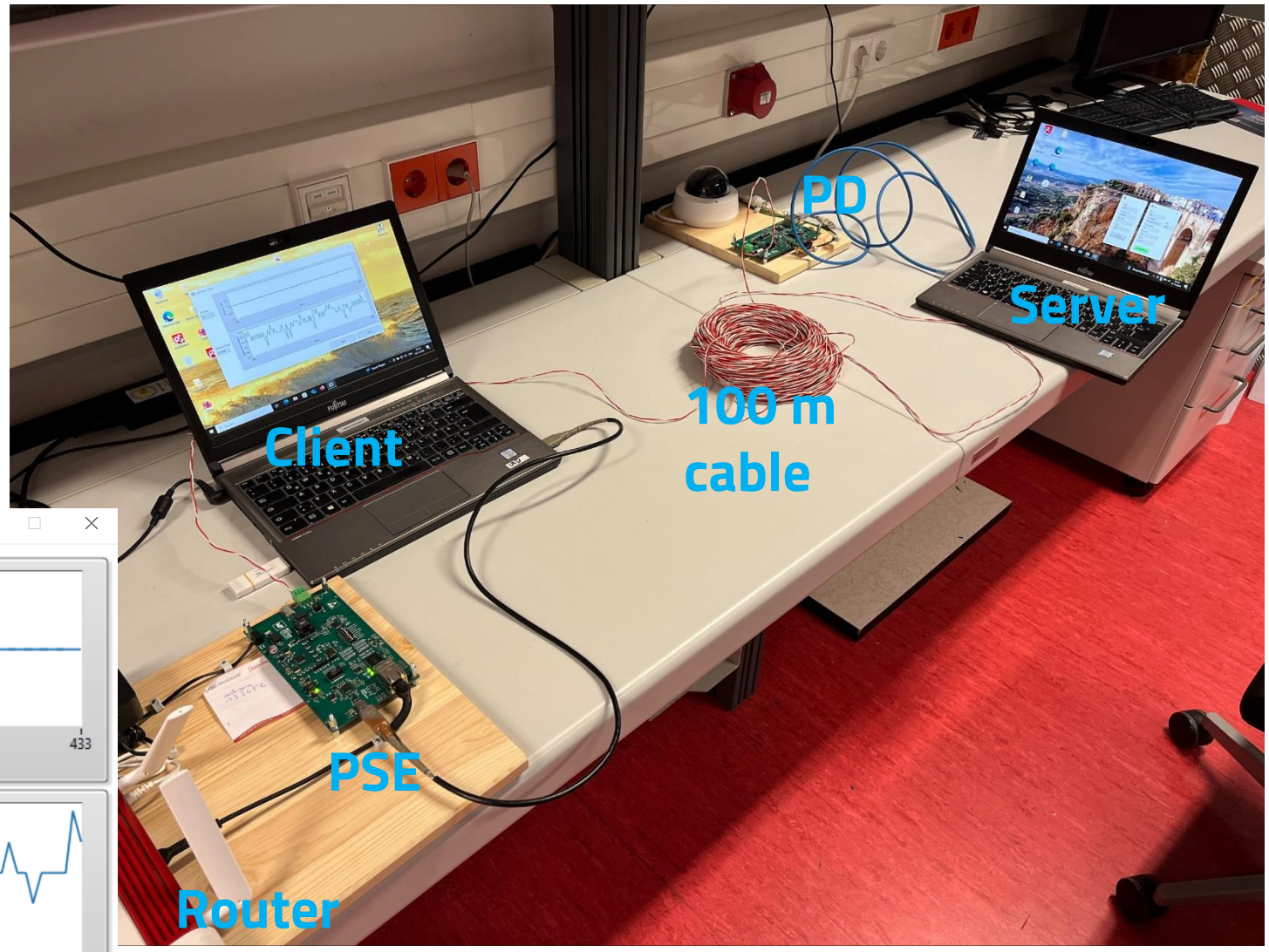
TIDA-010261

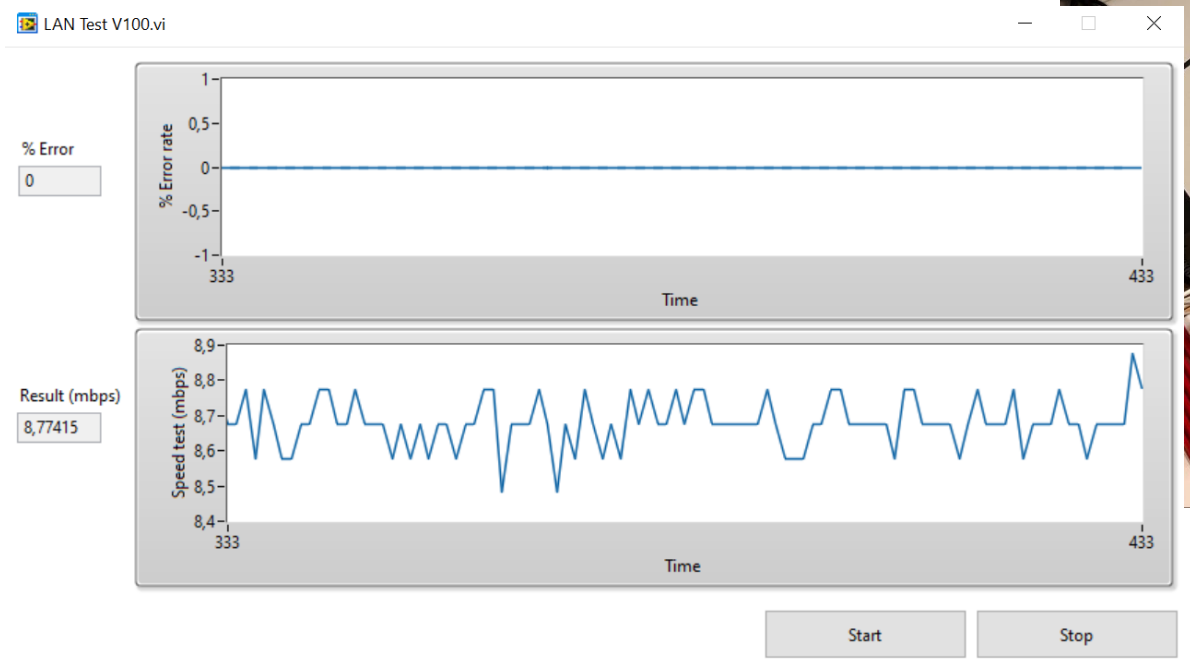
10BASE-T1L single-pair Ethernet sensor with power over data lines reference design

CABLE LENGTH TESTING

Unshielded twisted pair

- 100 m unshielded twisted pair cable 0,6 mm.
- Speed test with the demonstrator kit.
- Drop of DC-Voltage in 100 m cable: 1,5 V.





Thank you for participation!

Q&A