SUPPORT NOTE

SN029 | Introduction to Magnetics-on-Silicon Technology

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1. INTRODUCTION

In the electronics industry, there is a significant trend towards miniaturization of electronic devices. At the same time, system functionality should continue to be guaranteed or improved. Even though the advancing semiconductor technology improvements already allow for very small nodes and thus a very high integration level passive components still need to follow. As of today, the main bottle neck lies with magnetic components. Therefore, the overall solution volume of integrated systems is primarily decided by magnetics. To tackle this challenge, Würth Elektronik introduced its magnetics-on-silicon technology. The technology is based on the same thin-film fabrication process used for CMOS. The fabrication is done by a lithography process combining plasma deposition and electroplating processes. With this production process, any magnetic structure, such as inductors, coupled inductors, or transformers, is possible. Further, the production process offers high flexibility in terms of shape and chip size.

Figure 1 shows an example of a micro inductor as well as a micro transformer with an interleaved winding structure.

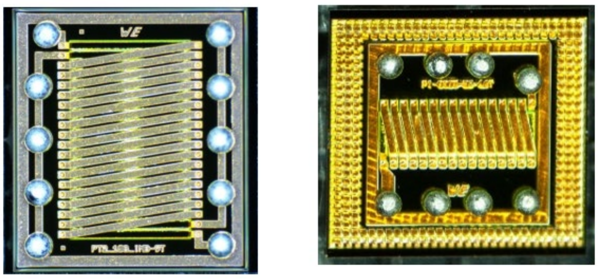


Figure 1: Example structures: left micro transformer, right micro inductor.

Fitting to the ongoing trend of miniaturization, the technology is meant for high frequency operation allowing for a small magnetic component size.

2. LAYER STACK-UP

The magnetics are built on undoped silicon used as substrate material. The top and the bottom layer consist of electroplated copper with a 25 µm copper thickness. The top and bottom copper layers are connected through vias throughout the structure. Between both copper layers, a 6 µm thick sputtered Cobalt-zirconium-tantalum (CZT) CZT magnetic core is embedded. To ensure the needed isolation between the layers, polyimide is used as insulation material. The overall profile height of the component is only 200 µm.

Figure 2 shows a sketch of the described layer stack-up.

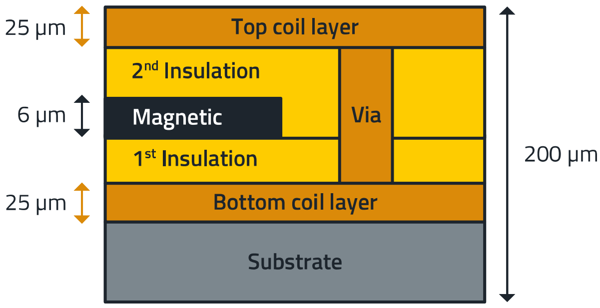


Figure 2: Layer stack-up.

By using a special CZT magnetic core material the BH, or hysteresis loop is optimized to make it compatible with high-frequency applications. With the narrow BH loop, the core AC losses can be kept low at high frequencies, enabling this technology to operate in power applications even at tens of megahertz. In addition, the amorphous CZT core offers a high saturation flux density needed for power applications. For signal applications such as isolating the signal path of a digital isolator with low current requirement the technology can also be used for the commonly high frequencies in hundreds of megahertz.

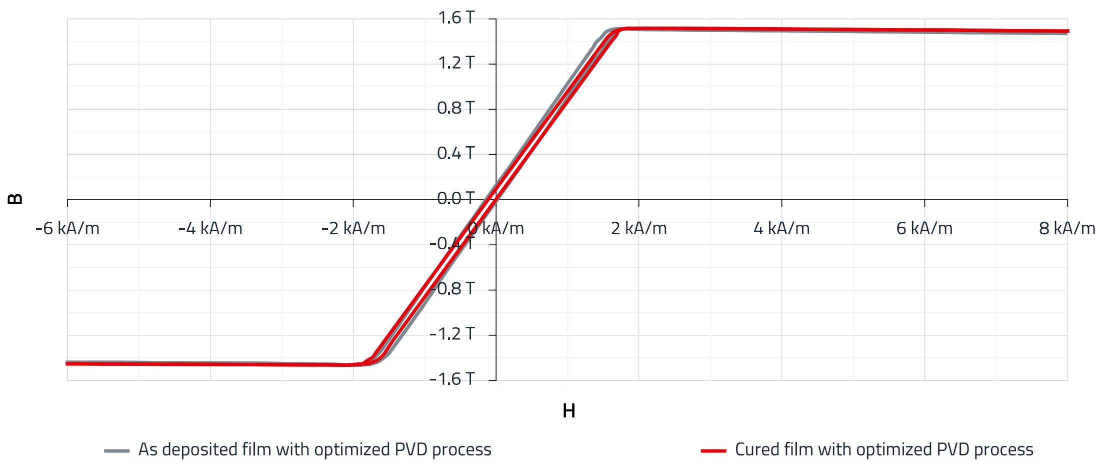


Figure 3: BH-loop of CZT magnetic core material.

To further minimize eddy current losses, the core is built-up as a laminated structure with thin oxide layers as a dielectric between the CZT layers. The core material has been characterized by a vibrating-sample magnetometer (VSM). The core material hits magnetic saturation around 1.3T – 1.4T. The given BH-loop characteristics show the hard saturation (sharp roll off) behavior of the magnetic core (Figure 3).

3. TECHNOLOGY SPECIFICATIONS

Due to the small chip size of components, the inductance range is mainly within the nanohenry range. There is a general trade-off between the most important parameters, such as inductance, resistance, saturation current and chip area. Würth Elektronik offers customization to achieve the best fitting magnetics design for the target application. The following list should give an idea of what is possible as of today. It does not show the real technology limitations, but it shows what has already been produced:

Micro transformer specifications:

- L: 5 - 500 nH
- Q-Factor > 12 at 10 - 50 MHz
- L/R_{DC} > 200 nH/Ω
- Isolation voltage up to 3 kV
- Couple factor up to 0.95

Micro inductor specifications:

- L: 5 - 500 nH
- L/A up to 300 nH/mm^2
- Q-Faktor 15…20 at 10 - 50 MHz
- L/ R_{DC} > 400 nH/Ω
- Saturation current 0.2 A ~ 2 A
- L tolerance: ±10%

4. INTEGRATION OPTIONS

The technology offers many flexible integration options. Chips can be ordered as wafer level chip scale package (WLCSP), including 250 µm diameter solder balls. This option offers the opportunity for package-in-package integration and is the easiest way to build-up prototypes since it allows for easy PCB assembly as shown in Figure 4.

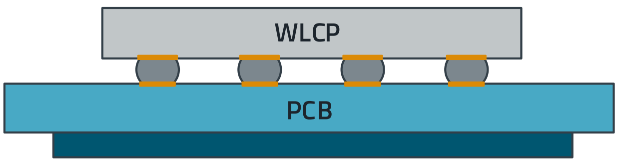


Figure 4: WLCSP mounted on PCB using ~250 µm solder balls for easy prototyping.

Chips can be ordered as bare dies with copper pads for wire bonding integration. If gold wire bonds are used, a nickel-gold lead finish can be added on top of the copper pads. Further, the technology allows for direct die embedding on the customer's side. Either the chips can be directly embedded into the customer's IC, or Würth Elektronik can source the chip IP. This requires that the production processes are compatible with each other. If required, the chip can also be embedded directly into a PCB instead of an IC. The flexible integration possibilities also allow for a chiplet approach. In summary, these are the available backend options and shipment possibilities:

Backend processes:

- Cu pads + RDL
- NiAg finish
- Solder balls
- Wire Bonding

- PCB Integration

Possible shipment conditions:
- Full thickness or Back-grinded wafer
- IC integration
- Tape & Reel

5. TARGET APPLICATIONS

Both power and signal applications can be targeted. Integrated DC/DC converters, isolated and non-isolated, are suitable use cases in terms of power applications. Empirical experience shows that the sweet spot in terms of highest Q-factor is at an operational frequency between 20 MHz - 30 MHz. As an example, Figure 5 shows a dual output power transformer design meant for an integrated isolated DC/DC converter within a monolithic GaN gate driver IC.

Figure 5: Dual output transformer for GaN gate drive.

Due to the very fast switching speed of GaNs, the parasitics of the overall design pose a substantial challenge. Therefore, the level of integration must be as high as possible.

Further, common isolated power applications make use of integrated pulse transformers. The current technological trend of AI also pushes the requirements for magnetic components to new limits in terms of inductance and current density. With ever increasing switching frequencies of 60 MHz and beyond the needed inductance value for PMICs used in this field of application becomes very small (L < 10 nH), enabling the use of silicon-based power inductors with low inductance and resistance but high saturation current reaching a current density of $J > 4\ A/mm^2$.

Aside from isolated power conversion for the internal power supply, the internal isolated signal transfer within digital isolators represents a great example of a signal application of this technology. Digital isolators like the WPME-CDIP 18024x15401x of Würth Electronic can transmit extremely high data rates, such as 100 Mbps. By building up an inductive isolation barrier instead of a capacitive one, it is possible to realize both the internal power conversion as well as the signal transfer at once.

Figure 6 shows an example of a center tapped 1:1 transformer for the simultaneous transfer of signal and power.

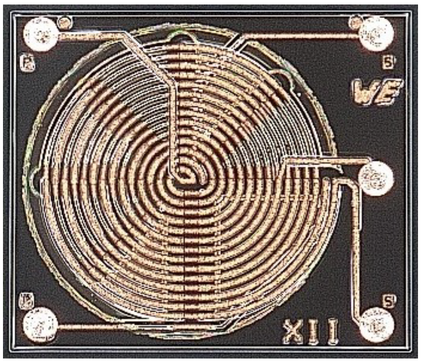


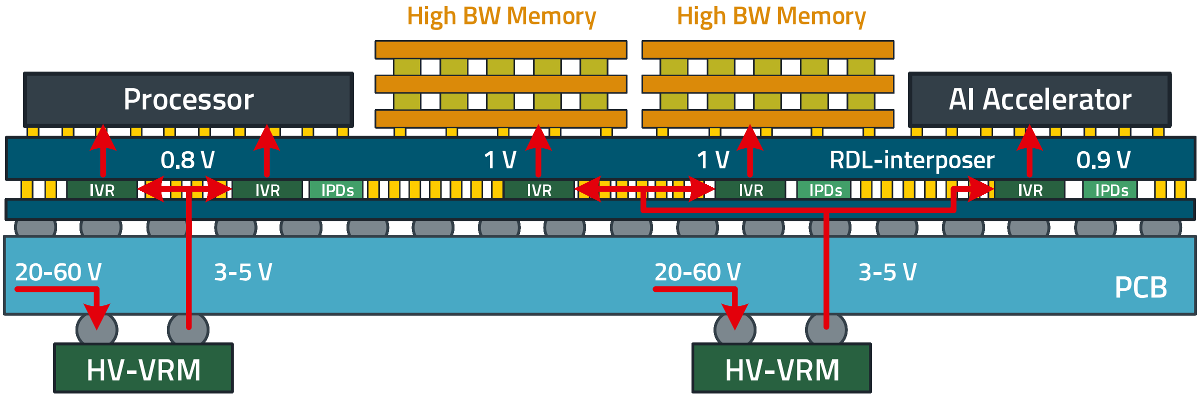
Figure 6: Center tapped transformer for signal and power transfer.

6. RELIABILITY

The technology is fully qualified according to the highest AEC-Q200 conditions with a temperature range of -55°C - +150°C. The qualification tests were performed internally and a full summary, including sample size, test descriptions and conditions, can be sent on request.

7. SUMMARY

Würth Elektronik´s innovative magnetics-on-silicon will support next generation IC development by increasing the level of integration of magnetics. Such next generation ICs like the fully monolithic IC, including the processor, high bandwidth memories and on-chip accelerator used for AI are shown in Figure 7. For high-speed communication, the requirements of power management in terms of dynamic load jumps are very challenging. Therefore, the power conversion needs to be as close as possible to the respective point of load to minimize the on-chip parasitics. Further, as every single load has its own power demand as well as core voltage, the power conversion needs to be optimized exactly for every single load. This can be realized by adding customized integrated passive devices (IPD) like a silicon-based magnetic offered by Würth Elektronik.



AI: Artificial Intelligence
BW: Bandwidth
IVR: Integrated Voltage Regulator
IPDs: Integrated Passive Devices
PCB: Printed Circuit Board
HV-VRM: High Voltage - Voltage Regulator Module
RDL-interposer: Redistribution Layer Interposer

Figure 7: Example of a monolithic processor IC (source: IEE Symposium 2024).

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