SINGLE PAIR ETHERNET FILTER DESIGN

Christian Koch
Field Application Engineer

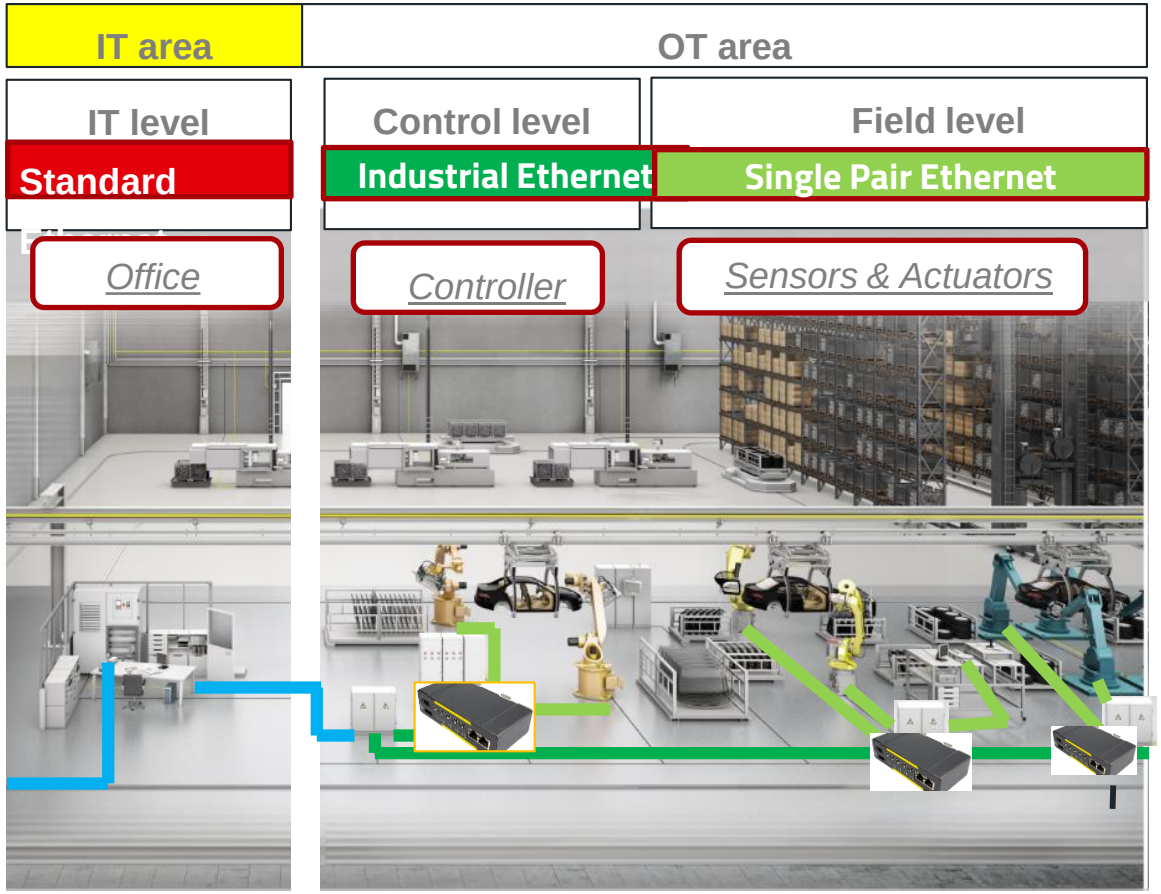
WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

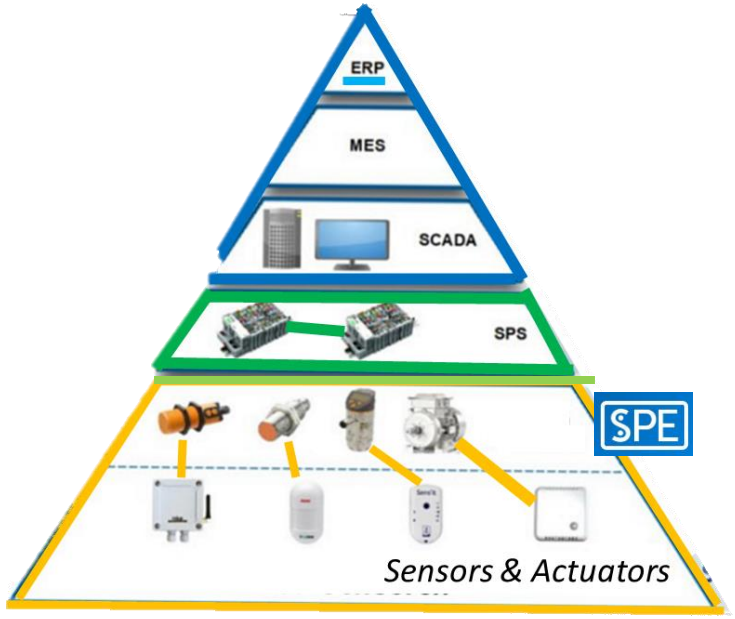
Agenda

- **Introduction Single Pair Ethernet**
- Signal filtering
- SPE filter solutions
  - 10BASE-T1
  - 100BASE-T1
  - 1000BASE-T1

- **Power over Data Line (PoDL)**
  - Function of components
  - Improvements of PoDL design
  - Solutions for high currents

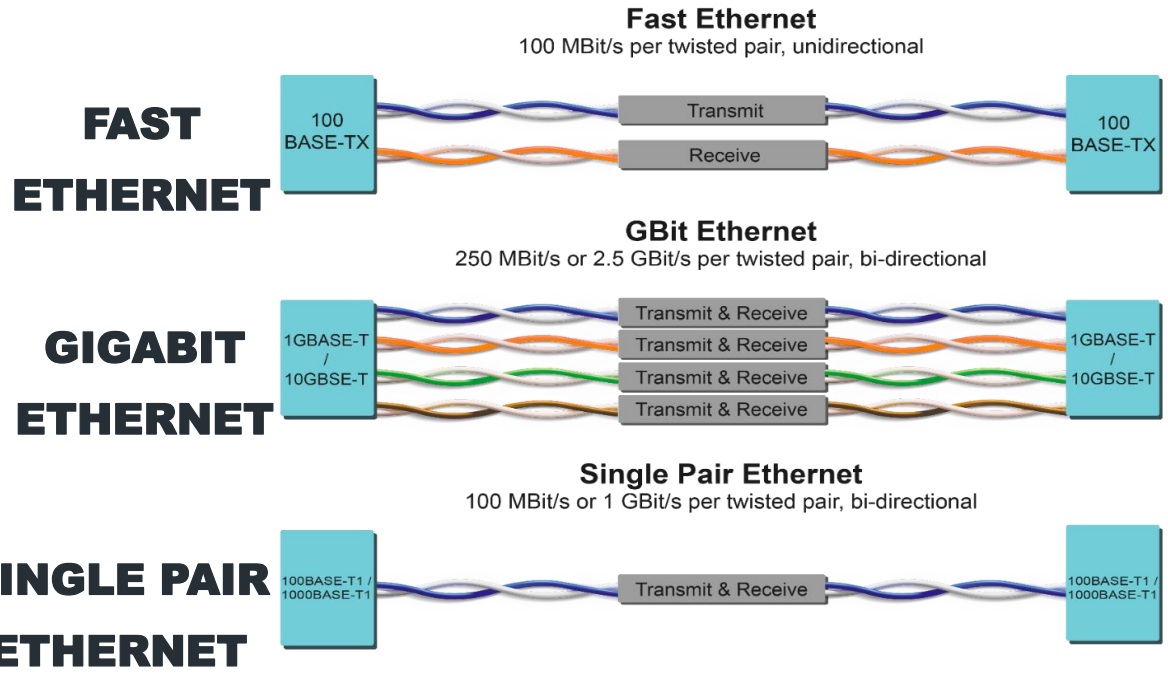
SPE factory automation





Simple switch converts from Industrial Ethernet to SPE

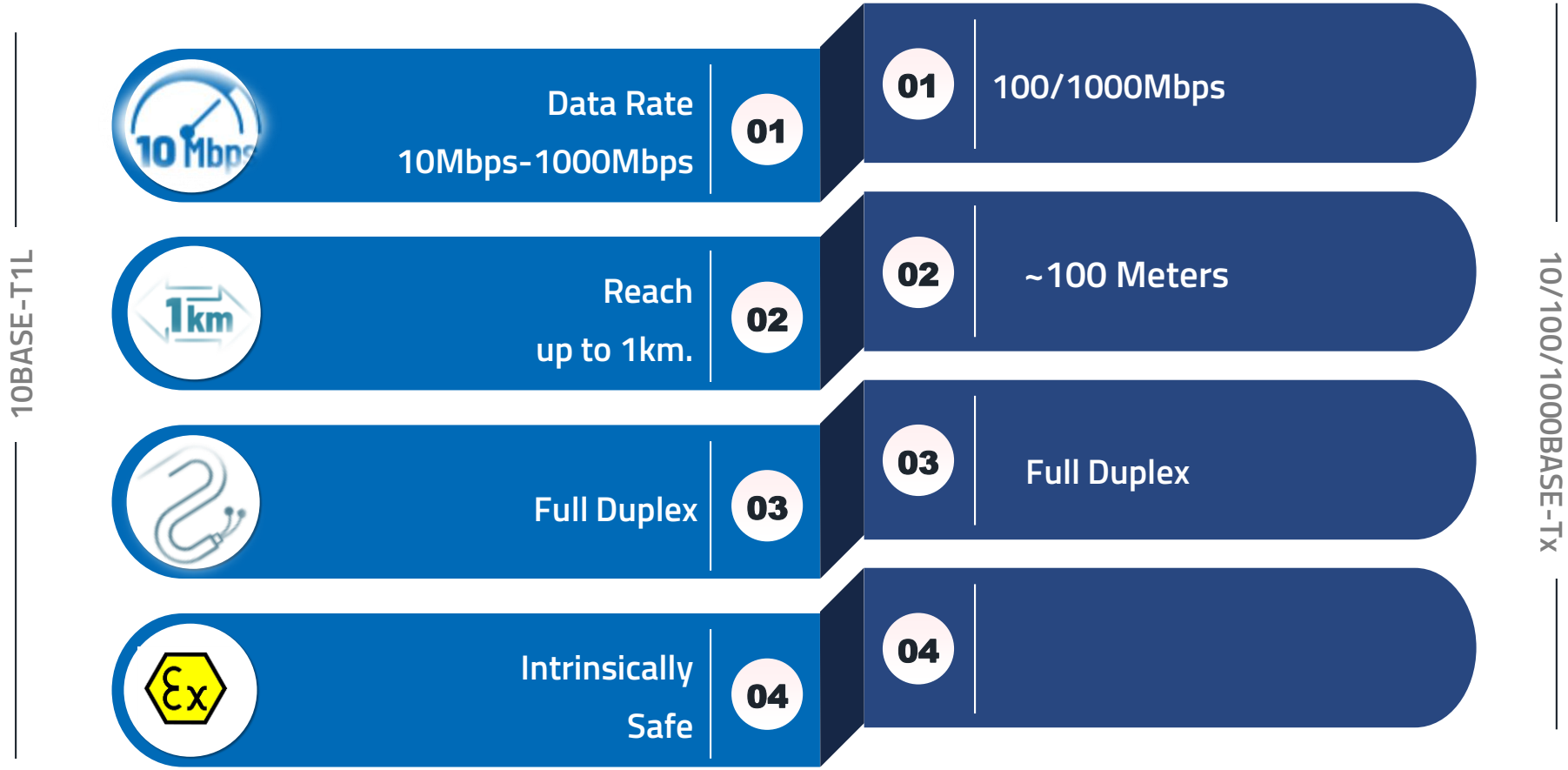
SPE Cables



STANDARD GBit Ethernet 4 Pair Cabling

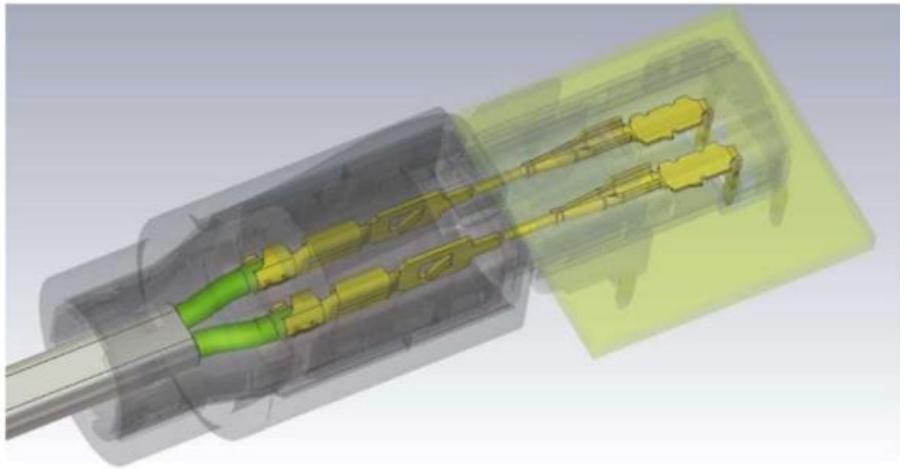
SPE Single Twisted Pair Cabling

SPE Standards 2022



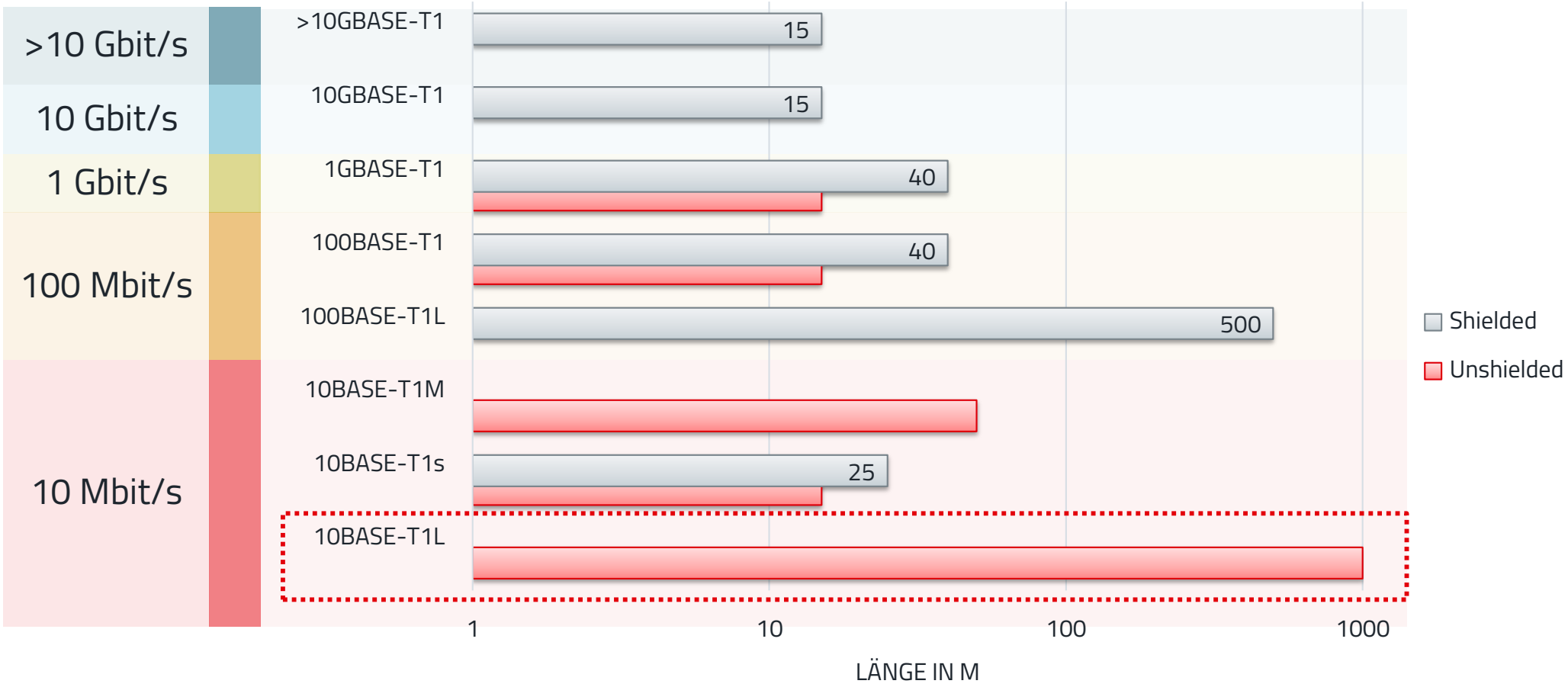
SPE Connectors

IEC 63171-6 (e.g. Harting)



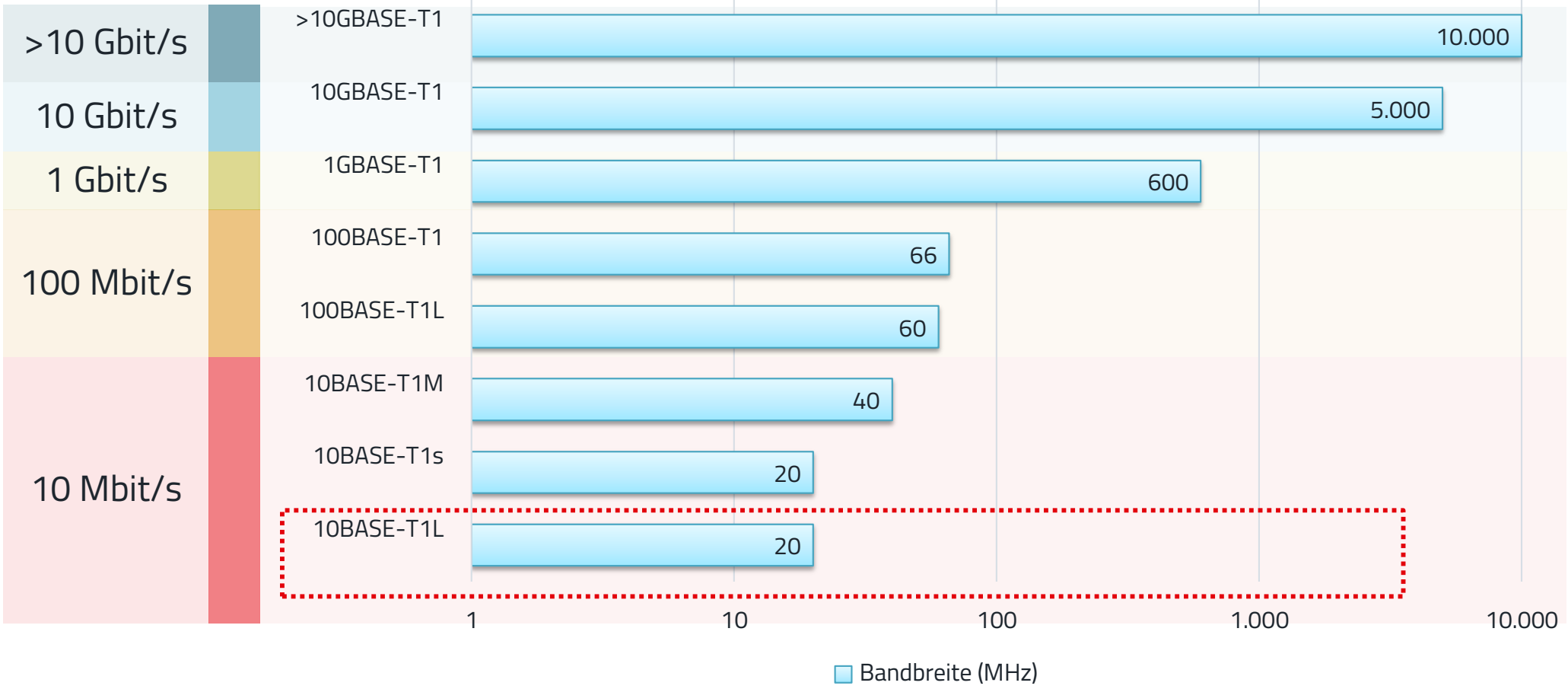
2. SPE - Technische Daten

2.1 Verkabelungslänge



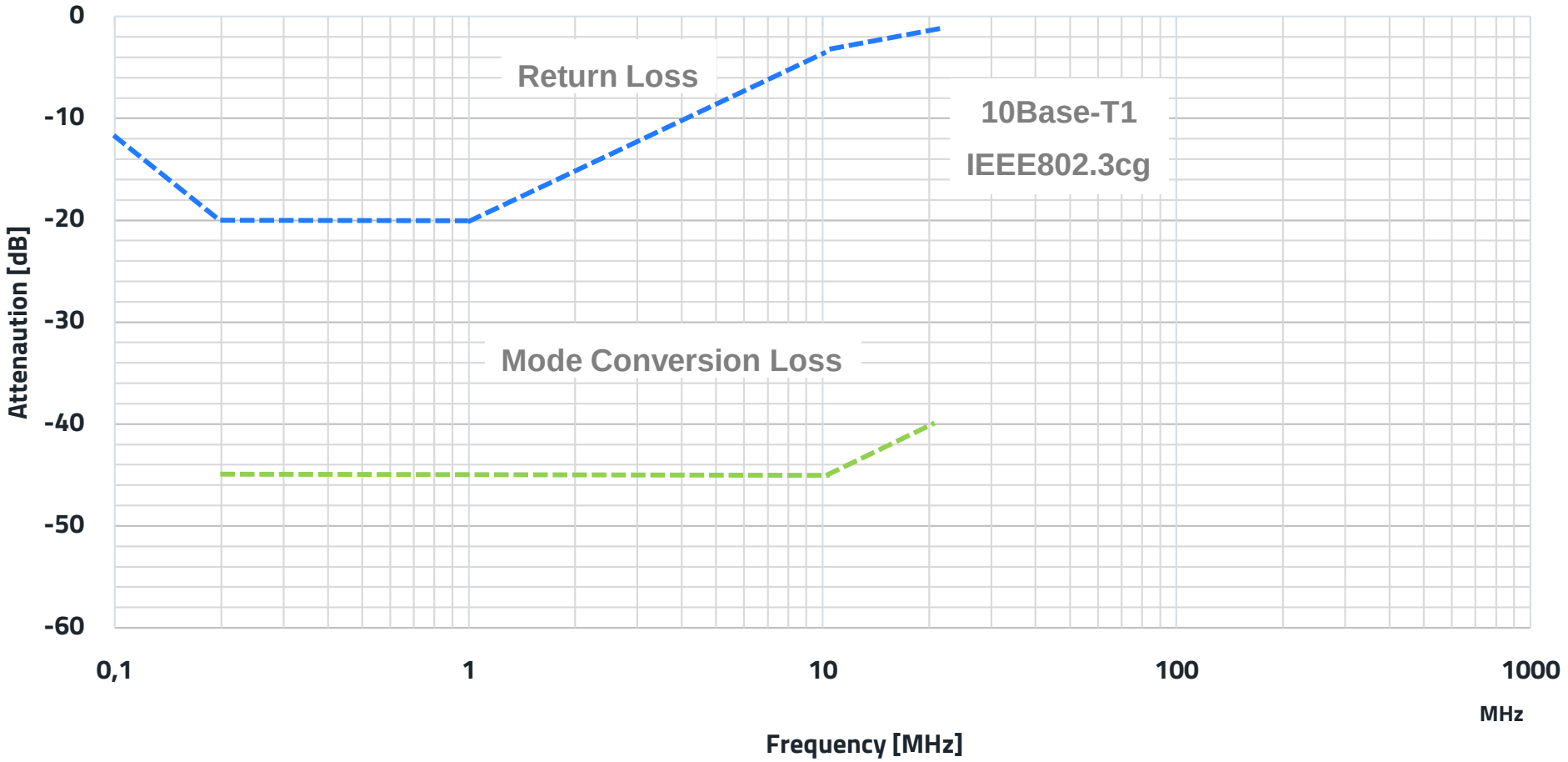
2. SPE - Technische Daten

2.2 Bandbreite

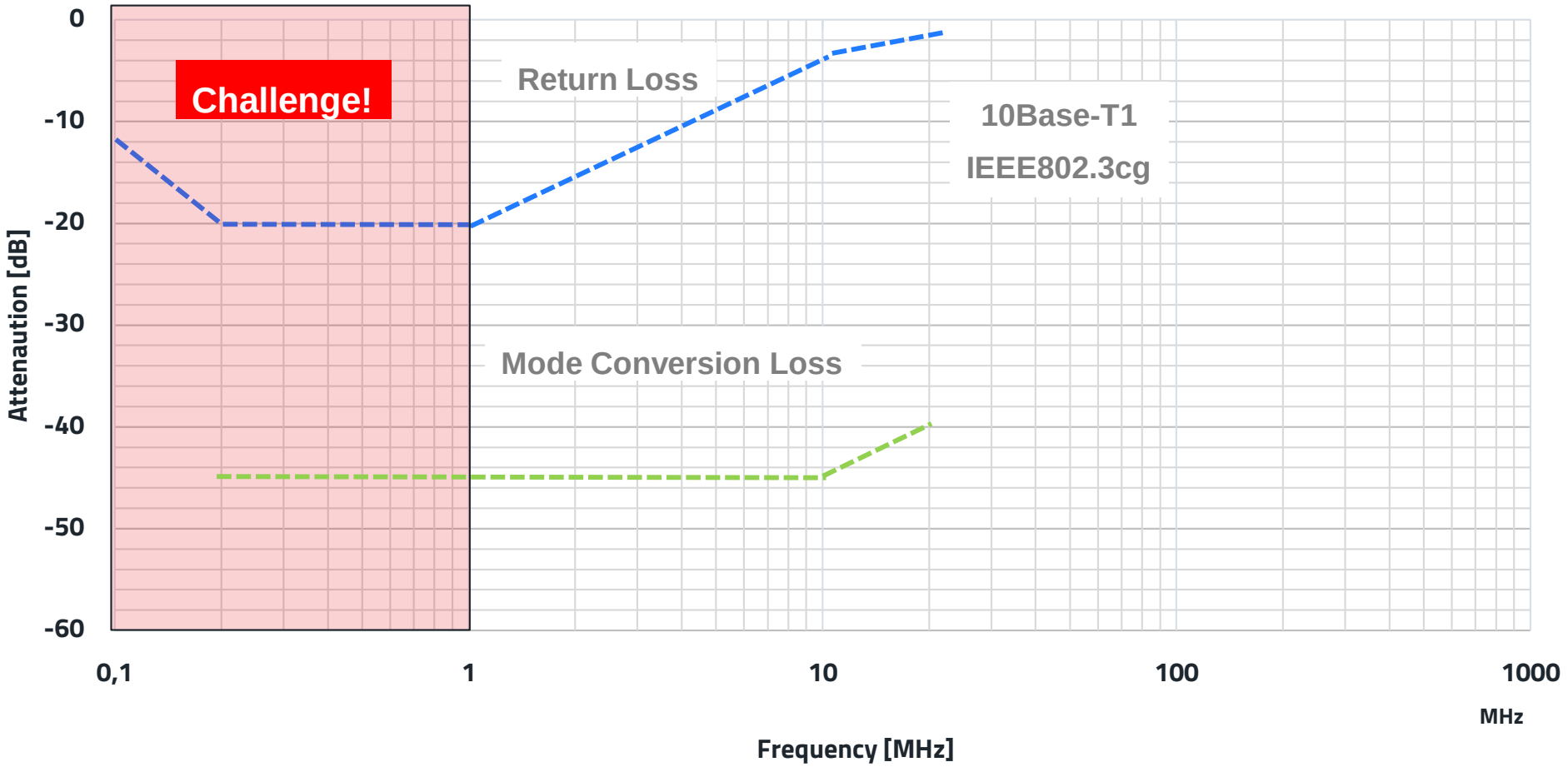


10BASE-T1L

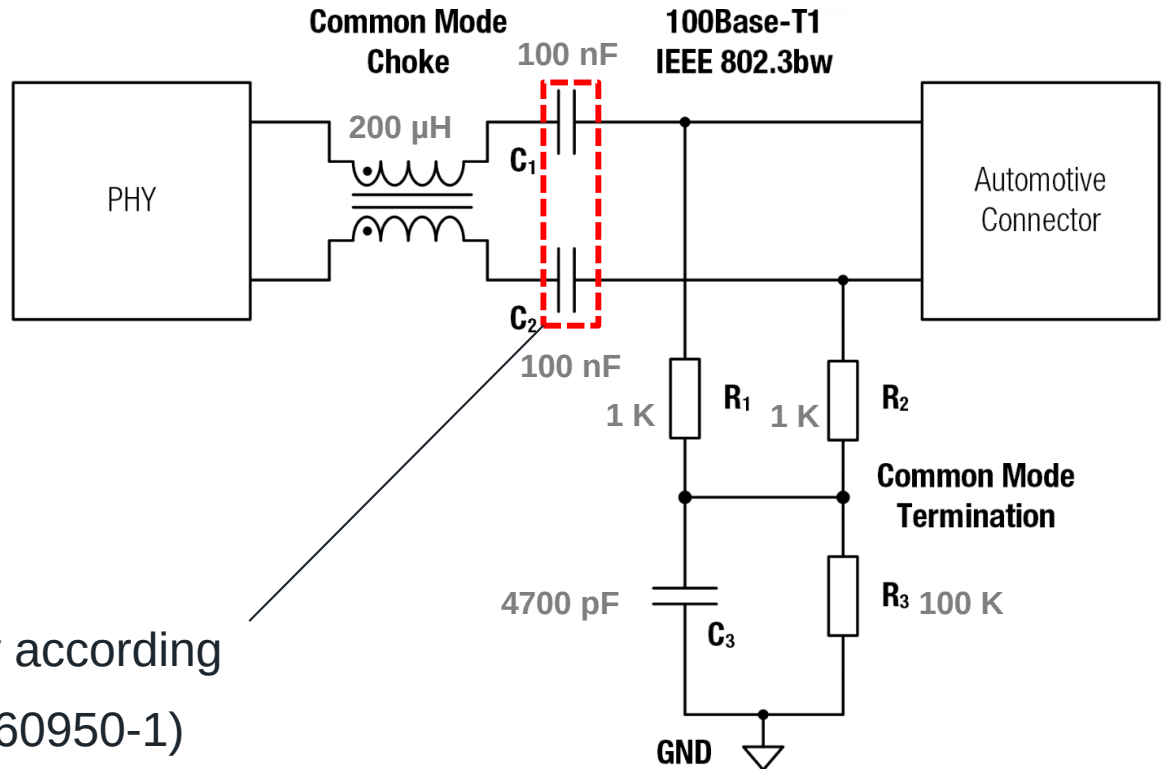
10BASE-T1


0
-10
-20
-30
-40
-50
-60
Attenaution [dB]
Return Loss
10Base-T1
IEEE802.3cg
Mode Conversion Loss
0,1
1
10
100
1000
MHz
Frequency [MHz]

10BASE-T1


Challenge!
Return Loss
10Base-T1
IEEE802.3cg
Mode Conversion Loss
0
-10
-20
-30
-40
-50
-60
Attenaution [dB]
0,1
1
10
100
1000
MHz
Frequency [MHz]

100BASE-T1 Automotive Ethernet



50 VDC isolation

-> Not sufficient for safety according

to IEC 62368-1 (old: IEC 60950-1)

10BASE-T1L

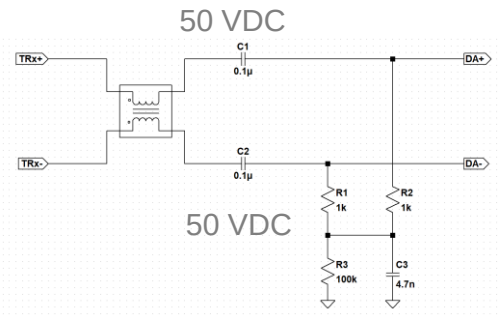
Comparison of different solutions

50 V Capacitors

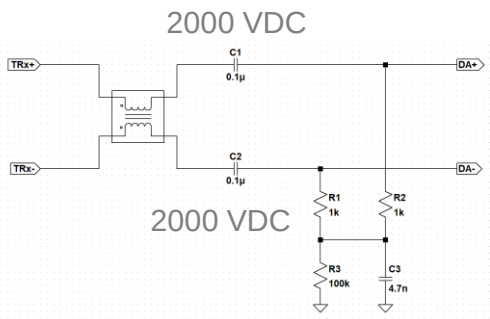
2000 V Capacitors

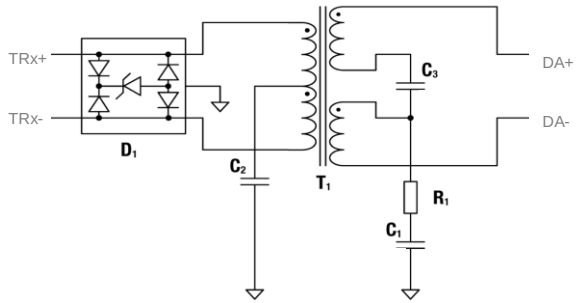
Signal Transformer

50 VDC



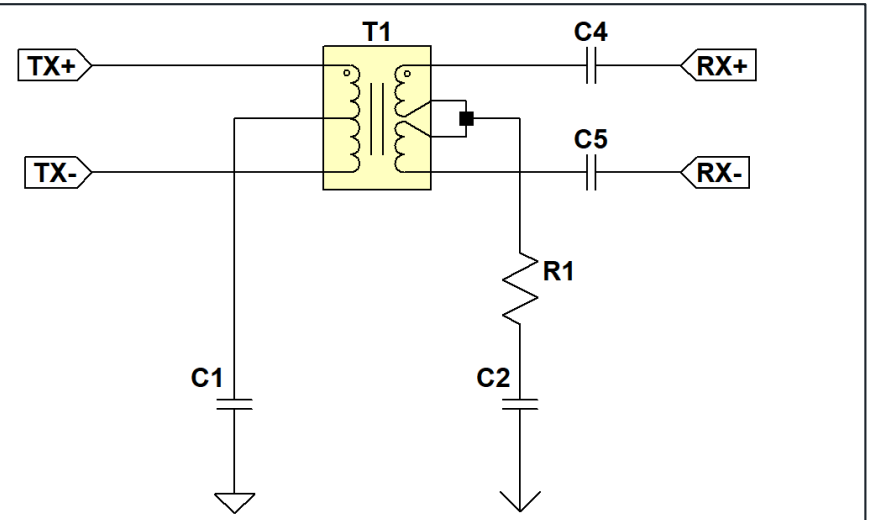
2000 VDC





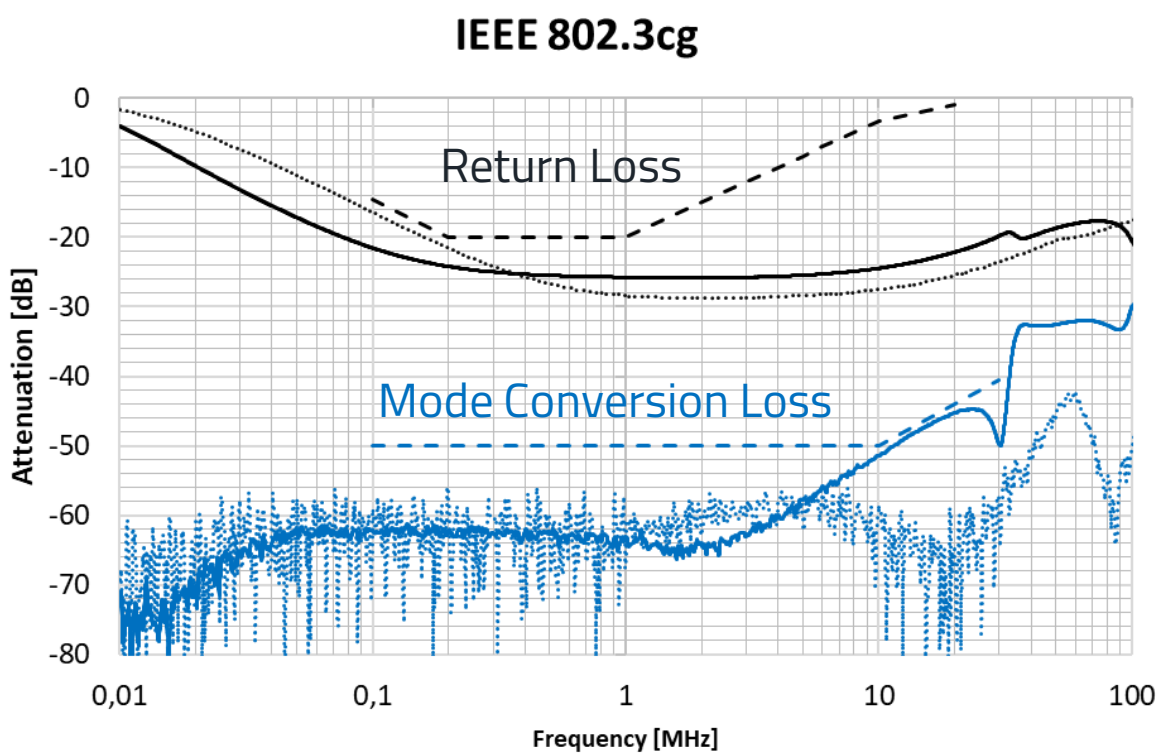
10BASE-T1L

Circuit



Name	Value	Isolation	Size	Article number
C1	100 nF	50 V	0402	885012205086
C2	1 nF	2 kV	1206	885342208024
C4, C5	470 nF	100 V	0603	885012207130
T1	600 µH	1500 V	5.35 x 6.55 mm	74930200
T1	350 µH	1500 V	1812	74930000
R1	100 Ω		0603	

Limits



Droop measurement

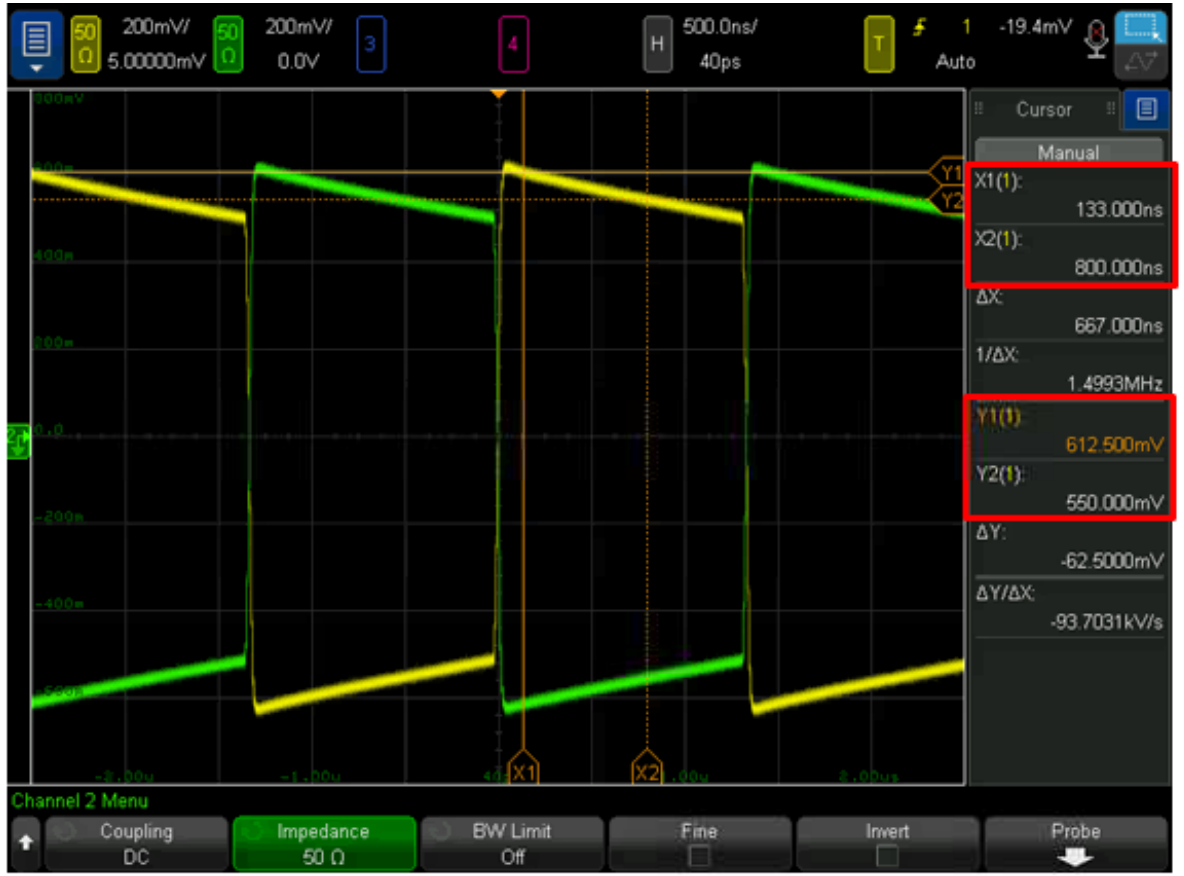
146.5.4.2 Transmitter output droop

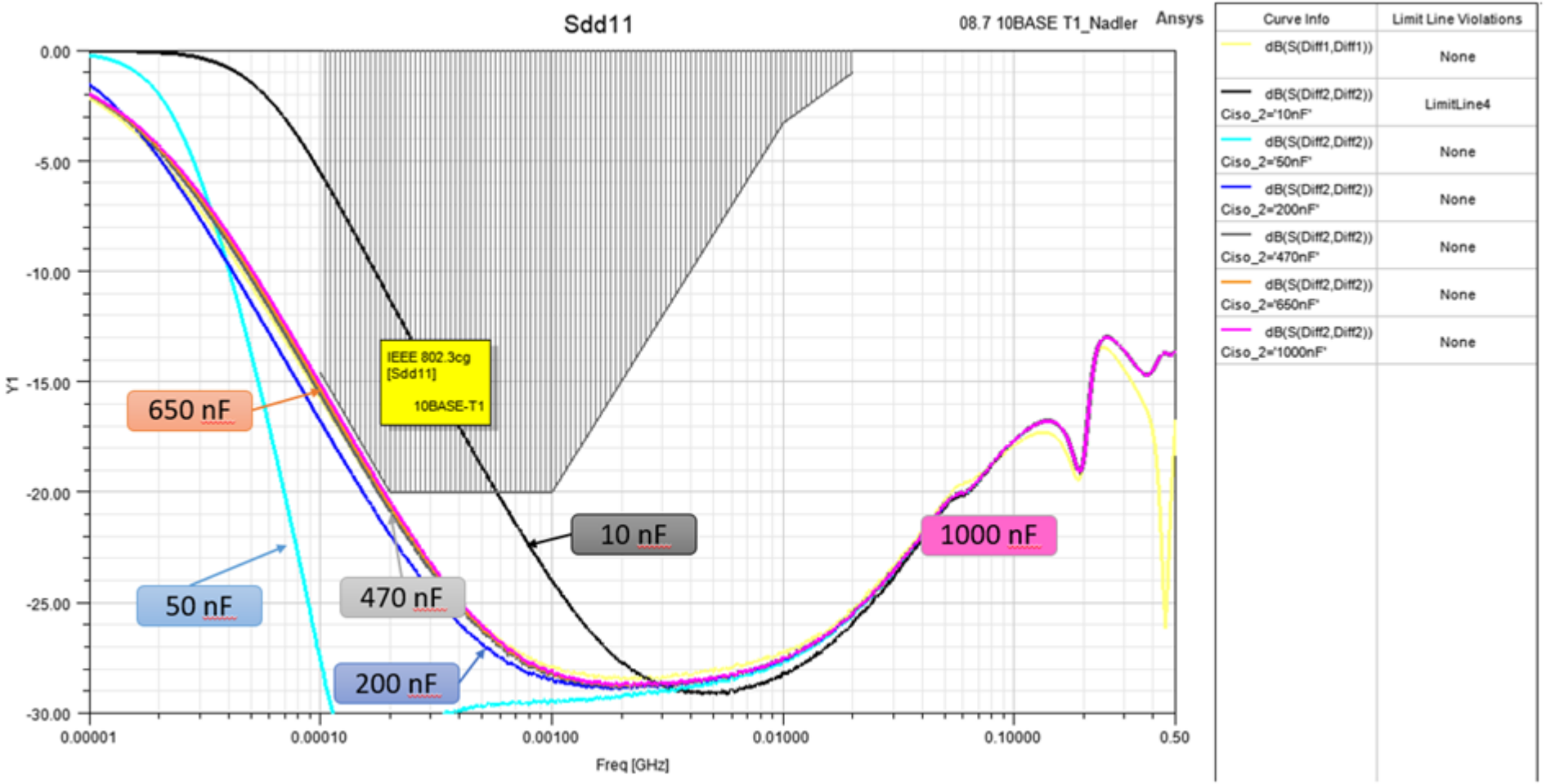
With the transmitter in test mode 2 and using the transmitter test fixture shown in Figure 146–20, the magnitude of both the positive and negative droop shall be less than 10% measured with respect to an initial value at 133.3 ns after the zero crossing and a final value at 800 ns after the zero crossing.

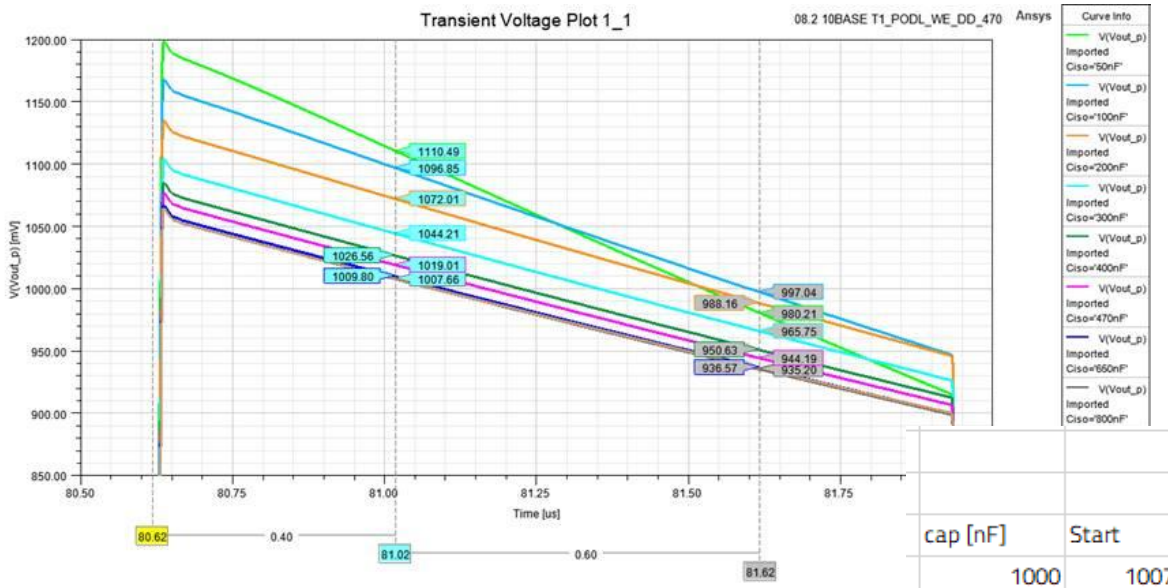
Source: IEEE802.3cg

$$U_{\Delta\%} = \frac{100\ \%}{V_{133ns}} * (U_{133ns} - U_{800ns})$$

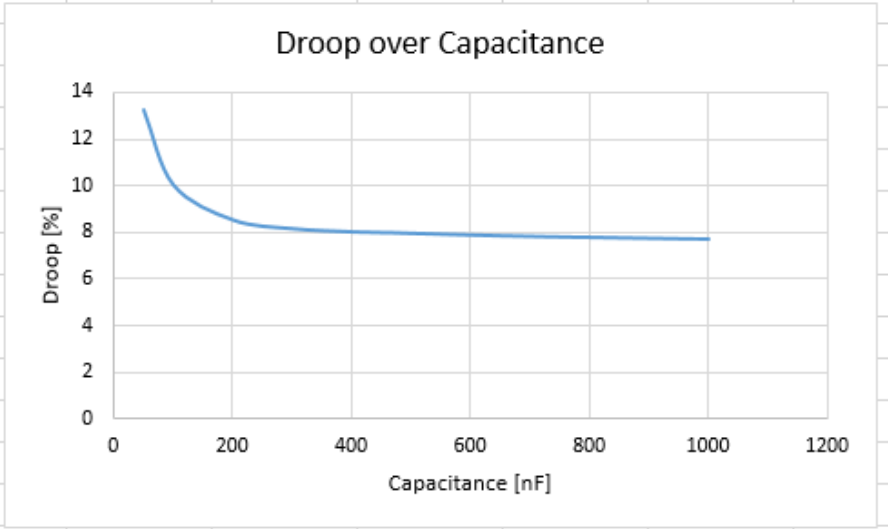
$$= \frac{100\ \%}{612{,}5\ mV} * (612{,}5\ mV - 550\ mV) = 10{,}2\ \%$$




Sdd11
08.7 10BASE T1_Nadler
Ansys
0.00
-5.00
-10.00
-15.00
-20.00
-25.00
-30.00
Y1
0.00001
0.00010
0.00100
0.01000
0.10000
0.50
Freq [GHz]
IEEE 802.3cg
[Sdd11]
10BASE-T1
650 nF
50 nF
470 nF
200 nF
10 nF
1000 nF
Curve Info
Limit Line Violations
dB(S(Diff1,Diff1))
None
dB(S(Diff2,Diff2))
Ciso_2='10nF'
LimitLine4
dB(S(Diff2,Diff2))
Ciso_2='50nF'
None
dB(S(Diff2,Diff2))
Ciso_2='200nF'
None
dB(S(Diff2,Diff2))
Ciso_2='470nF'
None
dB(S(Diff2,Diff2))
Ciso_2='650nF'
None
dB(S(Diff2,Diff2))
Ciso_2='1000nF'
None

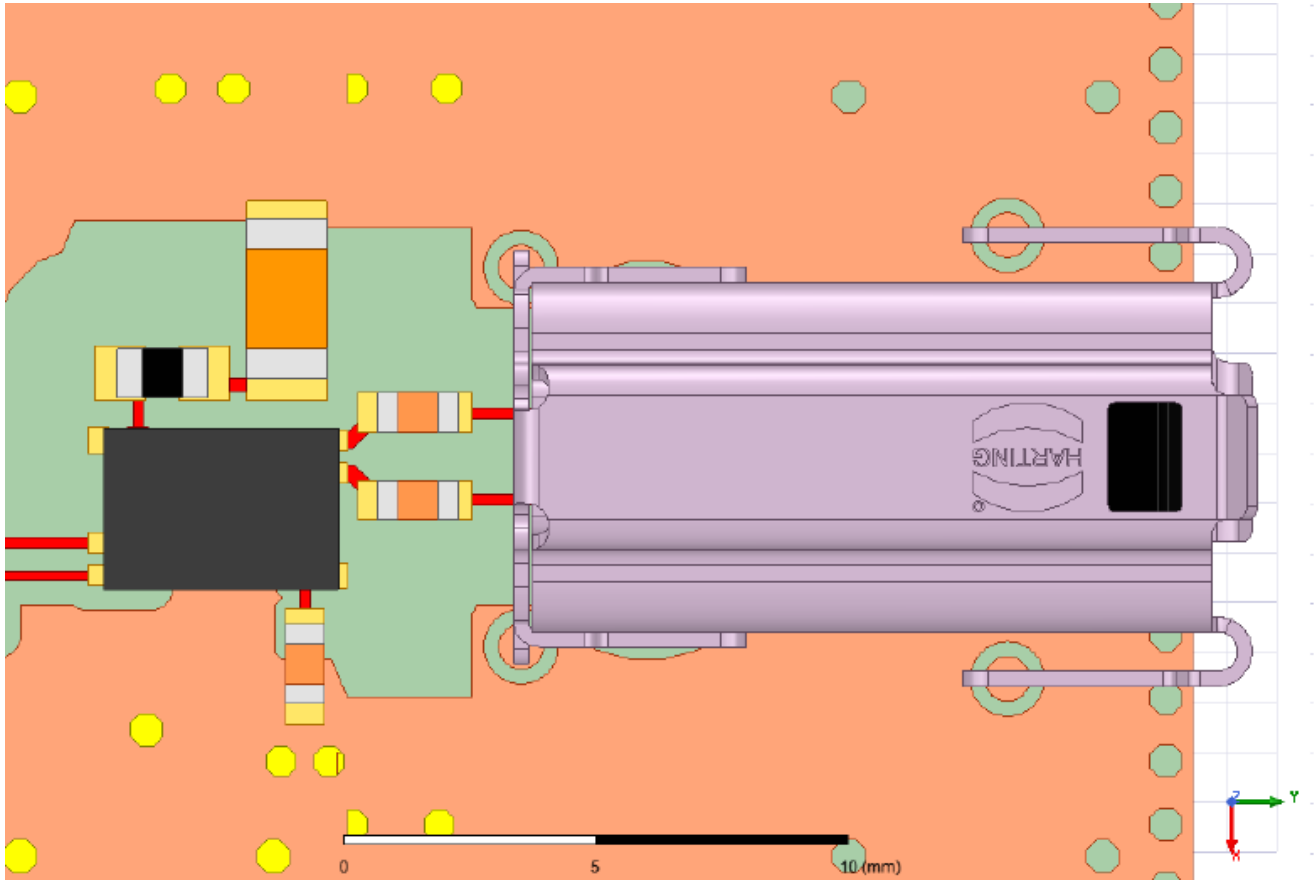


cap [nF]	Start	End	Percent
1000	1007,86	936,03	7,67389934
800	1007,66	935,2	7,74807528
650	1009,8	936,57	7,8189564
470	1019	944	7,94491525
400	1026,56	950,63	7,98733471
300	1044,21	965,75	8,12425576
200	1072	988	8,50202429
100	1096,85	997	10,0150451
50	1110	980	13,2653061



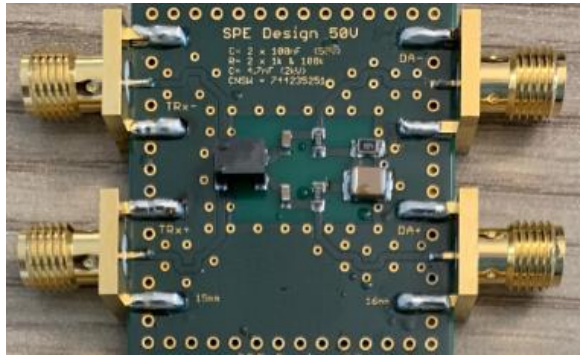
10Base-T1L

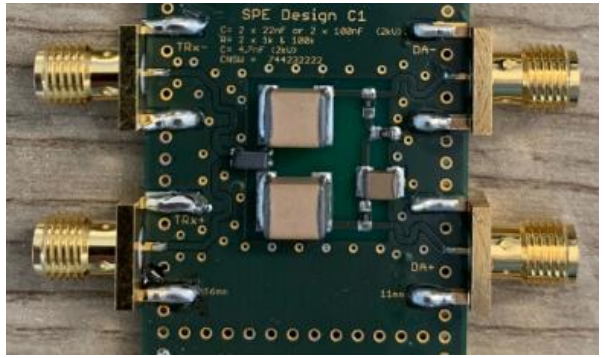
Physical size

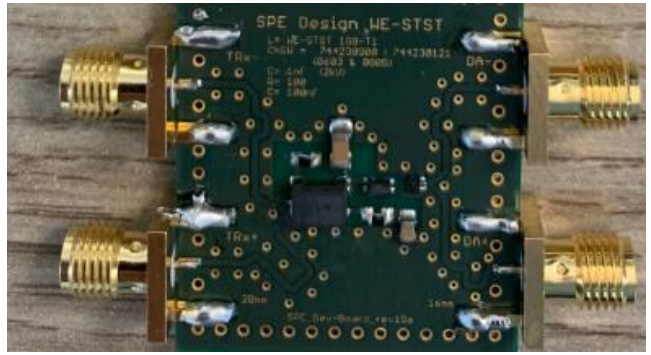


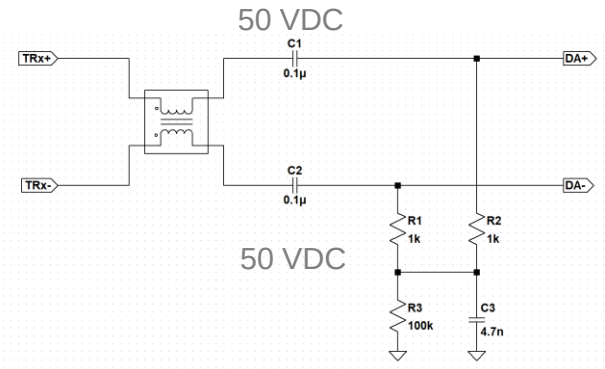
100BASE-T1L

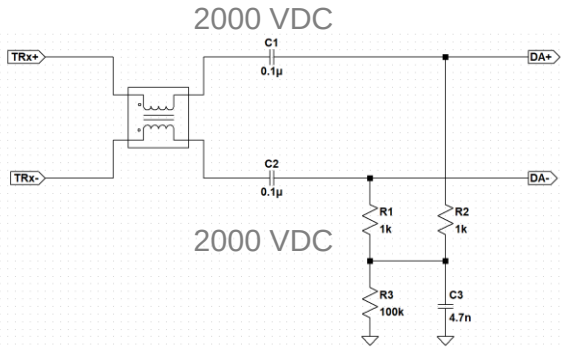
100BASE-T1L

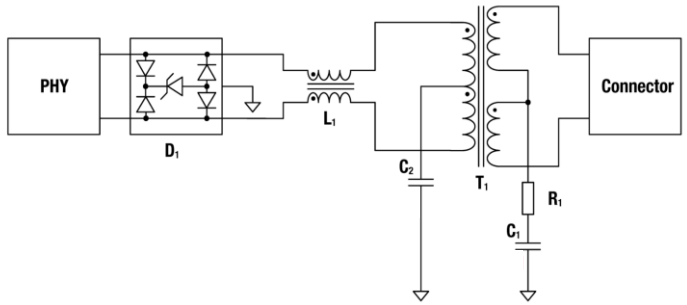

SPE Design 50V
TRx-
TRx+
DA-
DA+


SPE Design C1
TRx-
TRx+
DA-
DA+


SPE Design WE-STST
TRx-
TRx+
DA-
DA+


50 VDC
TRx+
TRx-
C1
0.1µ
C2
0.1µ
DA+
DA-
R1
1k
R2
1k
R3
100k
C3
4.7n
50 VDC

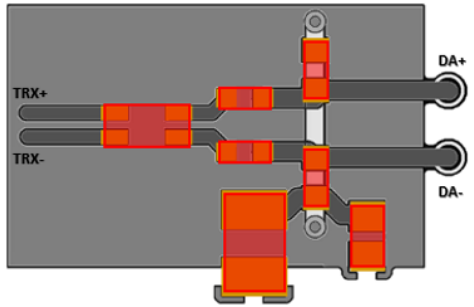

2000 VDC
TRx+
TRx-
C1
0.1µ
C2
0.1µ
DA+
DA-
R1
1k
R2
1k
R3
100k
C3
4.7n
2000 VDC


PHY
D1
L1
C2
T1
R1
C1
Connector

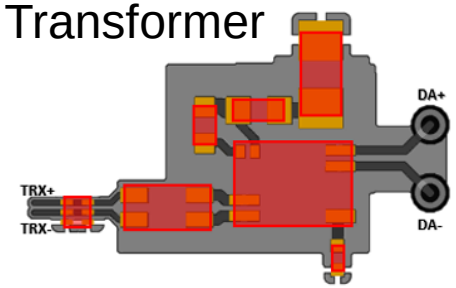
100BASE-T1L

Required space on PCB

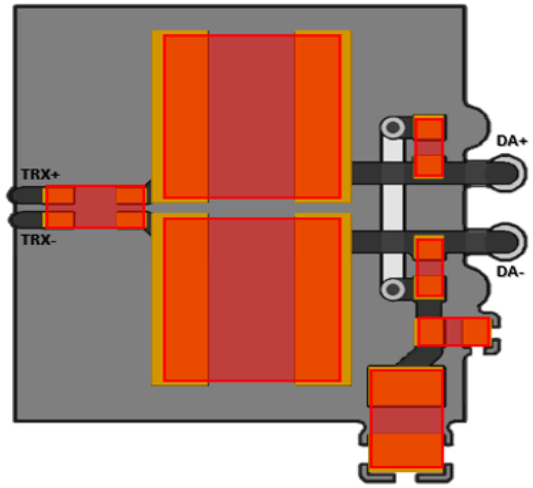
50 V



Transformer

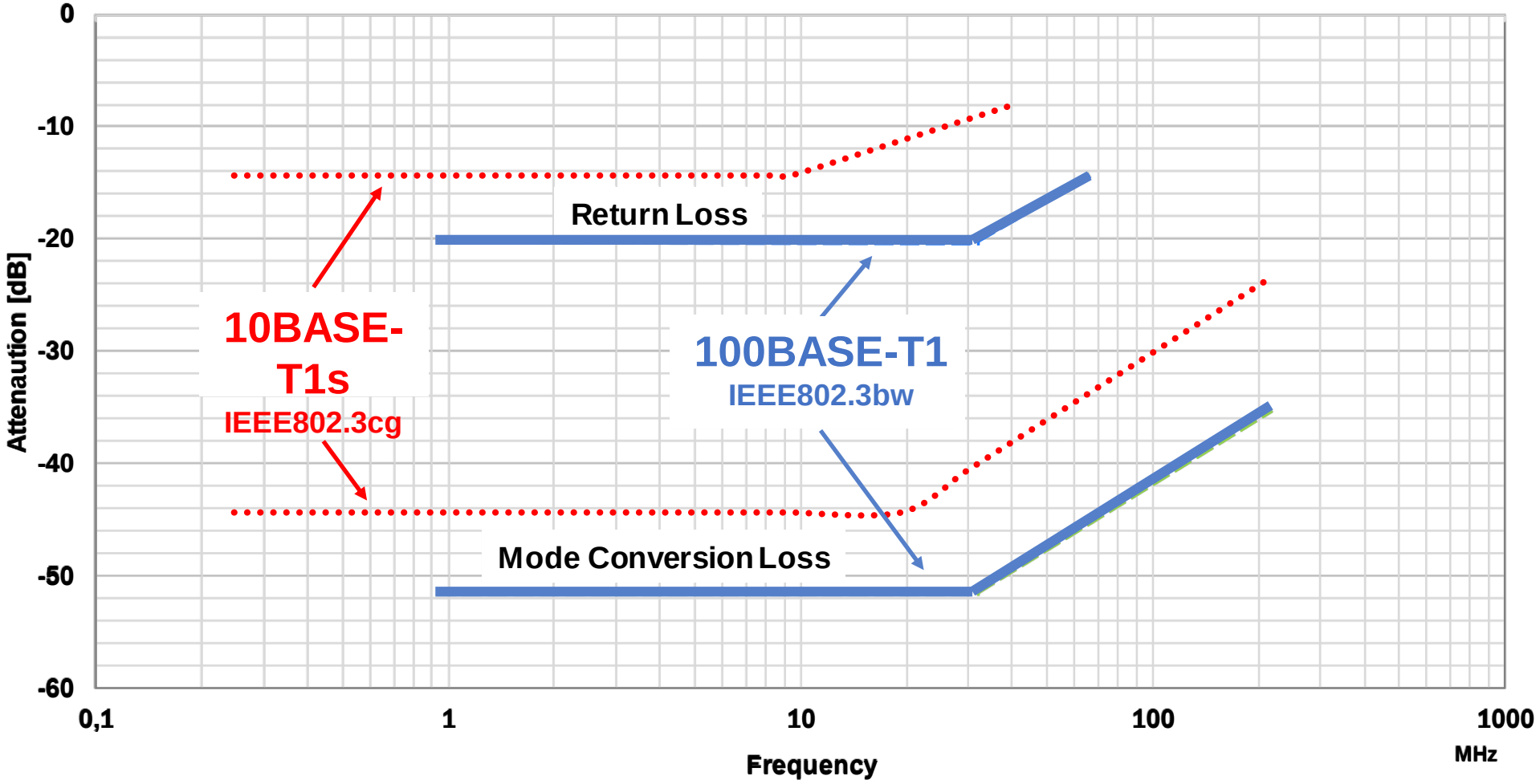


2000 V



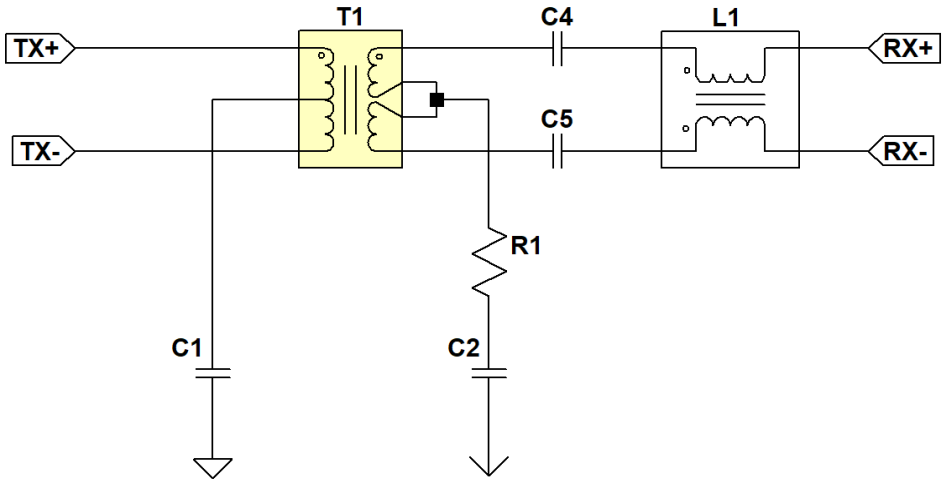
100BASE-T1 vs.10BASE-T1s

Schematic for 100BASE-T1 can be used for 10BASE-T1s!



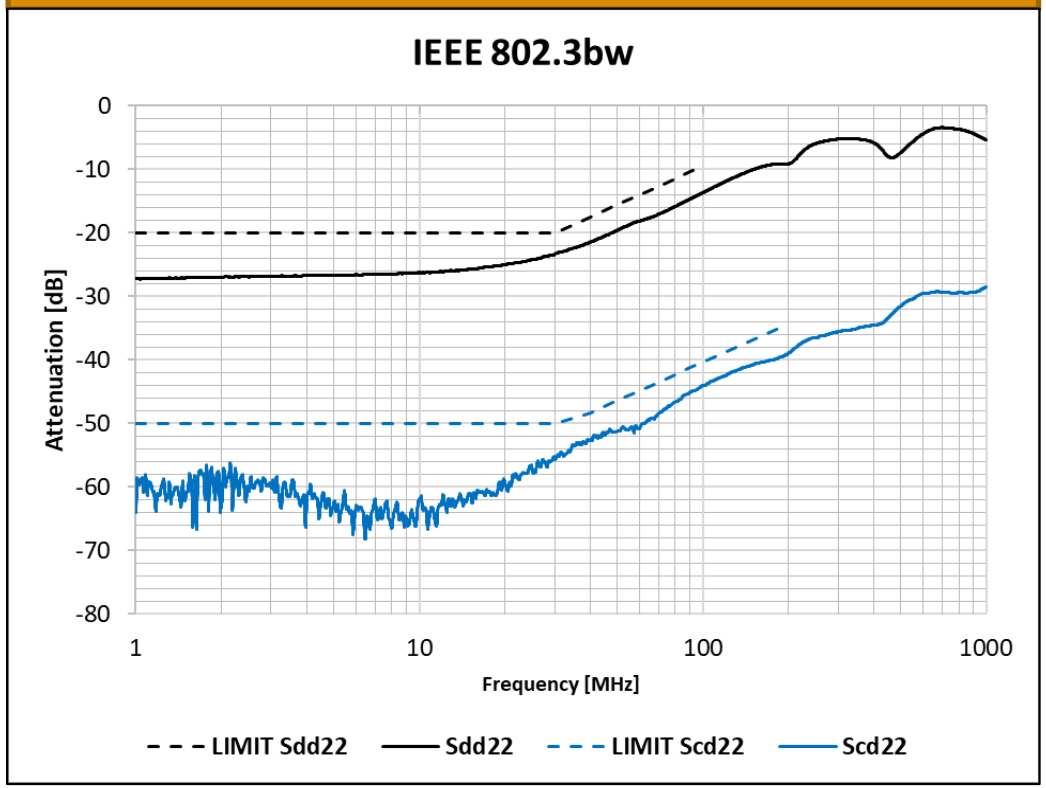
100BASE-T1L

Circuit



Name	Value	Isolation	Size	Article number
C1	100 nF	50 V	0402	885012205086
C2	1 nF	2 kV	1206	885342208024
C4, C5	470 nF	100 V	0603	885012207130
T1	350 µH	1500 V	1812	74930030
L1	2.57 µH	50 V (DC) 125 V (AC)	1206	744232222
R1	100 Ω		0603	

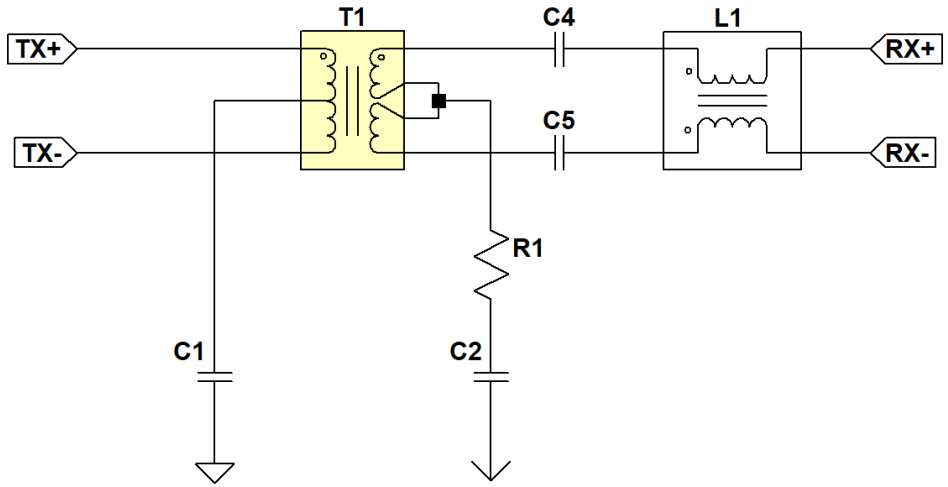
Limits



1000BASE-T1L

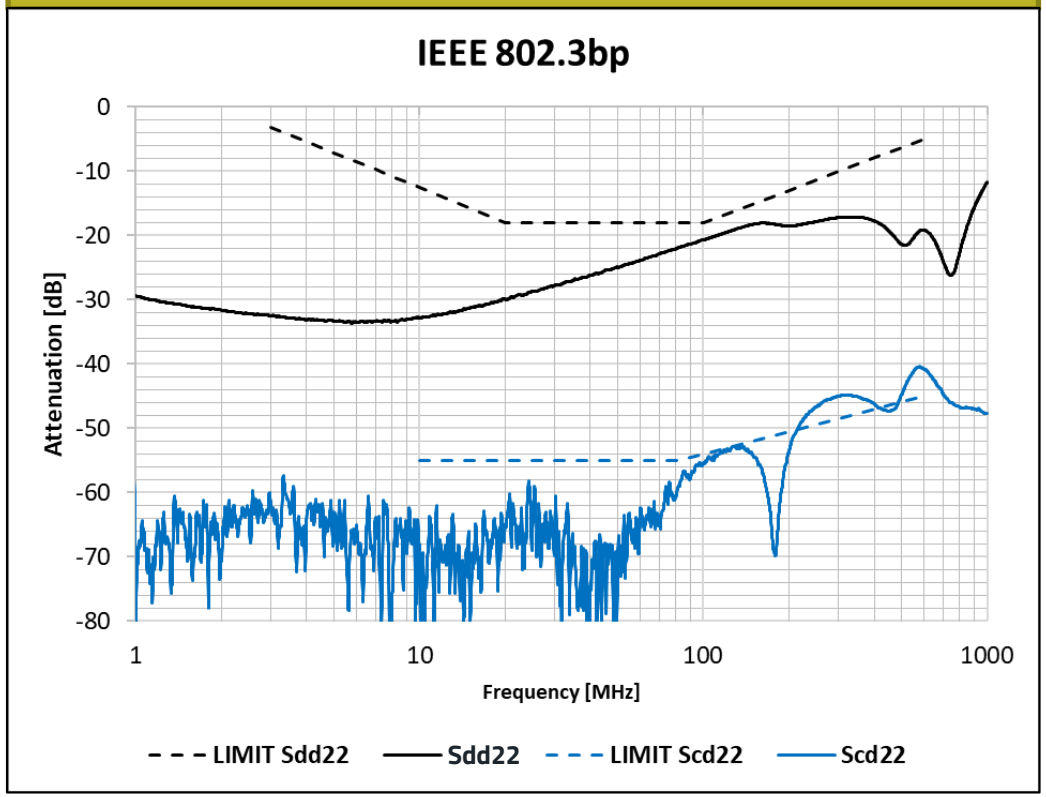
1000BASE-T1L

Circuit



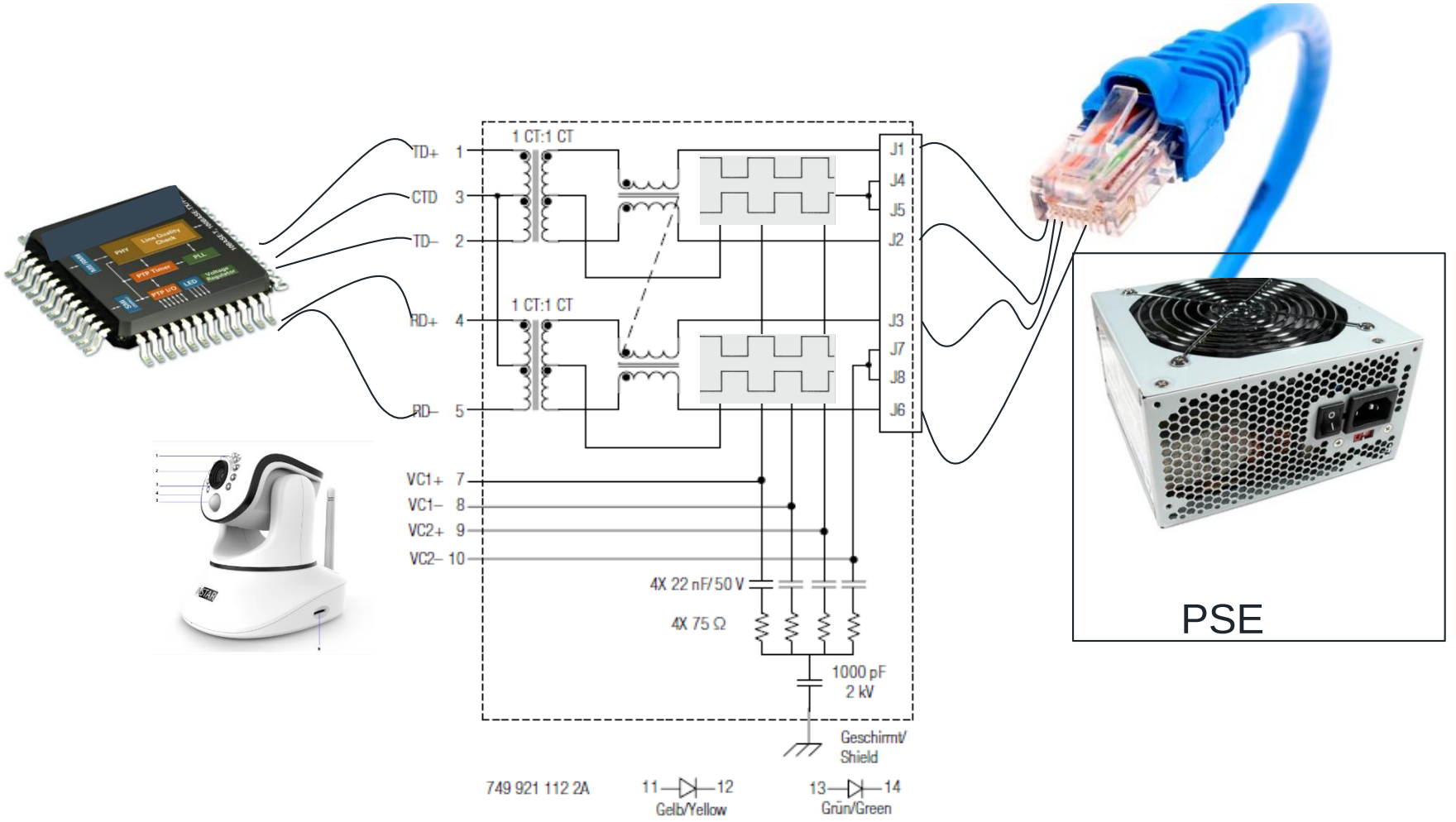
Name	Value	Isolation	Size	Article number
C1	100 nF	50 V	0402	885012205086
C2	1 nF	2 kV	1206	885342208024
C4, C5	470 nF	100 V	0603	885012207130
T1	110 µH	1500 V	1812	74930120
L1	304 nH	50 V (DC) 125 V (AC)	1206	744232261
R1	100 Ω		0603	

Limits

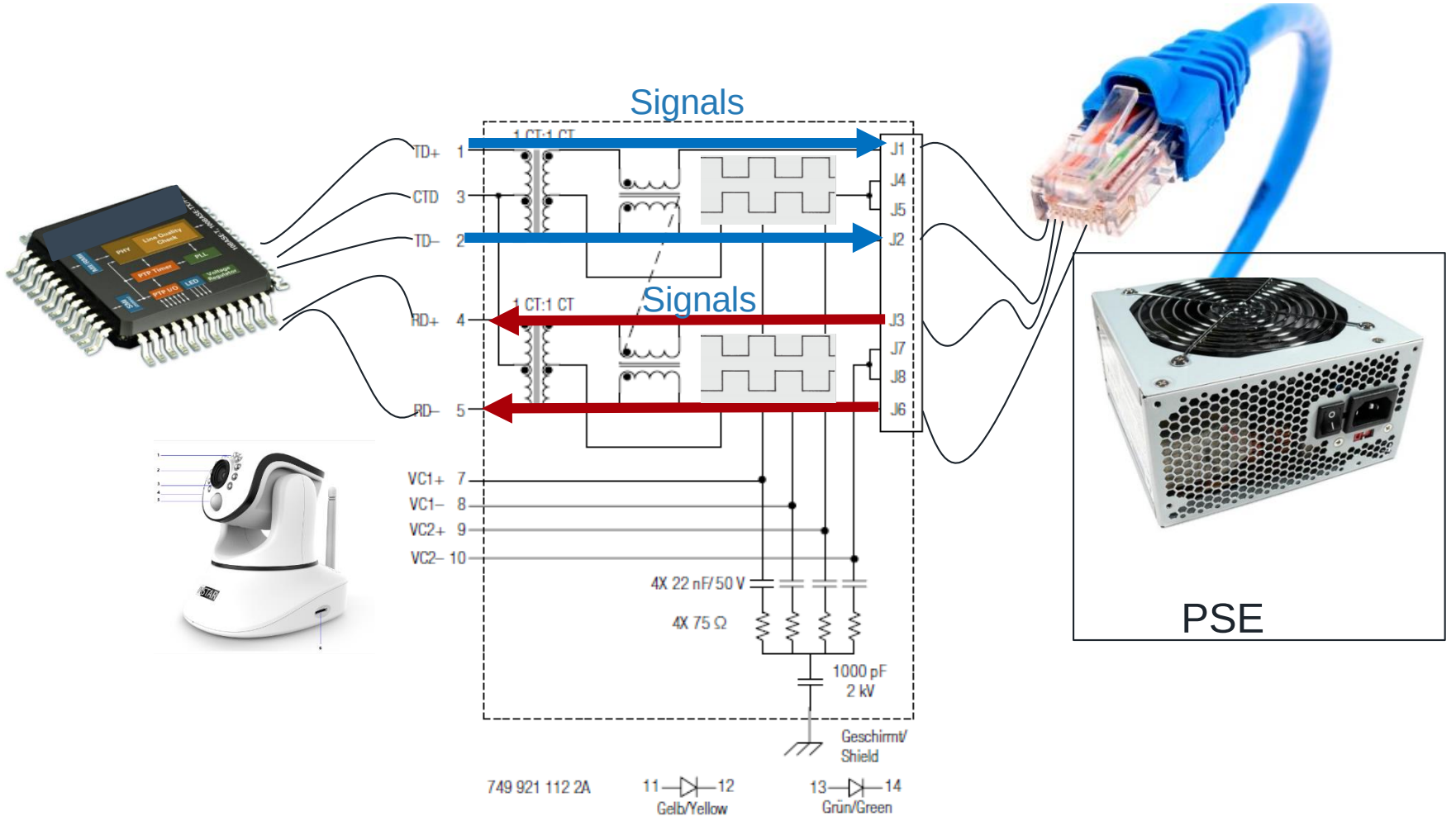


POWER OVER DATA LINE (PODL)

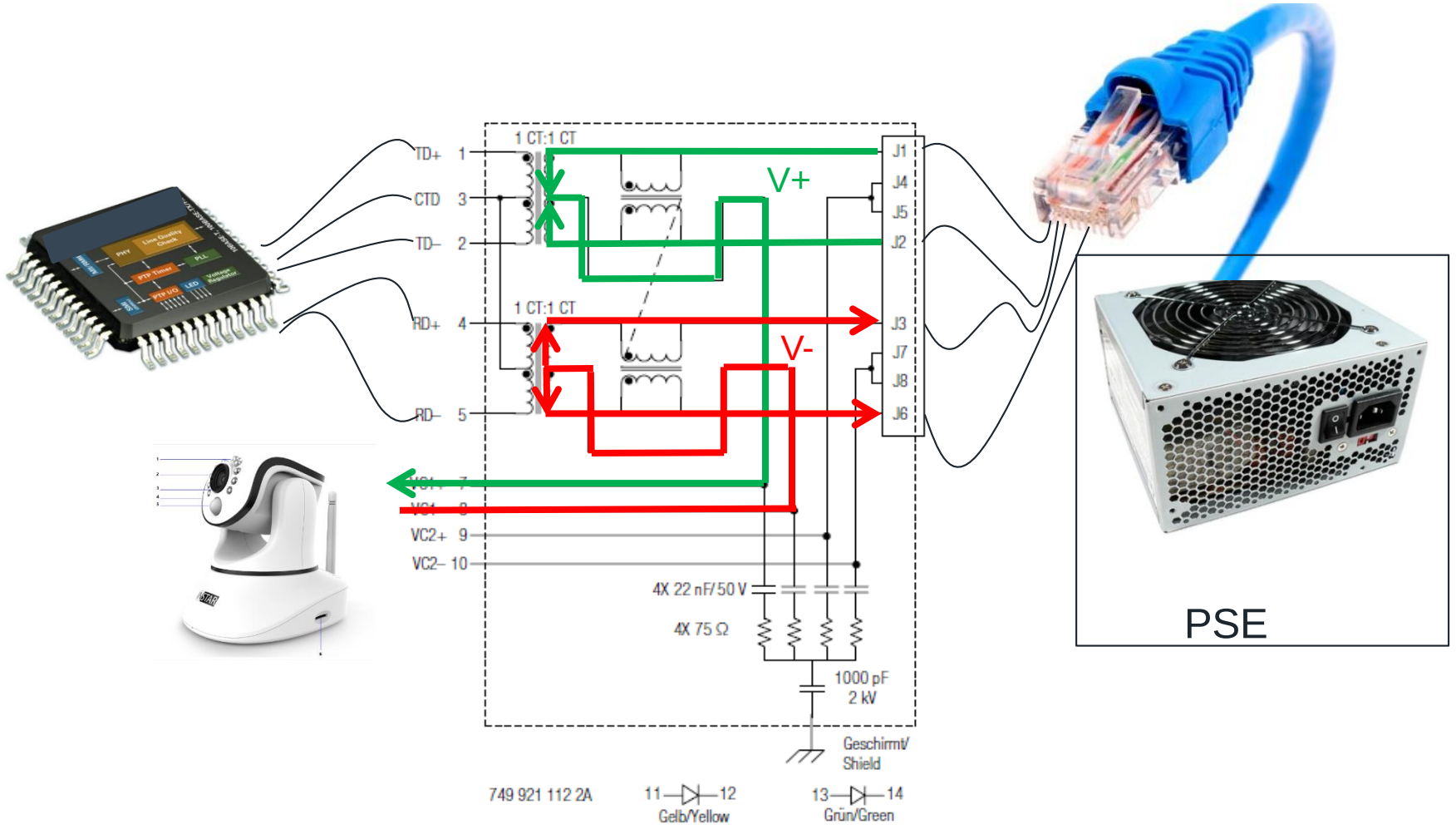
Power over Ethernet



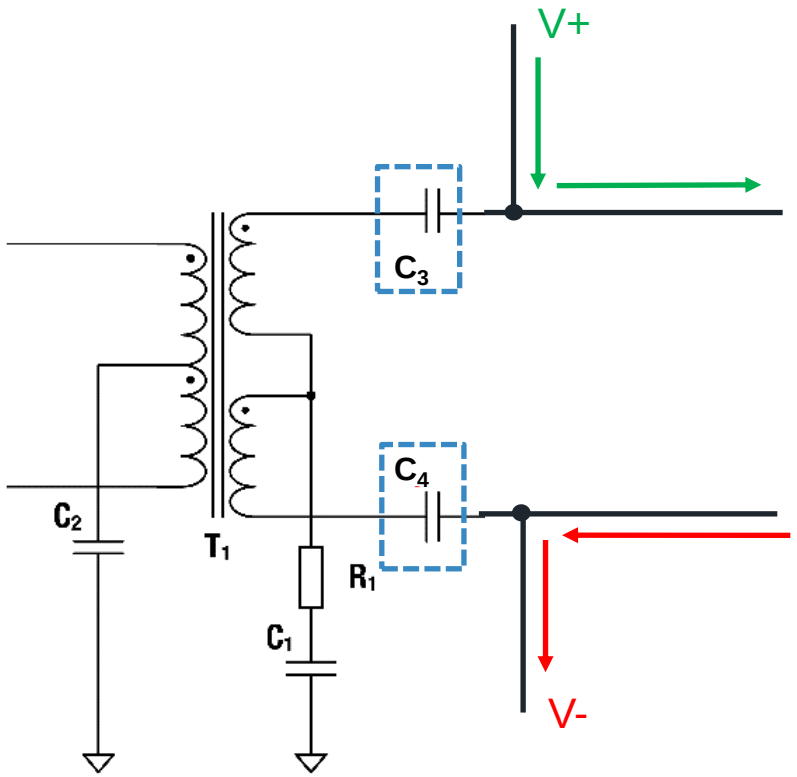
Power over Ethernet



Power over Ethernet

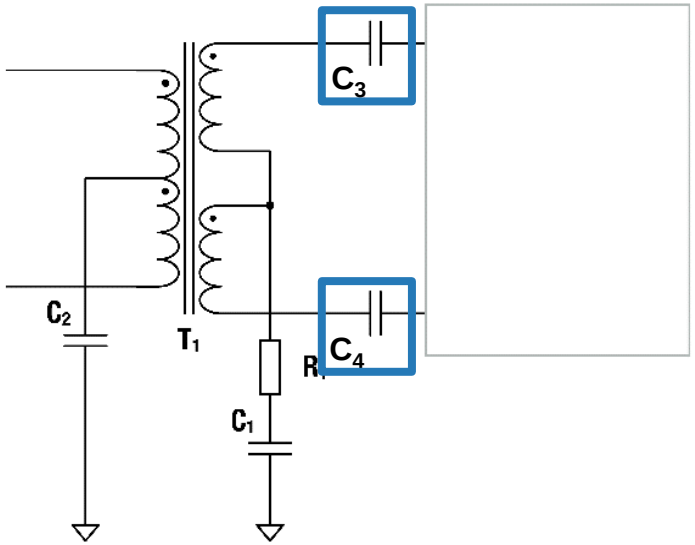


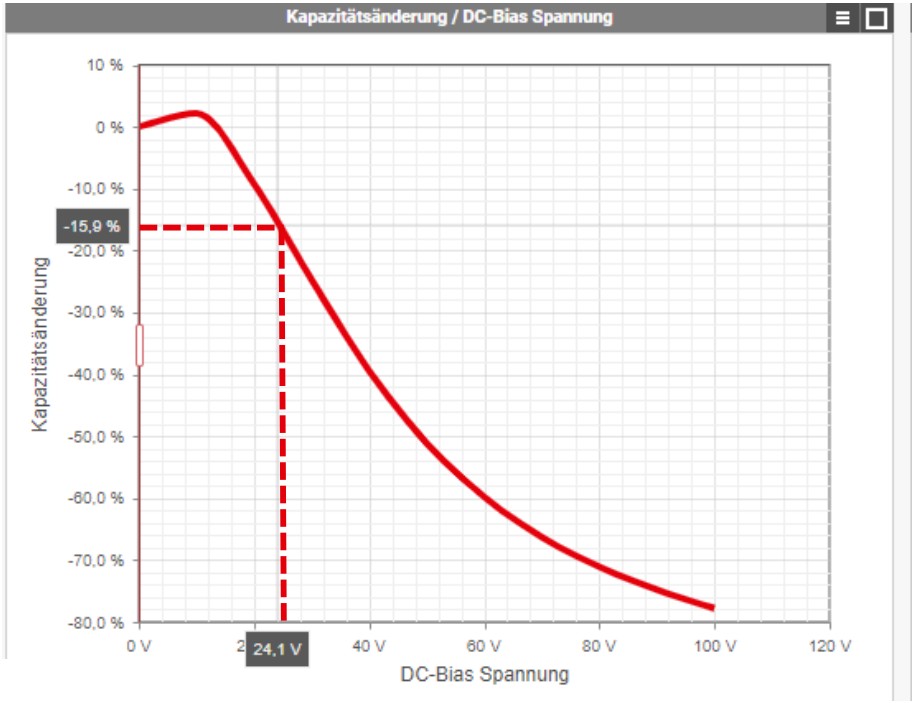
Power over data line



Power over data line

470 nF/100 V

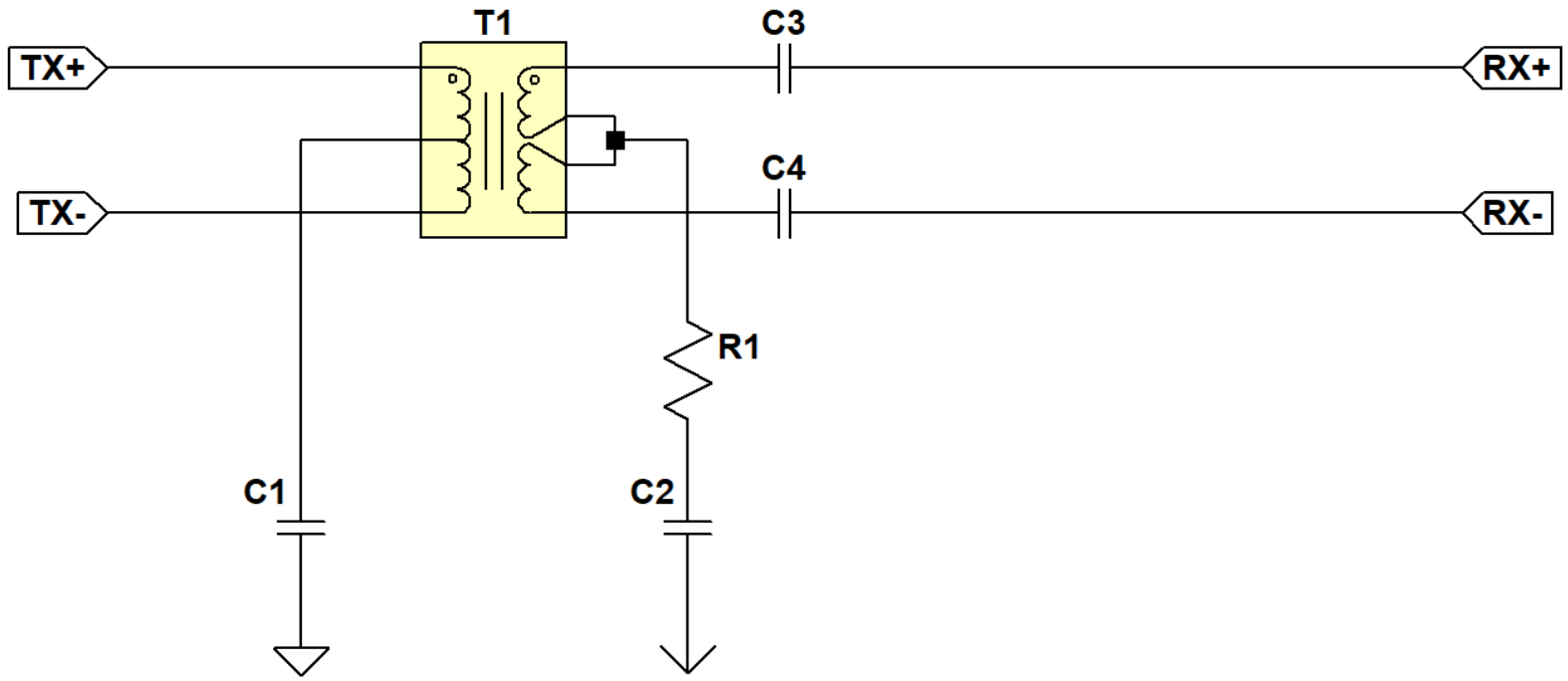




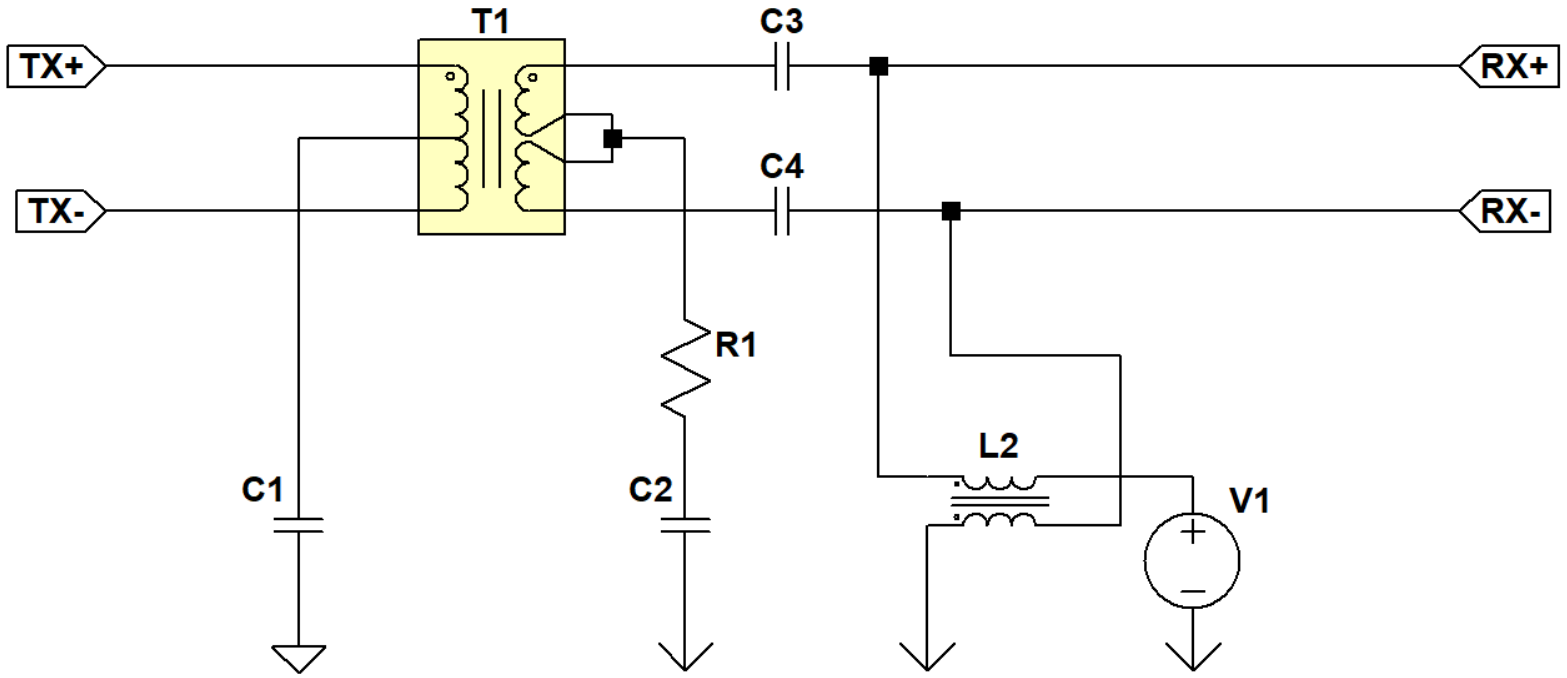
146.8.5 MDI DC power voltage tolerance

The DTE shall withstand without damage the application of any voltages between 0 V dc and 60 V dc with the source current limited to 2000 mA, applied across BI_DA+ and BI_DA–, in either polarity, under all operating conditions, for an indefinite period of time. This requirement ensures that all devices tolerate DC powering voltages, such as those in Clause 104, even if the device does not require power.

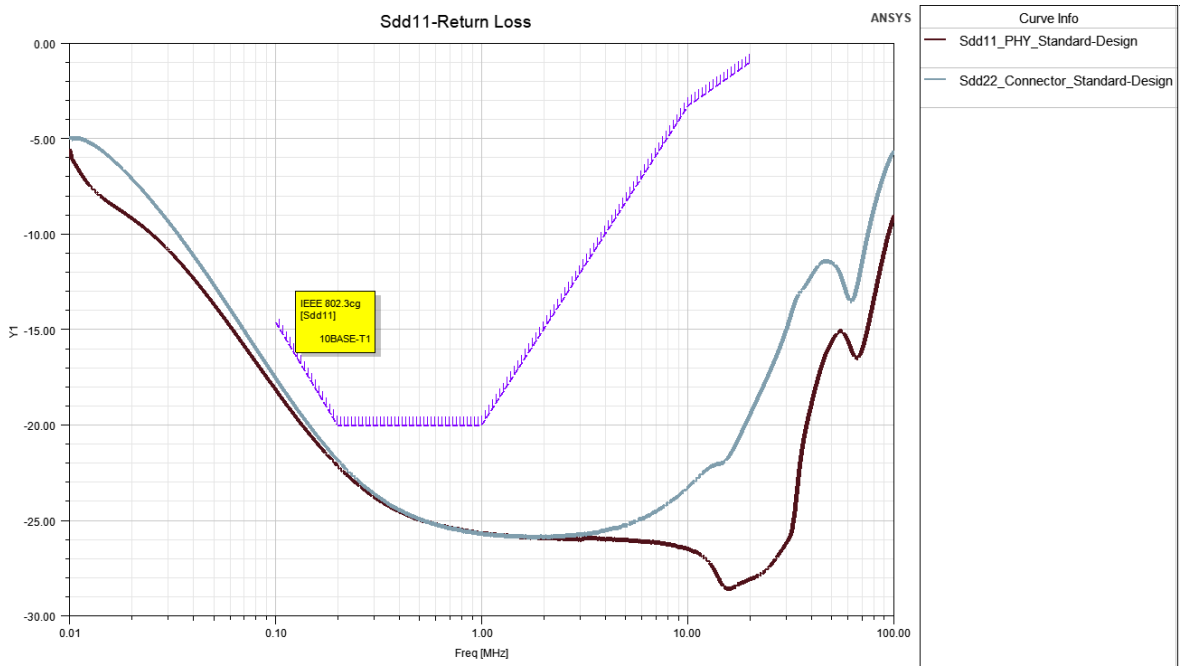
Power over data line

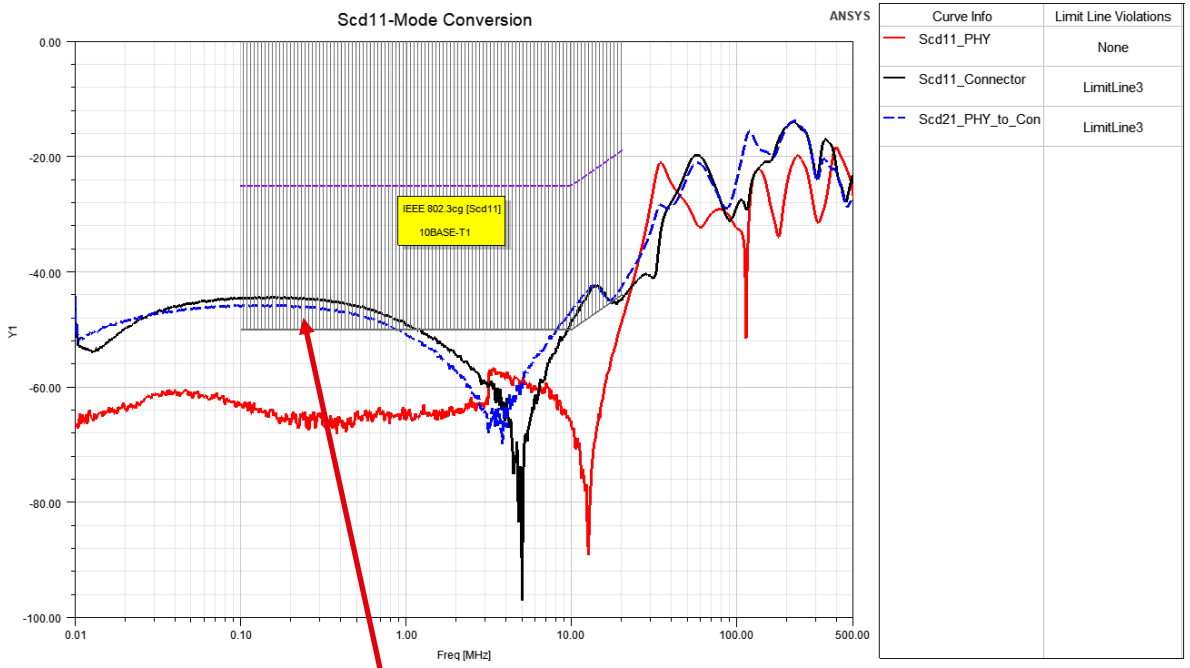


Power over data line



PoDL Performance (Standard Design)

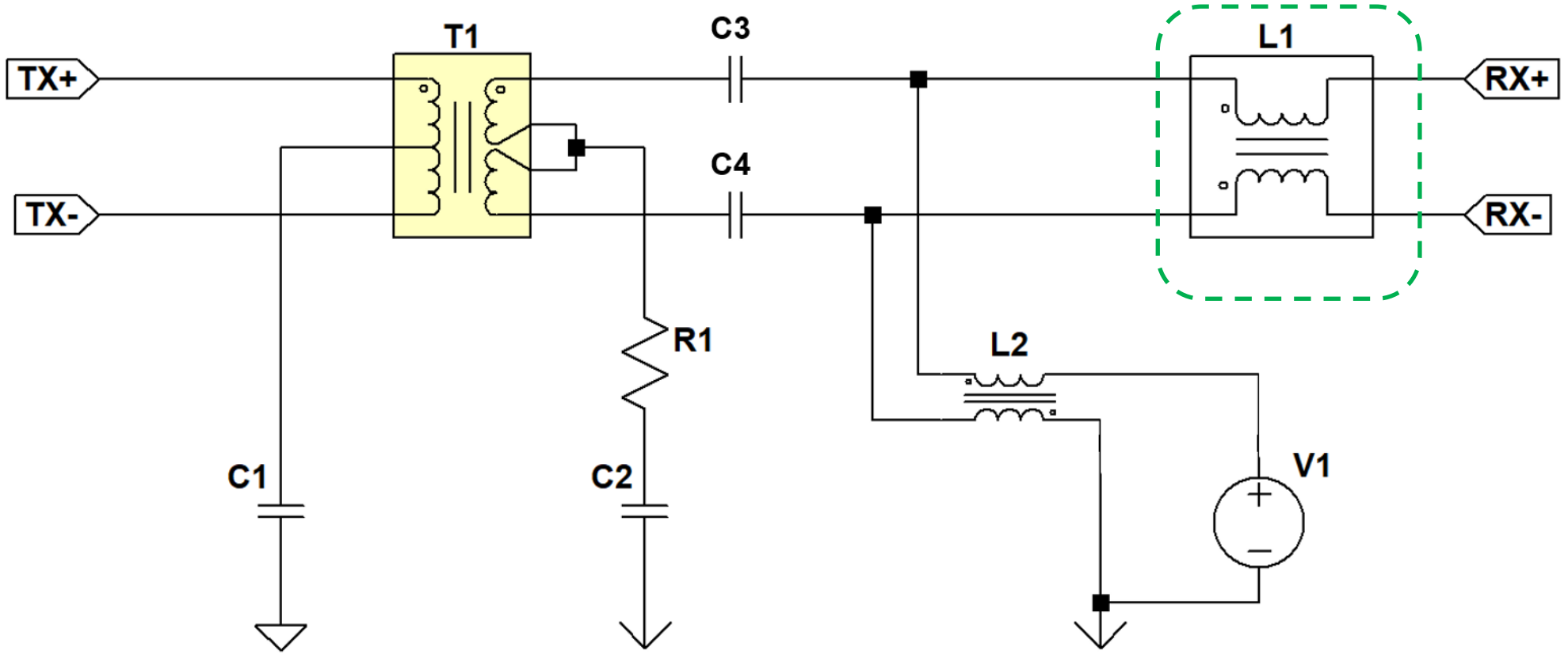




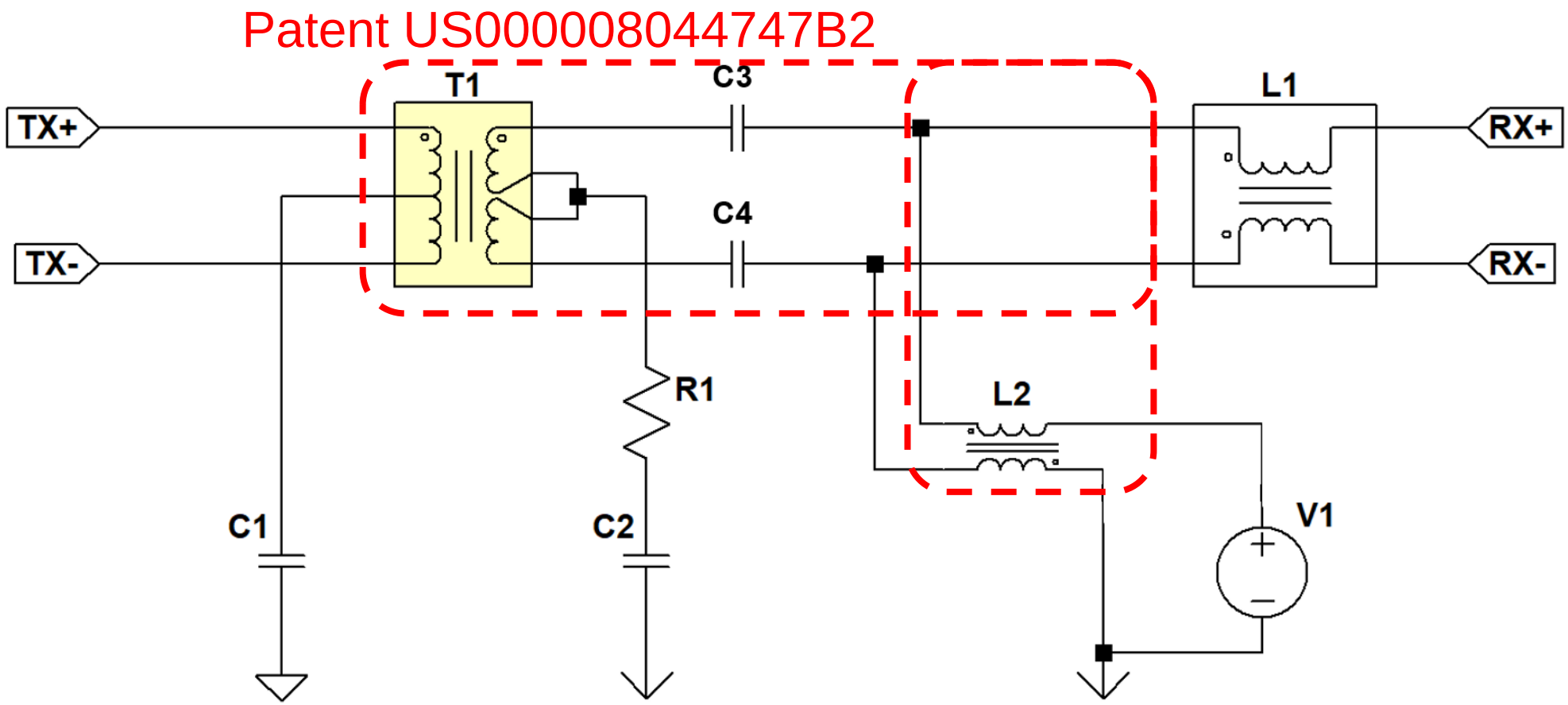
-45 dB violation: high mode conversion

IMPROVEMENTS ON THE PODL DESIGN

Design improvements

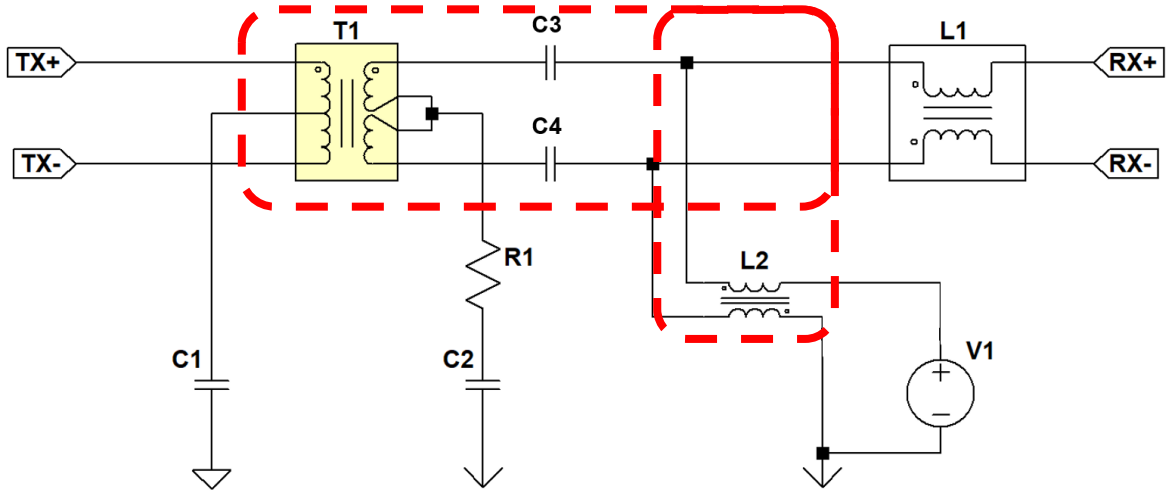


Design improvements

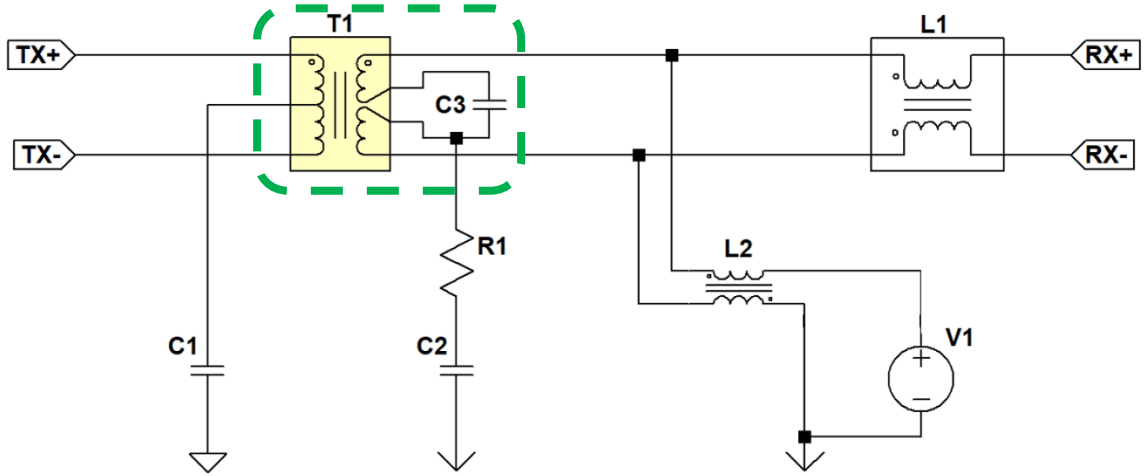


Design improvements

Patent US000008044747B2



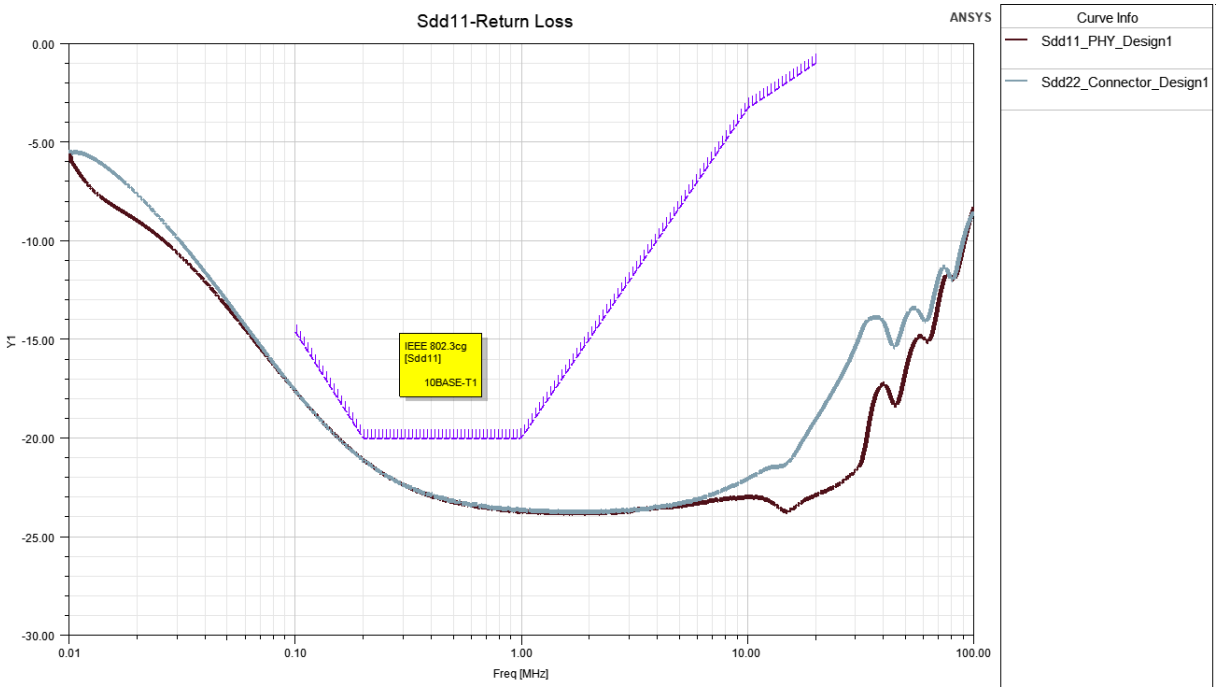
Alternative



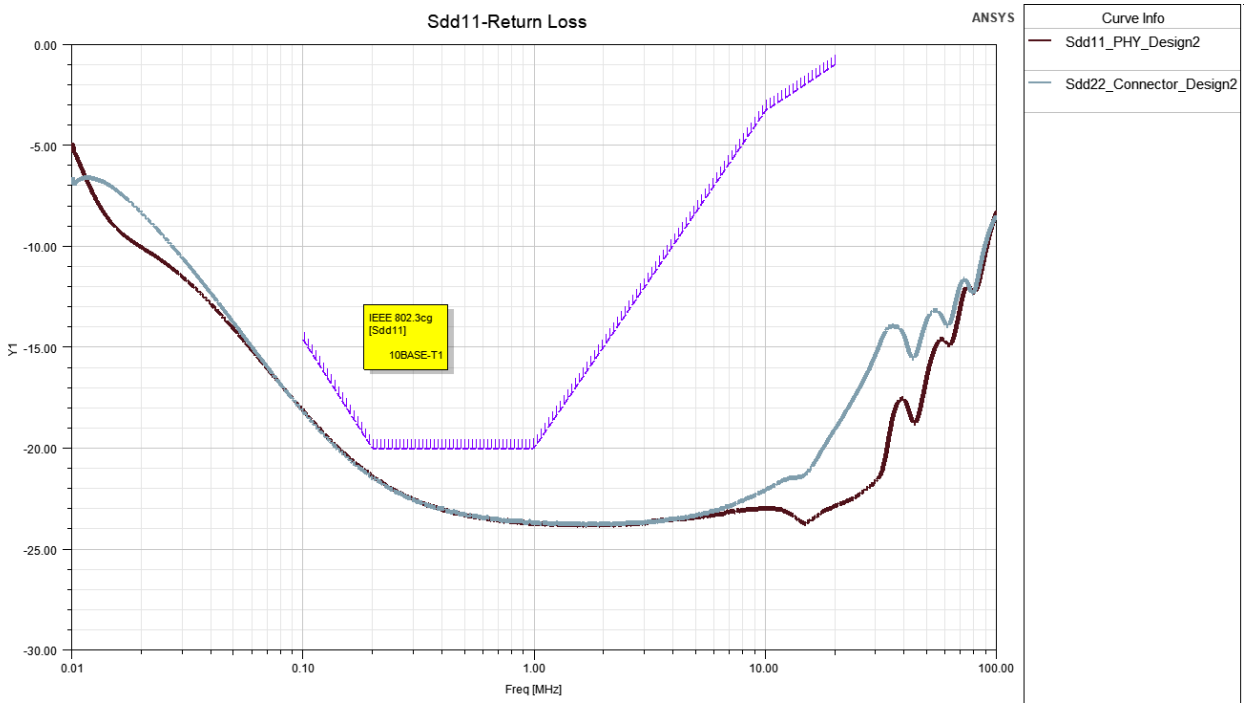
Design improvements (S_{dd11})

Return loss

Patent US000008044747B2



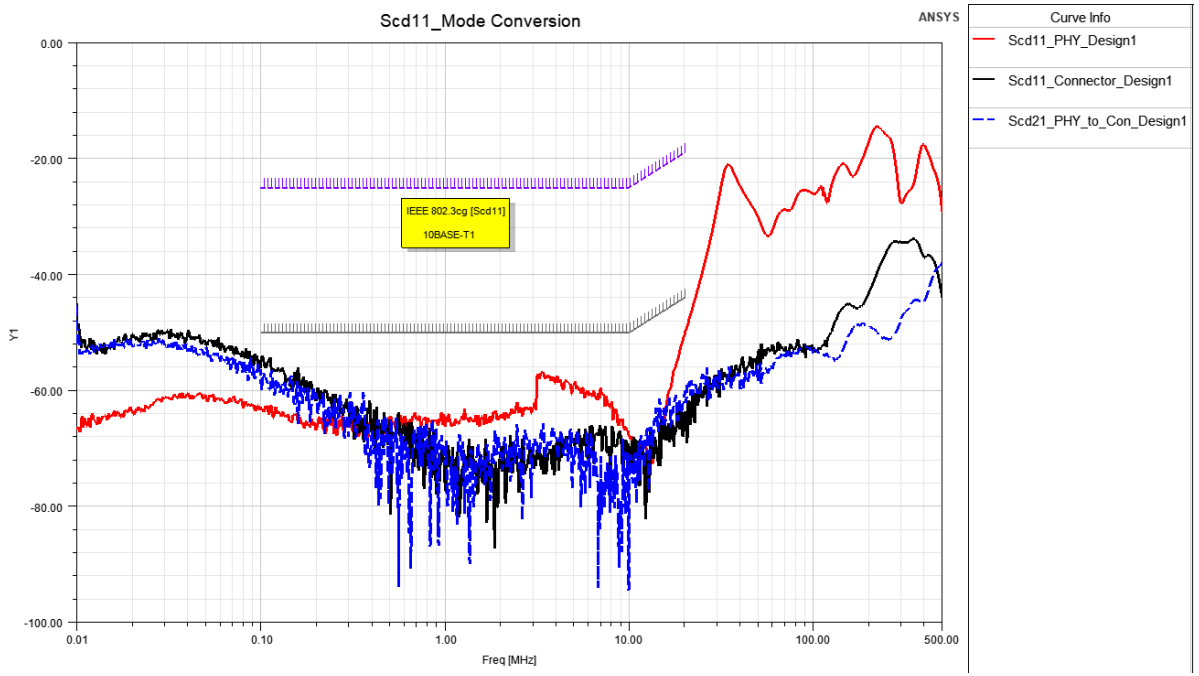
Alternative



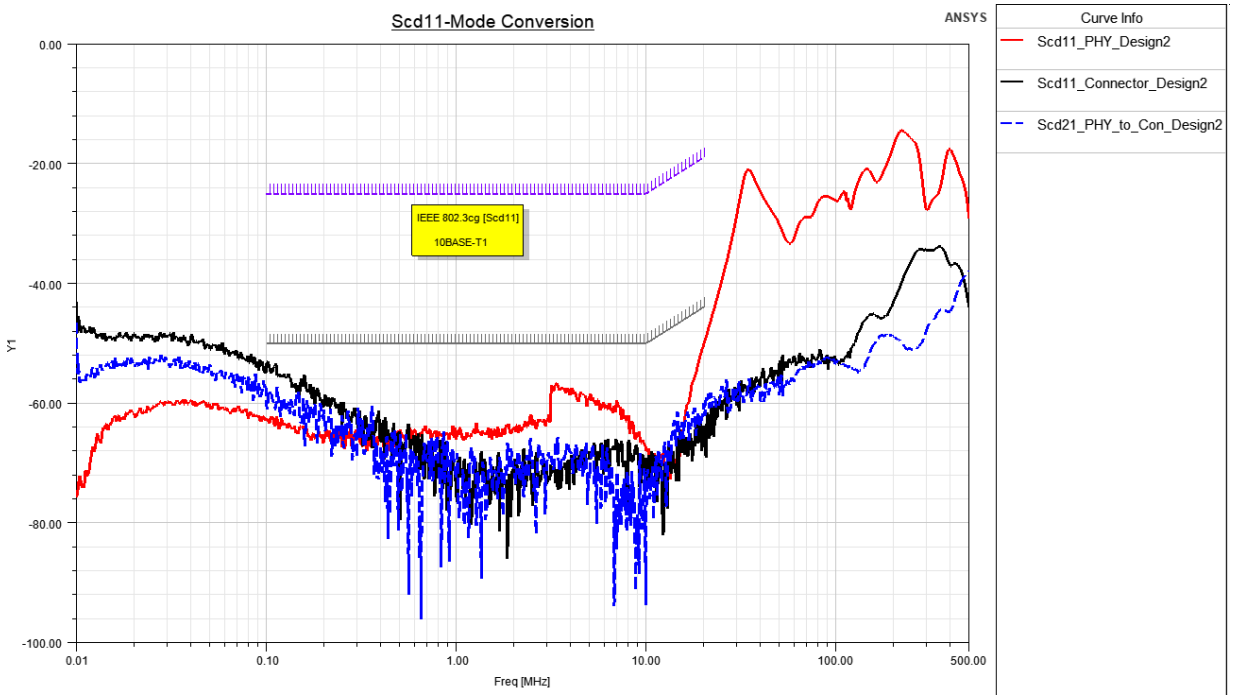
Design improvements (S_{cd11})

Mode conversion loss

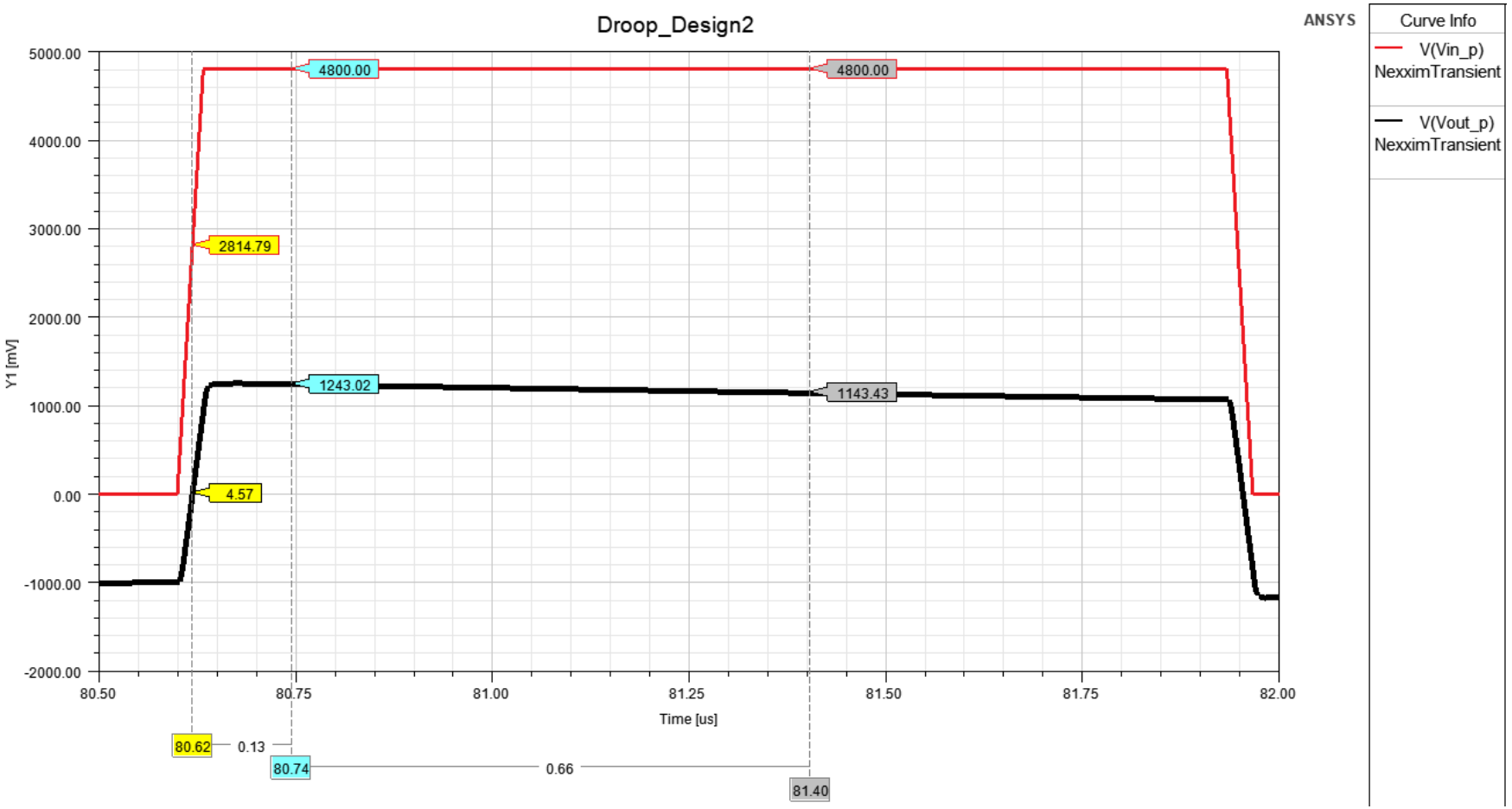
Patent US000008044747B2



Alternative



Voltage Droop Simulation



Droop:

Max:	10%
WE Design:	**8** %

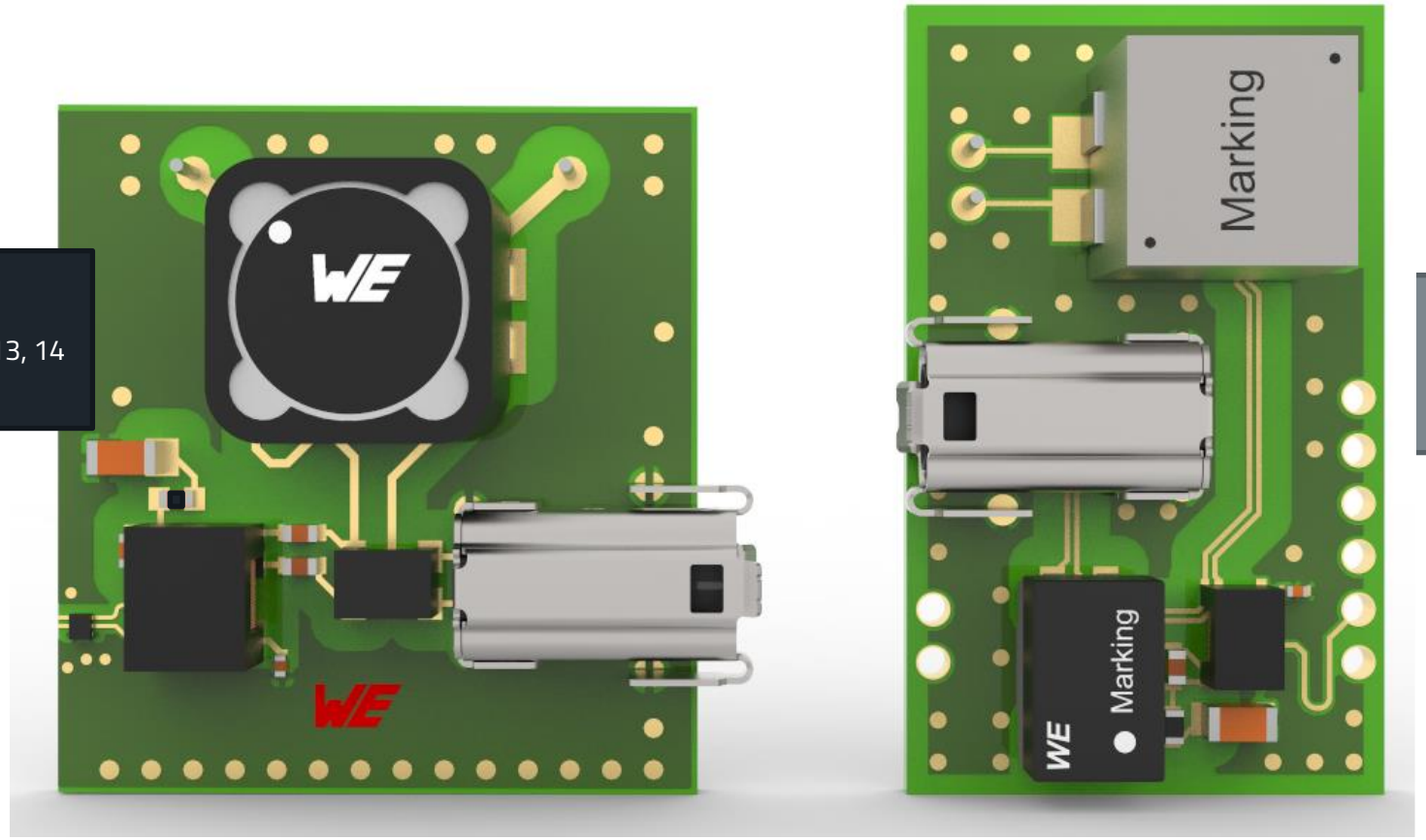
PoDL layout

Improvements

PoDL Classes

0, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 13, 14

I_{max} = 700 mA



All PoDL Classes

Class 0 - 15

I_{max} = 1600 mA

2021

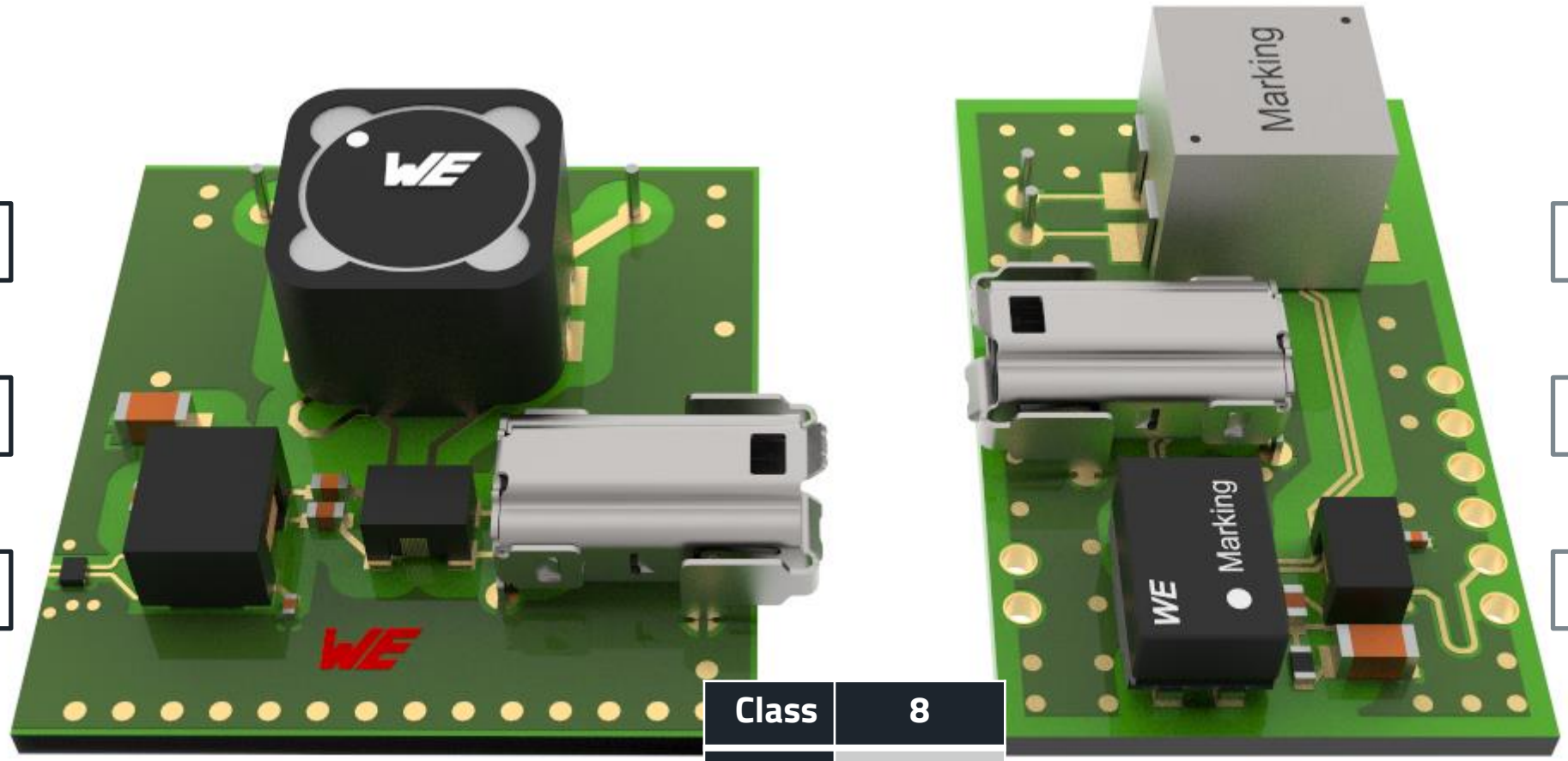
2022

PoDL layout

30 W

70 m

AWG 22



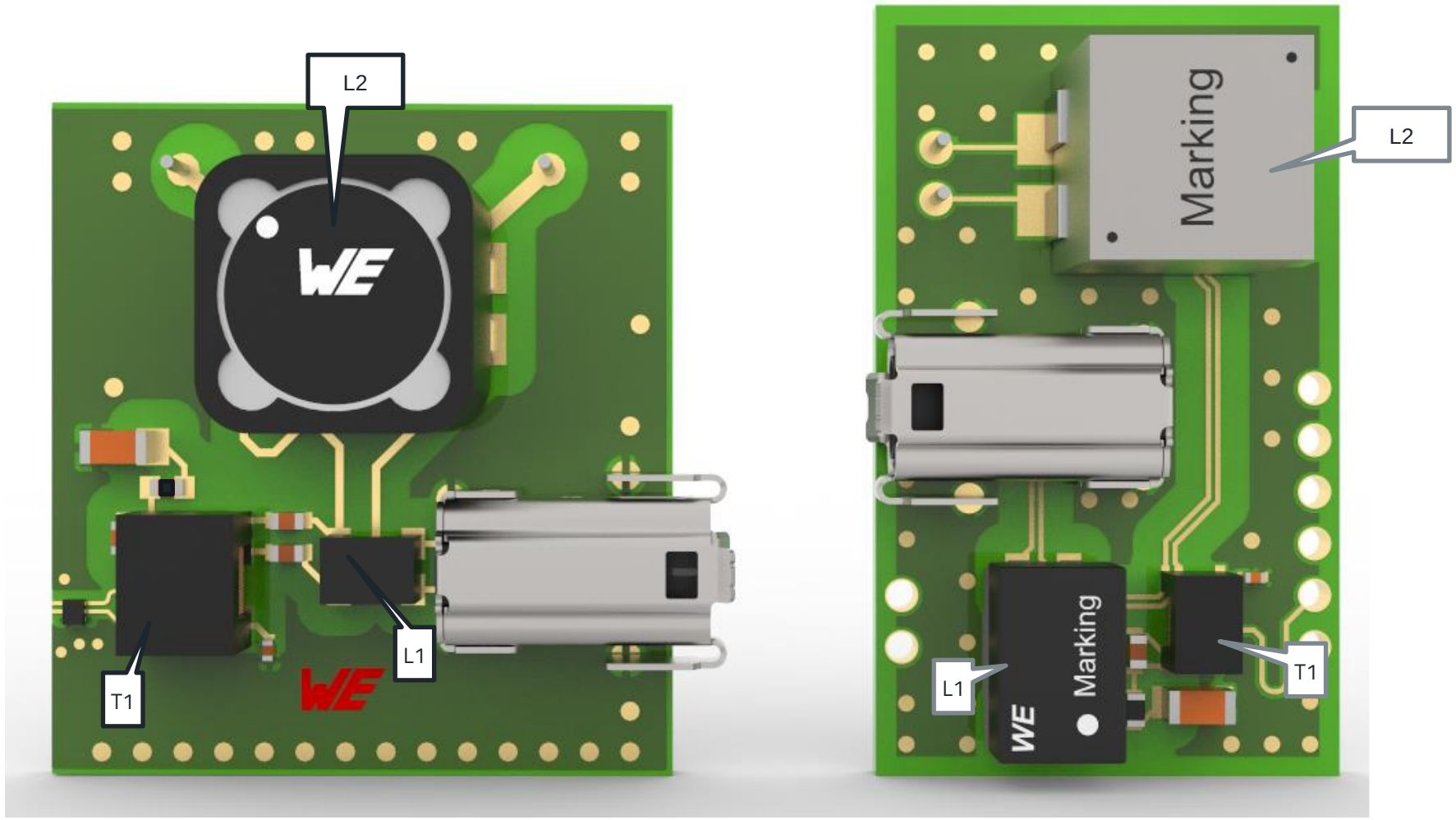
30 W

100 m

AWG 22

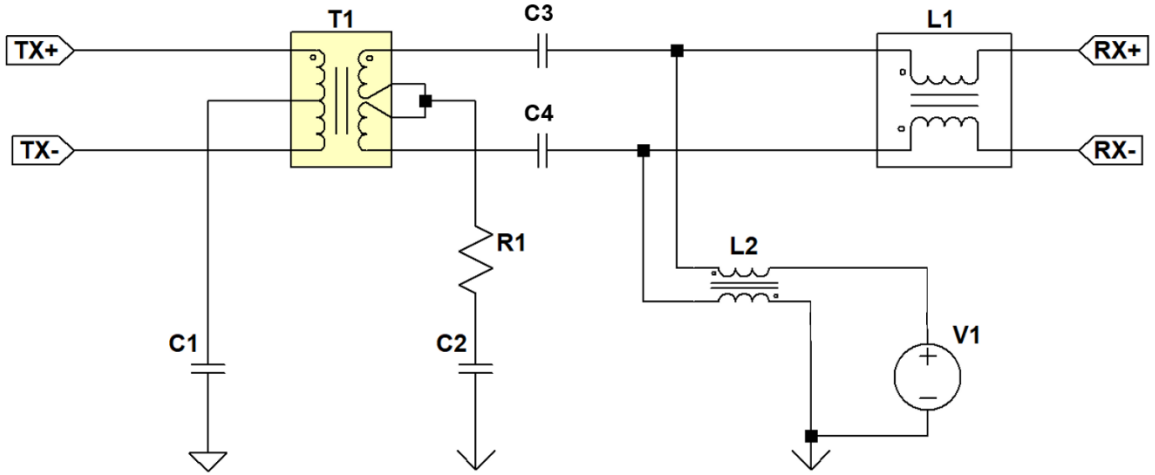
Class	8
U	48...60V
I	0,73A
P	30W

PoDL layout



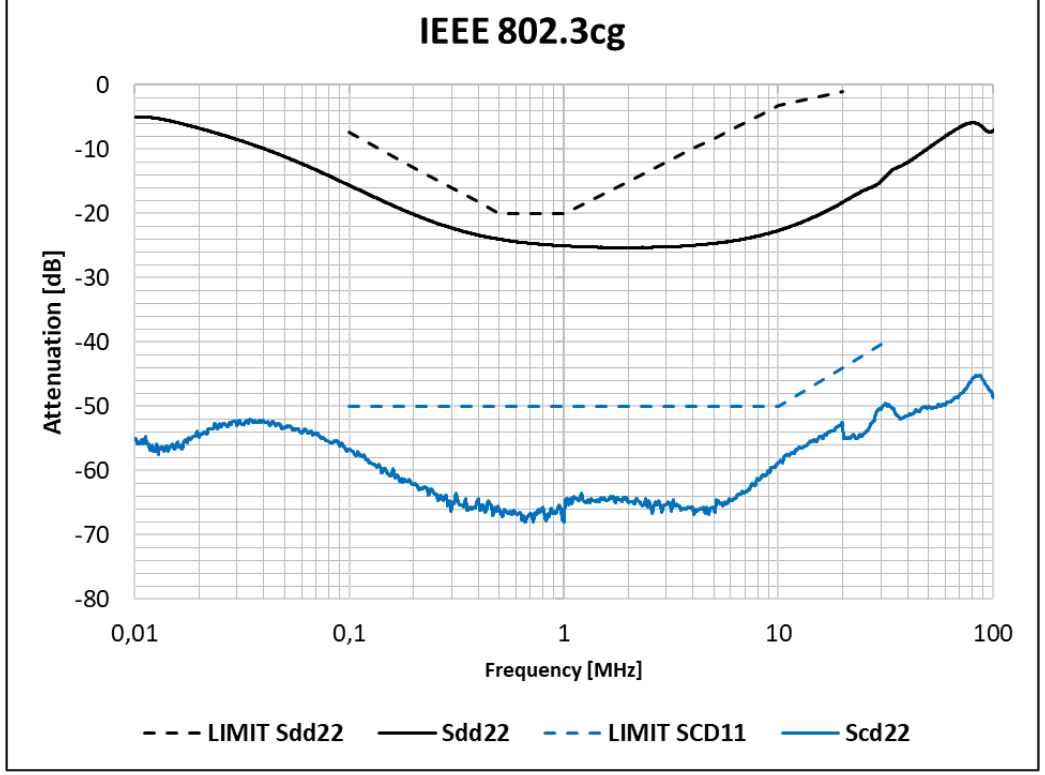
10BASE-T1L & PoDL

Circuit



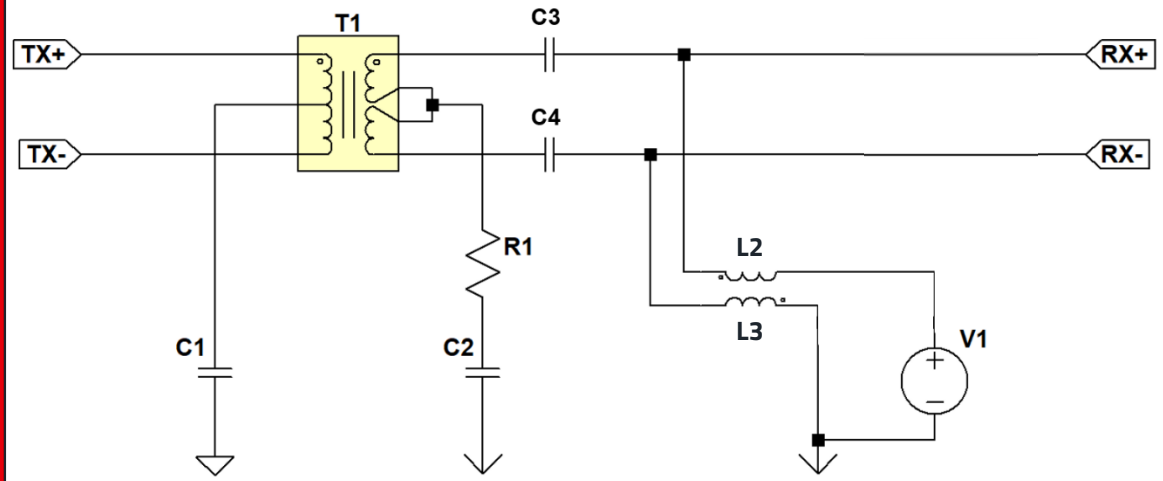
Name	Value	Isolation	Size	Current Rating	Article number
C1	100 nF	50 V	0402		885012205086
C2	1 nF	2 kV	1206		885342208024
C3, C4	470 nF	100 V	0603		885012207130
T1	600 µH	1500 V	5.35 x 6.55 mm		74930200
L1	250 µH 250 µH	125 V 80 V	1812 9.2 x 6 x 5 mm	200 mA 1200 mA	744235251 744224
L2	220 µH	> 80 V	1280	700 mA	744870221
R1	100 Ω		0603		

Limits



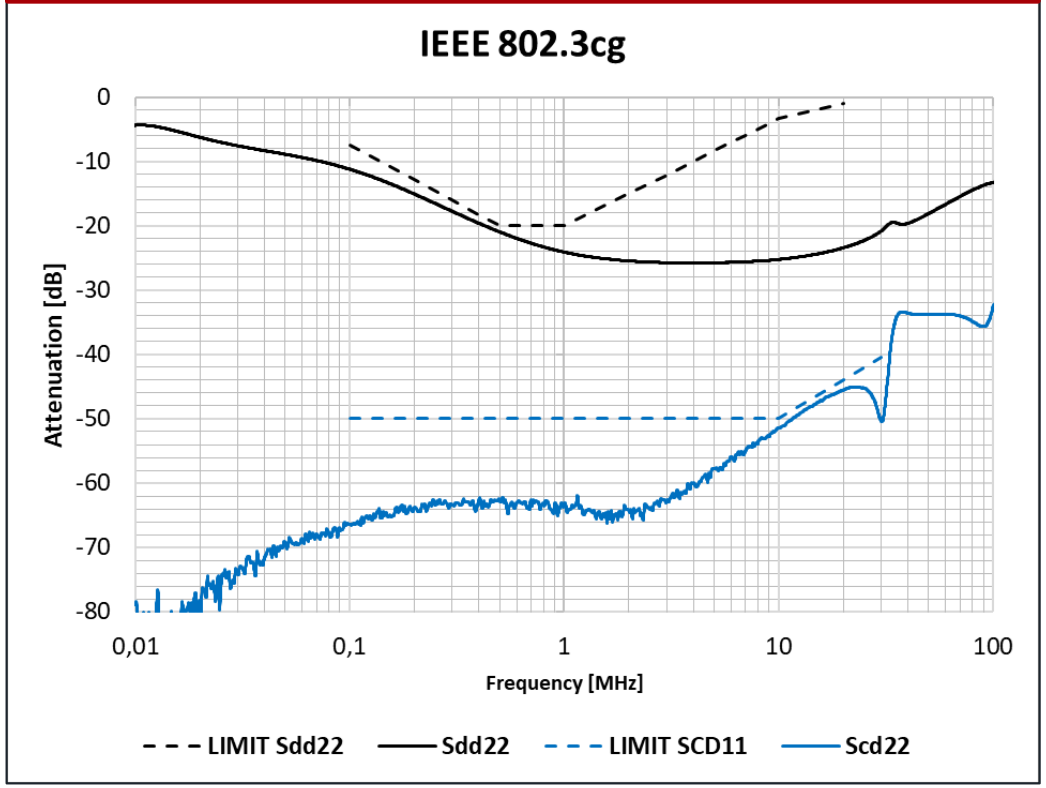
10BASE-T1L & PoDL Class 15

Circuit



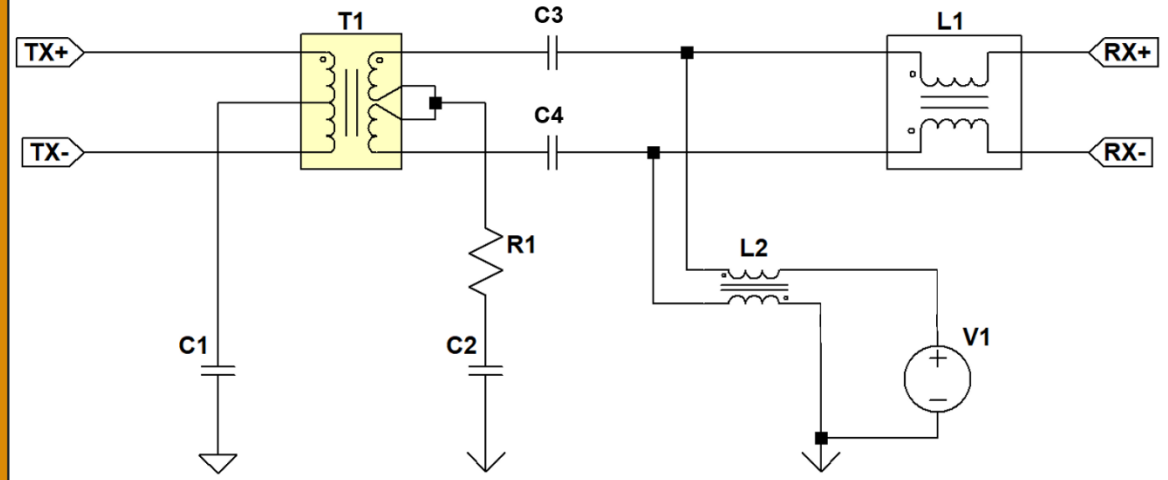
Name	Value	Isolation	Size	Current Rating	Article number
C1	100 nF	50 V	0402		885012205086
C2	1 nF	2 kV	1206		885342208024
C3, C4	470 nF	100 V	0603		885012207130
T1	600 µH	1500 V	5.35 x 6.55 mm		74930200
L2, L3	220 µH		1210	1800 mA	7447709221
R1	100 Ω		0603		

Limits



100BASE-T1L & PoDL

Circuit

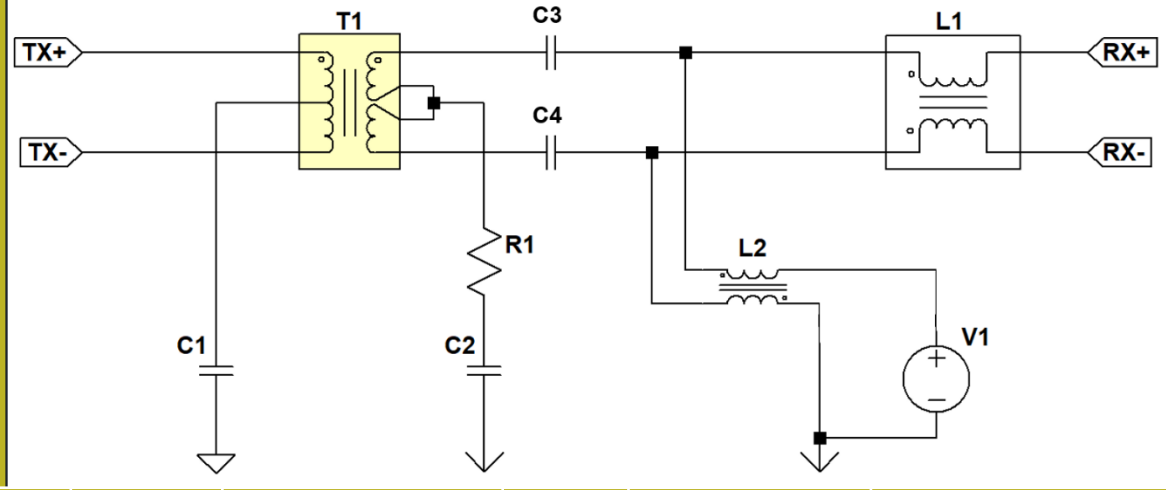


Name	Value	Isolation	Size	Current Rating	Article number
C1	100 nF	50 V	0402		885012205086
C2	1 nF	2 kV	1206		885342208024
C4, C5	470 nF	100 V	0603		885012207130
T1	350 µH	1500 V	1812		74930030
L1	10 µH	80 V	9.2 x 6 x 5 mm	1600 mA	744226
L2	100 µH	80 V	7332	300 mA	744878101
R1	100 Ω		0603		

Limits

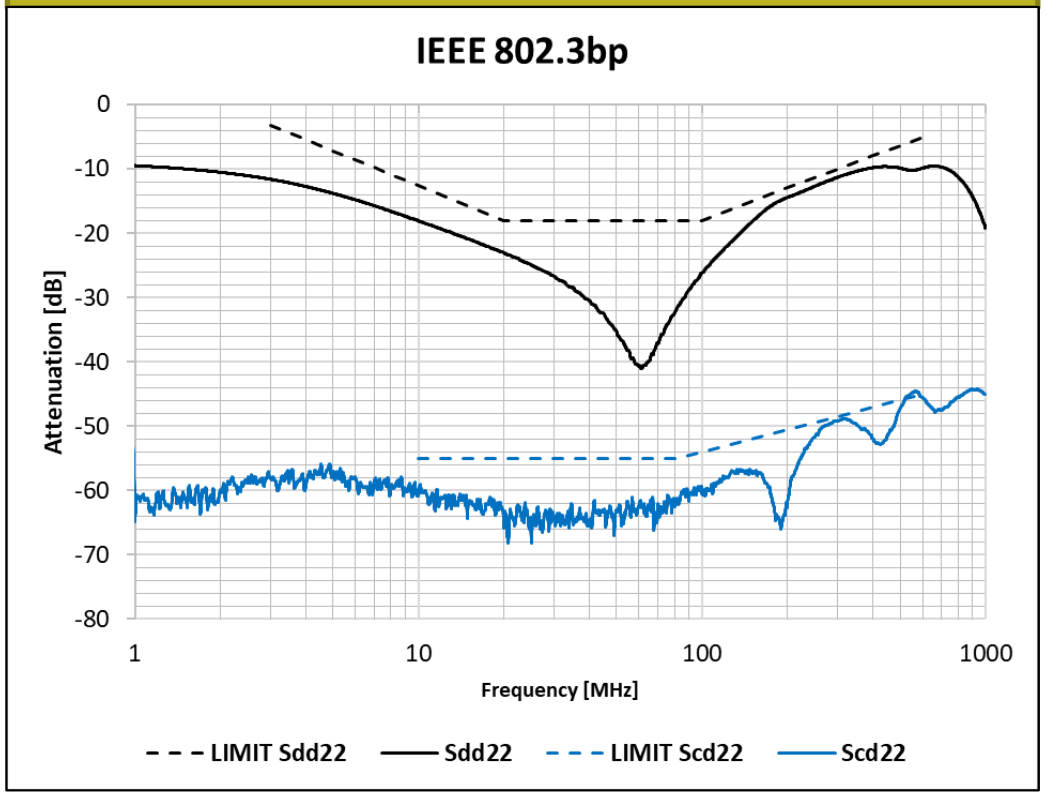
1000BASE-T1L & PoDL

Circuit



Name	Value	Isolation	Size	Current Rating	Article number
C1	100 nF	50 V	0402		885012205086
C2	1 nF	2 kV	1206		885342208024
C4, C5	470 nF	100 V	0603		885012207130
T1	110 µH	1500 V	1812		74930120
L1	304 nH	50 V (DC) 125 V (AC)	1206	310 mA	744232261
L2	2.2 µH	80 V (DC)	8018	1340 mA	74489430022
R1	100 Ω		0603		

Limits



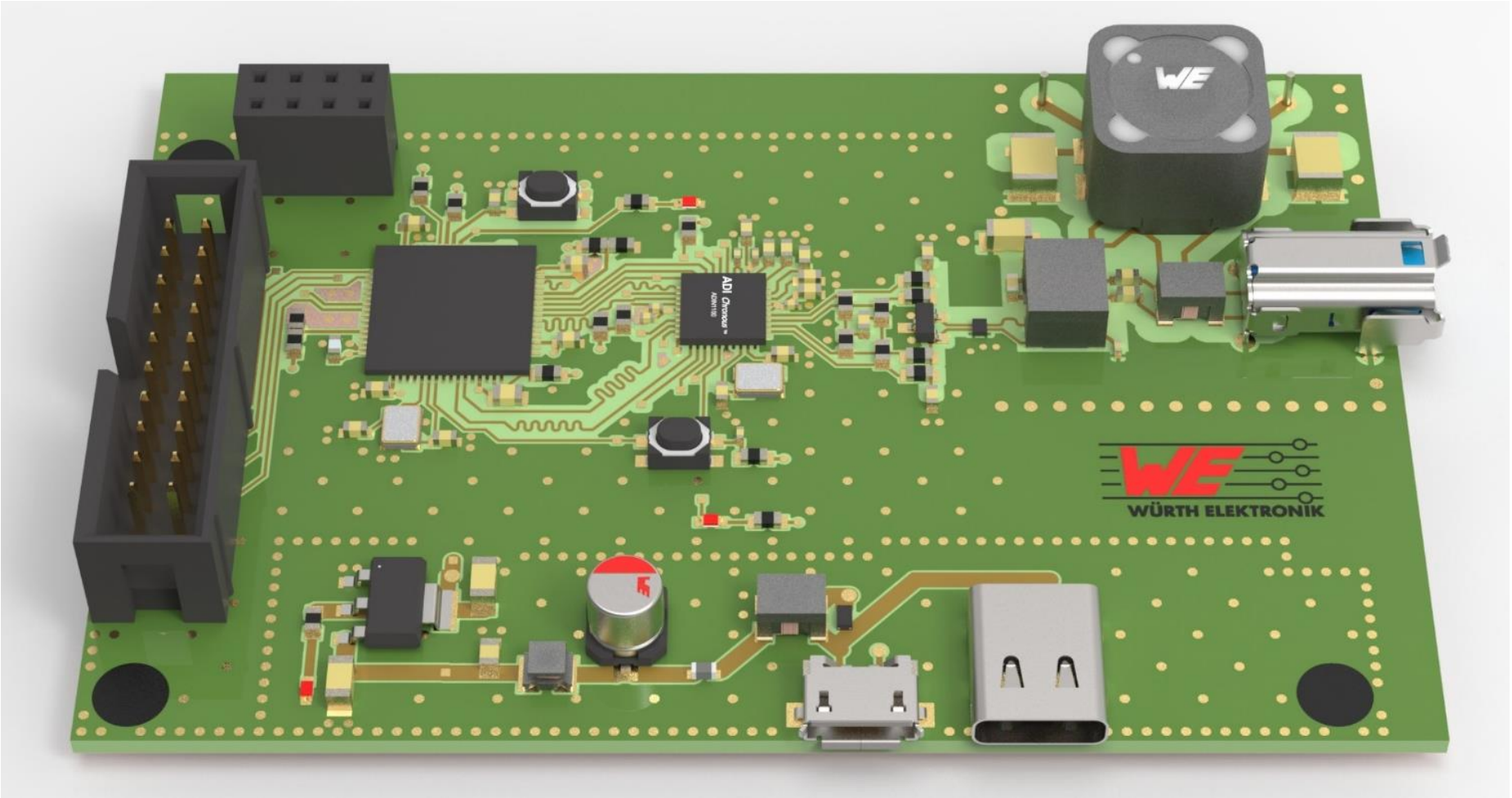
Power classes→ up to 1,6A is possible

Class	0	1	2	3	4	5	6	7	8	9
U	5,5…18V	5,5…18V	14…18V	14…18V	12…36V	12…36V	26…36V	26…36V	48…60V	48…60V
I	**0,1A**	**0,22A**	**0,25A**	**0,47A**	**0,1A**	**0,34A**	**0,21A**	**0,46A**	**0,73A**	**1,3A**
P	0,5W	1W	3W	5W	1W	3W	5W	10W	30W	50W

Class	10	11	12	13	14	15
U	20…30V	20…30V	20…30V	50…58V	50…58V	50…58V
I	**0,092A**	**0,24A**	**0,632A**	**0,231A**	**0,6A**	**1,579A**
P	1,32W	3,2W	8,4W	7,7W	20W	52W

PoDL board

WE Ref design



Application Note

Single Pair Ethernet for Industrial Applications

mode choke 744272222 not only provides common mode suppression but also has a positive influence on return loss and mode conversion loss. Due to the low cut-off frequency, the dimensions (10 mm x 8.7 mm) and inductance value (2 x 2200 µH) of the common mode choke are correspondingly large. The common mode rejection for 74472222 is illustrated in figure 15.

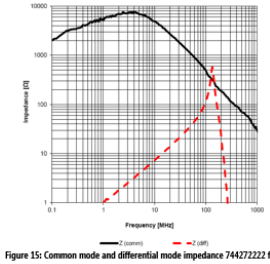


Figure 15: Common mode and differential mode impedance 744272222 for 10BASE-T1

A more compact and electrically at least equivalent solution is the design with a transformer. Figure 16 shows the transformer design for 10BASE-T1. In contrast to chapter 4, no common mode choke is required for the 10 Mbit/s design. The reason is the good interference suppression of the transformer at low frequencies. Another difference is the capacitor C_3 on the two center pins which extends the transformer bandwidth up to 35 kHz and thus helps to improve the return loss in low frequencies.

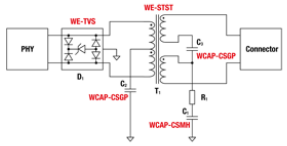


Figure 16: 10BASE-T1 transformer design

Since it is not possible to split the center pin on all transformer types, two capacitors can be used on the outer transformer pins as an alternative to C3 between the transformer center pins. This design enlarges the circuit minimally, but has the advantage, that the similar circuit can be used for Power over Dataline (PoDL) applications. For PoDL the voltage on both capacitors drops only half, thus preventing DC saturation. If only data is transmitted, capacitors with an isolation voltage of 25 V are sufficient, whereas with PoDL an isolation voltage of 100 V is necessary.

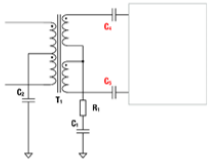


Figure 17: Capacitors C_4 and C_5 on the outer transformer pins as alternative to C_3

In addition to the insulation voltage of the capacitors, their capacitance is important for both circuit diagrams. Simulations and measurements result in a minimum value of 100 nF to meet the limits of IEEE802.3cg. However, the section "146.5.4.2 Transmitter output droop" mentions a maximum voltage drop of 10% between 133.3 ns and 800 ns for a test signal of the PHY chip. To meet this requirement, two changes can be made. Either the inductance of the transmitter is increased, which also goes along with the increase in size or capacitors with larger capacitance values are used. The second possibility is more space-saving, cheaper and easier to implement. In this case 470 nF capacitors are used to achieve the best compromise between the droop and return loss requirements. As figure 18 and the following equation shows, this circuit design achieves a voltage drop of about 8.3% and is therefore within the standard.

Application Note

Single Pair Ethernet for Industrial Applications

frequency ranges. Due to the lower cut-off frequency at 100BASE-T1 of 1 MHz, the impedance of the choke must be high in low frequencies and, if possible, also cover higher frequencies up to 200 MHz. The number of windings and core size is correspondingly larger.

The GND termination typically consists of three resistors, where the first two 1 kΩ resistors are responsible for signal termination, and the 100 kΩ resistor together with the capacitor decouples common-mode components in the signal.

The coupling capacitors have capacitances of typically 100 nF and come with 50 V isolation voltage. They are comparatively small and cost-effective, which is why they are used in automotive applications with low-voltage environments and a maximum cable length of 15 m.

3.2 Isolation requirements

Outside the automobile, the IEEE 802.3 standard for signaling systems stipulates the insulation requirement according to IEC 62368-1, which corresponds to 1500 V AC for 60 seconds. A DC voltage of 2250 V DC for 60 seconds or certain test voltage pulses are also permitted. These high insulation voltages cannot be maintained by the 50 V capacitors, so alternative solutions must be sought. The following chapter therefore describes a solution with transformer. Detailed measurements and a comparison with capacitors with 2000 V insulation voltage follows in the chapter Performance Comparison SPE automotive vs. SPE industrial Solutions

At 1 – 66 MHz, the frequency range for SPE 100BASE-T1 is in the Gigabit Multipair Ethernet (1 - 62.5 MHz) range. It is therefore obvious to design a circuit for SPE that is based on the circuit diagram of Gigabit Ethernet, see figure 8.

The central element of the circuit is a signal transformer, which provides the galvanic isolation and ideally does not influence the data signals. The transformer is terminated at its center pins with capacitors to GND. A common mode choke is used for common mode interference suppression. To ensure protection against ESD pulses, a TVS diode is placed between the common mode choke and the PHY chip. ESD suppression is even better if the TVS diode is located between the connector and the transformer. However, in order not to cause a short circuit between

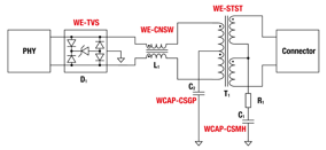


Figure 8: SPE schematic with a transformer solution

The following chapter describes the individual components of the circuit in more detail.

3.3 Galvanic isolation with a transformer

For SPE a signal transmitter of the WE-STST series is selected. Its compact design compared to conventionally manufactured LAN transformers, together with high inductance of 350 µH, offers good signal characteristics even at lower frequencies. In addition, it is SMT mountable and is manufactured 100 % automatically.

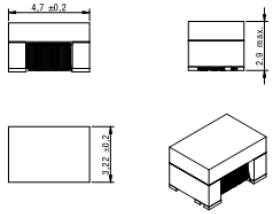


Figure 9: WE-STST shapes and dimensions

The transformer consists of a core of MgZn, which is wound bifilarly from two sides, i.e. windings of primary and secondary side are on top of each other for signal coupling. Insulation is provided by a plastic sheathing of the wires, both on the primary and secondary side. Due to the direct coupling and the transmission ratio of 1:1, differential signals are transmitted. Direct voltage components are blocked.

Besides the galvanic isolation, a signal transformer needs to transfer data in a determined frequency range of 1 – 66 MHz for 100BASE-T1 Single Pair Ethernet. For

www.we-online.com/ANP085