EMV Expertentreff SEW / Würth / ADI

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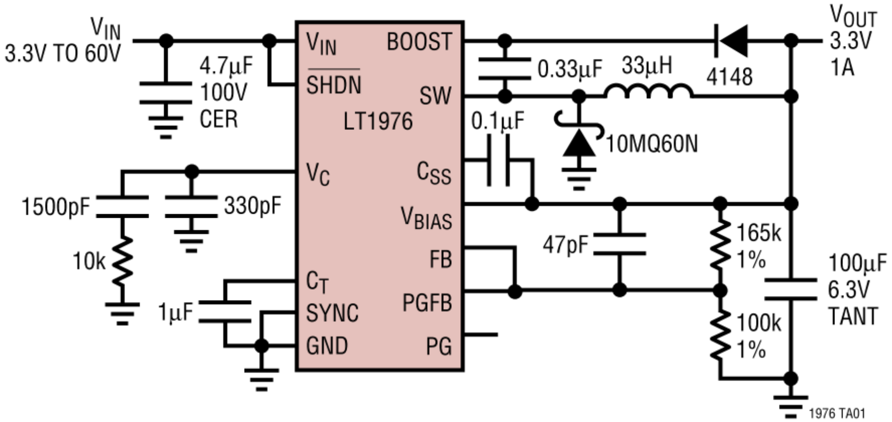
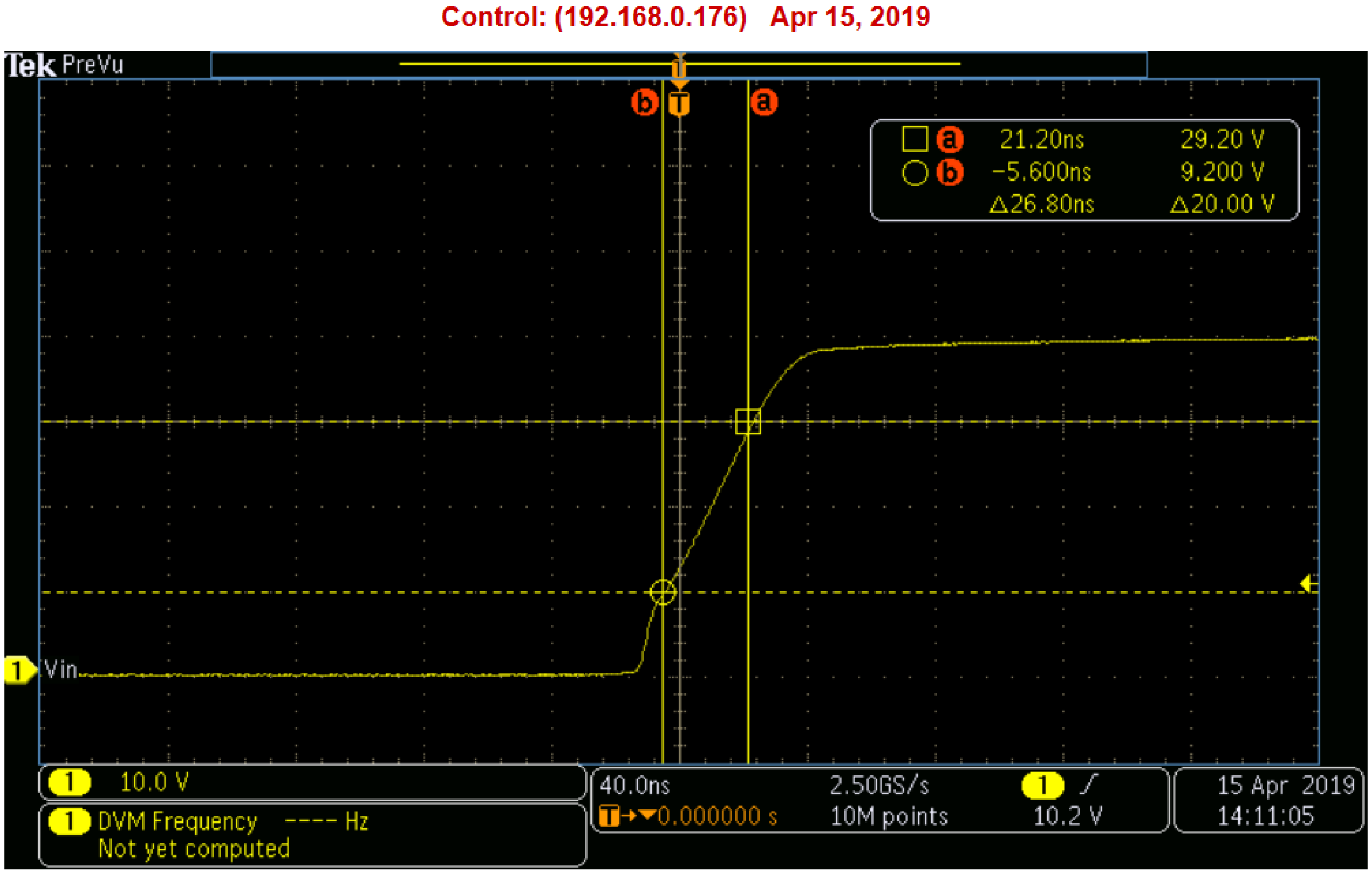
PCB Layout Considerations

Frequency Contents In Switch Mode Power Supplies

- State of the art 2003: LT1976
  - 60V/1.5A step-down
  - Diode rectified
  - 200kHz switching frequency
  - Measurement of SW node
    - Vin=40V
    - Iout=1A
    - dV/dt=0.75V/ns

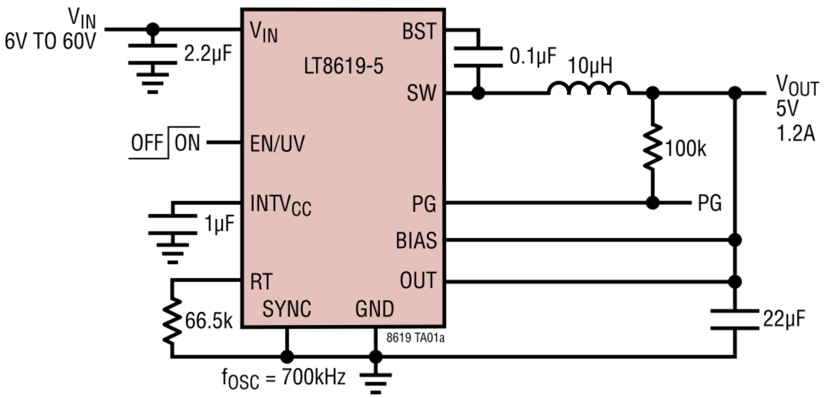


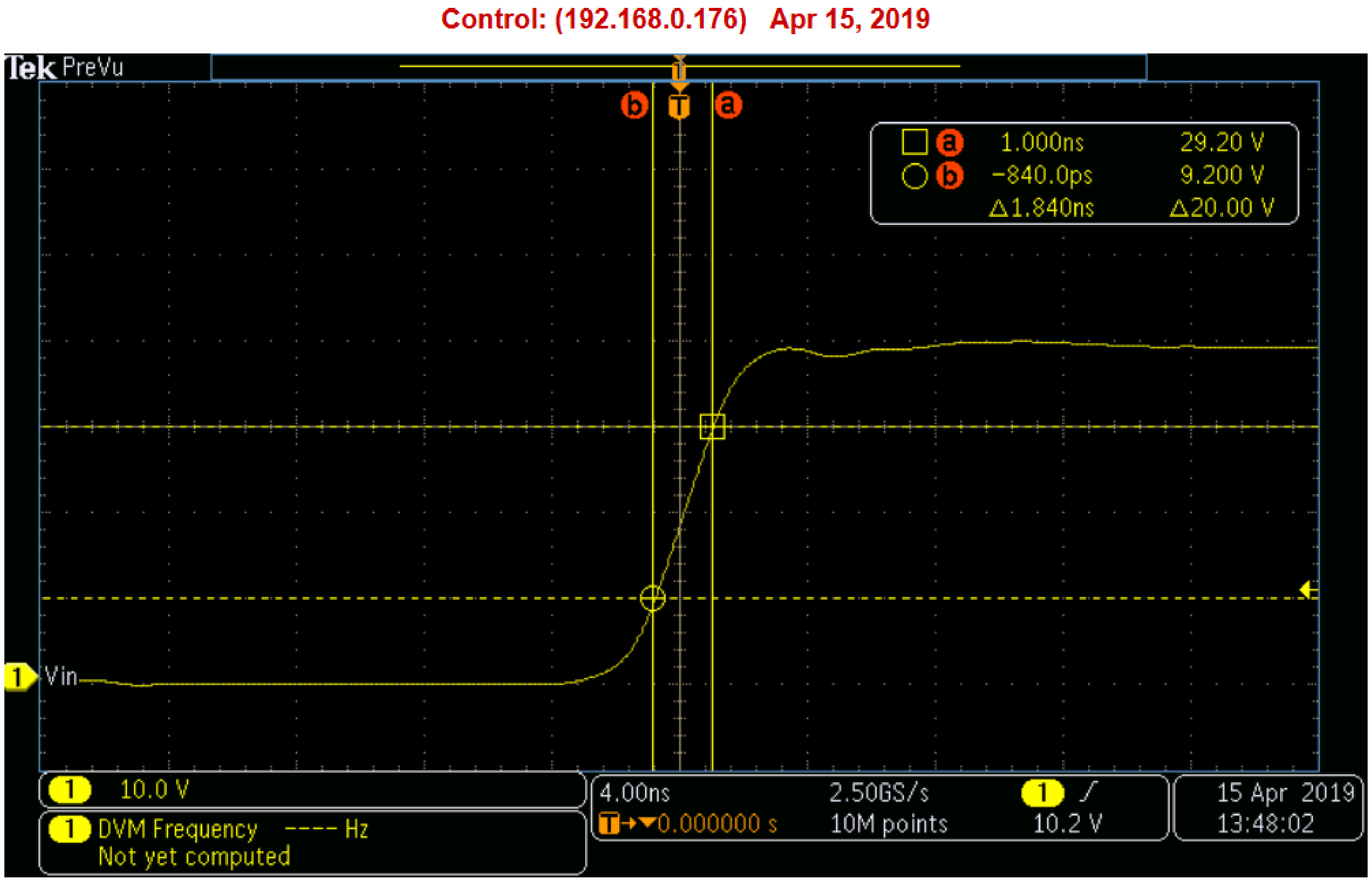


Frequency Contents In Switch Mode Power Supplies

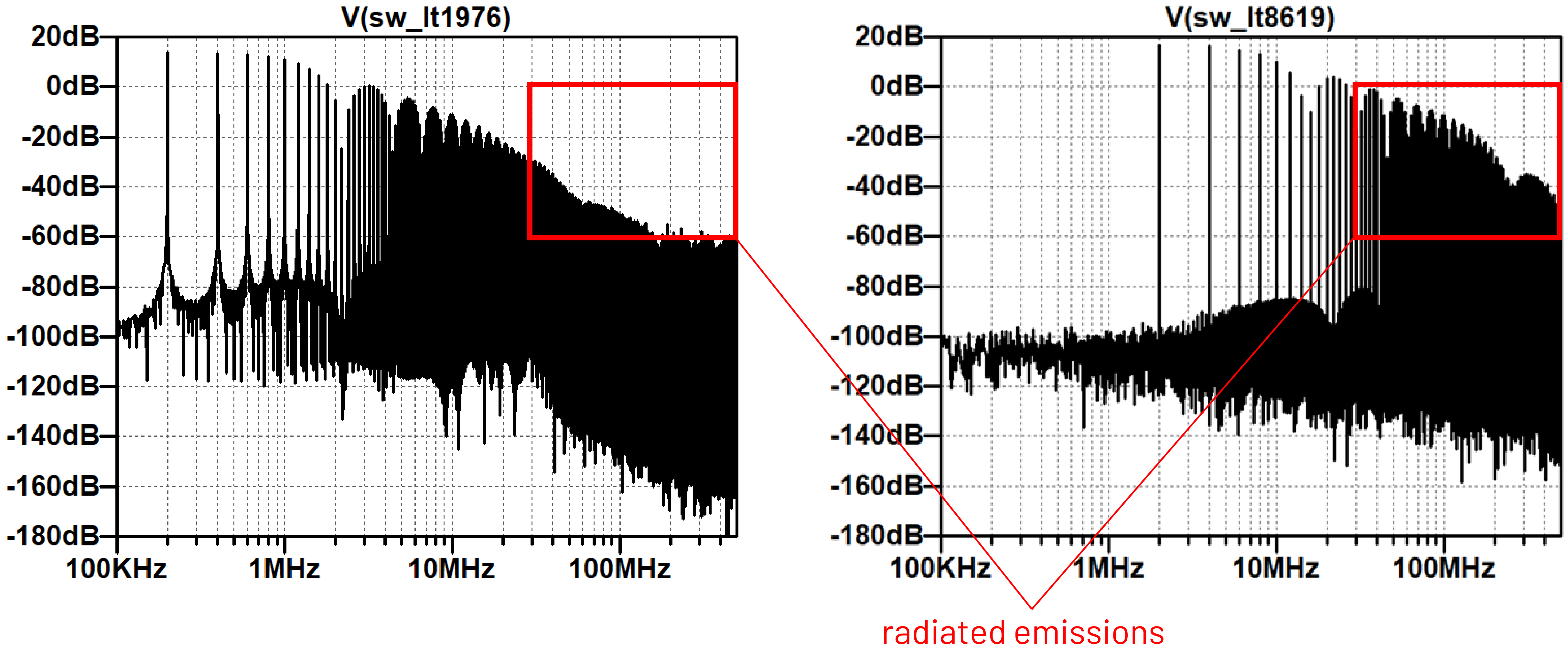
- State of the art 2019: LT8619
  - 60V/1.2A step-down
  - Synchronous rectification
  - 2MHz switching frequency
  - Measurement of SW node
    - Vin=40V
    - Iout=1A
    - dV/dt=10.9V/ns

5V, 1.2A Step-Down Converter





Frequency Contents In Switch Mode Power Supplies

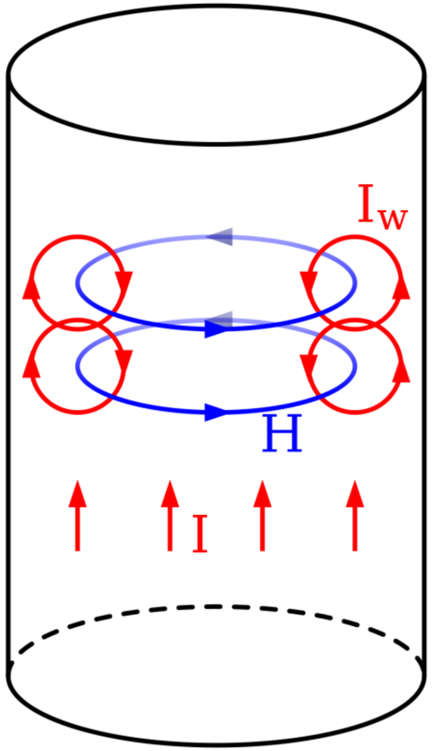


ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

Physical Background

Skin Effect – Physical Background

- Alternating current I creates an alternating magnetic field H.
- These alternating H field circles induce eddy currents I_W
- The eddy currents rotate in the direction that creates an H field that opposes the original H field that caused them (use right hand rule)
- I_W is higher in higher conductivity material
- Eddy currents I_W have no return path outside of the conductor
- AC current density is highest under the surface of the conductor



$$\delta = \sqrt{\frac{\rho}{\pi f \mu_r \mu_0}}$$

ρ = resistivity of conductor

δ = skin depth

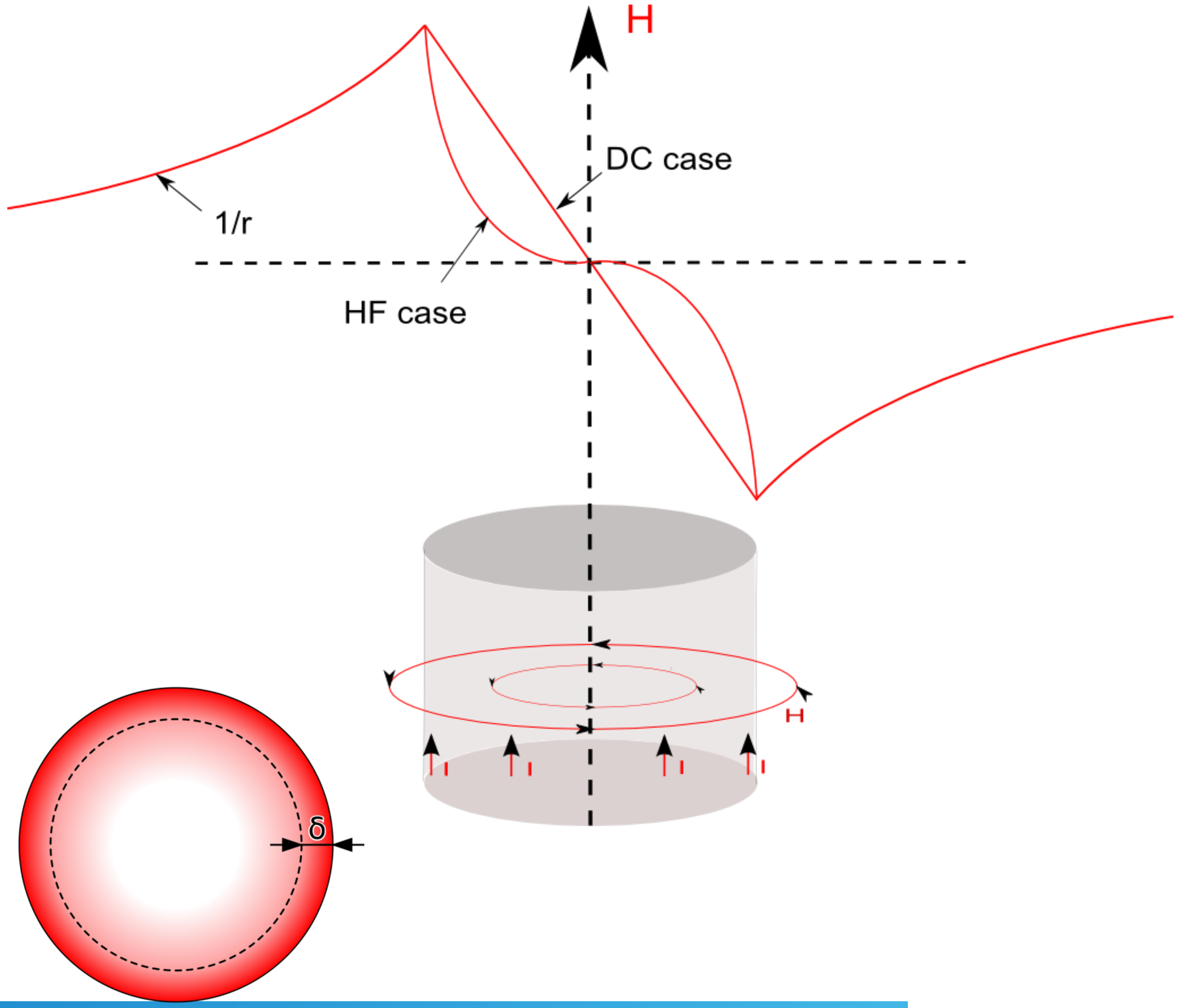
f = frequency

μ_r = relative permeability

μ_0 = permeability constant

Skin Effect

- AC current density is forced to the outside
- For most calculations the simplification can be used that the current flows uniformly only in the area with a thickness of δ
- The current density at the depth δ is 1/e (~37%)
- Neither AC magnetic fields nor AC electric currents can flow deep inside a good conductor. The induced magnetic field will force the current to the outside



Skin Effect

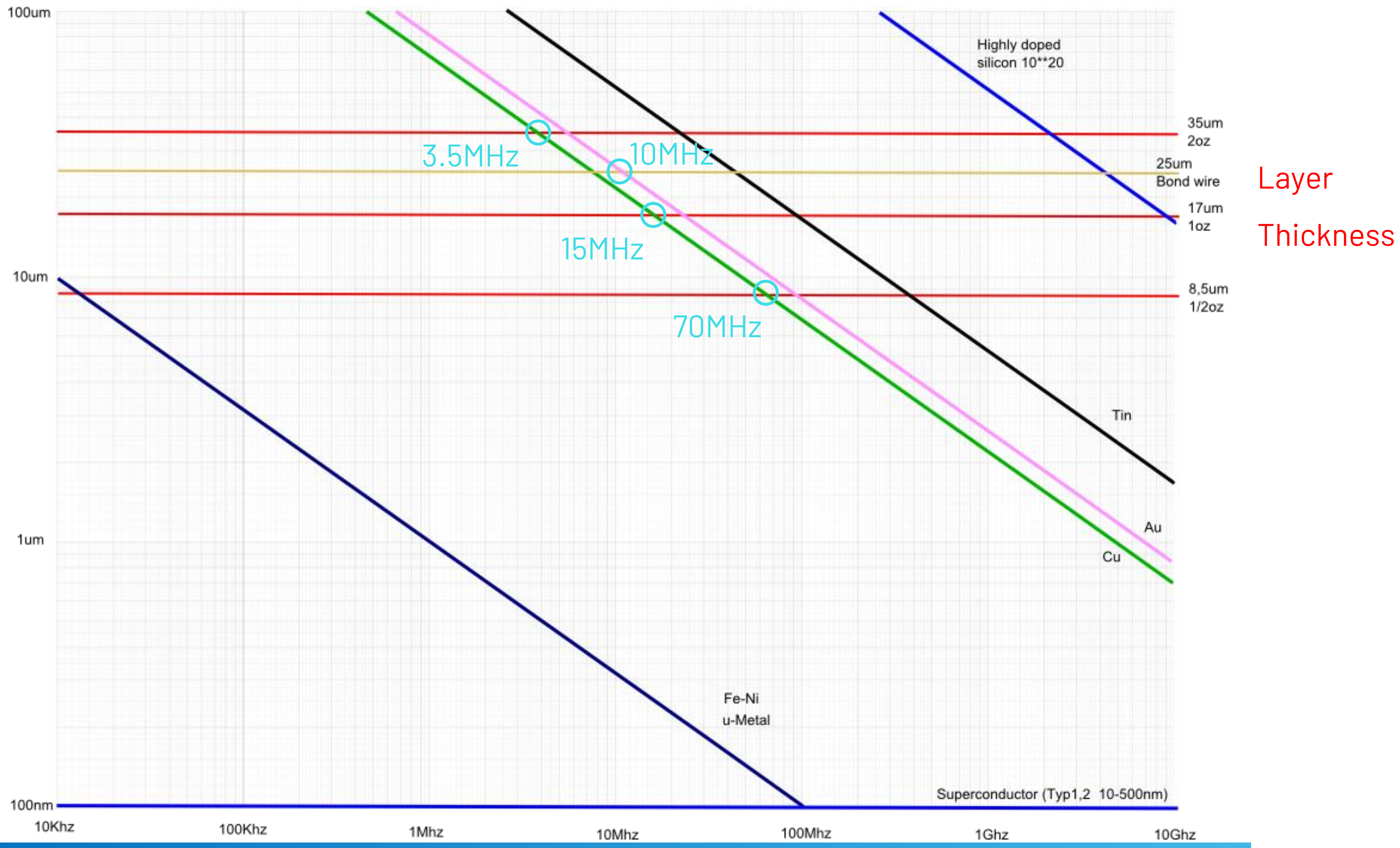
- Lower resistance materials have lower skin depths

	Resistivity (Ωm)	Skin Depth @ 1 MHz (µm)	Skin Depth @ 100 MHz (µm)
Copper	1.68e-8	66	6.6
Tin	1.09e-7	166	16.6
10^{20} cm^{-3} heavily doped silicon	1e-5	1600	160

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_r \mu_0}}$$

Skin Effect

- Skin depth vs. frequency for various materials



Conductor Inductance And Skin Effect

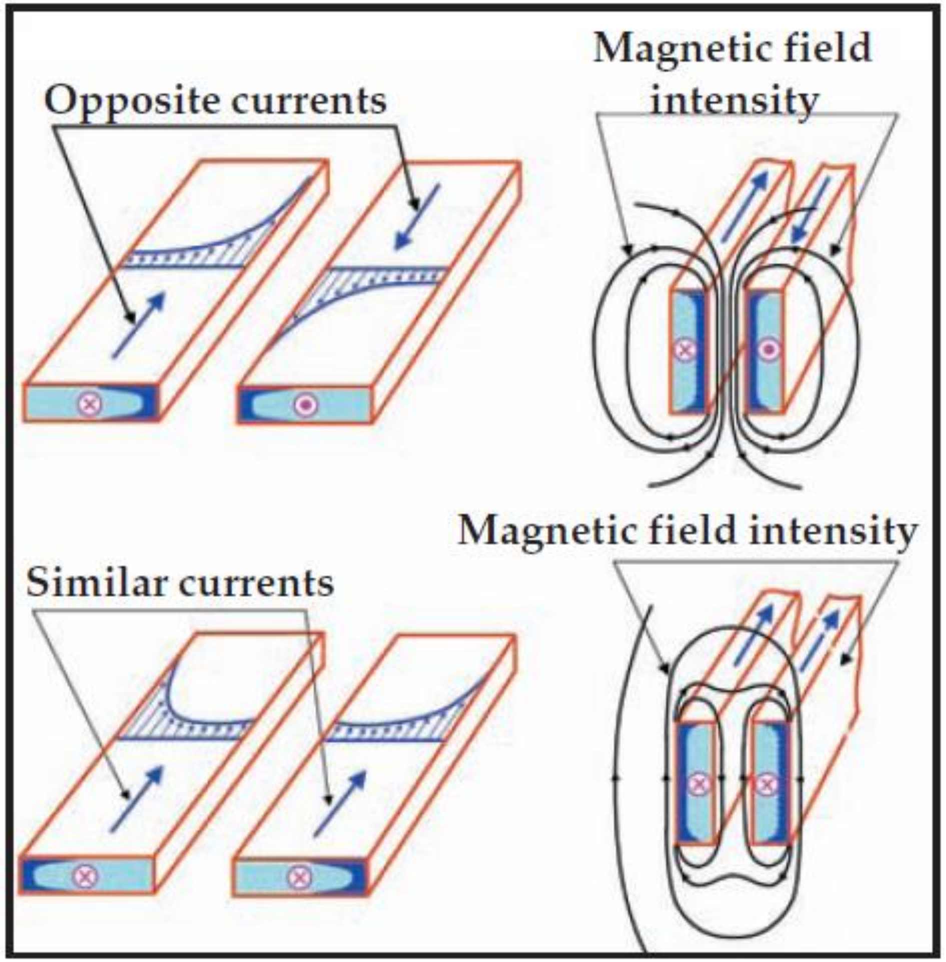
- Inductance per unit length of a straight wire consists of internal and external components
  - Internal inductance: $L_{int} = \frac{1}{2} \cdot 10^{-7} \frac{\mathrm{H}}{\mathrm{m}}$
    - Assumptions:
      - Uniform current density in conductor, only true for DC currents
      - μ_r=1 for non-ferromagnetic materials
  - Total inductance: $L = 2 \cdot 10^{-7} \left[\ln\left(\frac{4l}{d}\right) - 1 + \frac{\mu_r}{4} + \frac{d}{2l}\right] l$
    - l: Length of conductor
    - d: Diameter of conductor
    - μ_r: Relative permeability
  - Skin effect lowers internal magnetic flux
    - Internal inductance decreases at higher frequencies
  - Total inductance for very high frequency: $L = 2 \cdot 10^{-7} \left[\ln\left(\frac{4l}{d}\right) - 1 + \frac{d}{2l}\right] l$
    - Skin depth is nearly zero, therefore no internal magnetic field exists

Skin Effect

- Conclusions:
  - AC current mainly flows within the skin depth at the outside of the conductor
  - At δ, the current density is attenuated to about 37% of the surface current density
  - The skin effect can be neglected if the dimension of the conductor cross section is smaller than the skin depth
  - The "skin frequency" is the frequency at which the skin effect becomes significant
    - With 35µm (2 oz) copper the skin effect becomes apparent at about 3.5 MHz
  - Skin effect decreases the effective inductance
  - Smaller diameter wire or vias have higher inductance than thicker ones
    - This is also true for non-circular wire cross sections: Wider traces have lower inductance than narrower ones

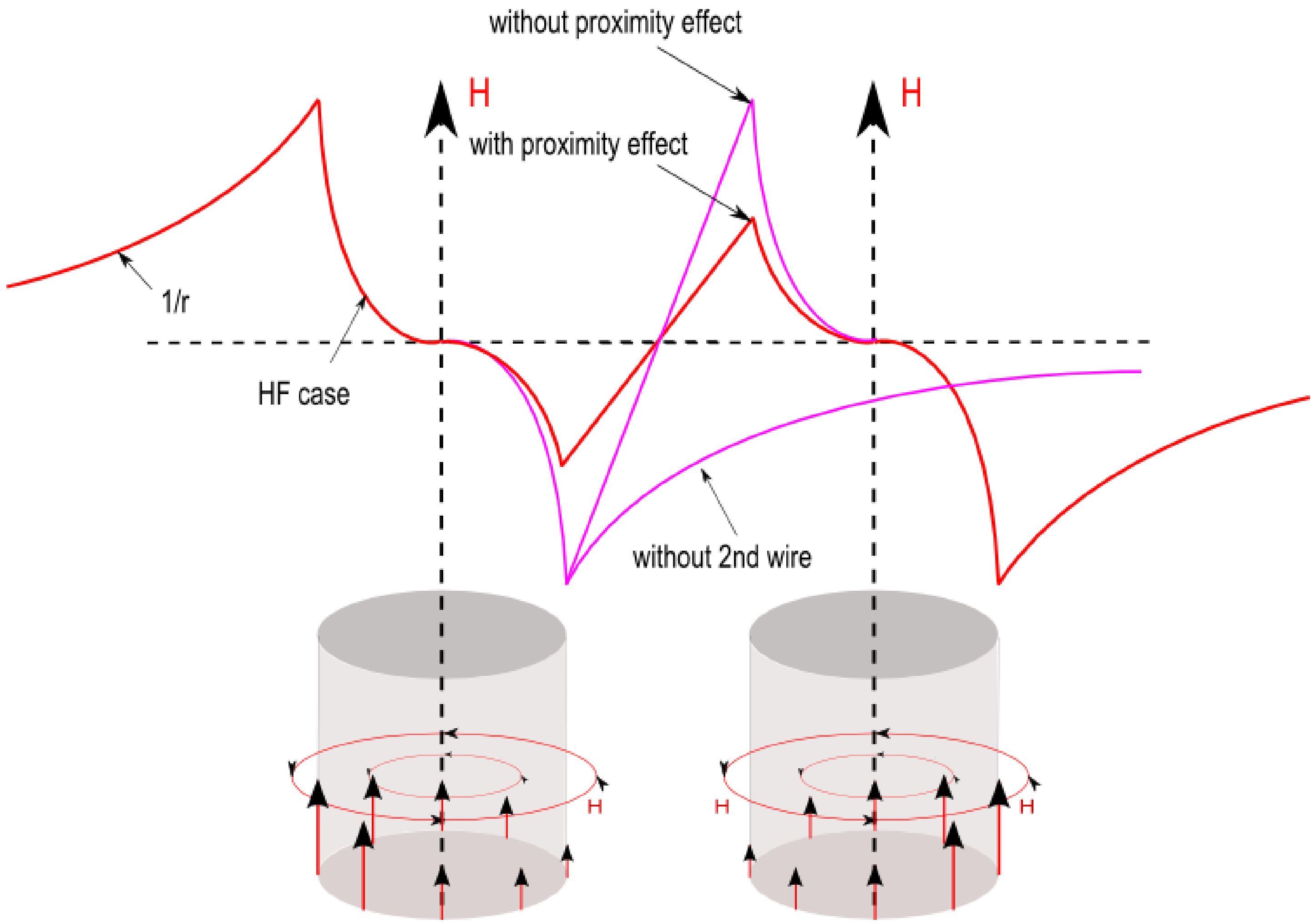
Proximity Effect

- Currents flowing in opposite direction attract each other
  - The same induction forces responsible for the skin effect work here in the opposite way, since the current has opposite direction
- Currents flowing in the same direction force themself apart
  - So they do inside the same conductor due to the skin effect



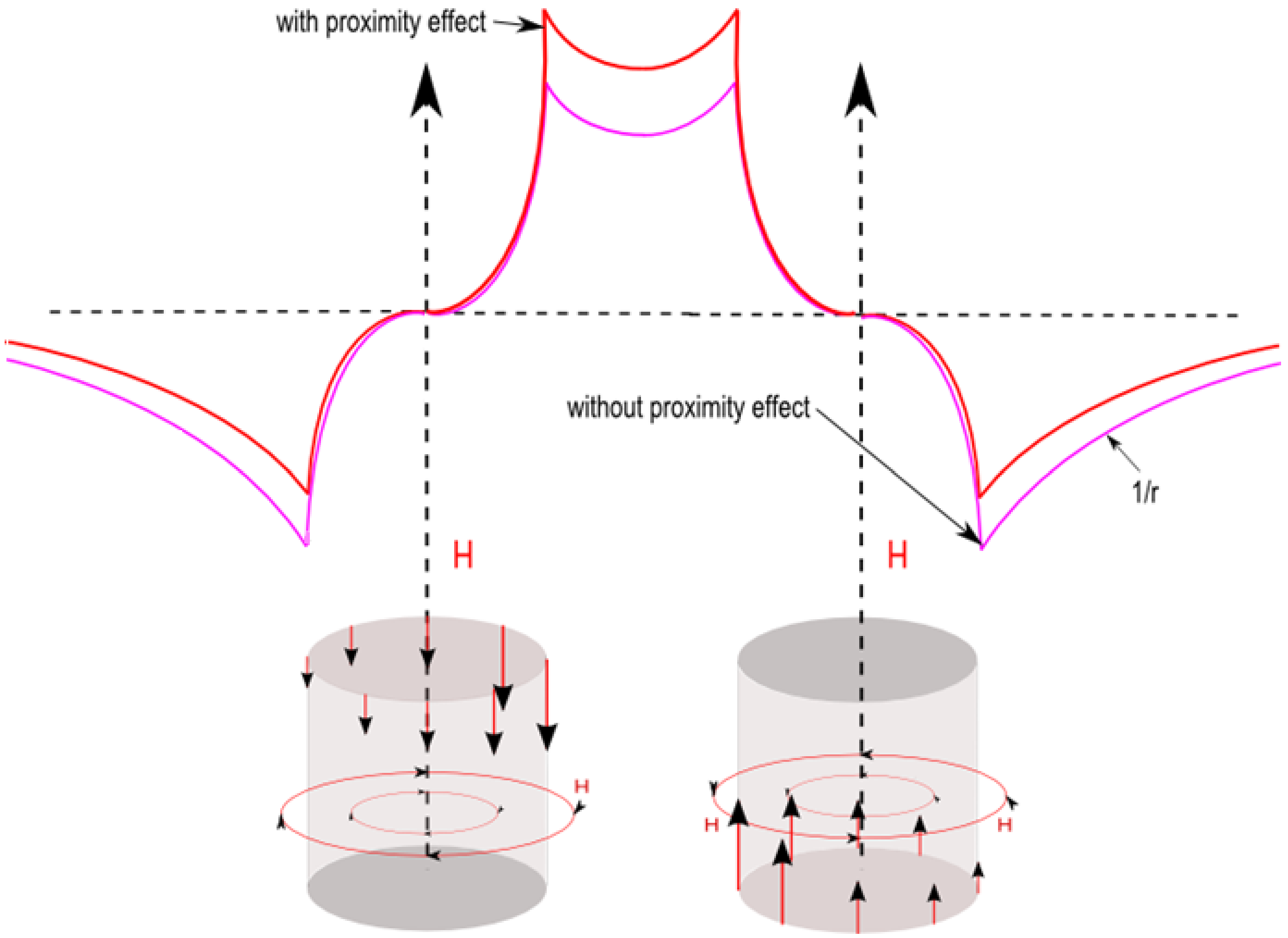
Proximity Effect

- Two wires same current & direction (typical for coils)



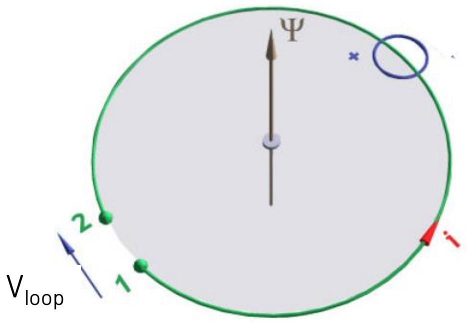
Proximity Effect

- Two wires opposite current direction (typical of PCBs)

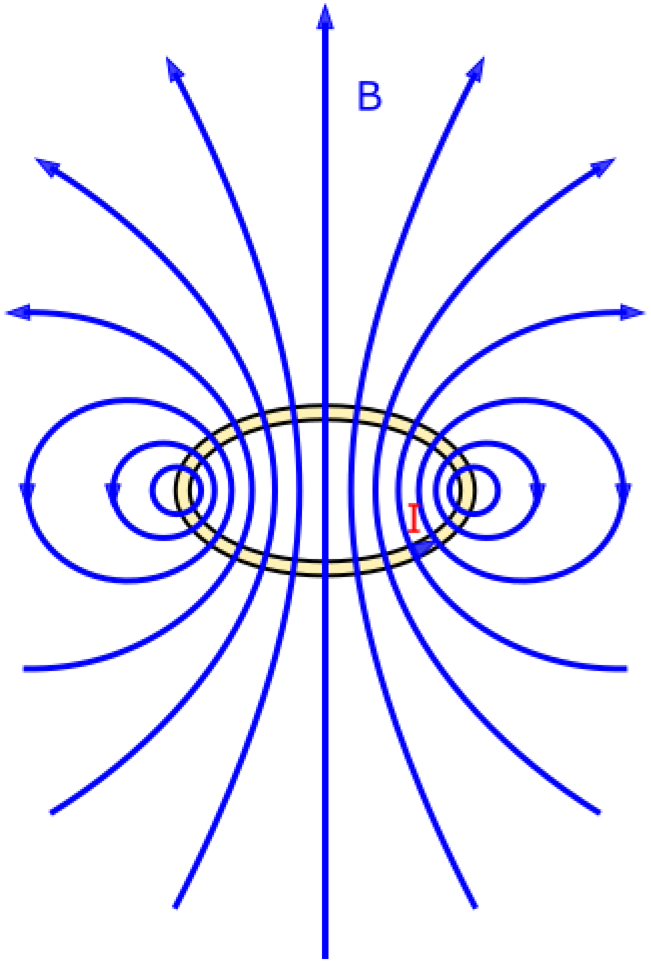


Loop Inductance

- Faraday's law of induction
  - $V = \frac{d\Phi}{dt}$ with $\Phi = \int_A \vec{B} \cdot d\vec{A}$
    - F: Electric Flux perpendicular to area
    - A: Area



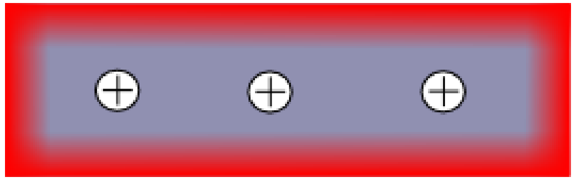
- $V = L\frac{dI}{dt}$
  - **⟹ Higher surrounded area leads to higher inductance**
  - **⟹ Keep hot loop area as small as possible**
    - Good to minimize magnetic coupling to surrounding loops, too
    - Emitted radio power is proportional to the loop area squared!



- Example: Inductance of a ring loop
  - $L_{ring} \approx \mu_0 \mu_r \frac{D}{2}\left[\ln\left(\frac{8D}{d}\right) - 2\right]$
    - D: Loop diameter, d: Wire diameter
    - ⟹ Inductance increases more than proportional with loop diameter

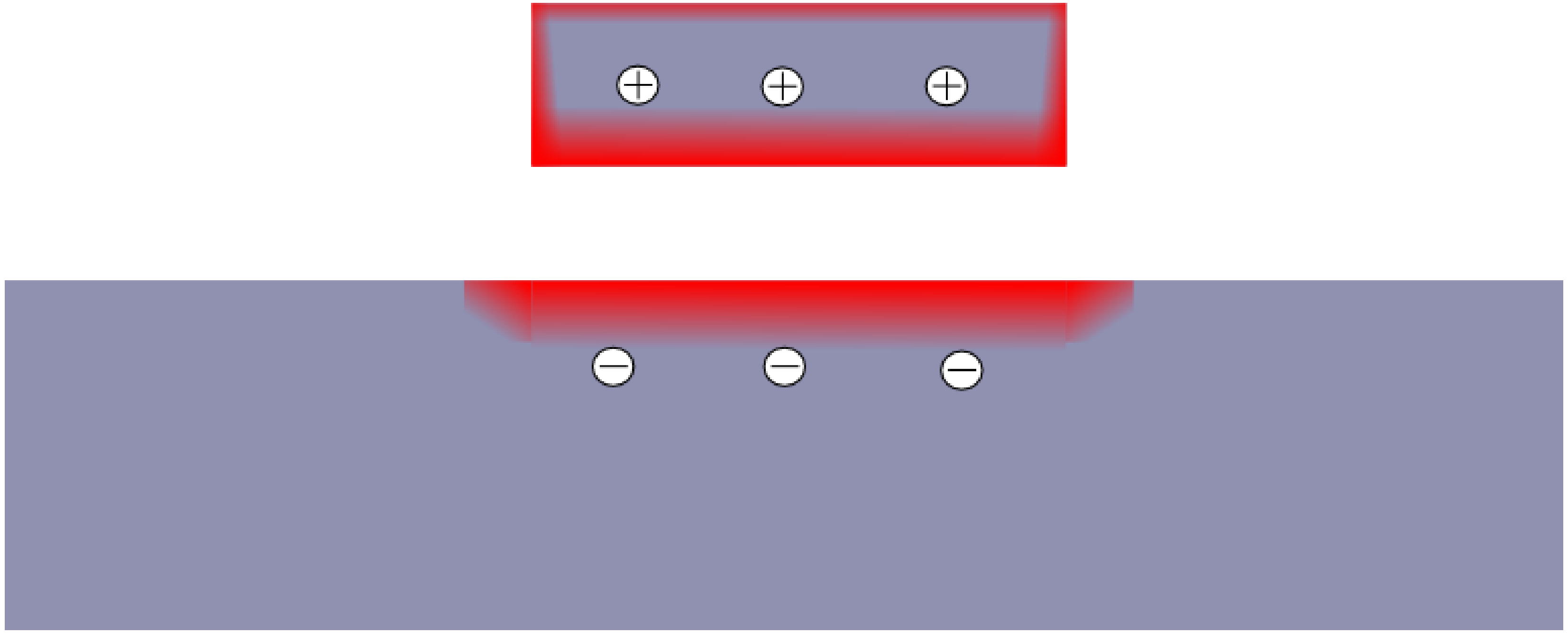
AC Current Density

- Rectangular conductor



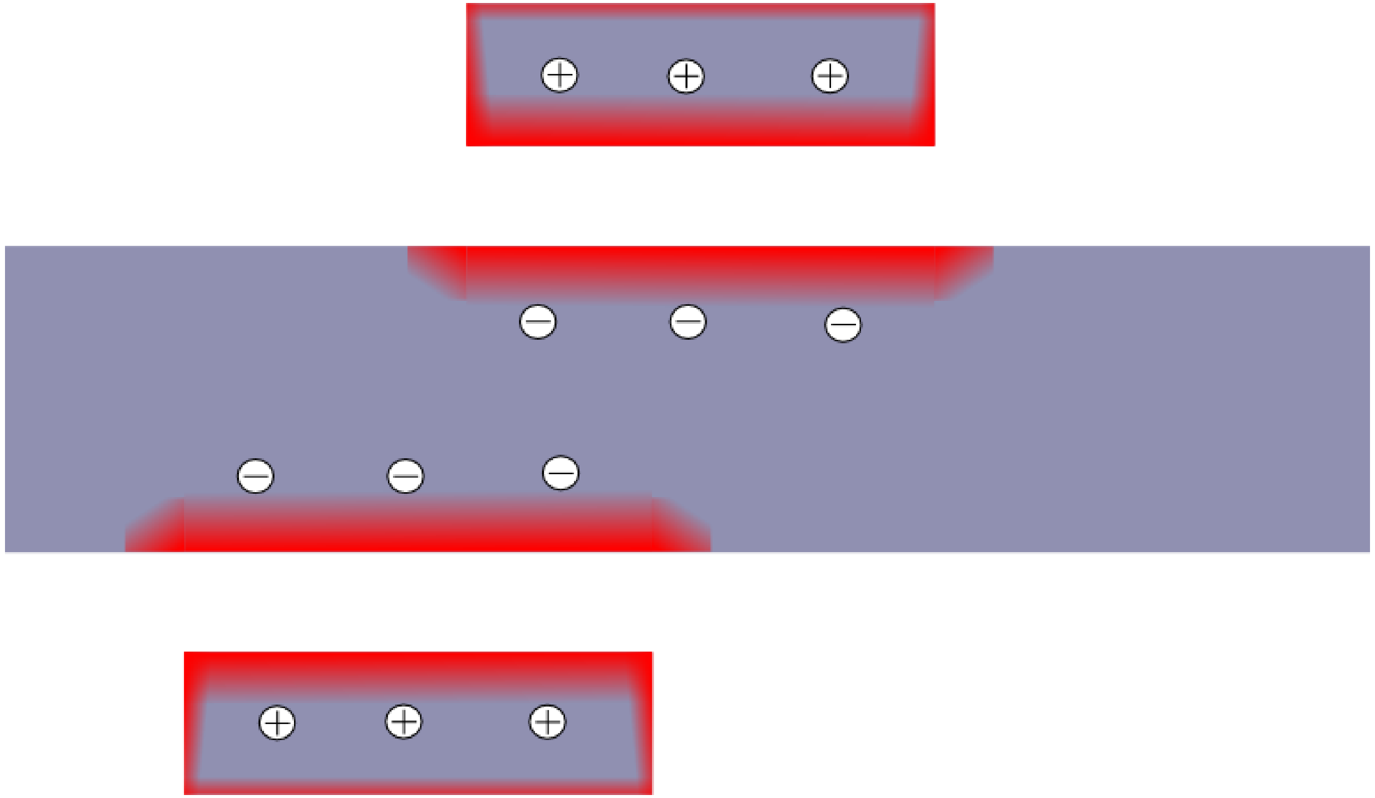
AC Current Density

- Rectangular conductor with return current in shielding plane
  - AC return current flows underneath the conductor
    - Minimum loop impedance with minimized loop area



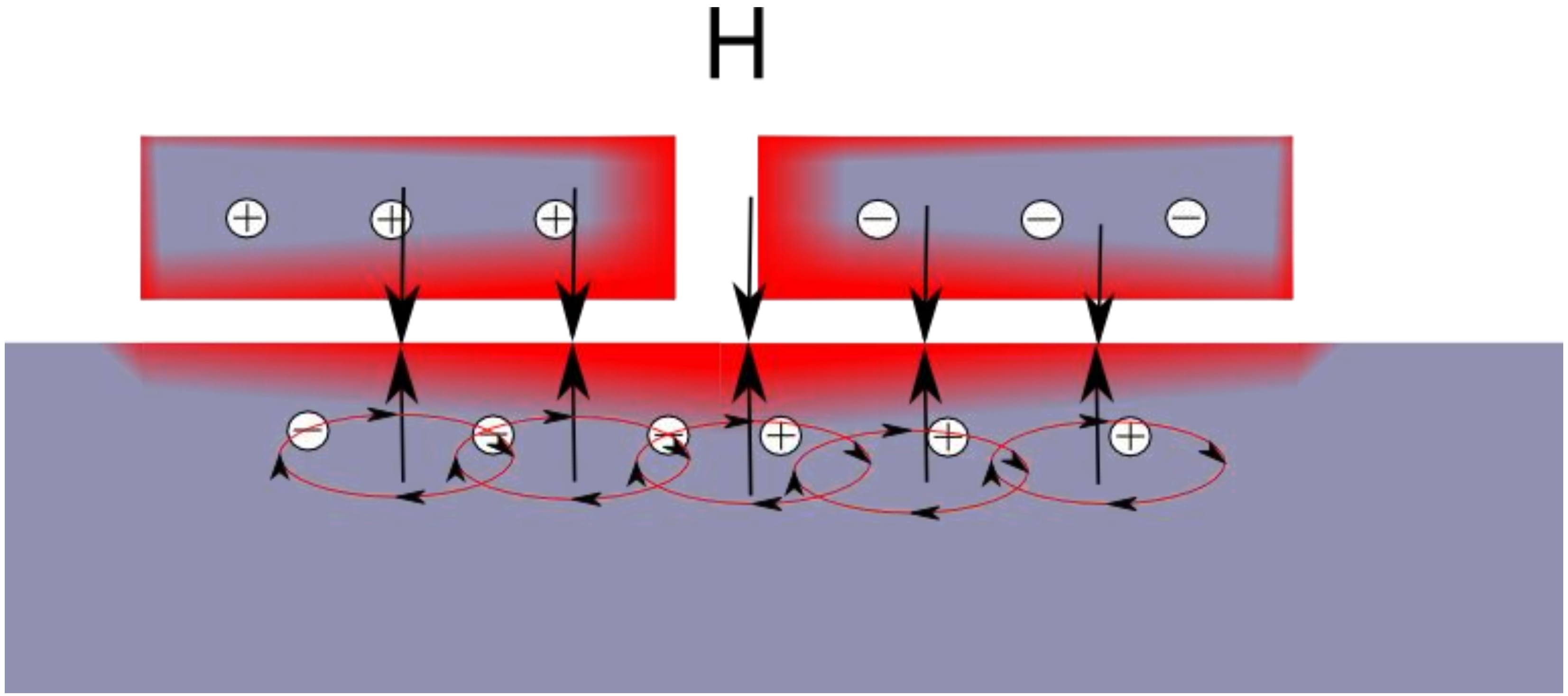
AC Current Density

- AC currents in a plane are isolated from each other for skin depths < ½ thickness
  - E.g. over 15 MHz for 35µm (2oz) copper plating



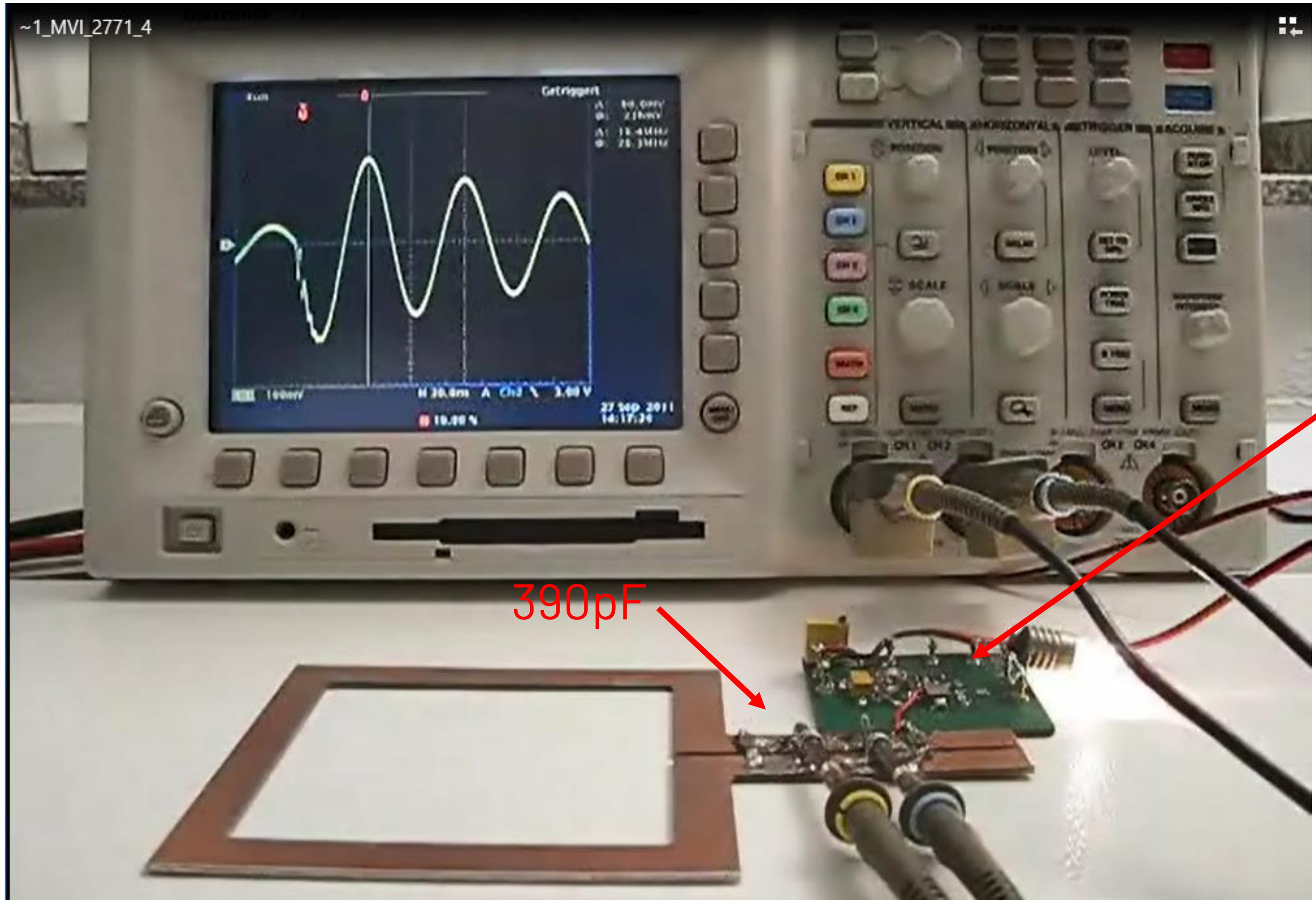
AC Current Density

- AC currents in conductors with no return path through a plane induce inverted currents in the plane
  - Eddy currents induced in the plane
  - Shielding effect due to partly cancelling magnetic fields



Lab Example: PCB Copper Loop

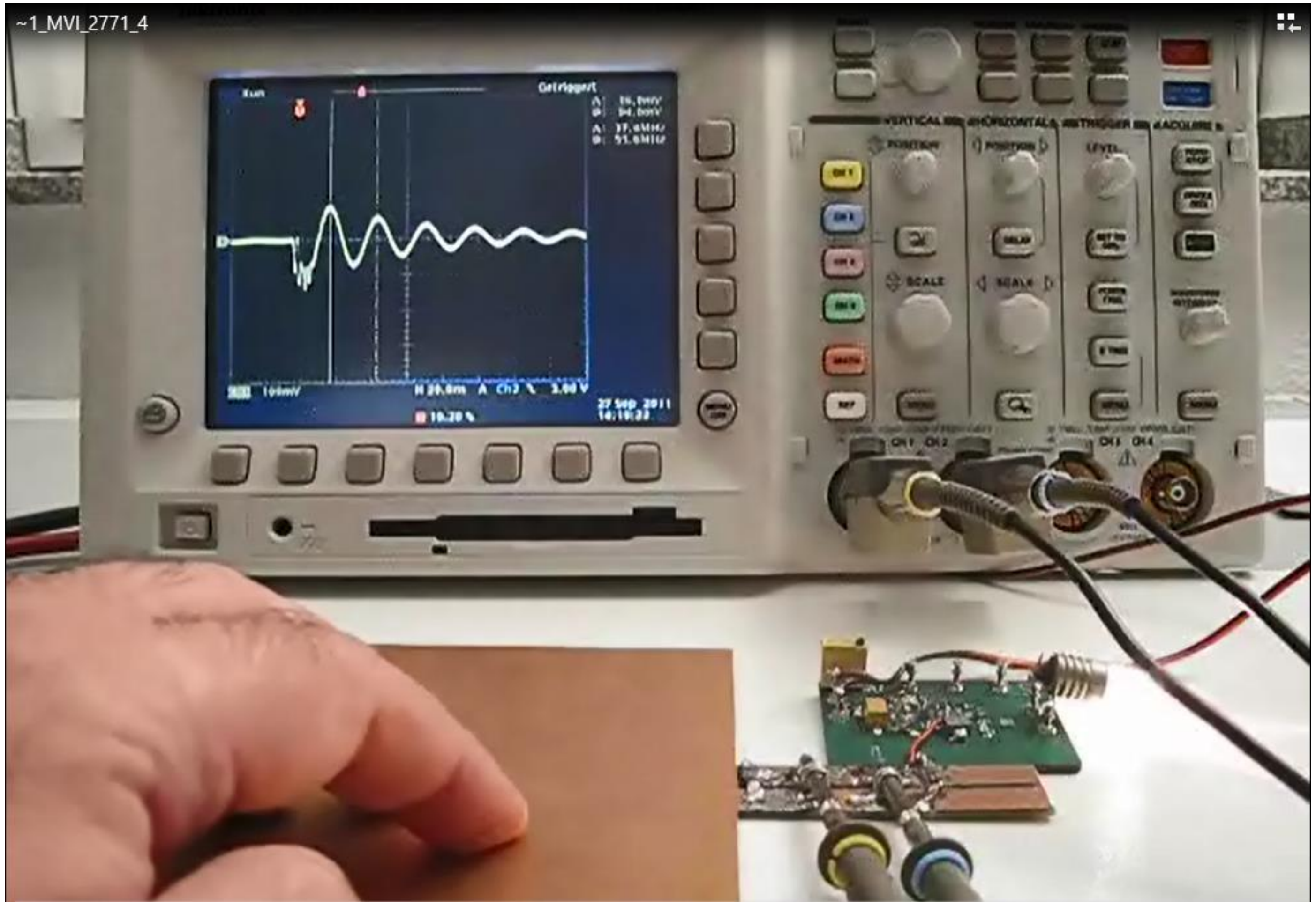
- Resonant tank circuit consisting of copper trace loop and 390pF capacitor
  - f= 18.4MHz ringing frequency
    - L_{loop}=192nH



SW node of SMPS acts as pulse generator

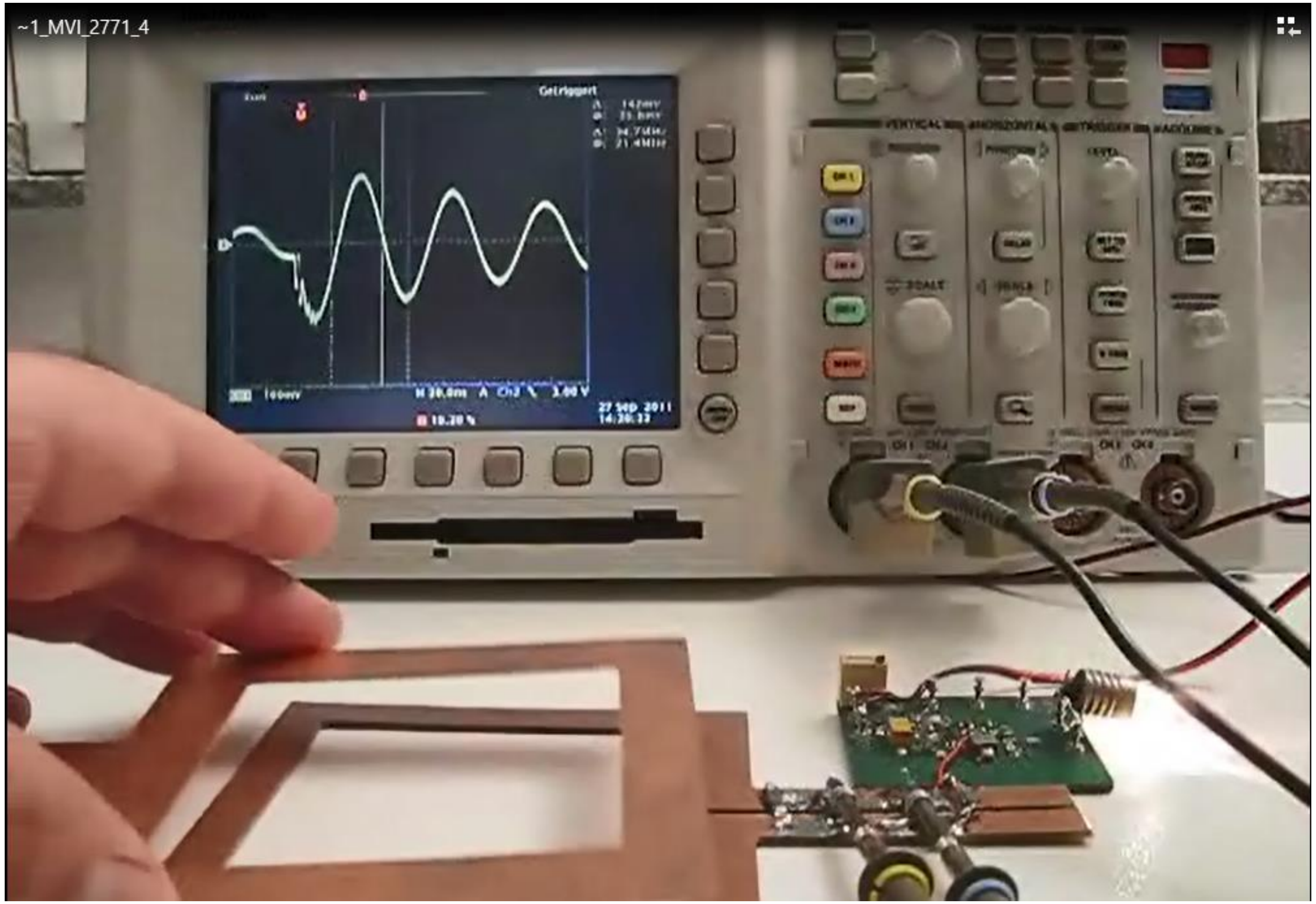
Lab Example: PCB Copper Loop

- Loop covered with one sided copper plane PCB with 1.5mm thickness
  - f=38.9MHz ringing frequency
    - L=43nH



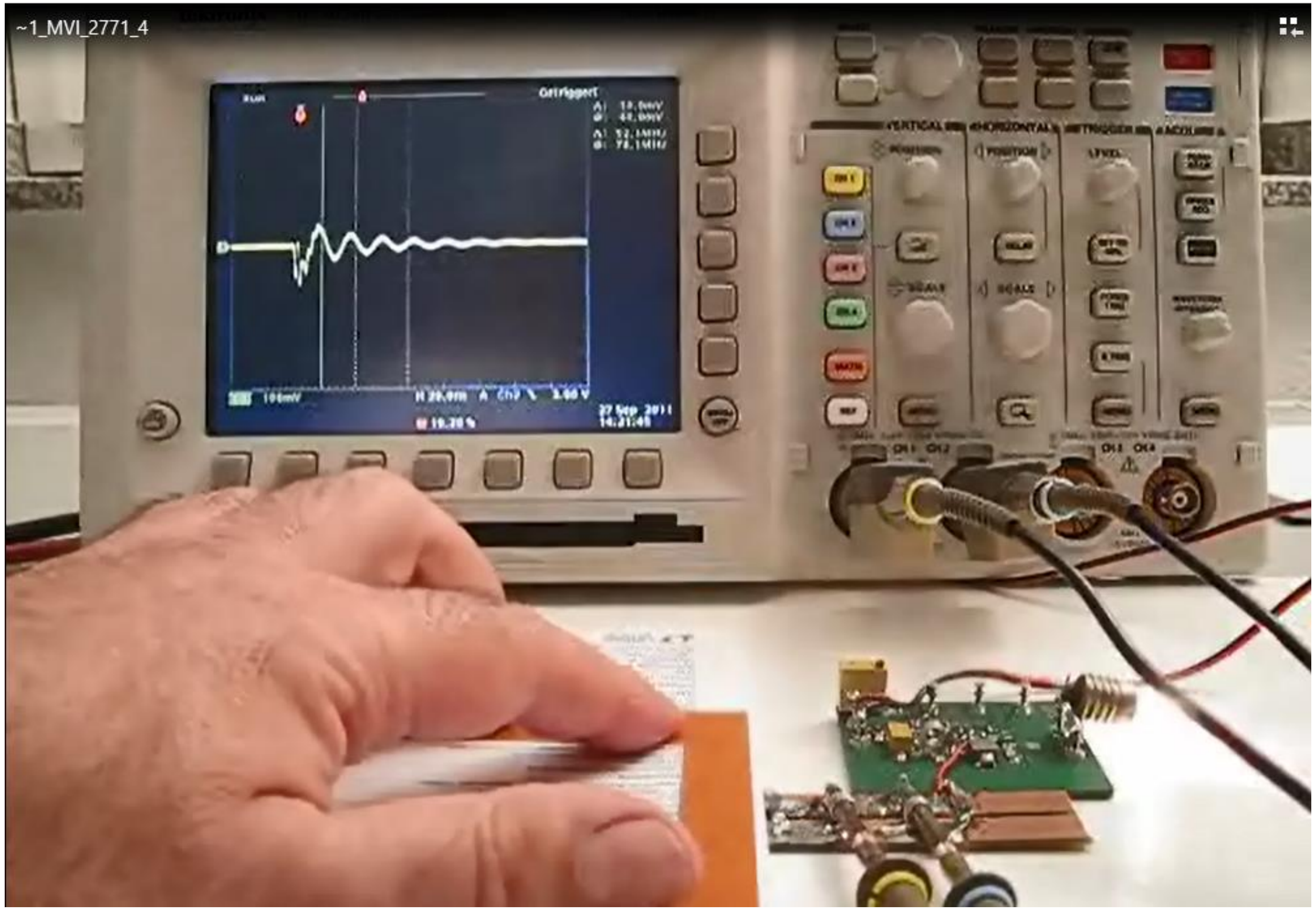
Lab Example: PCB Copper Loop

- Loop covered with a closed copper loop on FR4 of the same size with 0.5mm thickness
  - f=52.1MHz ringing frequency
    - L=24nH



Lab Example: PCB Copper Loop

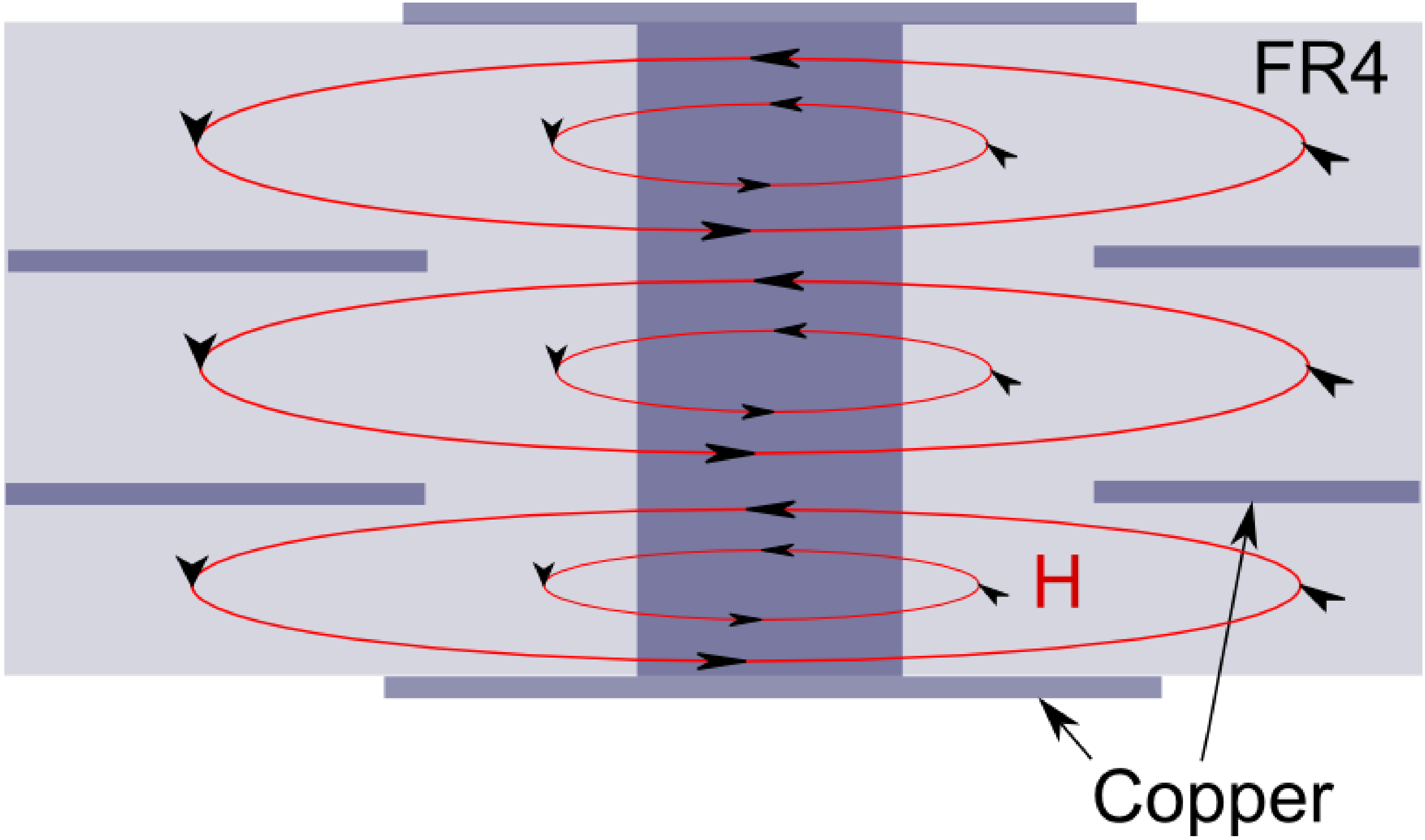
- Loop covered with a closed copper loop of the same size with 0.12mm paper spacer
  - f=69MHz ringing frequency
    - L=13.6nH



Conclusions

- Place solid planes under AC current paths in minimized distance
  - Return currents in the plane will flow directly beneath the signal wire
  - Induced eddy currents will lead to a shielding effect even without a return path through the plane
  - <u>Use always the next layer to the AC signal layer for shielding</u>
  - Multi layer board provide better shielding due to smaller layer distance
- Never interrupt the layer underneath AC signal paths
  - Use other layers for signal routing or route low frequency signals around
- Wider traces lead to lower inductance and resistance thus much lower impedance
  - Copper on a PC board is already paid for, remove only if required

Vias

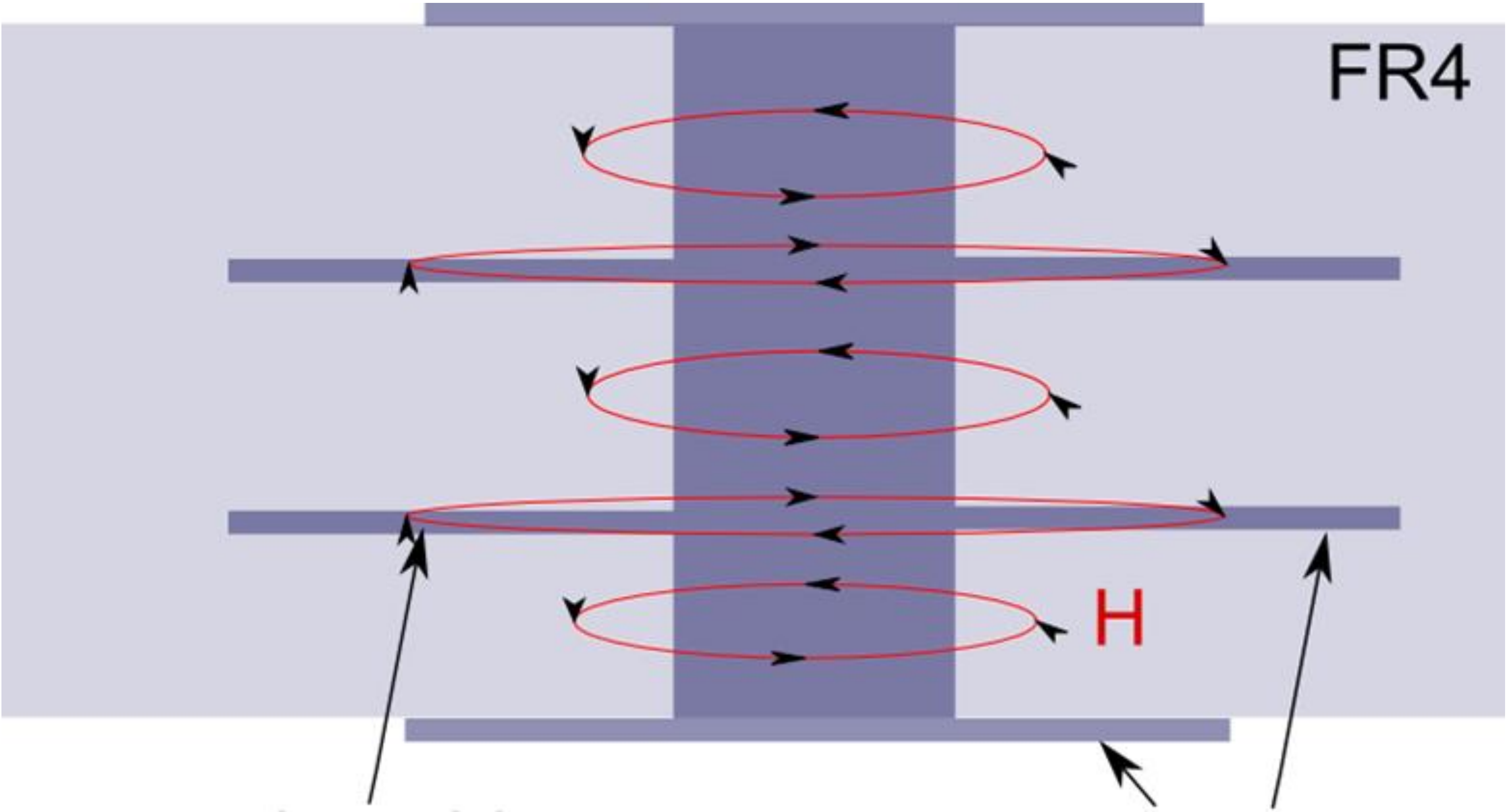


Vias

- Low diameter of vias leads to high inductance
- Inductance increases with length of via
- Most of the PCB material is FR4 with only a very small portion of thin copper
- Copper planes are oriented 90 degrees to the via so no effective shielding possible.
- A low inductance via is thick, short and would ideally have a coaxial outer shield - Unfortunately this is beyond normal PC board technology
  - This can be approximated with surrounding return path vias
    - Area consuming

Vias

- Connected pads around vias slightly decrease their inductance
  - Use in case multiple parallel vias are not possible due to space restraints in single layers



Conclusions

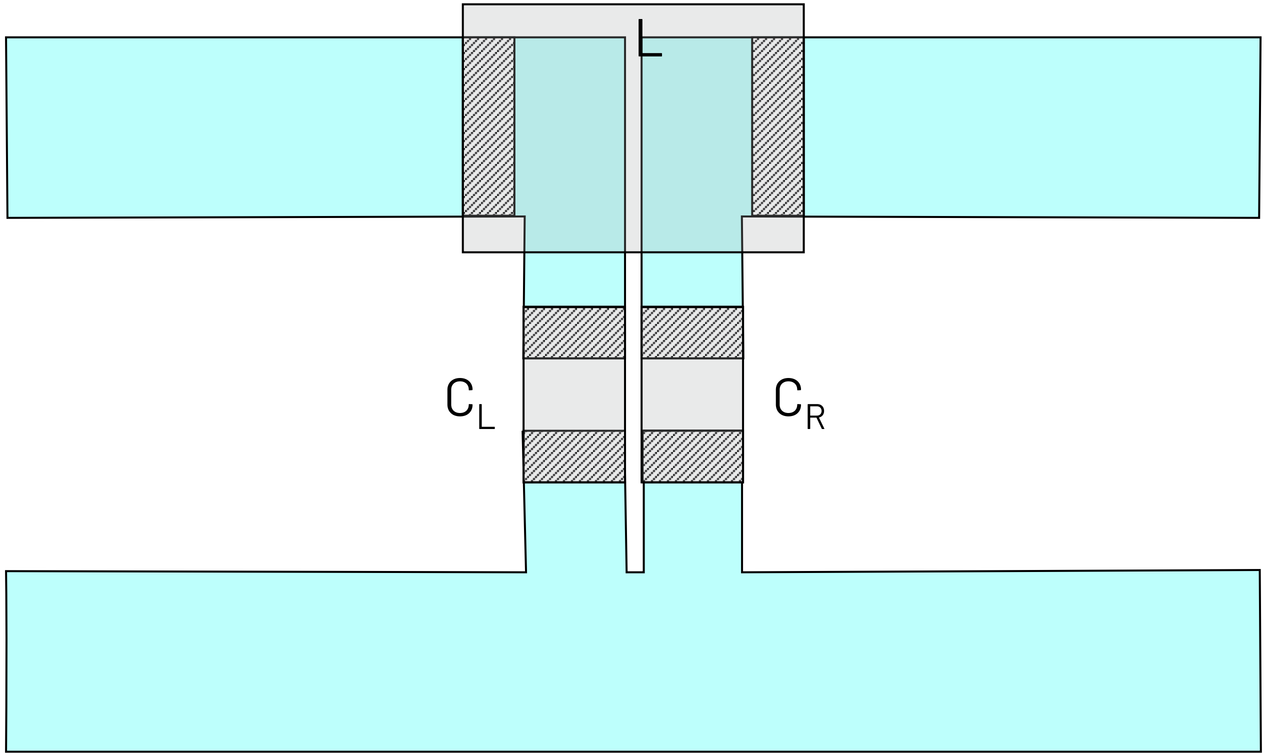
- Avoid vias in AC current paths
- If vias cannot be avoided use many in parallel and with maximum possible diameter
- Connect parallel vias in each layer
- Minimize passed number of layers
  - Vias from one layer to the next are shorter and have lower inductance than vias through the whole board
  - Use micro vias
- Place a connected pad around the via on every layer it is crossing to reduce inductance if the area is not sufficient for parallel vias
- A close distance of forward and return path vias reduces total inductance
  - Coaxial structure

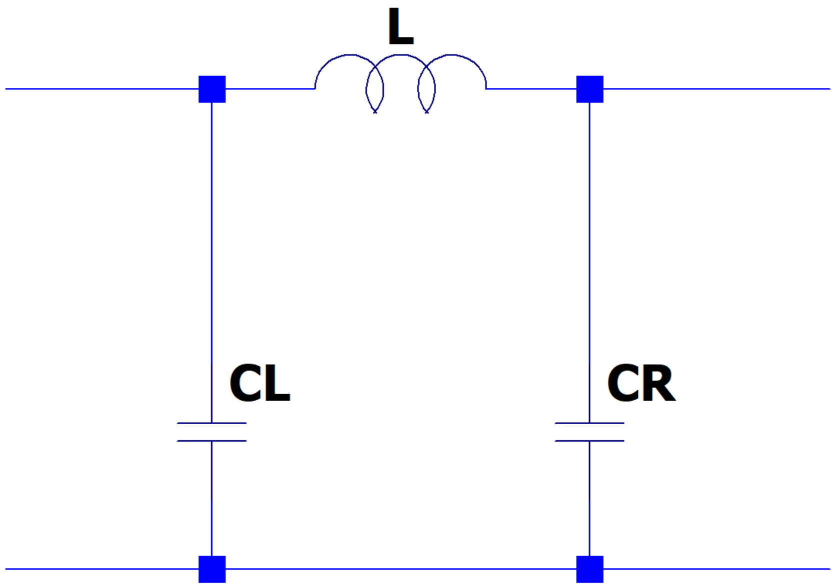
Limitations on Optimum Layout

- Location on PCB
  - E.g. neighbourhood
- Area limitation
- Single- or two-sided population
- Number of layers
- Available and blocked layers
- Via types
- EMI
- Parasitic properties
  - E.g. wire inductances, coupling capacitances

A Compact Filter Layout Example: Recommendable?

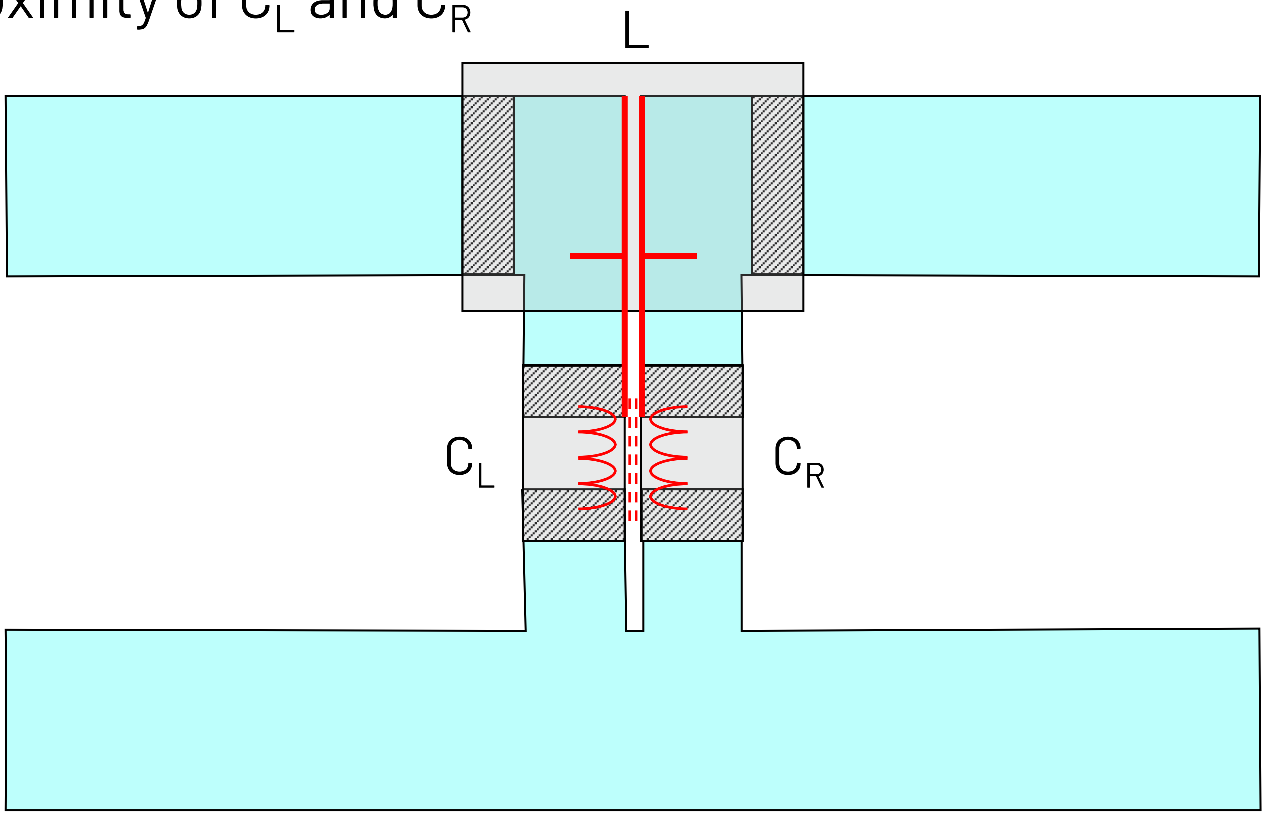
- What are the weaknesses of this layout?

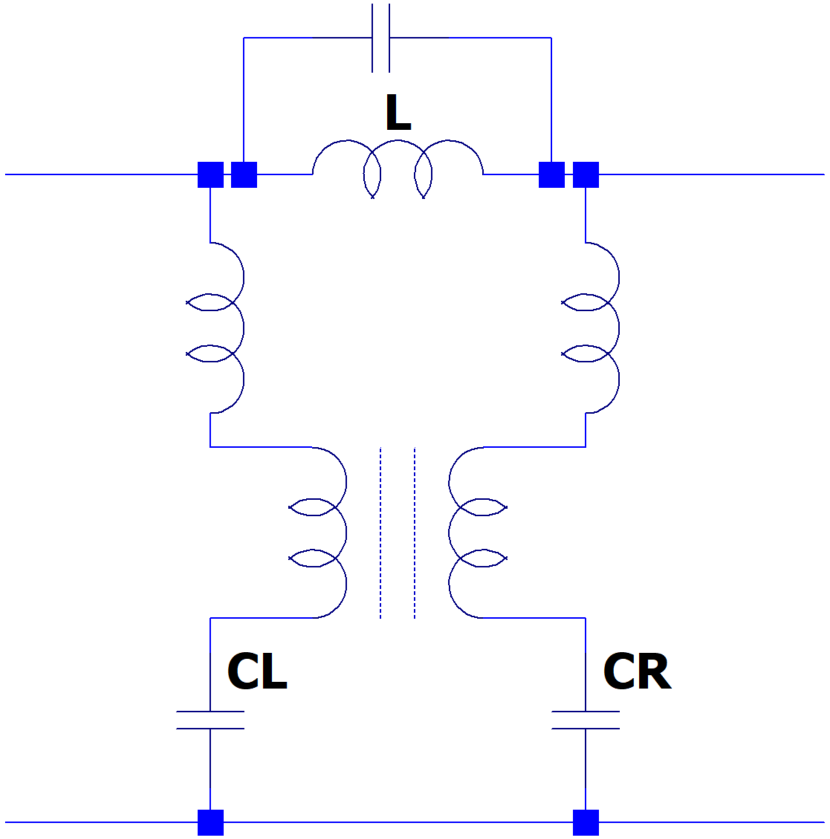




A Compact Filter Layout Example: Recommendable?

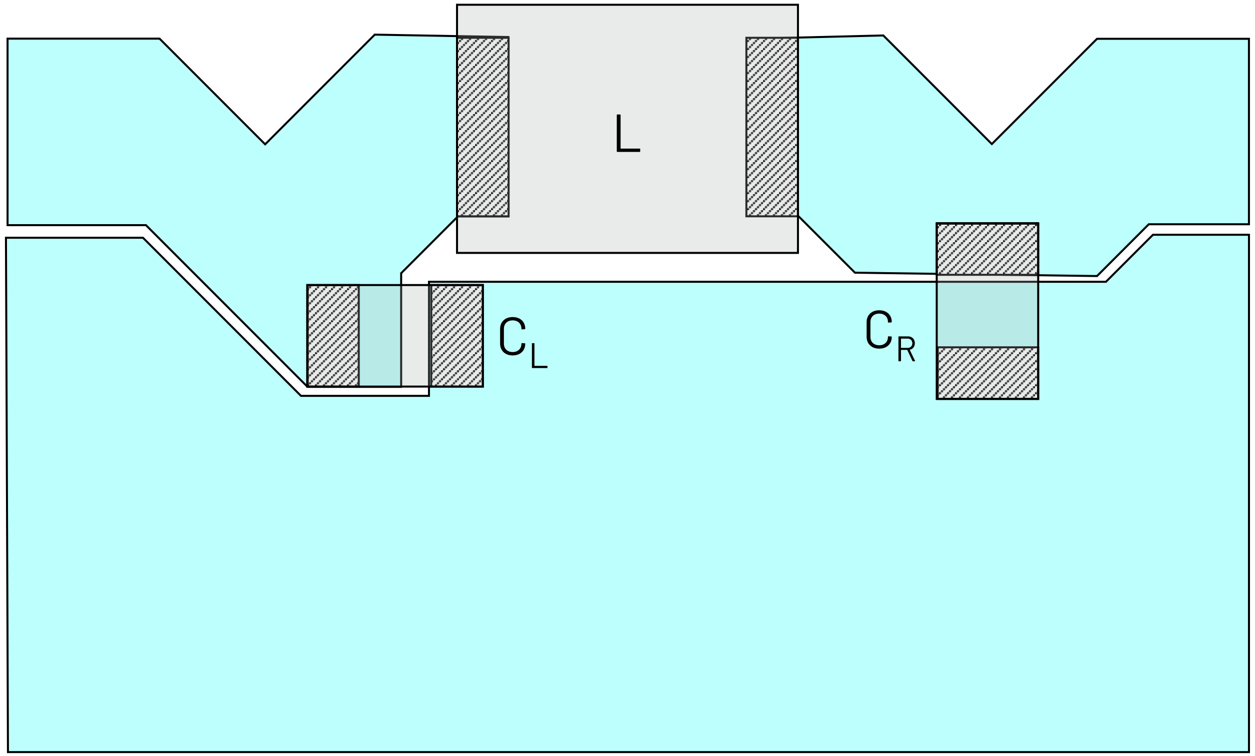
- Additional capacitive coupling parallel to L
- Magnetic coupling
  - Parallel traces to C_L and C_R
  - Proximity of C_L and C_R





A Compact Filter Layout Example: A Lot Better

- Reduced capacitive coupling parallel to L
- Reduced magnetic coupling (90° rotated capacitors, increased distance)
- Reduced parasitic L in series to capacitors

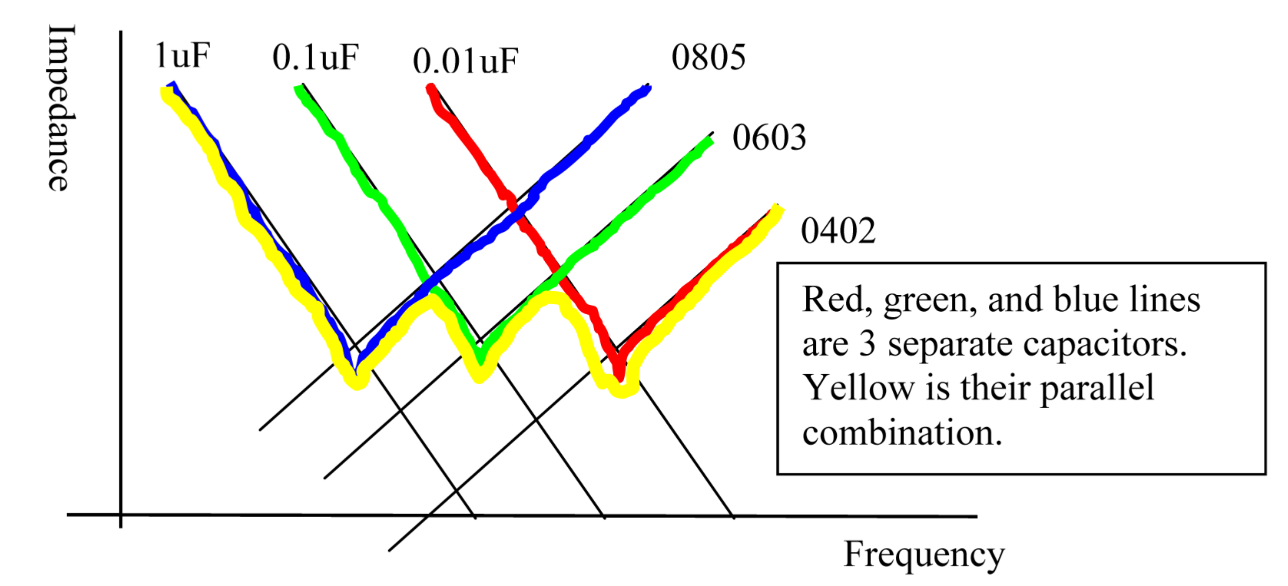


Paralleled Capacitors - A simulation

Combination Of Capacitors

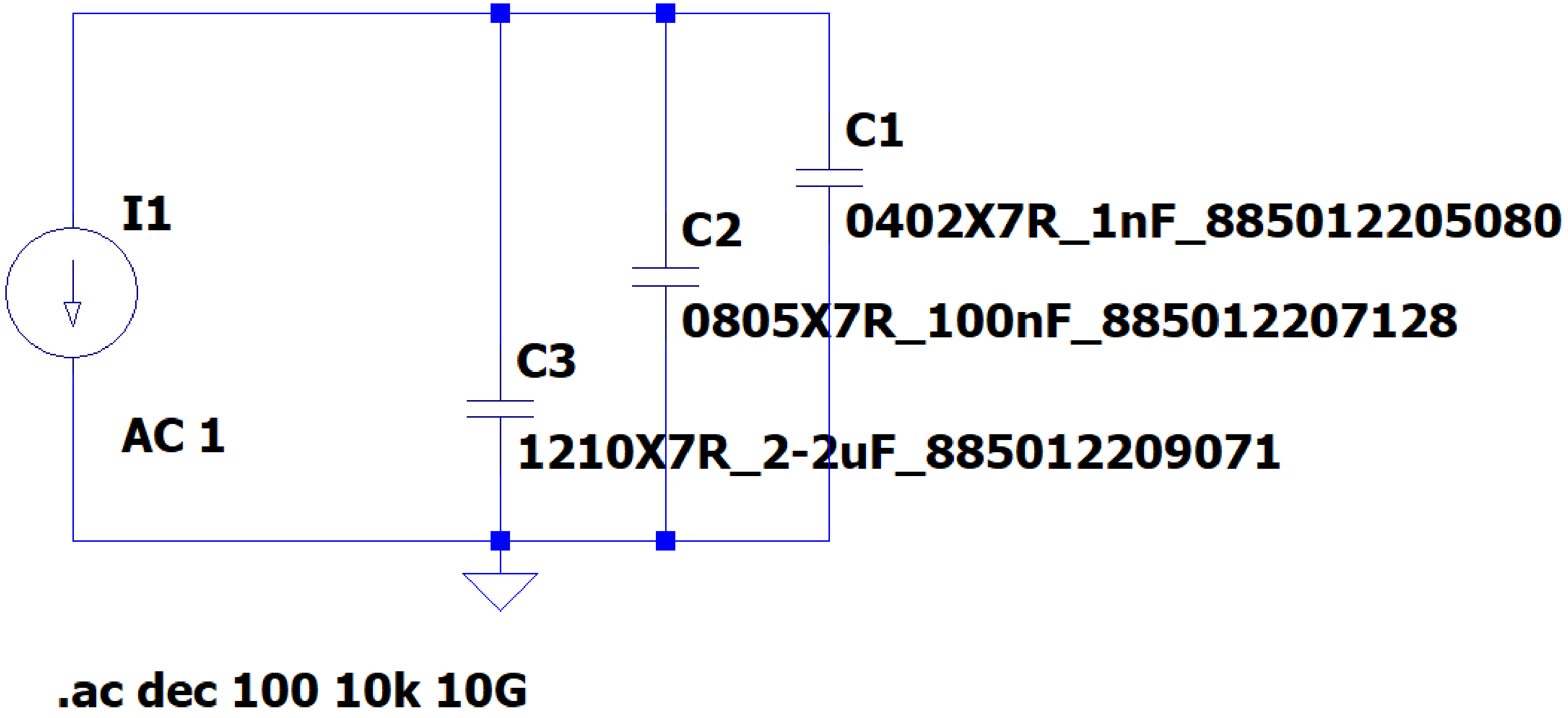
- Different sized Capacitors only contibute their desired Properties?
- Often used in App-Notes (even ours)
- Check in Simulation!

- Really?



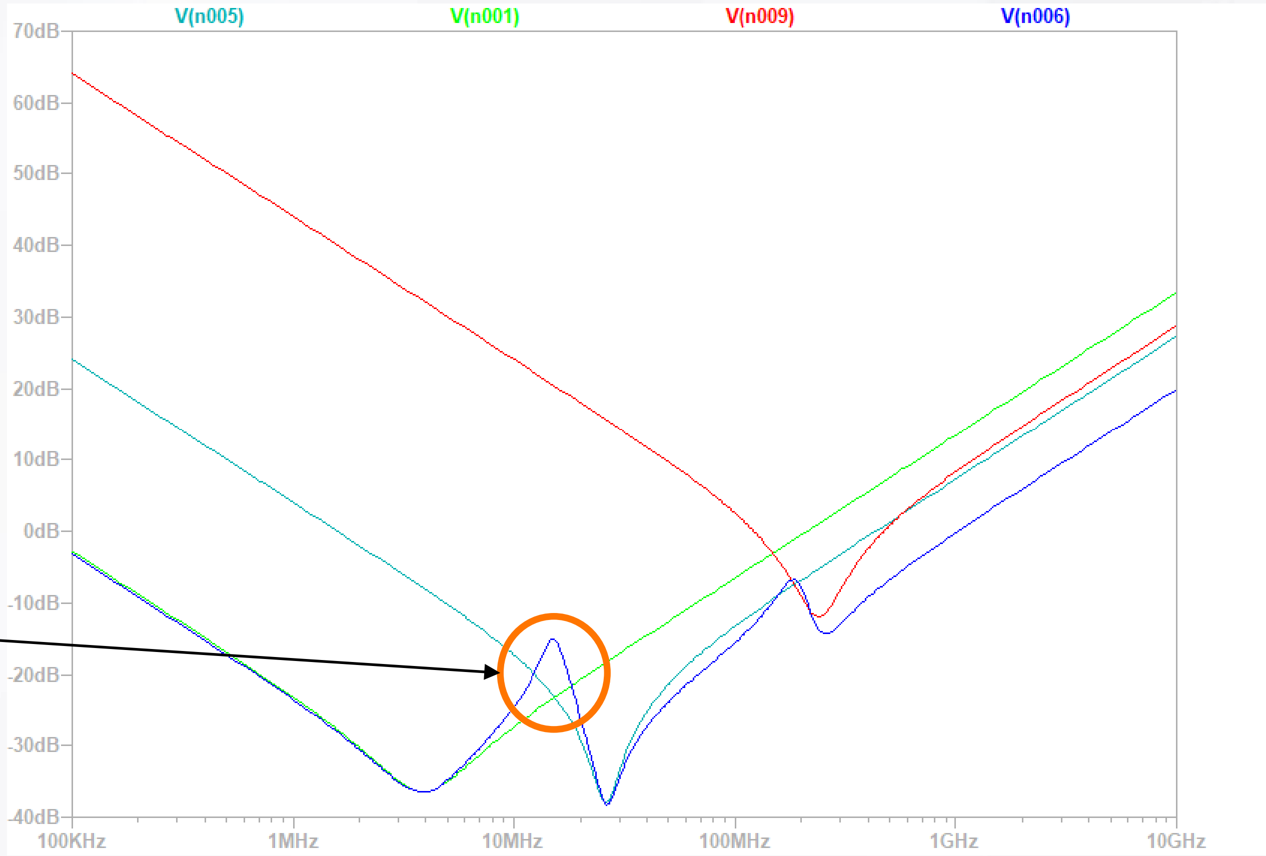
The Basic Configuration

- Assumed for 24V supply with 60V Buck
- 100V rated MLCC Caps
- No Bias Considered
  - It matters though...



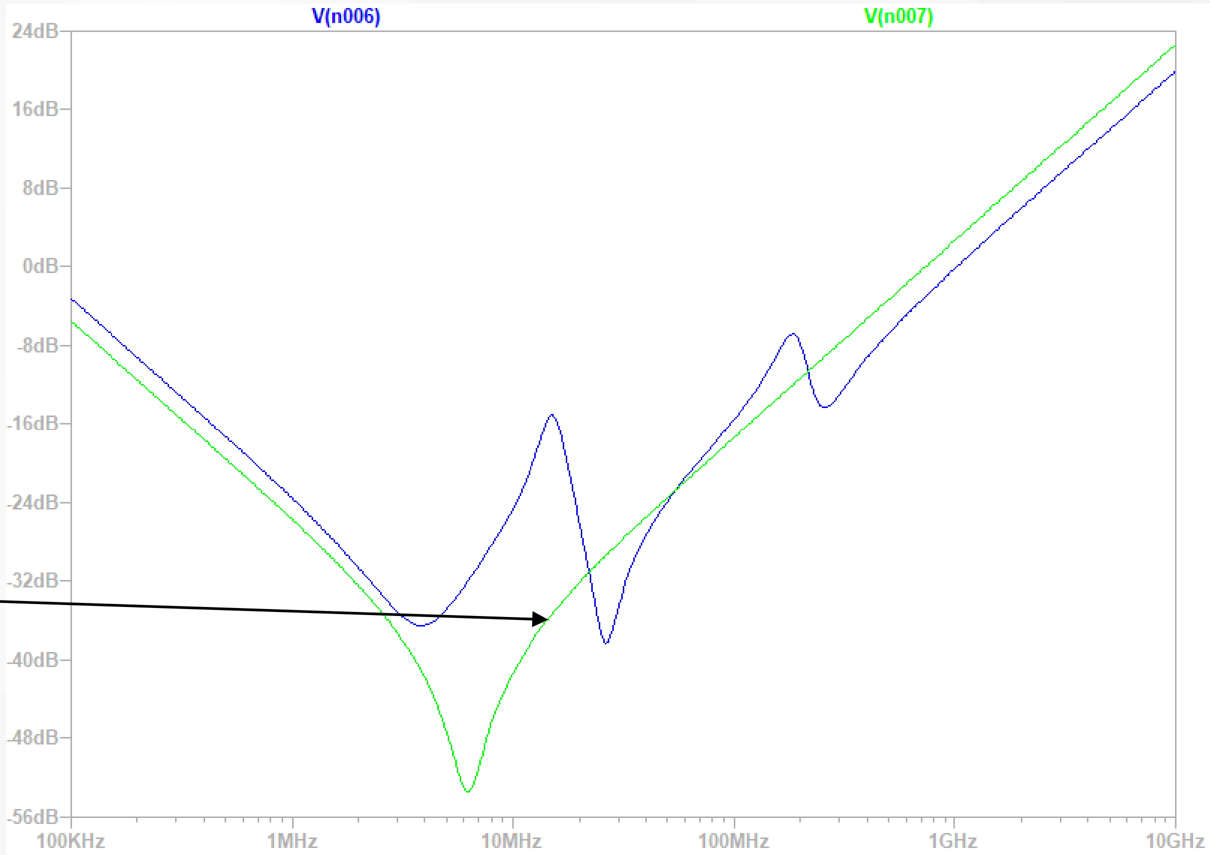
Combination Of Capacitors

- Combination of 2.2uF II 100nF II 1nF
- Looks almost like in Theory
- But not without a problem



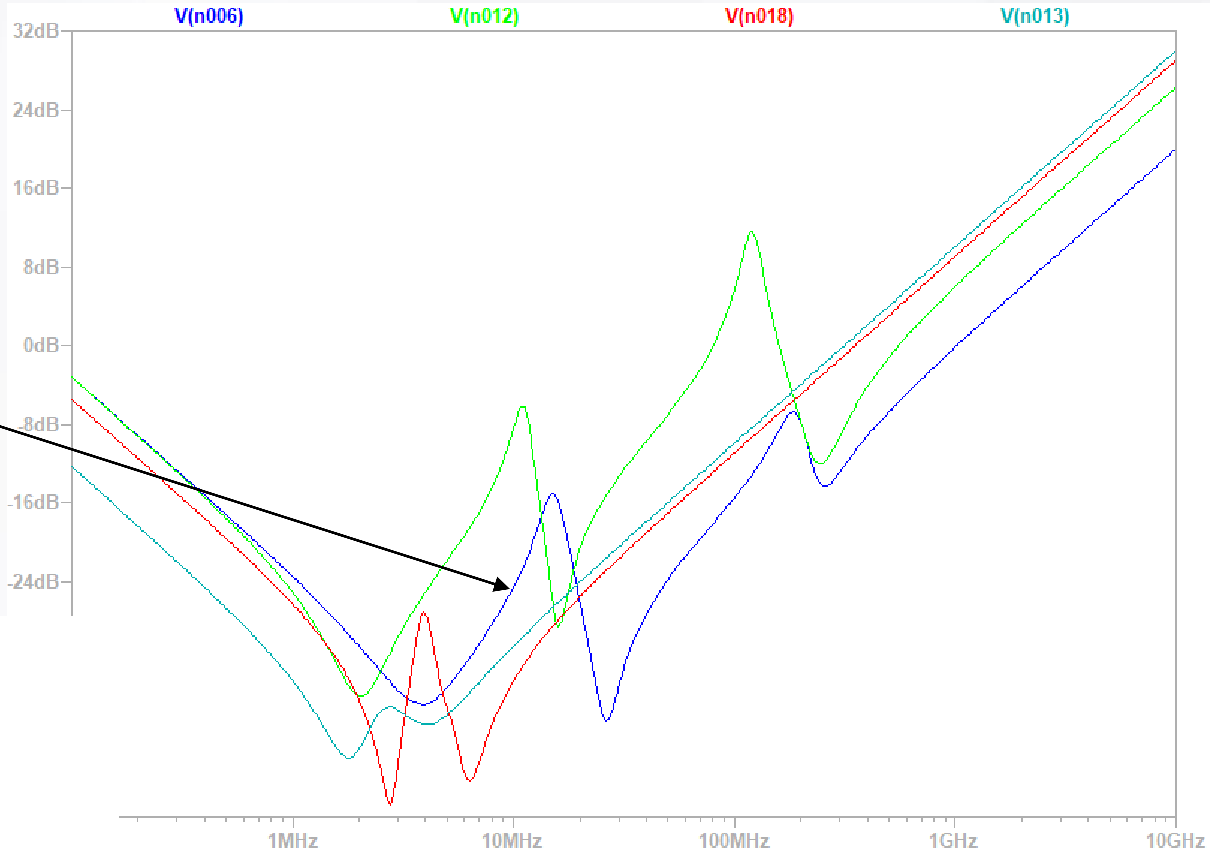
Combination Of Capacitors

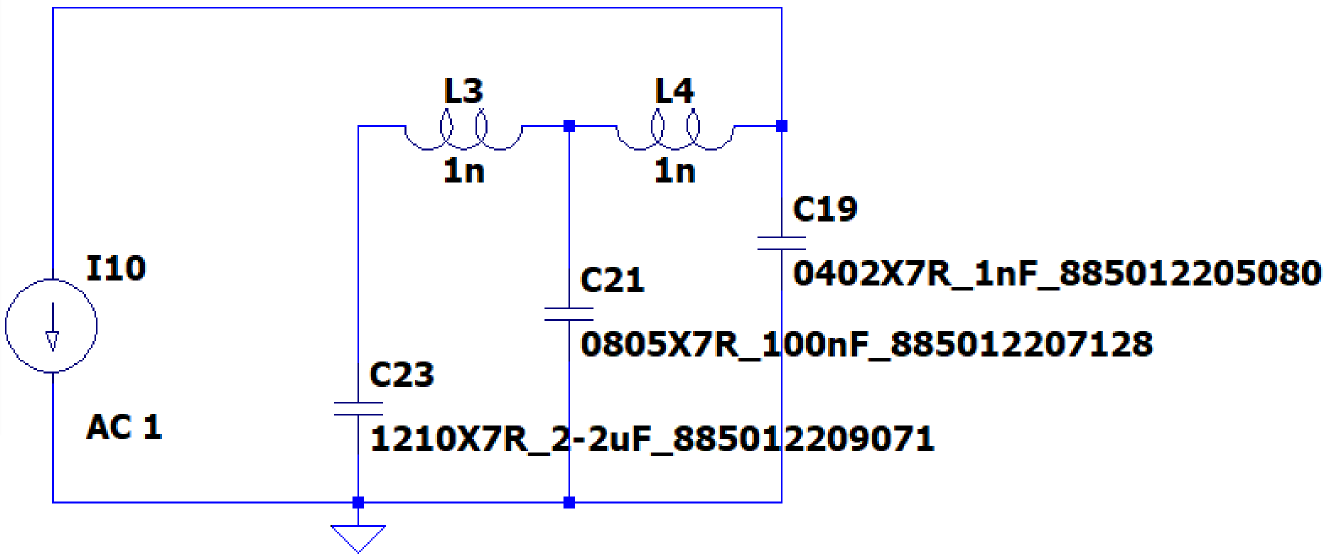
- Combination of 3x 1uF in comparison
- (Almost) the same cost and size
- About 20 dB improvement



Combination Of Capacitors

- Adding parasitic capacitance
- Our ideal reference
- +3x1uF
- +3x2.2uF





Practical Layout Recommendations

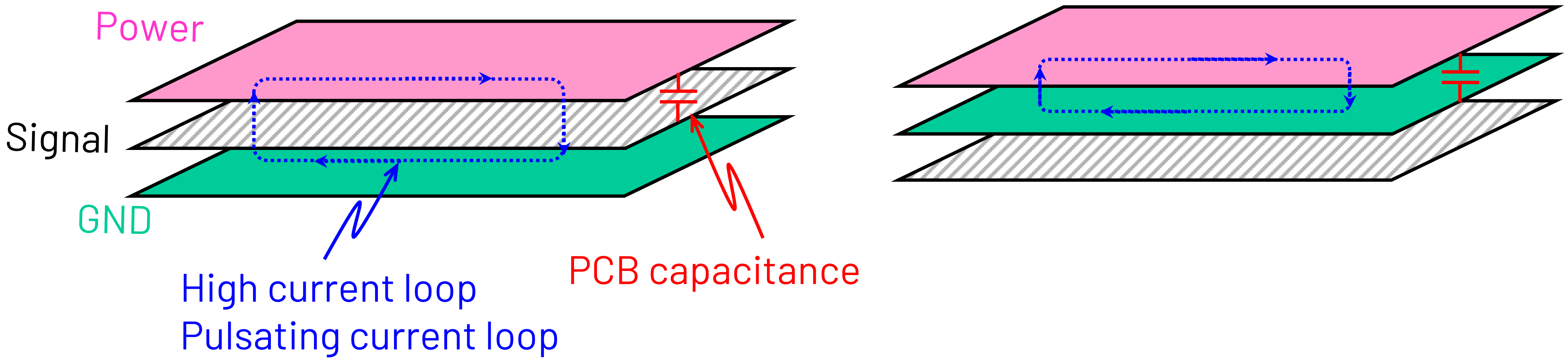
4-Layer PCB – Layer Placement

Undesired

Layer #1 – Power Component
Layer #2 – Small Signal
Layer #3 – GND
Layer #4 – Small signal / controller

Desired

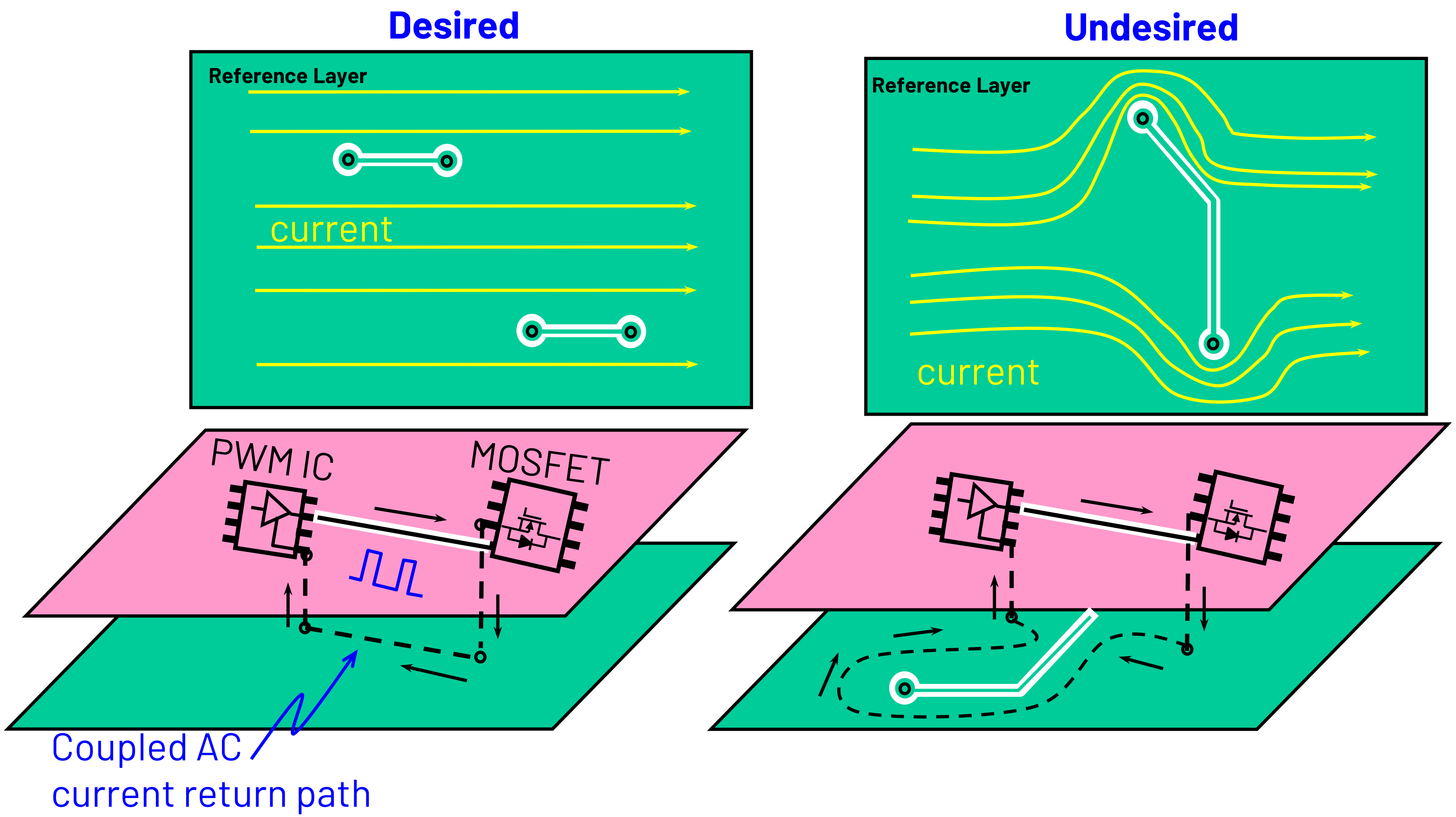
Layer #1 – Power Component
Layer #2 – GND
Layer #3 – Small Signal
Layer #4 – Small signal / controller



Place ground or DC voltage layer between power layer and small signal layer

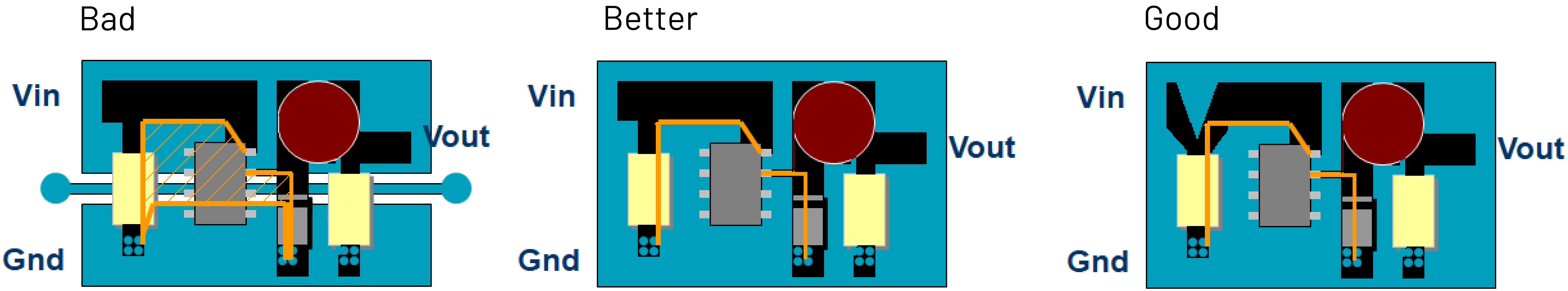
Small Signal Traces on Reference Layer

- If the small signal traces have to be routed on the reference layer, use short traces with proper direction



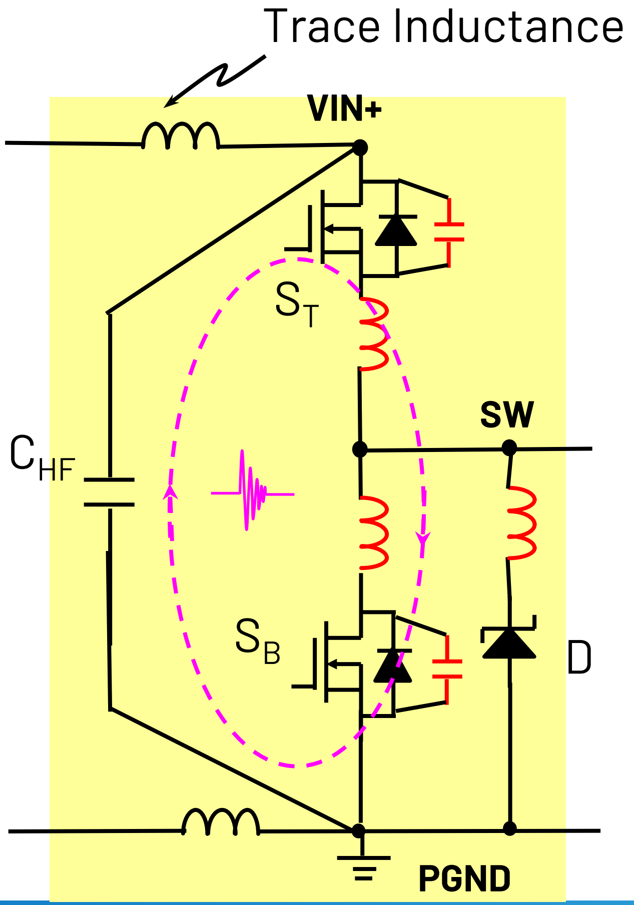
Ground Plane example

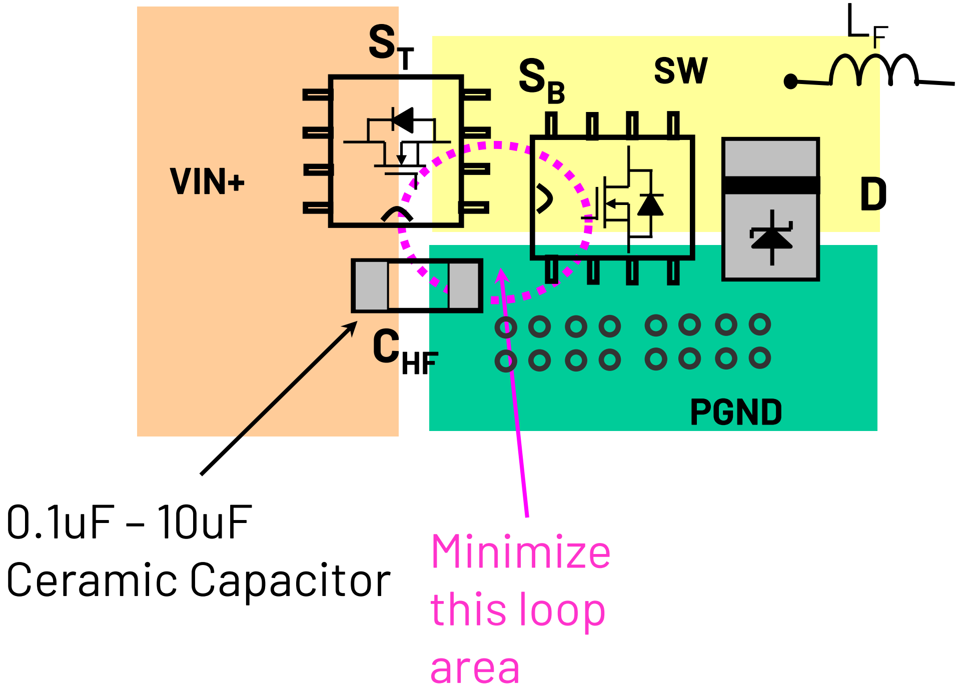
- Use multiple vias
  - In hot loops to reduce ESL
  - In power path to reduce current density (typically below 500mA/via)
- Smallest loop area in the plane is under forward path
- Never Split a ground plane under high frequency path



Parasitic Inductance in the Current Paths and Example Layout (Buck)

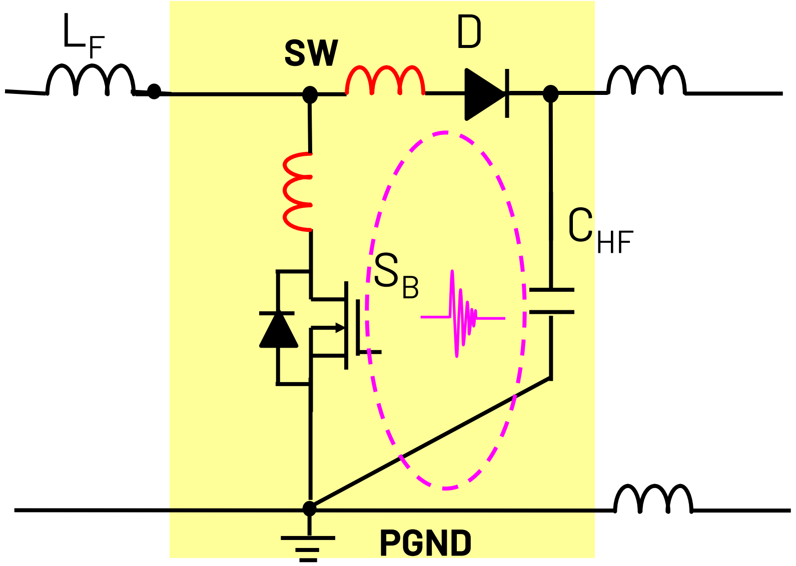
- Minimize loop between HF capacitor and MOSFETs
- It is desirable to keep DC/DC-controller, C_{HF}, C_{BOOST}, C_{INTVCC}, top FET and bottom FET on the same layer
- Use multiple vias for power connections and in hot loops



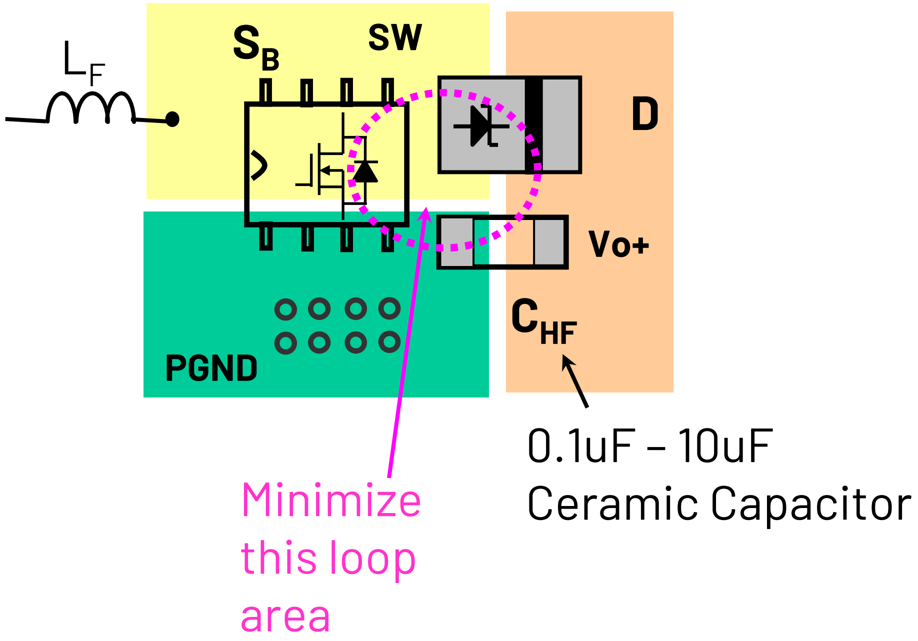


Output Noise Decoupling Capacitor (Boost)

- Minimize the critical pulsating current loop on the output side



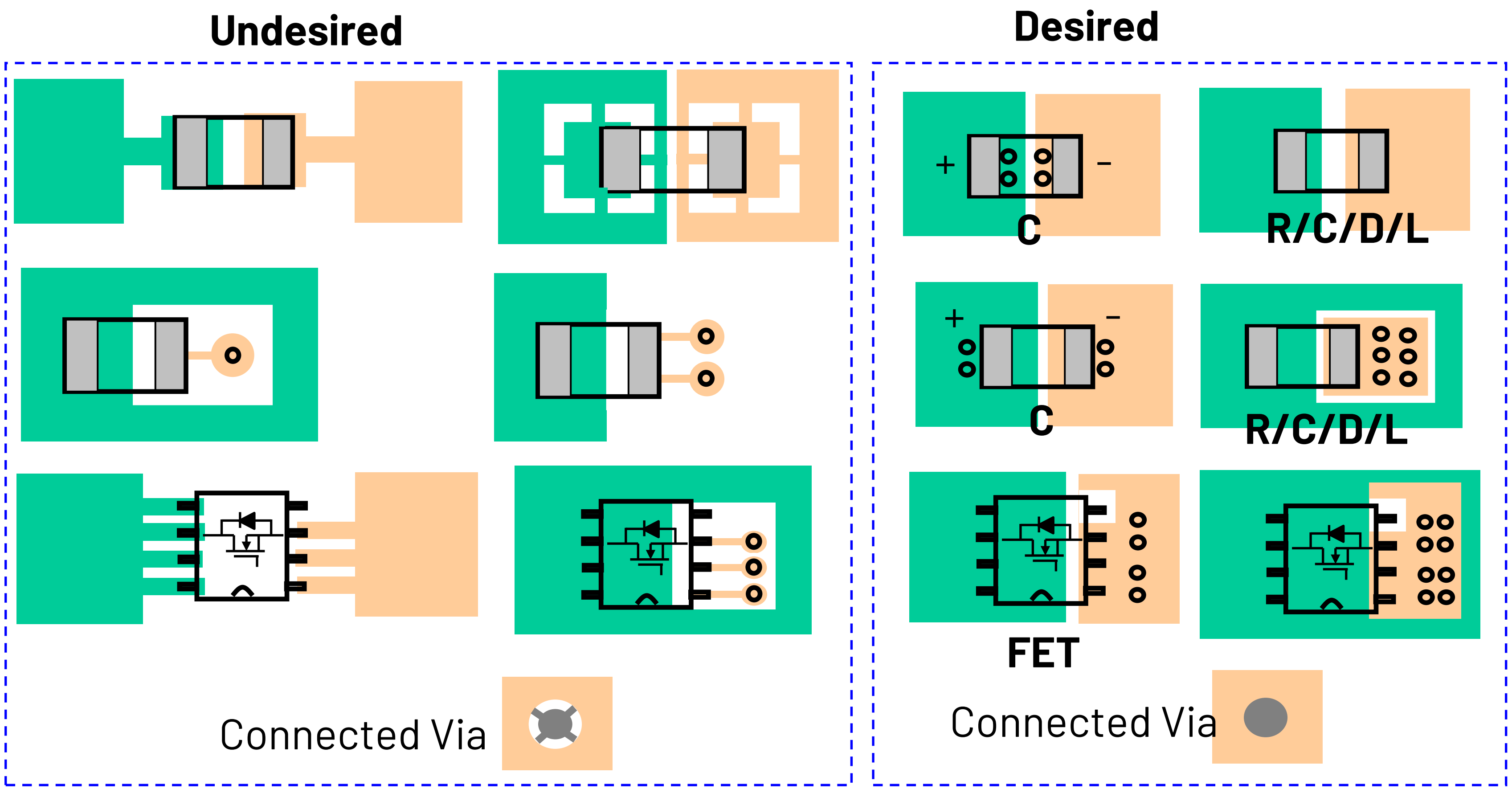
(a)



(b)

Land Patterns of Power Components

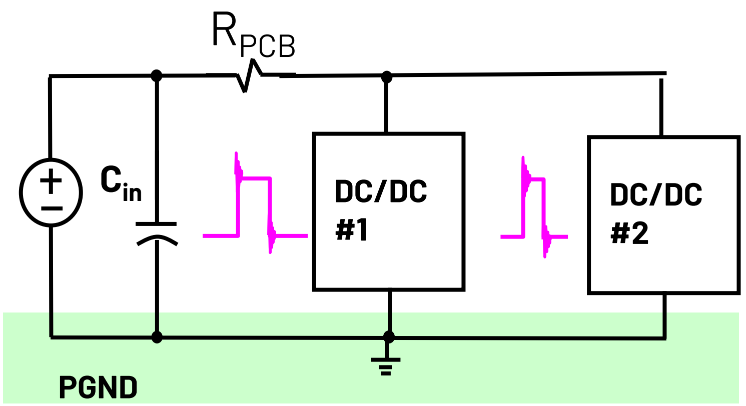
- Use wide / short copper trace for power components
- Use multiple vias for inter-layer connections
- Avoid improper use of “thermal relief”
- Minimize resistance and inductance



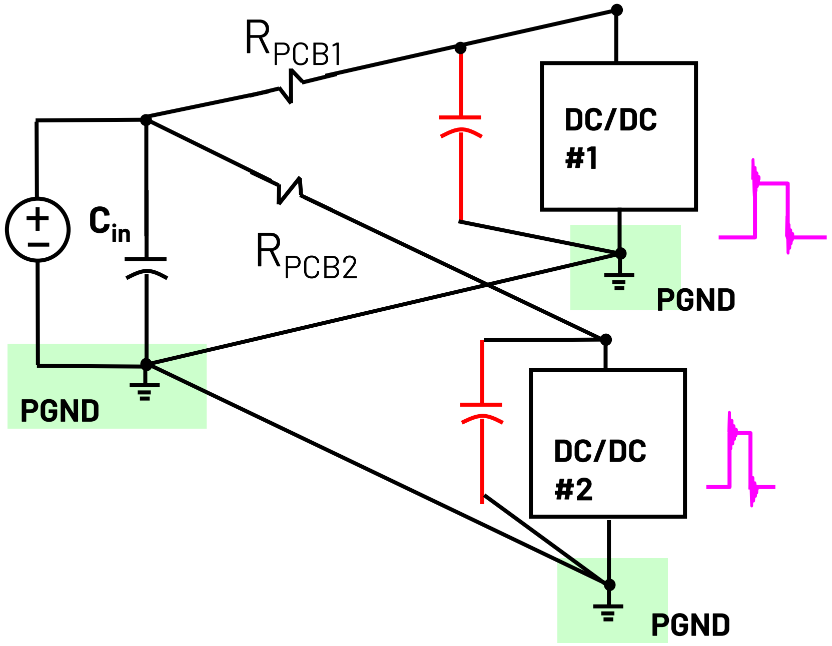
Separation of Input Paths Among Supplies

- Avoid ground return currents from other converters

Undesired

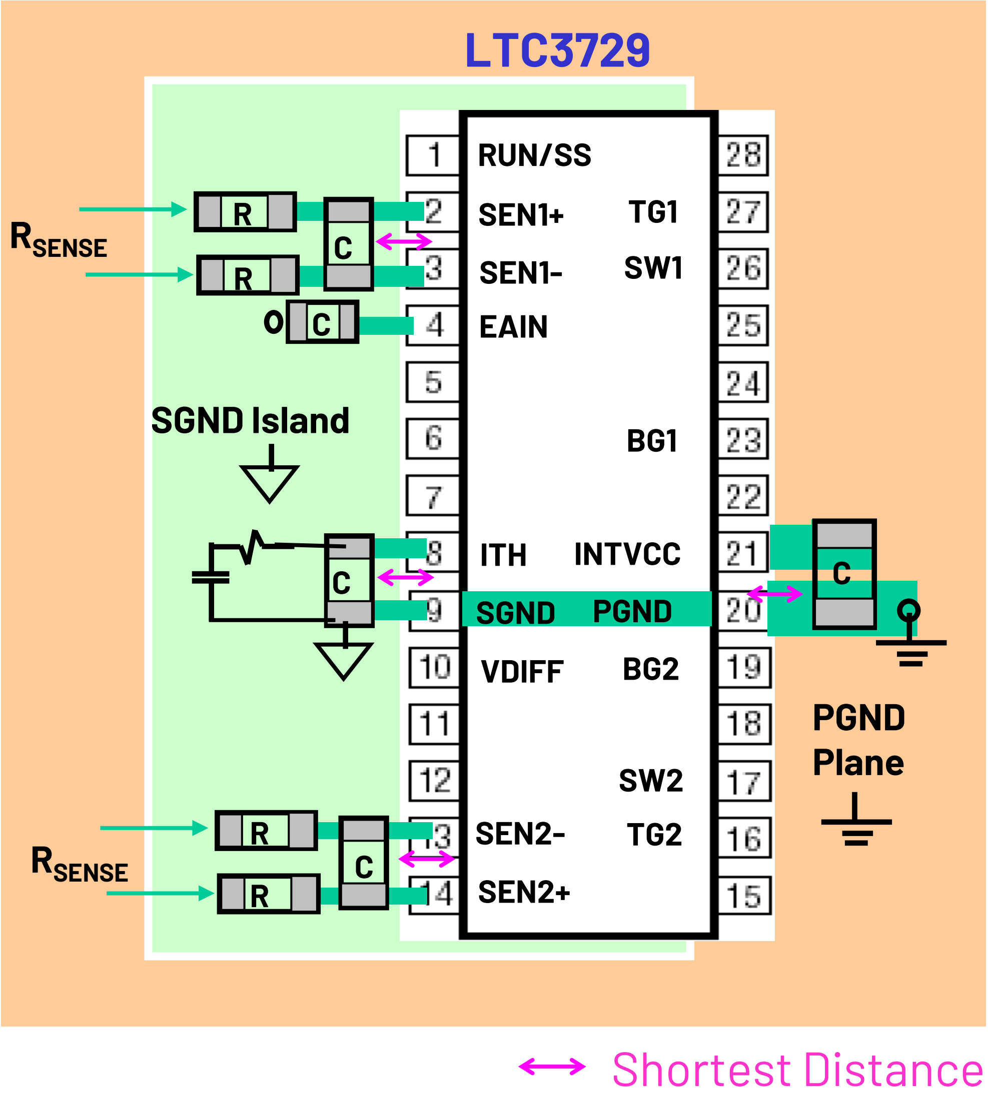


Desired



Decoupling Capacitor and Separated Grounds

- "Star" connection of PGND and SGND
  - Only required if current flow through SGND area has to be prevented
    - Avoid current flow in this area, so no SGND separation will be required
- Only slowly changing signals related to SGND
  - Decoupling for low-side gate drivers (INTVCC) has high RF content!
    - Connct to PGND



QFN Package Ground Separation

- SGND “island” can also be done with SGND on exposed pad
  - Thermal problems may occur
  - A good separation of noisy and sensitive signals is sufficient, SGND and PGND separation is not mandatory

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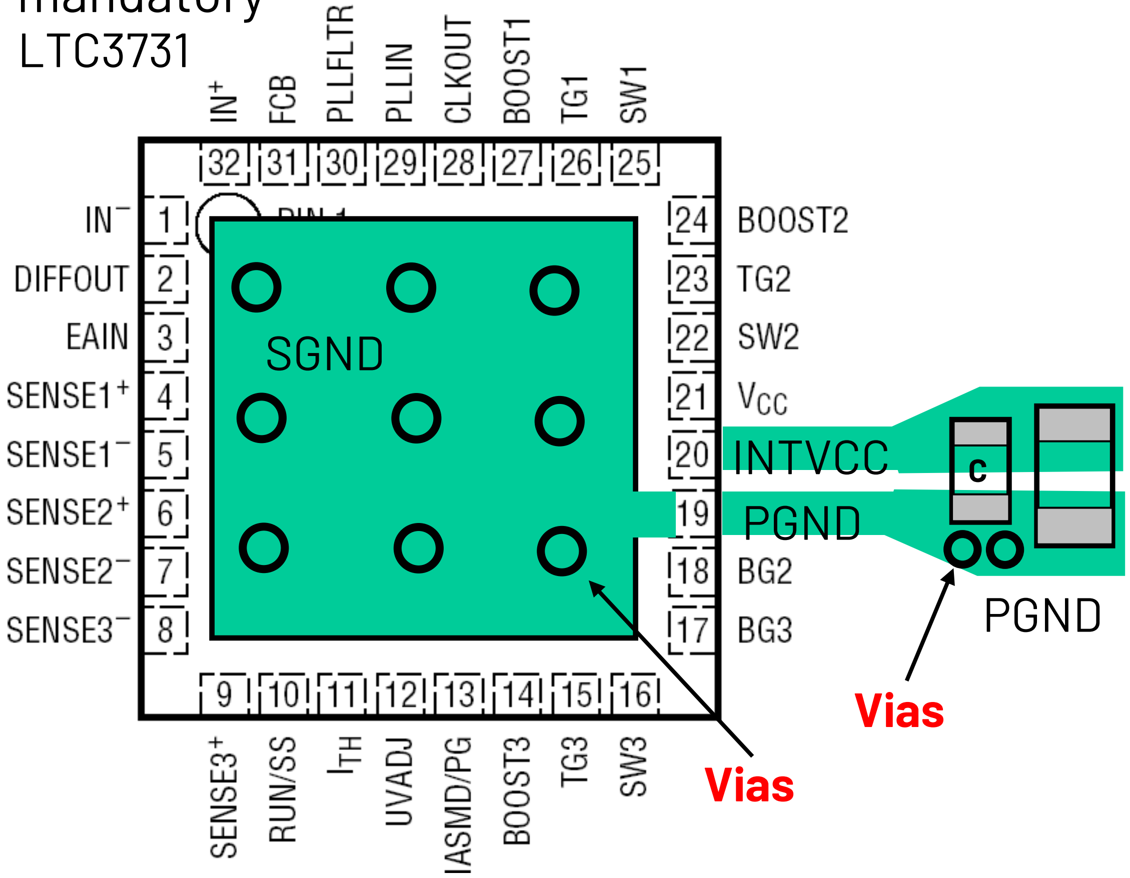
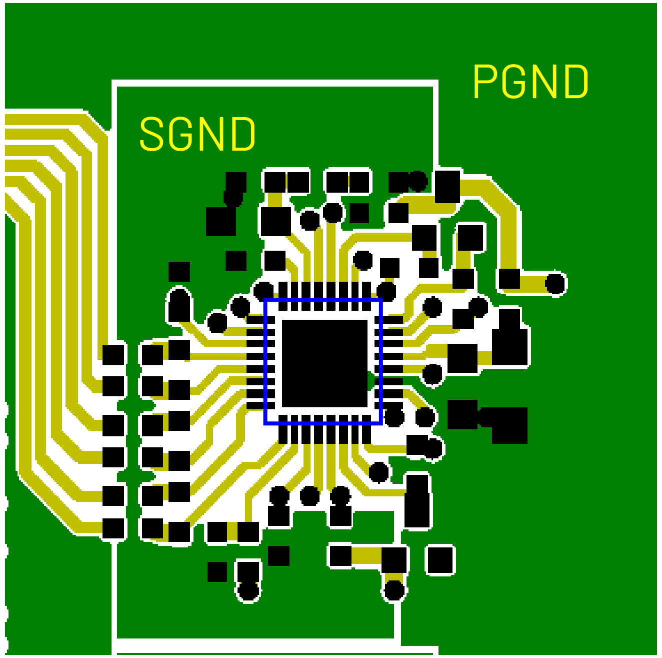


Example



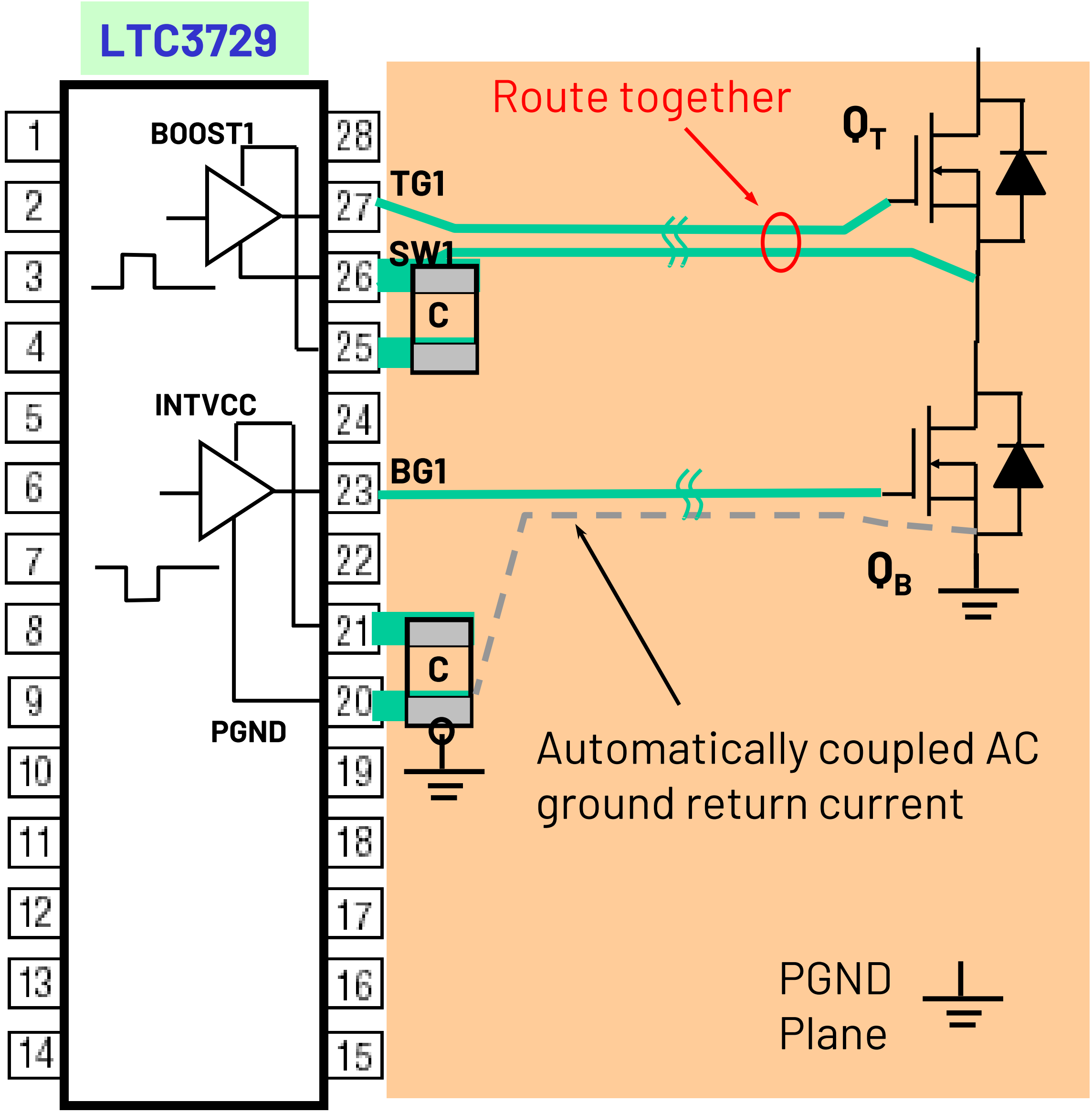
Sensitive Traces and Noisy Traces

- Most sensitive traces:
  - Feedback (FB, EAIN)
  - Loop compensation (V_C, COMP, I_{TH})
  - Current sensing (SENSE)
    - Sense+ / – traces for each channel should be routed together with minimum trace spacing. The filter capacitor should be as close to IC pins as possible. The filter resistor should be close to filter capacitor
  - Oscillator (RT, FREQ, PLL, f_{SET})
  - Soft start / tracking (SS, TK, TRACK)
  - Undervoltage comparator (EN/UV)
- Keep sensitive traces away from noisy traces
  - Avoid capacitive coupling
  - Avoid inductive coupling
    - Minimize loops
    - Avoid MLCC magnetic noise coupling

Sensitive Traces and Noisy Traces

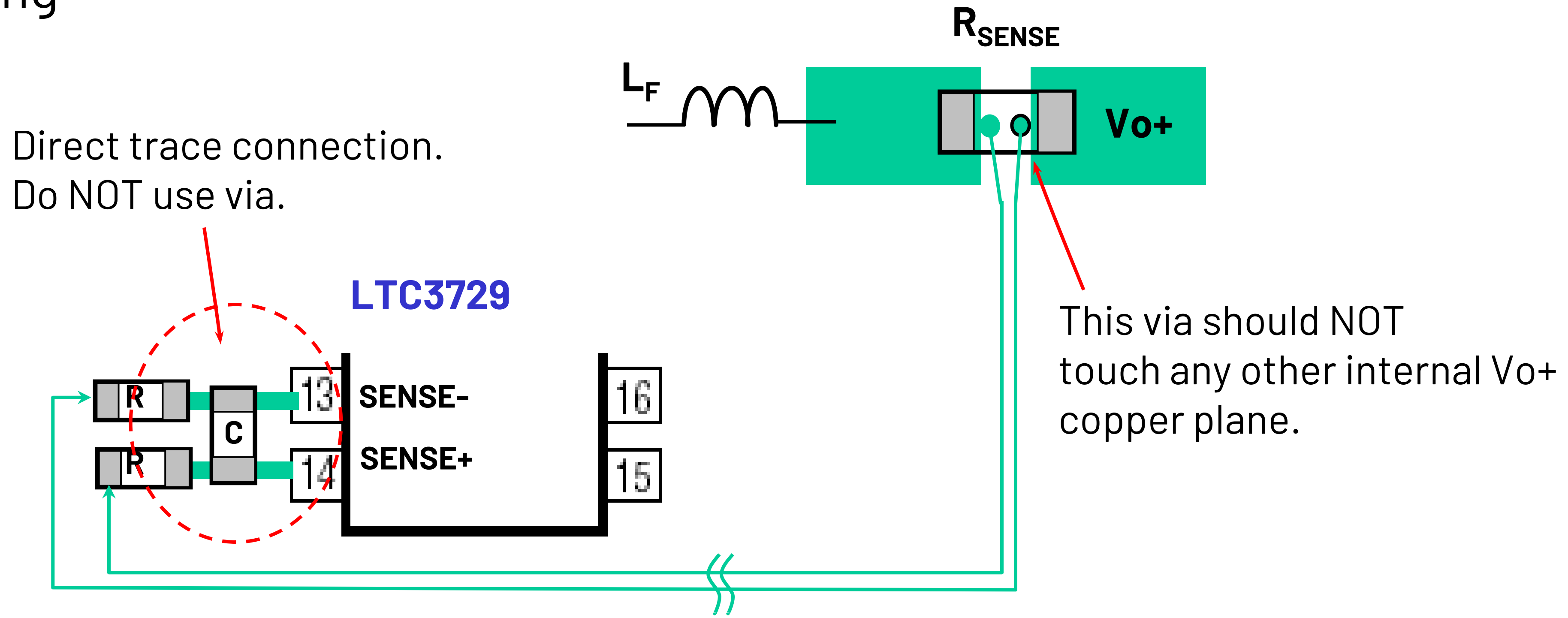
- Most noisy traces:
  - Switched inductor side (SW)
  - Gate signals to external MOSFETs (TG, BG, DH, DL)
  - Bootstrapped high-side gate driver supply (BST, BOOST)
- Keep them away from sensitive traces
- CLKOUT is a sensitive trace but it is also a noisy trace. So keep it away from other small signal sensitive traces and noisy traces
- Avoid overlapping between large SW copper area and sensitive traces in two neighborhood layers
- For each channel, route the SW and TG trace together with minimum space
  - Proximity effect: Minimize loop inductance

Gate Driver Traces



Current Sensing Traces

- Kelvin sensing of the current signal
  - Interference from SMPS and/or outside will mostly produce common mode noise when lines are routed tightly
- Keep current sensing traces away from noisy traces / copper area or use ground layer for shielding



Trace Widths

- General Guidelines:
  - Gate Drive, VCC, VREF – 20 to 25 mils minimum
  - Current Sense, Feedback, Misc. – 15 to 20 mils minimum
- Power Traces
  - DC current guideline according IPC-2221 with a lot of margin $I = k\Delta T^{0.44}A^{0.725}$

I = current in amperes

A = cross section in sq mils

ΔT = temperature rise in °C

k is a derating constant such that:

k = .048 for outer layers

k = .024 for inner layers

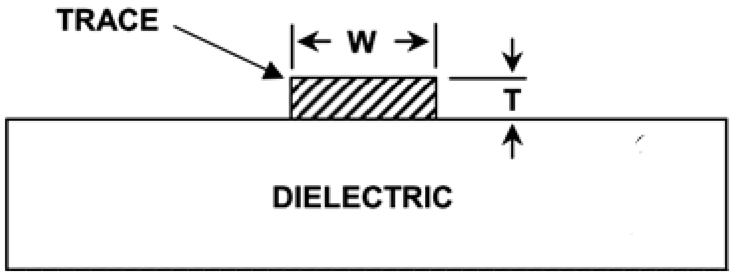
Thickness	T Rise	Allowable Current				
Width		0.25mm/10mil	0.5mm/20mil	1.0mm/40mil	3.0mm/120mil	6.0mm/240mil
35µm/1oz	10K	0.5A	1.0A	2.2A	4.5A	7.5A
	20K	0.8A	1.6A	3.0A	6.5A	11A
	45K	1.3A	2.5A	4.2A	9.5A	16A
	60K	1.6A	3.0A	4.8A	11A	18A
70µm/2oz	10K	1.0A	2.0A	3.5A	7.5A	11A
	20K	1.6A	2.8A	4.7A	11A	18A
	45K	2.5A	4.0A	6.8A	16A	26A
	60K	3.0A	4.5A	8.0A	18A	28A

Copper Thickness and PCB Resistance

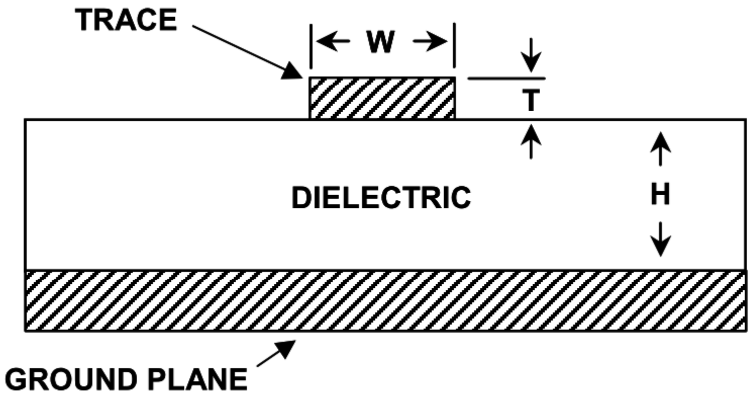
- Copper resistivity ($\frac{\Omega \cdot \text{mm}^2}{\text{m}}$): $\rho(T) = 1.724 \cdot 10^{-2} \cdot [1 + 3.9 \cdot 10^{-3} \cdot (T - 20°\text{C})]$
  - T: Copper temperature (°C)
- Resistance of a PCB copper trace: $R(T) = \frac{\rho(T) \cdot L}{W \cdot T}$
  - L: Length (m), W: Width (mm), T: Thickness (mm)
- Example: Resistance and power loss calculation
  - 1 oz copper (1.4 mil thick), 0.5 inch wide (500mils), 2 inches long (2000mils), at 70 °C with 20A current
  - $R_{copper} = \frac{\rho(T)[\frac{\Omega \cdot \text{mm}^2}{\text{m}}] \cdot \frac{1000\text{mils}}{25.4\text{mm}} \cdot Length[\text{mils}]}{Width[\text{mils}] \cdot Thickness[\text{mils}]} \cdot 10^{-3} \frac{\text{m}}{\text{mm}} = 1.94\text{m}\Omega$
    - V_{copper}=39mV, P_{loss}=0.78W
  - High current applications: 2 oz or higher for power layers recommended

Copper Trace Inductance And Capacitance

- Inductance of a long trace
  - No conducting material in proximity
  - $L = 2 \cdot 10^{-7} \cdot l \cdot \left[\ln\left(\frac{2l}{W+T}\right) + 0.5 + 0.2235 \frac{W+T}{l} \right]$
    F.E. Terman, *Radio Engineers Handbook*, McGraw-Hill, New York, 1945
  - l: length (m), w: width (m), t: thickness (m)
  - Example: L=8.3nH for l=1cm, w=0.5mm and t=35µm



- Inductance of a long trace with solid ground plane underneath
  - $\frac{L}{l} = \frac{120 \cdot \pi}{v_0} \left[\frac{1}{\frac{W}{H} + 1.393 + 0.667 \cdot \ln\left(\frac{W}{H} + 1.444\right)} \right]$
    From "Inductance Loop and Partial", C.R. Paul, Wiley, 2010
    - Assumptions: Perfect conduction, zero conductor thickness
    - Example: L=1.8nH for l=1cm, w=0.5mm and H=112µm
      - Online calculators taking T into account yield 0.8nH to 1nH



Edge Radiation

- AN-

Edge emissions are generated (see Figure 2) where differential noise from many sources meets the edge of the board, leaking out of a plane-to-plane space and acting as a wave guide.

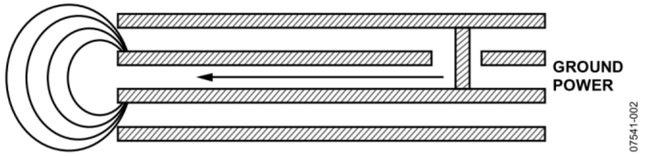


Figure 2. Edge Radiation From an Edge Matched Ground Power Pair

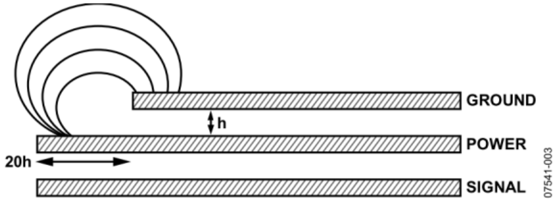


Figure 3. Edge Radiation From an Edge Mismatched Power Ground Pair

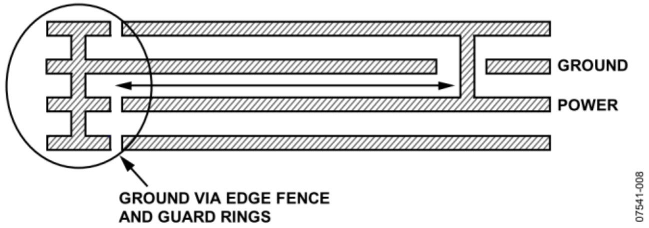


Figure 8. Via Fence Structure, Side View

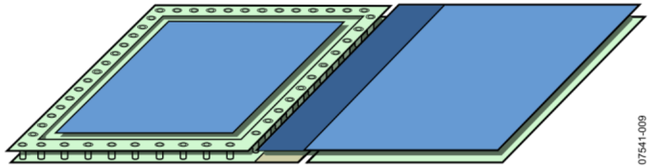


Figure 9. Via Fence and Guard Ring, Shown on the Primary Power Plane Layers

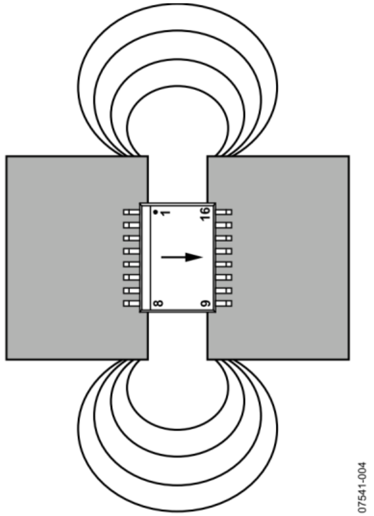


Figure 4. Dipole Radiation Between Input and Output

Summary - Layout Checklist

- Plan of the layout:
  - Prepare a schematic detailing important loops and connections
    - Keep high di/dt paths short to minimize $L_{parasitic}$
  - Determine minimum trace widths and voltage spacing
  - Location of the supply / load / bulk capacitors
  - Location of noisy and noise sensitive devices
    - Magnetic coupling
      - Unshielded or partially shielded inductors
      - Ceramic capacitors
      - Conductor loops
    - Capacitive coupling
      - Outer inductor winding
  - # of layers / layer placement / copper thickness
  - Obtain an example of similar (proven) layout for reference
    - Use the evaluation board layout whenever possible and reasonable

Additional Resources

- **AN136** - PCB Layout Considerations for Non-Isolated Switching Power Supplies
- **AN139** - Power Supply Layout and EMI
- **MT-094** - Microstrip and Stripline Design
- **AN-1142** - Techniques for High Speed ADC PCB Layout
- **AN-1119** - Printed Circuit Board Layout Guidelines for Step-Down Regulators, Optimizing for Low Noise Design with Dual Channel Switching Controllers

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