Reference Design

6 W Unipolar isolated auxiliary supply for SiC-MOSFET & IGBT gate driver

RD002 // ELEAZAR FALCO / EMIL NIERGES

1 Overview

This reference design presents an extremely compact auxiliary power supply providing a unipolar voltage adjustable between +15 V and +20 V. It sources a maximum output power of up to 6 W while covering an input voltage range from 9 to 18 V. The design is optimized for driving high-voltage SiC-MOSFET and IGBT devices and power modules without a negative gate drive voltage requirement, and can be easily integrated into the gate driver system. The extremely low interwinding capacitance of the WE-AGDT 750318114 transformer down to 6.8 pF helps to achieve high CMTI rating (Common-Mode Transient Immunity). This enables fast switching speeds which can yield efficiency and power density gains, as increasingly required in trending applications in e-mobility, renewable energy or industrial automation.

In this document, experimental results for output voltages of +15 V, +18 V and +20 V are provided.

Key Features

- Small size
  (Var.A: 27 mm x 14 mm x 14 mm) (Var.B: 40 mm x 14 mm x 13 mm)
- 4 kV primary-secondary isolation
- Only 6.8 pF typ. parasitic capacitance enabling high CMTI
- PSR Flyback topology with LT8302 (ADI Power by Linear)
- Load/line regulation less than 1 % typ.
- Up to 88 % peak efficiency (86 % at 6 W)
- Standard and AEC-Q qualified component assembly variants
- Two PCB Layout Variants (2-layer and 4-layer)

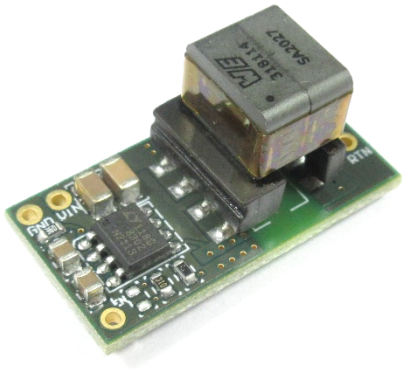

Figure 1: Board Image

Typical Applications

- E-mobility: Electric Powertrain
- On-board and Off-board battery chargers
- Industrial drives: AC motor inverter
- Renewable energy: Solar inverters
- Power factor correction (PFC) stages
- Switch-mode power supplies with SiC MOSFETs

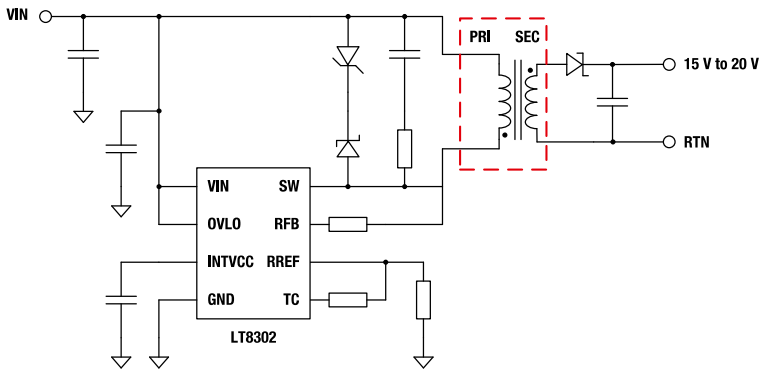

Figure 2: Simplified circuit schematic

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2 Technology and System Design Considerations

Silicon Carbide (SiC) technology is enjoying growing popularity in medium and high voltage power switching applications (typically above 300 V). The extremely fast switching speed of SiC-MOSFETs, their low on-resistance and excellent thermal performance (conductivity and stability) are some of the key advantages against its Silicon-based counterparts. SiC devices are thus starting to replace silicon-based devices like IGBT (Insulated Gate Bipolar Transistor) and Power-MOSFETs in industries like E-mobility, industrial drives and renewable energy.

The voltage required across the gate-source terminals of a SiC-MOSFET is typically found in the range of +15 V to +20 V for full turn-on and 0 V to -5 V for robust turn-off. Note that this negative voltage is sometimes required in order to keep the device off reliably, preventing spurious turn-on caused by parasitic resonant ringing or Miller-effect in hard-switched, half-bridge applications (see section 2.2). Some devices require a unipolar voltage instead, and reliable turn-off at fast switching speeds can be guaranteed by other means, for example, an active Miller Clamp. The RD001 reference design shows the bipolar voltage versions of this auxiliary gate drive supply, covering the most common positive and negative gate drive voltages required.

2.1 Gate Driver, SiC-MOSFET and Auxiliary Power Supply System

A low-power isolated auxiliary supply, typically a flyback, push-pull or half-bridge topology, provides the gate drive voltage level and power required to switch on and off the SiC device, in addition to the galvanic isolation between the high-voltage and low-voltage sides. Isolation is a requirement not only to meet relevant safety standards, but also to reduce electrical noise improving EMI and gate driver control robustness. The transformer in the auxiliary supply fulfils this primary task. Regarding the gate driver stage, an isolated gate driver IC with an output transistor stage in push-pull/totem-pole configuration is typically used to drive the gate-source of the SiC device based on a control signal from the controller system. The system connection is shown below:

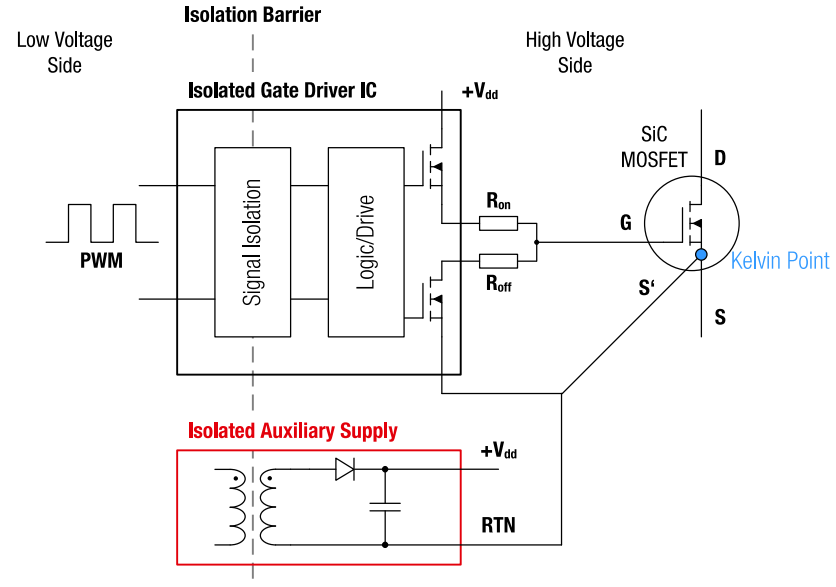

Figure 3: Connection of unipolar auxiliary supply with gate driver IC and SiC-MOSFET

Note that alternative implementations are also possible, for example using an external push-pull stage with discrete MOSFETs for higher peak current strength, or using a non-isolated gate driver IC plus a digital isolator or optocoupler providing the galvanic isolation of the PWM control signal. In all such cases, the connection to the auxiliary supply does not change from that shown in Figure 3 above.

It is also important to note that some SiC devices feature an additional Kelvin pin S' for the source terminal, as shown in the image. This connection provides a dedicated Gate-Source path for the gate drive current which is not 'shared' with the current of the power loop (Drain-Source) at the source terminal. This prevents common-source inductance issues during fast switching transitions, caused by the high dI/dt of the power loop current causing a voltage drop across the source parasitic inductance which opposes the applied gate drive voltage, slowing down the switching speed. The isolated ground of the auxiliary supply (RTN) must be connected to this terminal if available, as in the image.

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2.2 Parasitic Gate Voltage Ringing, Miller-effect Turn-on and Active Miller Clamp

A half-bridge configuration is the building block of many switching power converters (Figure 4 left), with a high-side and a low-side SiC-MOSFET device switching alternately. Each transistor typically has its own auxiliary power supply and gate driver circuit:

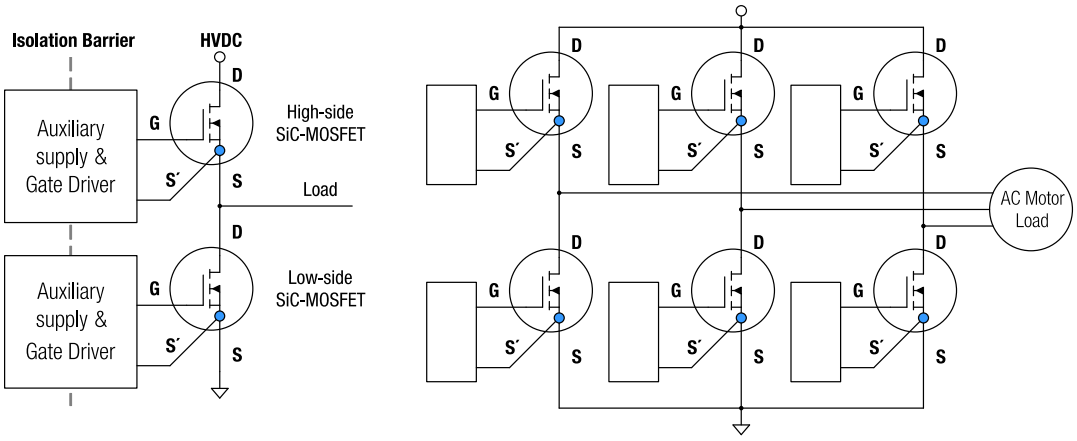

Figure 4: SiC-MOSFET half-bridge configuration (left) and 3-phase inverter application example (right)

When the high-side SiC device is turning on, the complementary low-side SiC device is already turned off as 'dead time' is used. Dead time is a short time window during switching transitions where both devices are kept off in order to prevent shoot-through or cross-conduction. This is caused by both devices being turned on at the same time due to control signal propagation delay mismatch in the gate driver, parasitic ringing, etc. During this 'dead time', the 'body-diode' of the low-side device (or an external anti-parallel diode) keeps current in the loop flowing. At turn-on of the high-side device, the very fast switching speed of SiC-MOSFETs together with the typically high application voltage causes a very high dV/dt to appear across the terminals of the low-side device (which is already off) (Figure 5). This dV/dt in turn causes an instantaneous displacement current to flow through the gate-drain capacitance C_{gd} into the gate circuit of the device. Although the gate-source impedance (Z_{gs}) is a parallel combination of the gate-source capacitance (C_{gs}) with the sum of the total turn-off gate resistance (R_g) and the gate loop inductance (L_p), for high frequency harmonics this typically approximates the impedance of C_{gs}, and therefore C_{gd} and C_{gs} form an effective capacitive divider. Based on this, C_{gs} should be considerably higher than C_{gd} in order to prevent the voltage bump generated across gate-source to exceed the threshold voltage of the device, turning it on and causing a shoot-through event. This is known as Miller-effect turn-on, with both SiC devices fully or partially on at the same time, effectively connecting the HVDC bus to GND through a low resistance path. This is a very dissipative event with consequences ranging from just a drop in efficiency and higher operating temperature up to even catastrophic damage of the devices in severe cases.

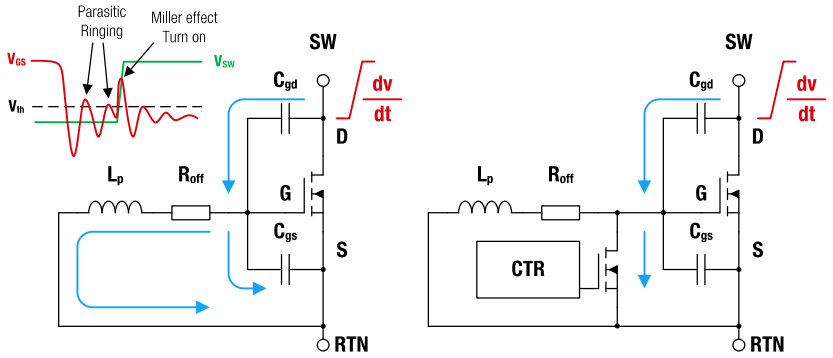

Figure 5: SiC-MOSFET Parasitic turn-on due to Miller effect and gate resonant ringing without Miller clamp (left) and active Miller clamp concept (right)

Such spurious turn-on event may not always appear, since the severity of the Miller-effect and amplitude of resonant ringing is dependent on several factors like the switching speed, component parasitics or PCB layout, amongst others. If spurious turn-on is however observed, several solutions are available. One of them is to use a negative gate drive voltage for turn-off of the SiC device (e.g. RD001), which provides extended margin to its threshold voltage. If only a unipolar gate drive voltage can be used due to particular system requirements, an active Miller clamp could solve the issue.

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The active Miller clamp, in its simplest form, consists of a transistor connected right across the gate and source terminals of the SiC device and a simple control circuit (Figure 5 right). The Miller clamp can be implemented either externally with discrete components or by using a gate driver IC with embedded active clamp circuitry. The principle of operation is simple: the control circuit 'monitors' the gate-source voltage and turns on the clamp transistor when it drops below a threshold level during the turn-off transition. In this way, a very low impedance path for the Miller current is provided, since the transistor is in parallel with Z_{gs}, and it would 'ideally' bypass the parasitic elements across the gate-source terminals and thus shunt most of the Miller current caused by the high dv/dt (Figure 5 right). This will help to reduce the amplitude of the gate-source voltage bump and of the parasitic ringing, in turn helping to avoid spurious Miller-effect turn-on. PCB layout is however very important, and the clamp transistor should be placed as close as possible to the gate terminal right at the SiC device package and connected directly with very short traces. Note that long traces can easily make the Miller clamp solution less effective due to the added inductance in the shunt path.

2.3 Auxiliary supply: Output power requirement

During the switching transitions of the SiC-MOSFET device, power is dissipated in the gate current loop resistance as current flows to charge and discharge the gate capacitance of the device to the supply voltage, in order to turn it on and off respectively. The auxiliary supply of the gate driver system needs to source this power, which depends on the gate voltage, the switching frequency and the total gate charge of the SiC-MOSFET, as follows:

$$P = Q_g \cdot f_{sw} \cdot \Delta V_{gs}$$

Where:

Q_g: Total gate charge of SiC device for ΔV_{gs} (see Q_g vs V_{gs} curve in SiC device datasheet)

f_{sw}: Switching frequency of SiC device

ΔV_{gs}: Gate-to-source voltage (full-swing) (e.g. for V_{dd} = +15 V and V_{ee} = -4 V, then ΔV_{gs} = 19 V) (note that V_{ee} = 0 V for unipolar drive, as in this case)

Note that the output stage circuitry of some isolated gate driver ICs is powered directly from the auxiliary supply. Its additional estimated power consumption should be added to the previously calculated gate drive power budget.

In Figure 6 below, it can be observed how during turn-on, the $+V_{dd}$ rail charges the gate capacitance of the SiC device (C_g) via the high-side transistor of the gate driver IC push-pull stage. During turn-off, C_g discharges via the low-side transistor.

For the example of V_{dd} = +15 V and 6 W of output power sourced by the auxiliary supply, the maximum average current in the output rail would be around 400 mA. Each equivalent gate resistance R_{on} and R_{off} dissipate half of the gate drive power, independent of its value (e.g. for 4 W of gate drive power, then 2 W each). Please note that R_{on} and R_{off} are not only set by external discrete resistors added, but also a contribution of parasitic resistances of the SiC device package as well as on-resistances of the push-pull transistors in the gate driver IC output stage, which in many cases are not negligible.

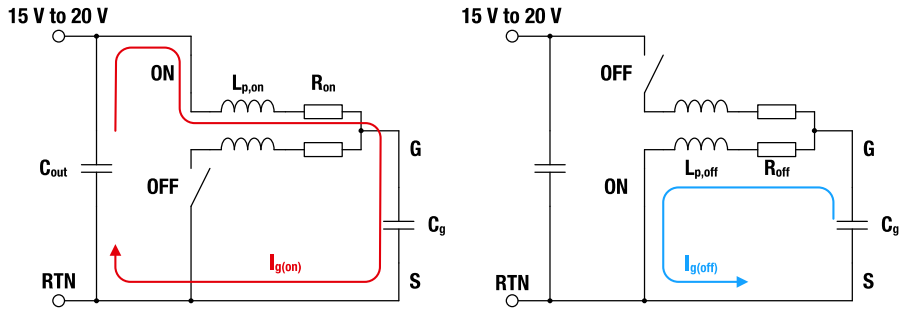

Figure 6: SiC-MOSFET gate current loops from auxiliary supply output rails for turn-on (left) and turn-off (right)

Note also that R_{on} and R_{off} limit the gate current peak (I_g) during each respective switching transition and in turn, adjust the switching speed of the SiC device, but their value do not affect the average gate drive power requirement. If very fast switching speed is required, the gate resistance should be reduced together with the respective loop parasitic inductance ($L_{p,on}$ and $L_{p,off}$). This will allow for higher gate drive peak current and, in turn, faster dI/dt, which would speed up the switching transition.

Regarding PCB layout, it is very important to place the auxiliary supply and in particular, the output capacitors, very close to the gate driver and SiC device gate terminal in order to minimize the area of the gate current loop, and with it the parasitic inductance L_p. Multi-layer Ceramic Capacitors (MLCC) like the CSGP series from Wurth Elektronik are also recommended, due to their extremely low package lead inductance L_c and ESR. The paralleling of several capacitors would allow for a higher di/dt of the gate drive current and faster switching speed due to significant reduction of total L_c and ESR. The final value and configuration of the output capacitors can be freely adjusted by the designer under consideration of switching speed of the SiC device as well as maximum voltage ripple and transient response of the auxiliary supply.

2.4 A critical factor in fast-switching SiC gate driver systems: Isolation Barrier Parasitic Capacitance and CMTI

CMTI is the acronym for 'Common-mode Transient Immunity', and it is measured in kV/µs or V/ns. It is an indication of the maximum rate of change of voltage (dv/dt) which can be tolerated across the isolation barrier of the gate driver system before malfunction occurs, causing loss of control of the SiC device and erratic behavior of the system. The CMTI rating directly depends on the parasitic capacitance value across the isolation barrier.

Isolated gate driver ICs in the market use different techniques to transfer the control signal information across the isolation barrier (i.e. capacitive coupling, magnetic coupling, optical coupling, etc). In the auxiliary power supply, the energy is transferred via the magnetic field using a transformer. In both cases, a parasitic capacitance exists across the isolation barrier, and in the case of the auxiliary supply, it corresponds to the transformer's interwinding capacitance. In the previous example of the half-bridge configuration, the very high dv/dt generated during the switching transition, in addition to ringing and Miller effect turn-on issues, also causes displacement currents through the isolation barrier parasitic capacitance of the high-side gate drive circuit, between the high-voltage side and the low-voltage side, where the controller and sensitive circuitry reside (Figure 7). Note that the isolated 'ground' or 'reference' of the high-side gate driver (GND_ISO or RTN) is directly connected to the source terminal of the SiC device and, in turn, to the SW node which is subject to high dv/dt transitions. Conversely, the low-voltage 'ground' or 'reference (GND) is kept to a constant voltage (DC). The generated displacement current ($i_c(t)$) across the total isolation barrier parasitic capacitance (C_{pt}) is approximated as:

$$i_c(t) = C_{pt} \frac{dv_{ps}}{dt}$$

A too high displacement current may cause different issues in the system. In addition to distortion and delay of control signals, loss of control of the SiC device due to erratic behavior caused by high common-mode signals stressing the controller is also a possibility. The lower the isolation barrier parasitic capacitance, the lower the generated displacement current for a set dV/dt value. Said another way, a lower C_{pt} would allow a higher dV/dt value for the same displacement current. Higher dV/dt means faster switching speed, which in turn helps to achieve higher efficiency, a smaller overall solution size and a lower system cost of the power converter. Since a fast-switching speed is one of the key advantages of SiC devices, the parasitic capacitance across the isolation barrier (transformer interwinding capacitance and isolated gate driver IC) should be very low in such applications.

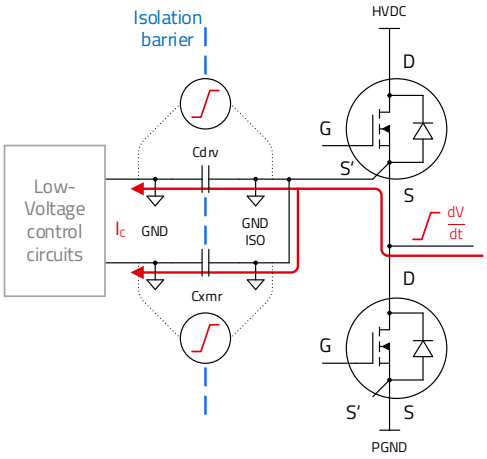

Figure 7: Displacement Currents across the isolation barrier parasitic capacitance caused by very high dV/dt in a half-bridge configuration

The WE-AGDT Transformer series from Würth Elektronik feature a very low interwinding capacitance down to 6.8 pF, helping the gate driver system to achieve CMTI ratings above 100 kV/µs.

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In addition to the functional and reliability aspects, a lower isolation barrier parasitic capacitance may also help to improve EMI performance. It should be observed that the high dv/dt is not only applied between the SW node and DC nodes like DC-Power and system ground (GND) on the PCB, but it also appears between the high dv/dt conductive nodes in the circuit board and Earth potential (to which the product chassis might be connected). This generates common-mode displacement currents across the isolation barrier parasitic capacitance, adversely affecting EMI performance. The lower the parasitic capacitance C_{pt} across the isolation barrier, the higher the impedance presented to any common-mode noise currents coupling between the HV and LV sides (see Figure 8). As a result, improved EMI performance, especially in radiated emissions frequency spectrum, as well as a lower attenuation requirement for the common mode input EMI filter can be expected.

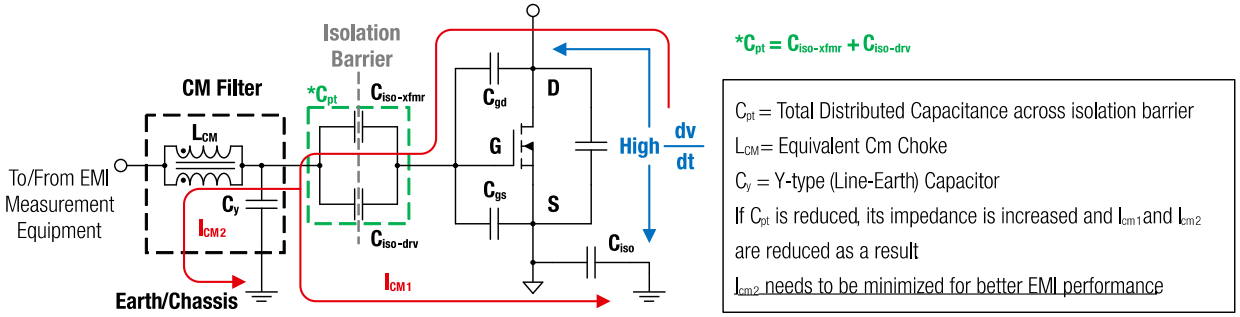

Figure 8: Simplified example of common-mode noise current coupling path for EMI considerations

For further information on SiC gate driver system considerations, please also refer to the Application note ANP082 on we-online.com/ANP082

3 Electrical Specification

	Minimum	Nominal	Maximum	Units
Input Voltage	9	12	18	(V)
Output Voltage (15V variant)	15.02	15.05	15.09 (*) / 15.5 (**)	(V)
Output Current (15V variant)	0		400	(mA)
Output Voltage (18V variant)	18.02	18.05	18.08 (*) / 18.64 (**)	(V)
Output Current (18V variant)	0		335	(mA)
Output Voltage (20V variant)	19.84	19.87	19.9 (*) / 20.79 (**)	(V)
Output Current (20V variant)	0		300	(mA)
Output Power	0		6	(W)
Switching Frequency (***)	80		360	(kHz)

Table 1. Electrical specification table

NOTE: Specification at 25 °C ambient temperature

(*) When adding a resistor on the isolated output for minimum-load current (for more info see section 7.3)

(**) When using only the clamping zener diode on the isolated output as per the BOM in sections 10 and 11

(***) Switching frequency varies with load current and input voltage

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4 Schematic

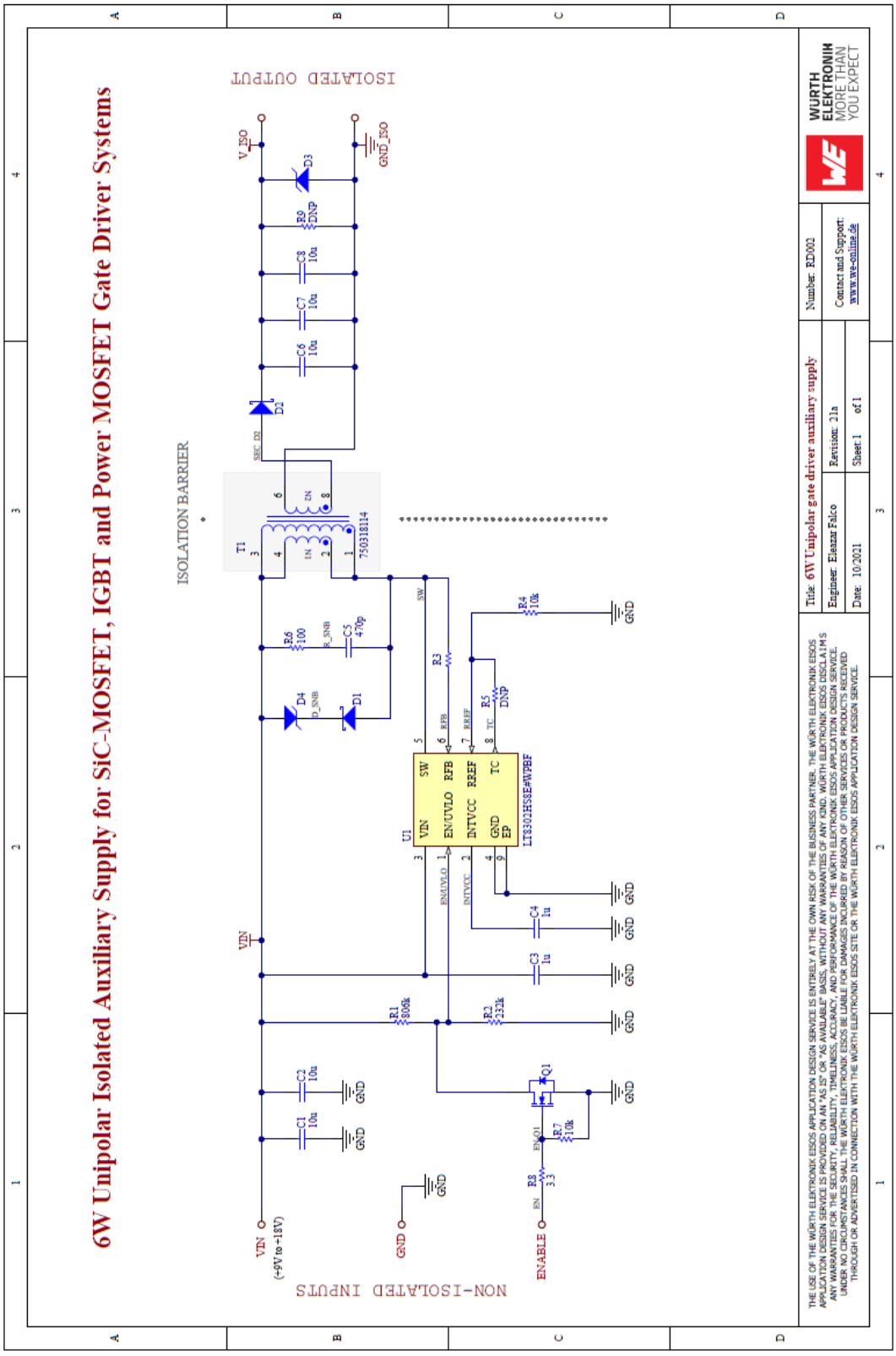

Figure 9: Schematic

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5 WE-AGDT 750318114 Transformer

Würth Elektronik has designed a new transformer for this PSR Flyback converter design, featuring optimal characteristics to drive high-performance, fast-switching SiC-MOSFET devices, and also suitable for Power MOSFETs and IGBTs alike.

Finding an optimal converter operating condition to achieve the smallest transformer size and at the same time high efficiency, good thermal performance and compliance with relevant safety standards were the key design objectives. The WE-AGDT 750318114 transformer uses a very compact EP7 assembly, 4 kV isolation voltage, overvoltage category II, pollution degree 2, fully insulated wire (FIW) and creepage/clearance distances according to standards IEC62368-1 and IEC61558-2-16. Additionally, it counts with AEC-Q200 qualification.

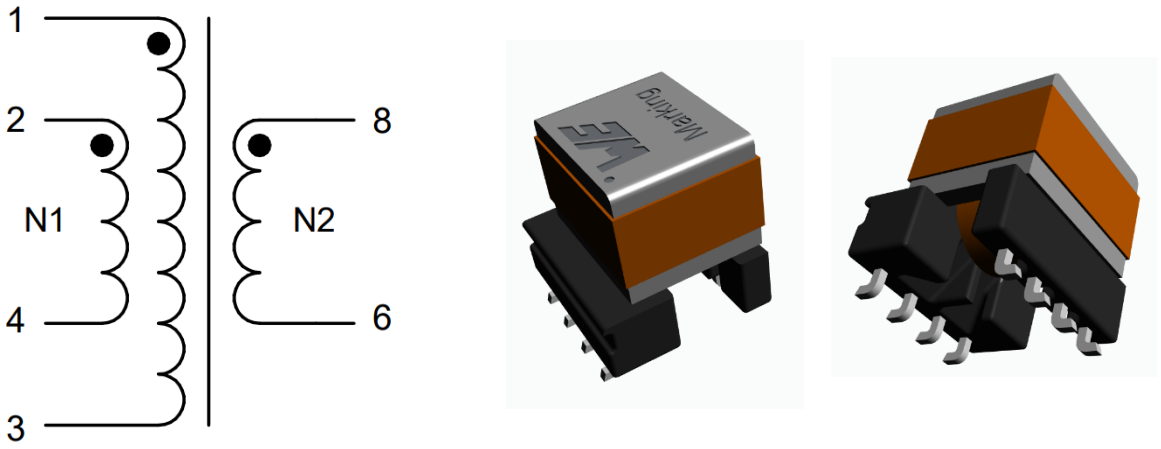

Figure 10: WE-750318114 Transformer details

Parameter	Test conditions	Value
DC resistance – primary	tie(1+2, 3+4), +20 °C	0.060 Ω ± 15%
DC resistance – Secondary	8-6, +20 °C	0.285 Ω ± 10%
Magnetizing inductance	100 kHz, 100 mV	6.00 µH ± 10%
Saturation current	20% roll-off of L_{mag}	6.2 A (typ.)
Leakage inductance	100 kHz, 100 mV	550 nH (max.)
Interwinding capacitance	100 kHz, 100 mV	6.8 pF (typ.)
Dielectric	N1 -> N2,3	4000 VAC, 1 minute
Partial discharge	1000 V_{rms}, 5 sec. 800 V_{rms} 15sec.	<10 pC
Turns ratio	(1-3):(2:4)	1:1 (±1%)
Turns ratio	(8-6):(1:3)	2:1 (±1%)
Temperature range		-40 °C / +130 °C

Table 2: WE-AGDT 750318114 transformer characteristics

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6 Board layout variants

This reference design is provided in two layout variants: a two-layer single-sided and a four-layer double-sided solution, as well as with two component assembly options: Standard and with AEC-Q qualified components.

6.1 Board layout variant A: Double-sided design

This variant is a four-layer design with all-SMD (surface mount) component assembly on top and bottom sides.

Figure 11: Board variant-A (a) top view (b) bottom view (c) dimensions

6.2 Board layout variant B: Single-sided design

This variant is a two-layer design with all-SMD (surface mount) component assembly only on top side.

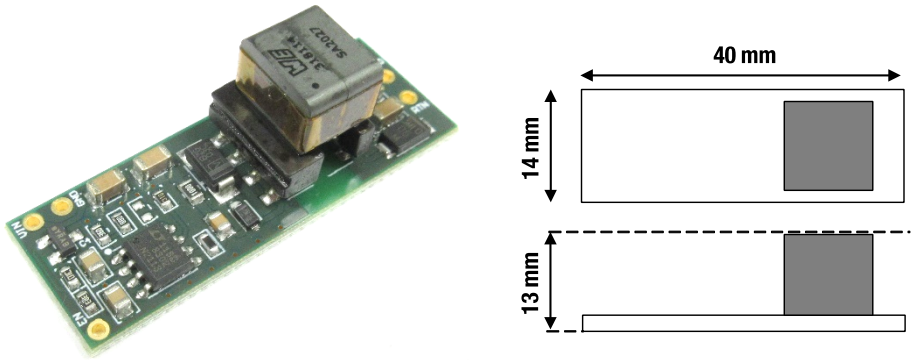

Figure 12: Board variant-B detail and dimensions overview

NOTE: No significant performance difference has been observed or can be expected between the two board layout variants, be this functional, thermal or regarding EMC behavior. The selection of the variant to use can therefore be made based only on the particular cost and mechanical constraints of the application. The compact layout lends itself optimally to integration onto a larger board together with the full gate driver system.

The PCB Layout design files (Altium Designer 21) as well as the fabrication files are available to download on we-online.com/RD002.

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7 Experimental results

7.1 Experimental test setup

The power supply has been tested for functional performance using an electronic load configured in constant-current (CC) mode. Alternatively, resistive-mode of electronic load or a discrete power resistor can also be used. Tests are carried out at 25 °C ambient temperature.

7.1.1 List of equipment required (and used in this case)

- 1 x Laboratory power supply (min. 25 V/1.5 A) (used EA-PSI 9040-40 T)
- 4 x 4-digit precision multimeter (it was used instead a Yokogawa WT3000E precision power analyzer)
- 2 x electronic loads (25 V/1 A min.) (used EA-EL 9080-45 T)
- 1 x oscilloscope (4 channel, 350 MHz or higher) (used Keysight InfiniiVision DSO-X-3034T)

7.1.2 System setup

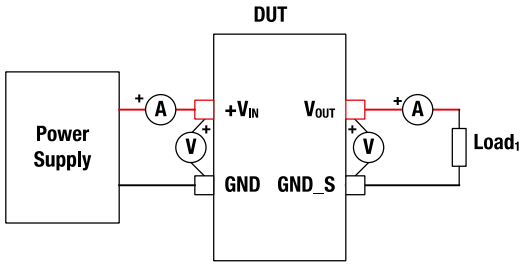

Figure 13: Example test setup

7.2 Output voltage regulation and power efficiency

The line and load regulation results show how the output voltage varies with variations in both the input voltage and output power, respectively.

7.2.1 Results for Vout = 15 V

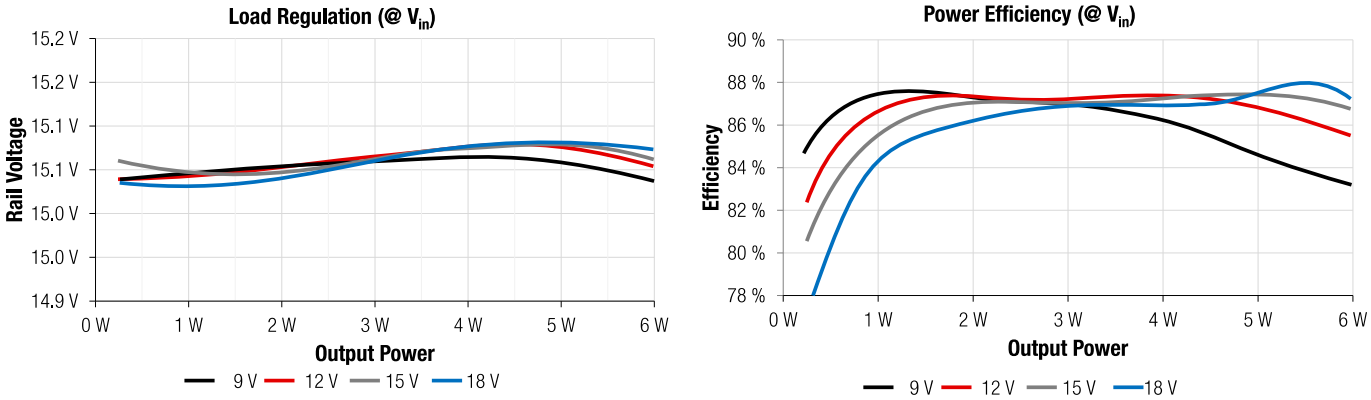

Figure 14: Load and Line Regulation (left) and Power efficieny (right) for V_{out} = 15 V variant (V_{in} = 9 V, 12 V, 15 V, 18 V)

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7.2.2 Results for Vout = 18 V

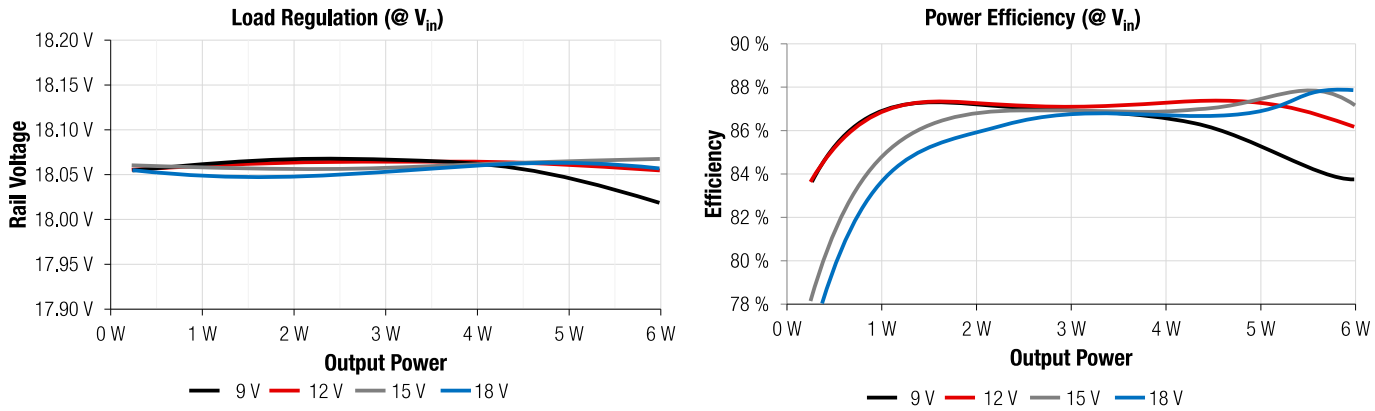

Figure 15: Load and Line Regulation (left) and Power efficieny (right) for V_{out} = 18 V variant (V_{in} = 9 V, 12 V, 15 V, 18 V)

7.2.3 Results for Vout = 20 V

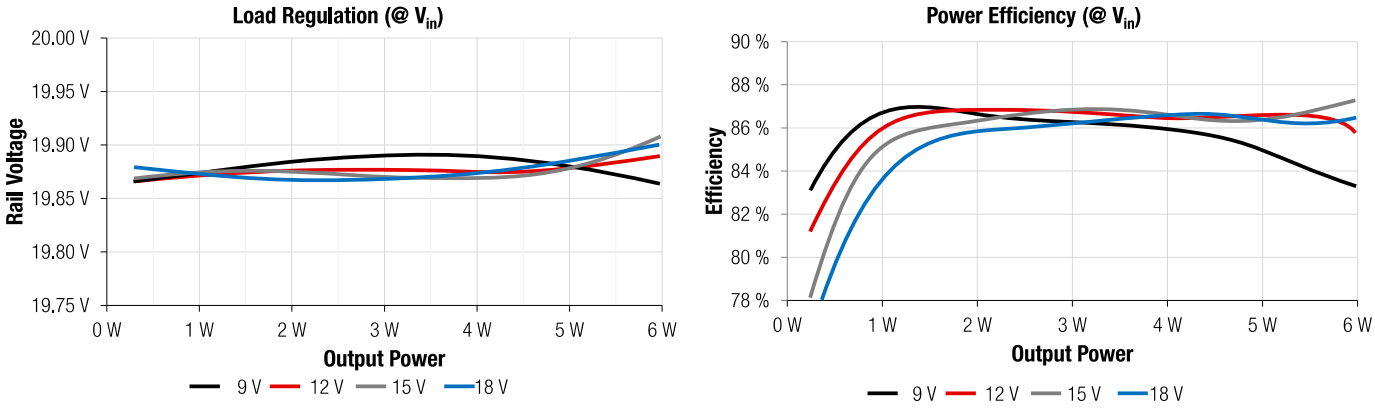

Figure 16: Load and Line Regulation (left) and Power efficieny (right) for V_{out} = 20 V variant (V_{in} = 9 V, 12 V, 15 V, 18 V)

7.3 No-load output voltage

The LT8302 IC controller requires a minimum load current in order to keep the output voltage regulated, preventing it from steadily increasing at no-load condition. No-load would be the scenario presented when the SiC-MOSFET or IGBT device is not switching. This requirement can be met by using a minimum-load resistor in the isolated output or alternatively a clamping Zener diode.

	15 V	18 V	20 V
Resistor (*)	15.02 V	18.08 V	19.88 V
Zener Diode (*) (**)	15.5 V	18.64 V	20.79 V

Table 3: Output voltage at no-load condition with minimum-load resistor or with zener diode

(*) See sections 10 and 11 (BoM variants) for details of the parts used in each case
(**) The zener diode is already included in the design for overvoltage protection, but it can additionally sink the minimum load current to clamp Vout

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8 Main waveforms, oscilloscope captures

In this section experimental results of the variant V_{out} = 15 V are shown. For the variants of V_{out} = +18 V and V_{out} = +20 V the measured results are very similar and therefore not included here.

8.1 Start-up and shut-down (@ V_{in} = 12 V and P_{out} = 6 W)

The start-up event shows a slight overshoot of the output voltage of less than 0.5 V and no ringing (Figure 17). During the shut-down event, the input capacitance supplies the energy until the voltage falls below the UVLO threshold and the controller stops switching, after which the output capacitance delivers the remaining stored energy and the output voltage falls to zero in about 1.5 ms (Figure 18). Note that the slowly rising slope of the input voltage is due to the soft-start of the laboratory power supply used.

Green: Input Voltage Pink: Output Voltage Yellow: SW Node

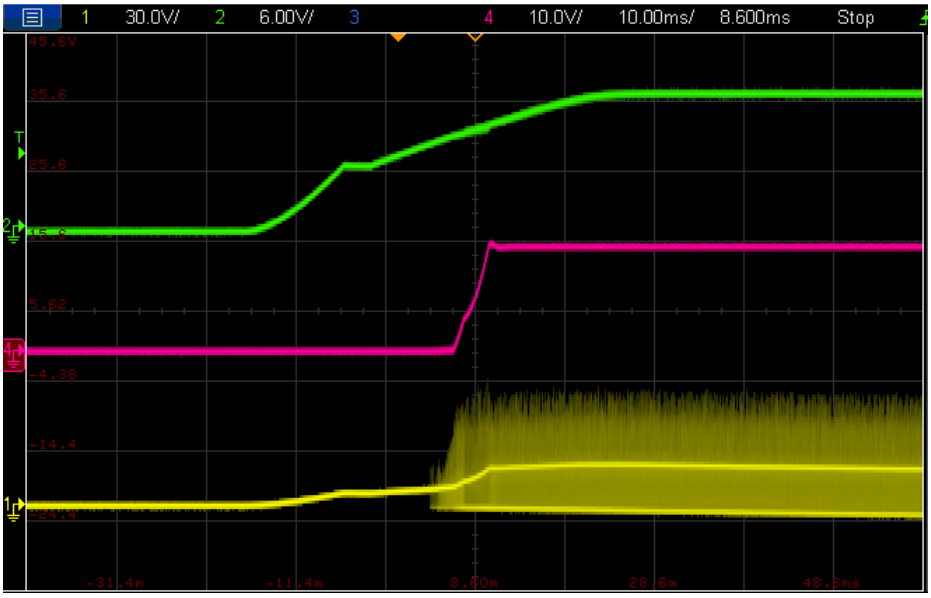


Figure 17: Start-up characteristic

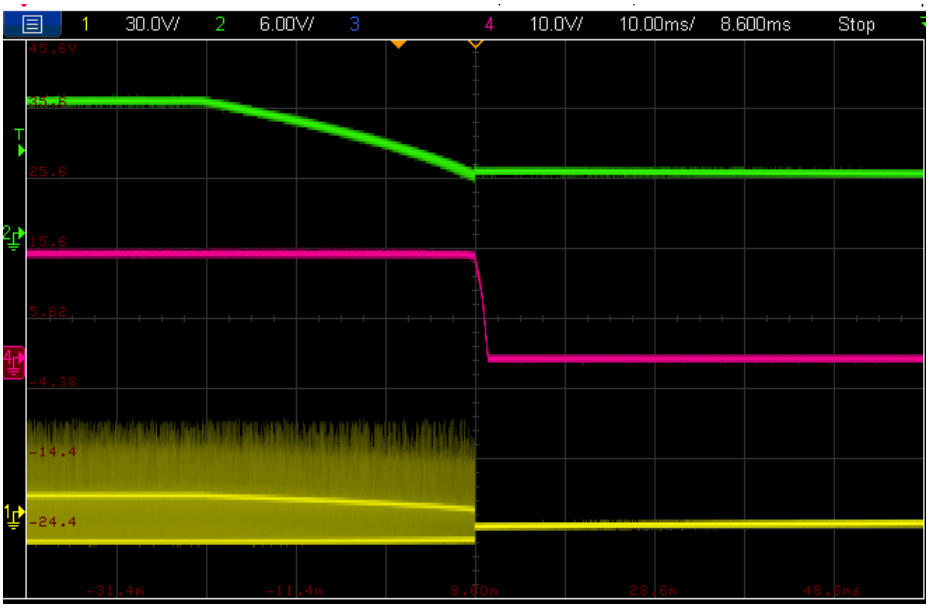


Figure 18: Shut-down characteristic

Reference Design

6 W Unipolar isolated auxiliary supply for SiC-MOSFET & IGBT gate driver

8.2 Steady-state operation

8.2.1 Operation mode with load power

Below are shown the transformer primary current and SW node voltage waveforms for 1 W and 6 W loads. At light load, the Flyback auxiliary supply will operate in discontinuous conduction mode (DCM) (Figure 19), whereas as the output power increases, the dynamic peak current limit increases accordingly eventually reaching boundary conduction mode operation (BCM) (Figure 20). Note that the converter does not operate in continuous conduction mode (CCM), since the current needs to fall to zero each cycle in order for the IC controller to sample and regulate the output voltage.

Pink: Transfomer Primary Current **Blue:** SW Node

Figure 19: 1 W load (DCM operation)

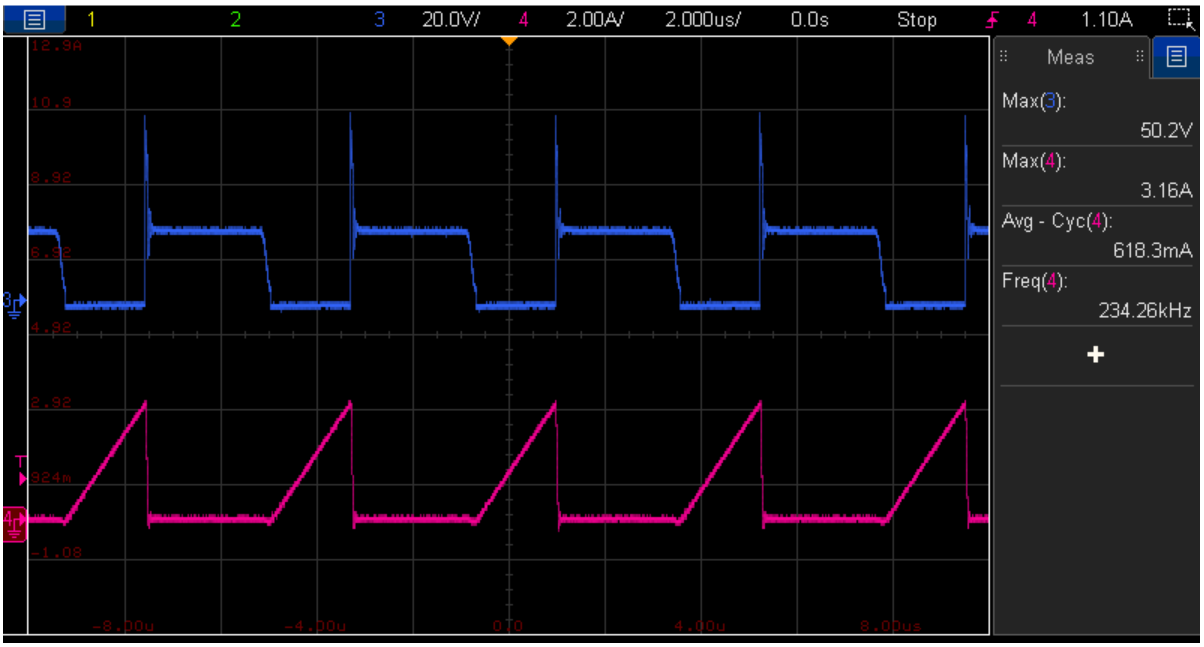


Figure 20: Full load (6 W) (BCM operation)

Reference Design

6 W Unipolar isolated auxiliary supply for SiC-MOSFET & IGBT gate driver

8.2.2 SW node clamping and damping snubbers

The SW node voltage must be kept under 65 V (LT8302 integrated MOSFET rating) and any ringing appearing after the MOSFET turns OFF must be fully damped before 250 ns after the switching event in order for the LT8302 to correctly sample and regulate the output voltage. The worst-case condition for maximum peak voltage clamping is at the maximum input voltage (18 V) and full-load (6 W). Regarding ringing damping, the worst-case corresponds to the minimum input voltage (9 V) and also full-load (6 W) (i.e. highest input current). Oscilloscope captures below under full-load (6 W) show maximum SW node voltage of 54.1 V and ringing fully damped before 200 ns, which not only meets the requirements, but also provides additional headroom to account for the impact of part-to-part tolerances and operating temperature deviations.

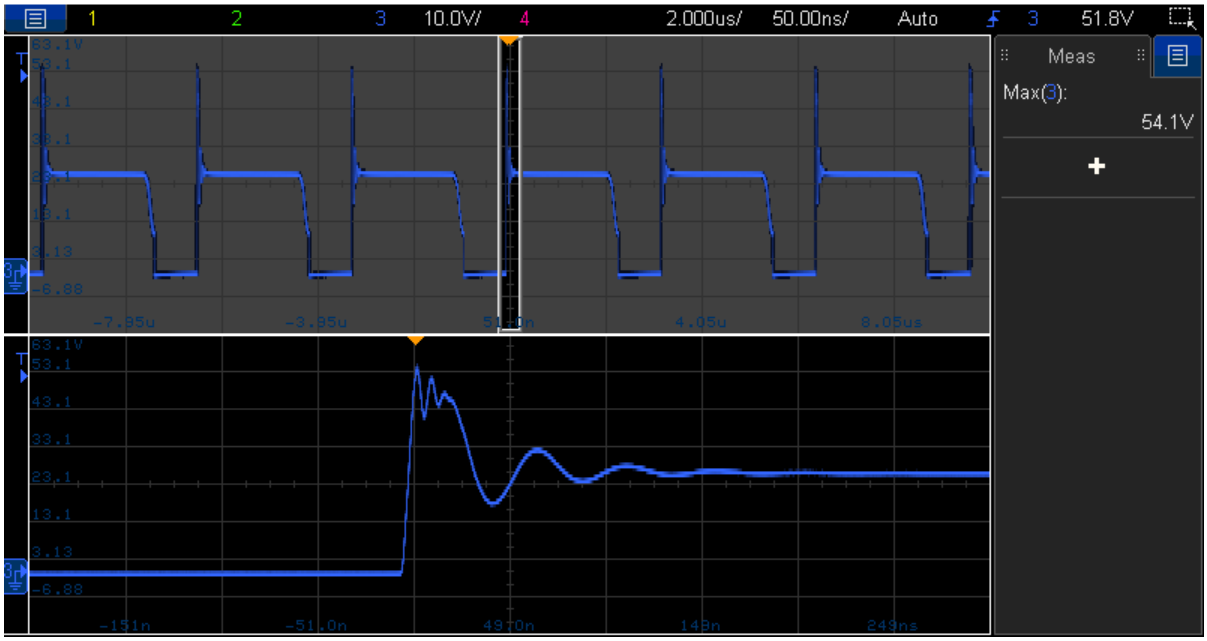


Figure 21: SW Node voltage clamping (V_{in} = 18 V, P = 6 W)

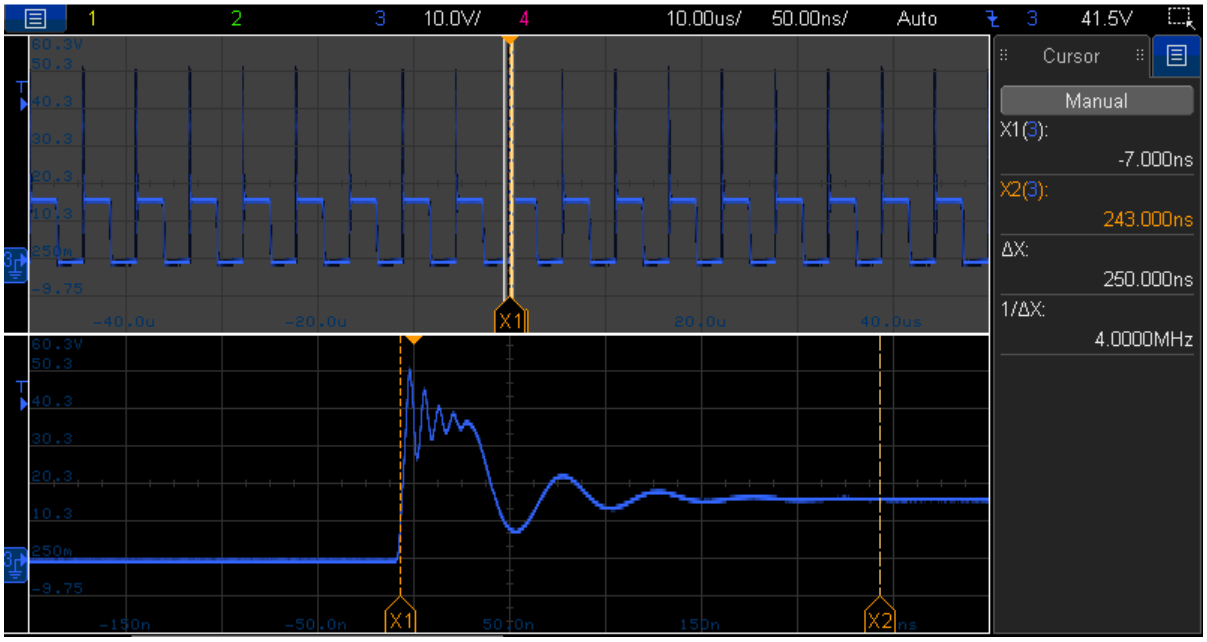


Figure 22: SW Node ringing damping (V_{in} = 9 V, P = 6 W)

Reference Design

6 W Unipolar isolated auxiliary supply for SiC-MOSFET & IGBT gate driver

8.2.3 Input and output Voltage ripple (at full load)

An input voltage ripple amplitude of around 235 mV (peak-to-peak) is observed, which corresponds to around 2% of the nominal input voltage (figure 23). The output voltage ripple is 130 mV, less than 1% of the nominal output voltage. Additional capacitance can be added to the input or output rails in order to reduce the ripple amplitude if desired.

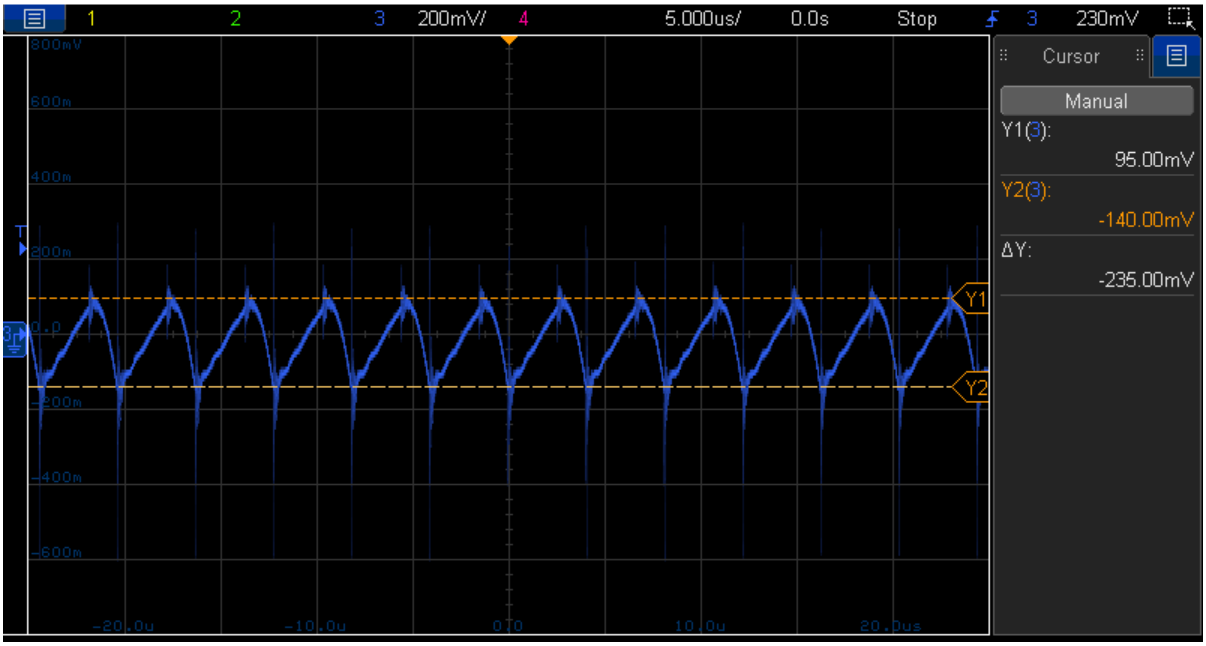


Figure 23: ΔV_{in} (at 12 V_{in}, 6 W)

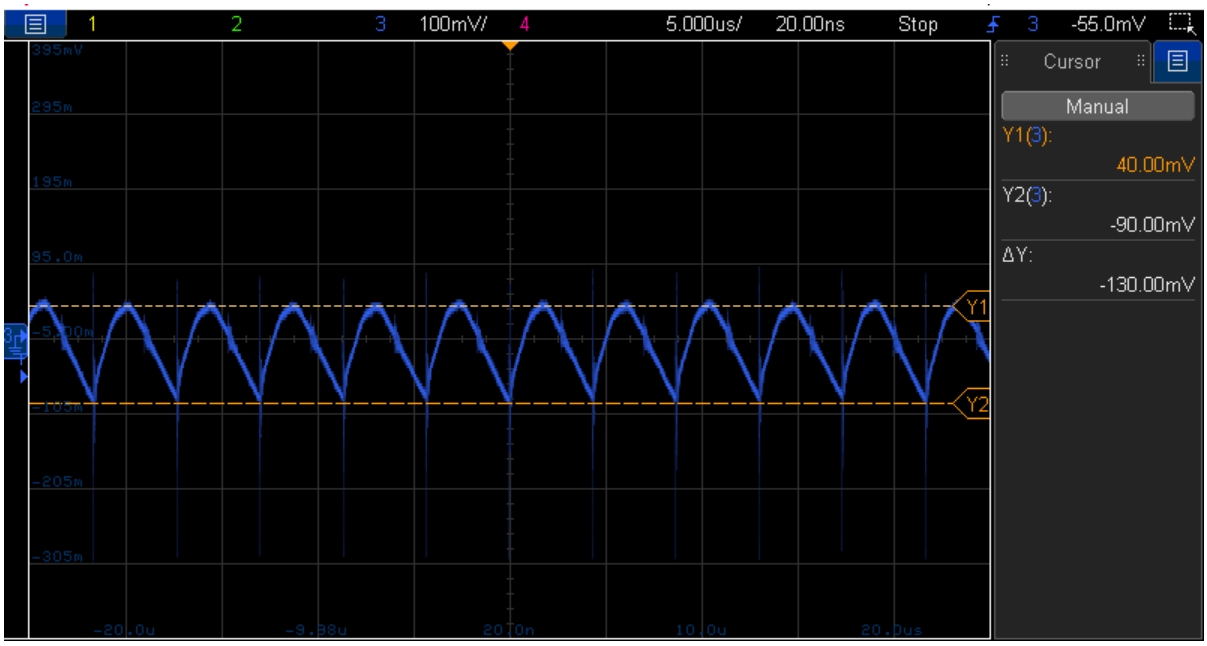


Figure 24: ΔV_{out} (at 12 V_{in}, 6 W)

Reference Design

6 W Unipolar isolated auxiliary supply for SiC-MOSFET & IGBT gate driver

9 Thermal performance

Thermal performance results over the full-load range (0 to 6 W) and at minimum input voltage (V_{in} = 9 V) representing worst-case condition are shown in this section. The results correspond to layout Variant-B board with V_{out} = 15 V. Note that the thermal performance of PCB layout variant A and the other output voltage variants did not show important differences (i.e. more than 5 ˚C temperature variations).

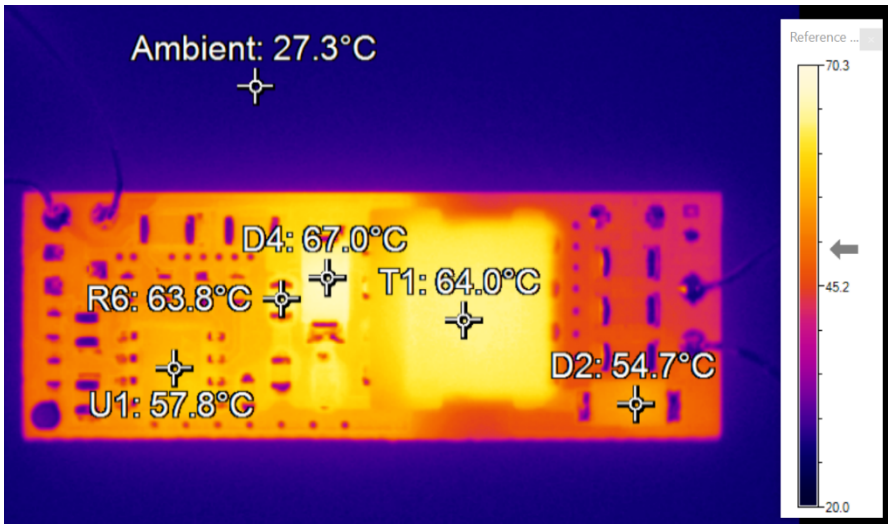


Figure 25: Board components temperature at V_{in} (min) = 9 V (worst-case) and 25 to 28 °C ambient

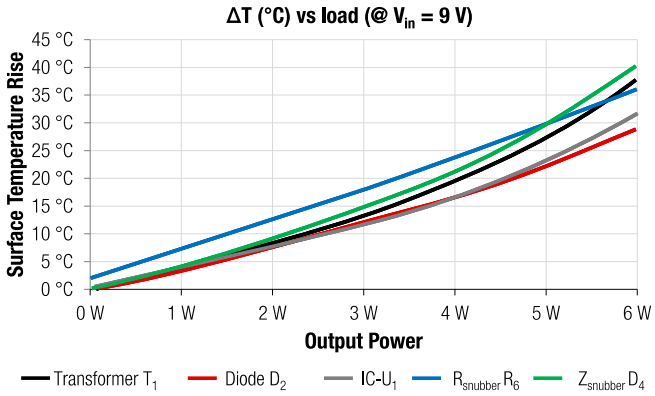


Figure 26: Temperature rise at V_{in} (min) = 9 V (worst-case)

Based on the above results, in order to keep internal/junction component temperatures within maximum ratings, it is recommended not to exceed a maximum ambient temperature of 85 °C (max) under operation for longer lifetime and higher reliability of the application.

If this ambient temperature is exceeded, the output power must be reduced (de-rated) accordingly.

Reference Design

6 W Unipolar isolated auxiliary supply for SiC-MOSFET & IGBT gate driver

10 Bill-of-Materials (BoM) Option 1: Standard

Bill-of-materials for the +15 V variant is shown in table 4. The component variations for the +18 V and +20 V versions are shown below.

Reference designator	Description	Package	Manufacturer	MPN
C1, C2, C6, C7, C8	MLCC 10uF 50V X5R 10%	1206	Würth Elektronik	885012108022
C3, C4	MLCC 1uF 50V X7R 10%	0805	Würth Elektronik	885012207103
C5	MLCC 470pF 50V X7R 10%	0805	Würth Elektronik	885012207084
D1	Barrier Schottky Rectifier 1 A, 100 V	µSMP	Vishay	V1PM10-M3H
D2	Barrier Schottky Rectifier 3A, 100 V	DO-221AC	Vishay	VSSAF3M10-M3
D3 (*)	Zener 15.25-16.04V, 0.5 W	DO-219AC	Vishay	PLZ16B-G3H
D4	Zener 27 V, 3 W	SMA	Vishay	BZG03C27-M3H
R1	Thick Film, 806k, 0.1 W, 1 %	0603	Yageo	RC0603FR-07806KL
R2	Thick Film, 232k, 0.1 W, 1 %	0603	Yageo	RC0603FR-07232KL
R3 (*)	Thin Film, 71.5k, 0.1 W, 0.1 %	0603	Yageo	RT0603BRD0771K5L
R4	Thin Film, 10k, 0.1 W, 0.1 %	0603	Yageo	RT0603BRD0710KL
R5 (DNP)	N/A	0603	N/A	N/A
R6	Thick Film, 100, 0.5 W, 5 %	0805	Bourns	CMP0805-FX-1000ELF
R7	Thick Film, 10k, 0.1 W, 1 %	0603	Yageo	RC0603FR-0710KL
R8	Thick Film, 3.3, 0.1 W, 1 %	0603	Yageo	RC0603FR-073R3L
R9 (*) (opt)	Thick Film, 5.6k, 0.25 W, 1%	0603	Panasonic	ERJ-UP3F5601V
Q1	MOSFET N-channel, 40 V	SOT23-3	Vishay	SQ2318AES-T1_BE3
U1	PSR Flyback Controller 65V 4.5A	SO-8	Analog Devices	LT8302HS8E#PBF
T1	Transformer 6uH, 6.2A, 7.5pF AEC-Q200	EP-7	Würth Elektronik	750318114

Table 4: Bill-of-Materials (BoM) for V_{out} = +15 V. Option 1: Standard

(*) For V_{out} = 18 V variant, use:

D3	Zener 18.02-18.96 V, 0.5 W	DO-219AC	Vishay	PLZ20A-G3H
R3	Thin Film, 85.6k, 0.1 W, 0.1 %	0603	KOA Speer	RN73H1JTD8562B25
R9 (opt)	Thick Film, 8.2k, 0.25 W, 1%	0603	Panasonic	ERJ-UP3F8201V

Table 5: Component variation for V_{out} = +18 V. Option 1: Standard

(*) For V_{out} = 20 V variant, use:

D3	Zener 20.15-21,20 V, 0.5 W	DO-219AC	Vishay	PLZ22A-G3H
R3	Thin Film, 94.2k, 0.1 W, 0.1 %	0603	Yageo	RT0603BRD0794K2L
R9 (opt)	Thick Film, 10k, 0.25 W, 1%	0603	Bourns	CMP0603-FX-1002ELF

Table 6: Component variation for V_{out} = +20 V. Option 1: Standard

Reference Design

6 W Unipolar isolated auxiliary supply for SiC-MOSFET & IGBT gate driver

11 Bill-of-Materials (BoM) Option 2: AEC-Q qualified components

Bill-of-materials for the +15 V variant is shown in table 7. The component variations for the +18 V and +20 V versions are shown below.

Reference designator	Description	Package	Manufacturer	MPN
C1, C2, C6, C7, C8	MLCC 10uF 50V X7R 10% AEC-Q200	1206	TDK	CGA5L1X7R1H106K160AC
C3, C4	MLCC 1uF 50V X7R 10% AEC-Q200	0805	Murata	GCM21BR71H105KA03L
C5	MLCC 470pF 50V X7R 10% AEC-Q200	0805	Kemet	C0805S471K5RACAUTO
D1	Barrier Rectifier 1 A, 100 V AEC-Q101	µSMP	Vishay	V1PM10-HM3
D2	Barrier Schottky Rectifier 3 A, 100 V AEC-Q101	DO-221AC	Vishay	VSSAF3M10-HM3
D3 (*)	Zener 15.25-16.04V, 0.5 W, AEC-Q101	DO-219AC	Vishay	PLZ16B-HG3/H
D4	Zener 27 V, 3 W, AEC-Q101	SMA	Vishay	BZG03C27-HM3
R1	Thick Film, 806k, 0.1 W, 1 %, AEC-Q200	0603	Yageo	AC0603FR-07806KL
R2	Thick Film, 232k, 0.1 W, 1 %, AEC-Q200	0603	Yageo	AC0603FR-07232KL
R3 (*)	Thin Film, 71.5k, 0.1 W, 0.1 %, AEC-Q200	0603	Panasonic	ERA-3AEB7152V
R4	Thick Film, 10k, 0.1 W, 0.1 %, AEC-Q200	0603	Panasonic	ERA-3ARB103V
R5 (DNP)	N/A	0603	N/A	N/A
R6	Thick Film, 100, 0.5 W, 5 %, AEC-Q200	0805	Vishay-Dale	CRCW0805100RJNEAHP
R7	Thick Film, 10k, 0.1 W, 1 % AEC-Q200	0603	Yageo	AC0603FR-0710KL
R8	Thick Film, 3.3, 0.1 W, 1 % AEC-Q200	0603	Yageo	AC0603FR-073R3L
R9 (*) (opt)	Thick Film, 5.6k, 0.25W, 1% AEC-Q200	0603	Panasonic	ERJ-PA3F5601V
Q1	MOSFET N-channel, 40 V, AEC-Q101	SOT23-3	Vishay	SQ2318AES-T1_GE3
U1	PSR Flyback Controller 65V 4.5A AEC-Q200	SO-8	Analog Devices	LT8302HS8E#WPBF
T1	Transformer 6uH, 6.2A, 7.5pF AEC-Q200	EP-7	Würth Elektronik	750318114

Table 7: Bill-of-Materials (BoM) for V_{out} = +15 V, option 2: AEC-Q qualified components

(*) For V_{out} = 18 V variant, use:

D3	Zener 18.02-18.96 V, 0.5 W, AEC-Q101	DO-219AC	Vishay	PLZ20A-HG3H
R3	Thin Film, 85.6k, 0.1 W, 0.1 %, AEC-Q200	0603	KOA Speer	RN73H1JTTD8562B25
R9	Thick Film, 10k, 0.25W, 1% AEC-Q200	0603	Panasonic	ERJ-PA3F8201V

Table 8: Component variation for V_{out} = +18 V, option 2: AEC-Q qualified components

(*) For V_{out} = 20 V variant, use:

D3	Zener 20.15-21,20 V, 0.5 W, AEC-Q101	DO-219AC	Vishay	PLZ22A-HG3H
R3	Thin Film, 94.2k, 0.1 W, 0.1 %, AEC-Q200	0603	KOA Speer	RN73H1JTTD9422B25
R9	Thick Film, 10k, 0.25W, 1% AEC-Q200	0603	Panasonic	ERJ-UP3J103V

Table 9: Component variation for V_{out} = +20 V, option 2: AEC-Q qualified components

Reference Design

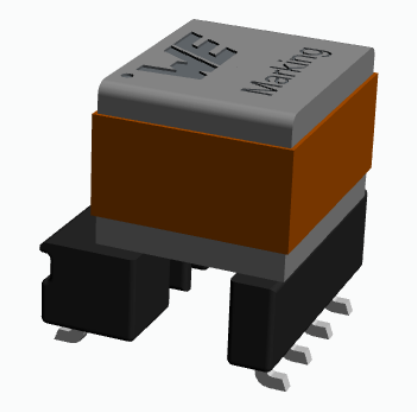
6 W Unipolar isolated auxiliary supply for SiC-MOSFET & IGBT gate driver

12 WE-AGDT series

The WE-AGDT (Auxiliary Gate Drive Transformer) transformers from Würth Elektronik are each optimized for its corresponding reference design. They provide bipolar (+15 V / -4 V, +19V / -4V, +20V / -5V) as well as unipolar (15 to 20 V; 0 V) options, with input voltage ranging from 9 to 36 V and maximum output power of 3 to 6 W. They are optimized for SiC-based applications, but they are also suitable for driving IGBT and power MOSFETs alike, and even high-voltage GaN-FETs with an additional output regulation stage.

Characteristics

- Interwinding capacitance as low as 6.8 pF typical
- Flyback with primary side regulation
- High efficiency and very compact. Surface mount EP7
- Common control voltages for SiC MOSFET & IGBT
- Wide range input voltages 9 to 36 V
- Safety: IEC62368-1 /IEC61558-2-16
- Basic insulation
- Dielectric insulation up to 4 kV
- Temperature class B
- Reference designs with TI and ADI controllers



Applications

Industrial drives, AC motor inverters, electric vehicle powertrain, battery chargers, solar inverters, data centers, uninterruptible power supplies, active power factor correction, switching power supplies with SiC-MOSFETs.

Order code	V_{in} range (V)	V_{out1} (V)	V_{out2} (V)	C_{w_w} (pF)	Frequency max (kHz)	IC Reference Design	Power (W)
750317893	9 – 18	15 – 20	-	6.8	350	LM5180	3
750317894	9 – 18	+15	-4	7.5			
750318207	18 – 36	15 – 20	-	8.2			5
750318208	18 – 36	+15	-4	7.0			
750318114	9 – 18	15 – 20	-	6.8		LT8302	6
750318131	9 – 18	+15	-4	7			
750319497	9 – 18	+19	-4	7			
750319496	9 – 18	+20	-5	7			

Table 10: WE-AGDT transformer series

Reference Design

6 W Unipolar isolated auxiliary supply for SiC-MOSFET & IGBT gate driver

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