Agenda

08:30 – 09:00		*Arrival / Registration / Coffee*
09:00 – 09:50		SMPS Topologies, tips and tricks (Analog Devices)
09:50 – 10:45		Filtering Considerations for DC/DC Converters (Wurth Electronics)
10:45 – 11:10		*Coffee Break & Networking Opportunity*
11:10 – 12:00		The Art of Loop Compensation (Wurth Electronics)
12:00 – 13:00		*Lunch*
13:00 – 13:50		LTspice Examples (Analog Devices)
13:50 – 14:45		Smart Selection of Inductors and Capacitors (Wurth Electronics)
14:45 – 15:10		*Coffee Break & Networking Opportunity*
15:10 – 16:00		PCB Board Layout Optimisation (Analog Devices)

ANALOG DEVICES

WÜRTH ELEKTRONIK
MORE THAN YOU EXPECT

PCB Board Layout Optimization

Fons Janssen
Field applications engineer

Agenda

Noise generated in switch mode power supplies

Noise coupling mechanisms

Magnetic self shielding

Example for electric coupling

Where the return current flows

Grounding

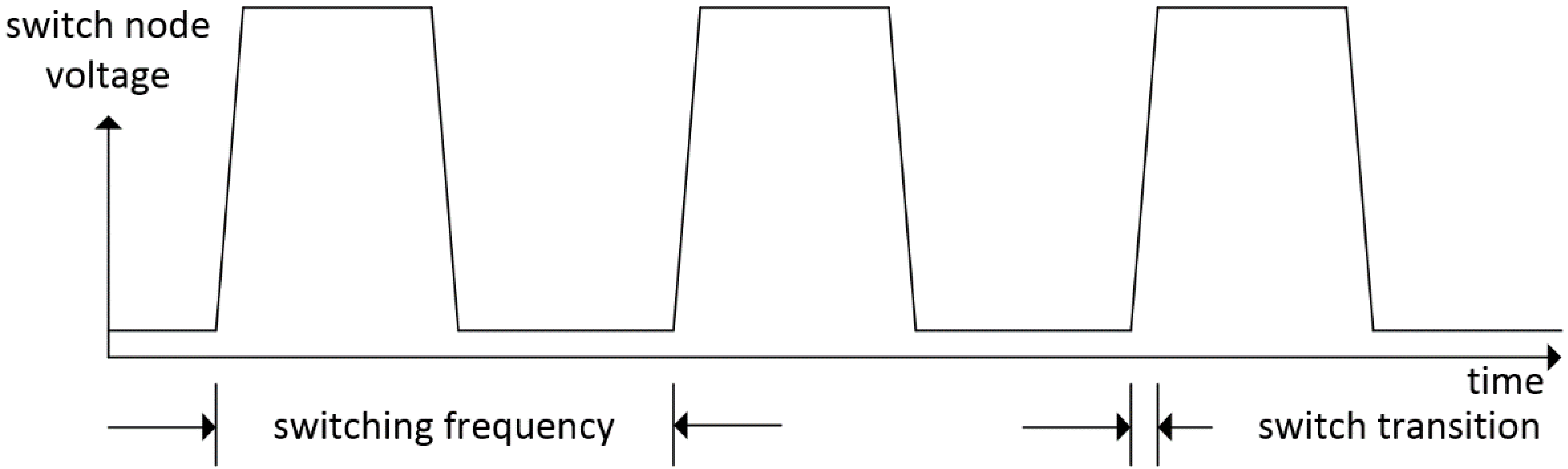
Examples

Multiple power supplies

PCB Layers

Kelvin sensing

Noise generated by a switch mode power supply

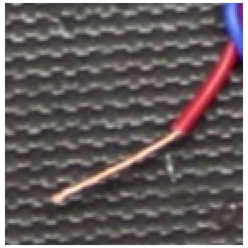


Switching frequency typically **500kHz** to **3MHz**

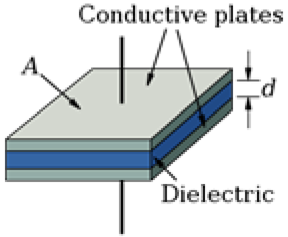
Switching transition typically **10MHz** to **200MHz** (100ns to 5ns)

The four different types of noise coupling

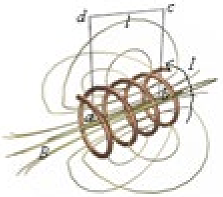
Conductive



Near field electric (capacitive)



Near field magnetic (transformer)



Far field electromagnetic (radio)

Conductive coupling

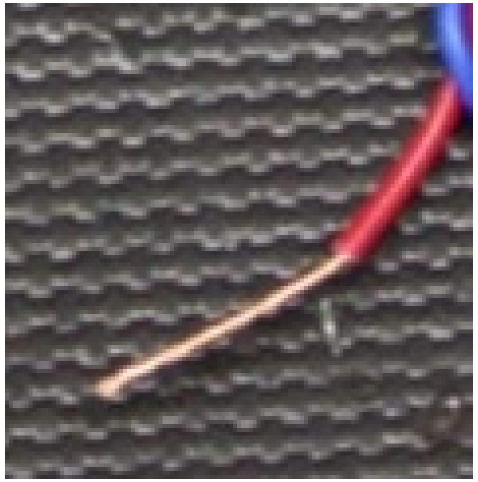
Same impedance

Requires two or more conductive contacts

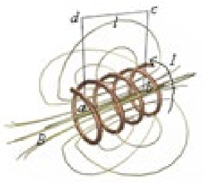
Most noise issues associated with conductive coupling

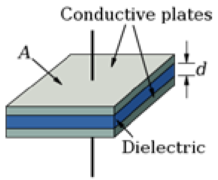
Typical examples:

- Shared signal path
- GND connections
- AC or DC power leads



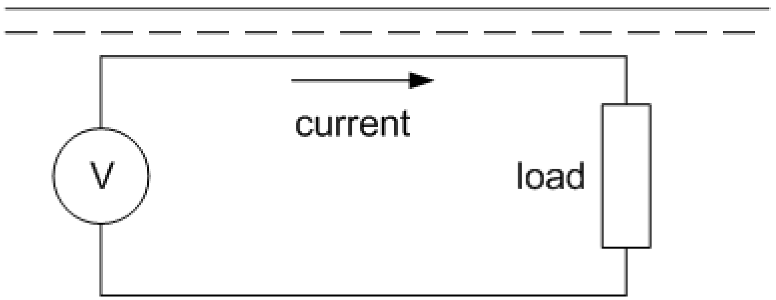
Near Field Coupling





Electric (E-field) or Magnetic (H-field) coupling

- Current causes H-field
- Voltage causes E-field



Solid line on top is picking up noise

Dotted line is protective trace with fixed potential:

- GND, Vin, amplified signal…

To find out if Electric or Magnetic coupling:

- Disconnect the load. If noise issue still exists, then coupling is electric field (E) type

Magnetic self shielding

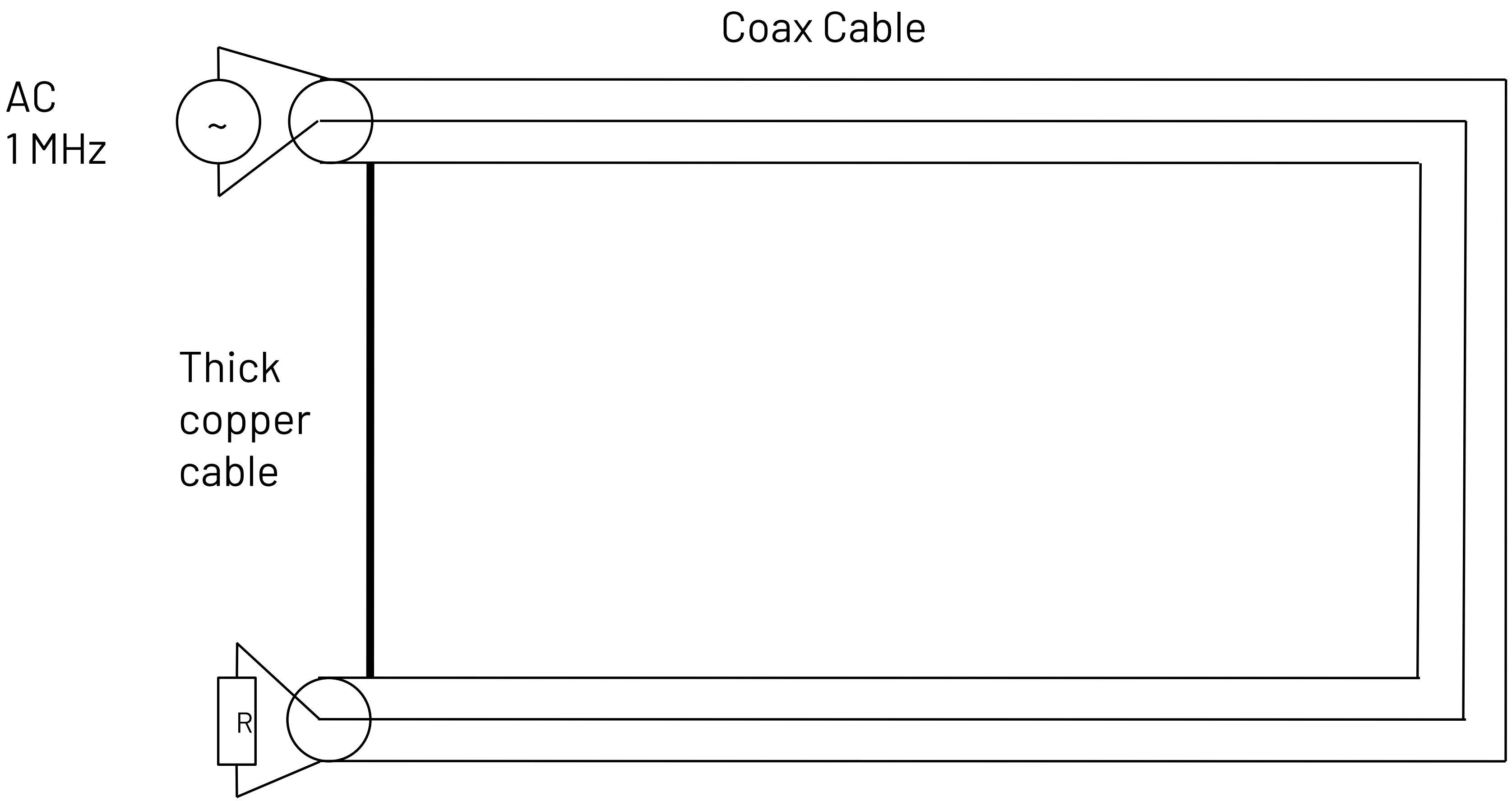
Measures to reduce trace inductance will also reduce magnetic fields

Bad field containment

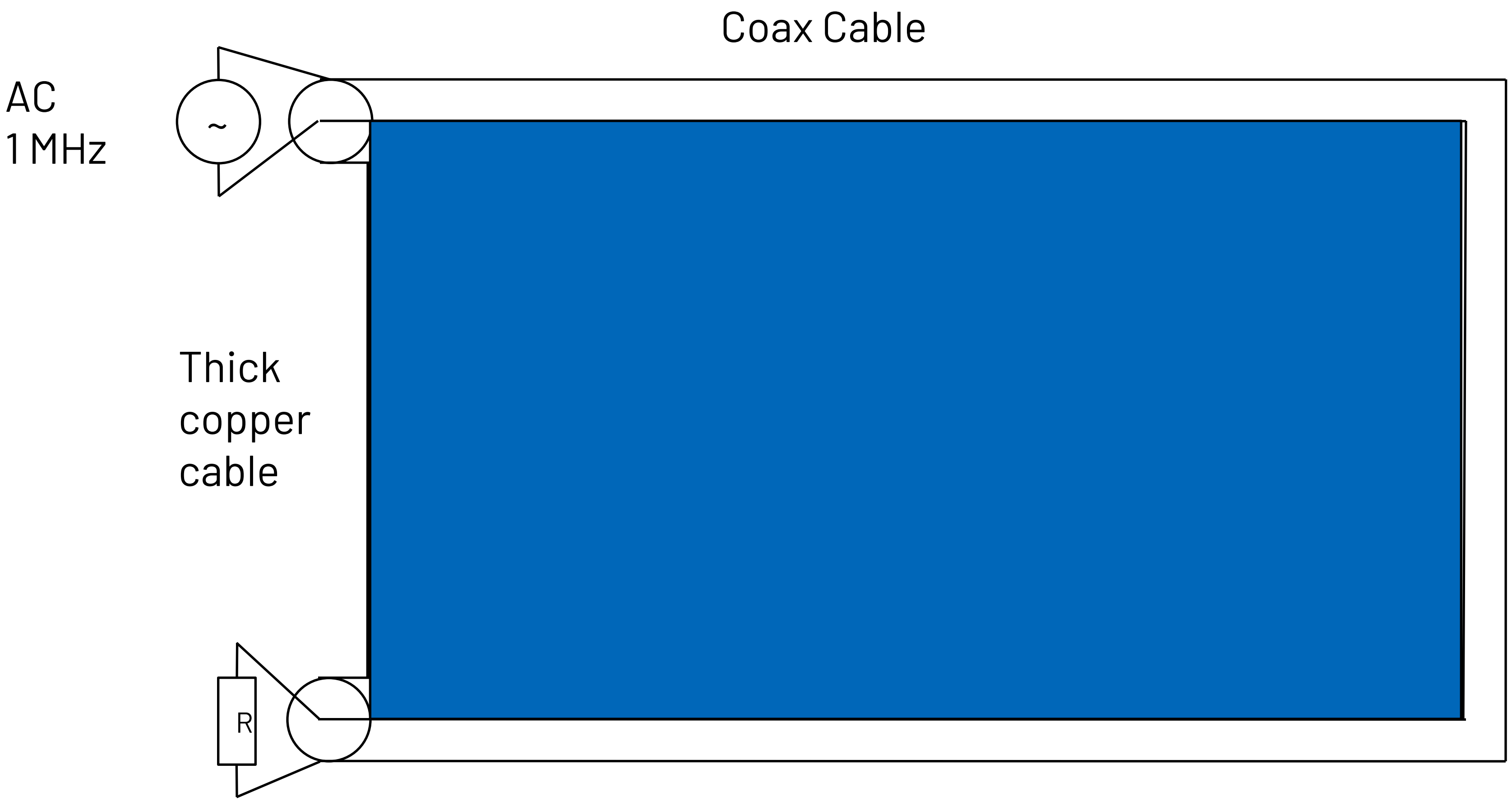
Good field containment

If the return path of the current completely encloses the current such as with a coax cable, very good field containment!

Where does the return current flow?



Where does the return current flow?



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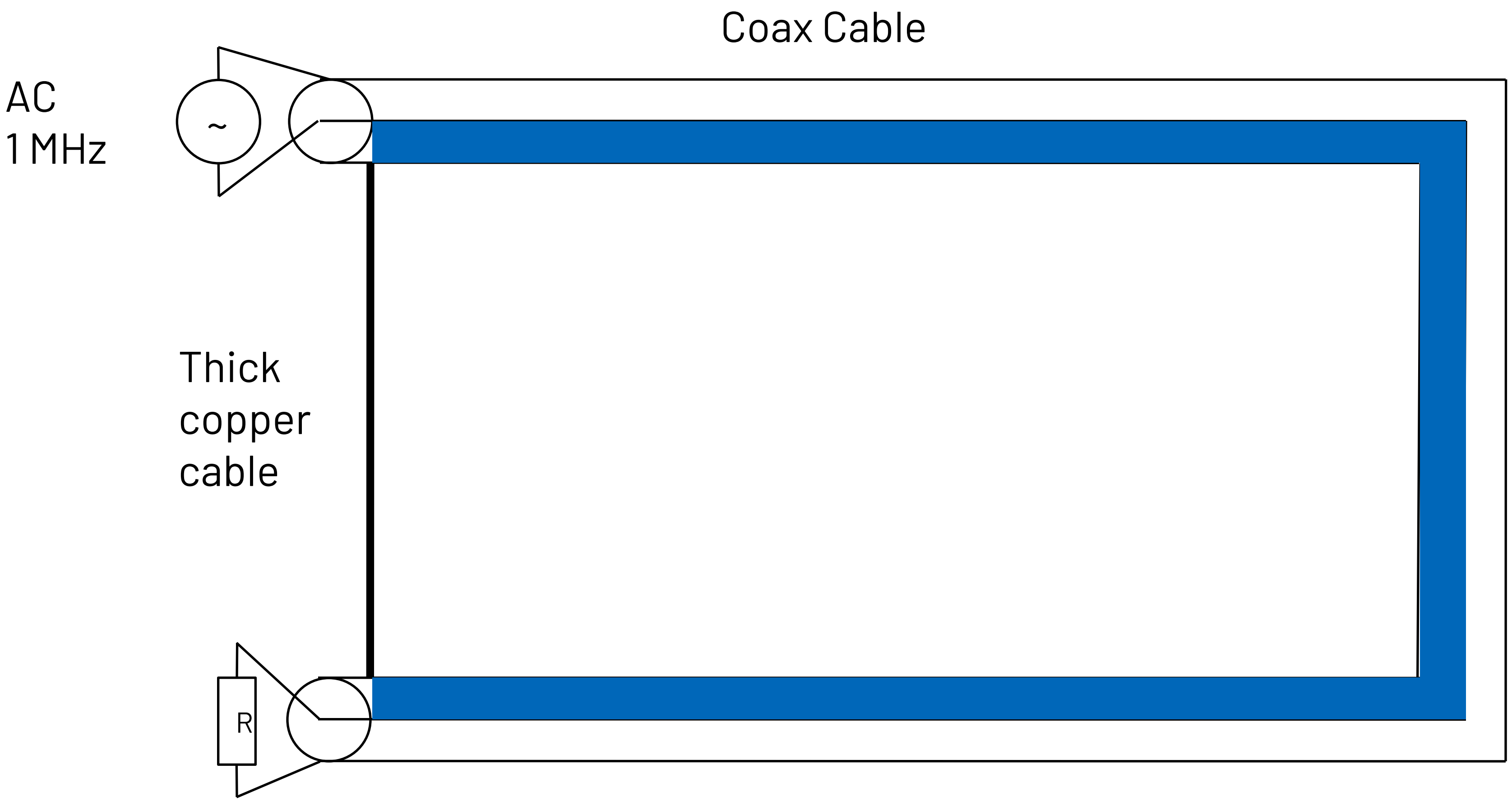
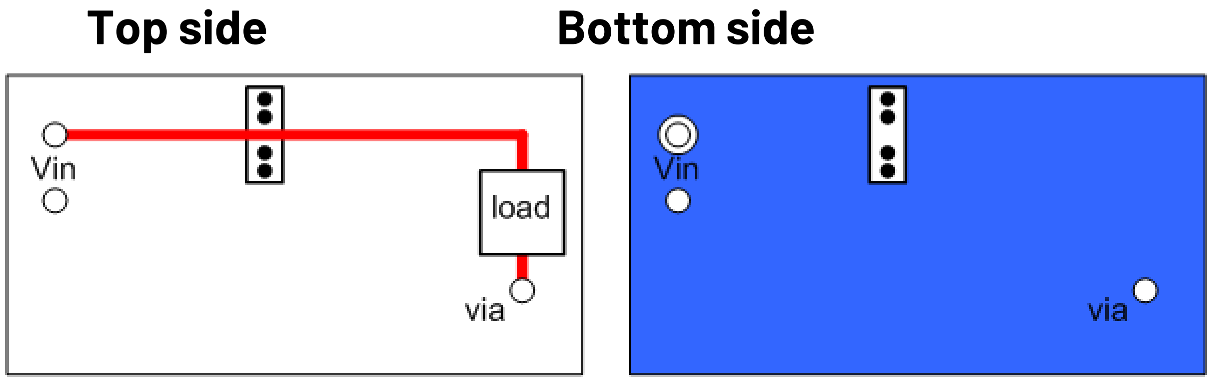


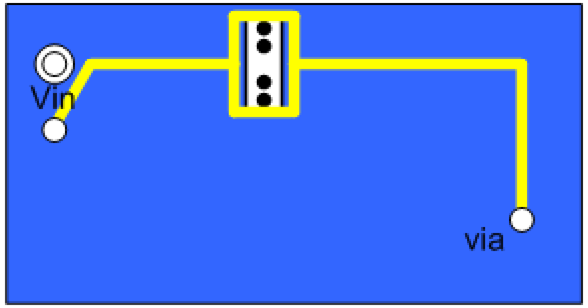
Know the return paths
How not to build hidden antennas

Two layer board with ground plane used for return currents

- Four dot component is through hole component (connector…)



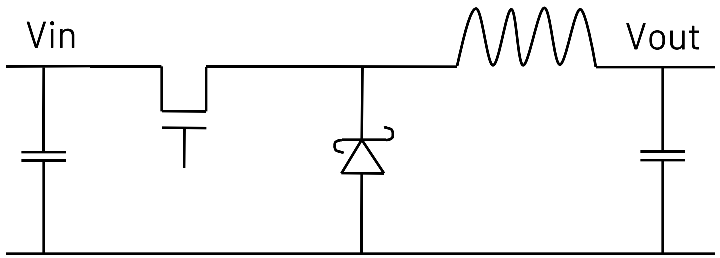
Return AC current flow:



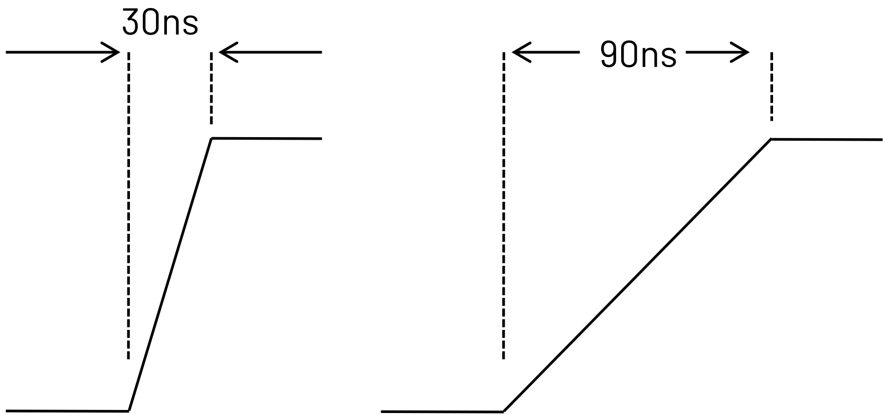
Gap will radiate at frequency defined by gap length

Layout, a very important ‘external’ component

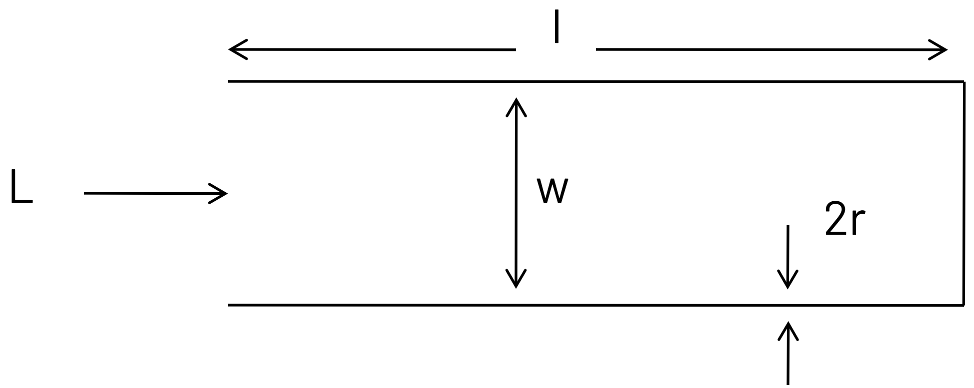
Basic Buck Topology



Switch Transition



Inductance of a conductor



$$L = \frac{MagneticFlux}{Current}$$

$$L = \frac{\mu l}{\pi}\left(\ln\frac{w}{r}\right)$$

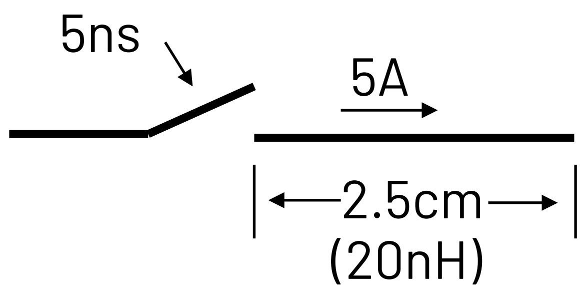
If l>>w>>r

Influence on Inductance:

- L increases as loop area increases
- L decreases as wire thickness increases

Voltage Offset due to fast Switch Transitions
Parasitic Inductance is our enemy

2.5cm of PCB trace has about 20nH of trace inductance

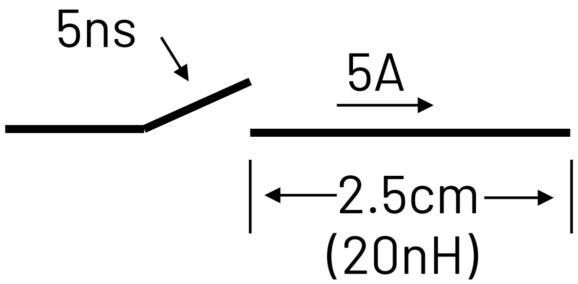


$$V = L\left(\frac{di}{dt}\right)$$

With switch transitions of 5ns, 2.5cm board trace length and 5A of current:

Voltage Offset due to fast Switch Transitions
Parasitic Inductance is our enemy

2.5cm of PCB trace has about 20nH of trace inductance

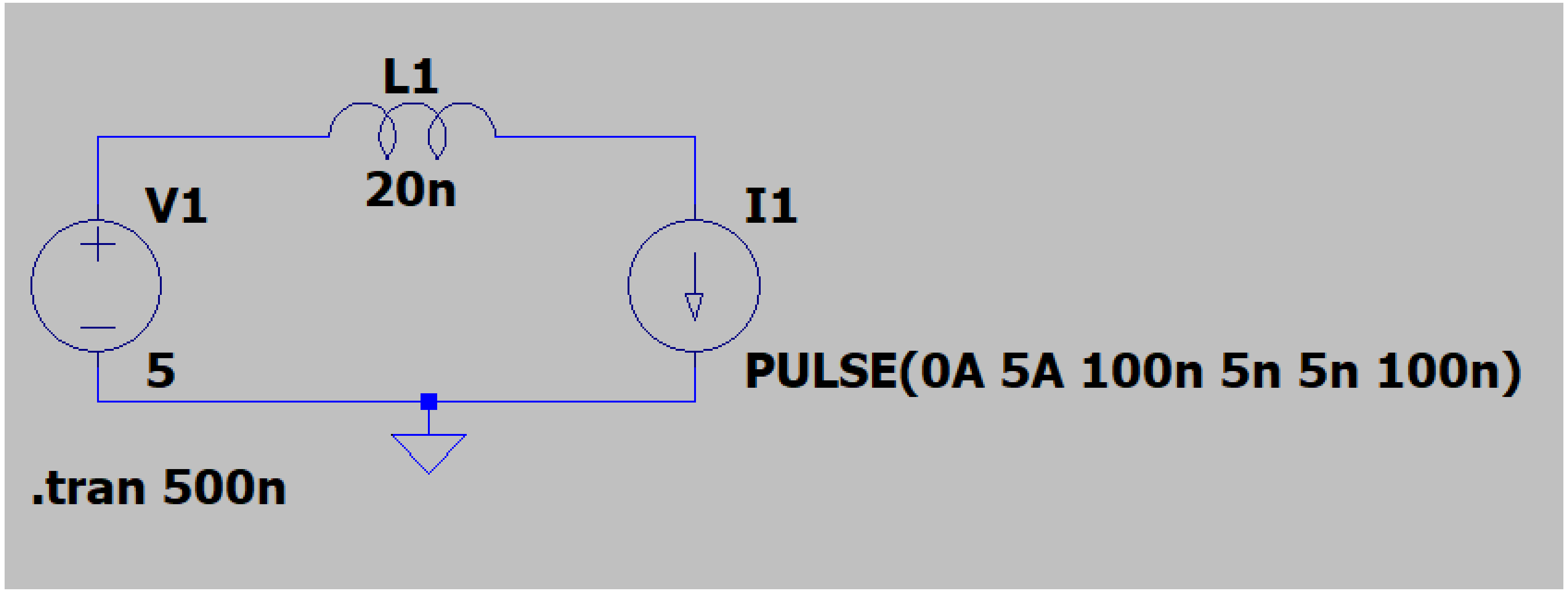


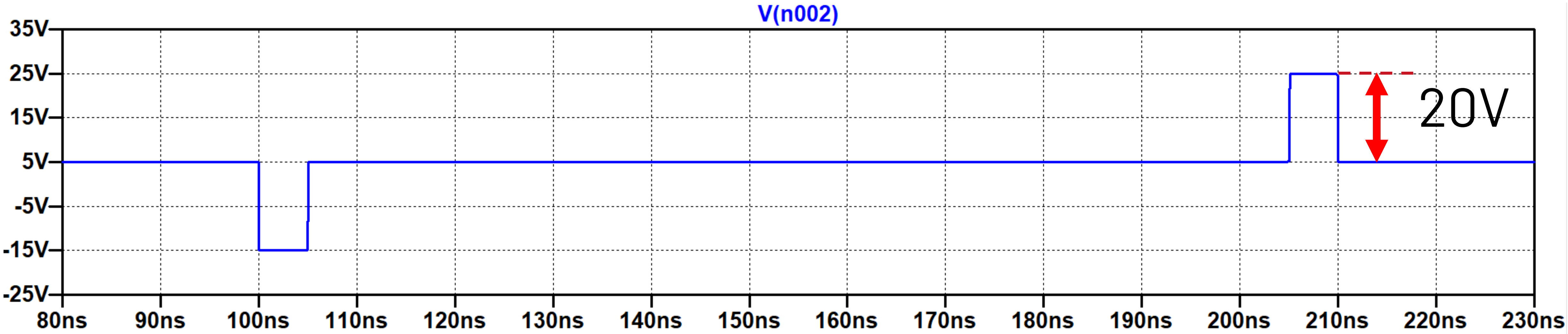
$$V = L\left(\frac{di}{dt}\right)$$

With switch transitions of 5ns, 2.5cm board trace length and 5A of current:

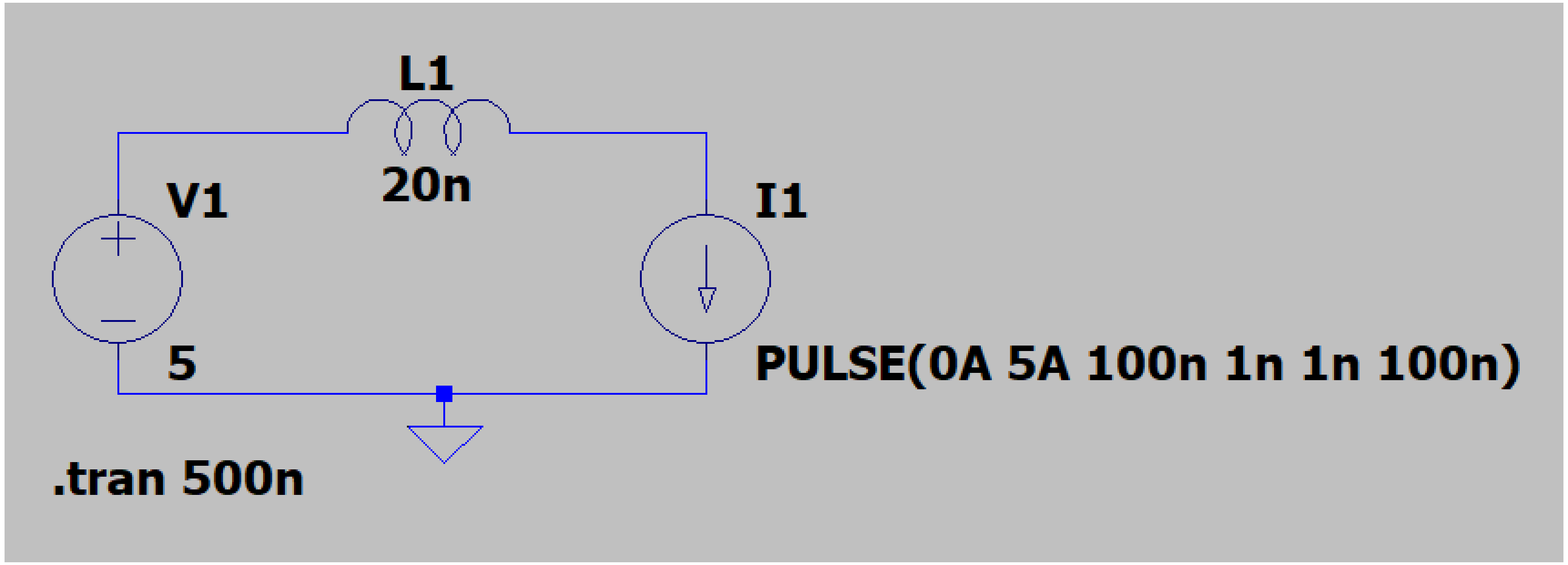
V = 20nH (5A/5ns) = 20V

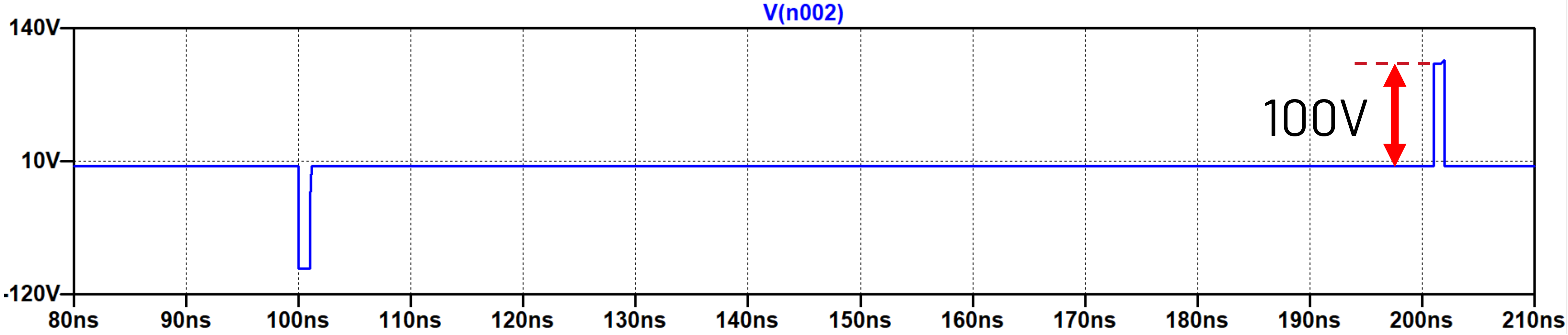
LTspice example, 20nH, 5A, 5ns





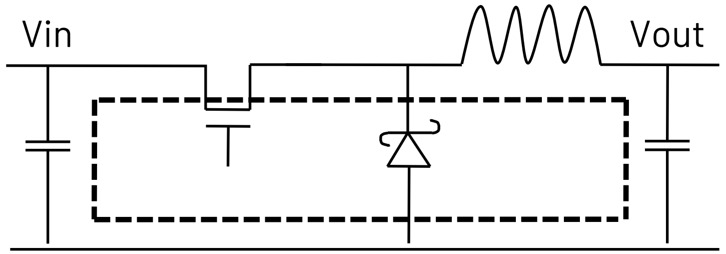
LTspice example, 20nH, 5A, 1ns



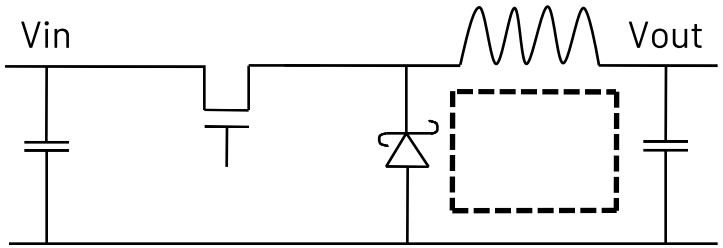


What are hot loops? Example Buck Regulator

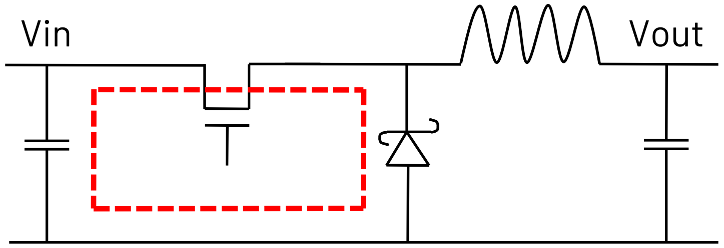
Current flow during on-time:



Current flow during off-time:



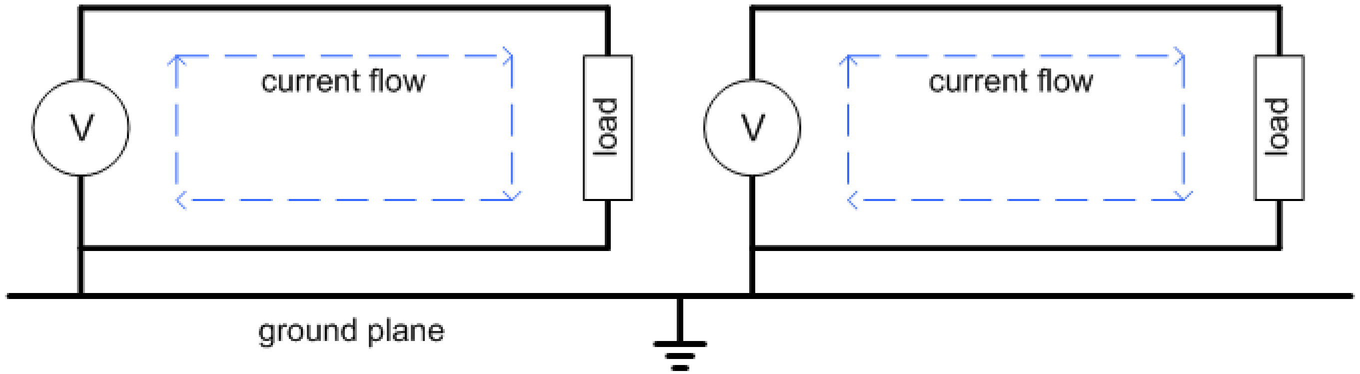
AC traces:



Keep AC traces as short as possible...(ASAP)

Ground Plane

For low noise, return signal directly and do not dump in GND plane



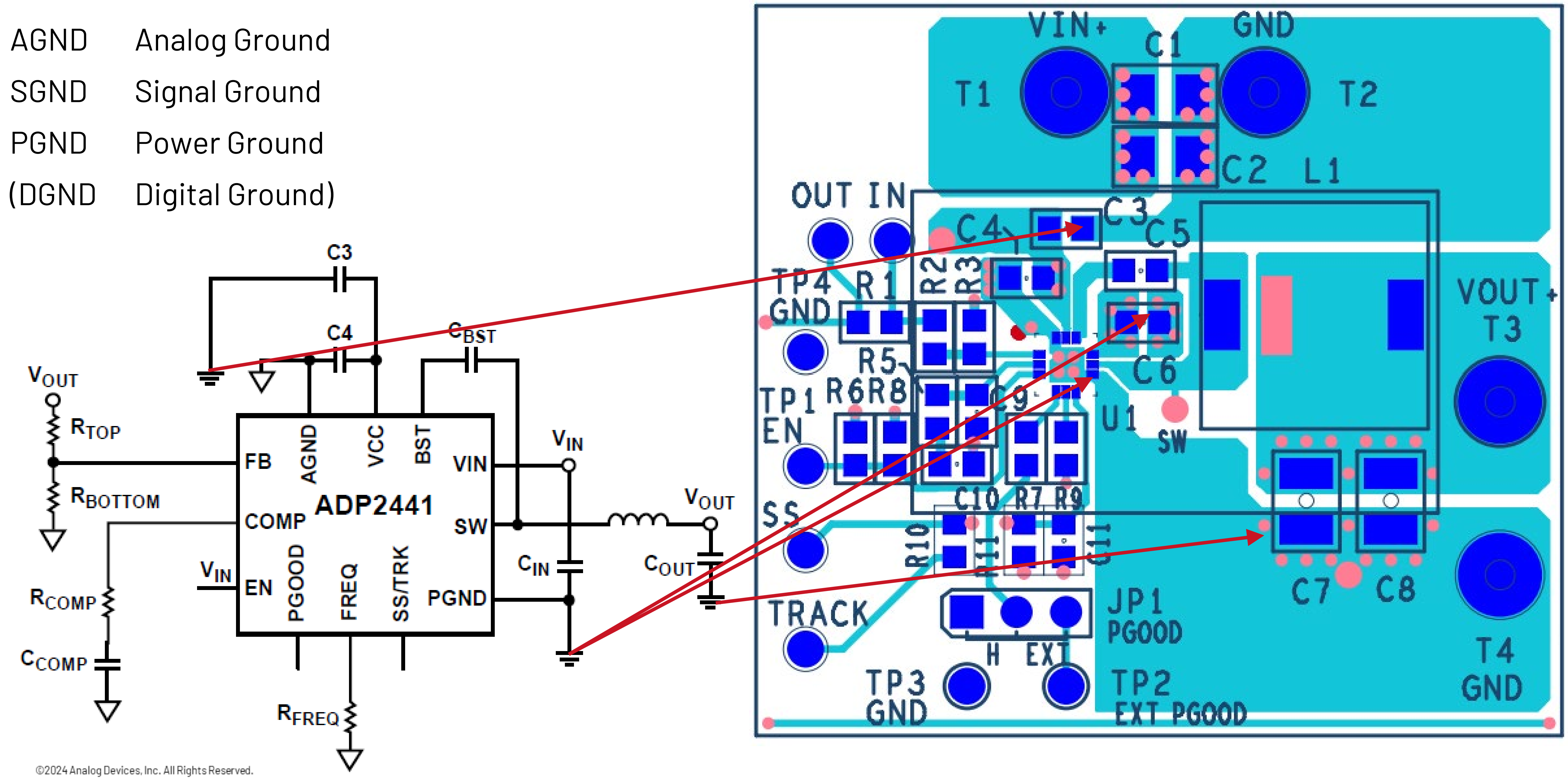
GND plane is intended as GND voltage reference only

If there are no currents flowing through the plane and if it is low impedance, it will be very clean

GND plane is used for shielding purposes

Grounding AGND / SGND / PGND

AGND	Analog Ground
SGND	Signal Ground
PGND	Power Ground
(DGND	Digital Ground)



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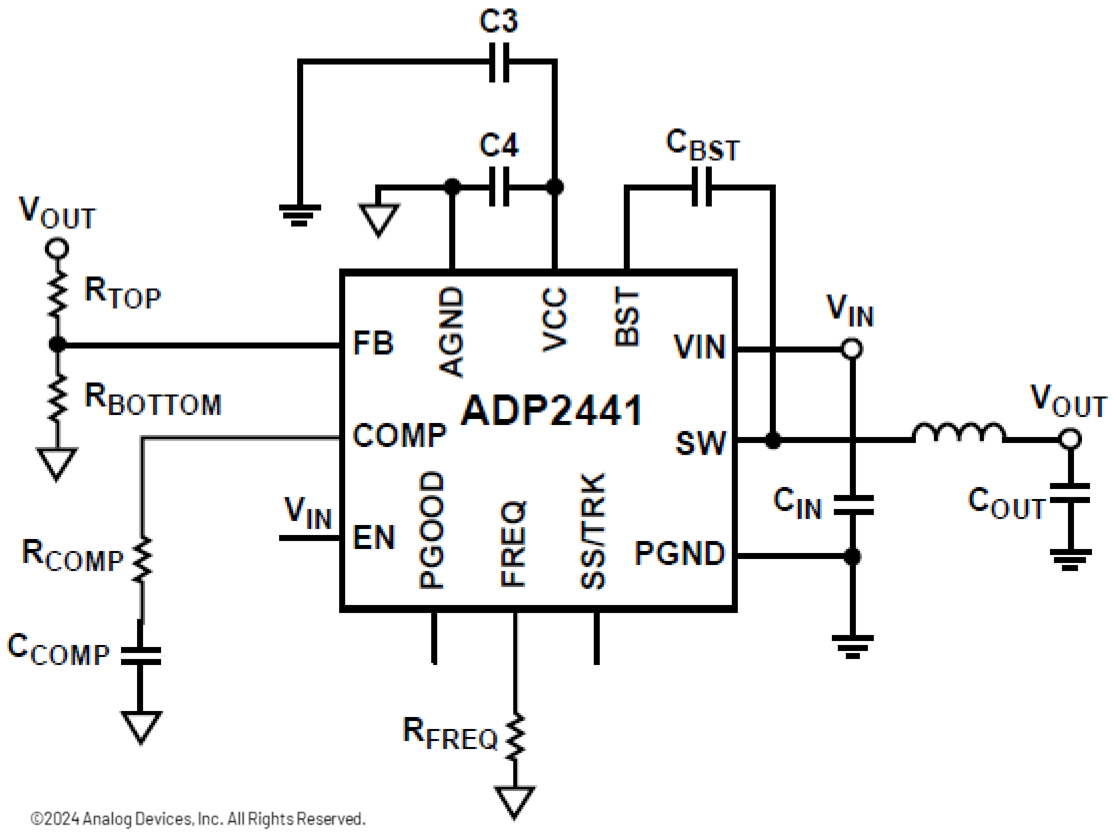
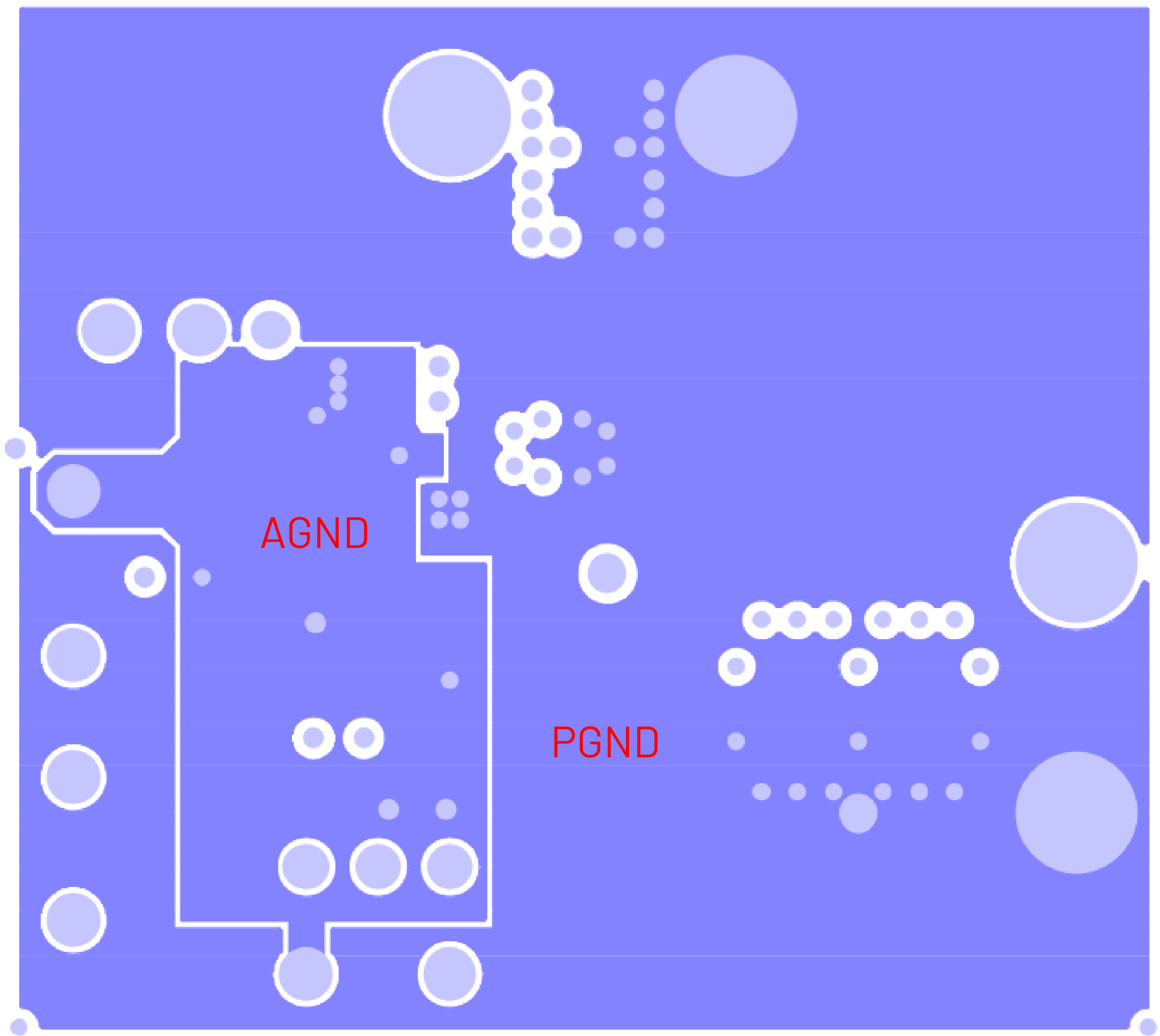
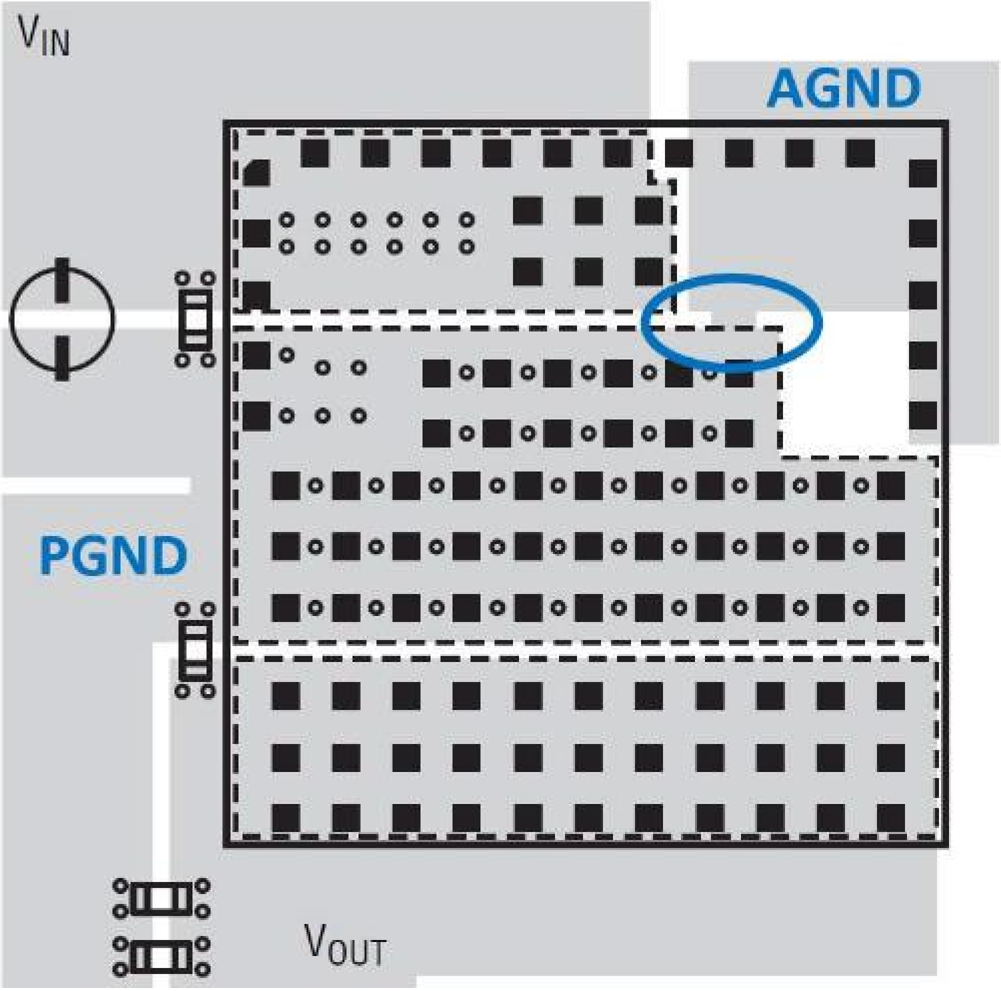
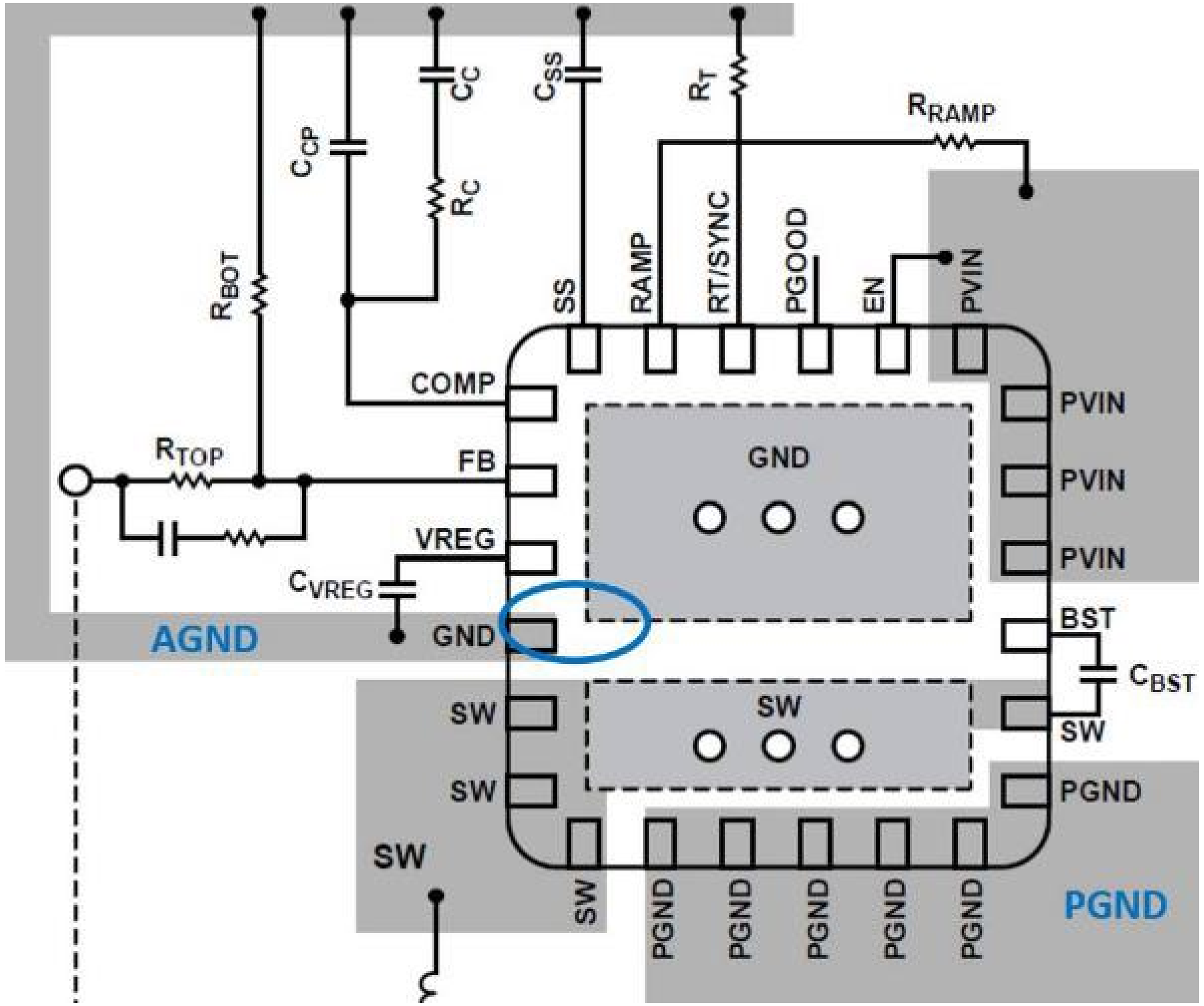




Example of close GND connection

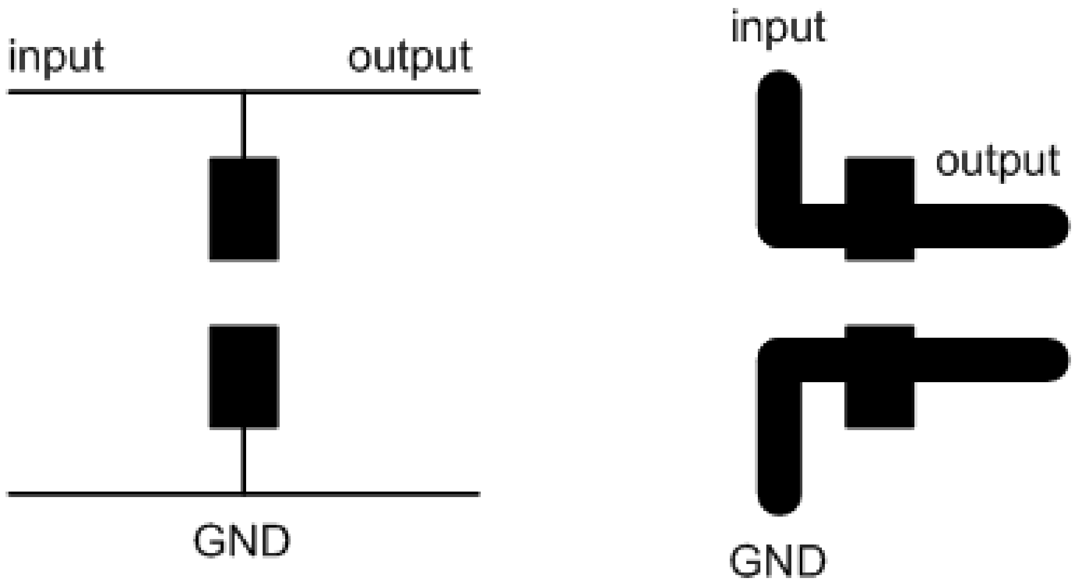


Example of separated GND connection



Bypassing techniques

For bypassing capacitors, layout is very important



very bad

good

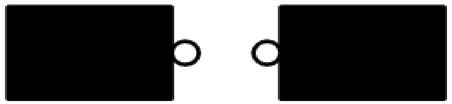
Bypassing techniques for exception when vias are needed

Very long thin traces add inductance. Capacitor is effectively isolated

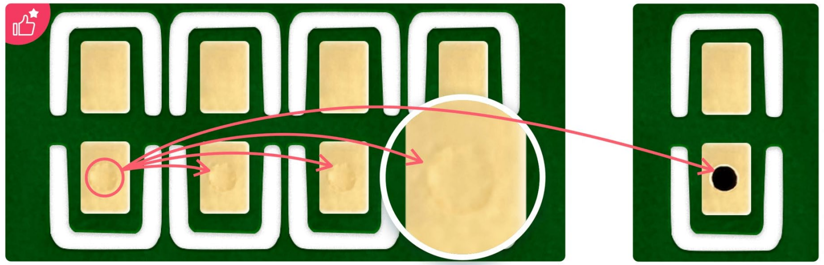
Vias close to pads lowers inductance

Multiple vias reduce inductance

Lowest inductance due to smallest loop area

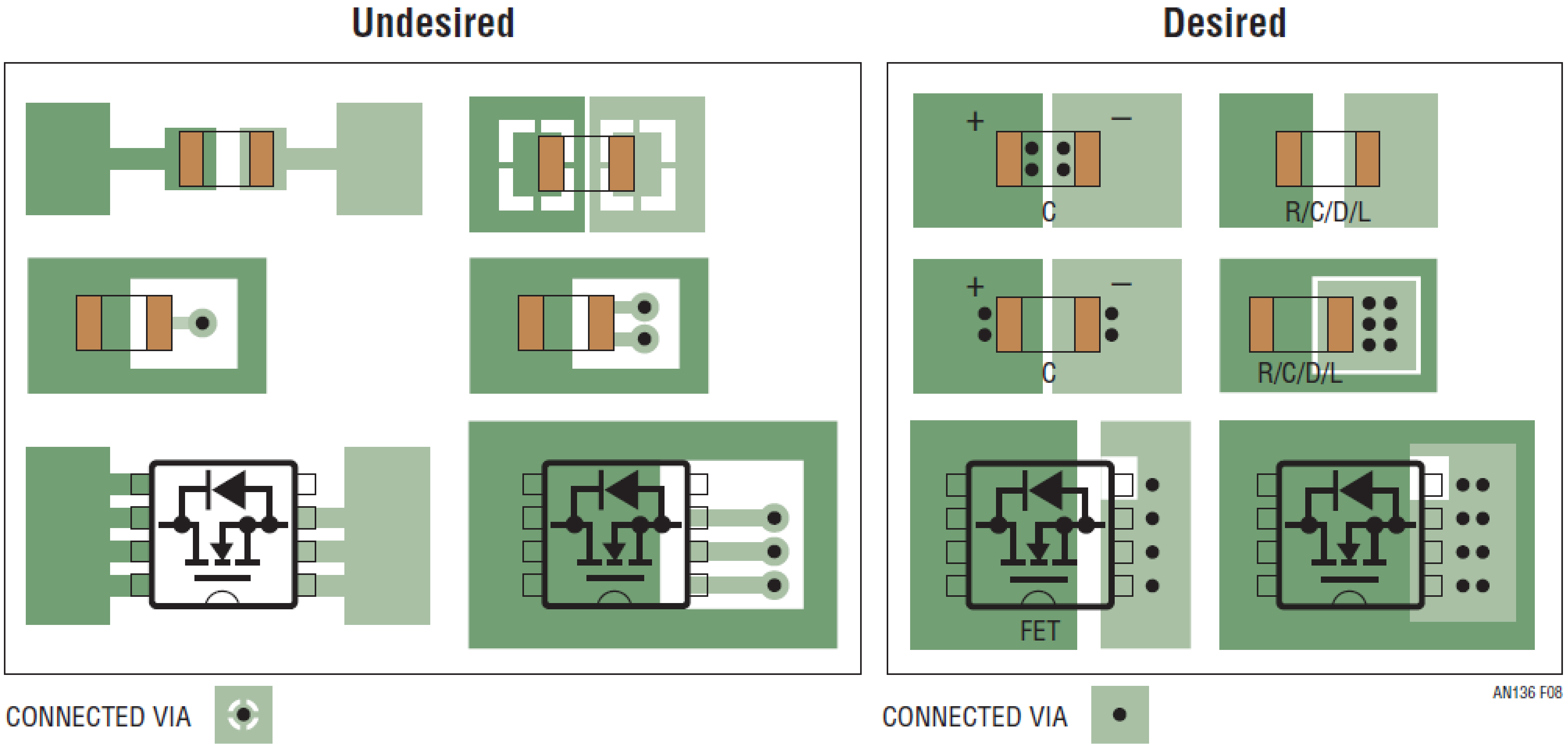


Or use via-in-pad for the lowest induction (source: jlcpcb.com)

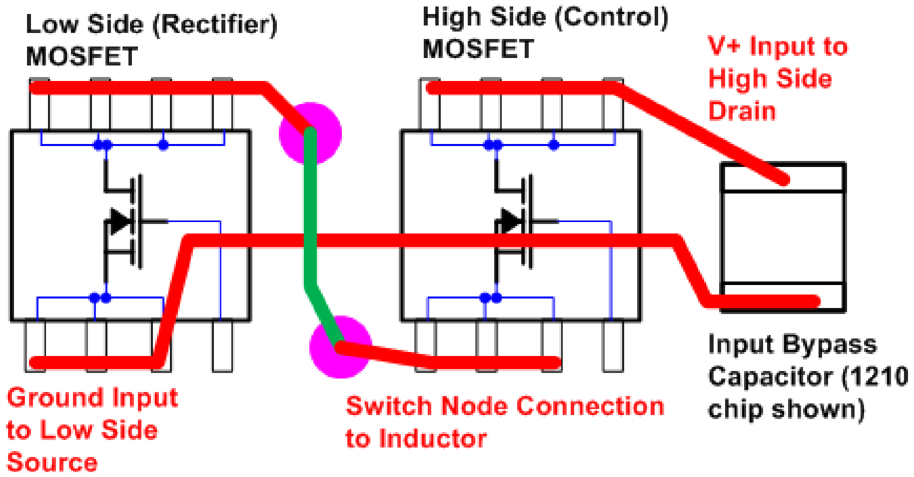


"Via-in-pad" with JLCPCB's FPOV process   Regular process

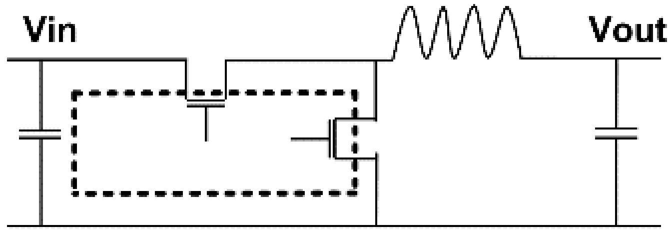
Other connection do‘s and don‘ts

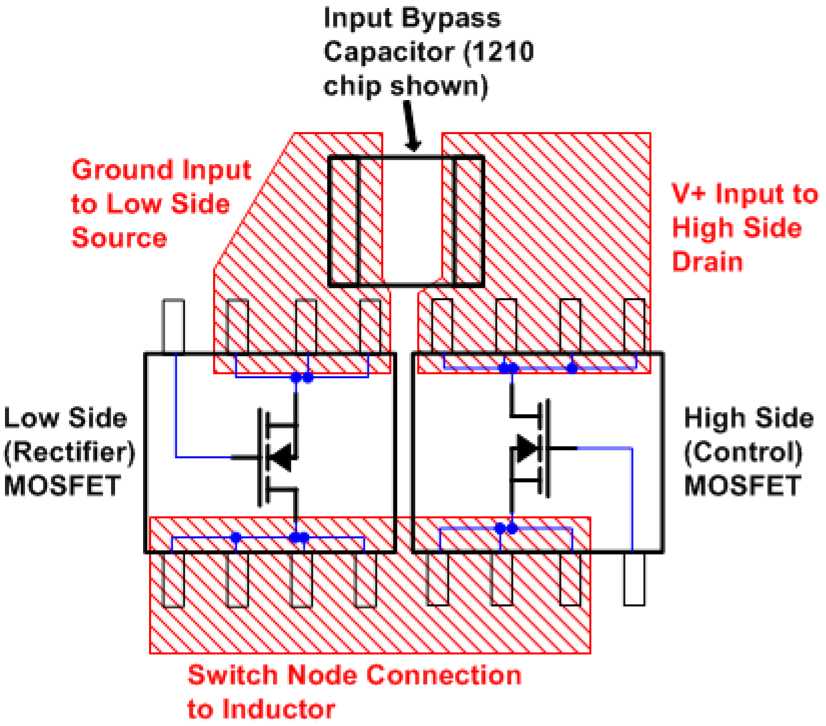


Using external power FETs in synchronous buck

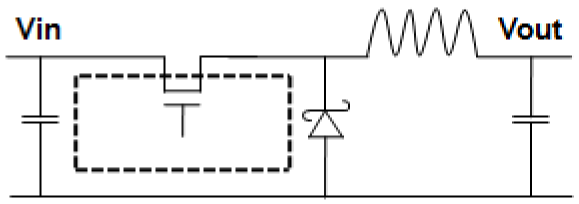


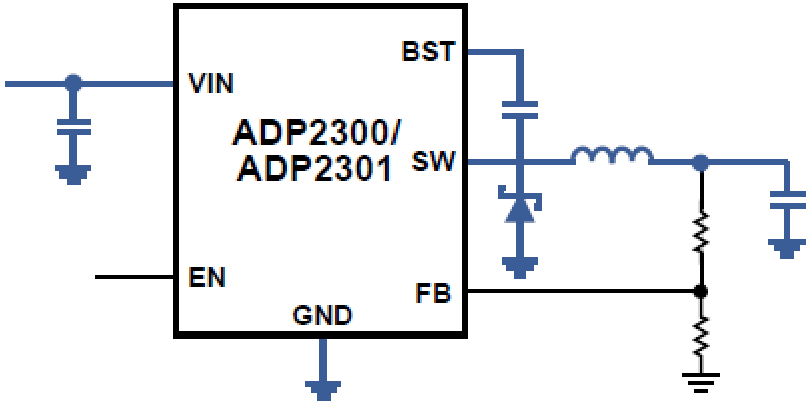
Poor Layout Example

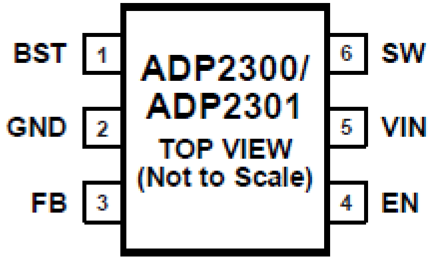


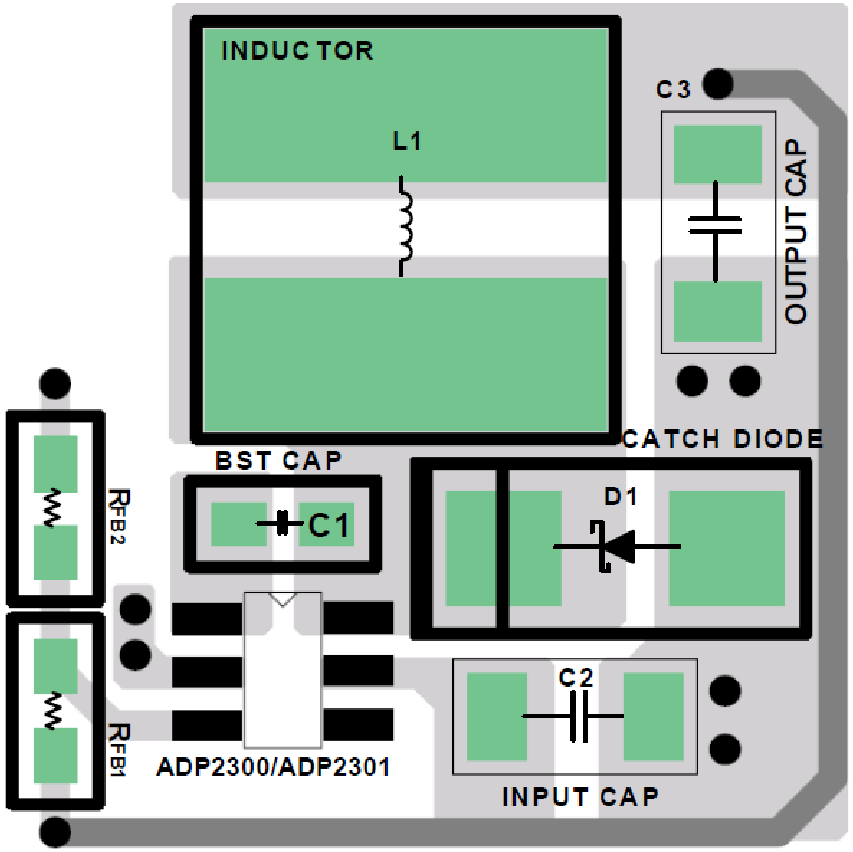


Layout example 1.2A, 20V, 700kHz/1.4MHz

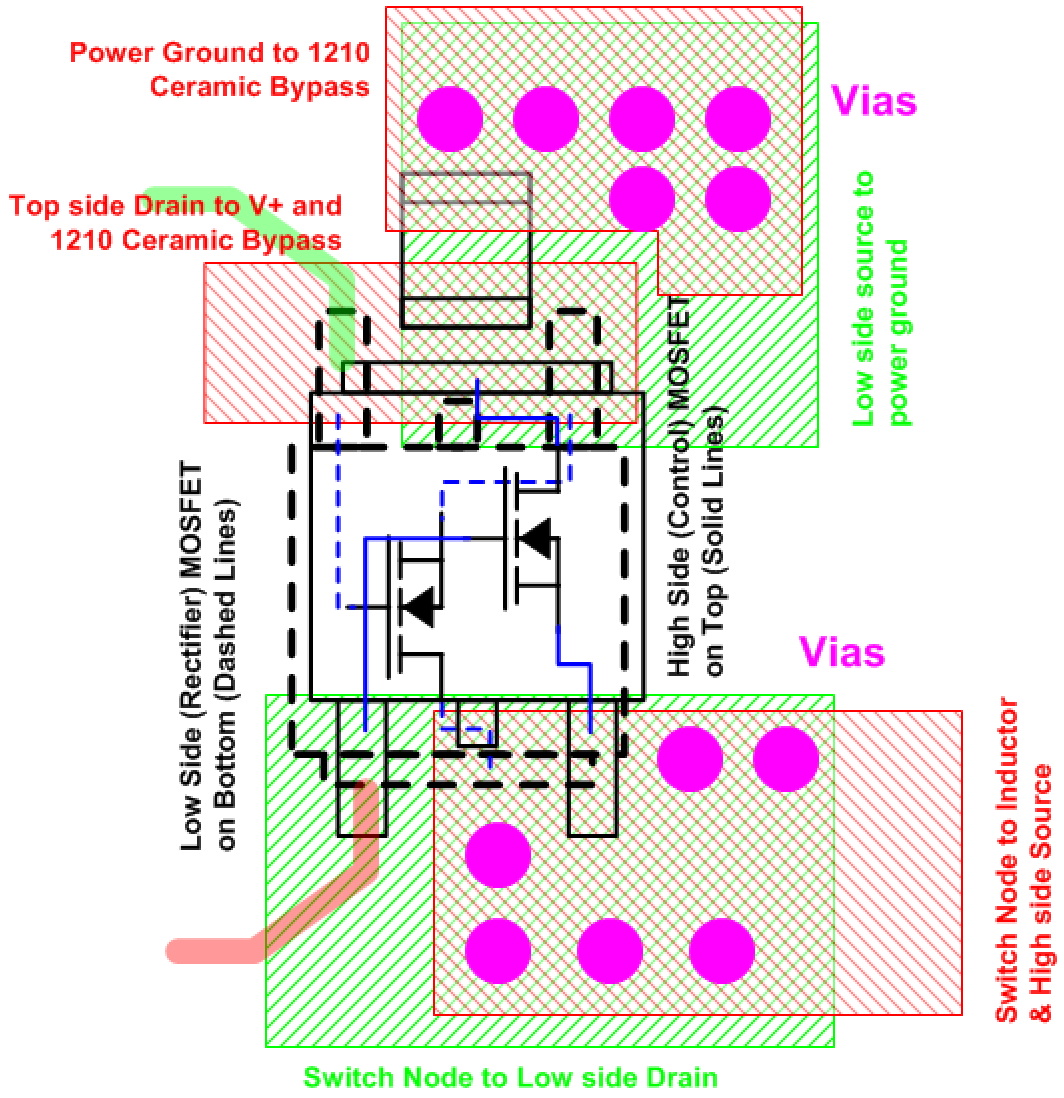




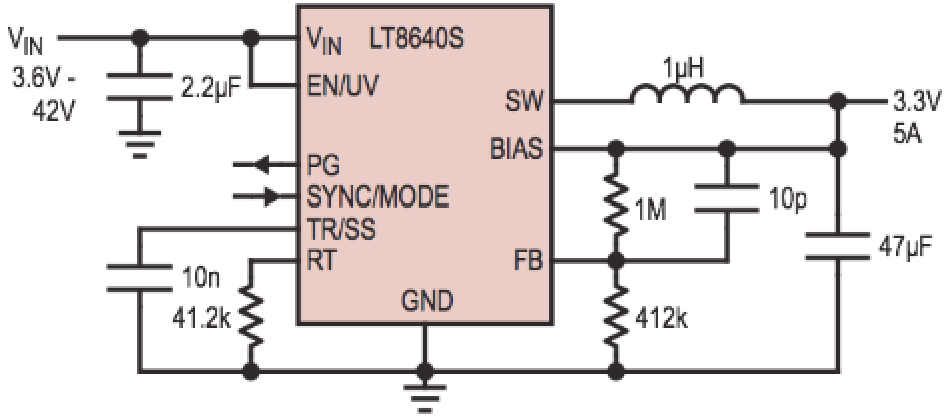


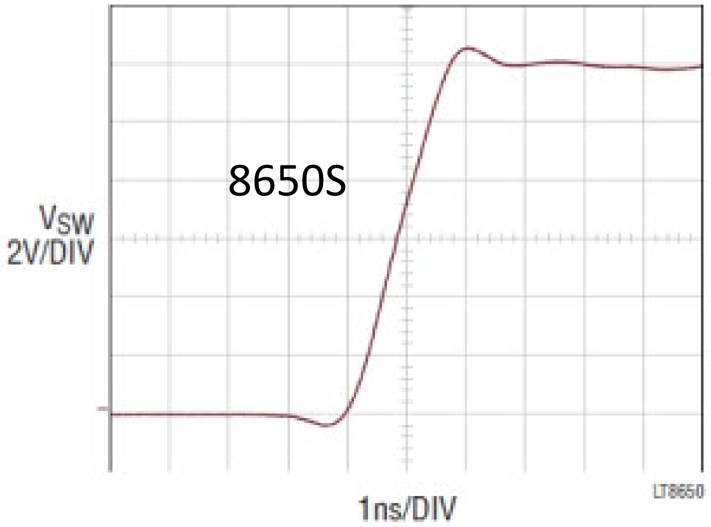


Using external power FETs in synchronous buck

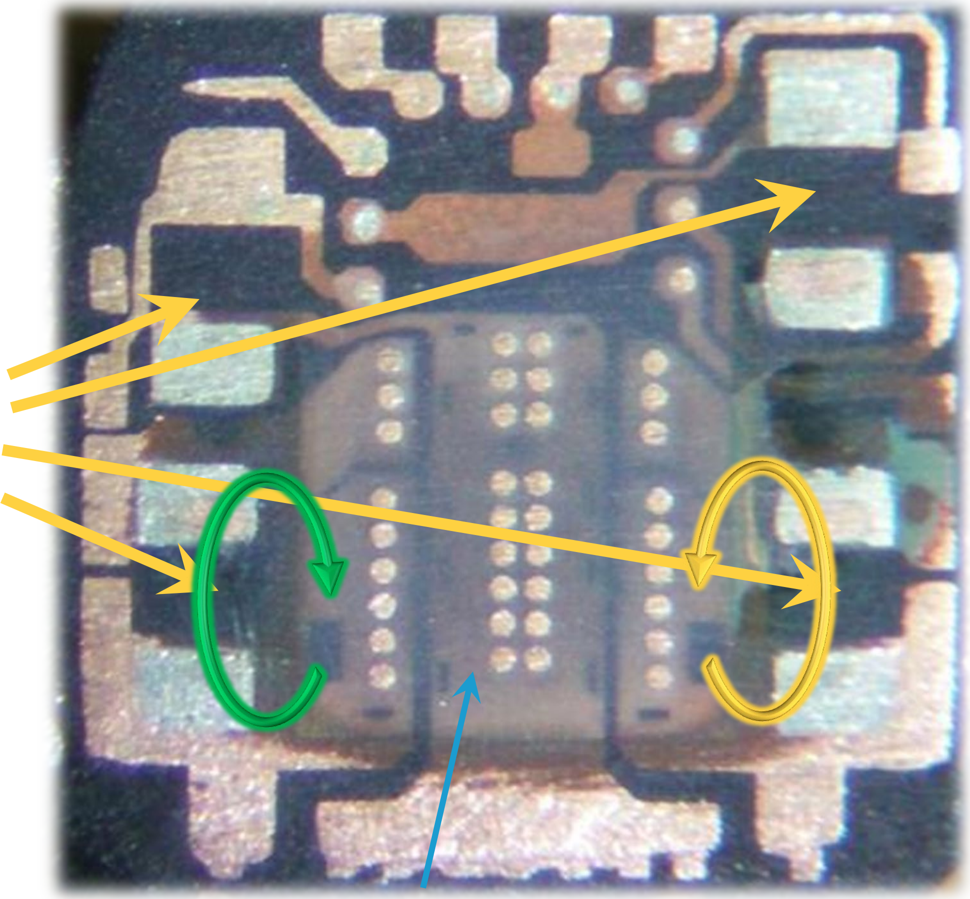


Silent Switcher 2





Four
Internal
Capacitors

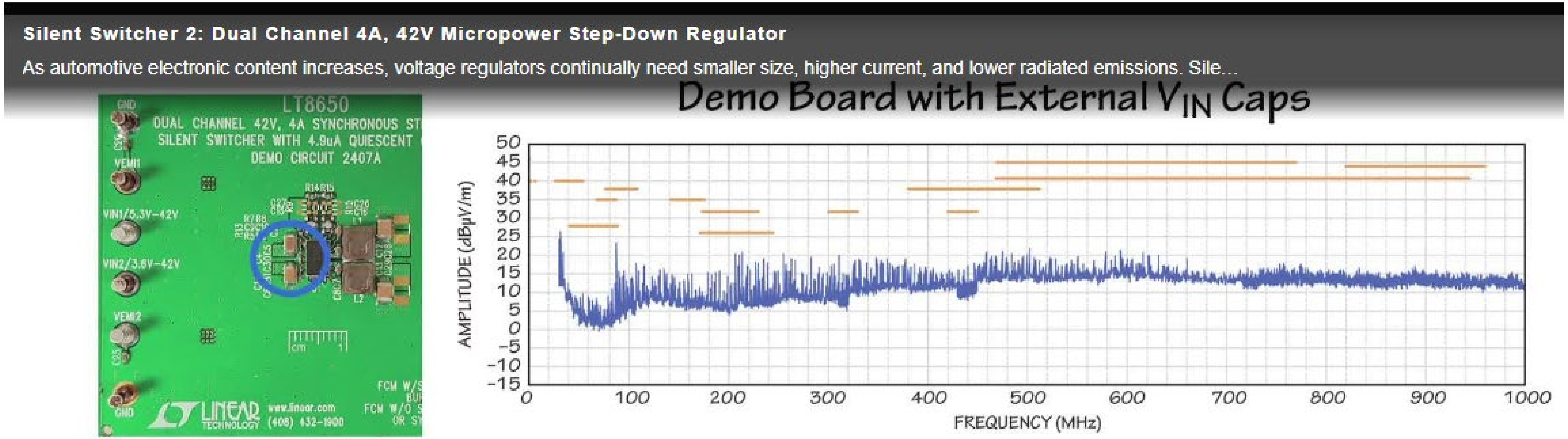


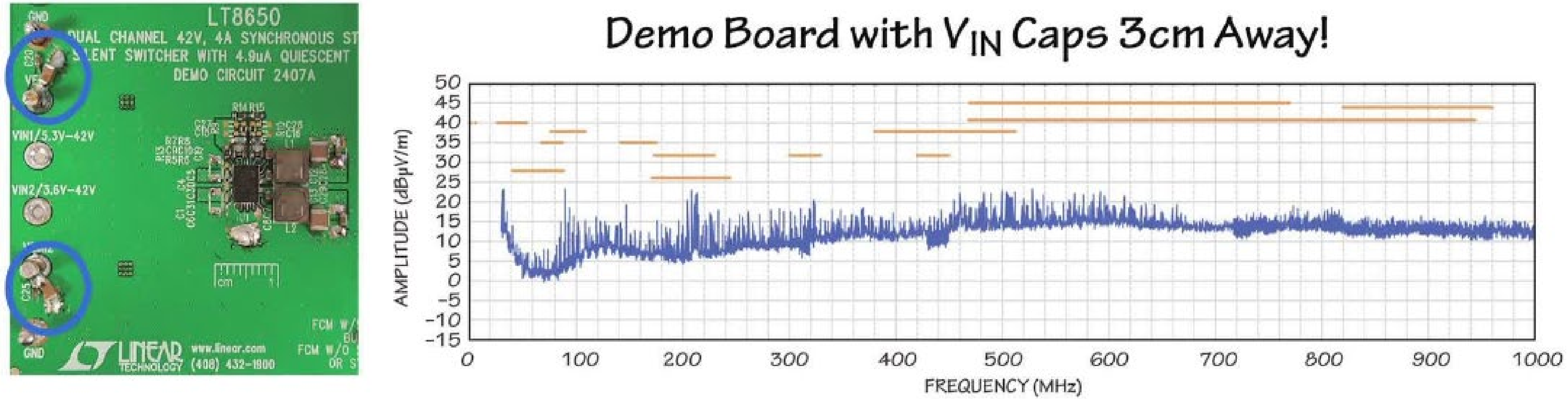
LT8640 die

Capacitors Internal

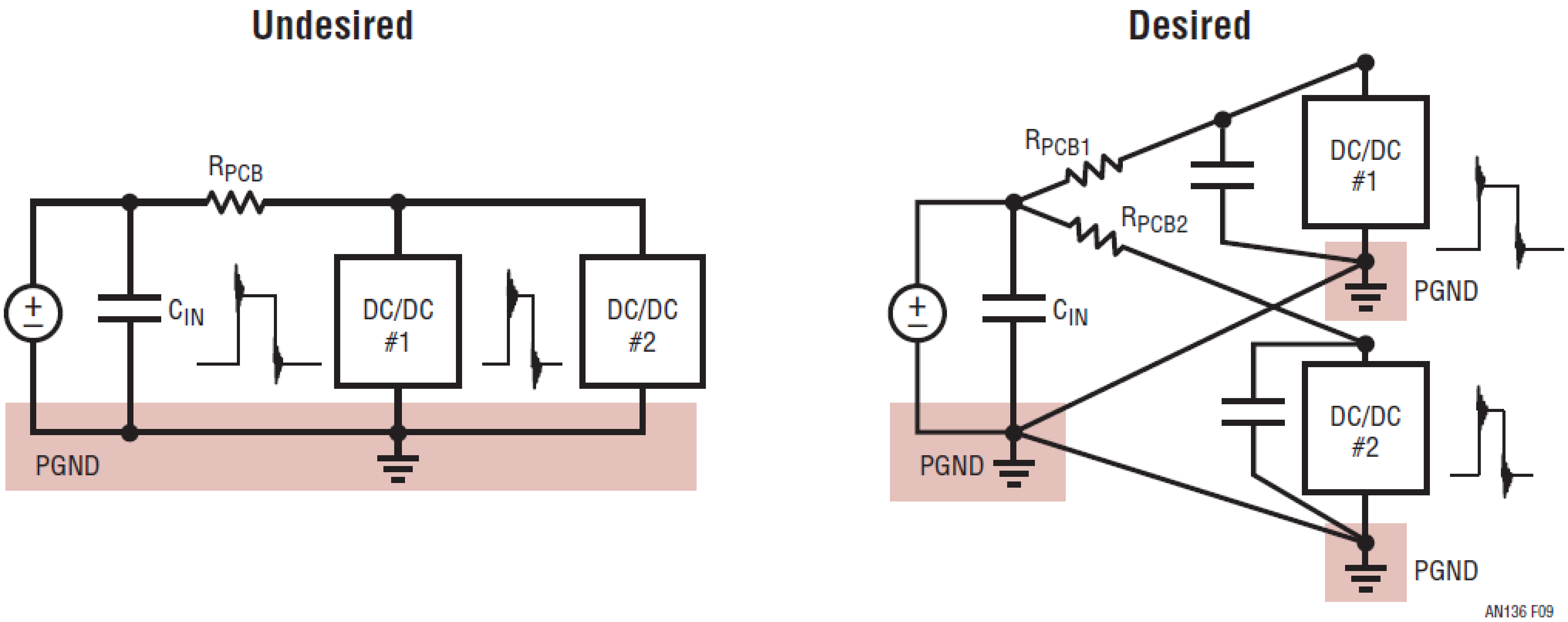
"S" suffix = Silent Switcher 2

Silent Switcher 2: Great Flexibility with Input Cap placement





Separate the Input Current Paths Among Supplies



Desired and Undesired Layer Arrangement

6-Layer PCB

Undesired

- Layer 1 - Power Component
- Layer 2 - Small Signal
- Layer 3 - GND Plane
- Layer 4 - DC Voltage or GND Plane
- Layer 5 - Small Signal
- Layer 6 - Power Component/Controller

(a)

Desired

- Layer 1 - Power Component
- Layer 2 - GND Plane
- Layer 3 - Small Signal
- Layer 4 - Small Signal
- Layer 5 - DC Voltage or GND Plane
- Layer 6 - Power Component/Controller

(b)

4-Layer PCB

Undesired

- Layer 1 - Power Component
- Layer 2 - Small Signal
- Layer 3 - GND Plane
- Layer 4 - Small Signal/Controller

(c)

Desired

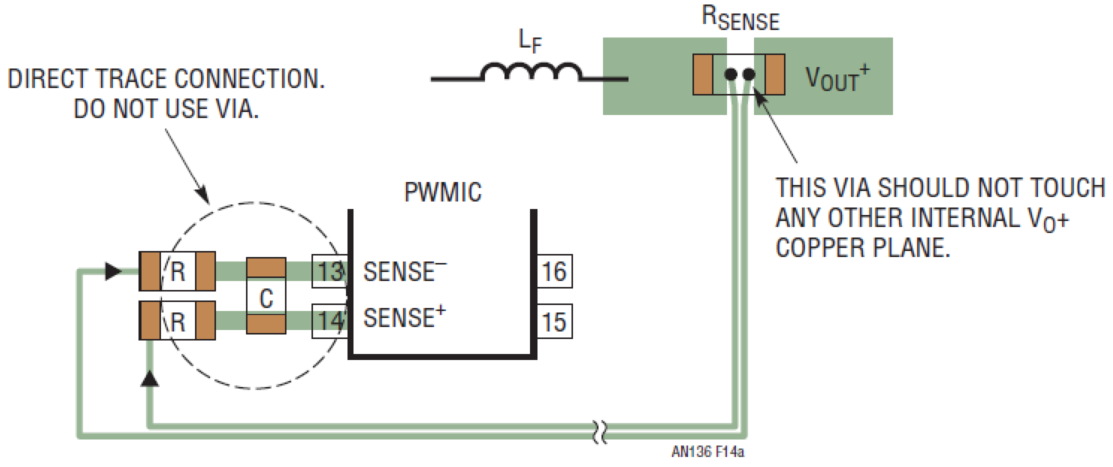
- Layer 1 - Power Component
- Layer 2 - GND Plane
- Layer 3 - Small Signal
- Layer 4 - Small Signal/Controller

(d)

AN136 F01

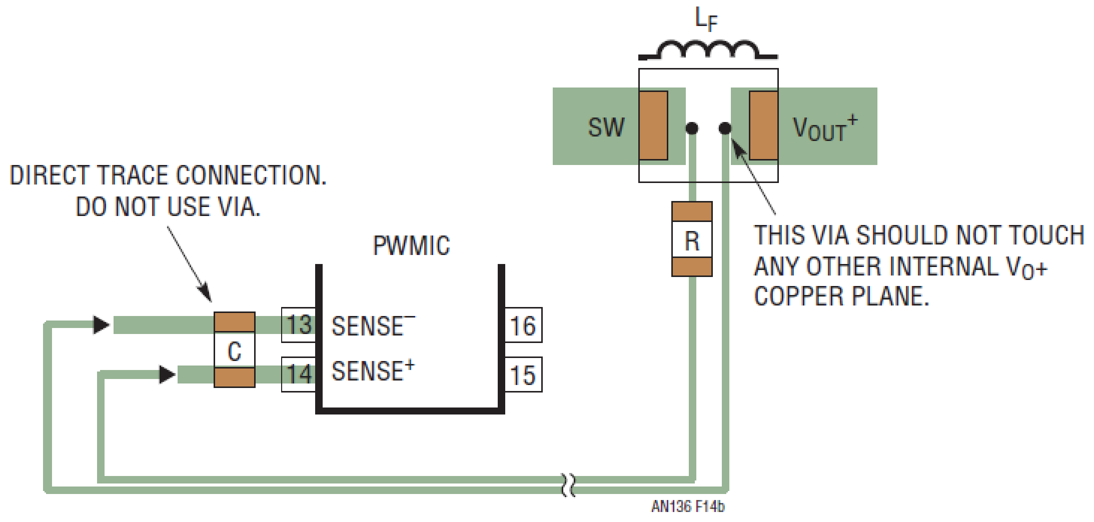
Kelvin current sense

Rsense



(a)

L DCR sense



(b)

Application Note 136

Application Note 136
June 2012

PCB Layout Considerations for Non-Isolated Switching Power Supplies

Henry J. Zhang

Introduction

The best news when you power up a prototype supply board for the very first time is when it not only works, but also runs quiet and cool. Unfortunately, this does not always happen. A common problem of switching power supplies is "unstable" switching waveforms. Sometimes, waveform jittering is so pronounced that audible noise can be heard from the magnetic components. If the problem is related to the printed circuit board (PCB) layout, identifying the cause can be difficult. This is why proper PCB layout at the early stage of a switching supply design is very critical. Its importance cannot be overstated.

The power supply designer is the person who best understands the technical details and functional requirements of the supply within the final product. He or she should work closely with the PCB layout designer on the critical supply layout from the beginning. A good layout design optimizes supply efficiency, alleviates thermal stress, and most importantly, minimizes the noise and interactions among traces and components. To achieve these, it is important for the designer to understand the current conduction paths and signal flows in the switching power supply. The following discussion presents design considerations for a proper layout design for non-isolated switching power supplies.

PLAN OF THE LAYOUT

Location of the Power Supply in System Board

For the embedded DC/DC supply on a large system board, the supply output should be located close to the load devices in order to minimize the interconnection impedance and the conduction voltage drop across the PCB traces to achieve best voltage regulation, load transient response and system efficiency. If forced-air cooling is available, the supply should also be located close to the cooling fan or have good air flow to limit the thermal stress. In addition, the large passive components such as inductors and electrolytic capacitors should not block the air flow to the low profile, surface mount semiconductor components such as power MOSFETs, PWM controller, etc. To prevent the switching noise from upsetting other analog signals in the system, avoid routing sensitive signal traces underneath the supply if possible. Otherwise, an internal ground plane between the power supply layer and small signal layer is needed for shielding.

It is necessary to point out that this power supply location and board real estate planning should be done at the early design/planning stage of the system. Unfortunately, sometimes people focus on other more "important" or "exciting" circuits on the big system board first. If power management/supply is the last thought and is relegated to whatever space is left on the board, this certainly does not help ensure efficient and reliable power supply design.

Placement of Layers

On a multilayer PCB board, it is highly desirable to place the DC ground or DC input or output voltage layers between the high current power component layer and the sensitive small signal trace layer. The ground and/or DC voltage layers provide AC grounds to shield the small signal traces from noisy power traces and power components. As a general rule, the ground or DC voltage planes of a multilayer PCB should not be segmented. If the segmentation is unavoidable, the number and length of traces in these planes must be minimized. The traces should also be routed in the same direction as the high current flow direction to minimize the impact.

Figures 1a and 1c provide examples of the undesired layer arrangement of the 6-layer and 4-layer PCB boards for switching power supply. In these examples, the small signal layer is sandwiched between the high current power layer and the ground layer. These configurations increase the

AHEAD OF WHAT'S POSSIBLE

analog.com

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Vos retours sont grandement appréciés!

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