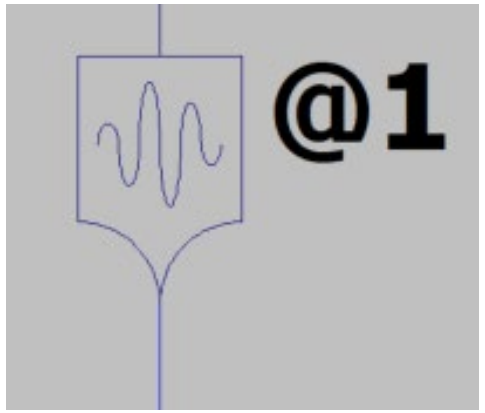
Generating SMPS Bode Plots in LTspice

Sven Rossa
Field Application Engineer
Sven.Rossa@analog.com

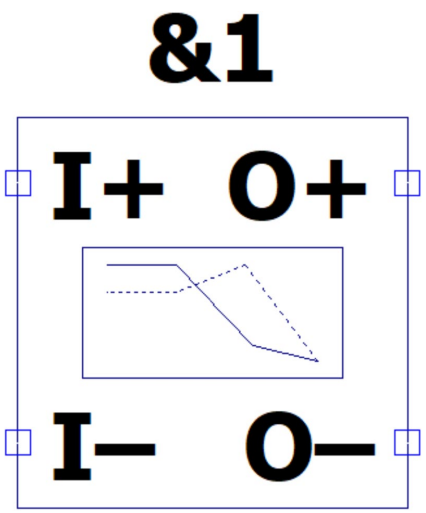
Introduction

- Generating DC/DC Converter Bode Plots with LTspice Frequency Response Analysis (FRA) tools
  - Using the FRA device
  - Using the FRA Probe

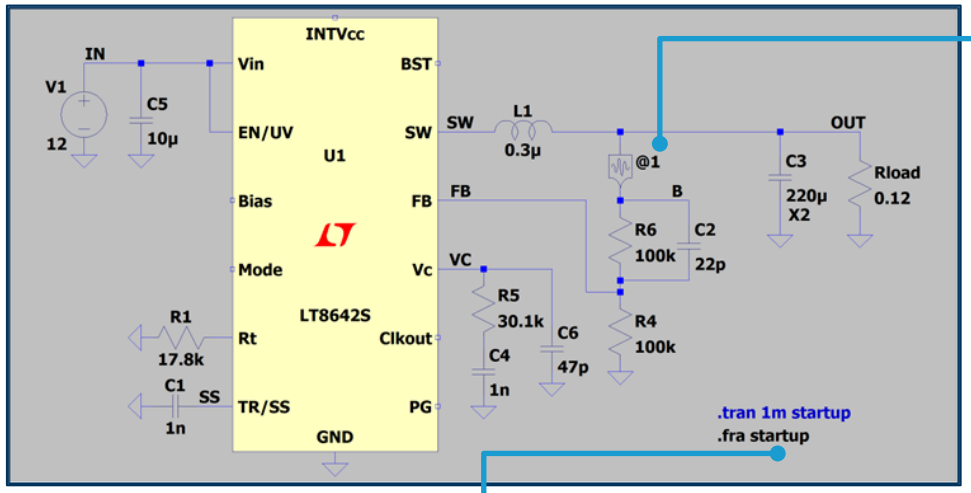
FRA Device

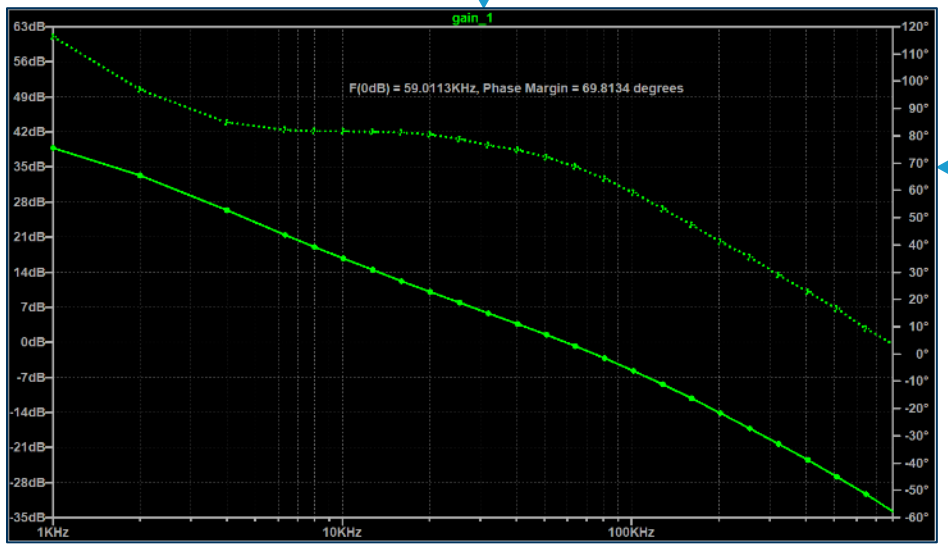


FRA Probe

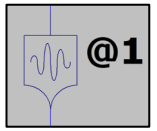


How To FRA

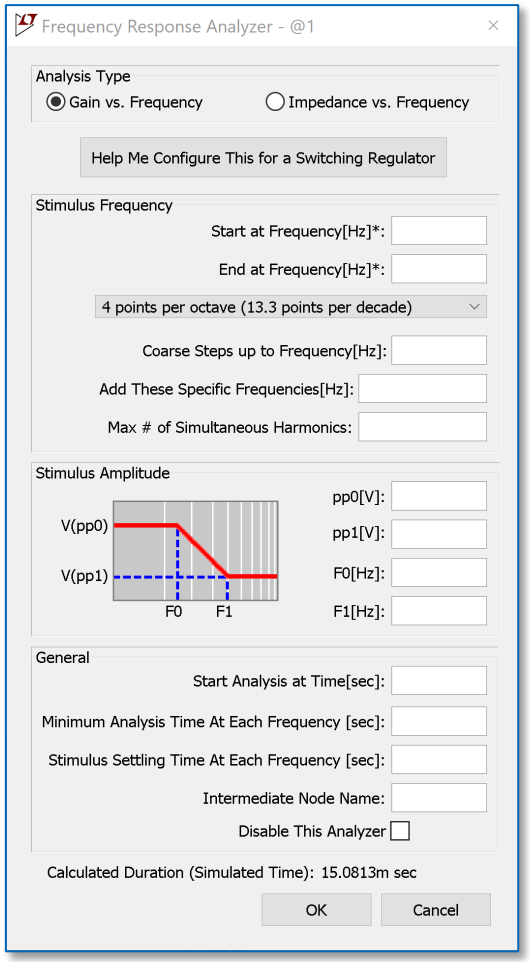




Right-click FRA device

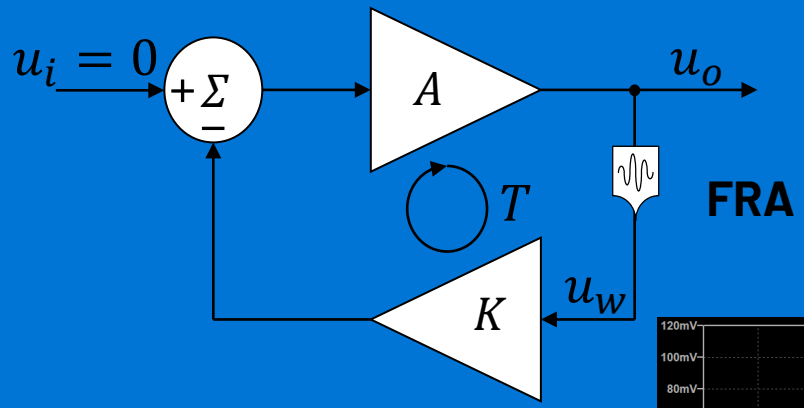


FRA device settings

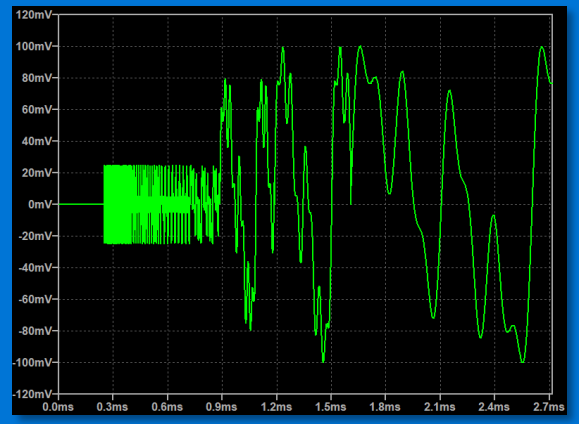


What does the FRA Device do?

- Transient Simulation
- The FRA component injects sinusoidal stimulus

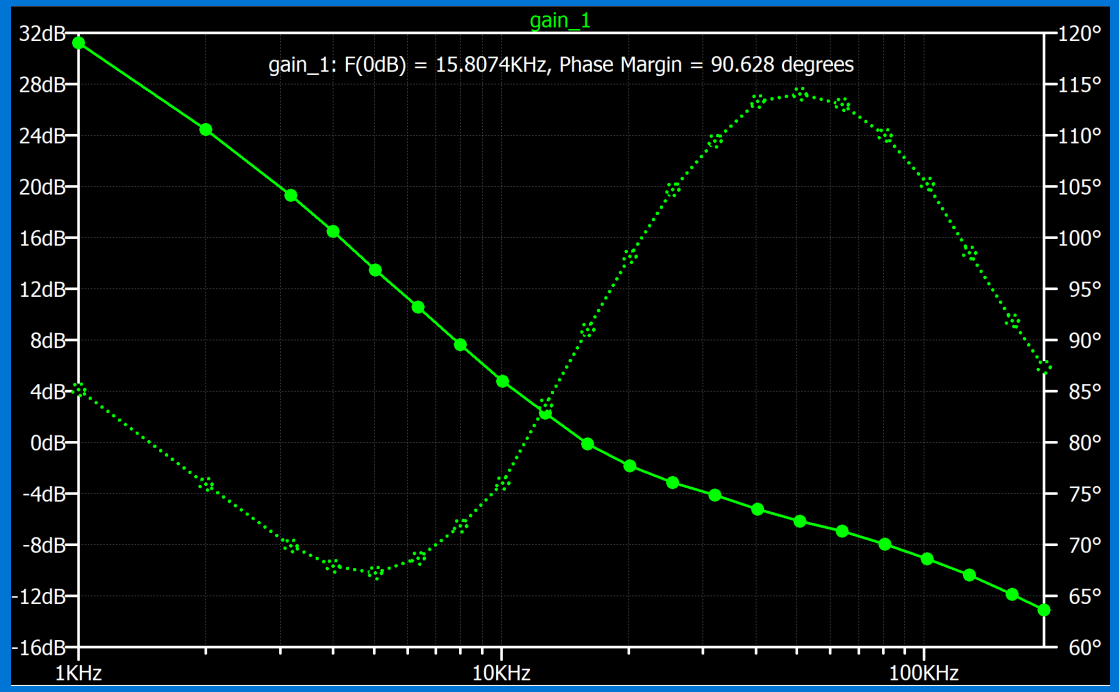


$$u_o = -Tu_w$$



Time

- Perturbation is measured at FRA nodes
- Bode plot is extracted by Fourier analysis

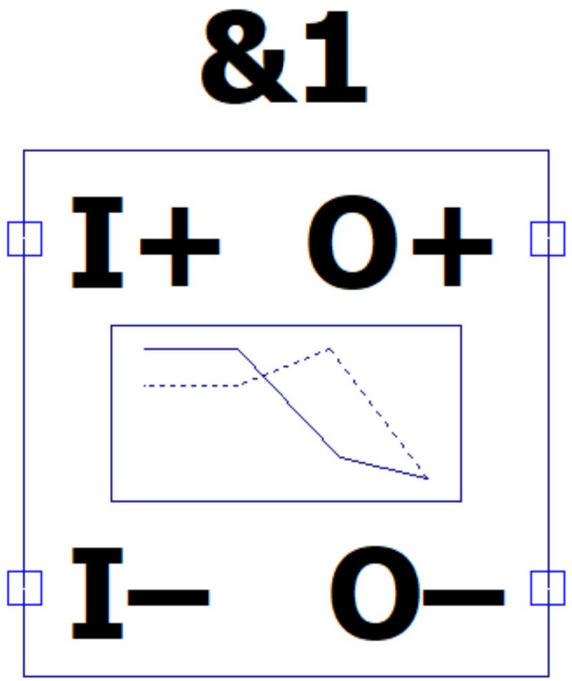


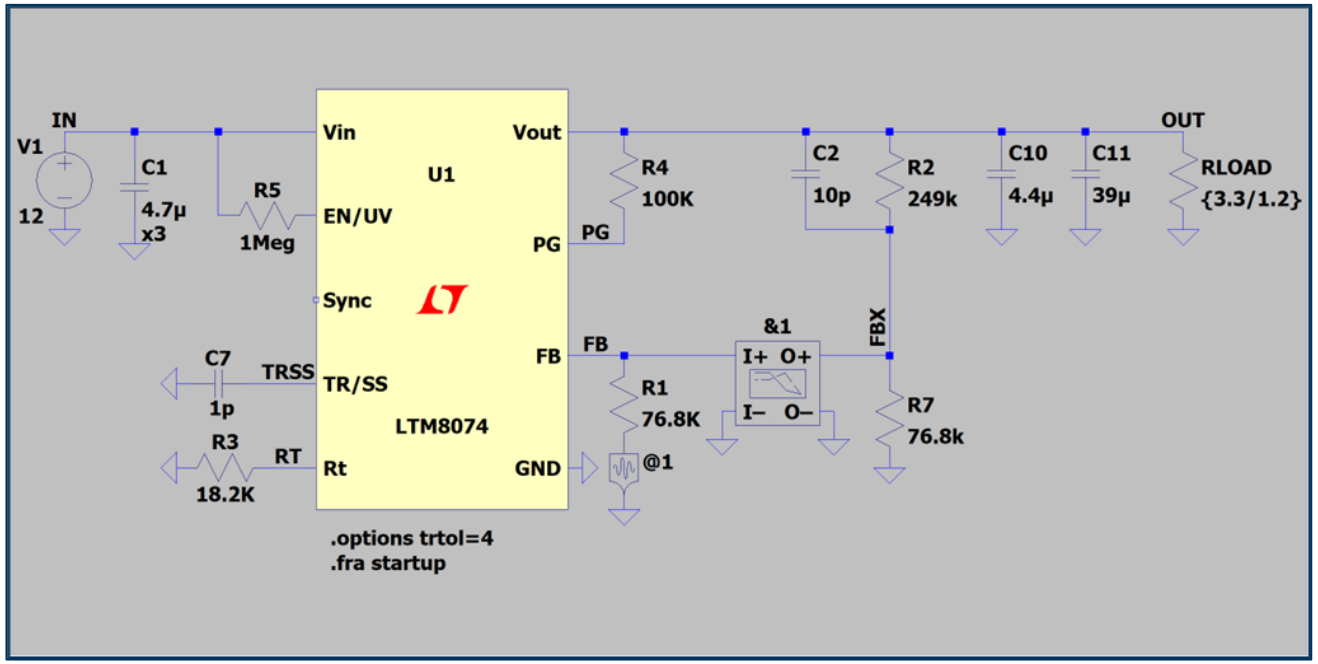
Frequency

What does the FRA Probe do?

4-terminal Frequency Response Analyzer Probe to be used in conjunction with the FRA Stimulus

- Enables Bode plots of any part the loop
- Simplifies analysis of µModules with integrated top feedback resistors; negative outputs; and current feedback

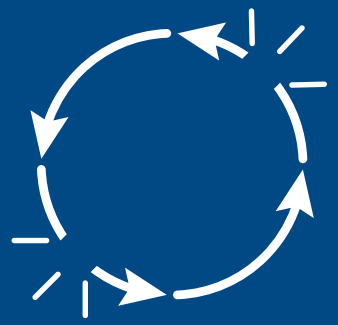




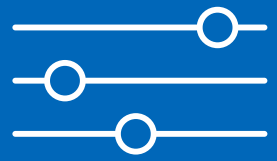
LTspice FRA: Step-by-Step How-To

1. Investigate and prepare the circuit

2. Break the loop



3. Initial FRA setup

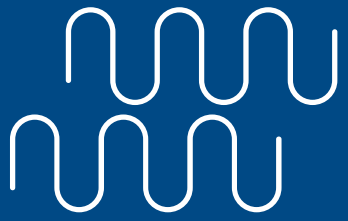


4. Inspect the FRA transient waveforms

5. Initial Bode Analysis

6. Optimize the stimulus

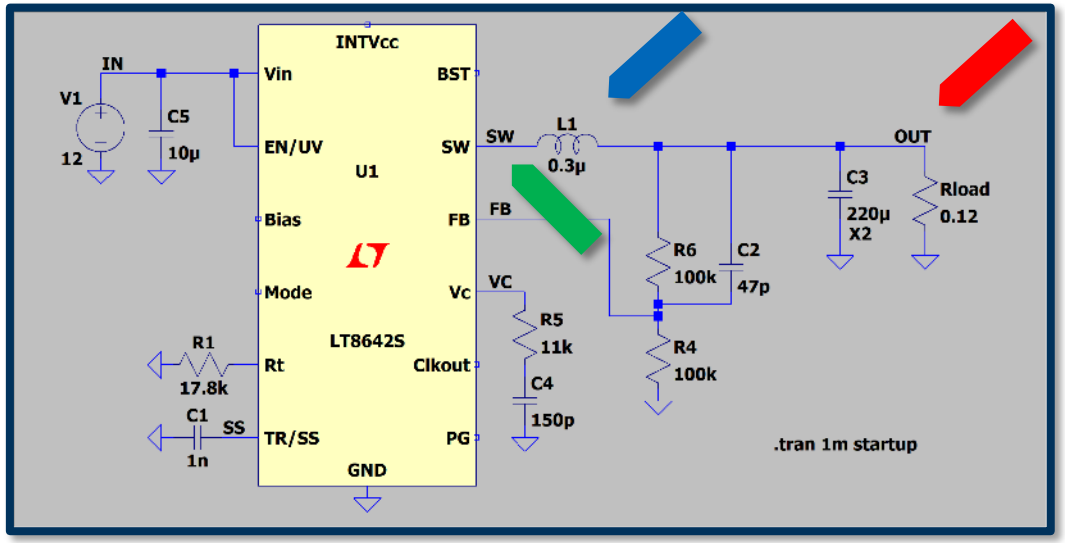
7. Extend to more frequencies

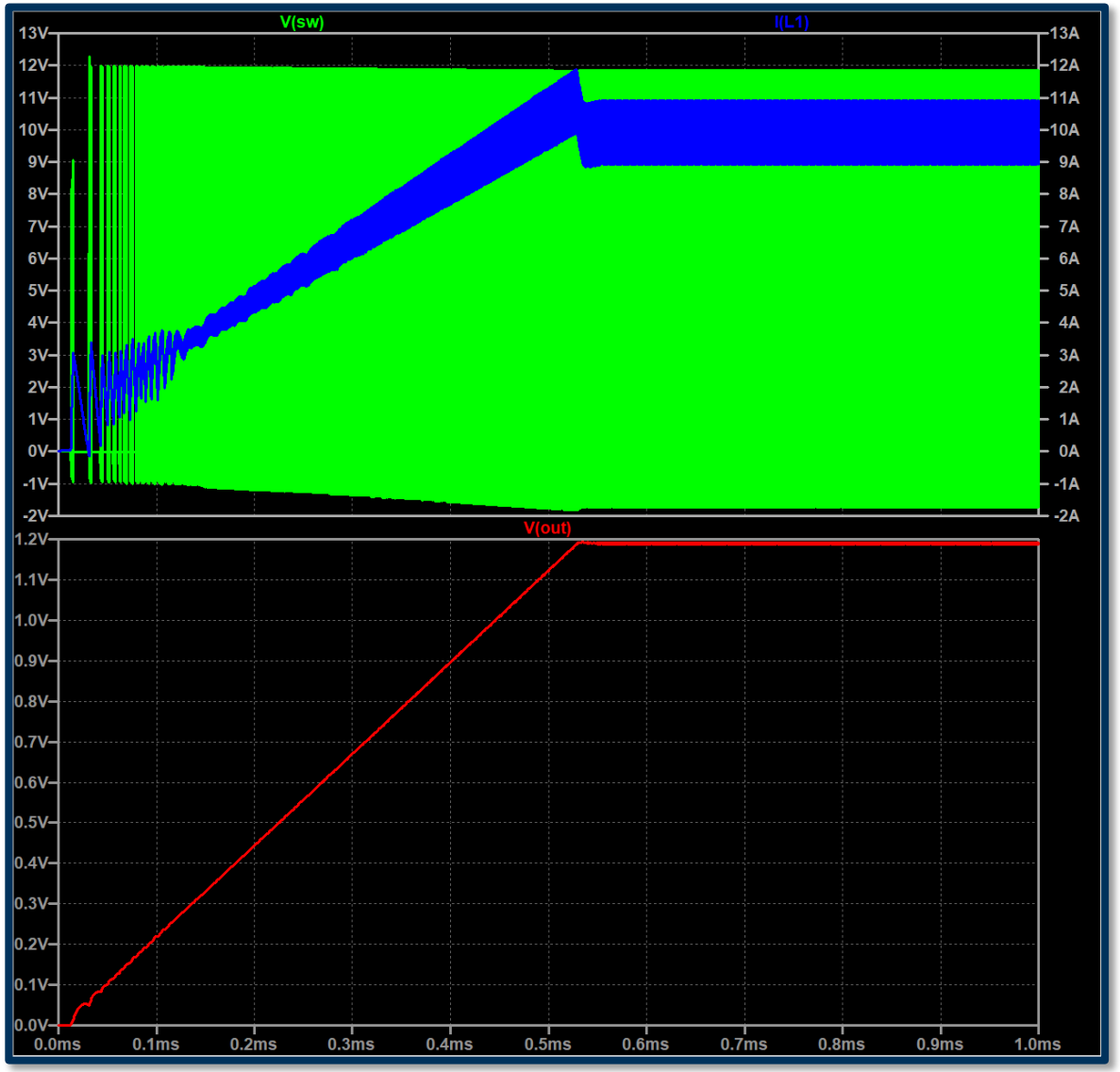


8. Speed up the analysis

1a. Investigate and Prepare the Circuit—Basic

Explore Basic .tran Startup



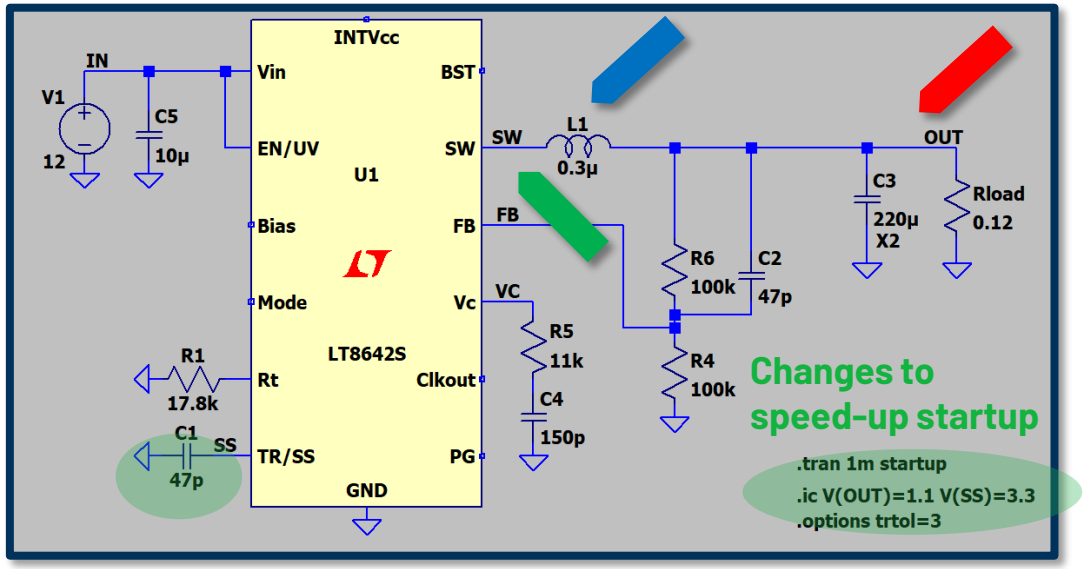


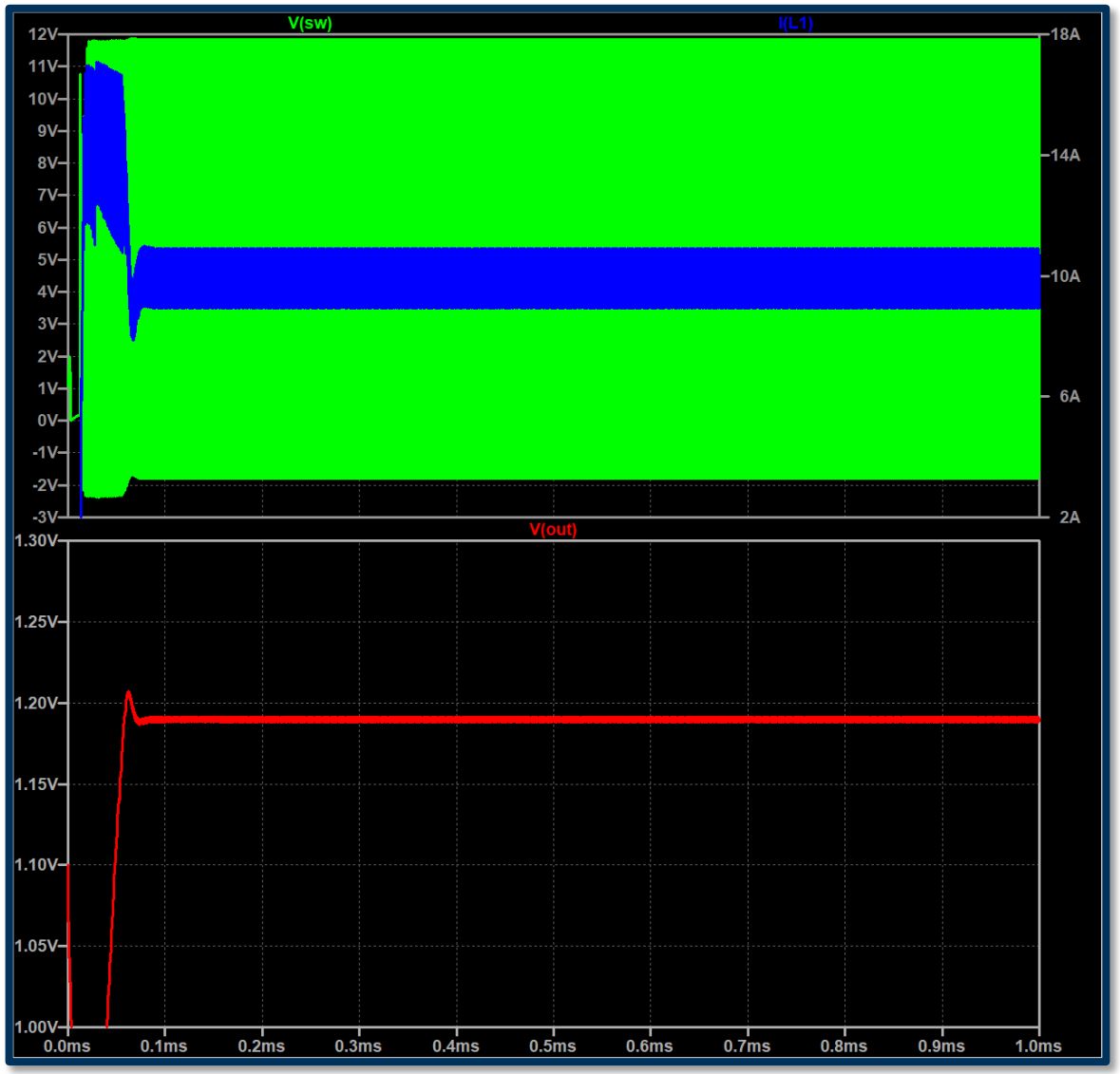
Plot and examine

- Switch node
- Inductor current
- Output voltage

1b. Investigate and Prepare the Circuit—Improved

Explore .tran with *Faster Startup*





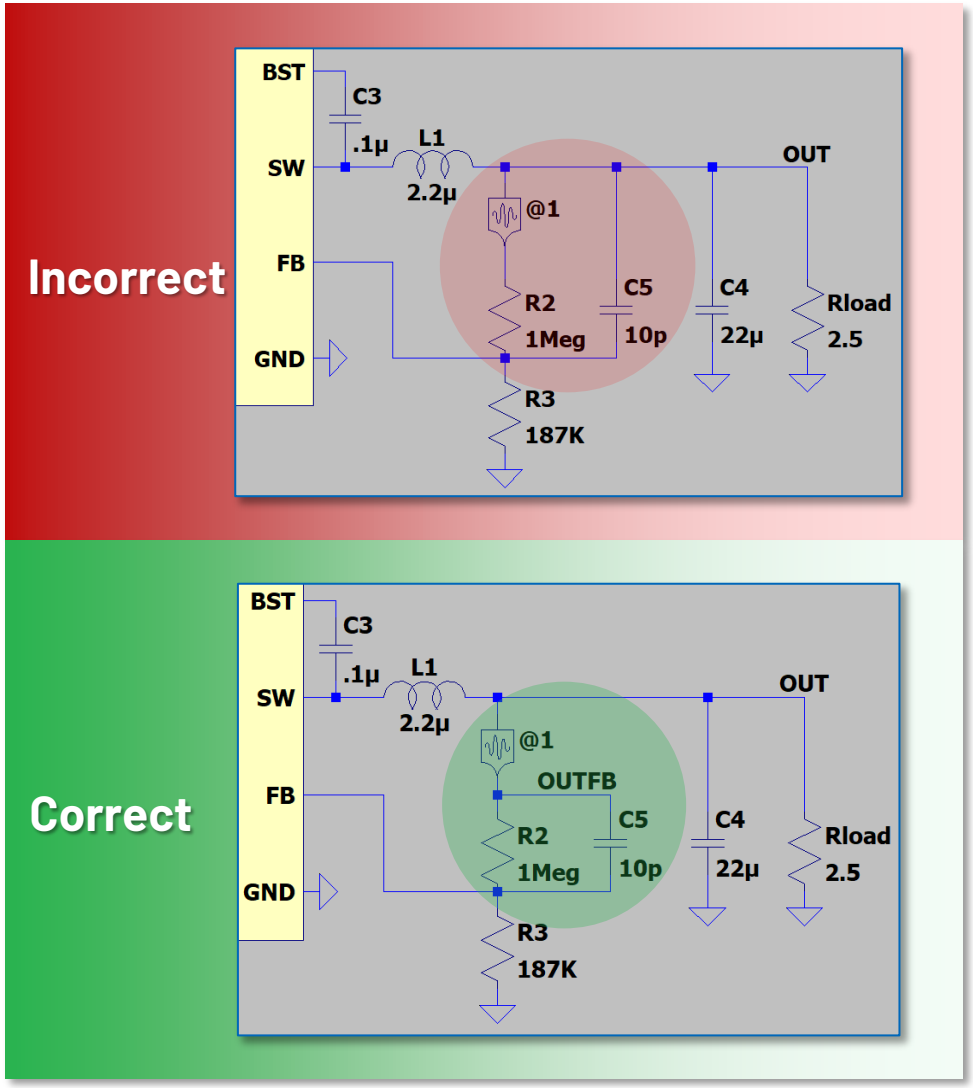
Consider speeding up the startup

- Add initial conditions, **reduce soft-start cap**
- Try higher trtol

Make note of

- Time required to settle to steady-state
  (~80µs in this example compared to 550µs previously)
- Final output voltage (~1.2V)
- Switching frequency (~2MHz, not shown)

2. Break the Loop



Criteria

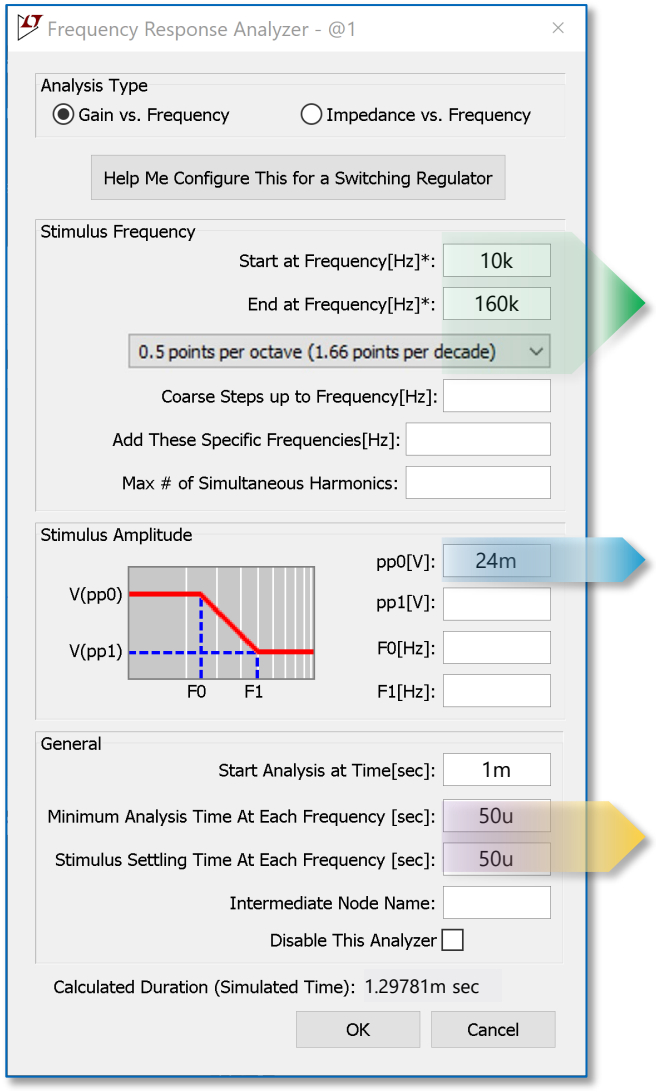
- Interrupt **all** feedback paths
- FRA component must point from **lower impedance (flat side)** to **higher impedance (pointy side)**

This requires engineering

- LTspice does not know the correct placement
- Many circuits have multiple places where the loop can be broken—if in doubt, try two places and compare the results (adjust the stimulus amplitude appropriately)

More examples near the end of this presentation

3. Initial FRA Device Setup—Start Small



Start with just two or three frequencies

- If you have an idea of the loop bandwidth, try Fstart = $f_{0dB} \div 8$ and Fend = $2 \bullet f_{0dB}$
- If you don't have a clue about the bandwidth, try Fstart = $f_{SW} \div 160$ and Fend = $f_{SW} \div 10$
- Set resolution to 0.5 points per octave

Start with pp0 = 1%~2% of common mode voltage

- Constant frequency parts tend to tolerate more stimulus than COT, boundary mode, etc.

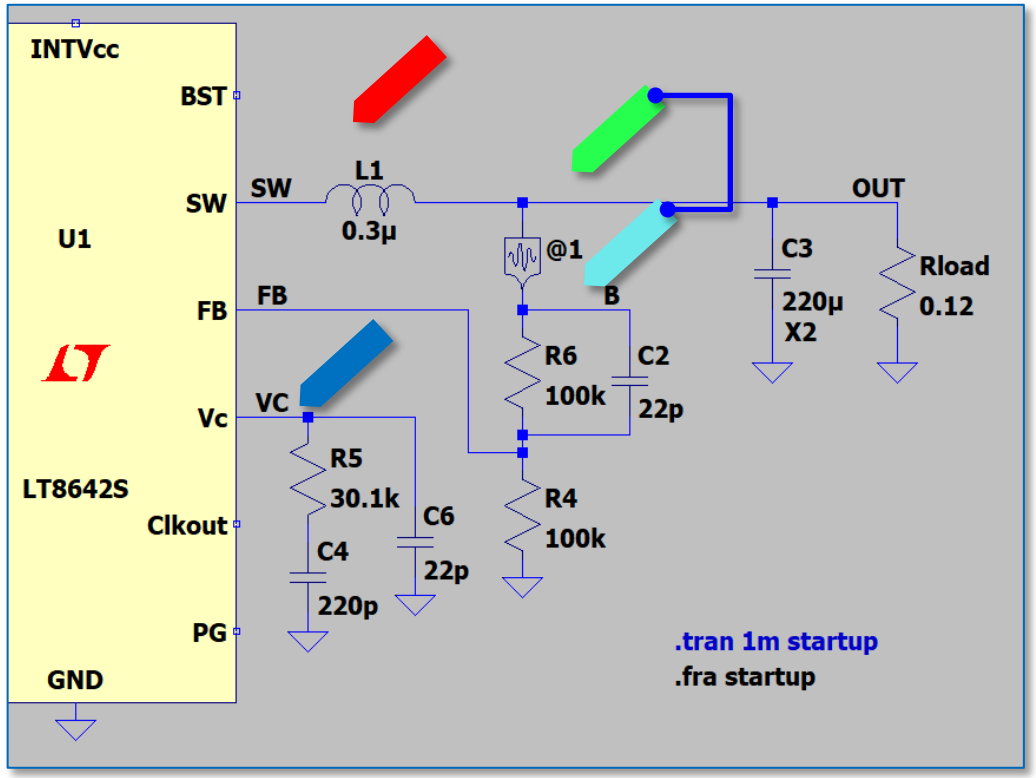
Allow plenty of settling and averaging time

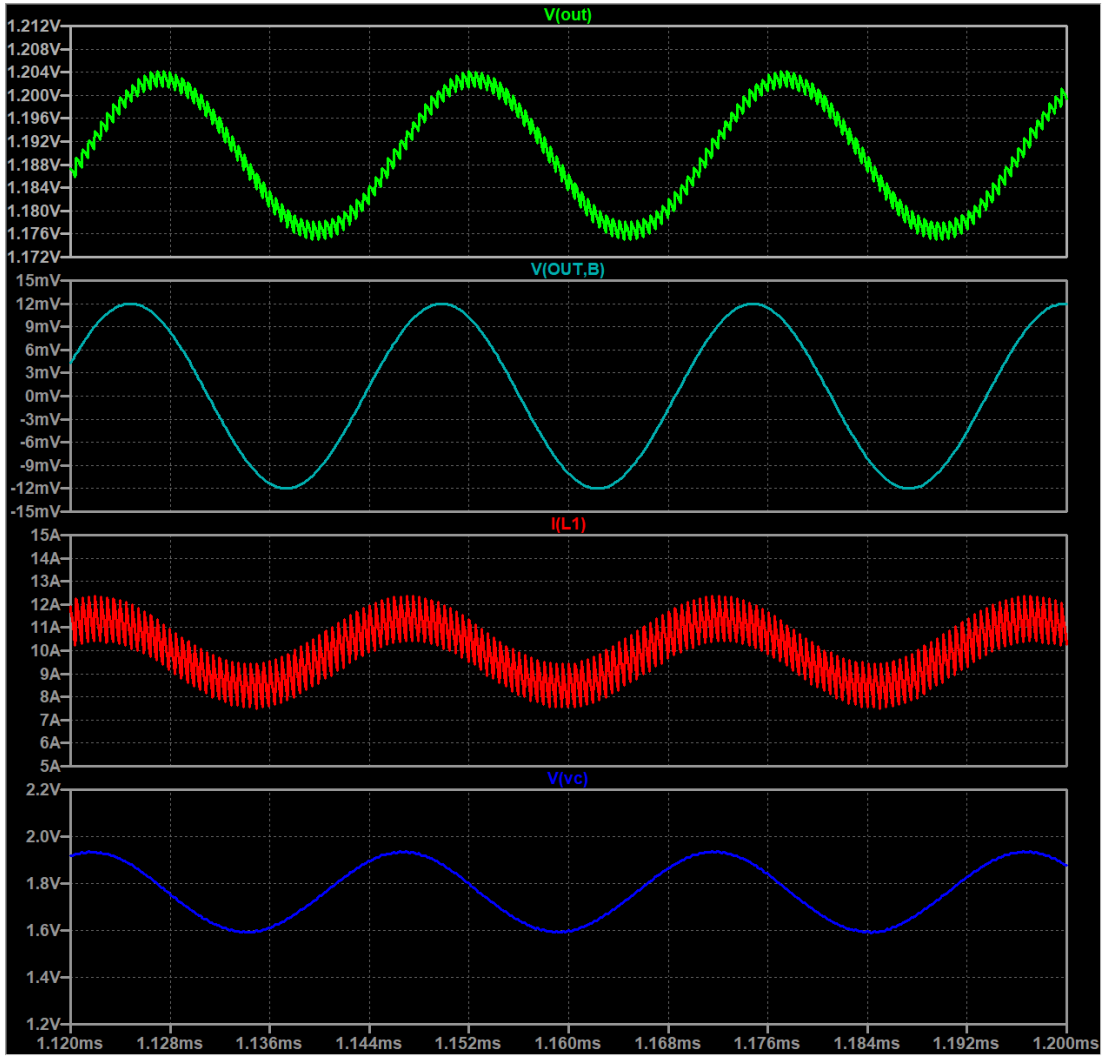
- 100~200 switching cycles is a good starting point

4a. Inspect the FRA transient waveforms

Plot and Examine

- Voltage at both FRA terminals, and the difference
- Inductor current
- Compensation pin voltage (if external)



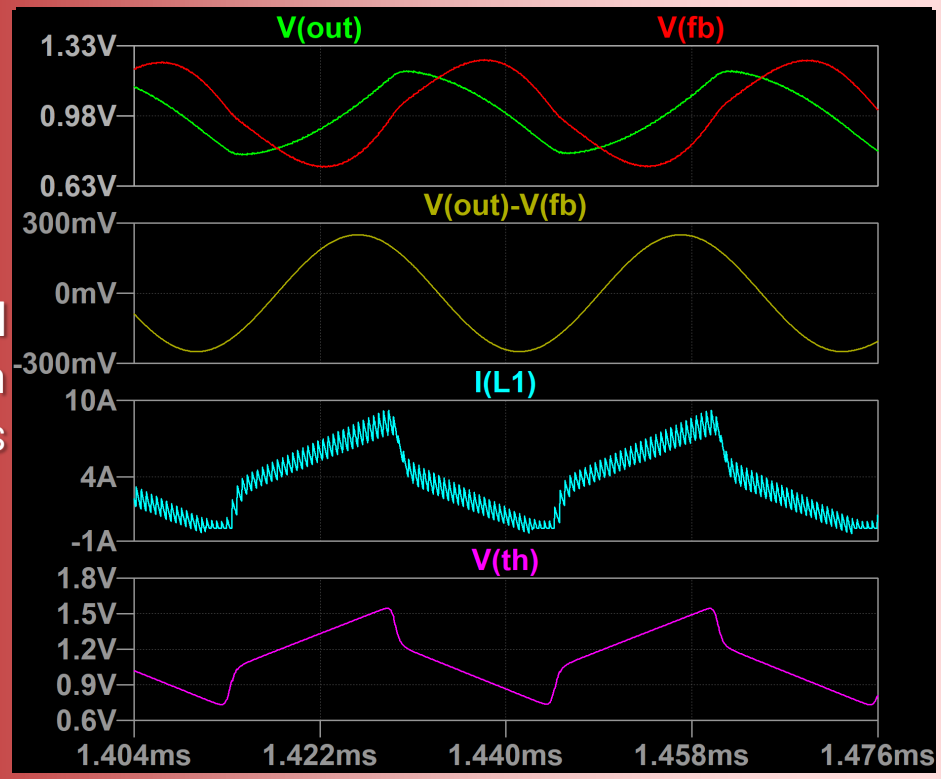


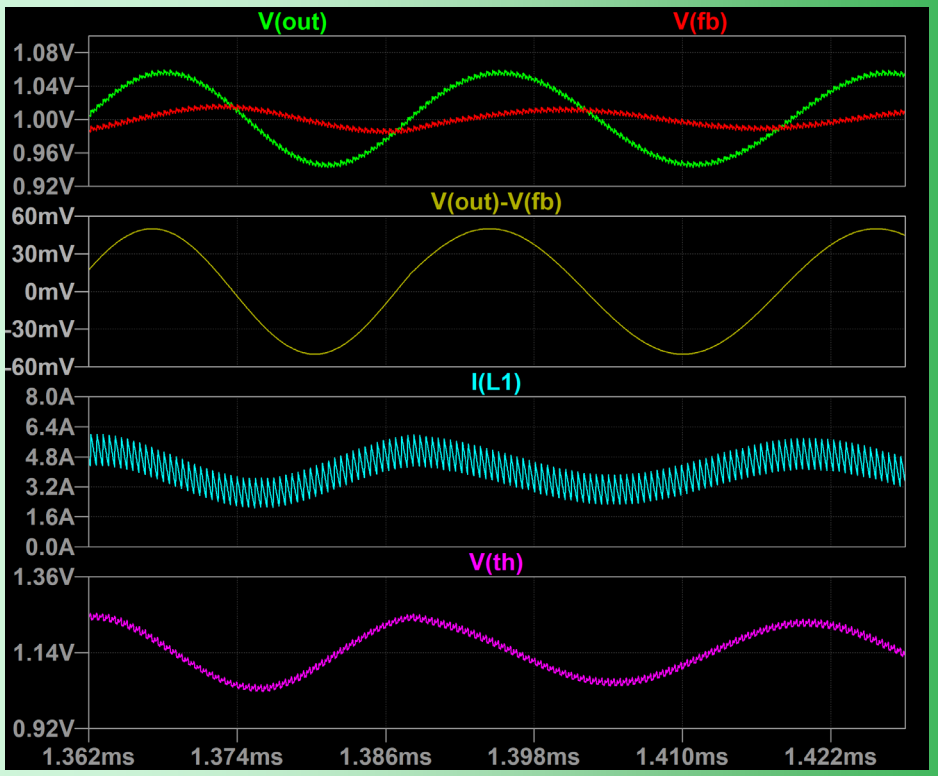
4b. Inspect the FRA transient waveforms

Ideally, sinusoidal pattern should be evident and symmetric

- Look for signs of non-linearity, which would indicate stimulus amplitude too large
- Note that there are discontinuities when the frequency changes – these are expected

Bad
too much stimulus





Good

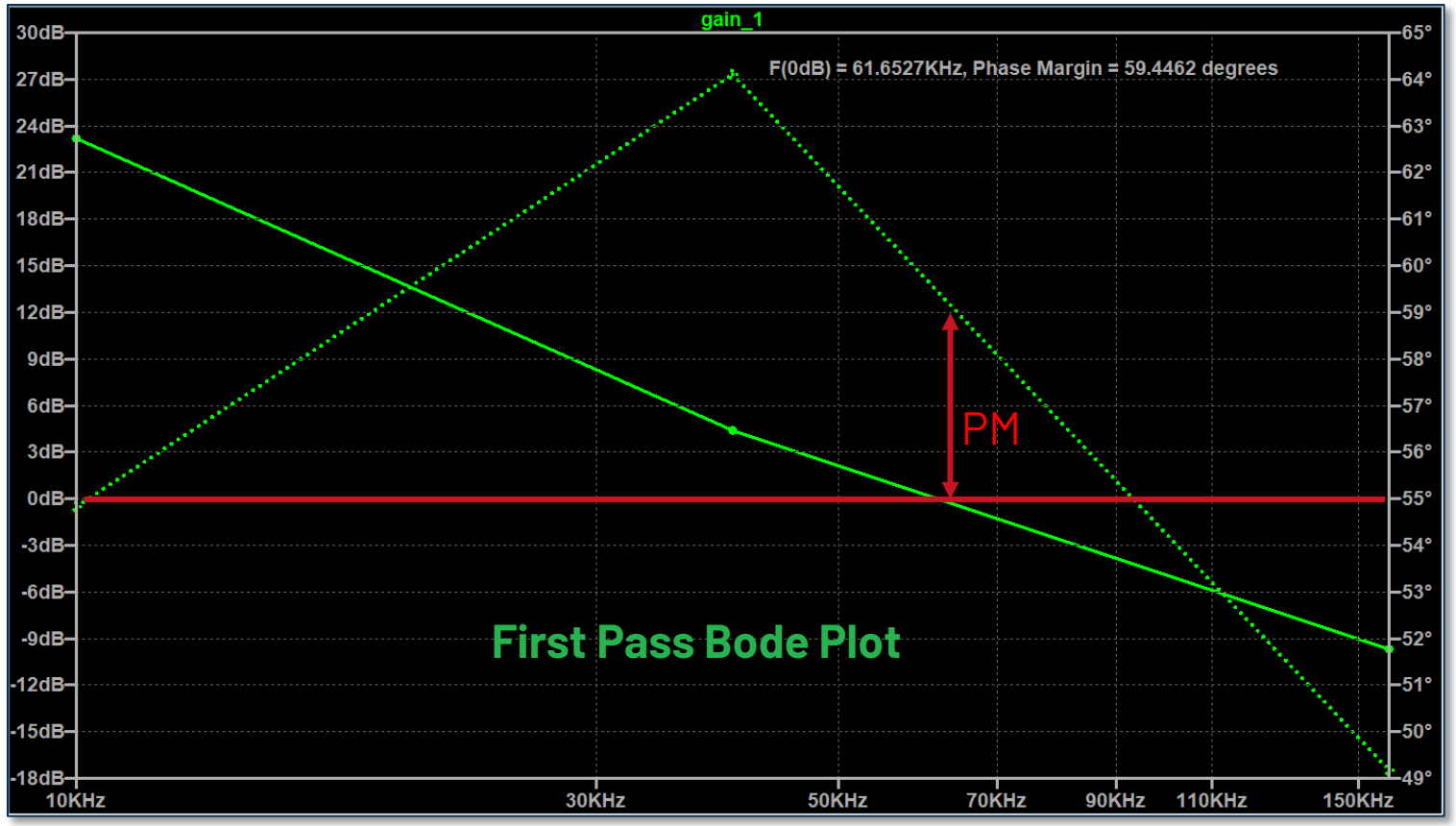
5. Initial Bode analysis

Find f_{0dB}

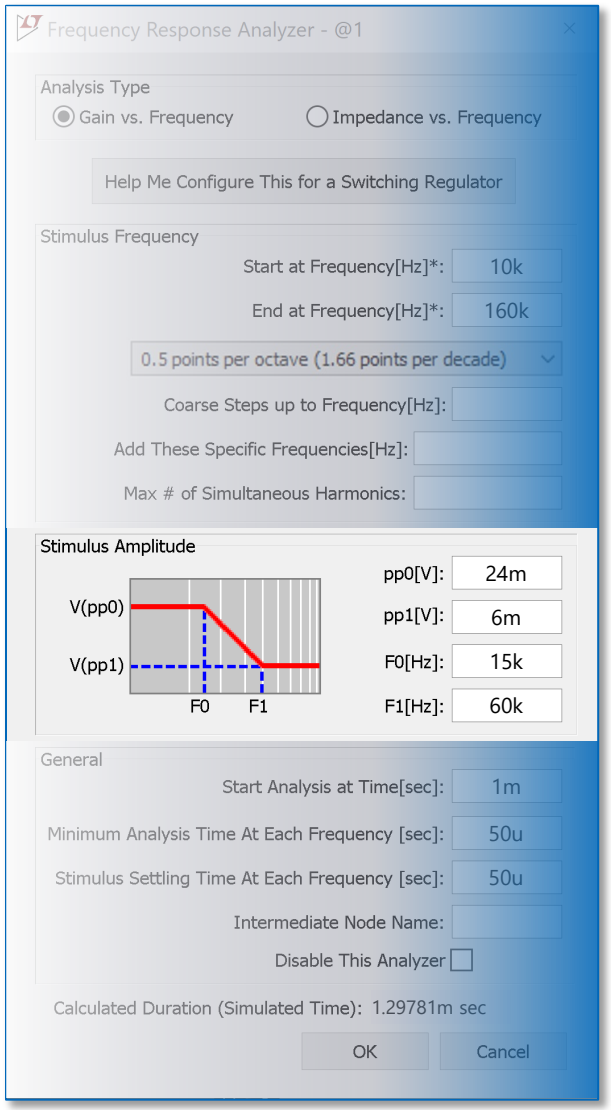
Adjust Fstart and Fend

- Fstart = $f_{0dB} \div 8$
- Fend = $2 \bullet f_{0dB}$

Re-run FRA



6. Stimulus amplitude (Rule of Thumb)



Specify frequency dependence

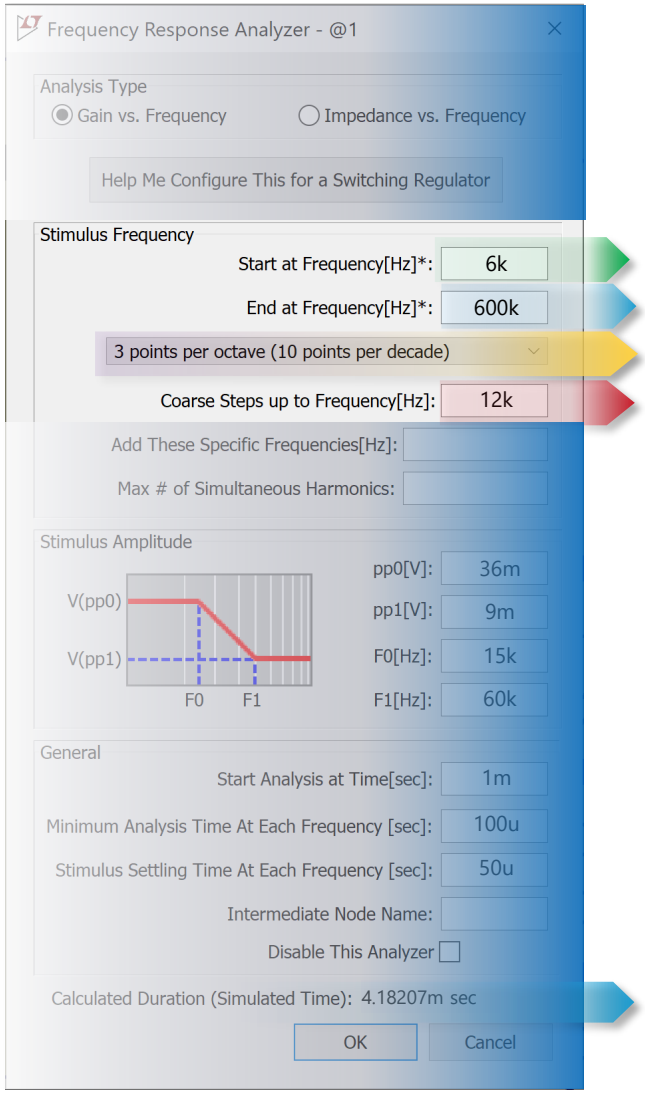
Need more signal at lower frequency due to high gain

Need less signal at higher frequency to avoid non-linear effects

A good starting point is:

- pp0 = V_{CM} ÷ 25~50
- pp1 = pp0 ÷ 4
- F0 = f_{0dB} ÷ 4
- F1 = f_{0dB}

7. Add more frequencies



Starting frequency ~f_{0dB} ÷ 10

- Lower Fstart leads to longer simulation time.
- Usually Fstart = f_{0dB} ÷ 10~20 is sufficient.

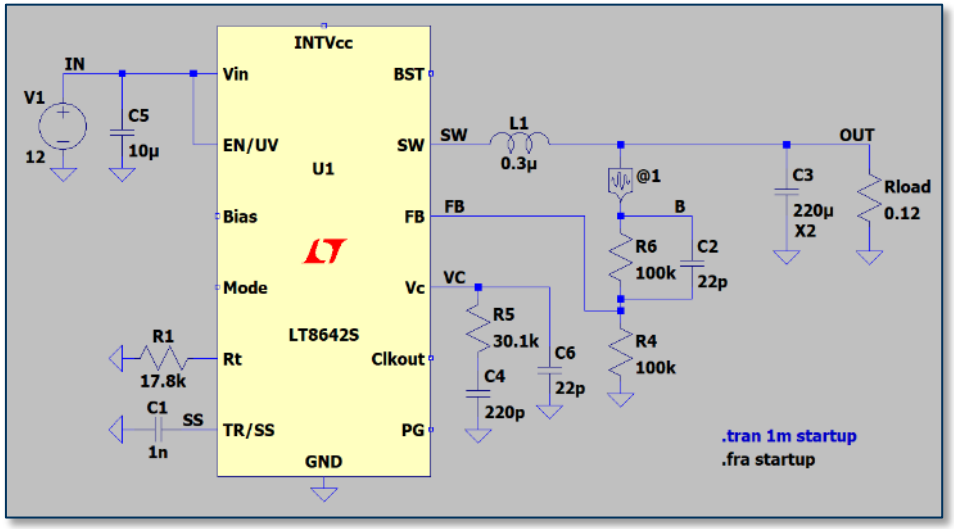
End frequency ~10 • f_{0dB}

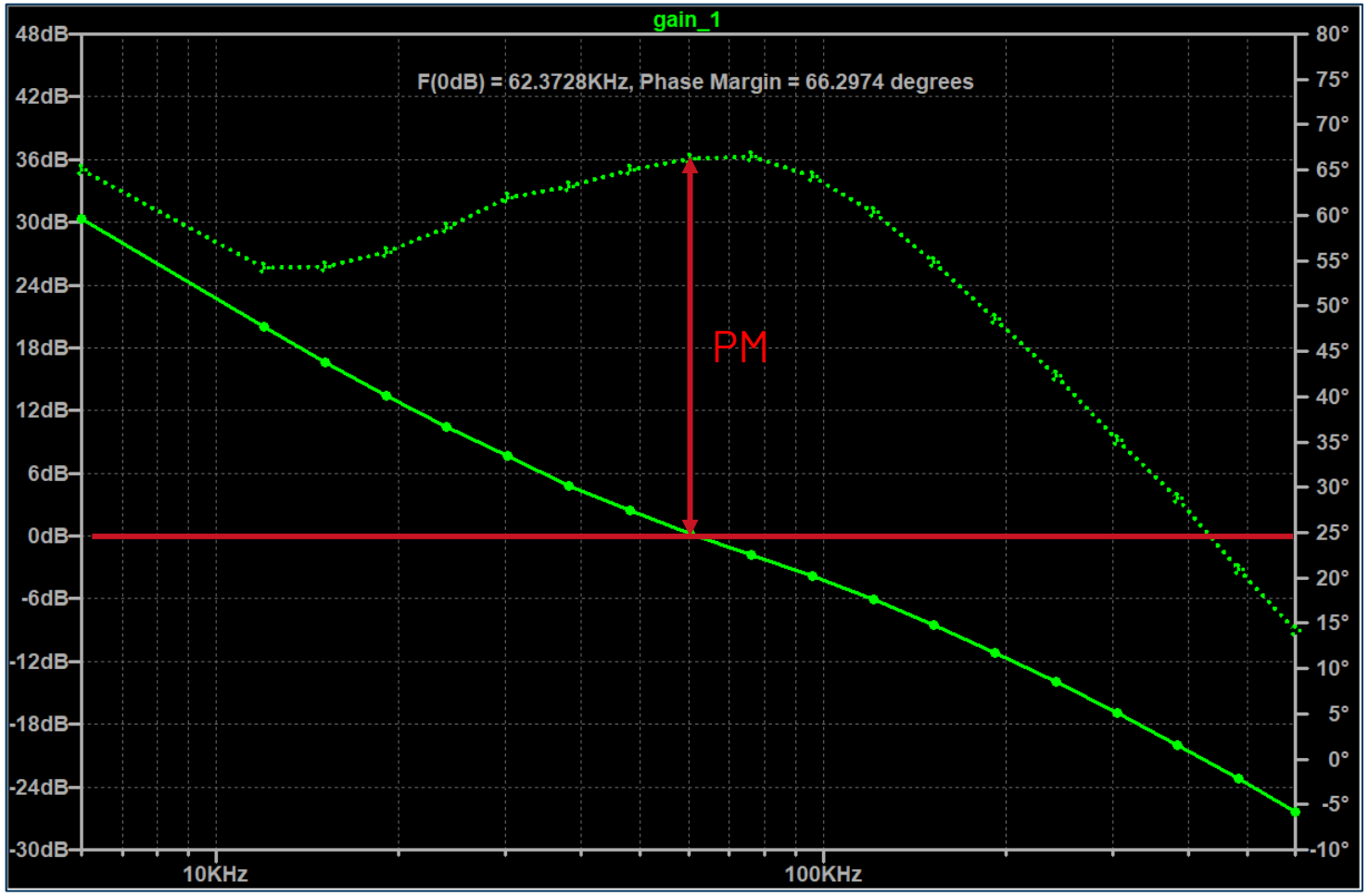
Increase frequency resolution to 2~3 points per Octave

Specify Fcoarse = 2 • Fstart

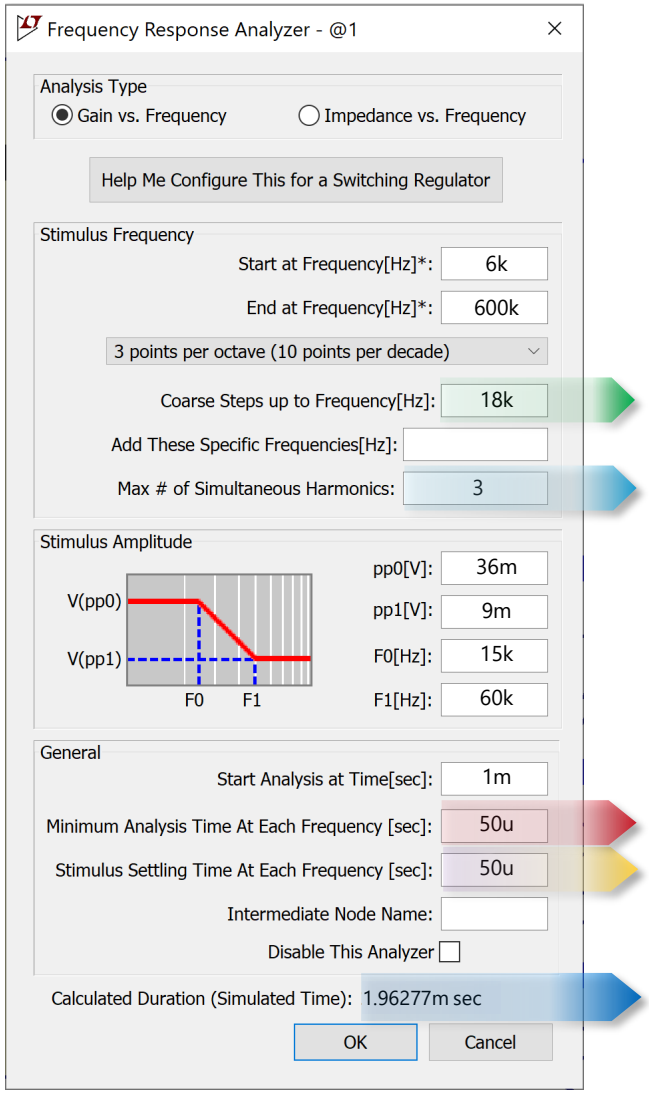
Note: The Simulation time will increase as we added more data points

Voila!





8. Speed up the FRA simulation



Increase Fcoarse (usually at least 2~3 • Fstart)

Increase max # of simultaneous harmonics (Nmax)

- Default is 1. Value of 2~4 can be quite beneficial.
- Note that this increases sensitivity to distortion → if increasing Nmax leads to phase/gain anomalies, reducing the amplitude may help
- The SPICE log indicates which harmonics are applied simultaneously

Decrease minimum analysis time (Tavgmin)

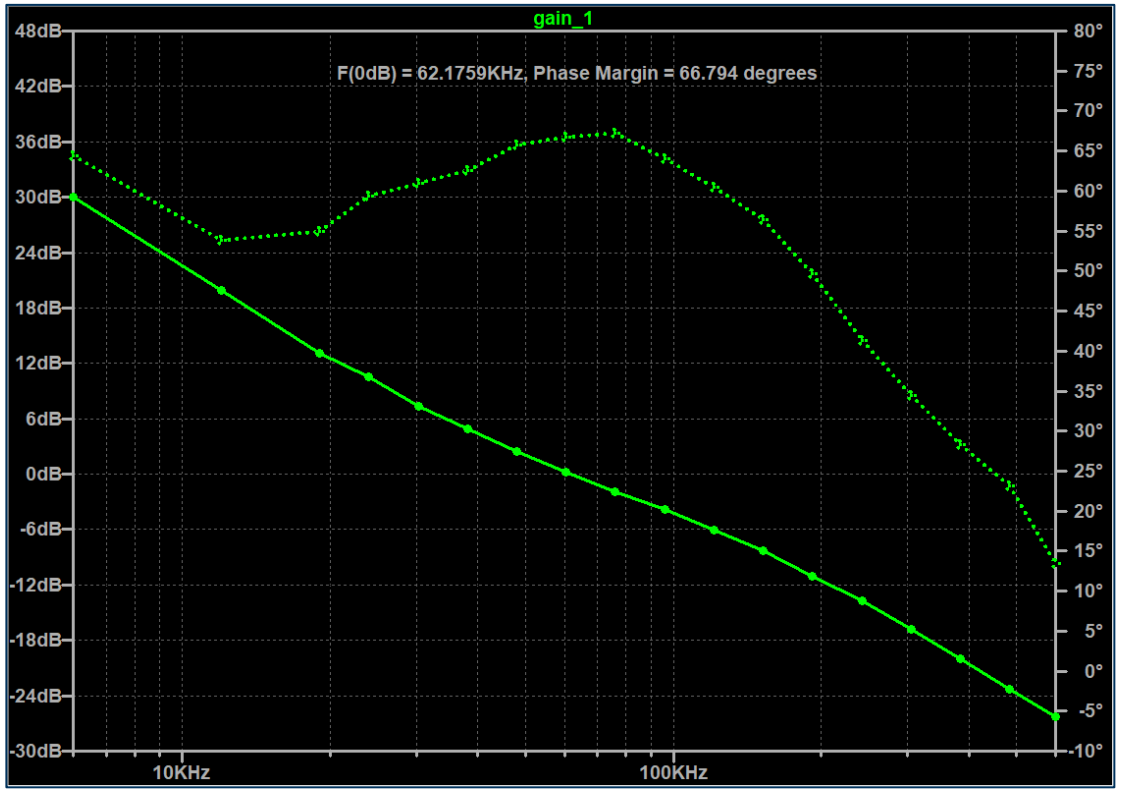
- If switching ripple is small relative to stimulus, less averaging is required (perhaps 50~100 ÷ f_{SW})
- Note that this only affects higher frequencies, so it's not worth making this too small

Reduce settling time (Tsettle) to 1~2 ÷ f_{0dB}

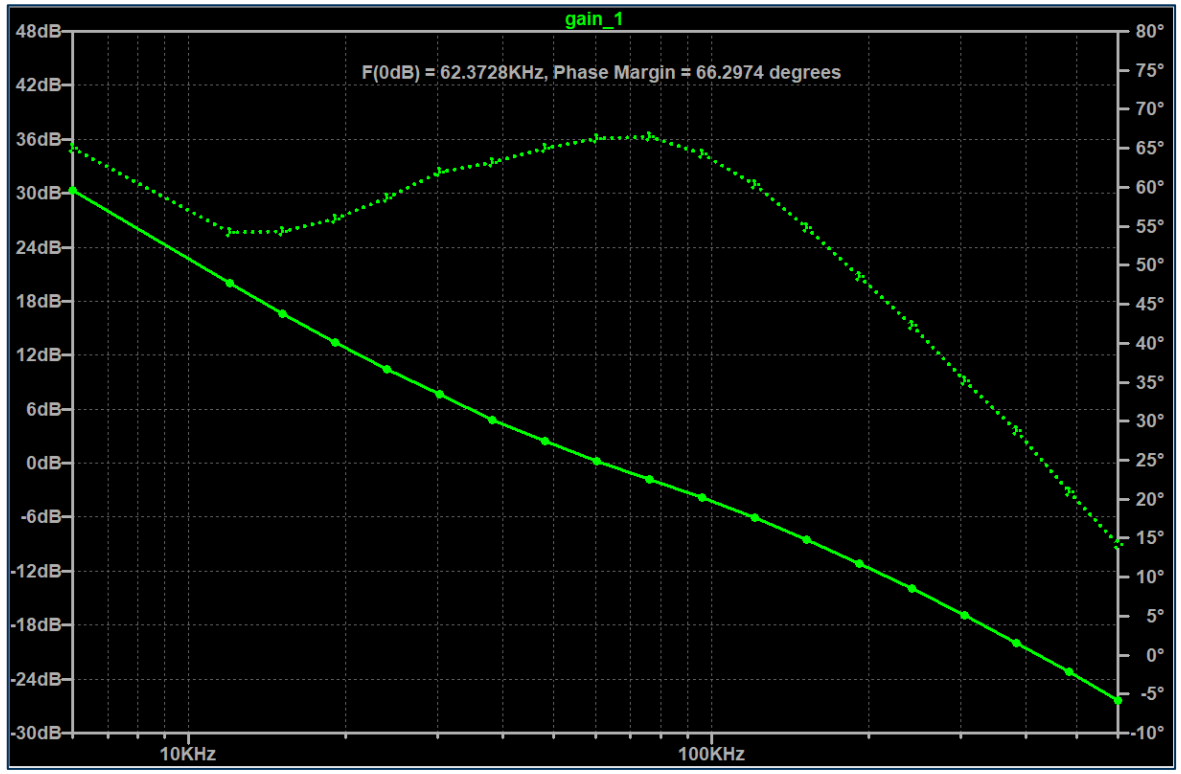
Pay attention to the sim time as you make changes

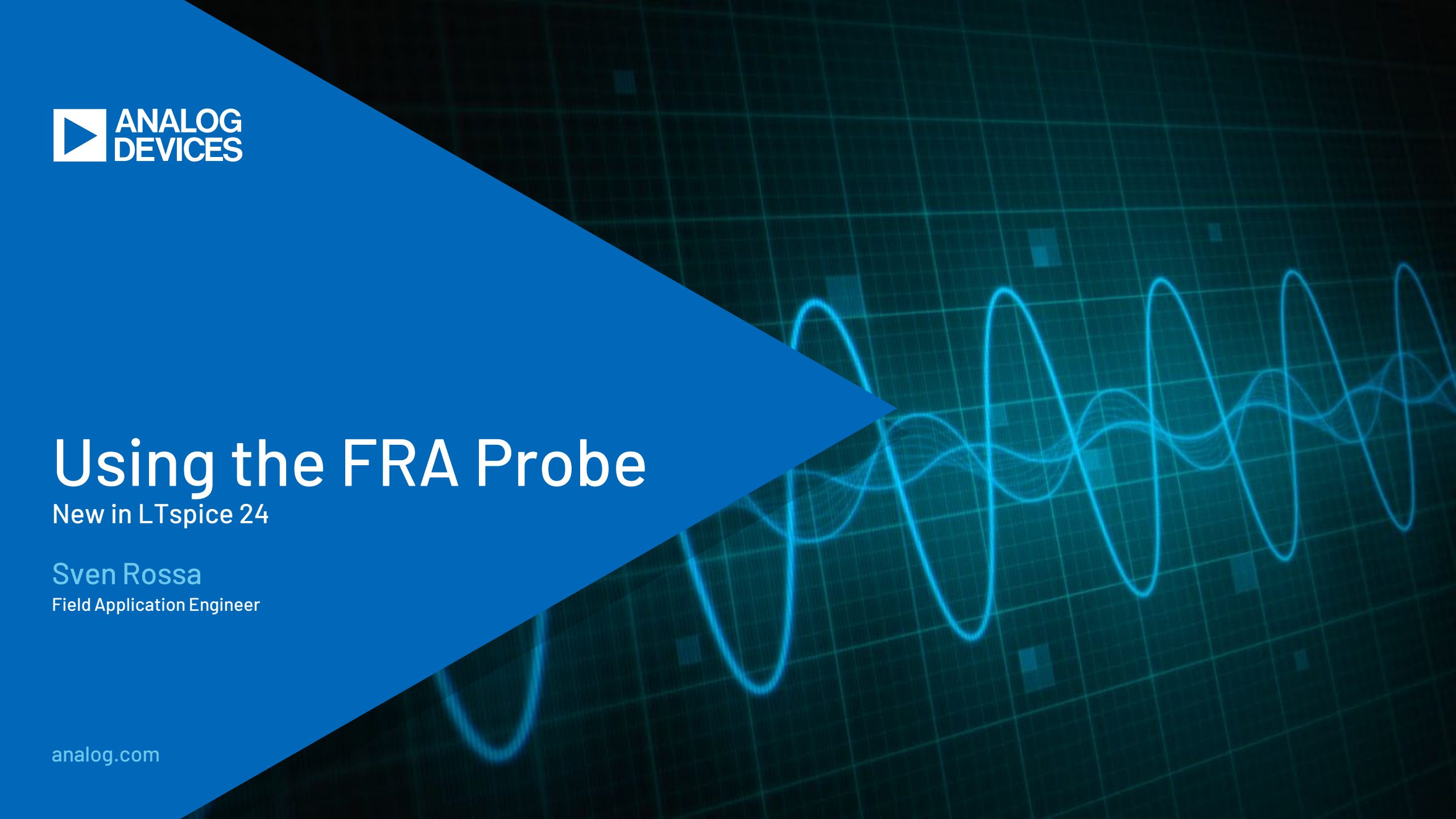
Presto!

Completed in 32 seconds



Completed in 70 seconds



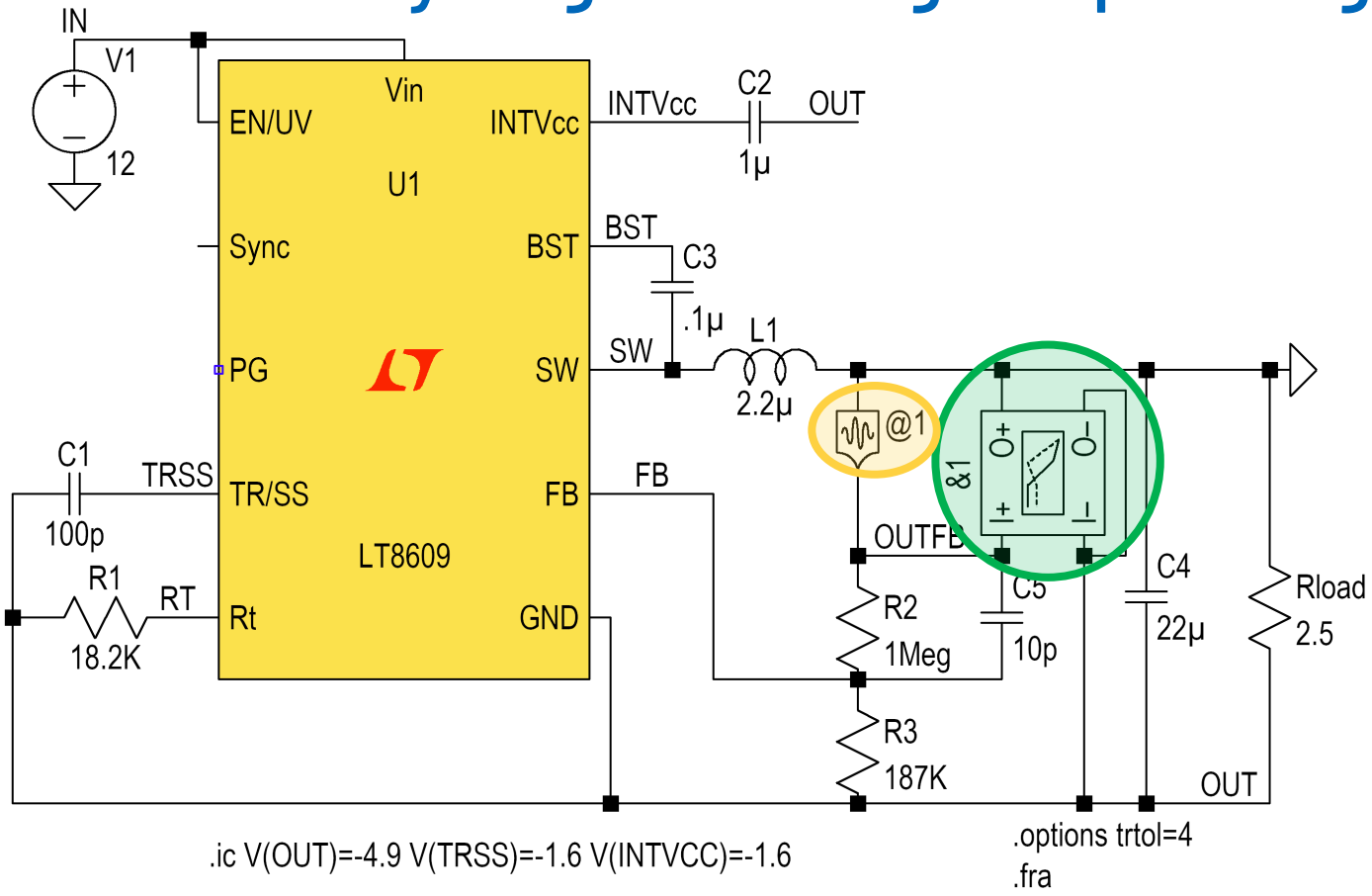


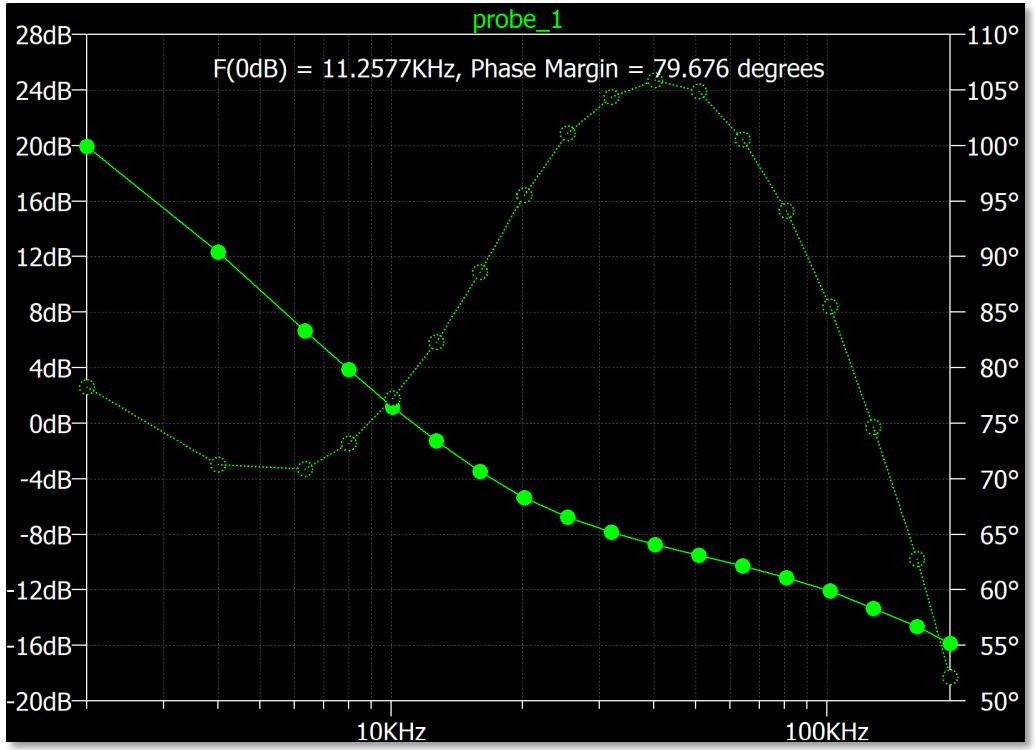
Using the FRA Probe

New in LTspice 24

Sven Rossa
Field Application Engineer

Ex. 1: Analyzing Inverting Output Regulators





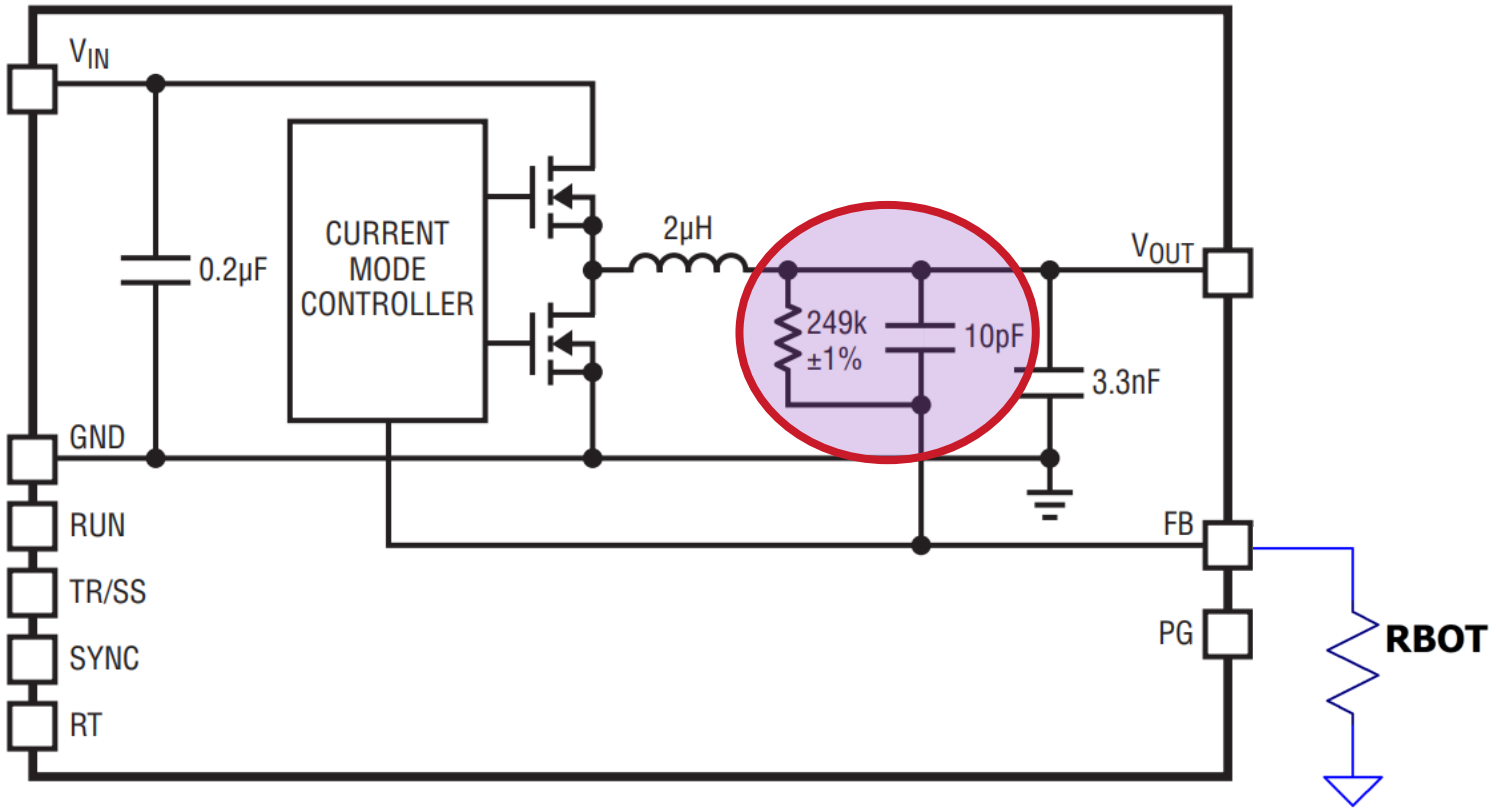
- Connect the positive (O+, I+) terminals of the **fraprobe** across the **fra stimulus device**, negative fraprobe terminals (O-, I-) to the negative output

Ex. 2: Analyzing µModules with Internal Feedback

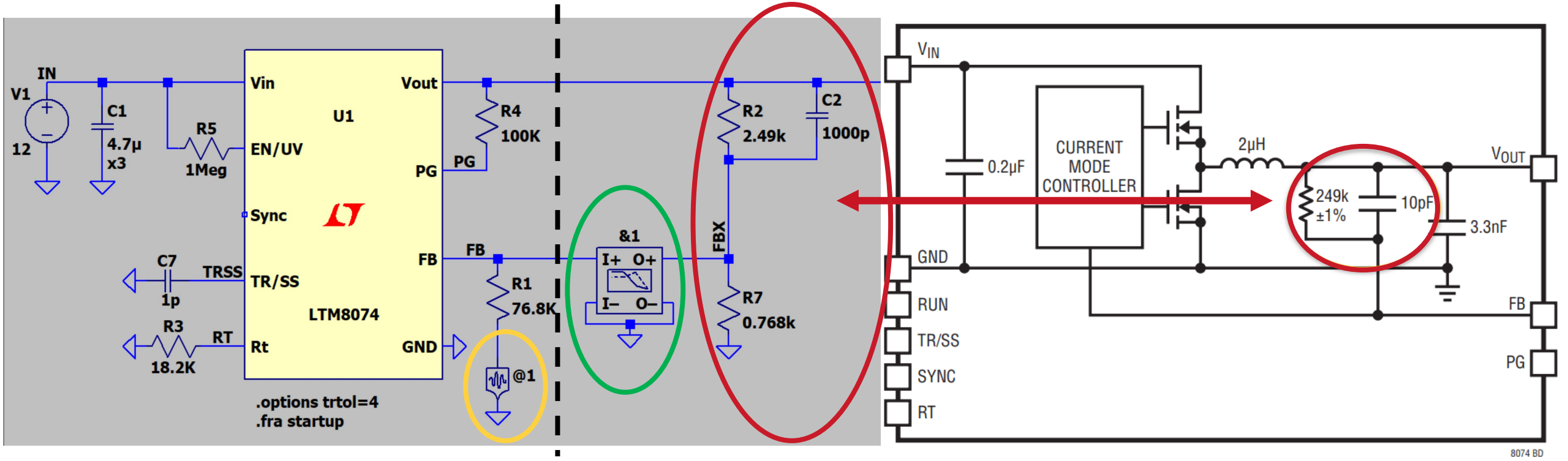
- Many µModules have **integrated feedback components**

  → There is no way to break the loop outside the module!

LTM8074 Block Diagram



Ex. 2 (cont): Analyzing µModules LTM8074 FRA to hardware testing



- Solution: Place external feedback divider, scaling 100x the current through the **internal components**
- Configure the **fra analyzer device** to stimulate the main loop
- Connect the **fraprobe** to analyze the loop gain

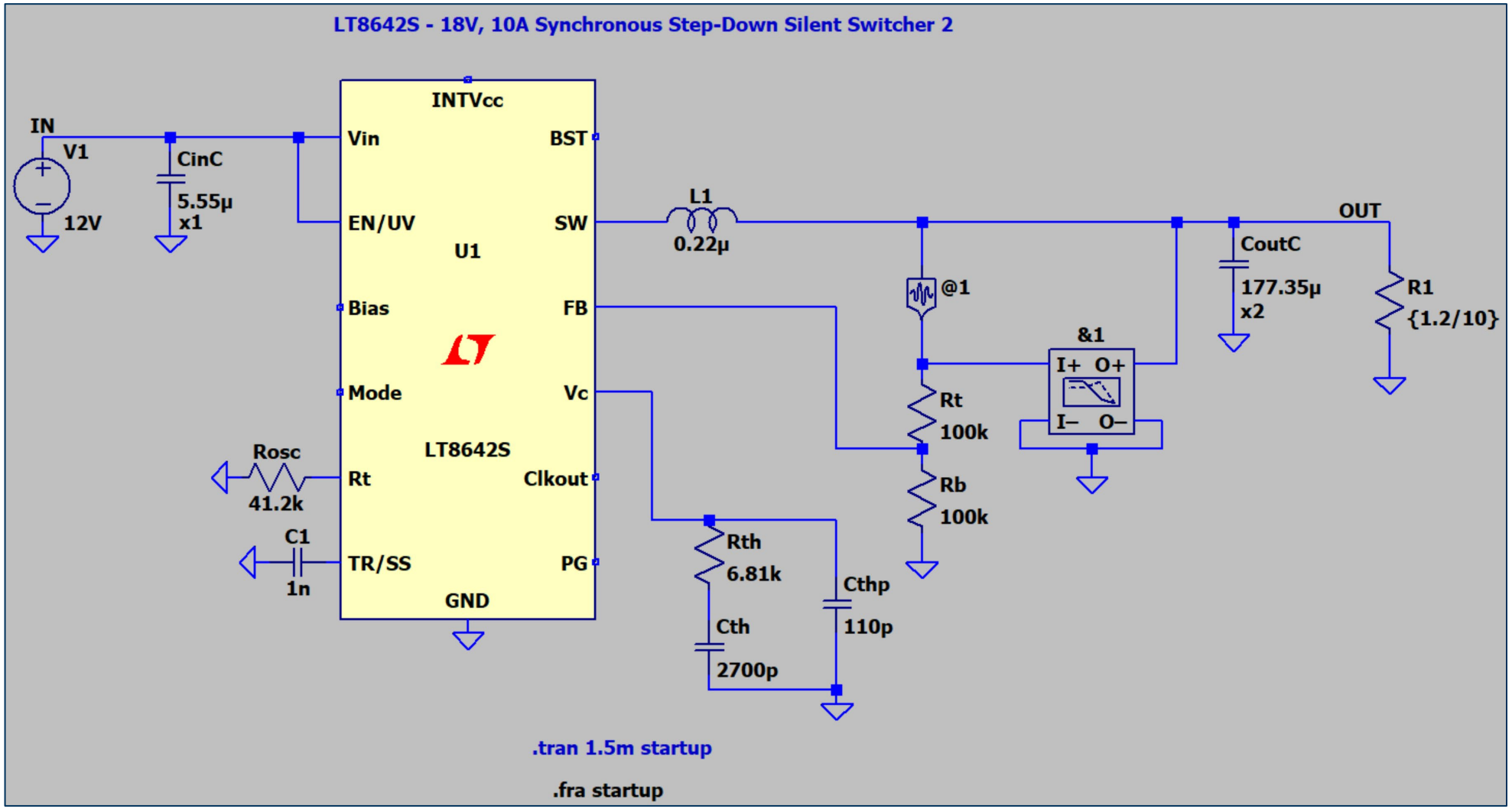
Note on Tool Correlation

LTspice and LTpowerCAD

Sven Rossa
Field Application Engineer

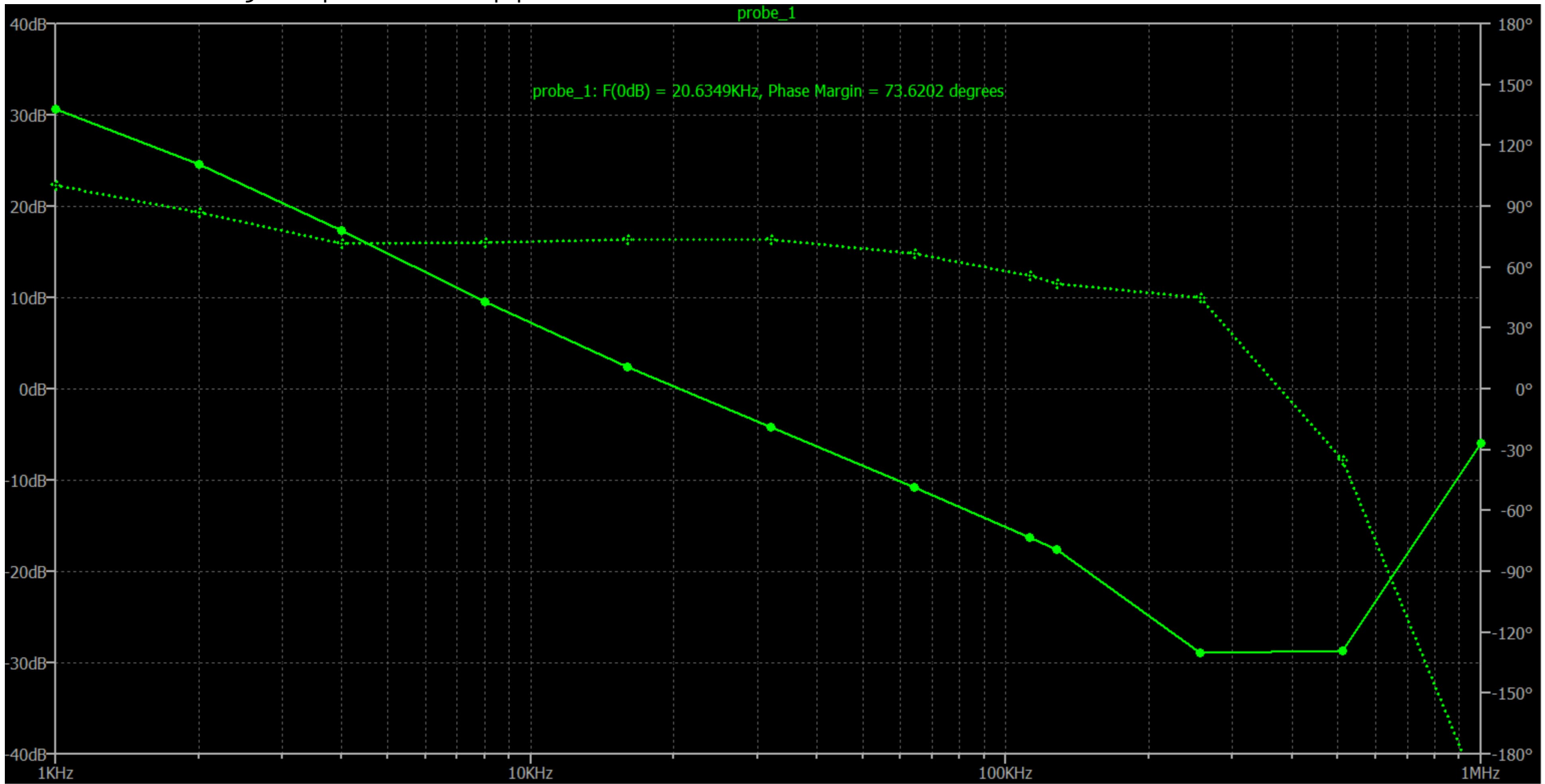
FRA: Bode Plot Agreeance

- Circuit exported from LTPOWERCAD
  - FRA Device / FRA Probe configured per “FRA setup procedure” section

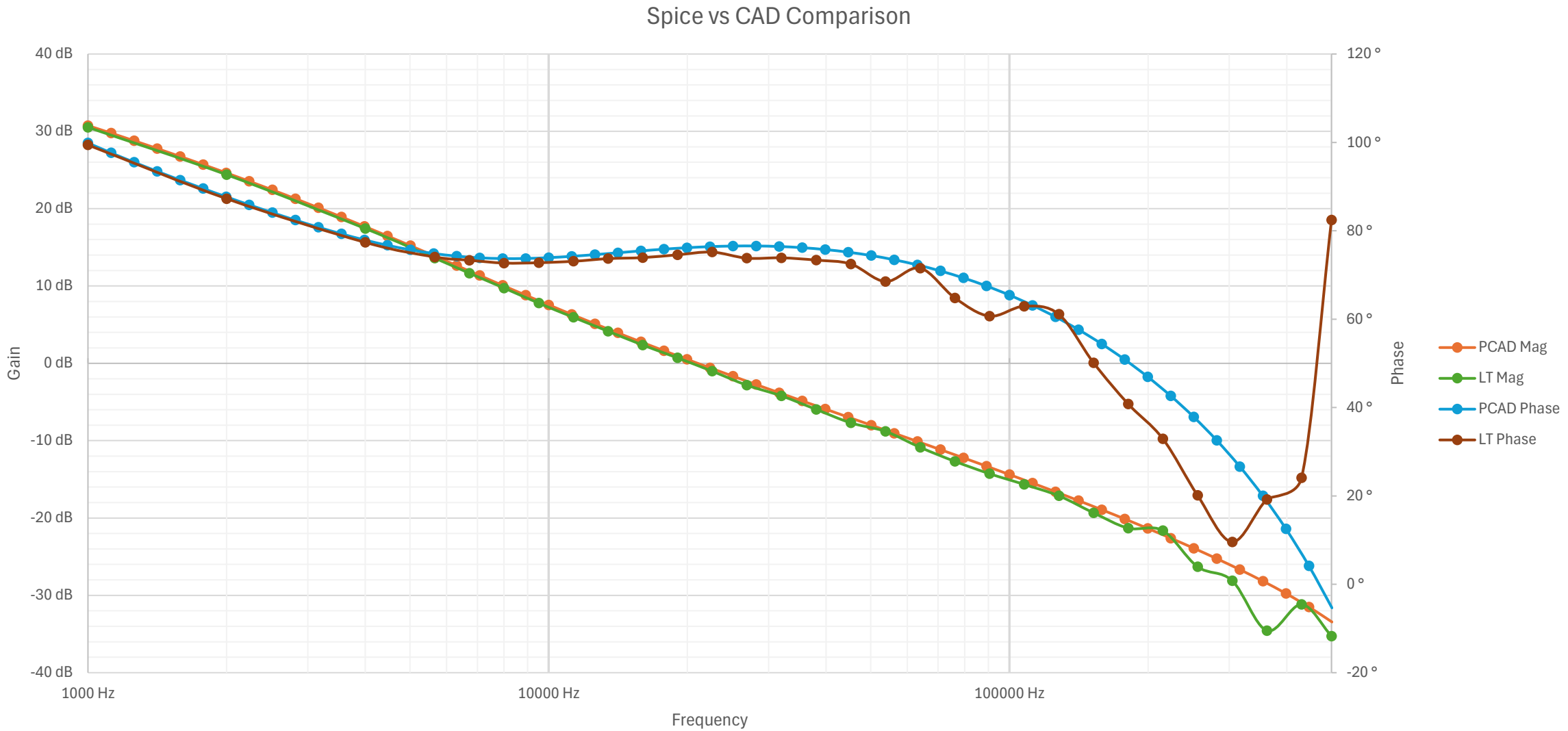


FRA: Bode Plot Agreeance

- Circuit exported from LTPOWERCAD
  - FRA / FRA Probe configured per “FRA setup procedure” section



FRA: Bode Plot Agreeance



Questions?