

Agenda

08:30 – 09:00	<i>Arrival / Registration / Coffee</i>
09:00 – 09:50	SMPS Topologies, tips and tricks (Analog Devices)
09:50 – 10:45	Filtering Considerations for DC/DC Converters (Wurth Electronics)
10:45 – 11:10	<i>Coffee Break & Networking Opportunity</i>
11:10 – 12:00	The Art of Loop Compensation (Wurth Electronics)
12:00 – 13:00	<i>Lunch</i>
13:00 – 13:50	LTspice Examples (Analog Devices)
13:50 – 14:45	Smart Selection of Inductors and Capacitors (Wurth Electronics)
14:45 – 15:10	<i>Coffee Break & Networking Opportunity</i>
15:10 – 16:00	PCB Board Layout Optimisation (Analog Devices)



LTspice examples

Frederik Dostal

Power Management Expert

analog.com



Agenda

New in LTspice24

Simulating loop stability

LTpowerCAD for loop analysis

Simulating Tollerances with Monte Carlo

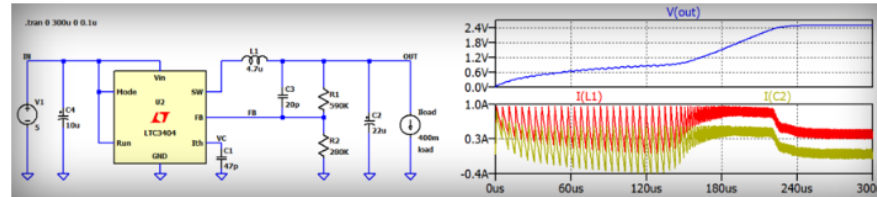
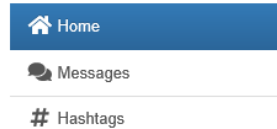
Simulating behavior of a power switch

LTspice Group.io User's Group



<http://groups.io/g/LTspice>

Several hundred posts per month



LTspice LTspice@groups.io

This group is dedicated to LTspice. It's independent from the owner of LTspice (ANALOG DEVICES (ADI) / Linear Technology).

LTspice is a free SPICE program for electronic circuit simulation.

The old LTspice group <https://groups.yahoo.com/neo/groups/LTspice/info> has been integrated into this group - messages, files and members have been merged. There is an additional folder with zip-files containing the files from the Yahoo group - <https://groups.io/g/LTspice/files/LTspiceFiles>.

Please don't attach files to your message. Instead upload **attachements** to the folder Temp -

<https://groups.io/g/LTspice/files/Temp>.

Don't discuss in the topic "New file uploaded ...". The messages in this topic will be regularly deleted. Instead start a new topic with a useful subject title.

Group Information

<http://www.analog.com/LTspice>

64,634 Members

20,626 Topics, Last Post: 9:47am

Started on 9/27/02

[Feed](#)

Group Settings

All subscribers can post to the group.

Posts to this group do not require approval from the moderators.

Posts from new users require approval from the moderators.

Messages are set to reply to group.

Subscriptions to this group do not require approval from the moderators.

Archives are visible to anyone.

Wiki is visible to subscribers only.

Members can set their subscriptions to no email.

Top Hashtags [\[See All\]](#)

#questions 11

#circuitmodels 1

Group Information

<http://www.analog.com/LTspice>

64,634 Members

20,626 Topics, Last Post: 9:47am

Started on 9/27/02

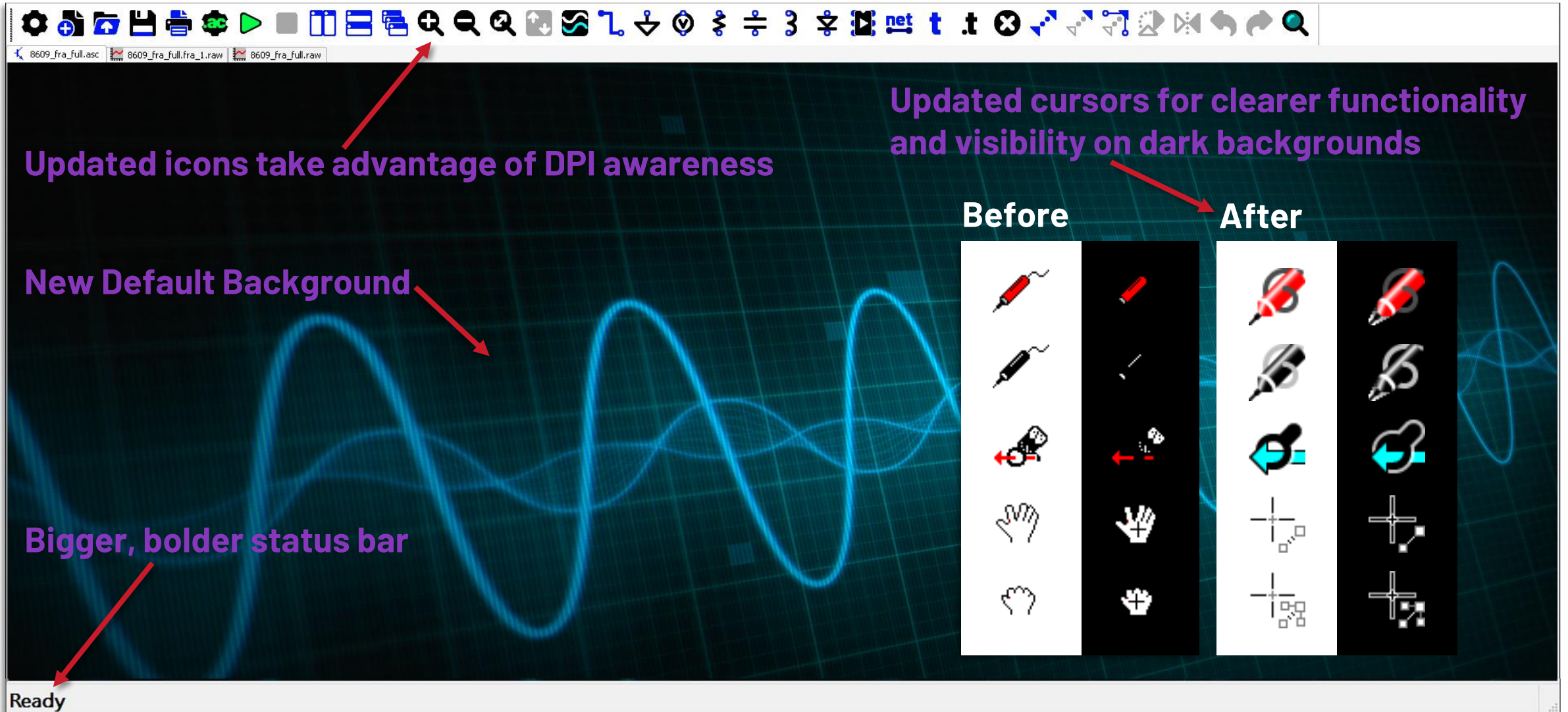
[Feed](#)



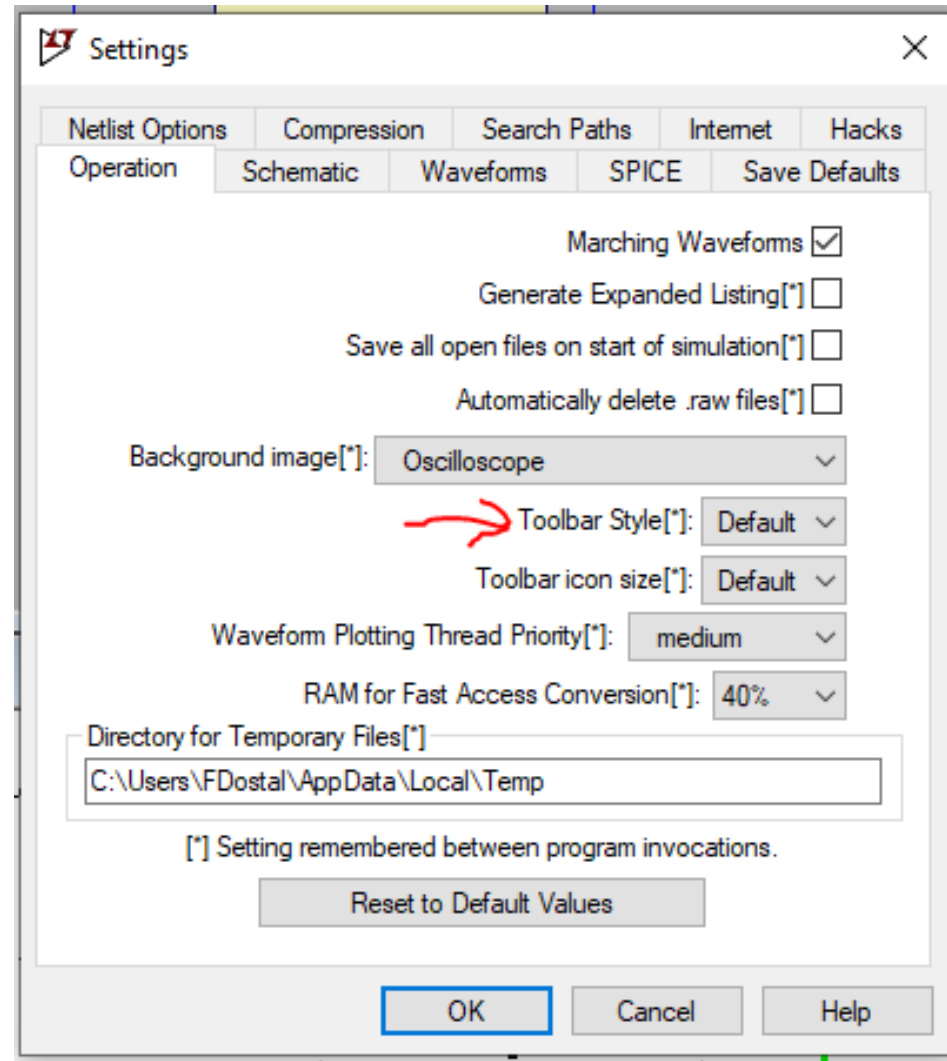
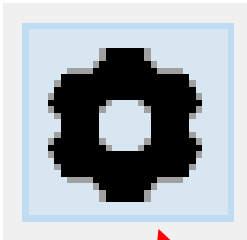
New in LTspice24

analog.com

LTspice 24 Refresh Overall Look and Feel



Revert back to classic toolbar style possible



Simulation Control



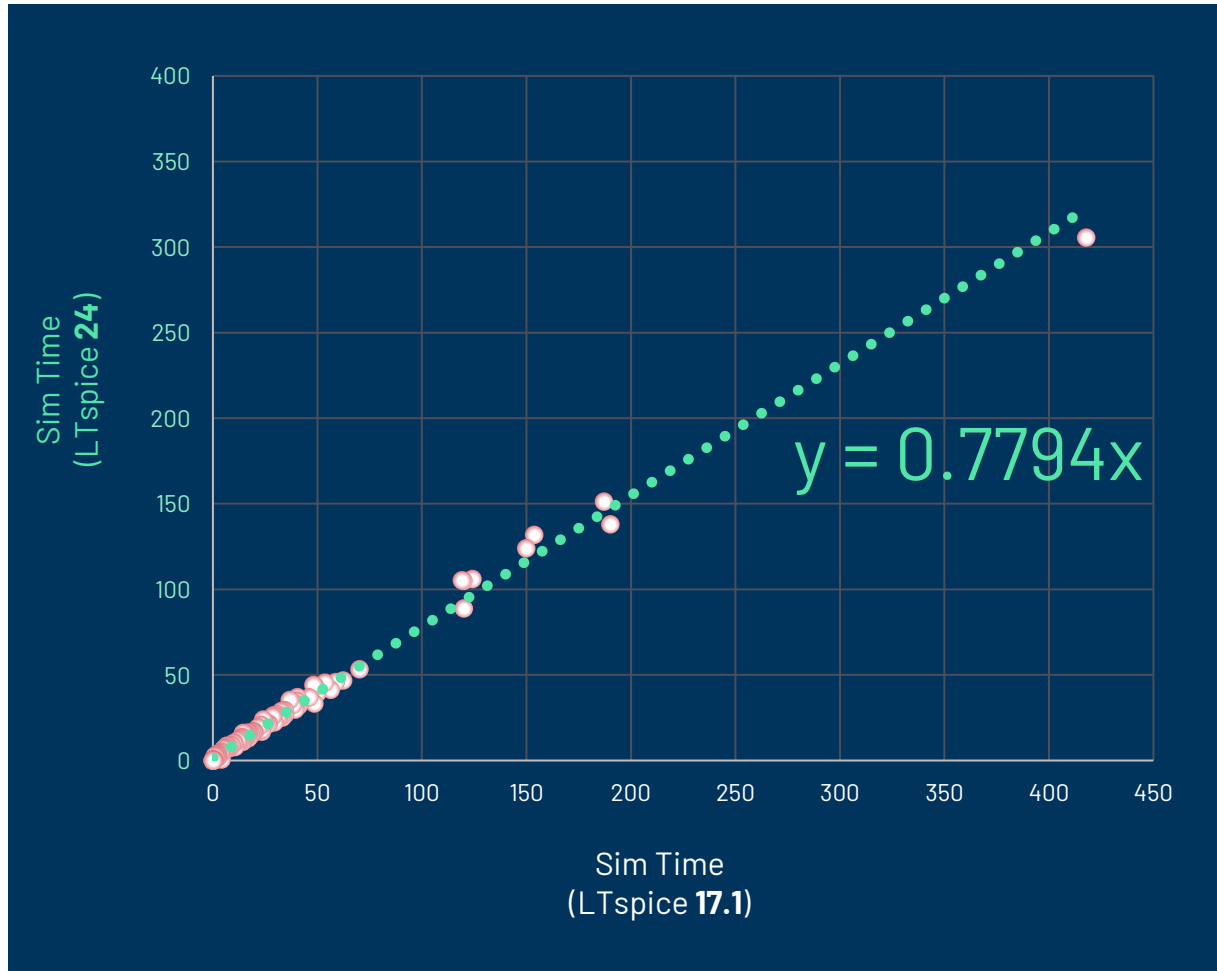
New **Configure Analysis** Toolbar Button and Shortcut ("A")

Improved Configure Analysis Dialog Functionality

- Captures all simulation commands on the schematic, *including comments*
- Populates tabs accordingly
- Automatically comment/uncomment schematic text

Shift + Left-Click toggles text between **directive** and **comment**

LTspice 24: Faster Simulations



- ▶ Improved simulation speed
 - Benchmarked ~200 popular MMP examples
 - ADI-standard Dell i7 Precision 5550 laptop
- ▶ Improved run-to-run consistency
- ▶ Changed default trtol to 2 for further improved performance

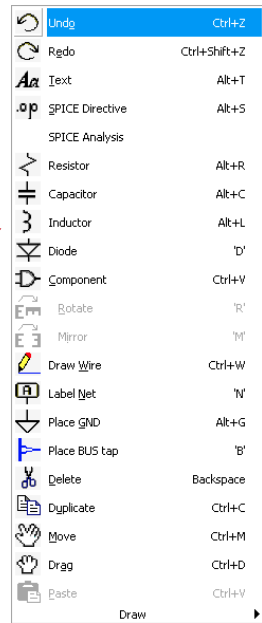
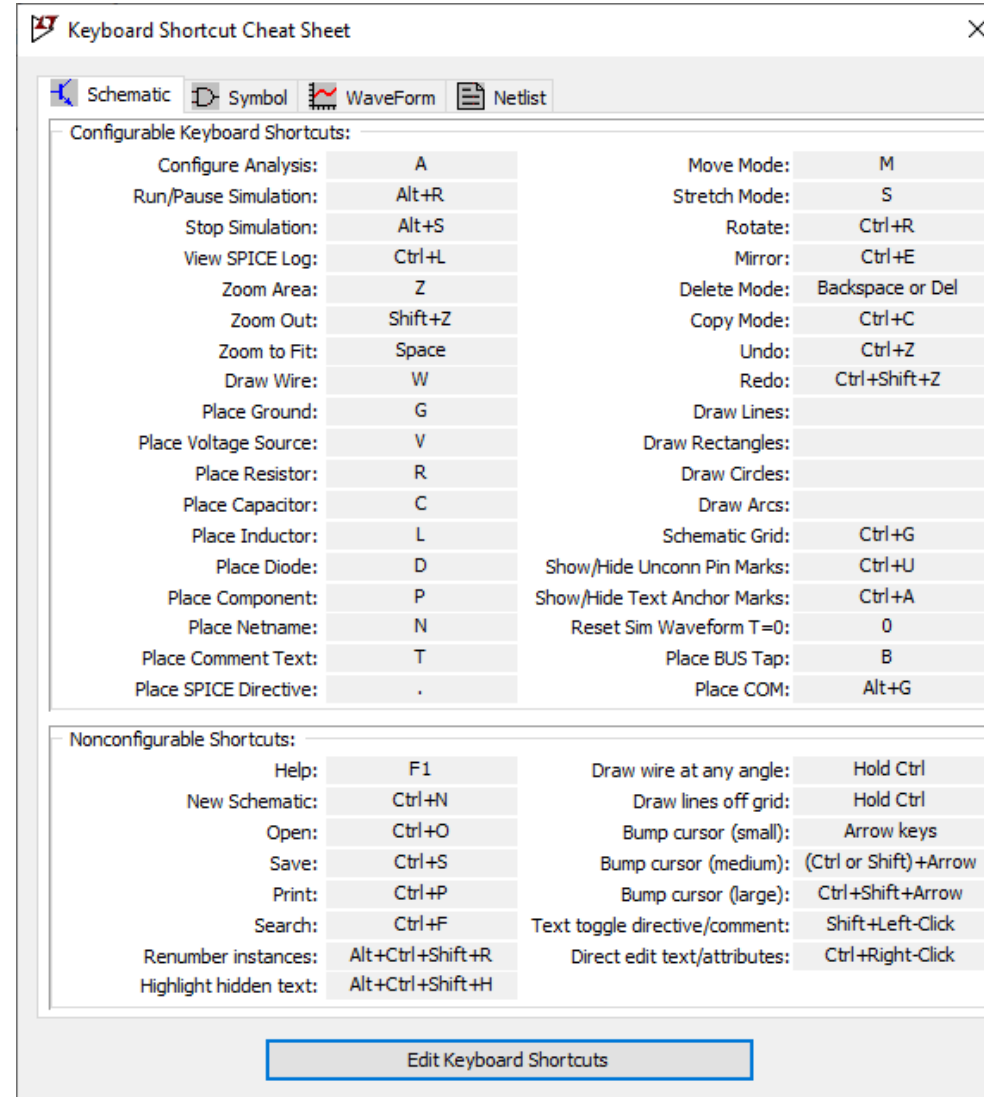
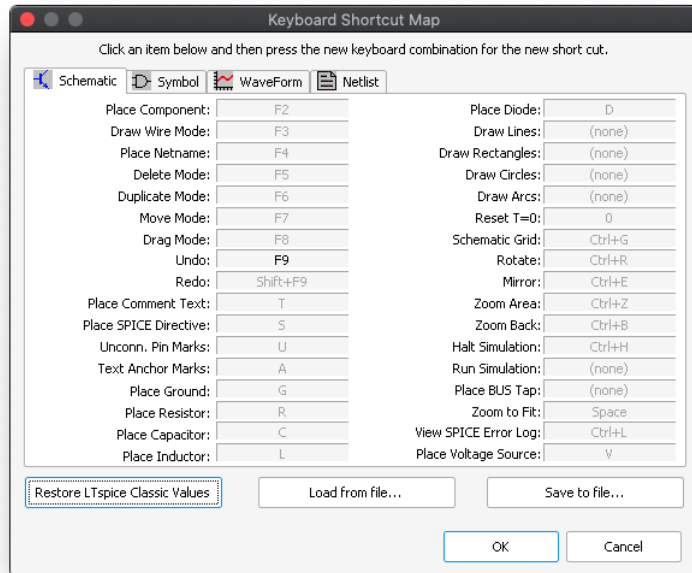
New Keyboard Shortcuts and Dynamic Cheat Sheet

Customization-safe

Return to old shortcuts via

Restore LTspice Classic Values

New Non-Modal, Floating Cheat Sheet Available from Help Menu



Frequency Response Analysis (FRA) Upgrades

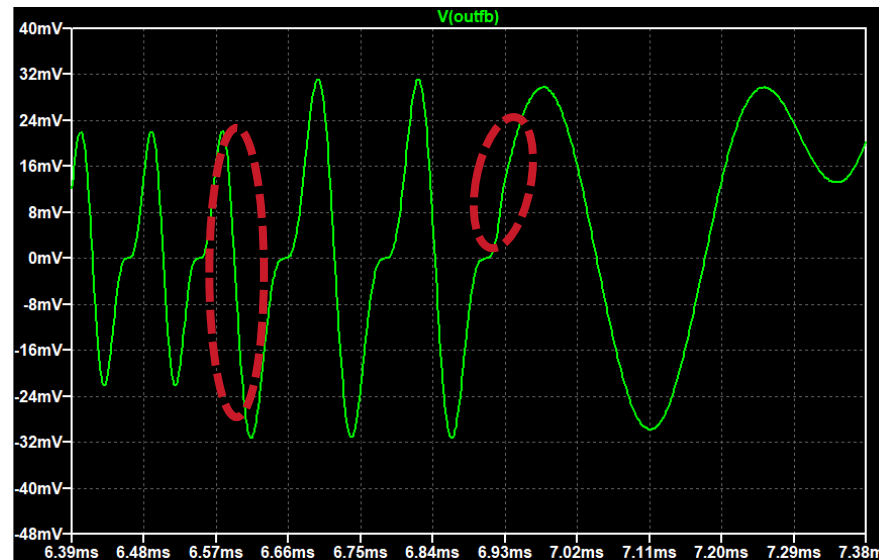
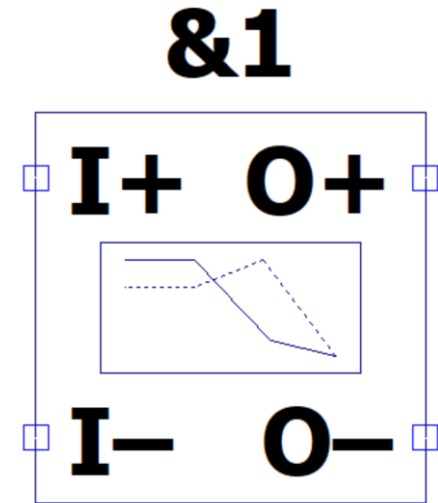
4-terminal Frequency Response Analyzer Probe

- Enables Bode plots of any part the loop
- Simplifies analysis of μ Modules with integrated top feedback resistors; negative outputs; and current feedback

Phase changed to represent phase margin (phase +180°)

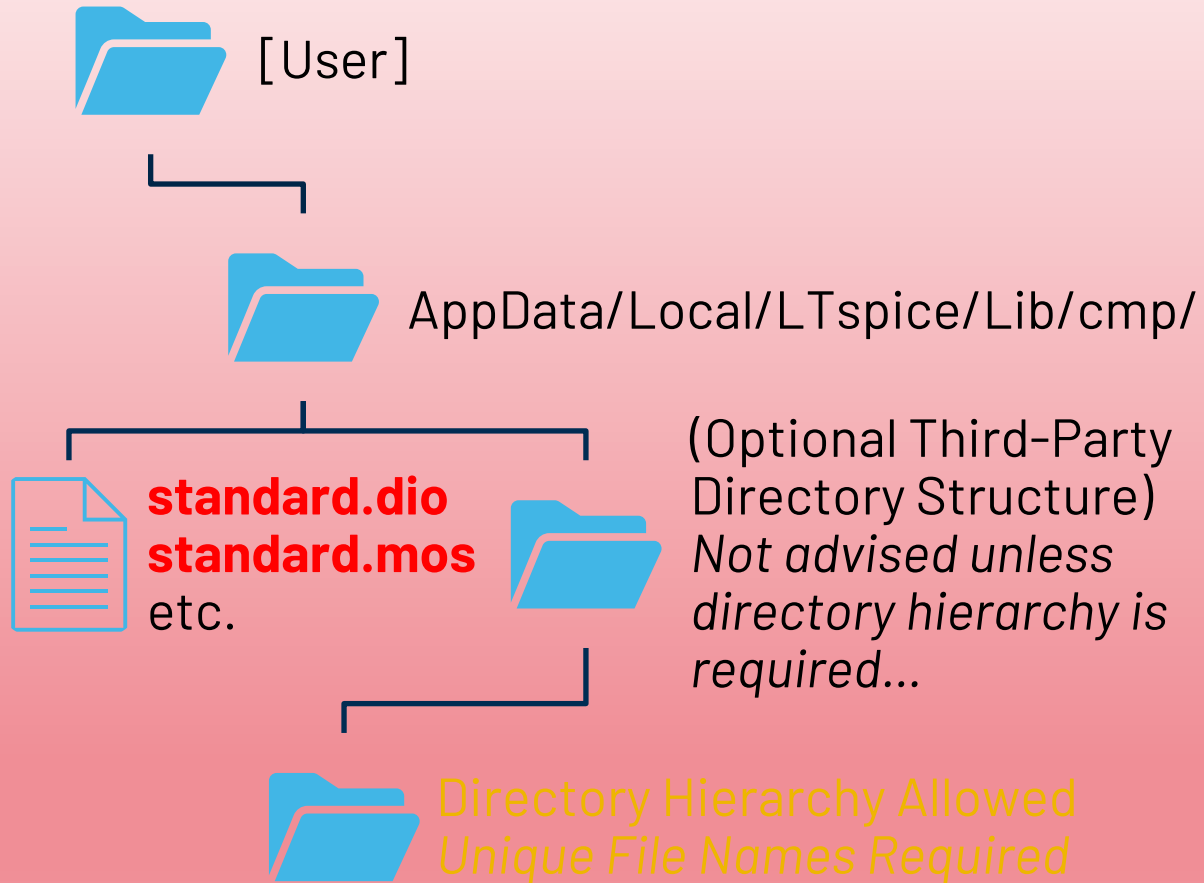
Smooth stimuli transitions between frequencies

- Faster settling / improved accuracy

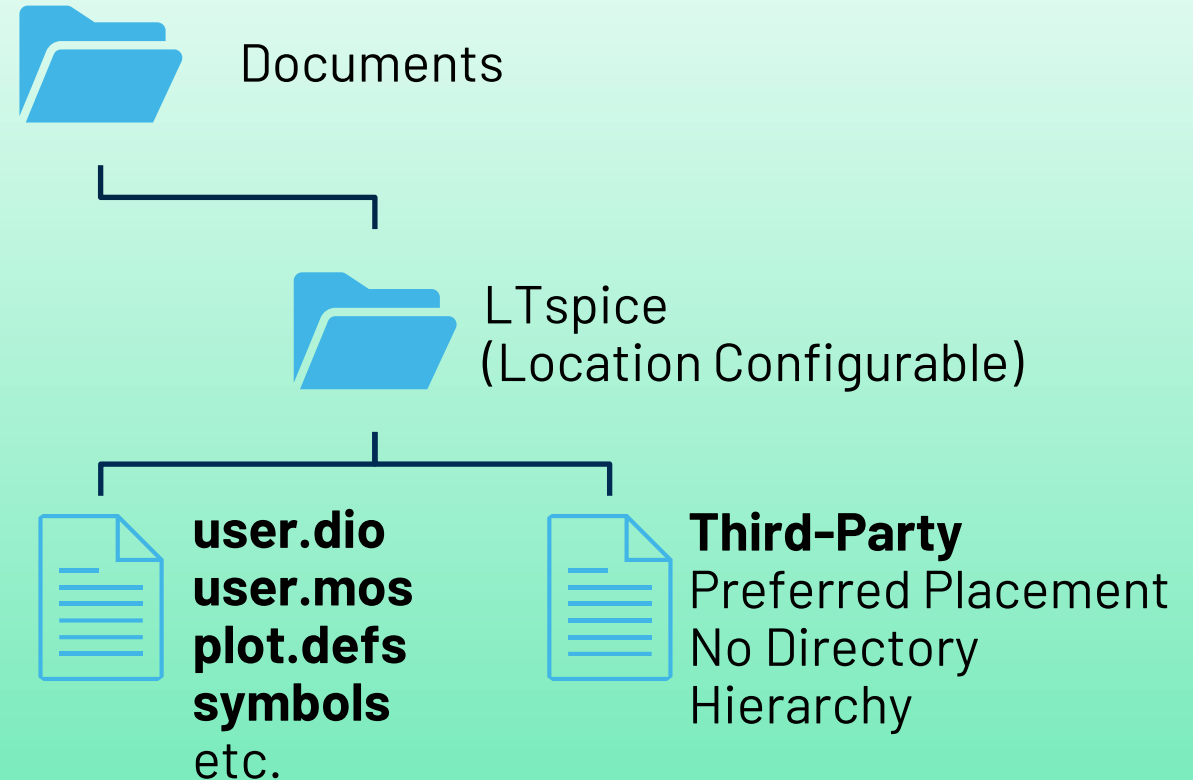


Component Libraries and AppData

LTspice Installs/Overwrites Files Here



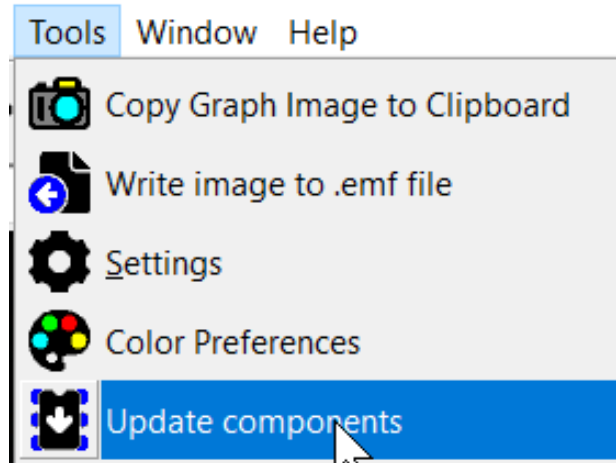
User Files Should be Placed Here



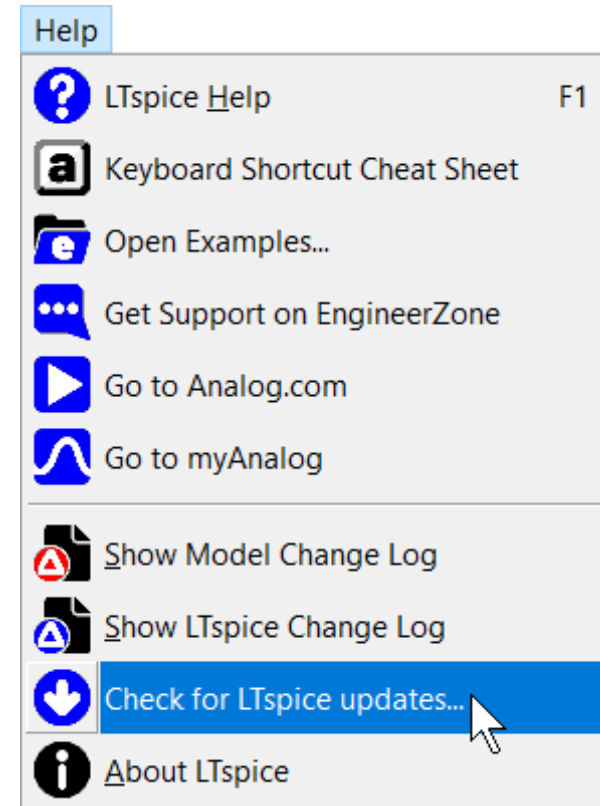
Components / Software may be separately updated

New since Ver. 24.

Update Components



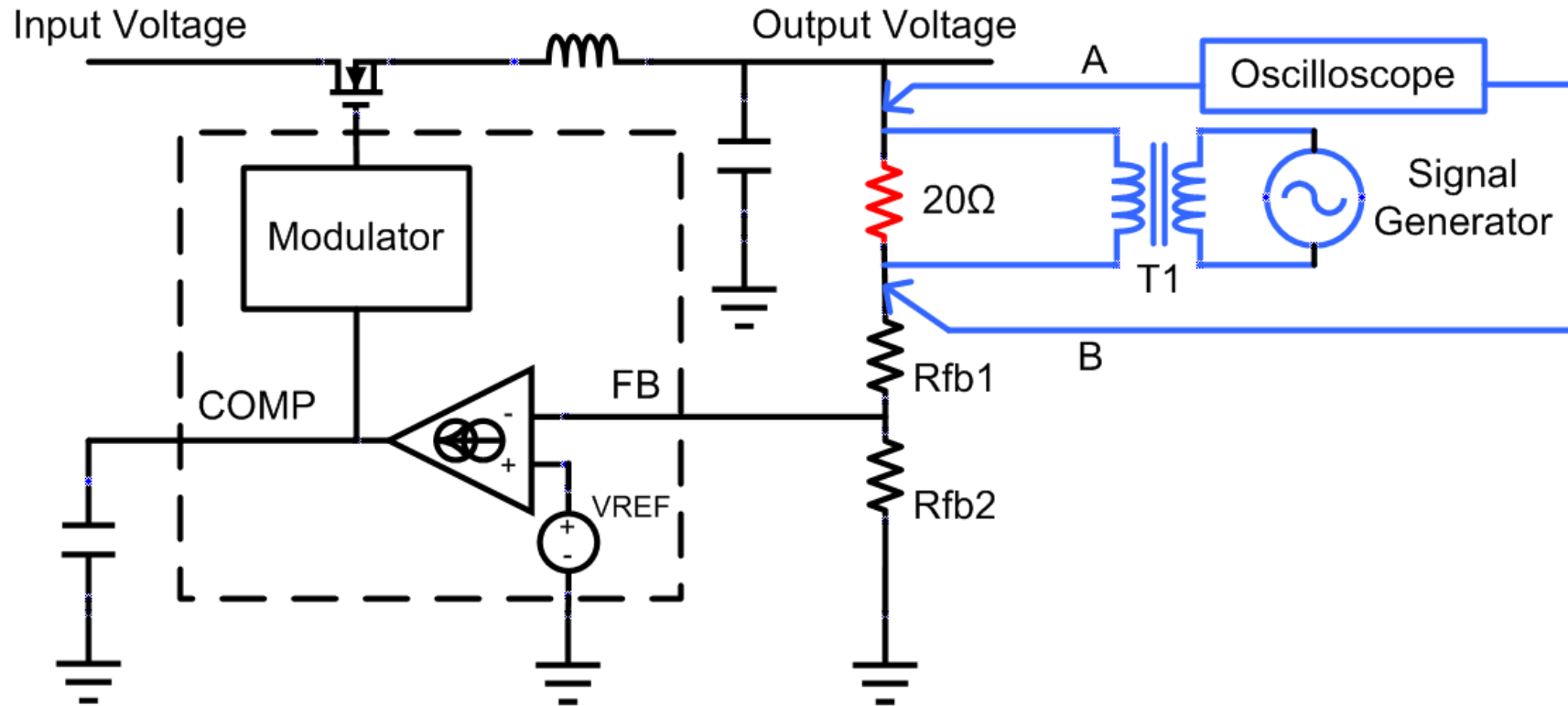
Update LTspice



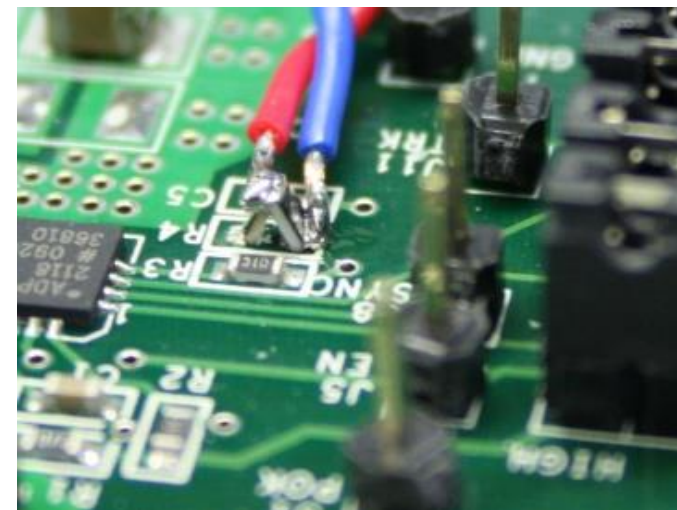
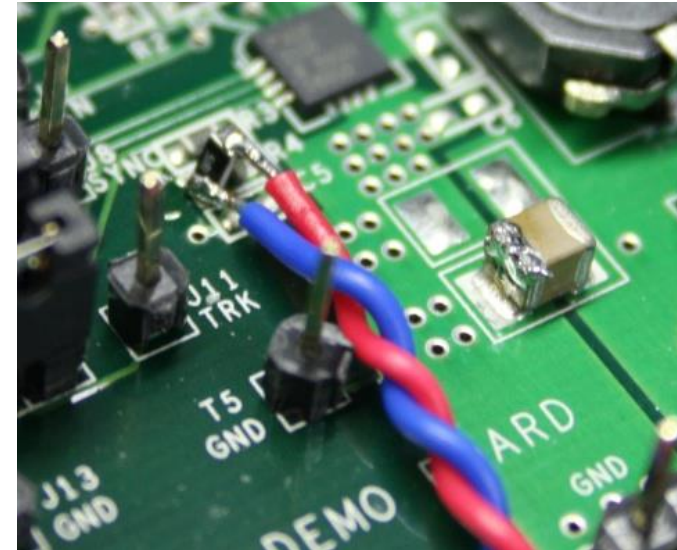
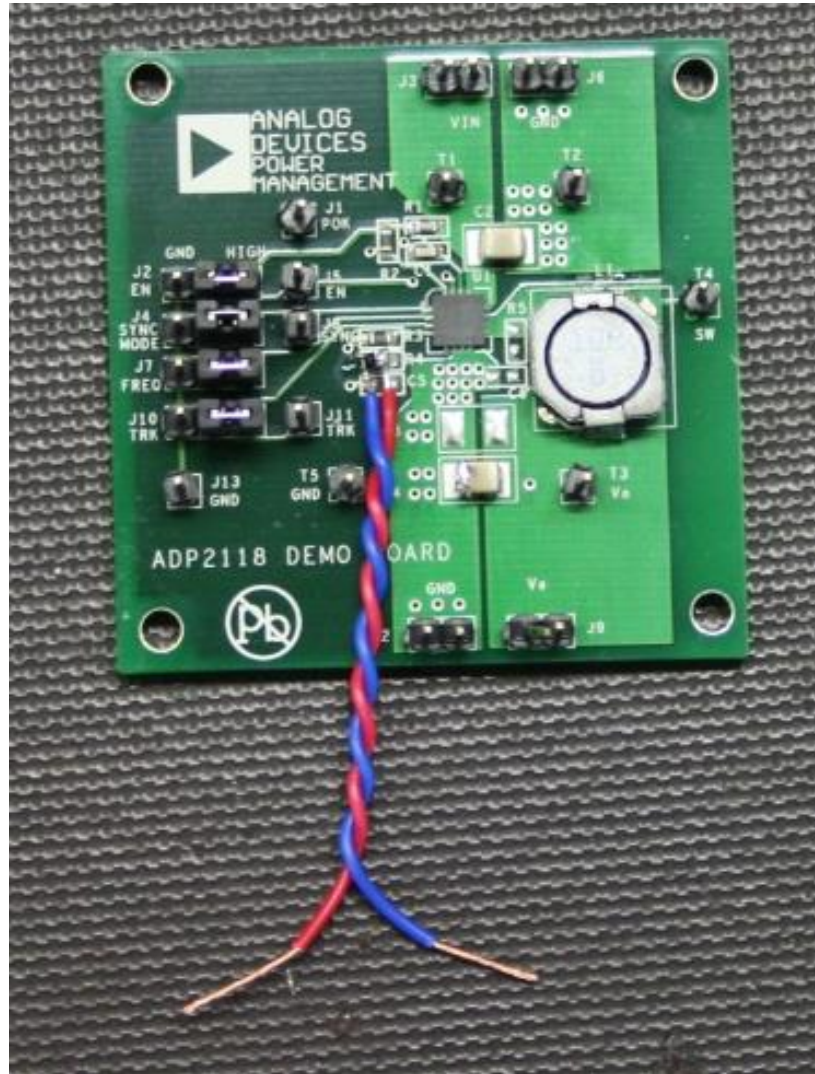


Simulating loop stability

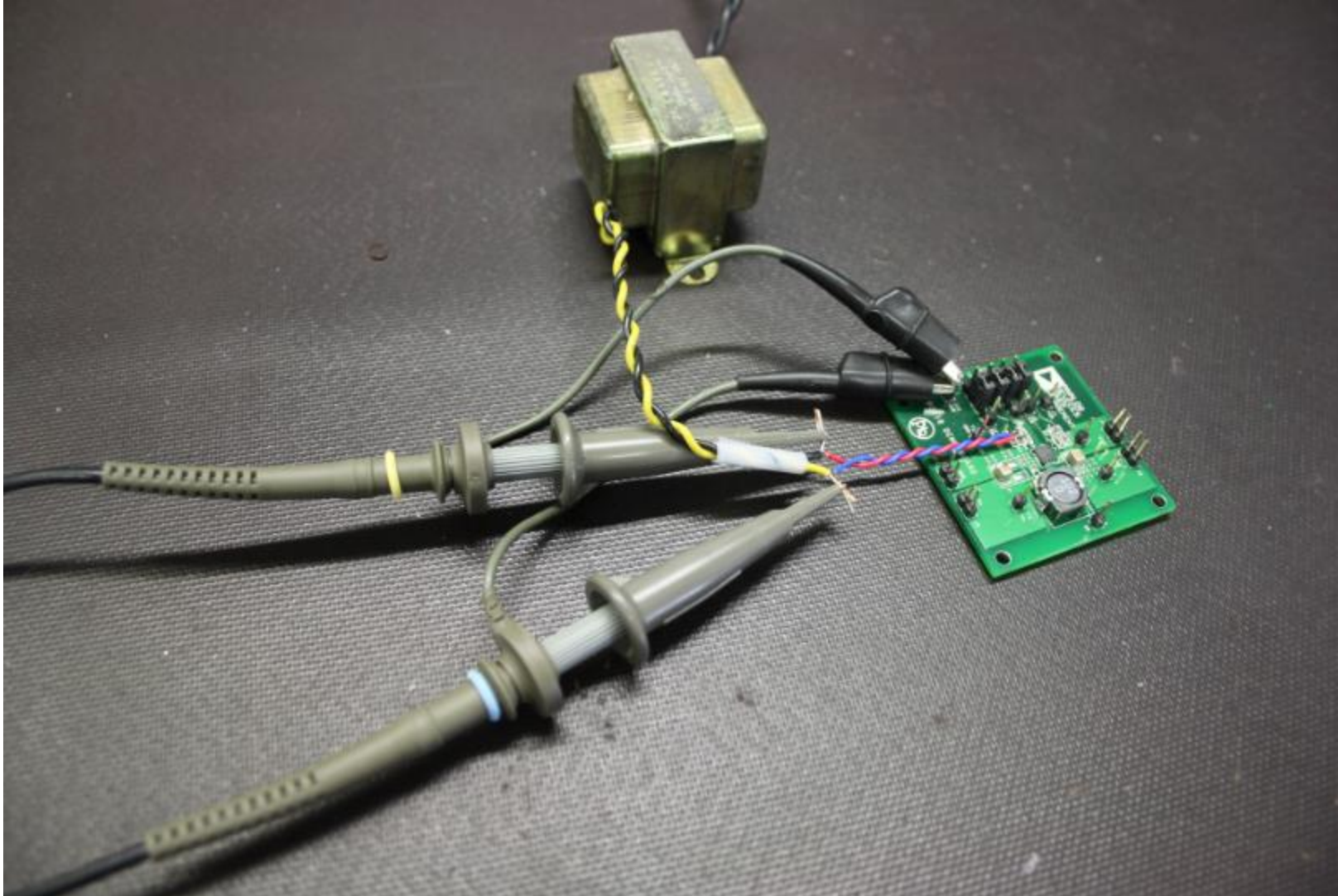
How to measure loop stability?



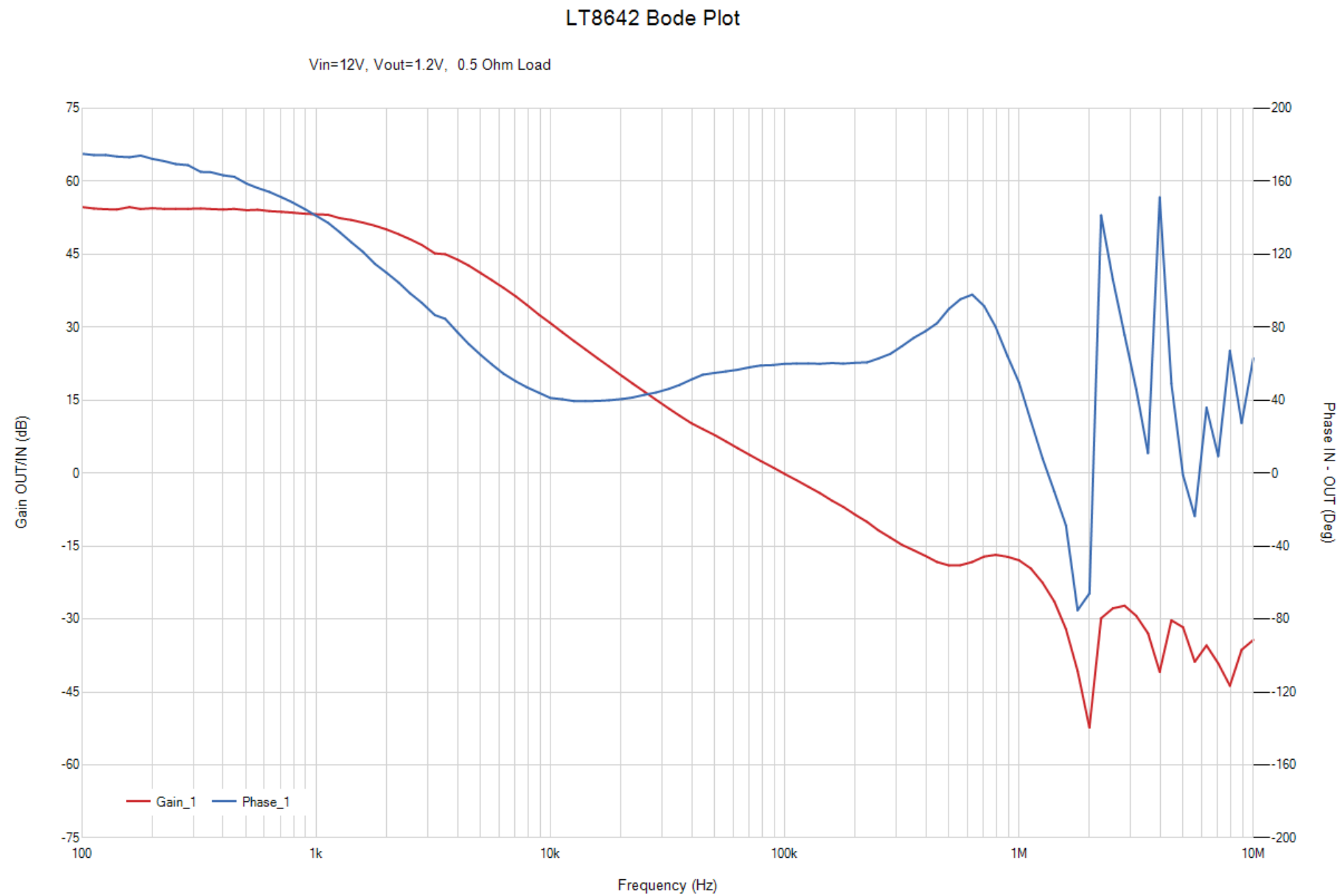
Practical Implementation



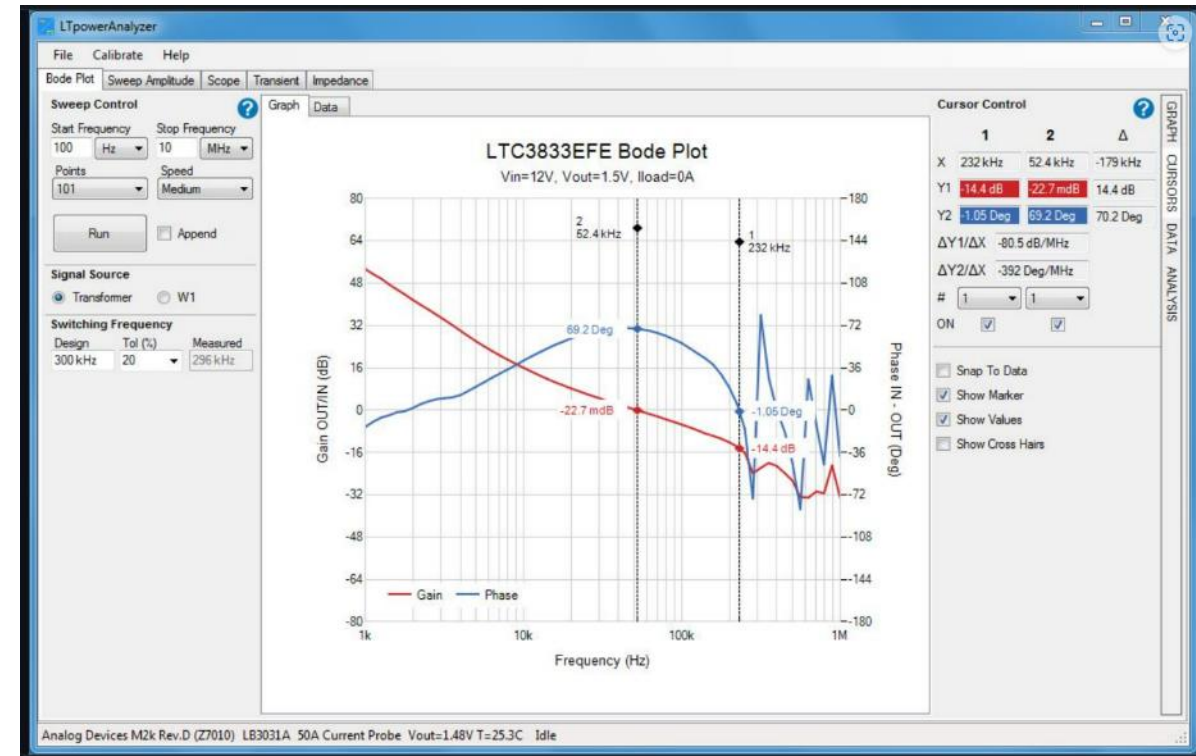
Practical Implementation



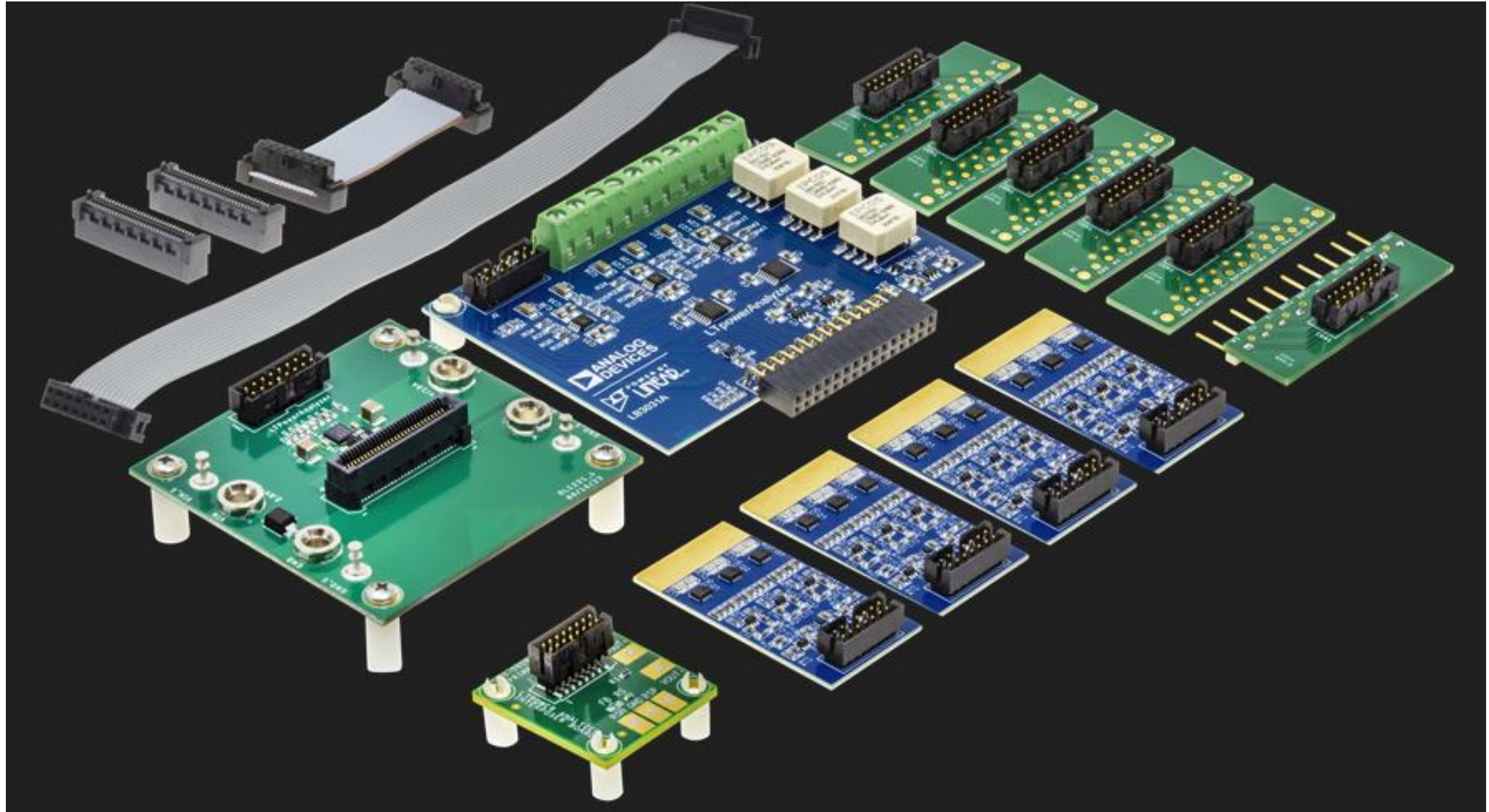
Bode Plot



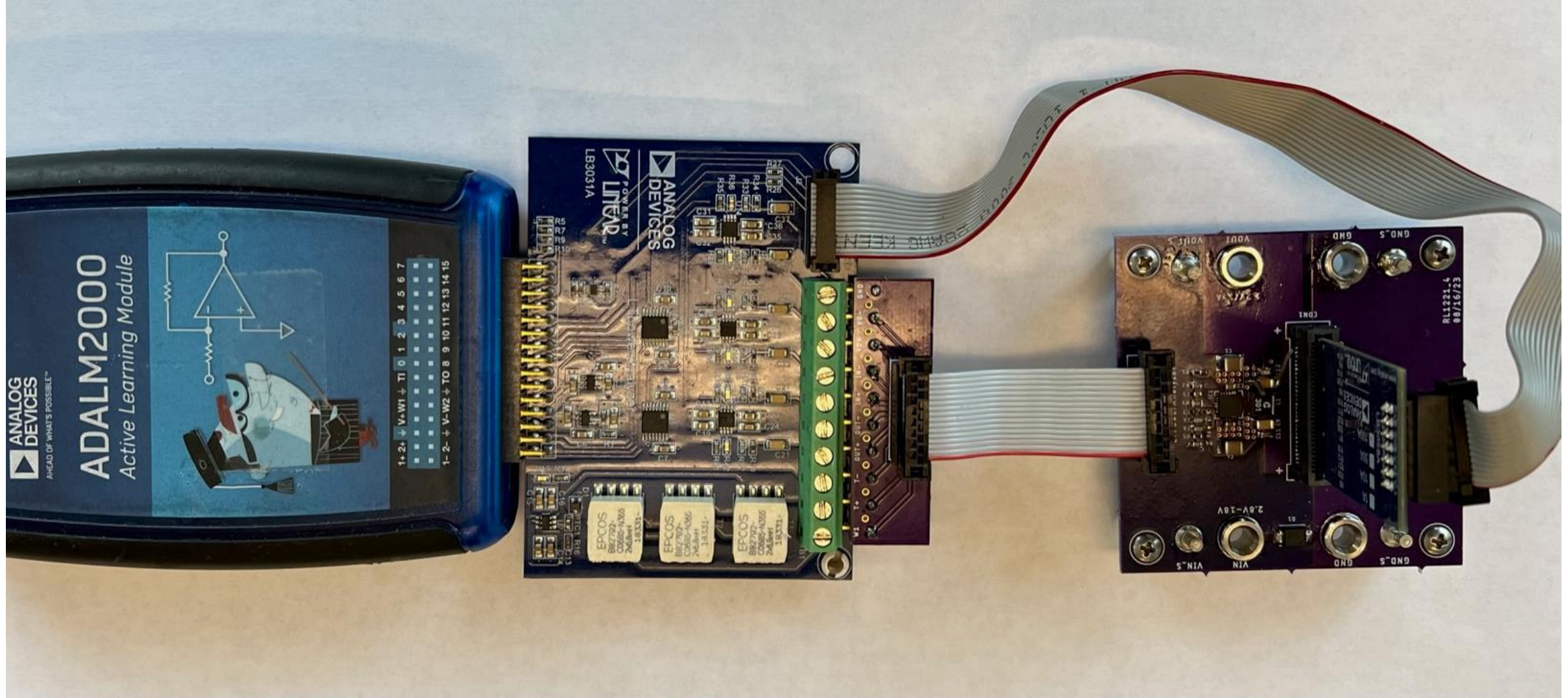
LTpowerAnalyzer: Bode Plots On the Go!



The LTpowerAnalyzer



The LTpowerAnalyzer



File Calibrate Help

Bode Plot Sweep Amplitude Scope Transient Impedance

Sweep Control

Start Frequency 100 Hz Stop Frequency 10 MHz
Points 101 Speed Medium

Run

☐ Append

Signal Source

☒ Transformer ☐ W1

Switching Frequency

Design 2 MHz Tol (%) 20 Measured 1.96 MHz

DC Probe Current

0 A Zero

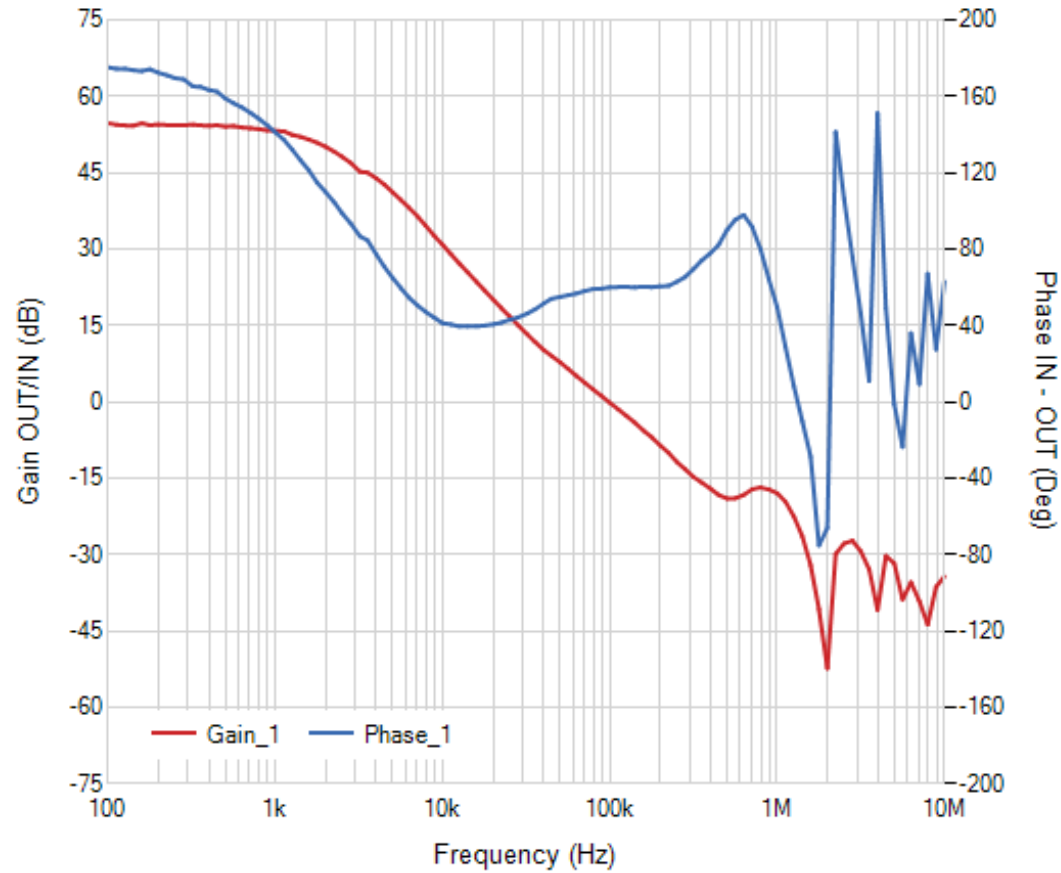
☐ Enabled

Graph

Data

LT8642 Bode Plot

Vin=12V, Vout=1.2V, 0.5 Ohm Load



Waveform Data Editor

#	Name	Visible	Select
1	Gain_1	☒	☐
1	Phase_1	☒	☐

GRAPH CURSORS DATA ANALYSIS

☒ Legend☐ Points

Hide All

Show All

Delete All

Delete

File Calibrate Help

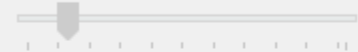
Bode Plot Sweep Amplitude Scope Transient Impedance

Configuration

☒ Bode ☐ Impedance

Signal Generator

Frequency 1 kHz Vout (pk-pk) 50 mV



☐ Enable

Signal Source

☒ Transformer ☐ W1

FFT

Average 64

Filter

Frequency 10MHz ☐ Enabled

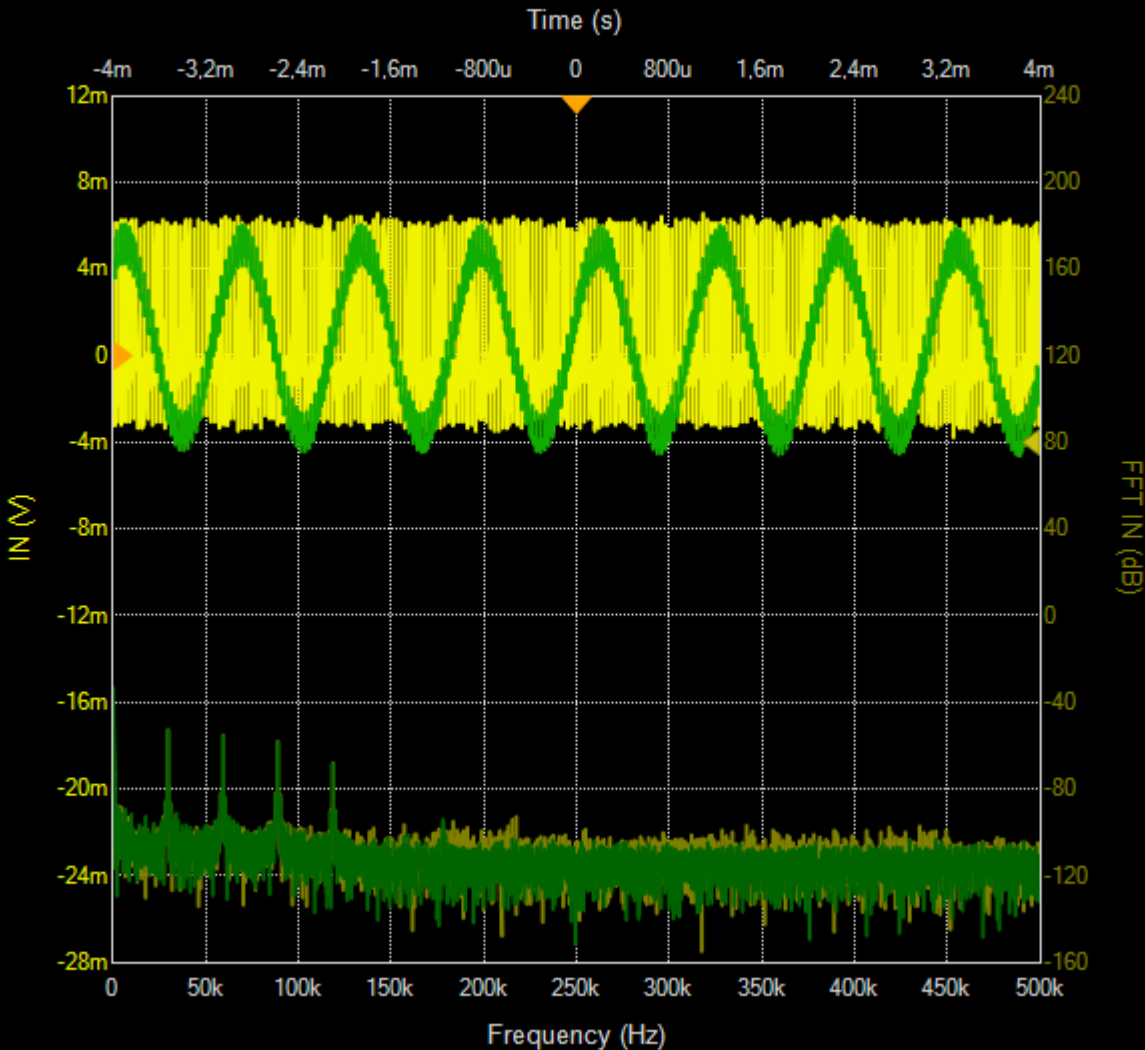
DC Probe Current

0 A Zero

☐ Enabled ☐ Fan

Run

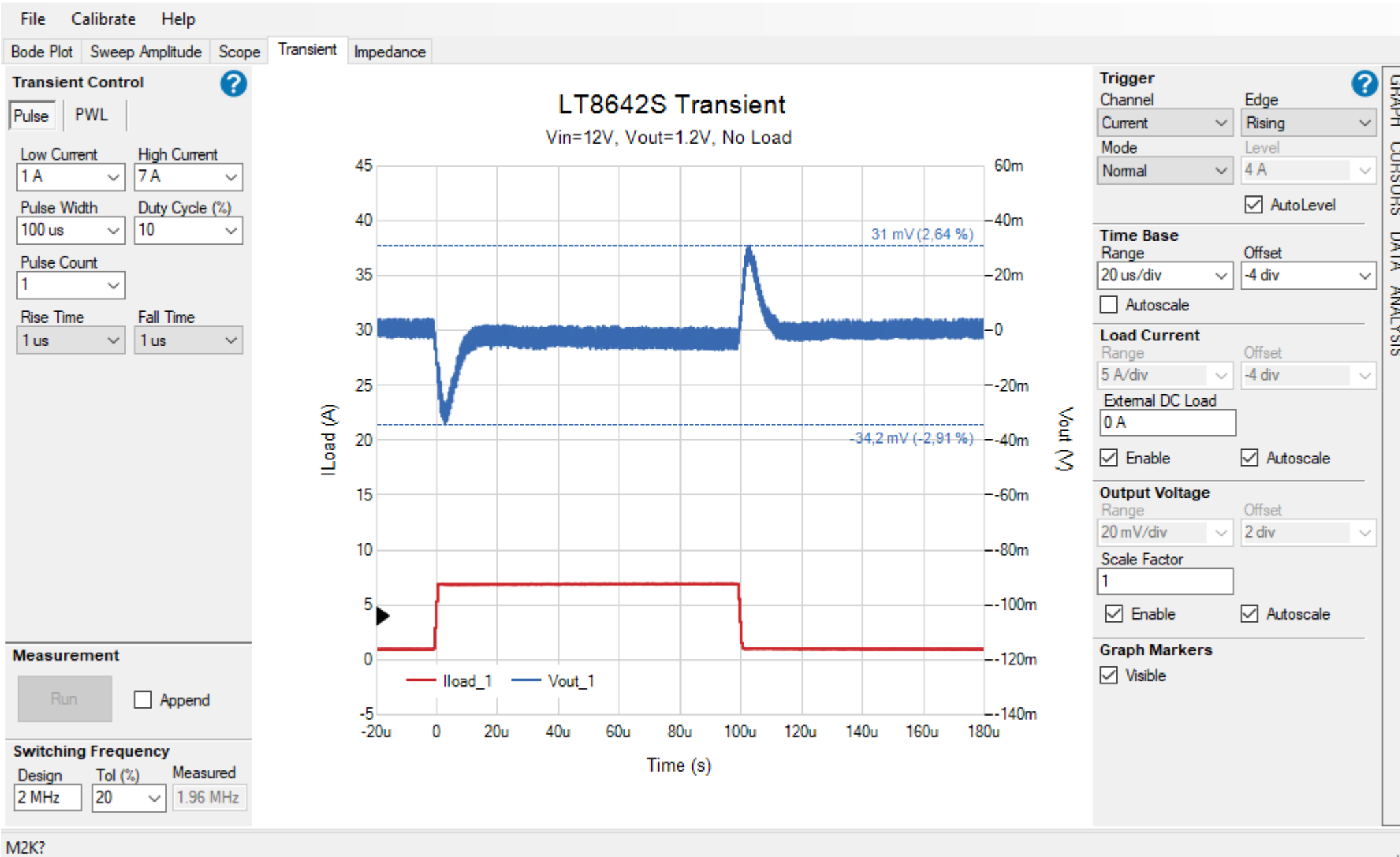
Single



Scope Analysis

Parameter	Value
Aquisition Time	16.38 ms
Sample Frequency	1 MHz
Signal Frequency	972.8 Hz
Cycle Count	15.94
Samples/Cycle	1028
Ripple IN (pk-pk)	11.06 mV
Ripple OUT (pk-pk)	54.03 mV
Signal FFT Bin	16
FFT Bin Size	61.04 Hz
FFT IN (pk-pk)	85.86 μ V
FFT OUT (pk-pk)	43.21 mV
Gain (OUT/IN)	51.53 dB
Phase (IN-OUT)	123.7 deg

GRAPH CURSORS ANALYSIS



File Calibrate Help

Bode Plot Sweep Amplitude Scope Transient Impedance

Sweep

Start Frequency Stop Frequency
100 Hz 10 MHzPoints Speed
101 Medium

Run

☐ Append

Switching Frequency

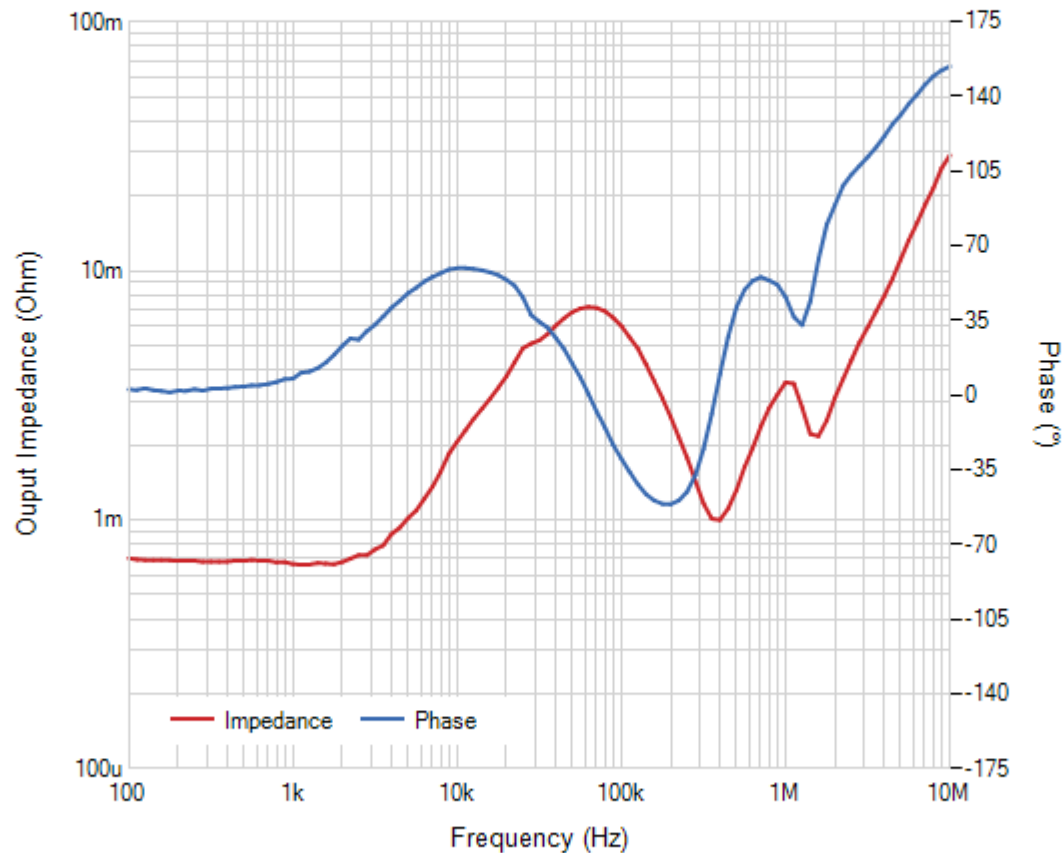
Design Tol (%) Measured
2 MHz 20 1.96 MHz

Graph

Data

LT8642S Ouput Impedance

Vin = 12V, Vout = 1.2V, 0.5 Ohm Load



X Axis

Minimum Maximum
100 Hz 10 MHz☒ AutoScale

Y1 Axis

Minimum Maximum
100 $\mu\Omega$ 100 m Ω ☒ AutoScale

Y2 Axis

Minimum Maximum Increments
-175 Deg 175 Deg 10☒ AutoScale

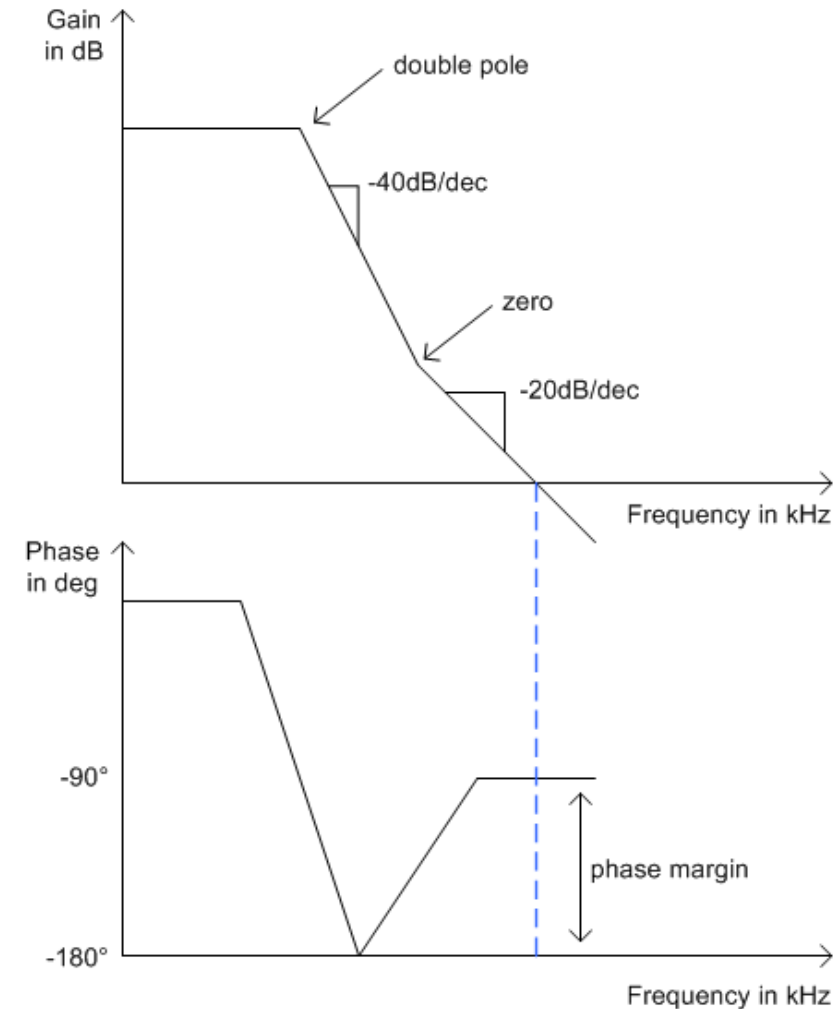
GRAPH CURSORS DATA ANALYSIS

The Bode Diagram

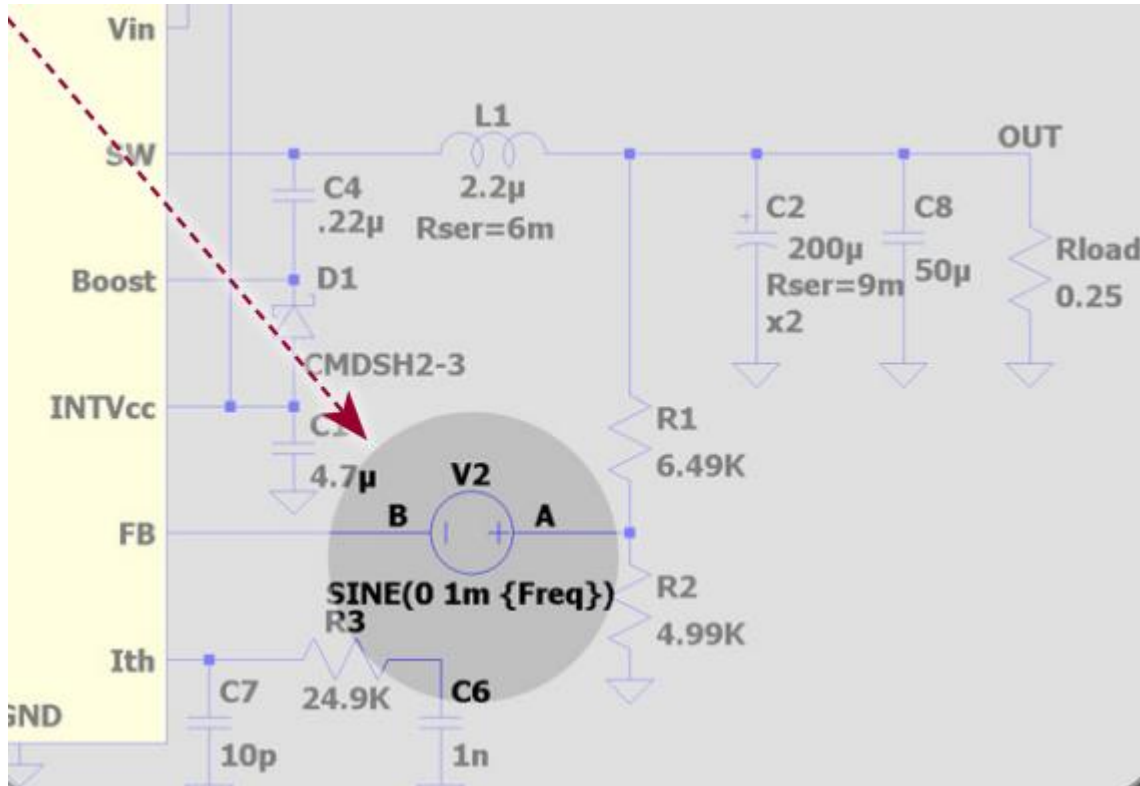
Phase margin is Phase at the frequency of 0dB crossover

0dB crossover goal 1/5th, 1/10th of switching frequency

Phase margin goal is > 45 deg



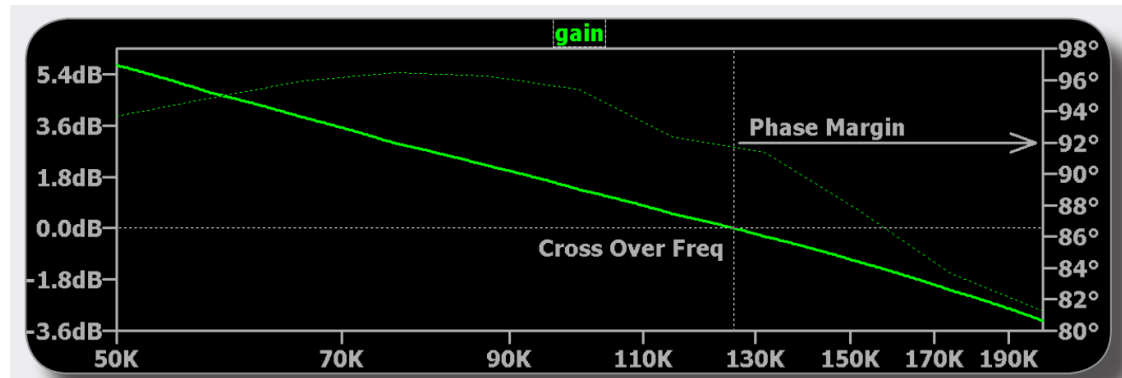
Bode Plot in old LTspice



```
.measure Aavg avg V(a)
.measure Bavg avg V(b)
.measure Are avg (V(a)-Aavg)*cos(360*time*Freq)
.measure Aim avg -(V(a)-Aavg)*sin(360*time*Freq)
.measure Bre avg (V(b)-Bavg)*cos(360*time*Freq)
.measure Bim avg -(V(b)-Bavg)*sin(360*time*Freq)
.measure GainMag param 20*log10(hypot(Are,Aim) / hypot(Bre,Bim))
.measure GainPhi param mod(atan2(Aim, Are) - atan2(Bim, Bre)+180,360)-180
```

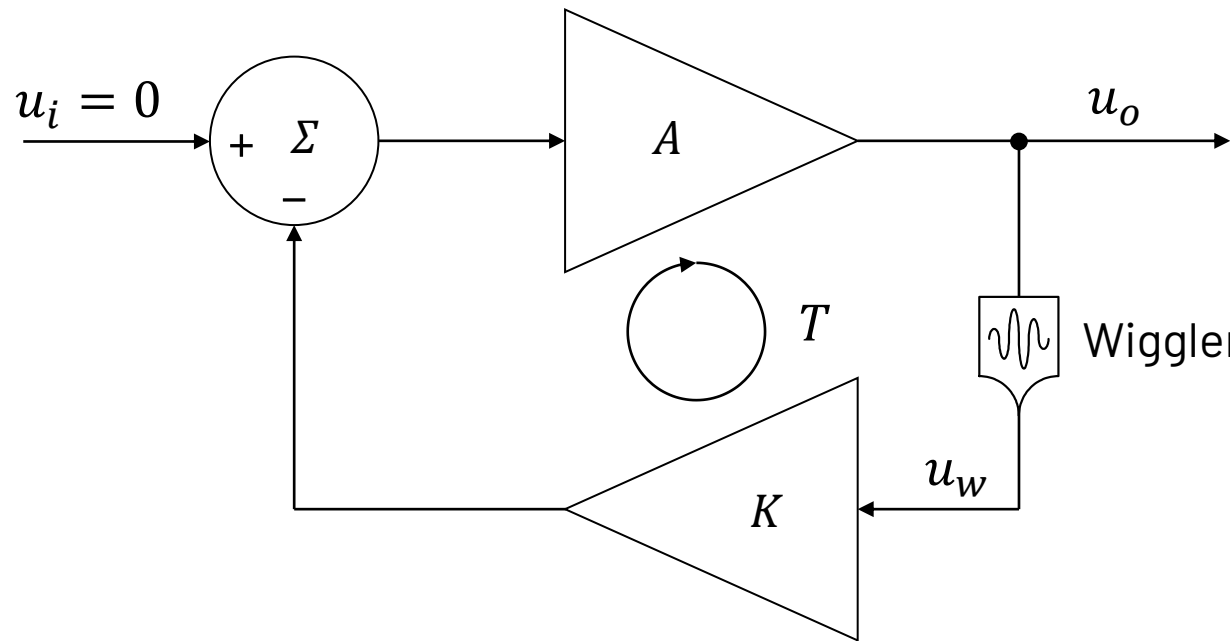
```
.param t0=.2m
.tran 0 {t0+25/freq} {t0}
```

```
.step oct param freq 5K 500K 5
.save V(a) V(b)
.option plotwinsize=0 numdgt=15
```

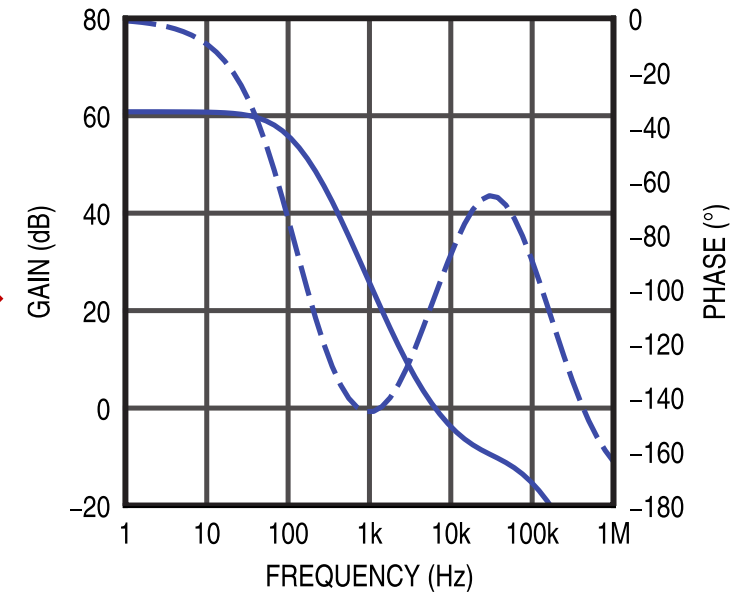


Stability Analysis, Small Signal

Power Supply: Input = Output = 0



$$u_o = -T u_w$$

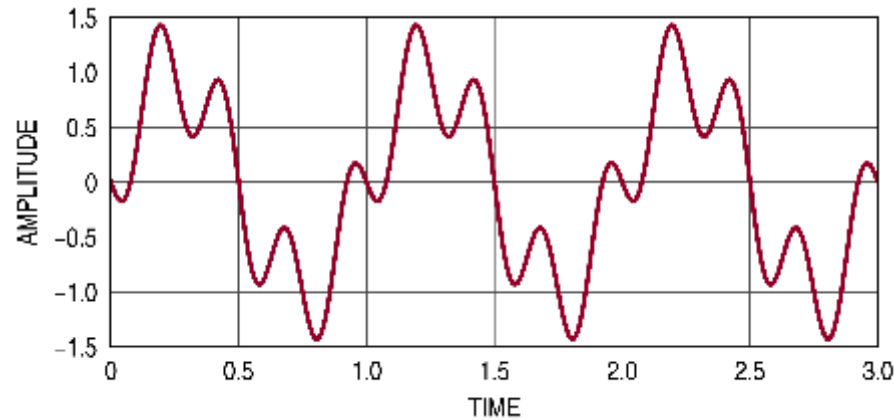


Principle of Superposition

Superposition
of Harmonics
(Stimulus)

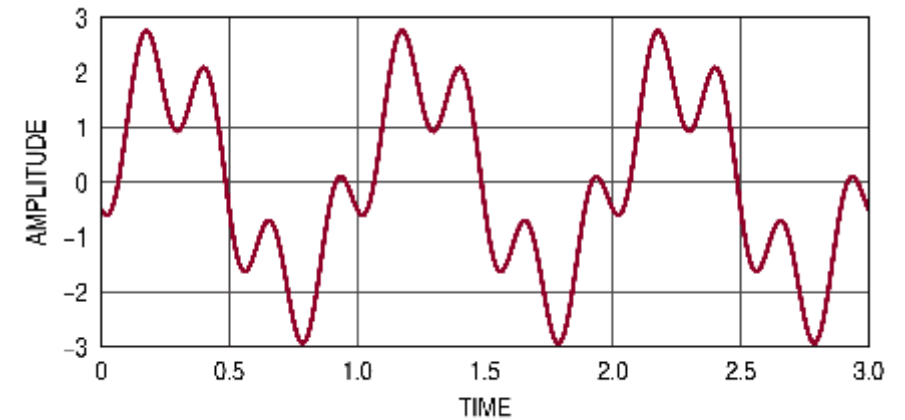
Linear
Time-Invariant
System

Superposition
of Harmonics
(Extraction)

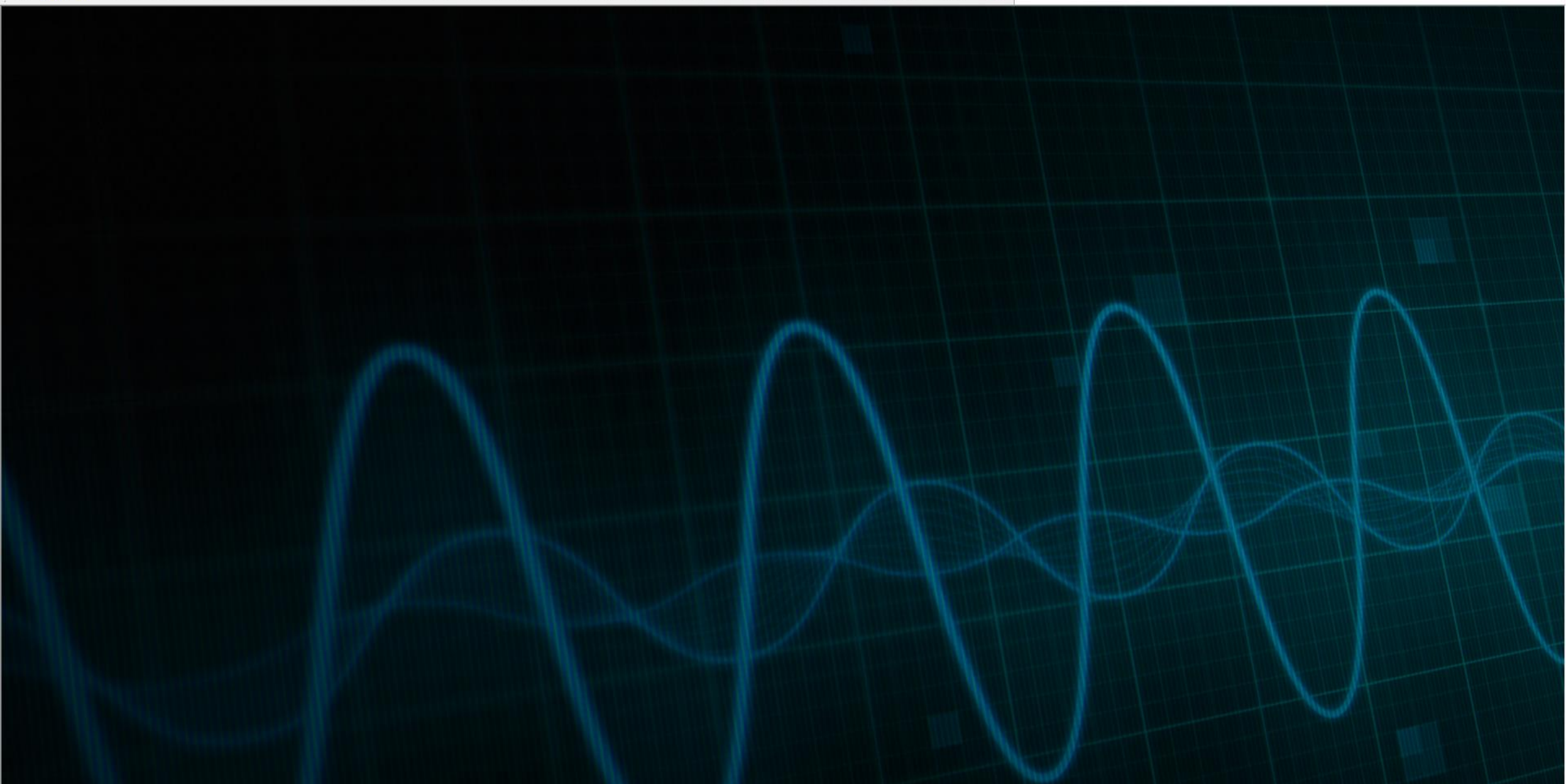


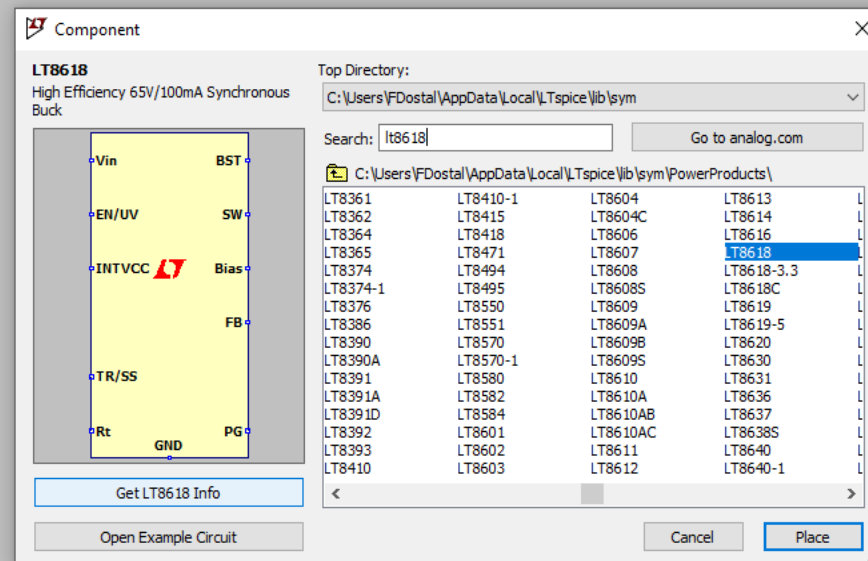
$$s(t) = \sin(2\pi t) + \frac{1}{2}\sin(8\pi t + \pi)$$

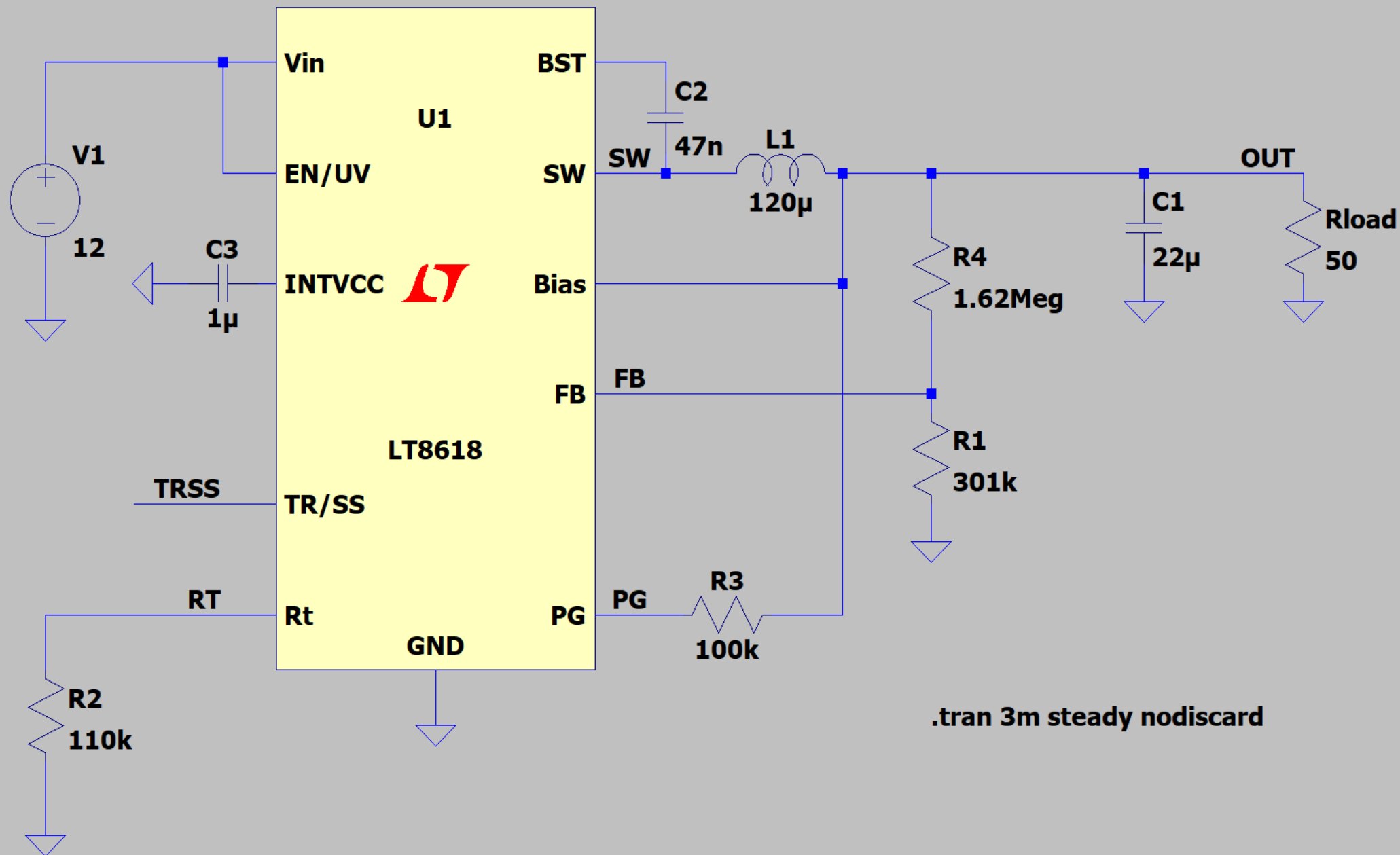
Harmonics nf With $n = 2^k$ ($k \in \mathbb{N}$)

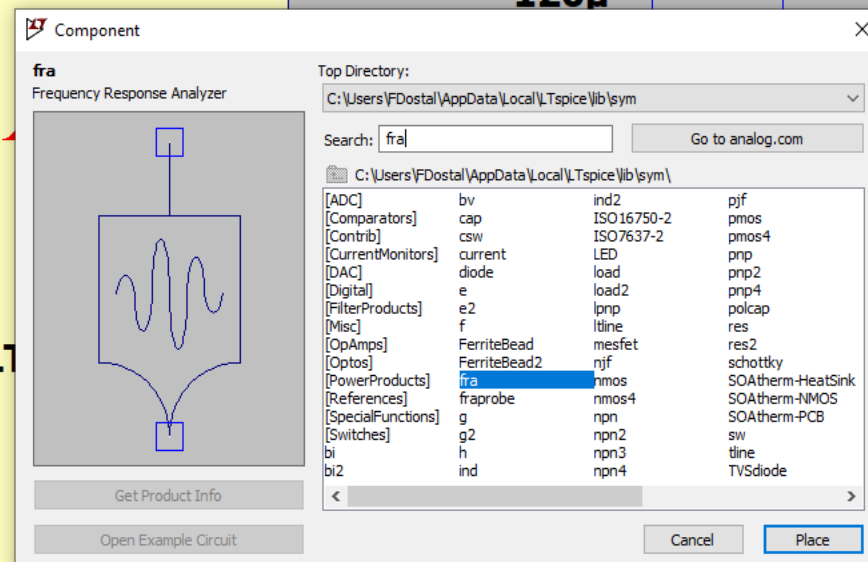
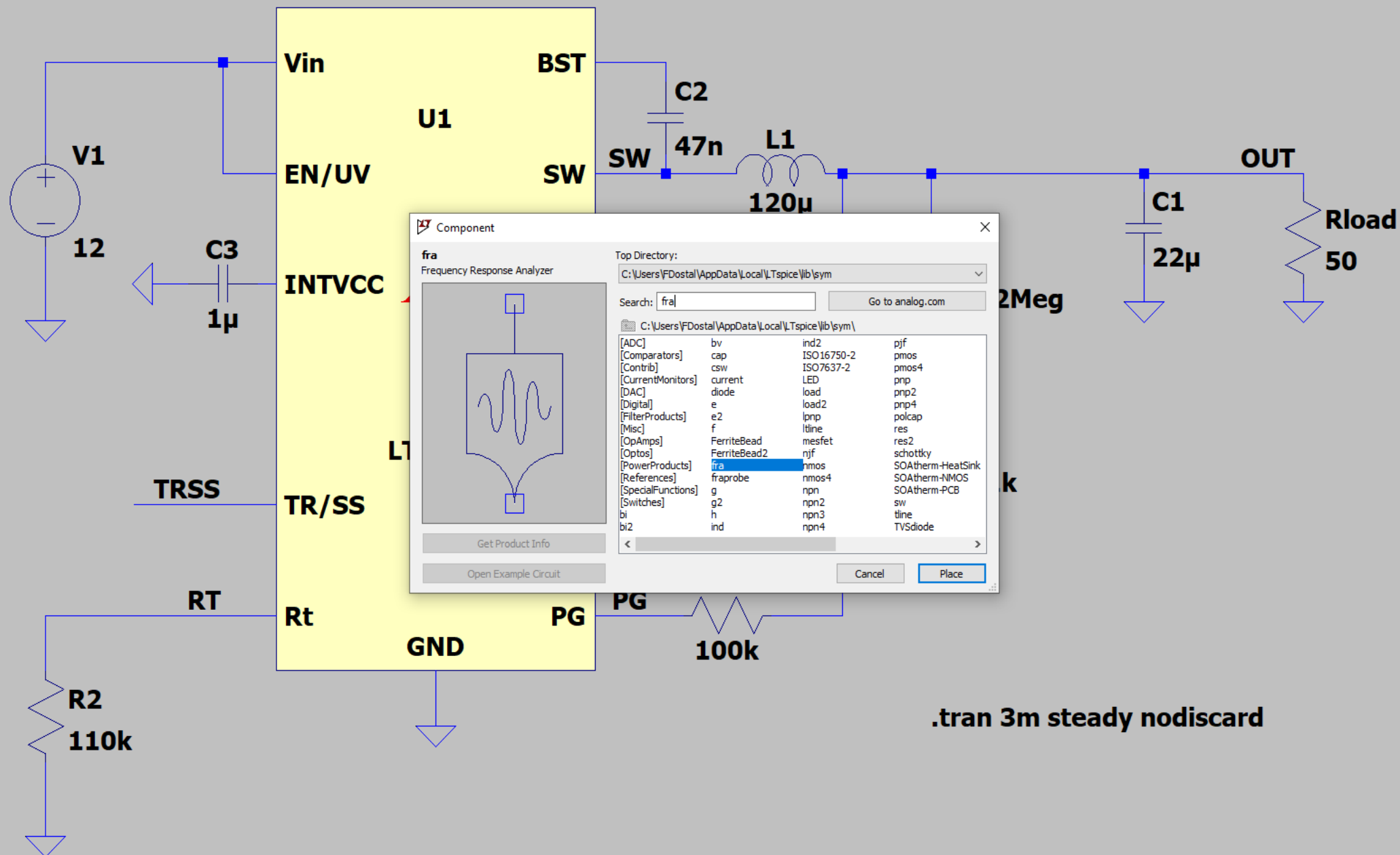


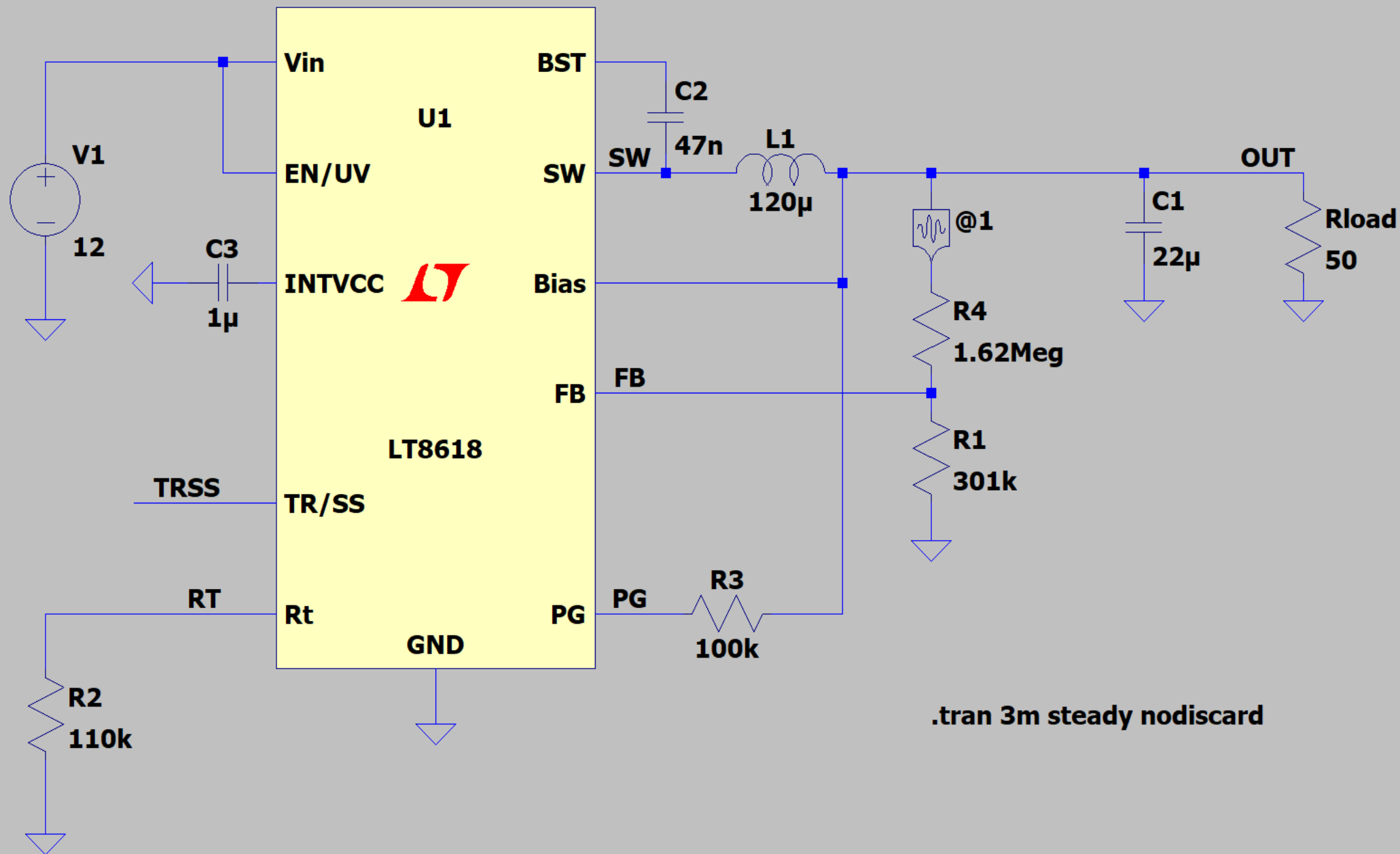
Nonlinear Circuit: Keep Stimulus Sufficiently Small.

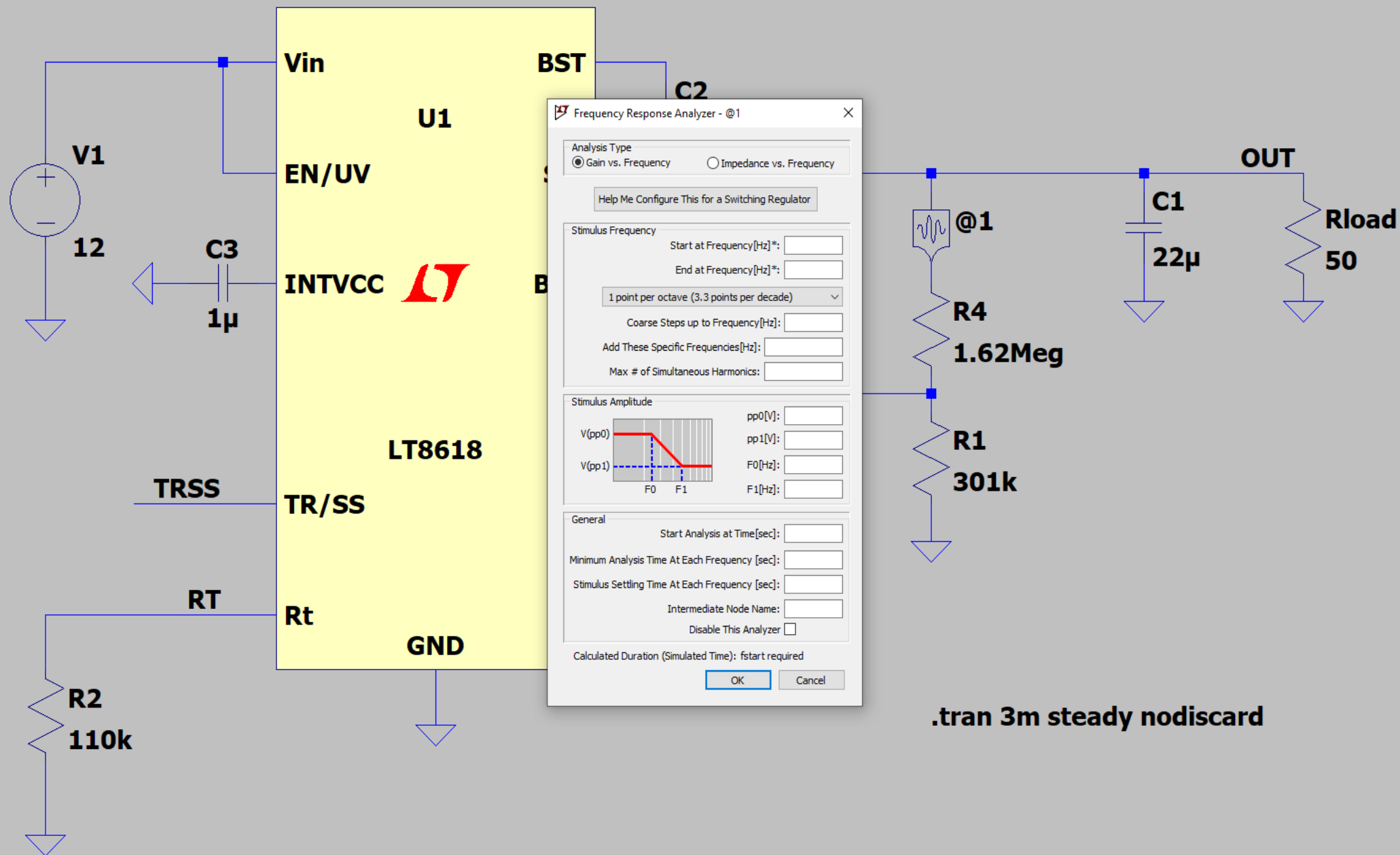












Settings

Frequency Response Analyzer - @1

Analysis Type
☒ Gain vs. Frequency ☐ Impedance vs. Frequency

Help Me Configure This for a Switching Regulator

Stimulus Frequency

Start at Frequency[Hz]*: 10

End at Frequency[Hz]*: 1000k

2 points per octave (6.6 points per decade) ▼

Coarse Steps up to Frequency[Hz]: 10k

Add These Specific Frequencies[Hz]:

Max # of Simultaneous Harmonics: 10

Stimulus Amplitude

V(pp0) 40m

V(pp1) 20m

F0[Hz] 1k

F1[Hz] 2k

General

Start Analysis at Time[sec]: 1.2m

Minimum Analysis Time At Each Frequency [sec]: 250u

Stimulus Settling Time At Each Frequency [sec]: 125u

Intermediate Node Name:

Disable This Analyzer ☐

Calculated Duration (Simulated Time): 102.536m sec

OK Cancel

Configure Gain FRA for a Switching Regulator

Optionally, enter approximate expected values below, and LTspice will initialize the detailed analyzer parameters. All fields are optional.

Approximate Switching Frequency[Hz]:

Approximate Closed-Loop Bandwidth[Hz]:

Approximate common mode voltage at FRA device [V]:

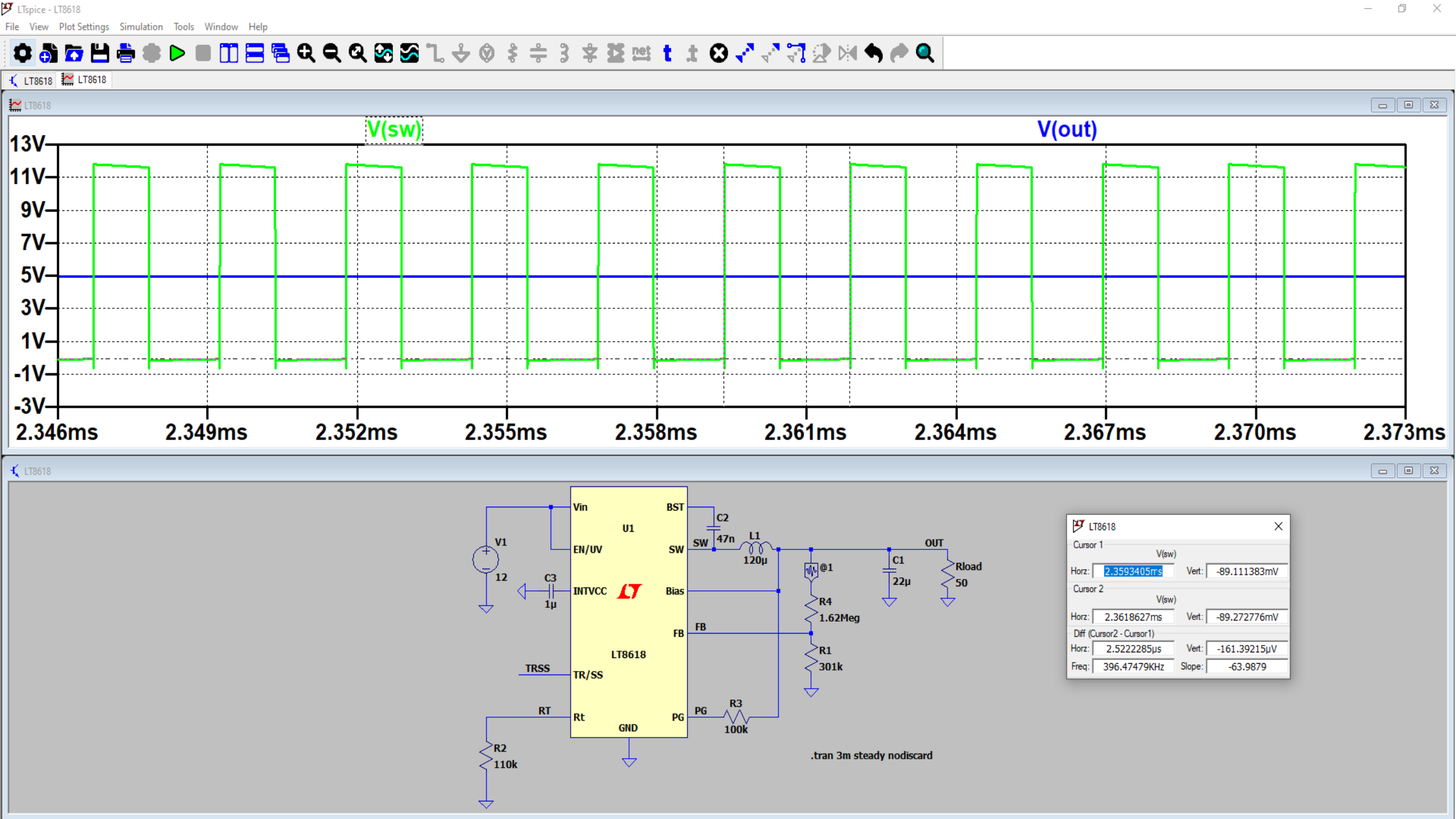
Configure FRA Cancel

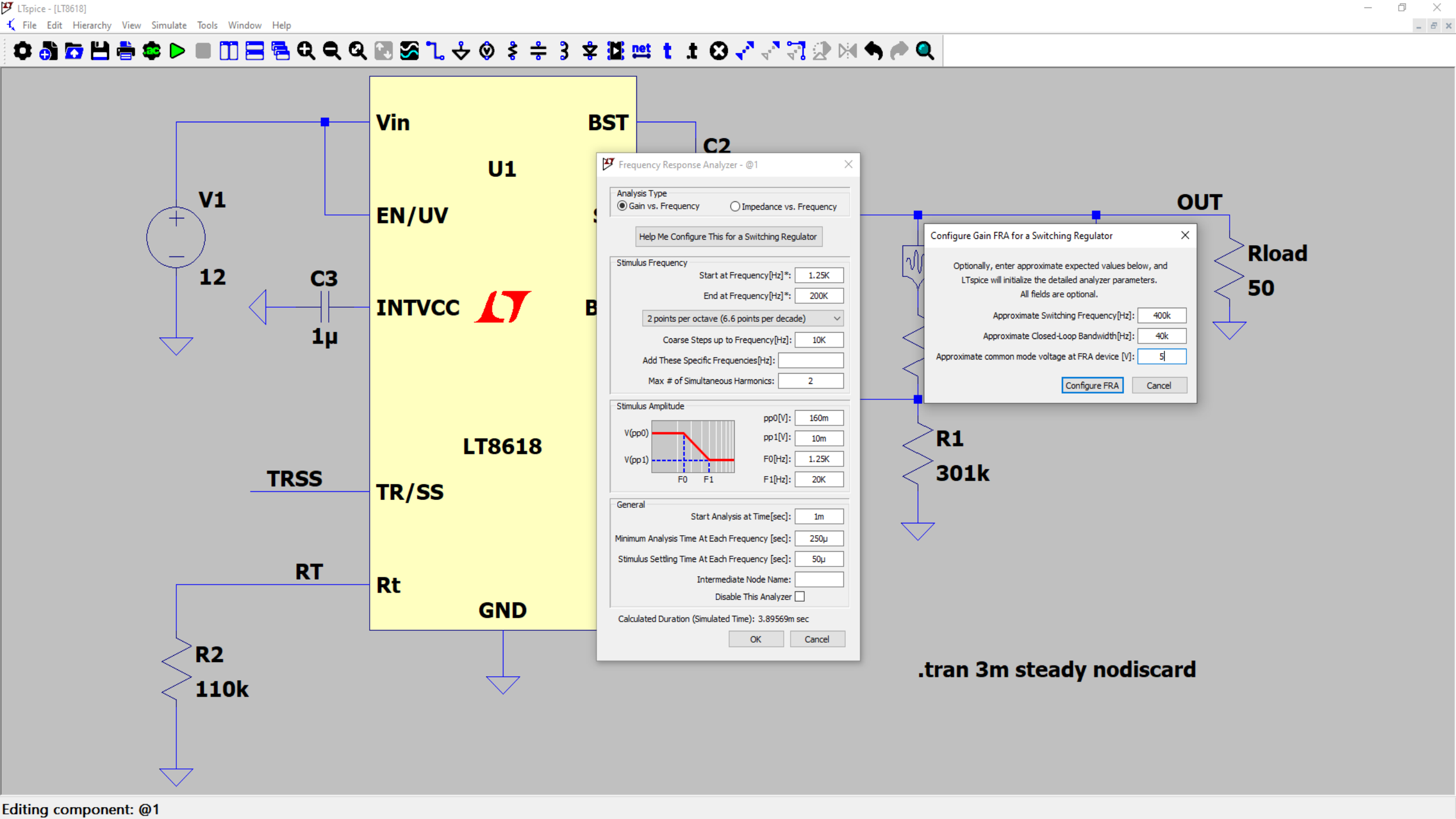
1 Point/Oct Below This Freq

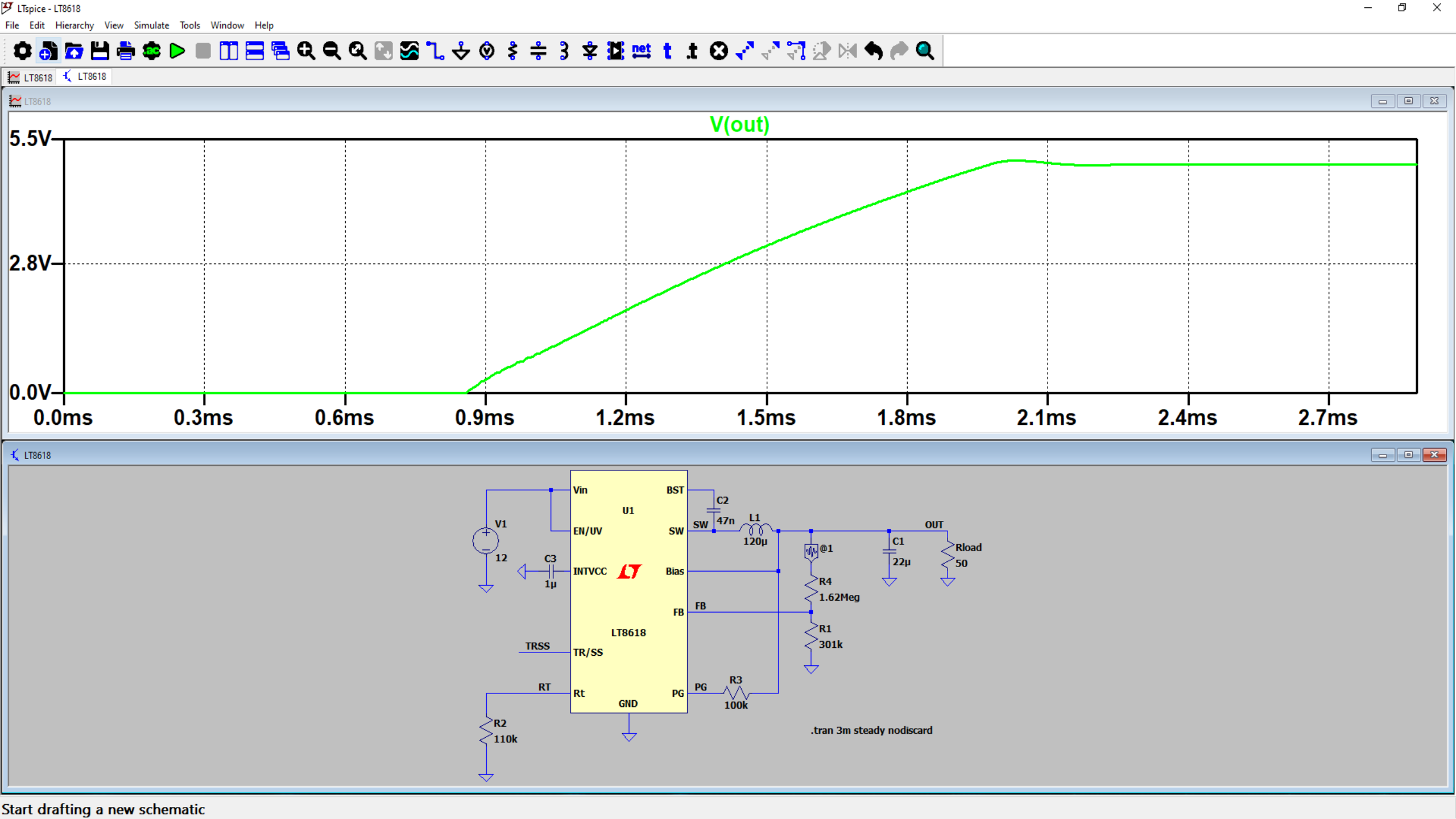
Multiple Freqs at Once

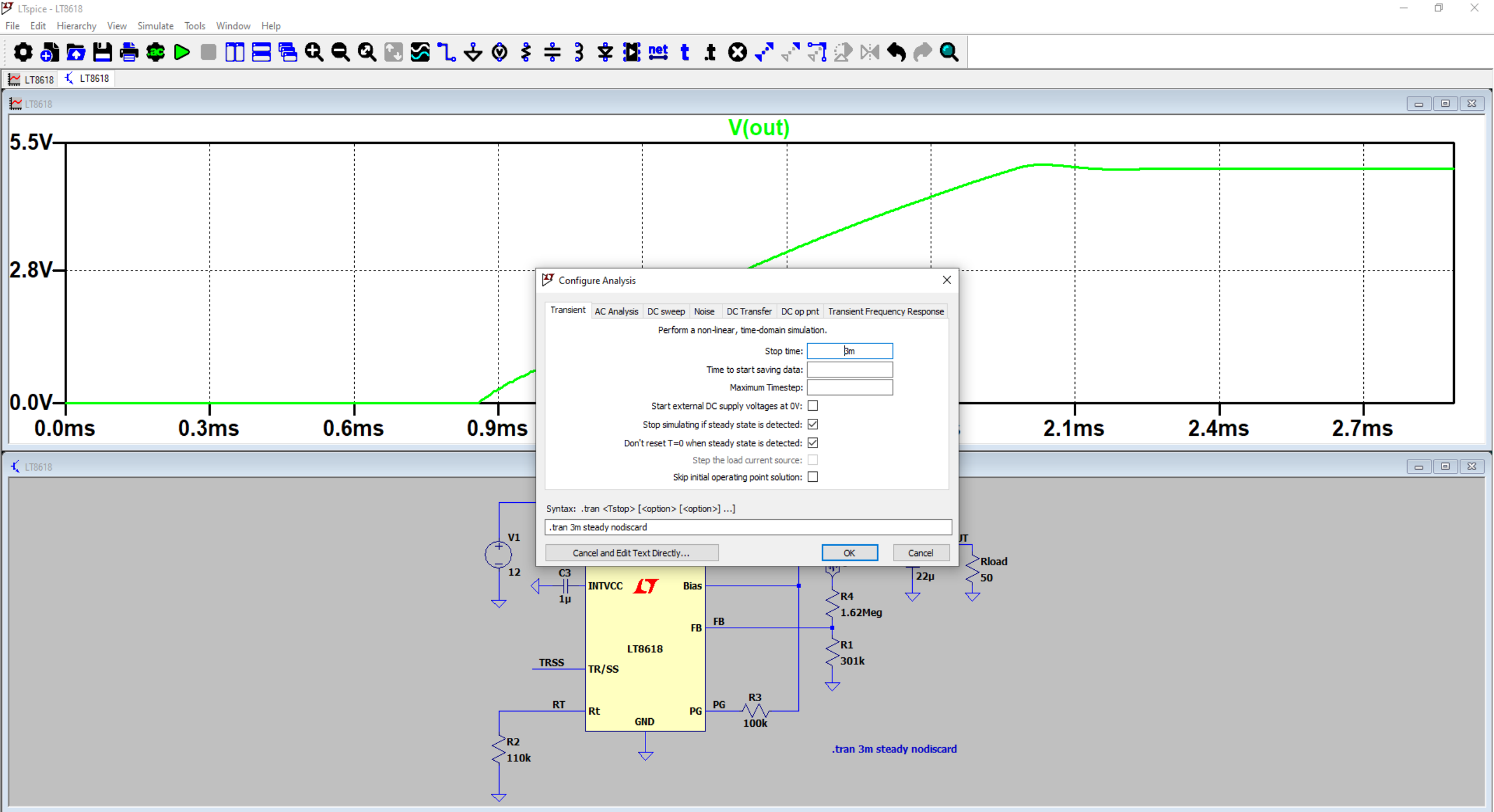
Averaging
Settling

Required Simulated Time

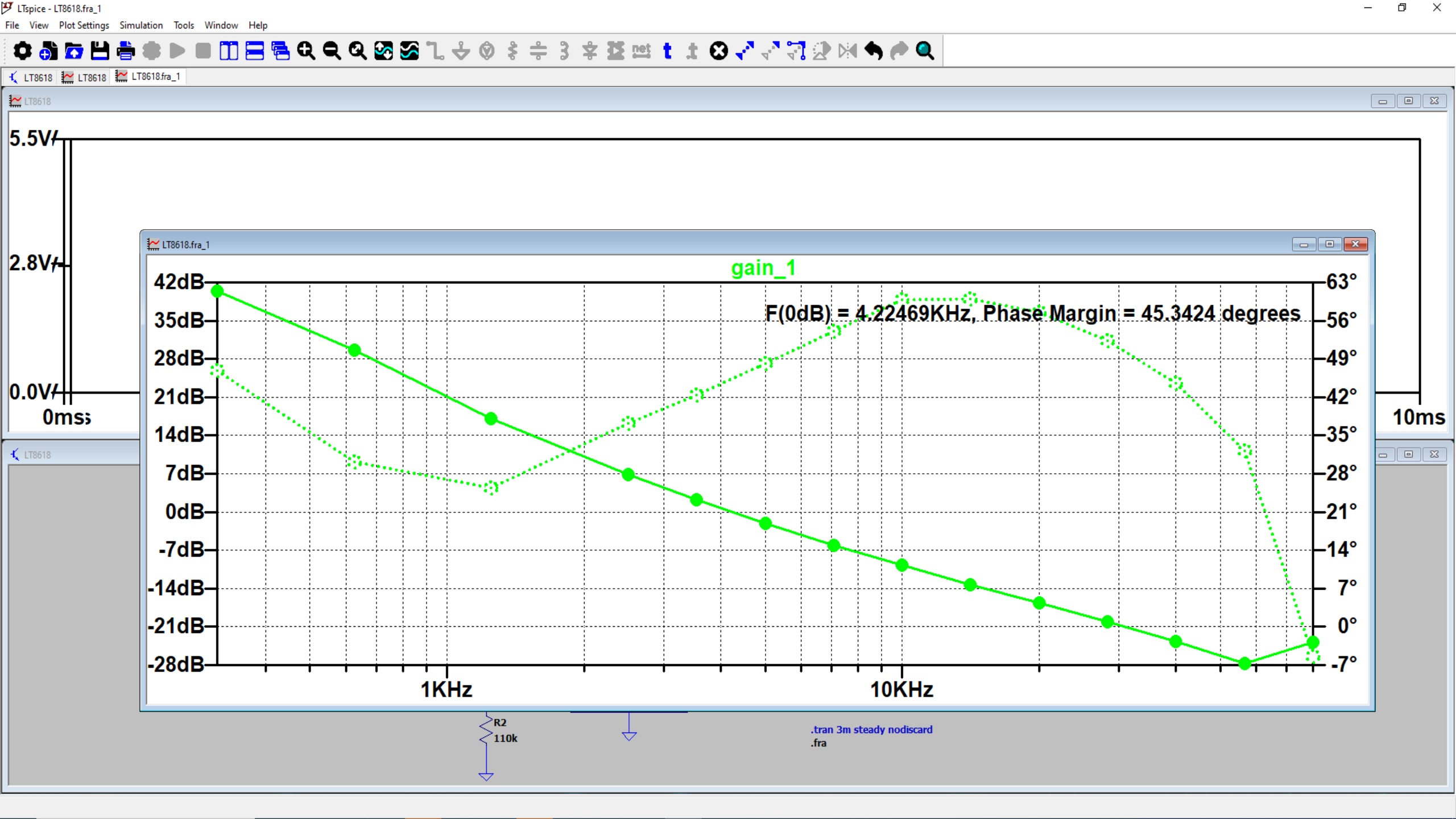






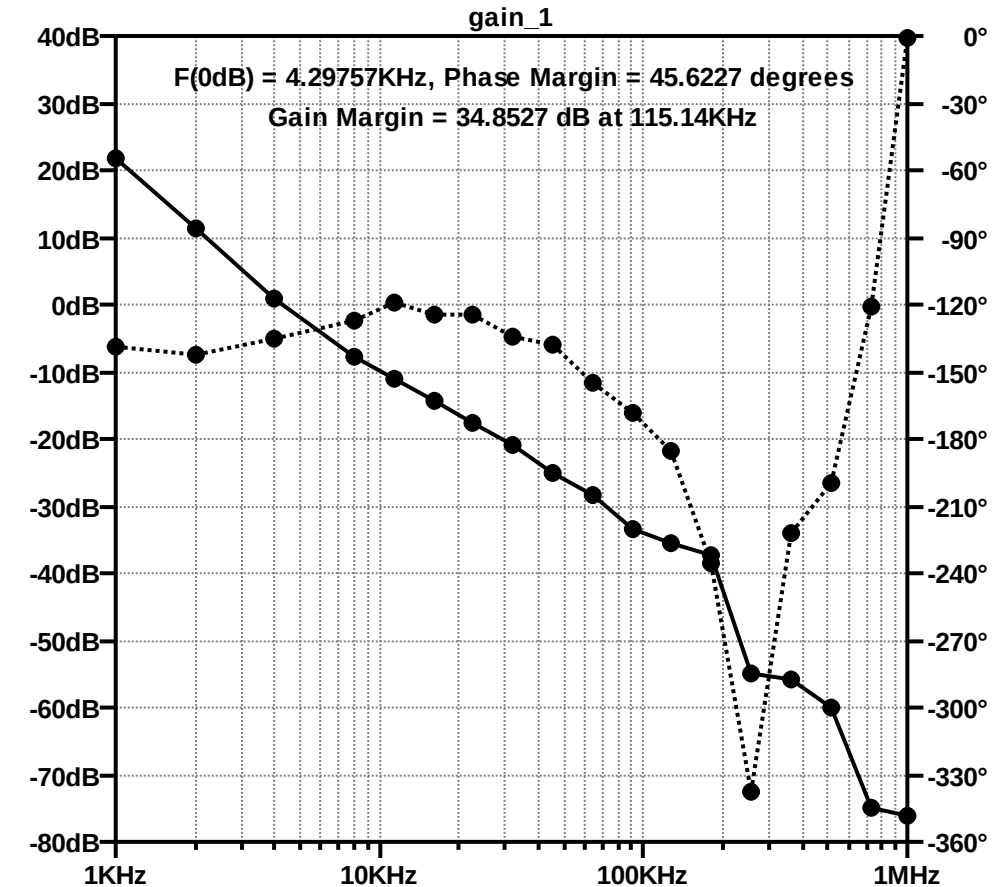
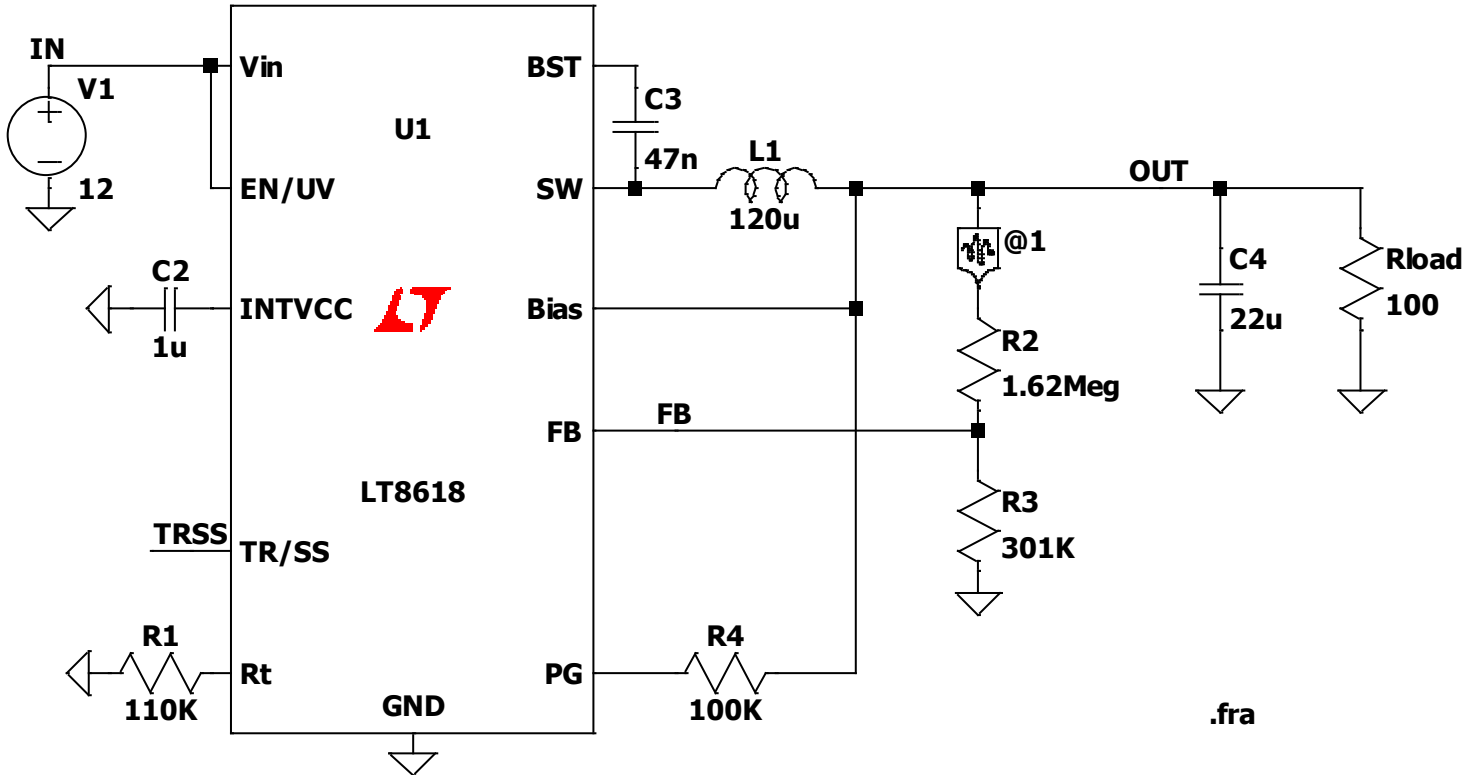


Right click to edit ".tran 3m steady nodiscard"



LT8618 (Buck)

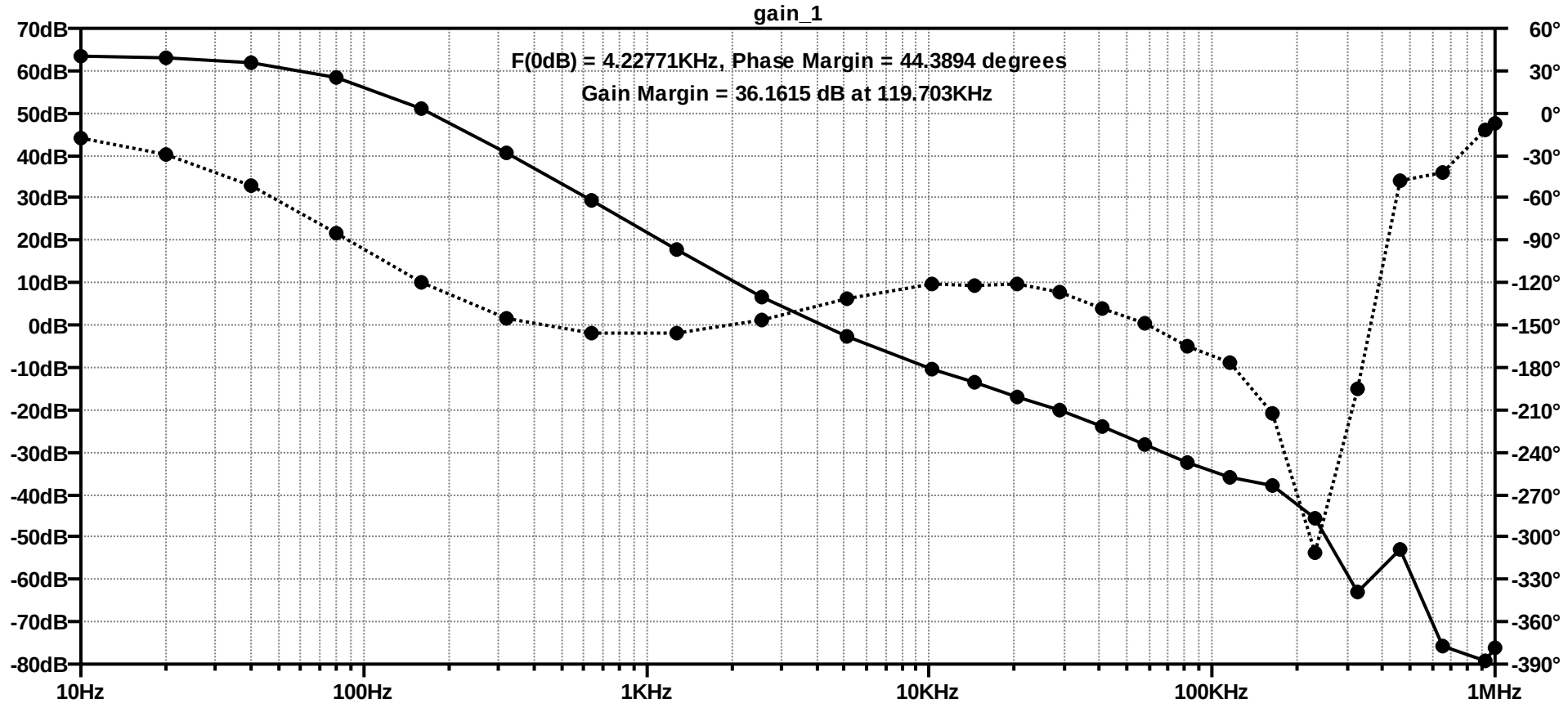
100mA Synchronous Buck, $f_{SW} = 400\text{kHz}$, $V_{OUT} = 5\text{V}$



Run Time 14.7s (On 5 Years Old Intel Core i9 7920X)

LT8618 (Buck)

100mA Synchronous Buck, $f_{SW} = 400\text{kHz}$, $V_{OUT} = 5\text{V}$

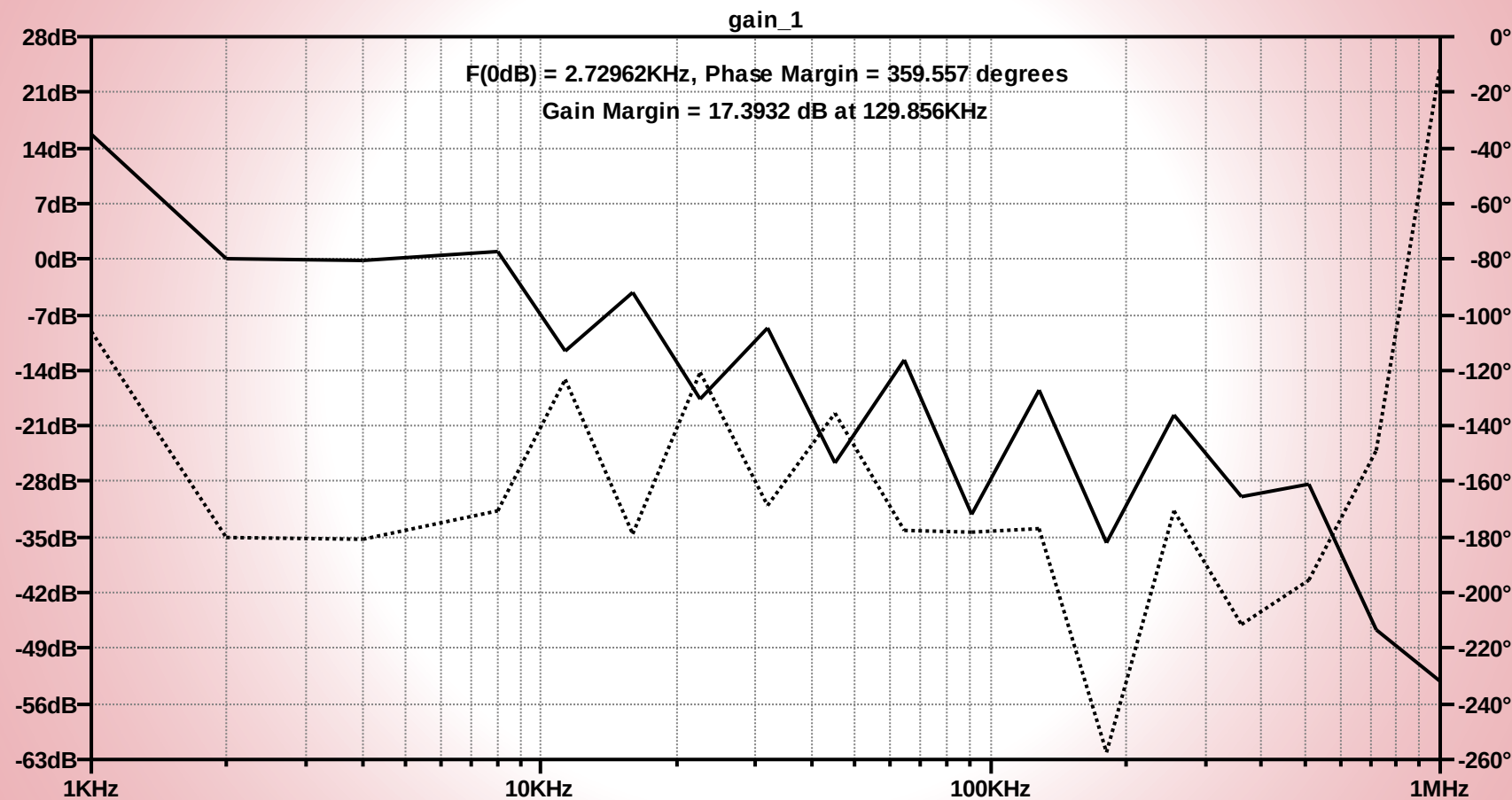


Run Time 9min 12s

LT8618 (Buck)



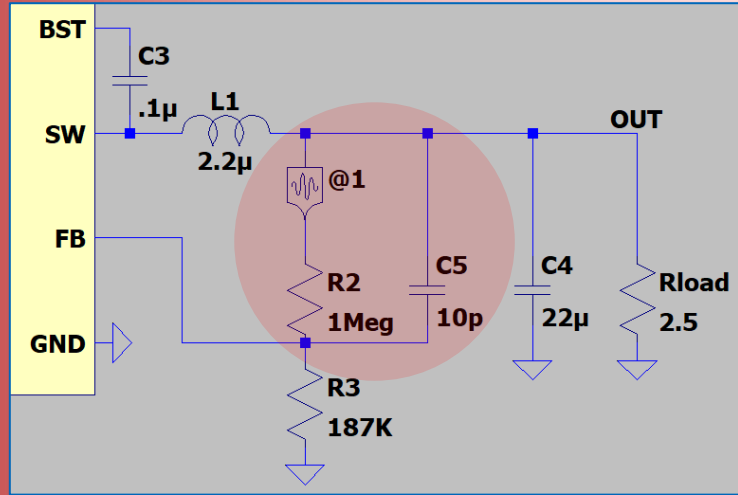
Stimulus Too Small



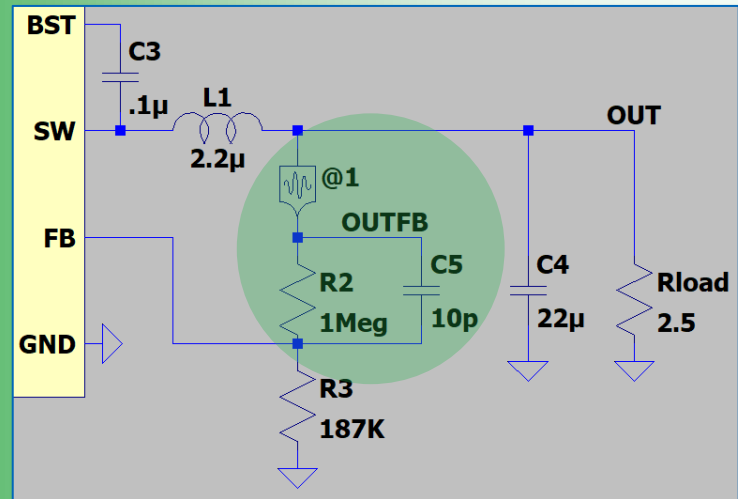
FAIL

Break the Loop

Incorrect



Correct



Criteria

- Interrupt **all** feedback paths
- FRA component must be point from **lower impedance (flat side)** to **higher impedance (pointy side)**

This requires engineering

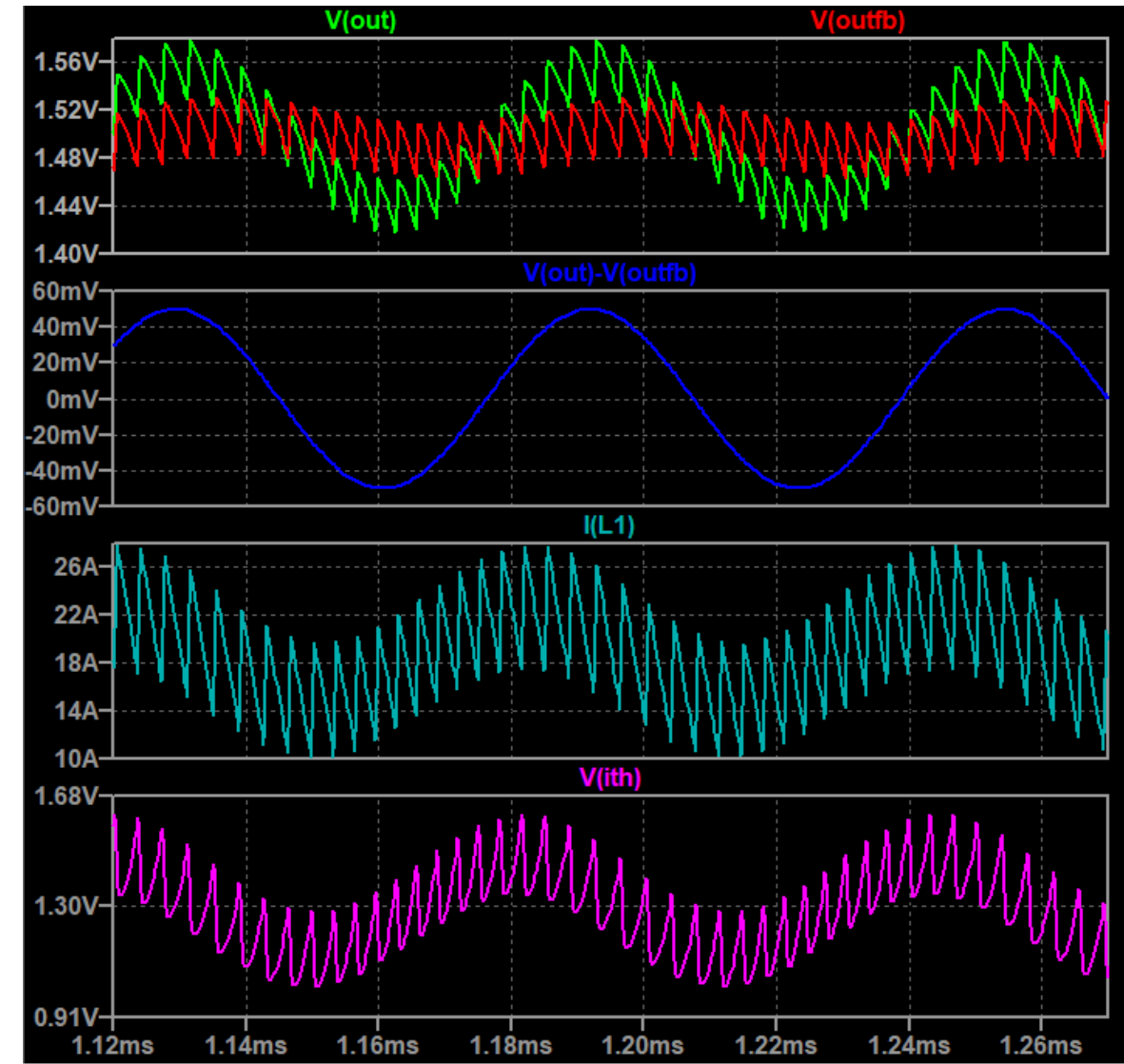
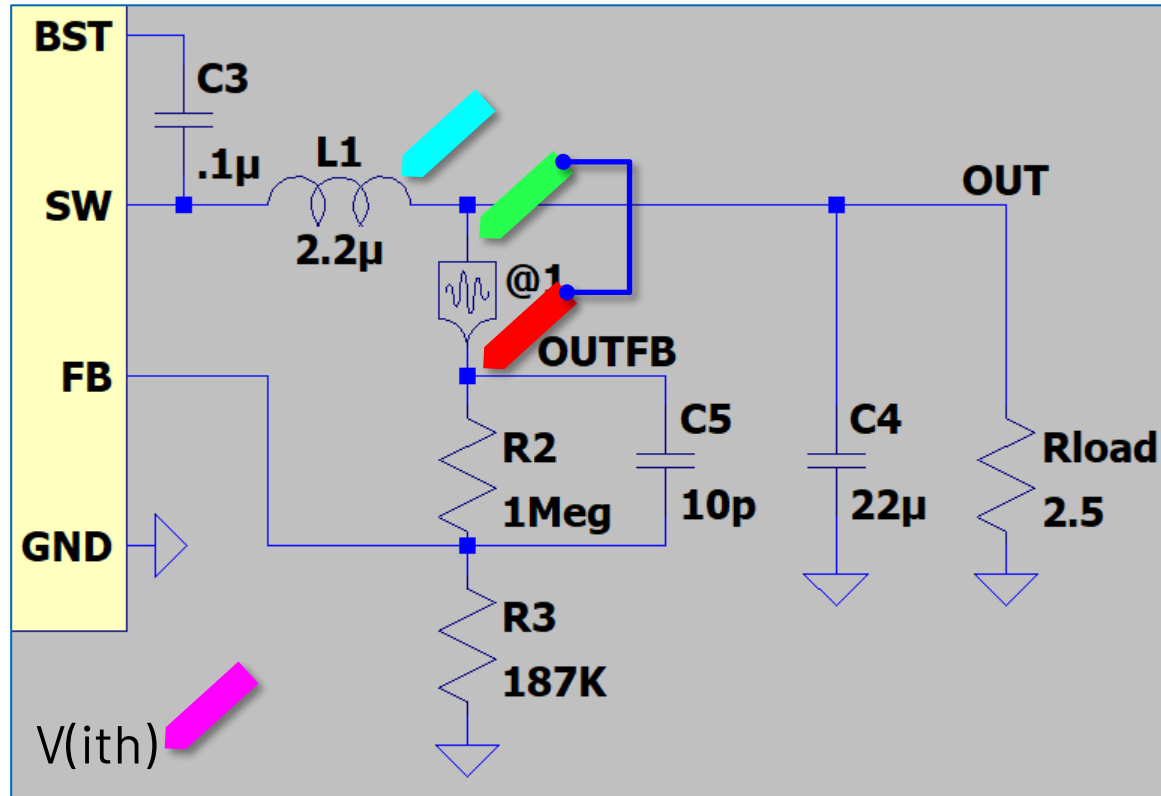
- LTspice does not know the correct placement
- Many circuits have multiple places where the loop can be broken—if in doubt, try two places and compare the results (adjust the stimulus amplitude appropriately)

Inspect the FRA transient waveforms

Voltage at both FRA terminals, and the difference

Inductor current

Control voltage (if external)

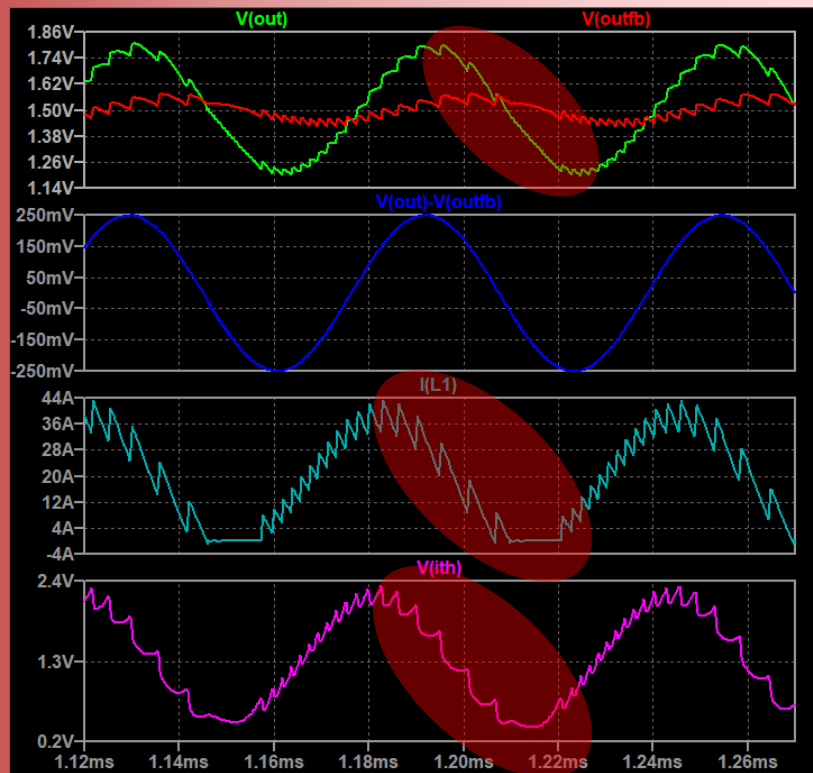


Inspect the FRA transient waveforms

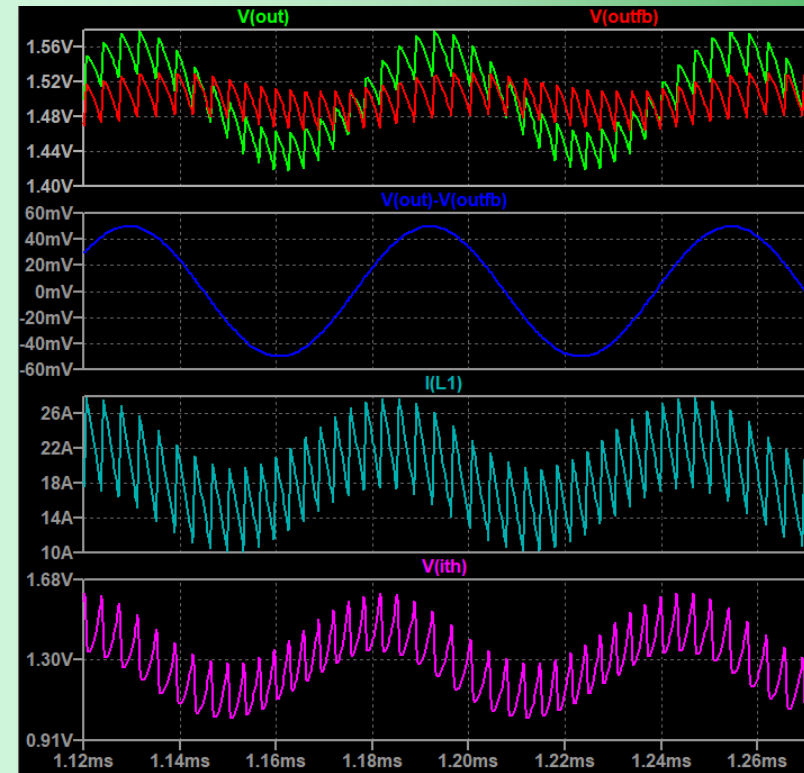
Ideally, sinusoidal pattern should be evident and symmetric

- Look for signs of non-linearity, which would indicate stimulus amplitude too large
- Note that there are discontinuities when the frequency changes – these are expected

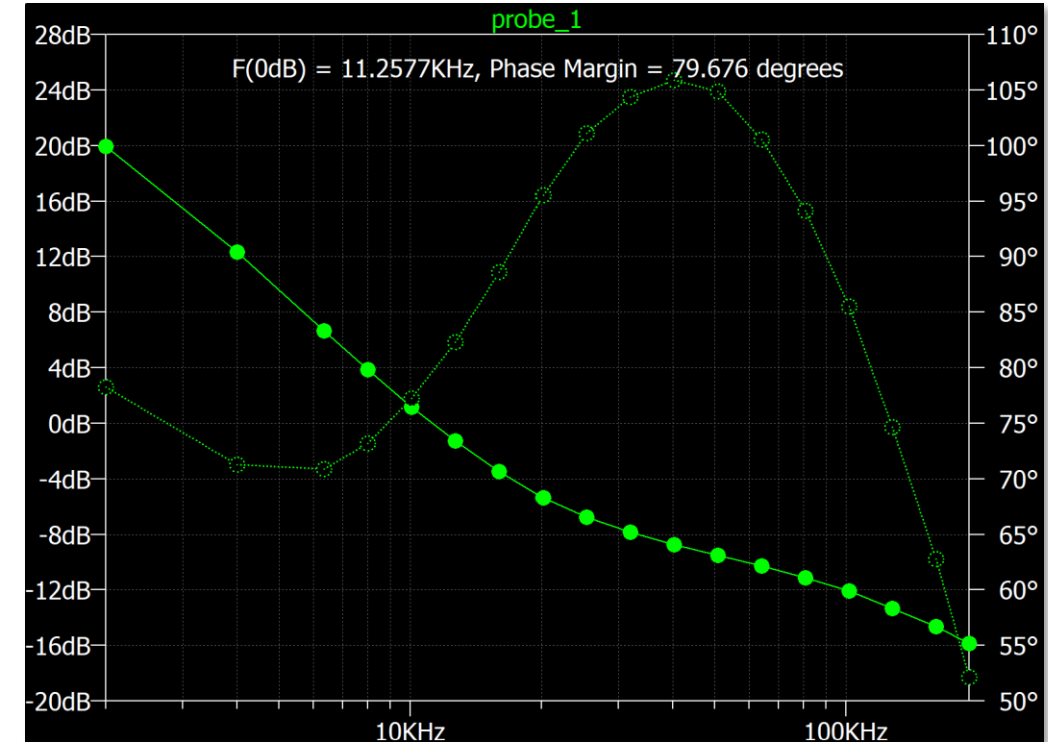
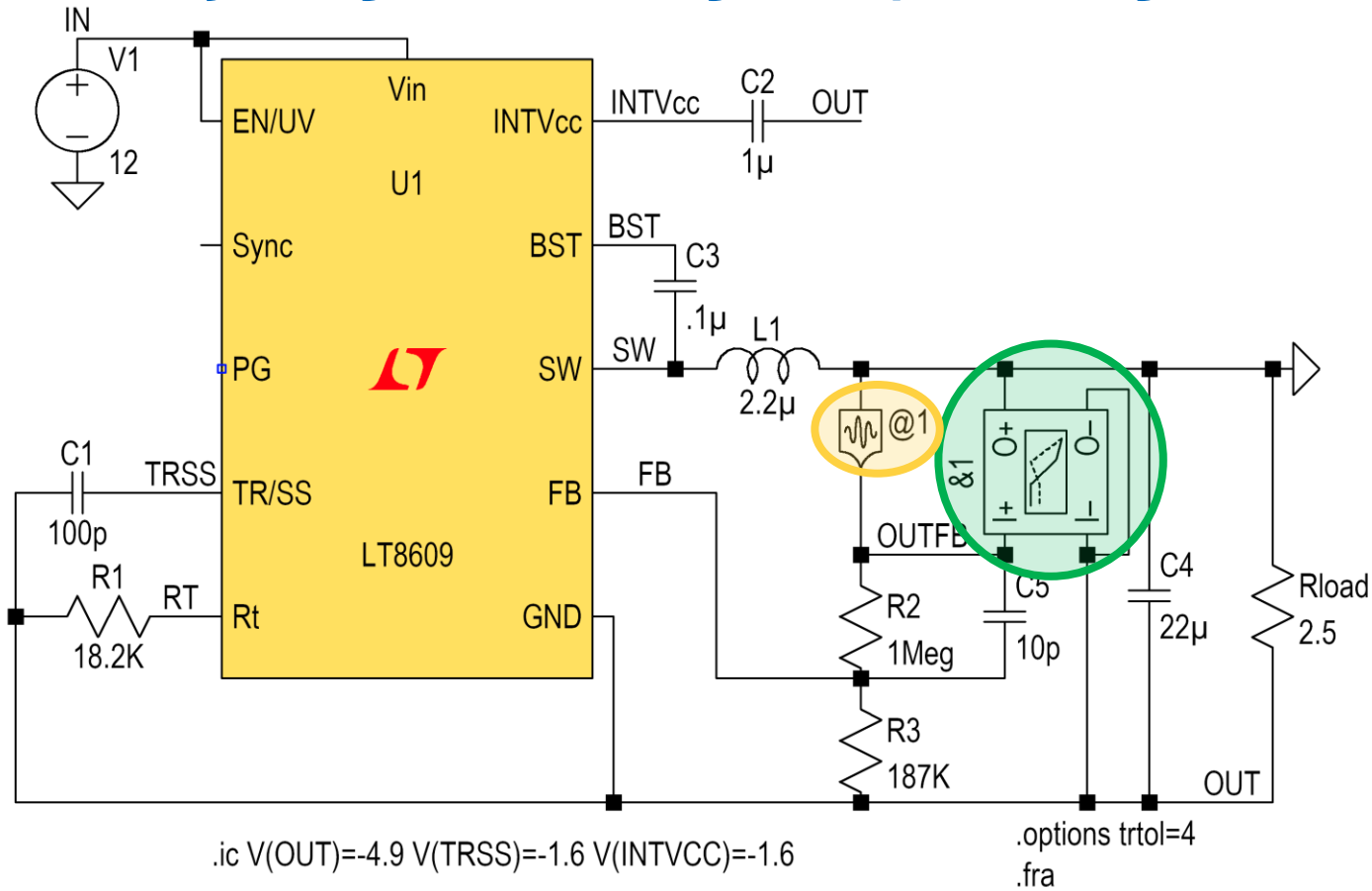
Bad
too much
stimulus



Good



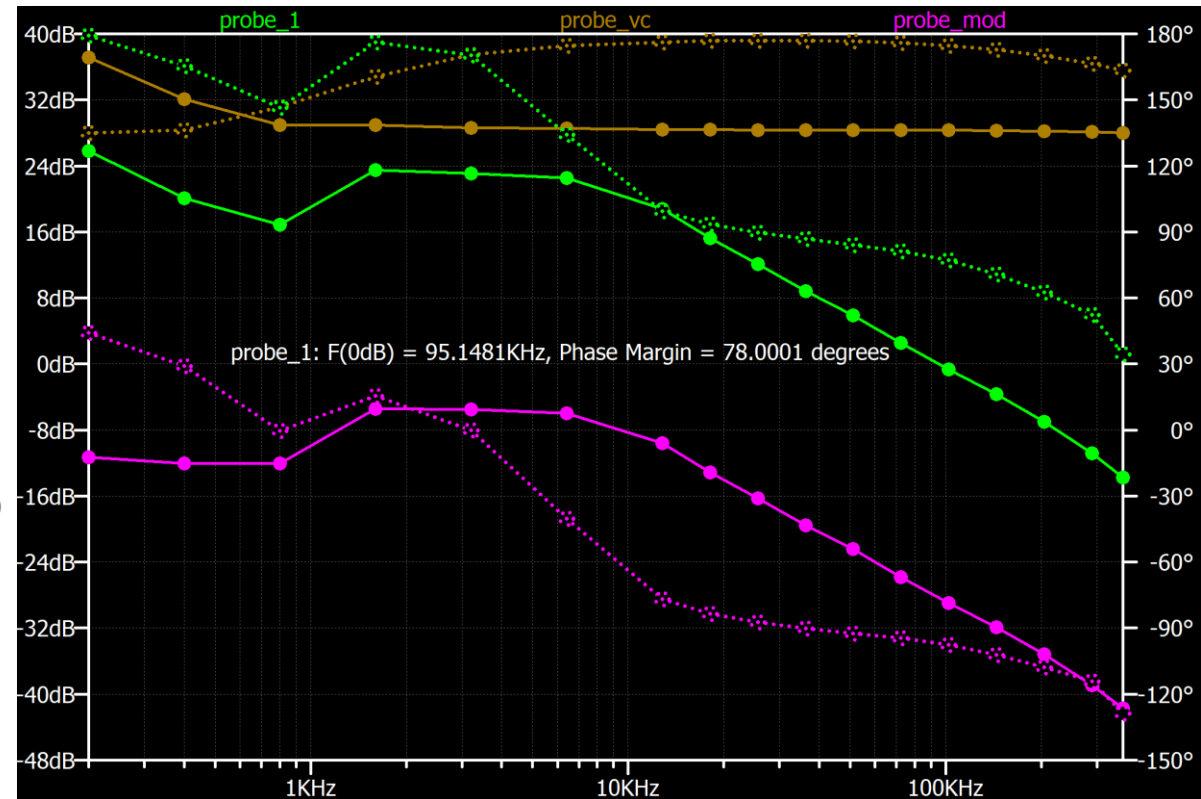
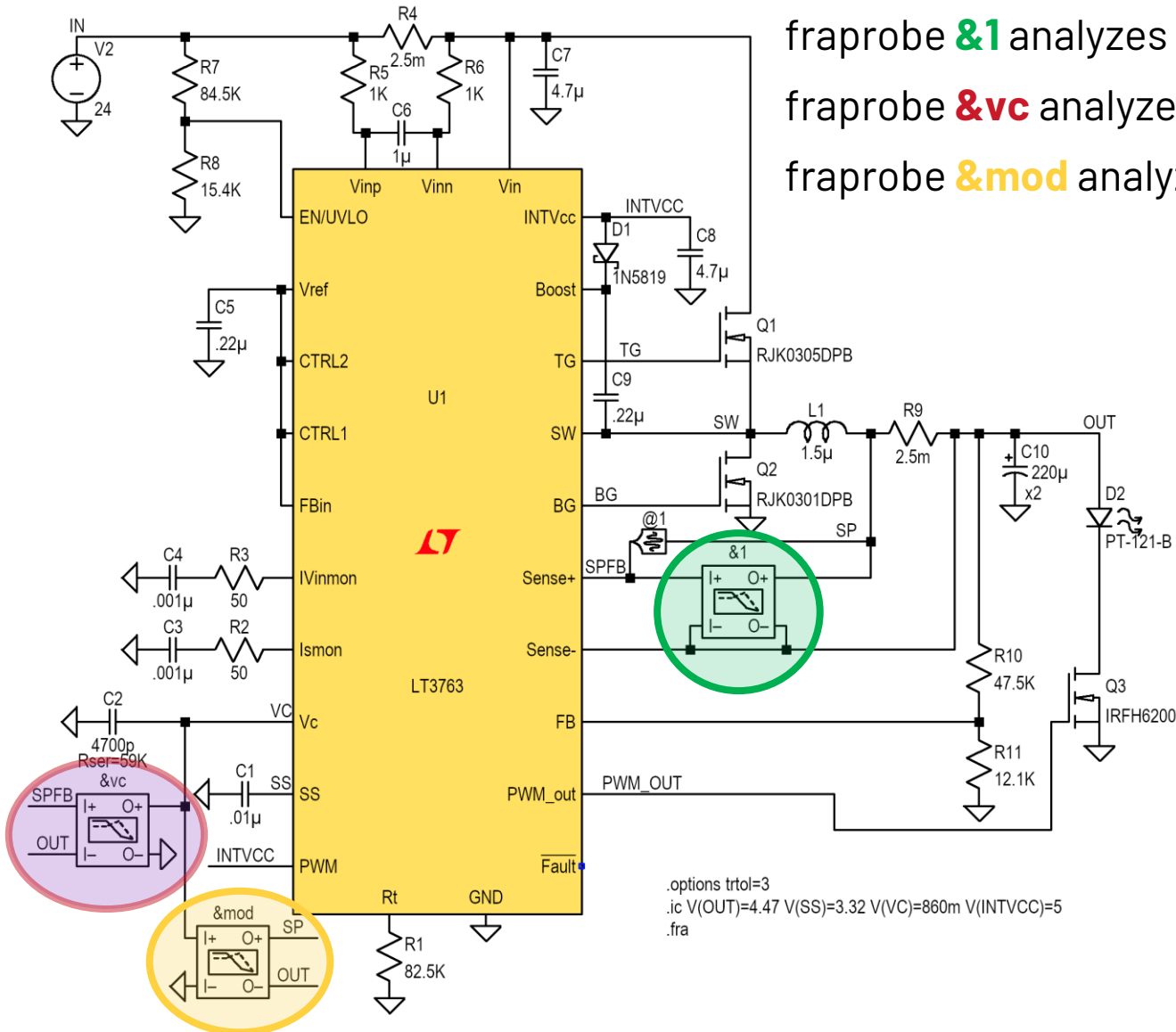
Analyzing Inverting Output Regulators



Connect the positive (O+, I+) terminals of the **fraprobe** across the **fra stimulus device**, negative fraprobe terminals (O-, I-) to the negative output

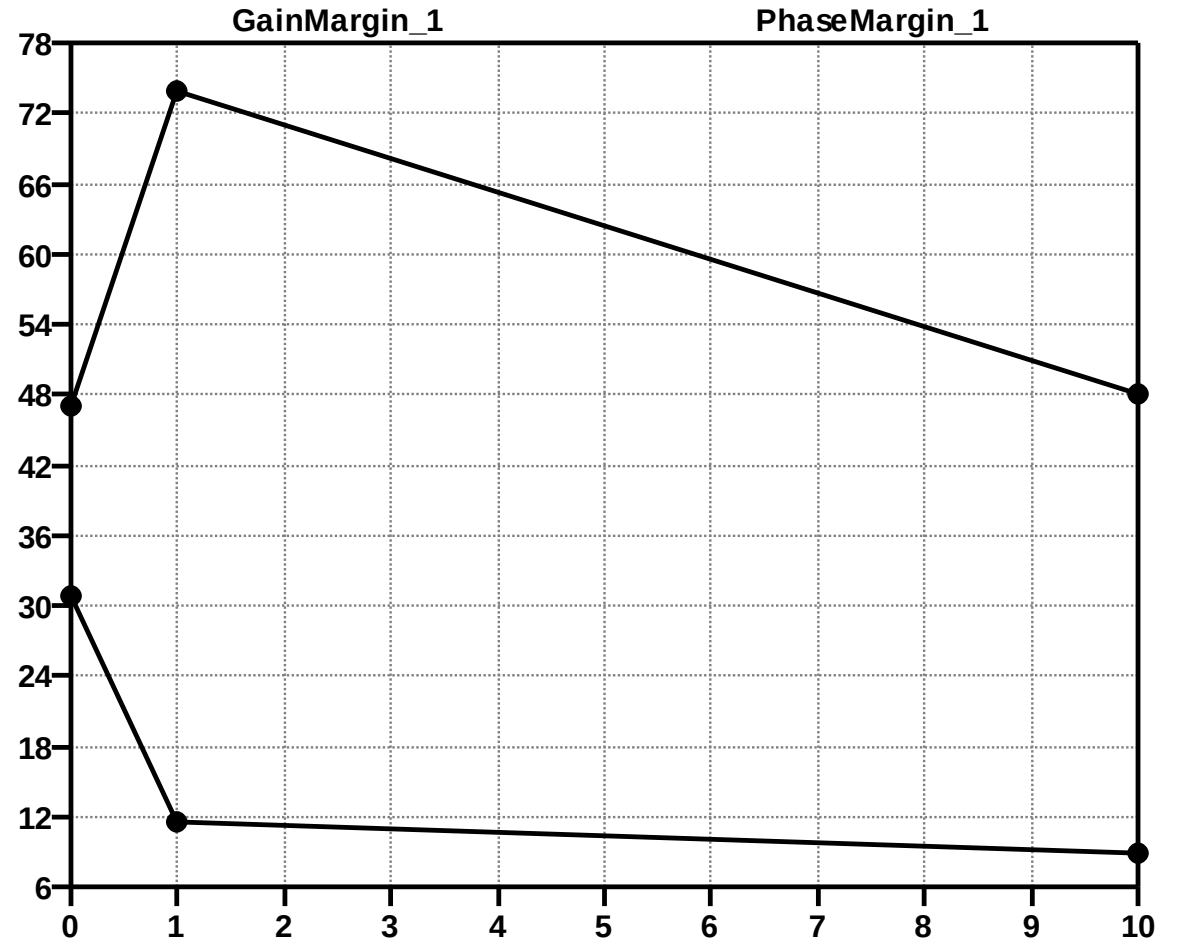
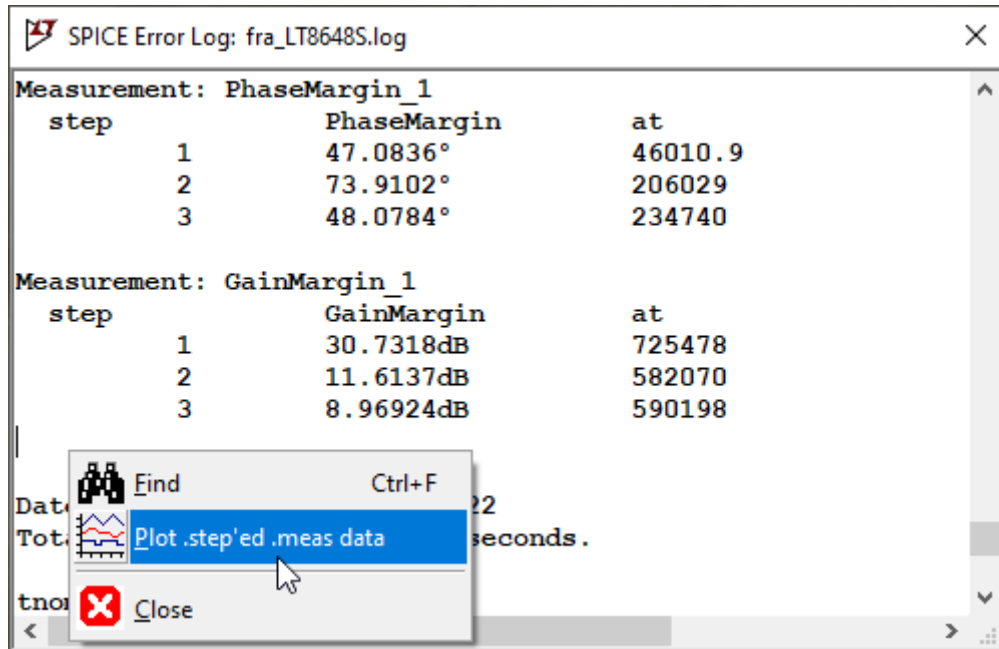
LTspice detects that the stimulus is grounded and automatically plots the **probe** gain

Current Feedback and Partial Loop Analysis



Example: Stepping A Parameter

Easily Plot Phase And Gain Margin





LTpowerCAD for loop analysis

LTpowerCAD in the center

LTpowerPlanner

System Level Power Tree

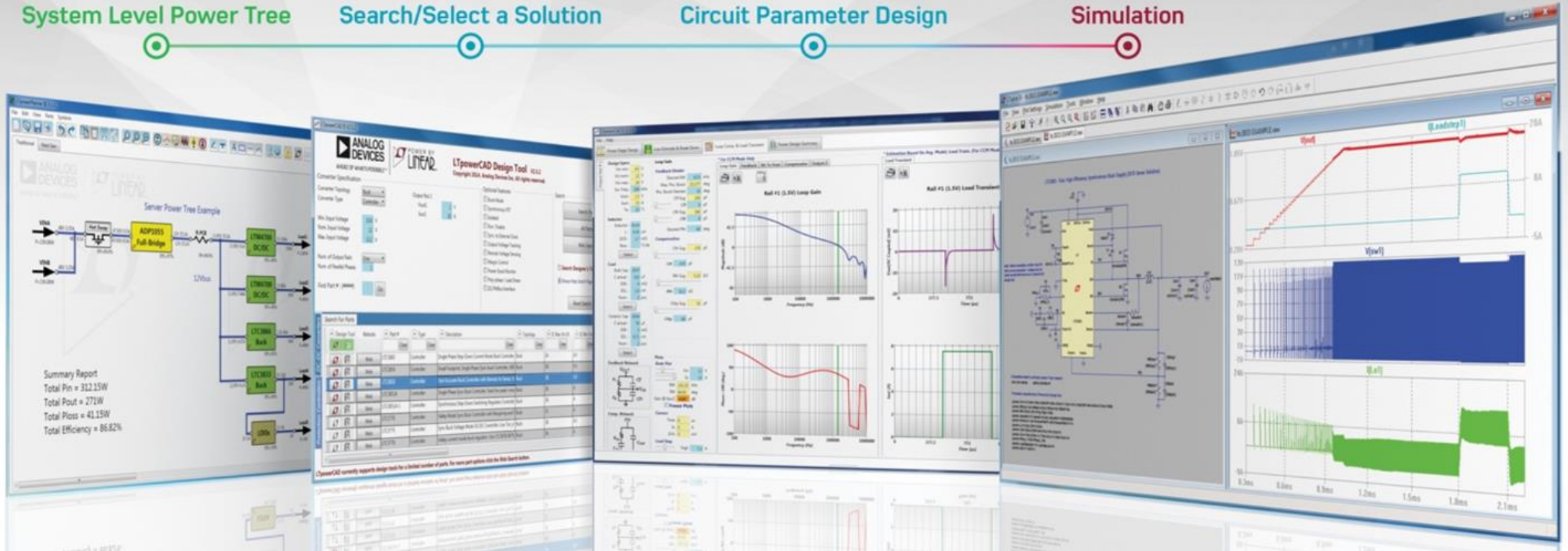
LTpowerCAD

Search/Select a Solution

Circuit Parameter Design

LTspice

Simulation



Selecting external components

LTpowerCAD II V2.7.1

File Help

Power Stage Design Loss Estimate & Break Down Loop Comp. & Load Transient Power Design Summary

Key

User Entry:
Calculated:

Part Specs

Max Vin: 38 V
Min Vin: 4.5 V
Max Vout: 5.5 V
Sugg. Max Iout: 50 A
Min Sw. Freq.: 200 kHz
Max Sw. Freq.: 2000 kHz

Design Specs

Vin min: 10.8 V
Vin nom: 12 V
Vin max: 13.2 V
Switching Freq: 502 kHz
Ta: 25 °C

Output Rail 1

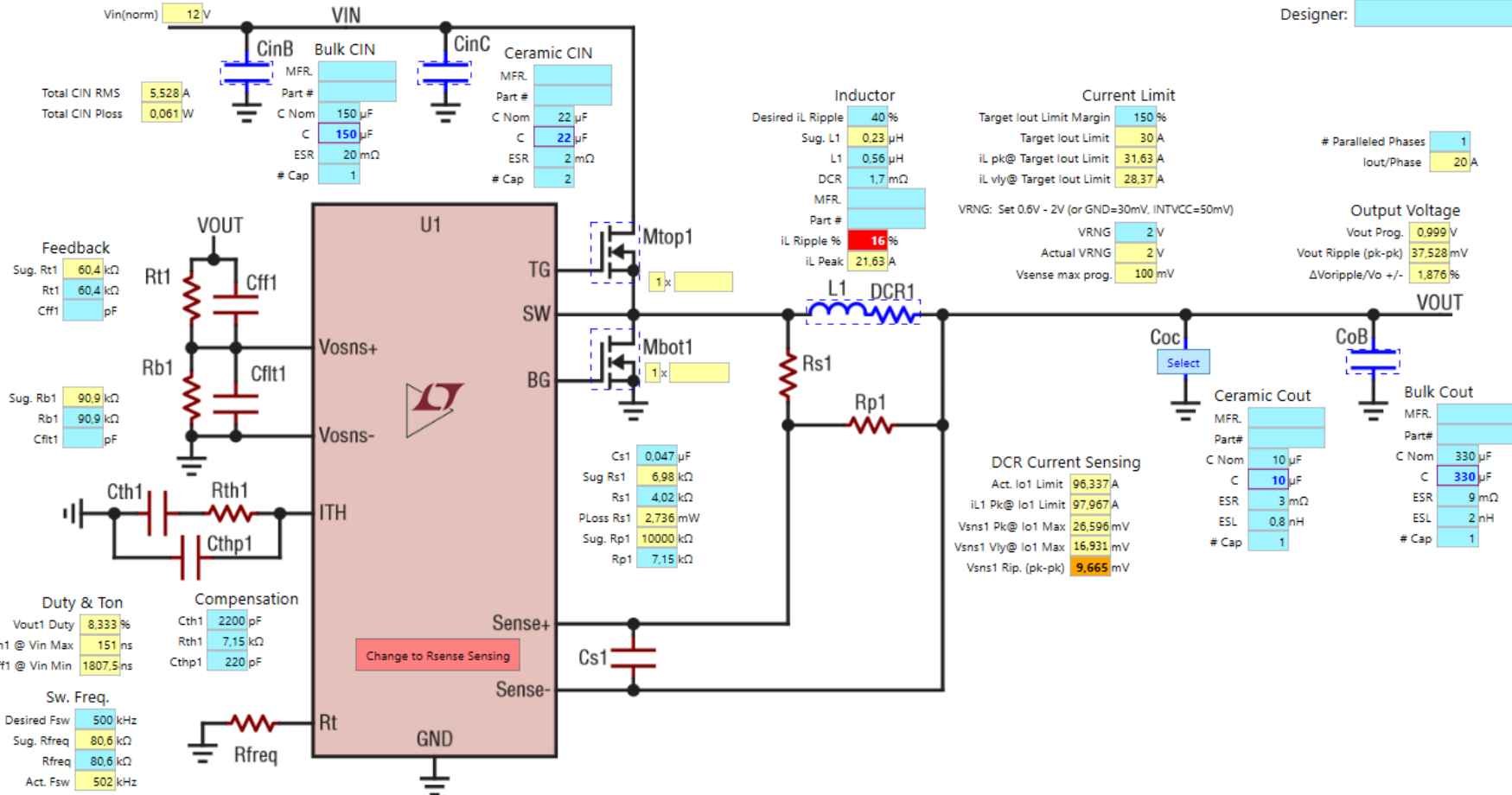
Vout1: 1 V
Iout1: 20 A

LTC3833 - Fast Accurate Step-Down DC/DC Controller with Differential Output Sensing

Project Name:

Date:

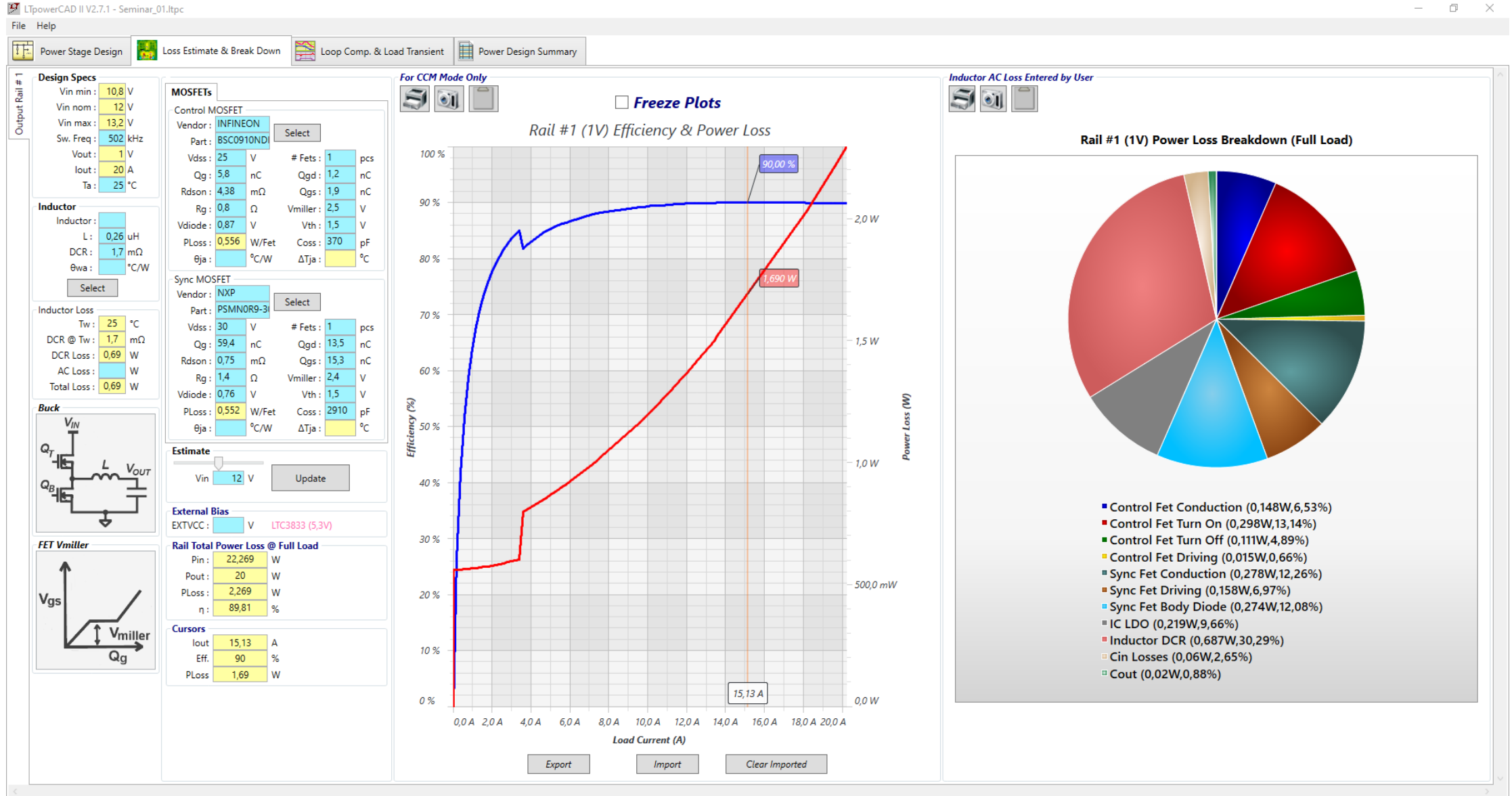
Designer:



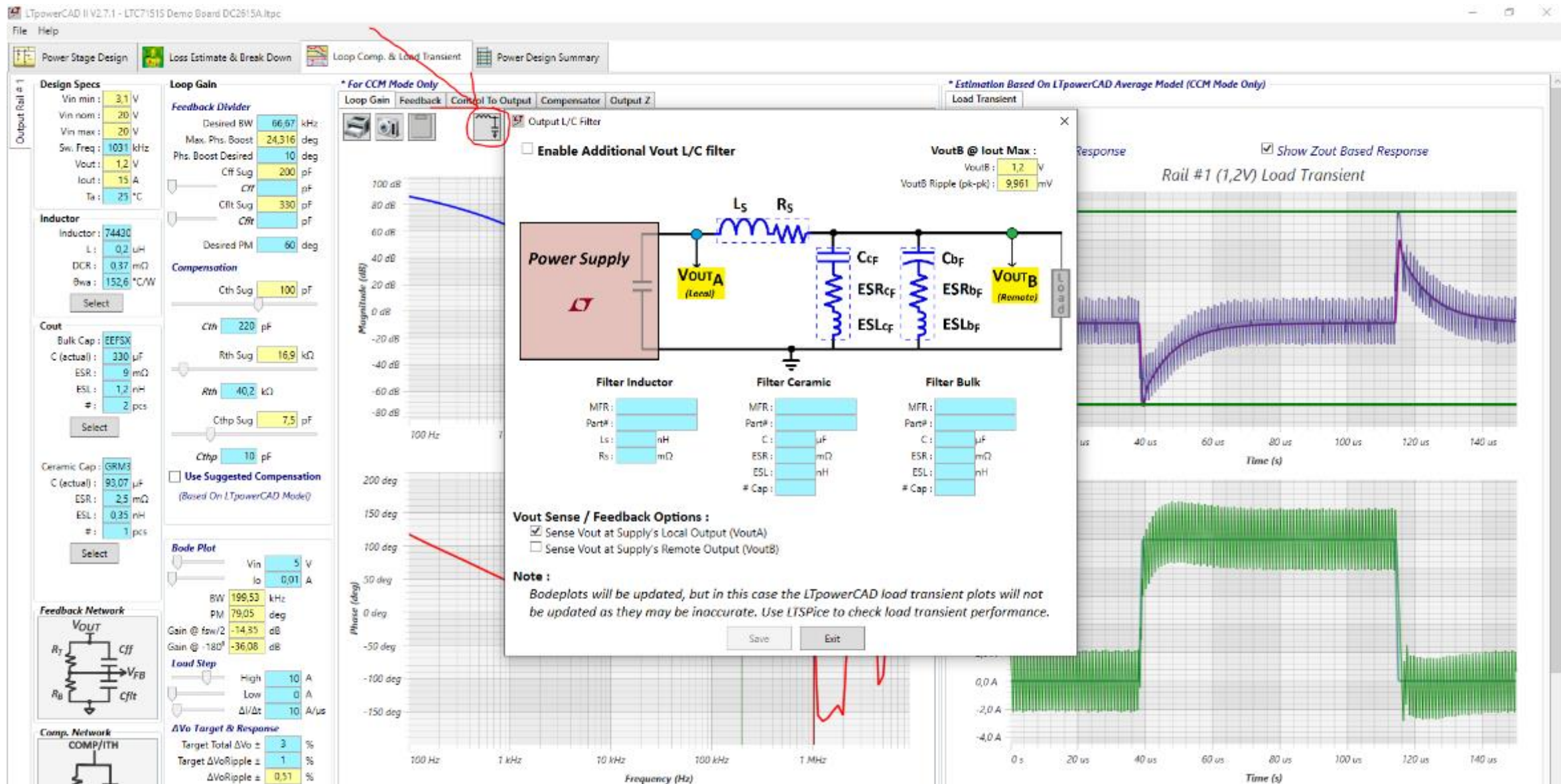
Feedback Loop & Transient Designs



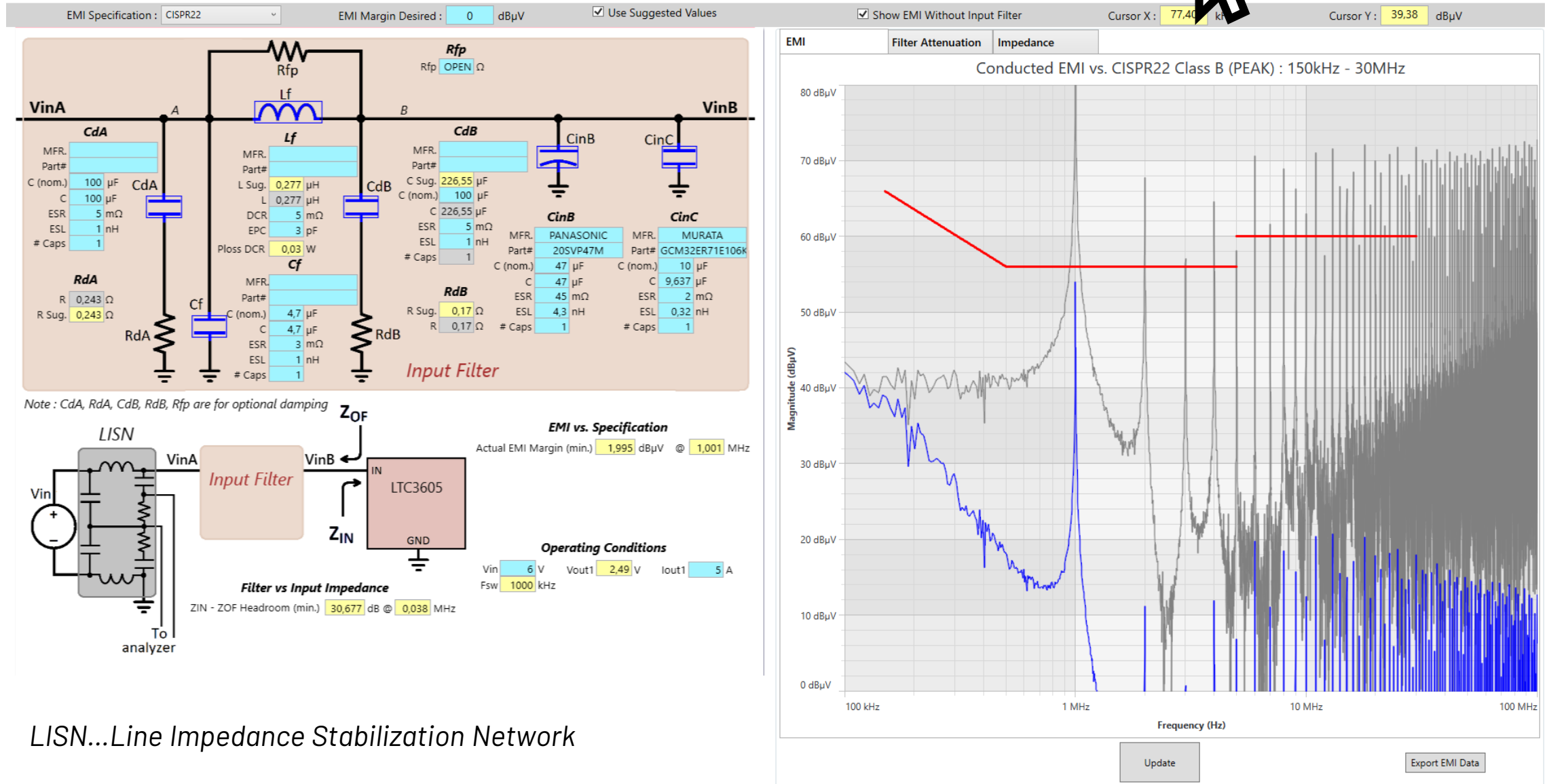
Efficiency Optimization



Designing an output filter



Conducted (Differential Mode) EMI Filter Design





Simulating Tolerances with Monte Carlo

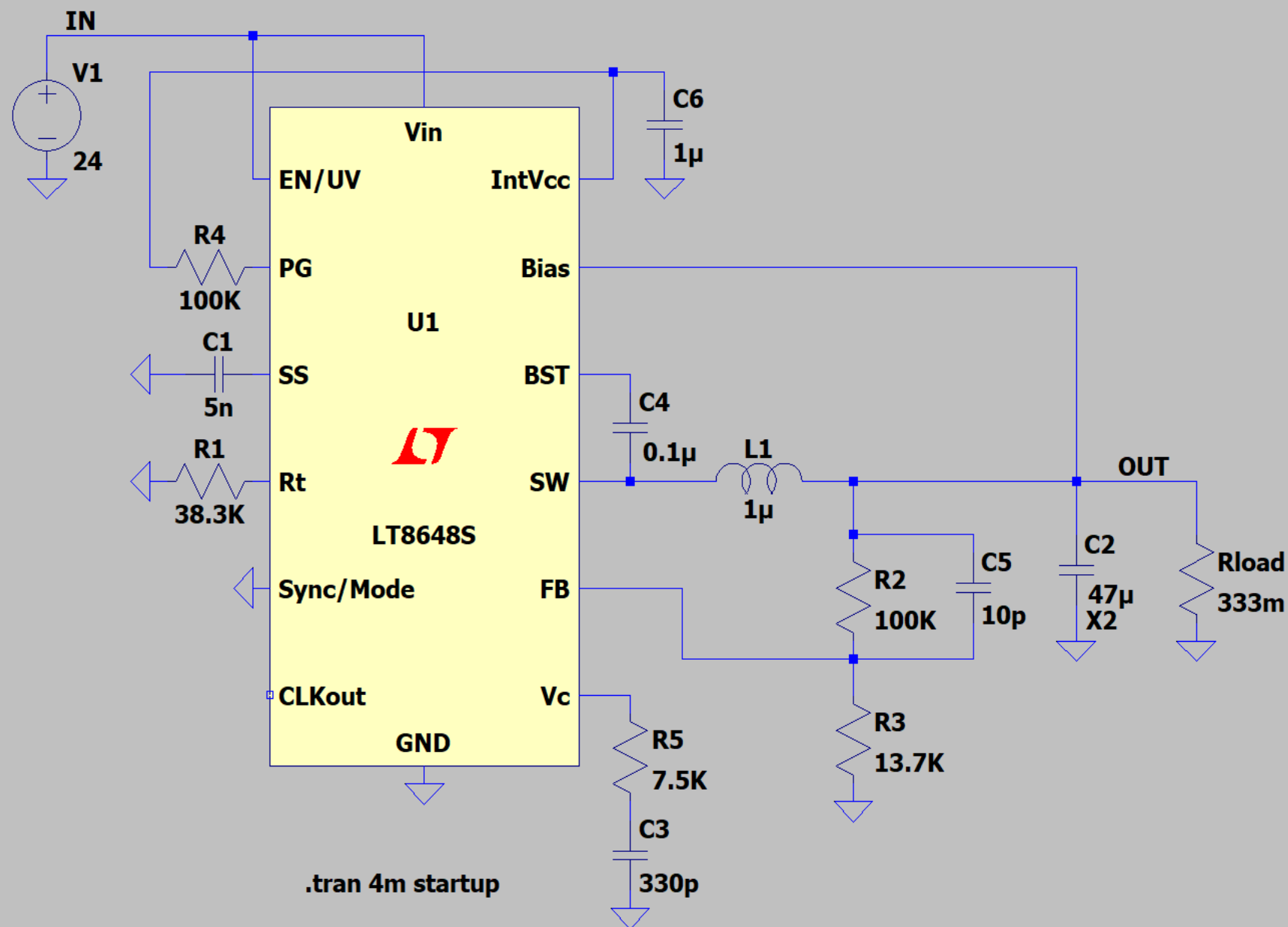
Monte Carlo Simulations: Statistical Functions

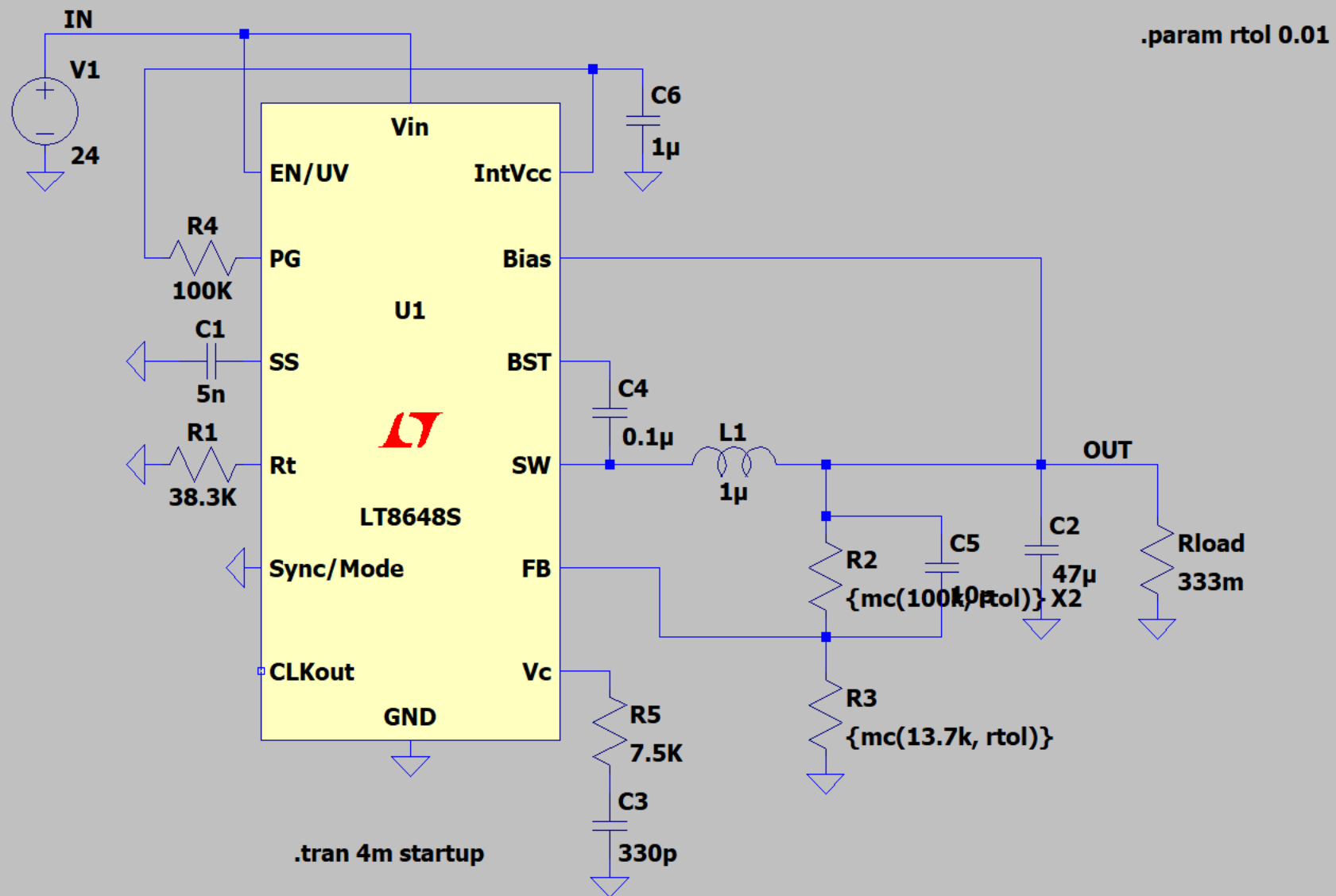
LTspice provides several statistical functions

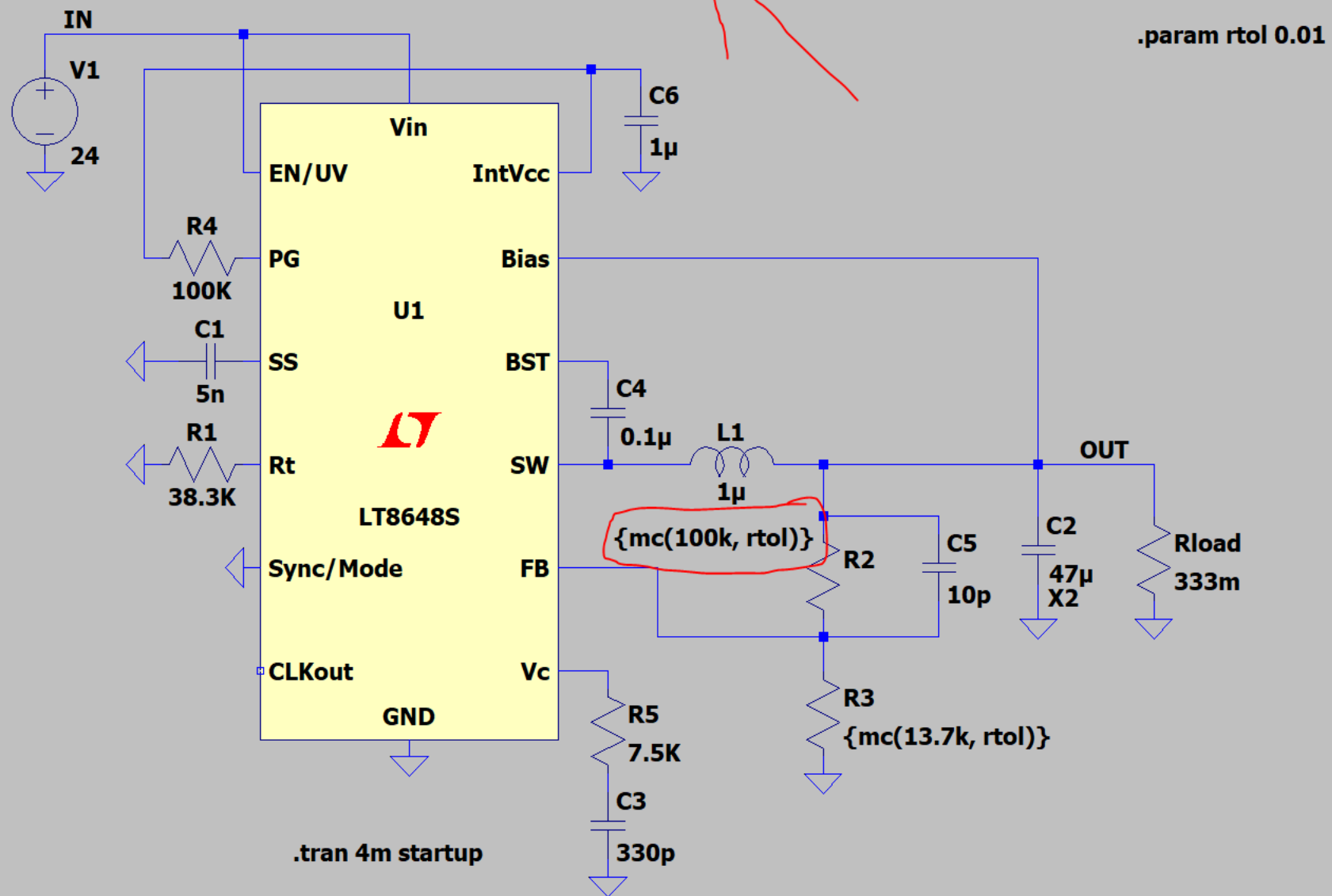
flat(x)	Random number between -x and x with uniform distribution
gauss(x)	Random number from Gaussian distribution with sigma of x.
mc(x,y)	A random number between $x*(1+y)$ and $x*(1-y)$ with uniform distribution.
rand(x)	Random number between 0 and 1 depending on the integer value of x.
random(x)	Similar to rand(), but smoothly transitions between values.

Most popular for Monte Carlo simulations:

- mc(x,y) for device parameters with target values not equal to zero
 - R, C, V, ...
- flat(x) for parameters which are ideally 0
 - offset



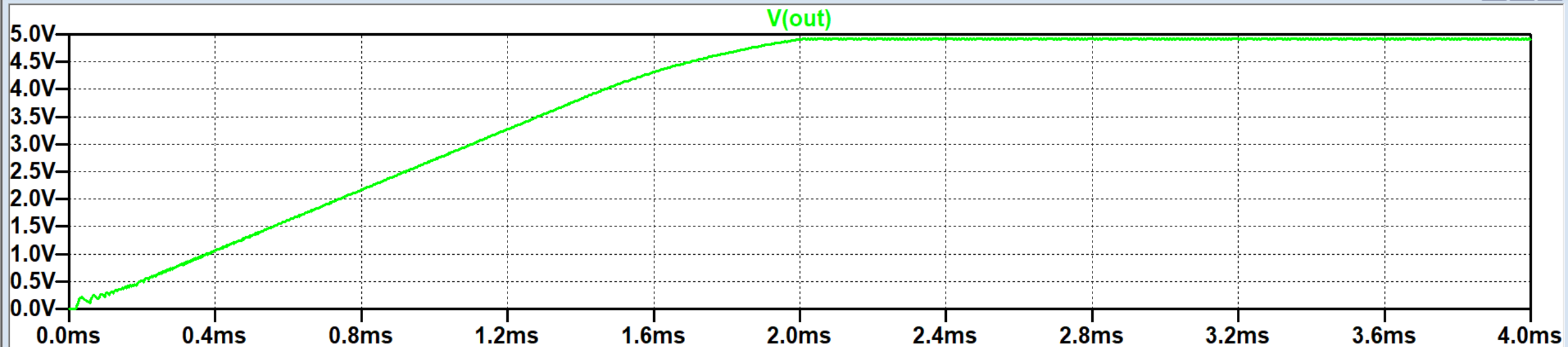




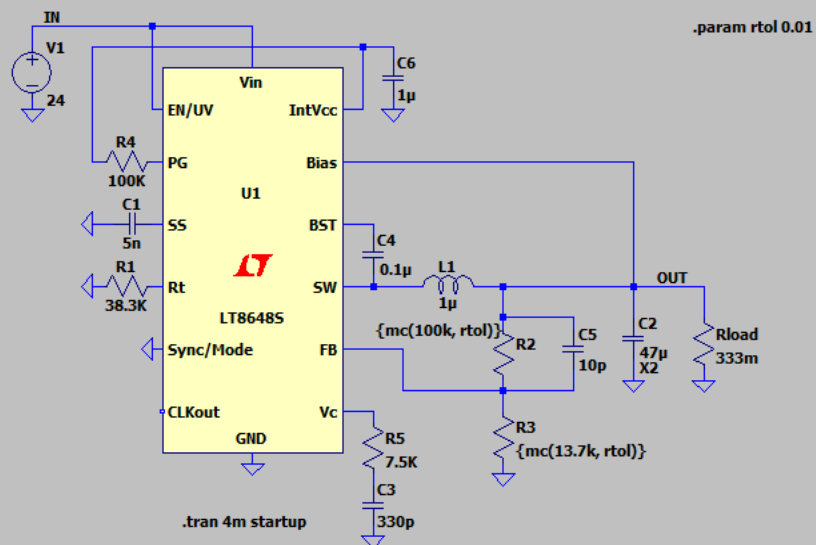


LT8648S LT8648S

LT8648S



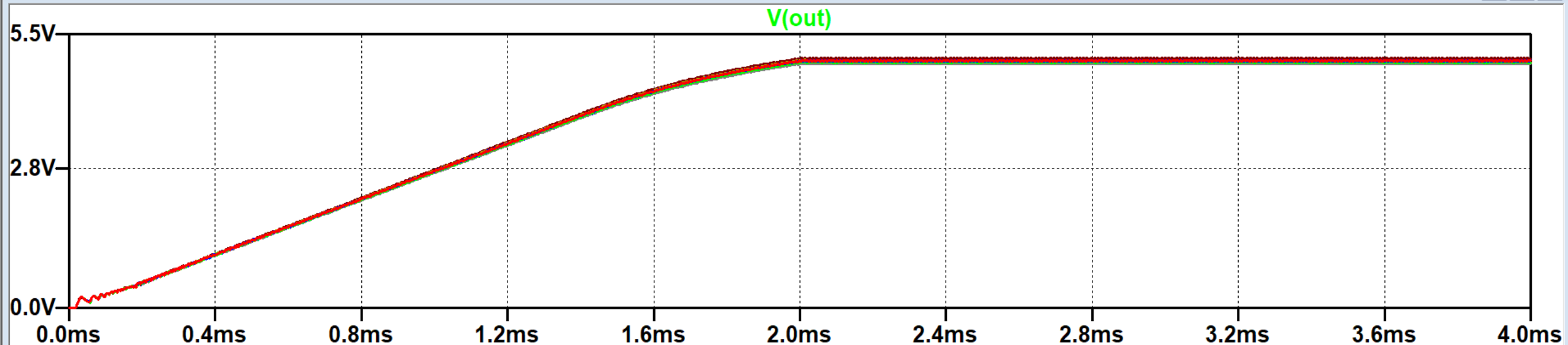
LT8648S



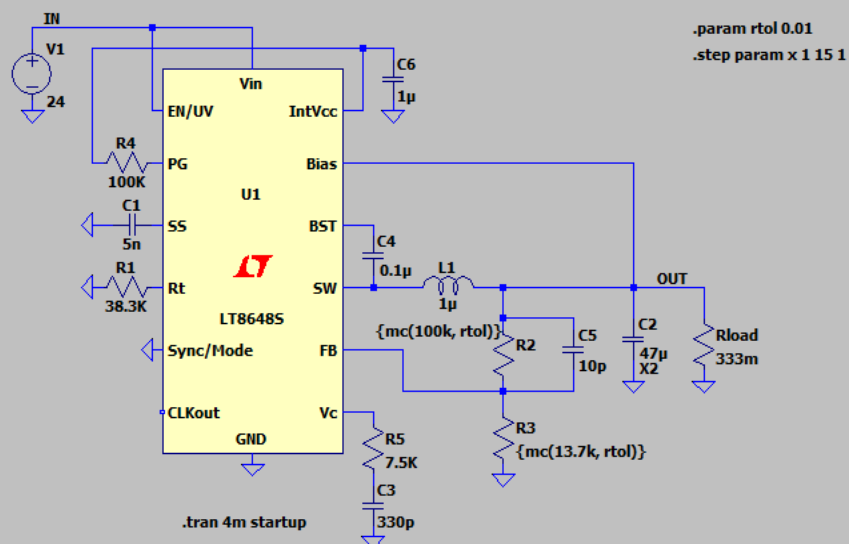


LT8648S LT8648S

LT8648S



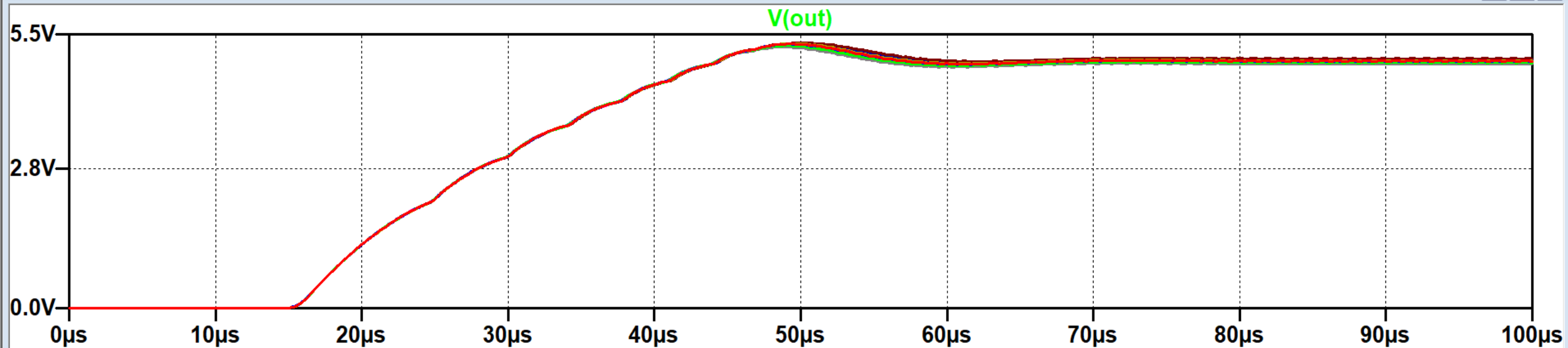
LT8648S



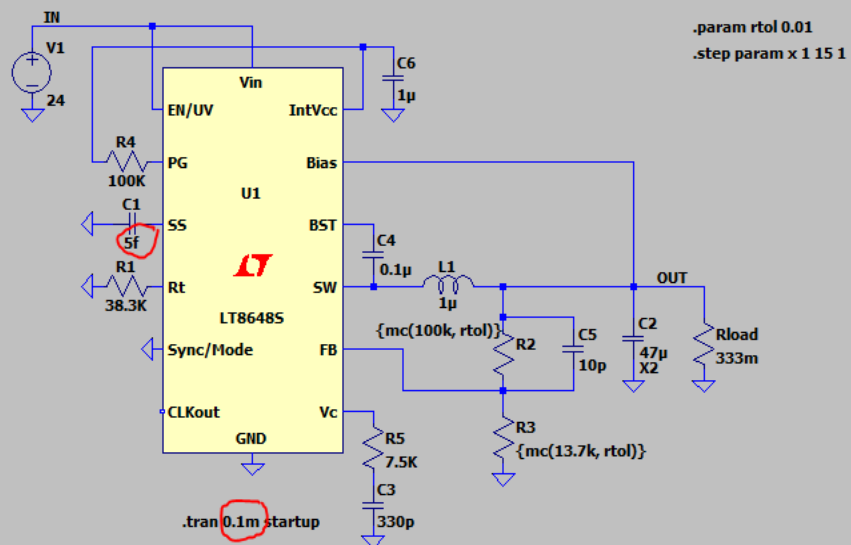


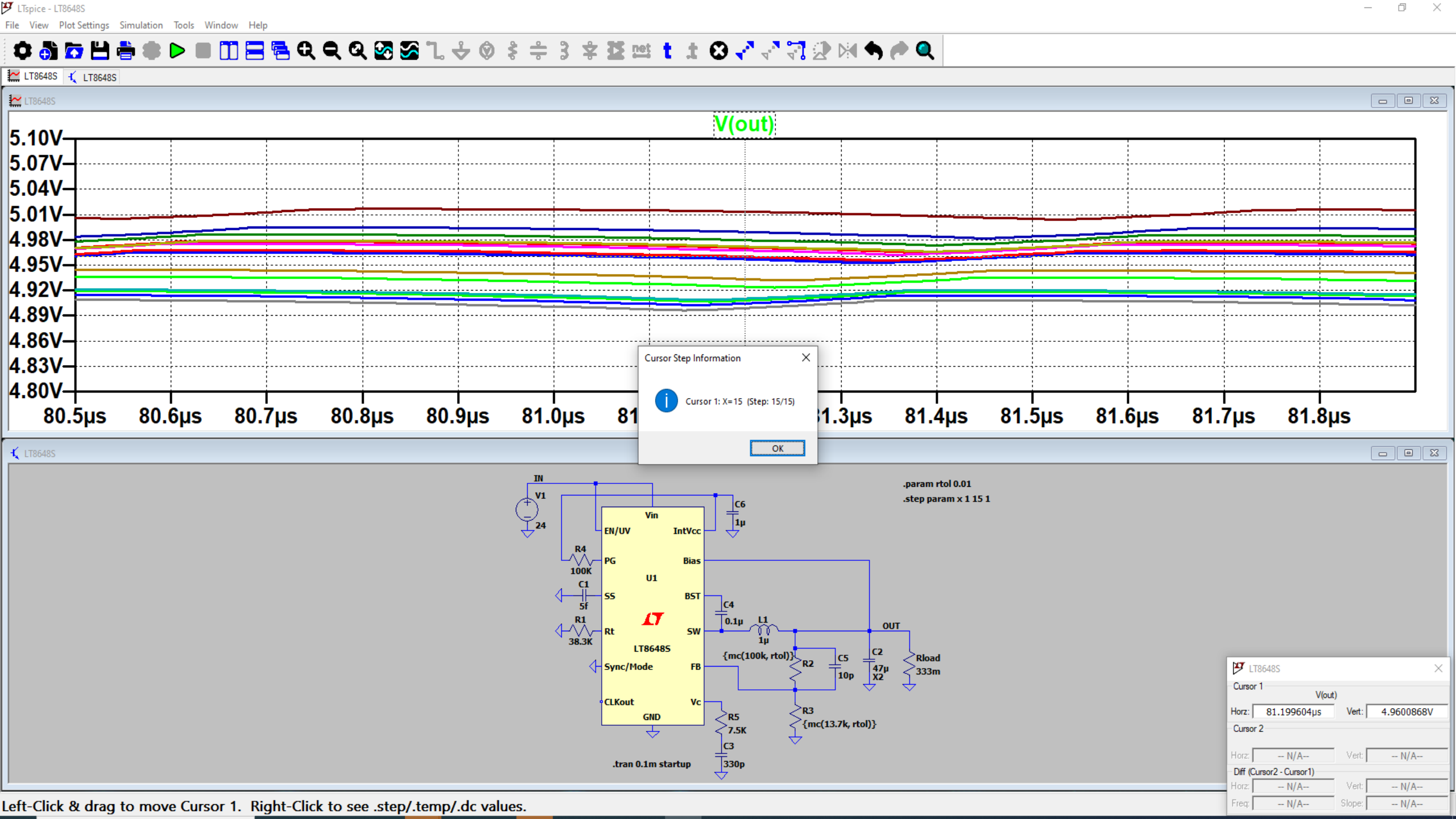
LT8648S LT8648S

LT8648S



LT8648S

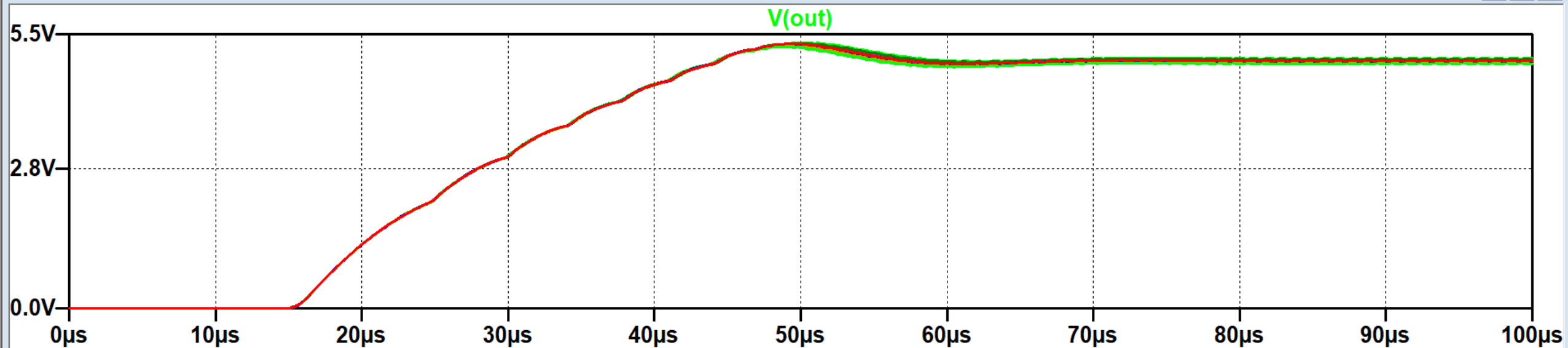




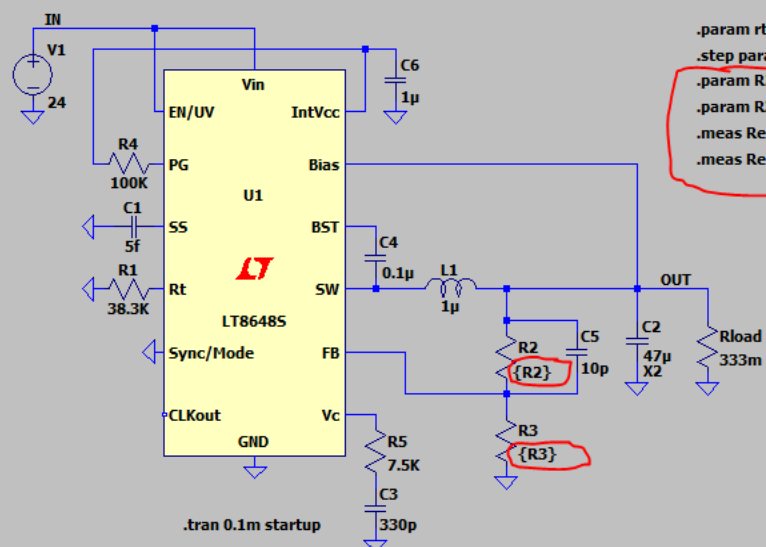


LT8648S LT8648S

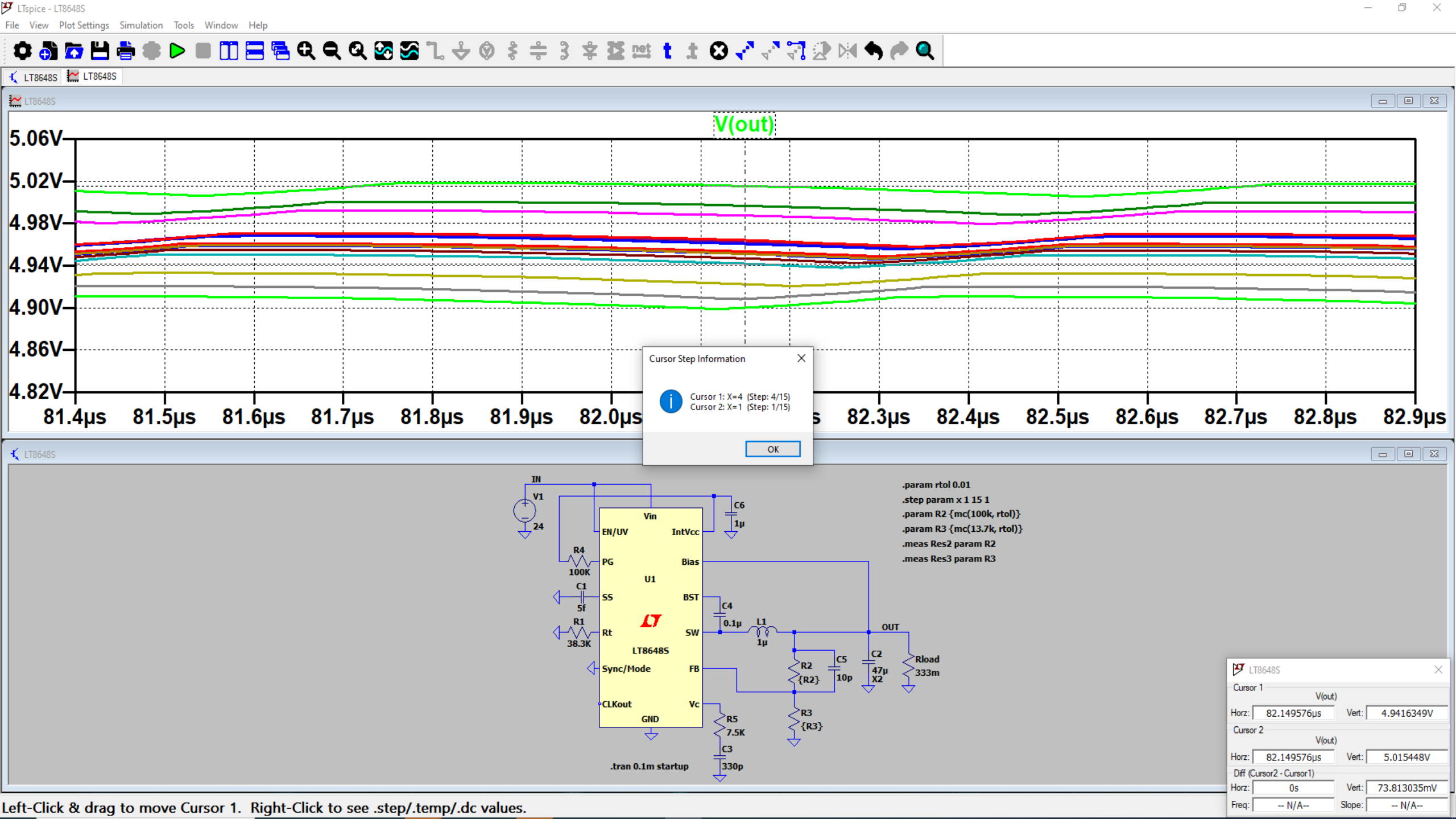
LT8648S



LT8648S



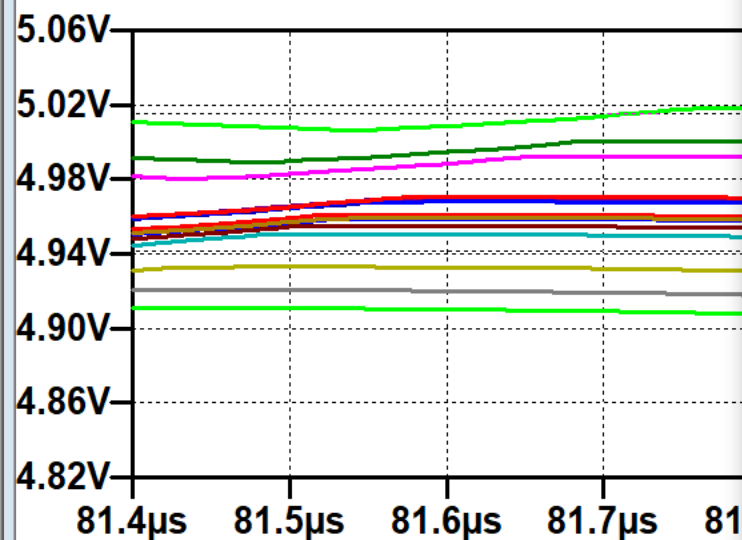
```
.param rtol 0.01
.step param x 1 15 1
.param R2 {mc(100k, rtol)}
.param R3 {mc(13.7k, rtol)}
.meas Res2 param R2
.meas Res3 param R3
```



LT8648S LT8648S

LT8648S



LT8648S

```
.step x=11
```

```
.step x=12
```

```
.step x=13
```

```
.step x=14
```

```
tnom = 27
```

```
temp = 27
```

```
method = modified trap
```

```
.step x=15
```

Measurement: res2

step	r2
1	100127
2	99959.7
3	100493
4	100027
5	99728.9
6	99891.4
7	99755.8
8	100214
9	99704.2
10	100605
11	100453
12	99284.7
13	99419.2
14	100999
15	99594.6

Measurement: res3

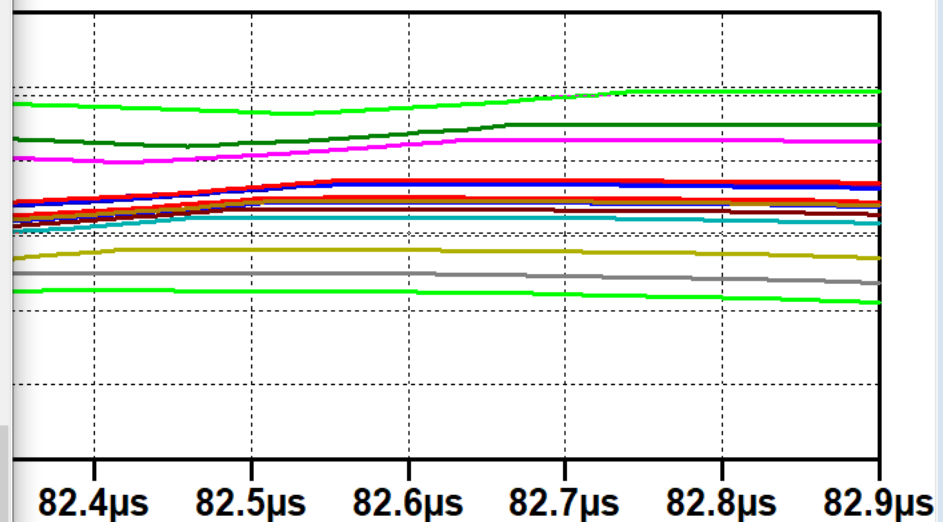
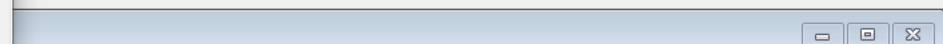
step	r3
1	13563.3
2	13723.3
3	13788.5
4	13757.7
5	13588
6	13833.9
7	13565.4
8	13727.9
9	13686.5
10	13777.6
11	13803
12	13710.8
13	13799.3
14	13836.1
15	13635.9

Total elapsed time: 22.236 seconds.

<

X

SPICE Output Log: C:\Users\FDosta\AppData\Local\LTspice\examples\Applications\LT8648S.log



```
m rtol 0.01  
param x 1 15 1  
m R2 {mc(100k, rtol)}  
m R3 {mc(13.7k, rtol)}  
s Res2 param R2  
s Res3 param R3
```

load
33m

LT8648S X

Cursor 1 V(out)

Horz: 82.149576μs Vert: 4.9416349V

Cursor 2 V(out)

Horz: 82.149576μs Vert: 5.015448V

Diff (Cursor2 - Cursor1)

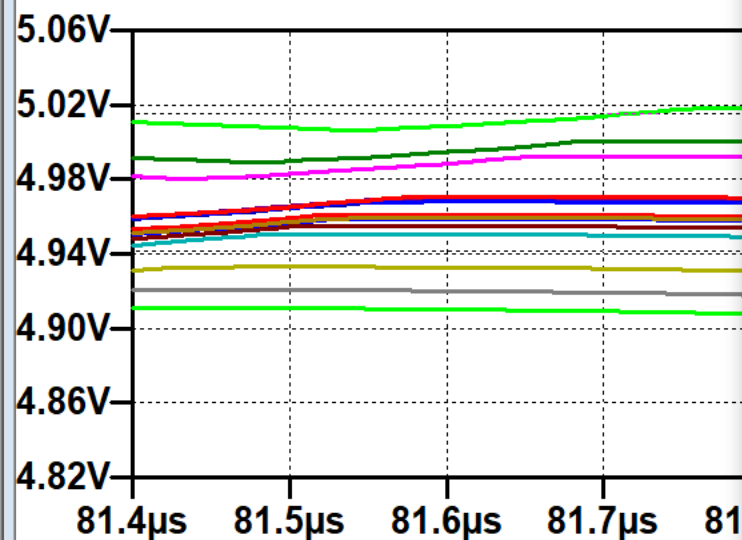
Horz: 0s Vert: 73.813035mV

Freq: -- N/A-- Slope: -- N/A--



LT8648S LT8648S

LT8648S



LT8648S

SPICE Output Log: C:\Users\FDosta\AppData\Local\LTspice\examples\Applications\LT8648S.log

.step x=11

.step x=12

.step x=13

.step x=14

tnom = 27

temp = 27

method = modified trap

.step x=15

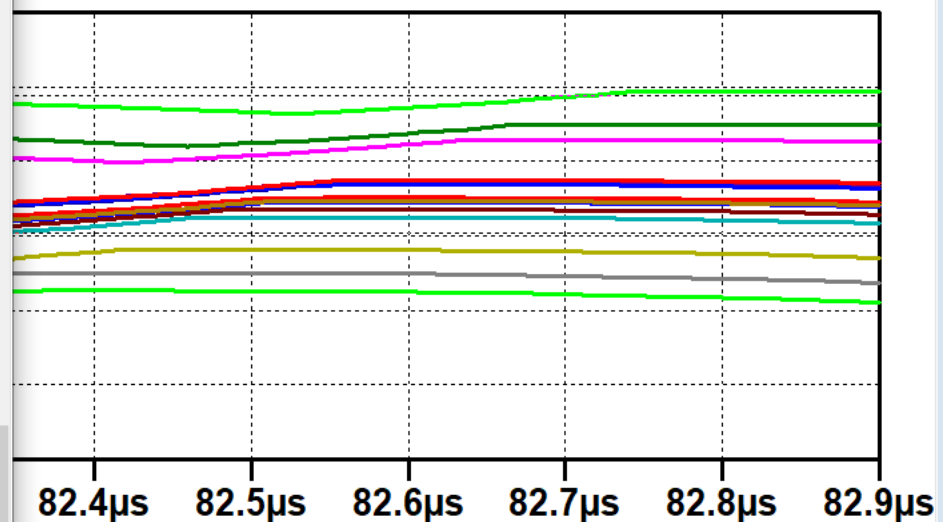
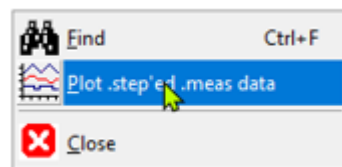
Measurement: res2

step	r2
1	100127
2	99959.7
3	100493
4	100027
5	99728.9
6	99891.4
7	99755.8
8	100214
9	99704.2
10	100605
11	100453
12	99284.7
13	99419.2
14	100999
15	99594.6

Measurement: res3

step	r3
1	13563.3
2	13723.3
3	13788.5
4	13757.7
5	13588
6	13833.9
7	13565.4
8	13727.9
9	13686.5
10	13777.6
11	13803
12	13710.8
13	13799.3
14	13836.1
15	13635.9

Total elapsed time: 22.236 seconds.



im rtol 0.01
param x 1 15 1
im R2 {mc(100k, rtol)}
im R3 {mc(13.7k, rtol)}
s Res2 param R2
s Res3 param R3

load
33m

LT8648S

Cursor 1 V(out)

Horz: 82.149576μs Vert: 4.9416349V

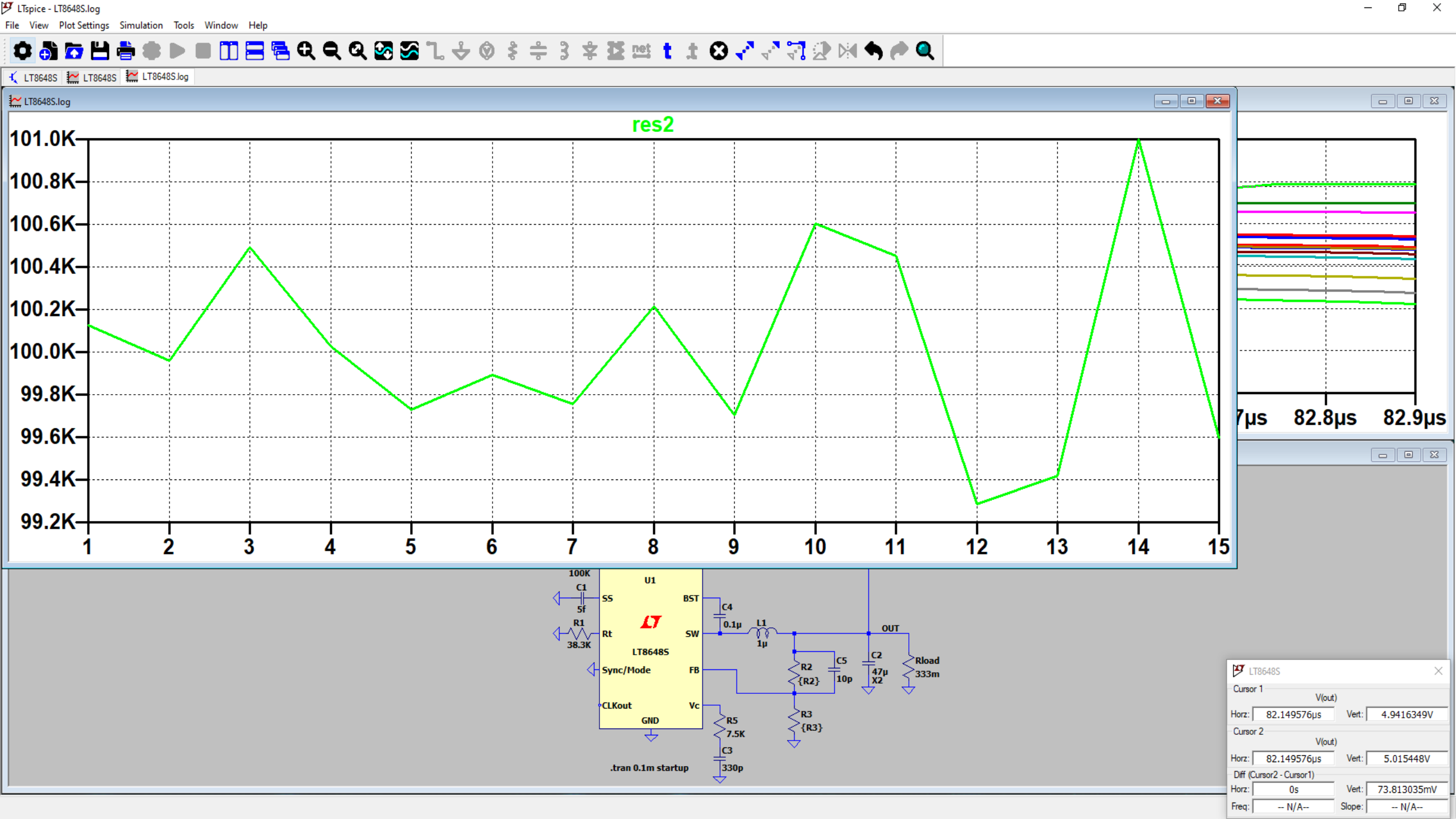
Cursor 2 V(out)

Horz: 82.149576μs Vert: 5.015448V

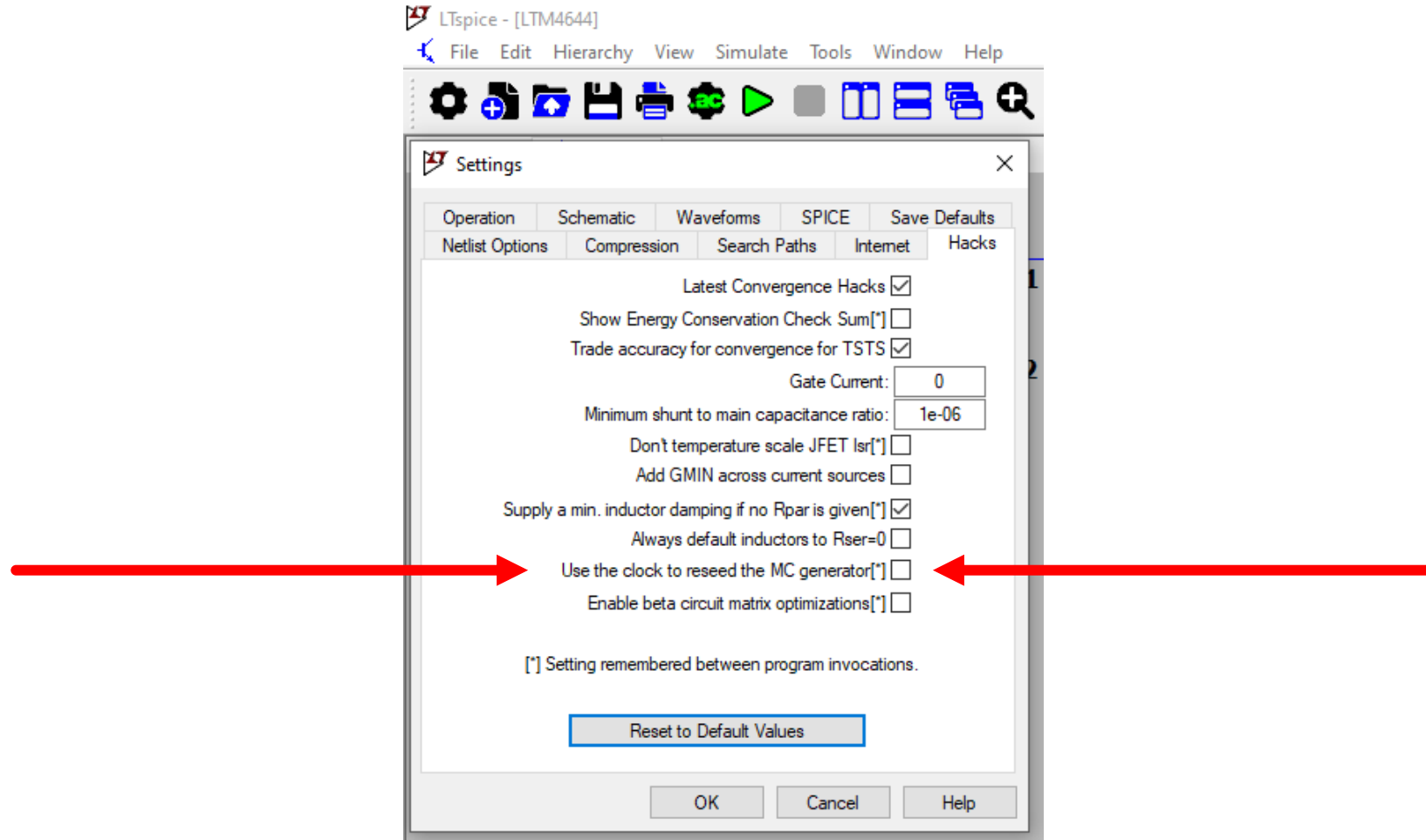
Diff (Cursor2 - Cursor1)

Horz: 0s Vert: 73.813035mV

Freq: -- N/A -- Slope: -- N/A --



Setting LTspice to use real random numbers



Reason for fixed 'random' pattern: While developing a simulation, it is very useful when repeated runs of the simulation behave the same. This way you can compare them and observe the differences resulting from changes YOU made to the schematic or to other parameters.



Simulating behavior of a power switch

[analog.com](https://www.analog.com)

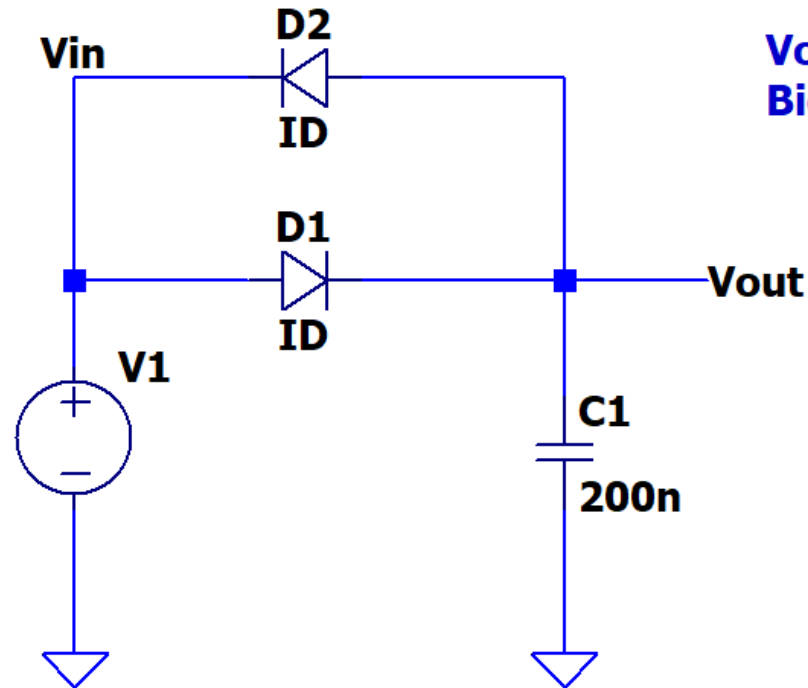
Voltage Source Current Limited

Usecase:

Simulating output Stages to drive capacitive loads like MOSFETS, IGBTs, SiC

C1=Load

For proper adjustment to a real Gate-Drive you may add a serial resistance to V1.



**Voltage Source with Current Limit
Bidirectional**

```
PULSE(0 10 1u 1n 1n 10u 20u 3)
.tran 100u
```

```
.model ID D(Ron=0 Roff=1G Vfwd=0 Ilimit=1)
```


Voltage Limiting Bidirectional I-Source

Use case: Driving power transistors (MOSFETS, SIC, IGBT) with large capacitive Gate.

D1, D2 are ideal Diodes

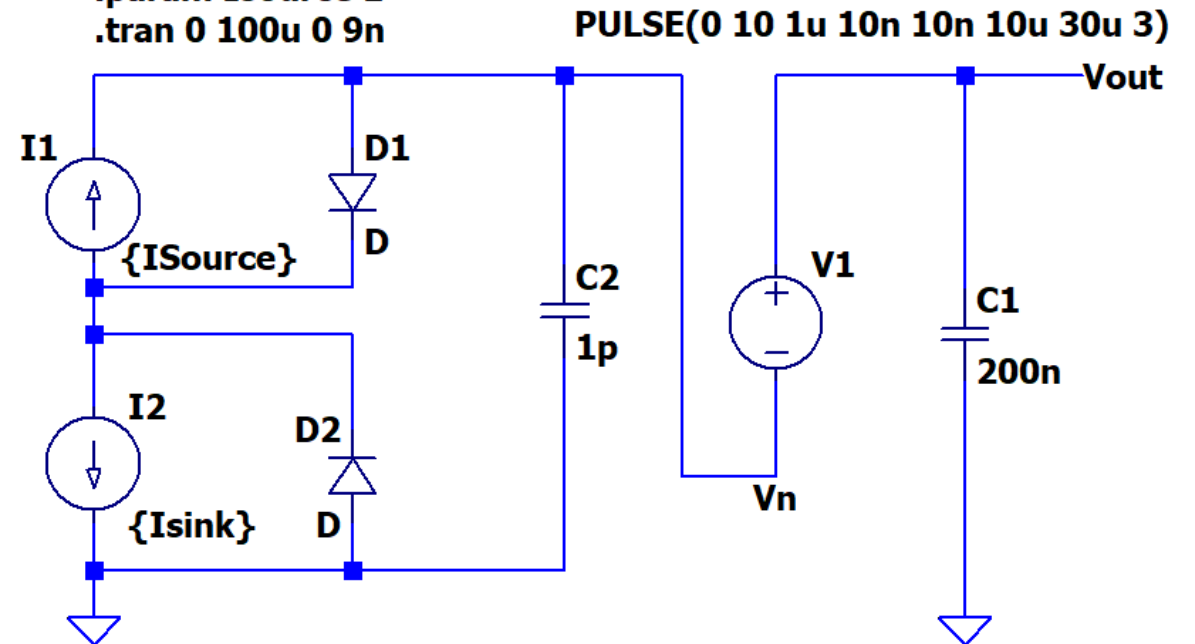
C2 is used to prevent high voltage spikes on Vn

C1 = Load

For proper adjustment to a real Gate-Drive you may add a serial resistance to V1.

Voltage Limiting Current Source

```
.model ID D(Ron=0 Roff=1G Vfwd=0)
.param Isink 1
.param Isource 1
.tran 0 100u 0 9n
```

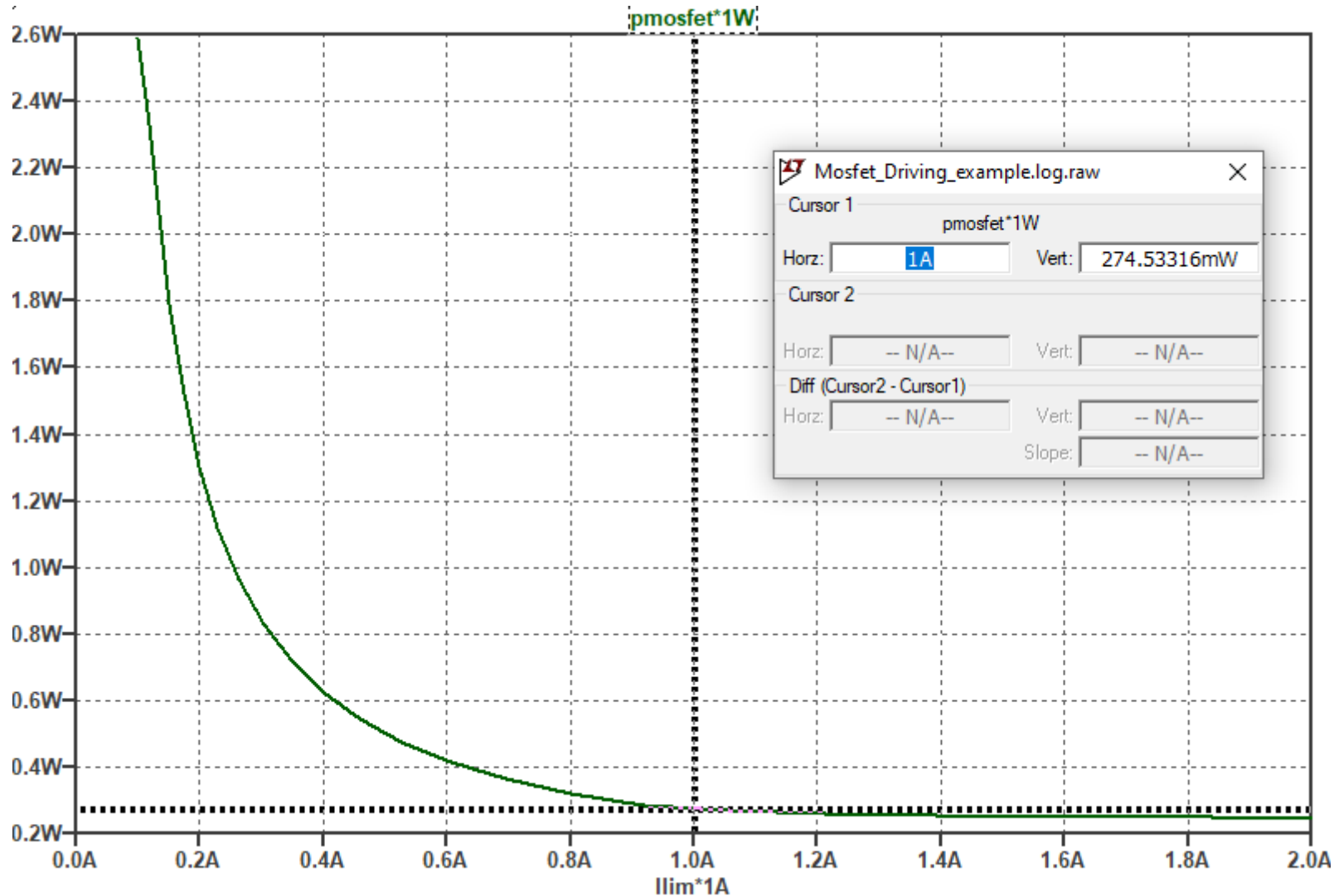




Steps to prepare:

1. Stepping the drive-current (I_{lim})
2. Measure Power-Loss
3. Plot stepped meas. data
 1. Ctrl-L (log-file)
 2. Right click: Plot stepped measurement data

Powerdissipation at different Drive Current



Conclusion:
Beyond 1A peak drive current, there is no further reduction in Power-loss of the MOSFET.

Powerloss of the MOSFET vs. Drive peak current

AHEAD OF WHAT'S POSSIBLE

analog.com

