Agenda

08:30 – 09:00		*Arrival / Registration / Coffee*
09:00 – 09:50		SMPS Topologies, tips and tricks (Analog Devices)
09:50 – 10:45		Filtering Considerations for DC/DC Converters (Wurth Electronics)
10:45 – 11:10		*Coffee Break & Networking Opportunity*
11:10 – 12:00		The Art of Loop Compensation (Wurth Electronics)
12:00 – 13:00		*Lunch*
13:00 – 13:50		LTspice Examples (Analog Devices)
13:50 – 14:45		Smart Selection of Inductors and Capacitors (Wurth Electronics)
14:45 – 15:10		*Coffee Break & Networking Opportunity*
15:10 – 16:00		PCB Board Layout Optimisation (Analog Devices)

ANALOG DEVICES

WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

LTspice examples

Frederik Dostal
Power Management Expert

analog.com

Agenda

New in LTspice24

Simulating loop stability

LTpowerCAD for loop analysis

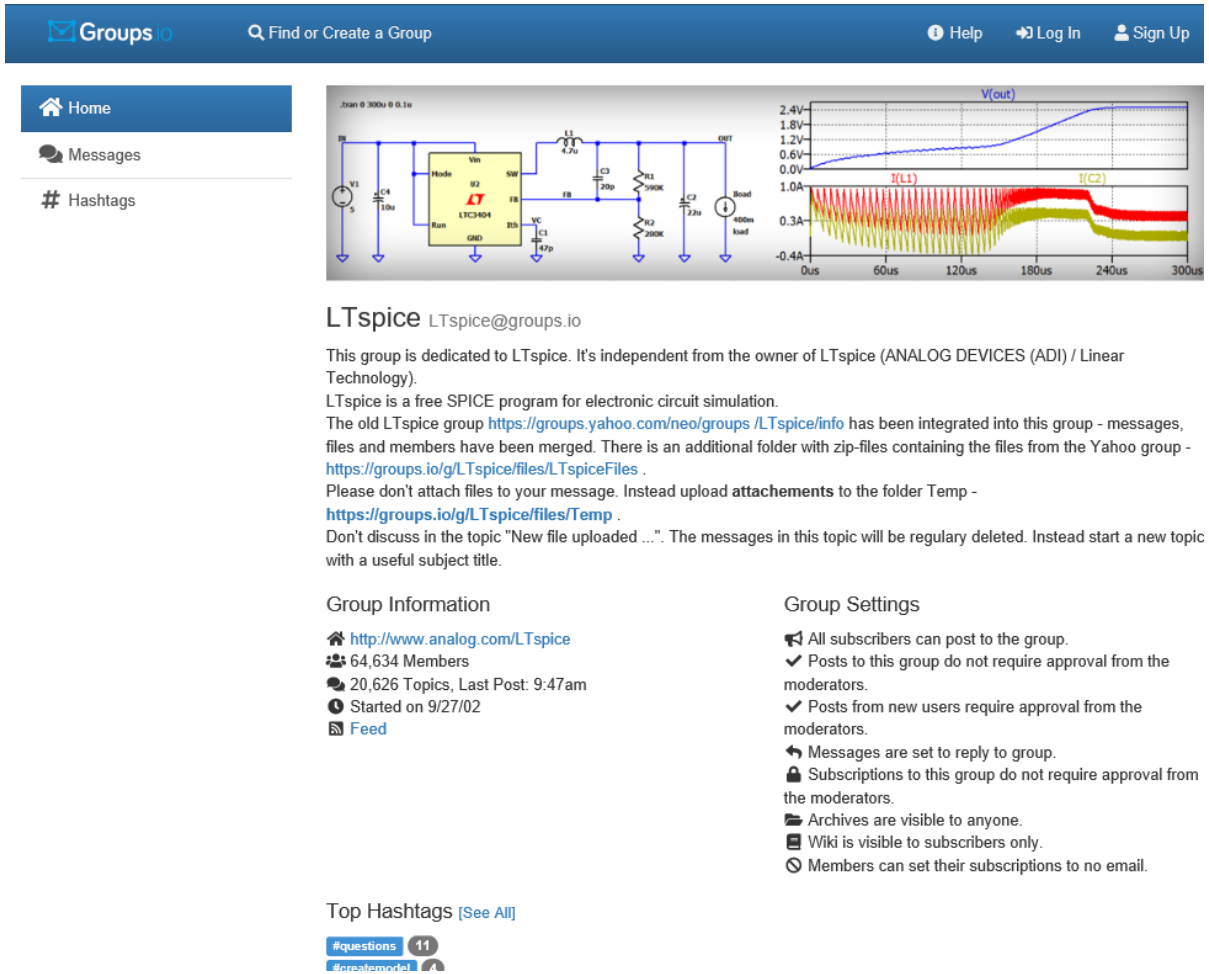
Simulating Tollerances with Monte Carlo

Simulating behavior of a power switch

LTspice Group.io User's Group

http://groups.io/g/LTspice

Several hundred posts per month



Group Information

http://www.analog.com/LTspice

64,634 Members

20,626 Topics, Last Post: 9:47am

Started on 9/27/02

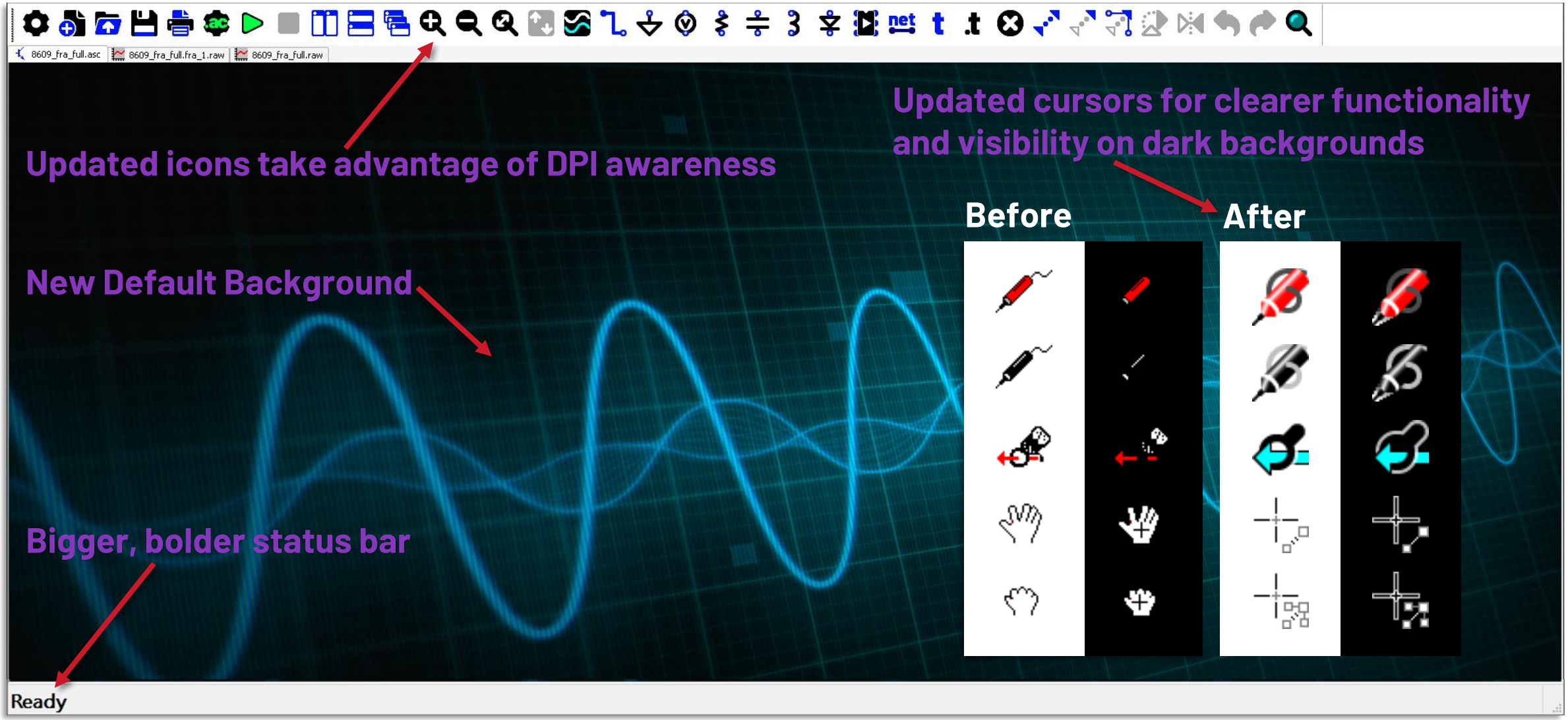
Feed

ANALOG DEVICES

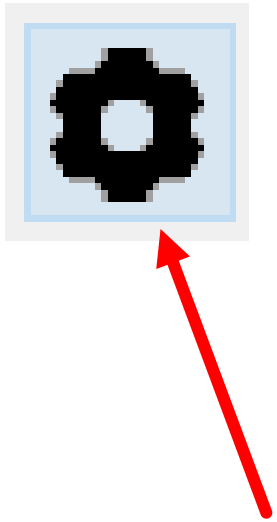
New in LTspice24

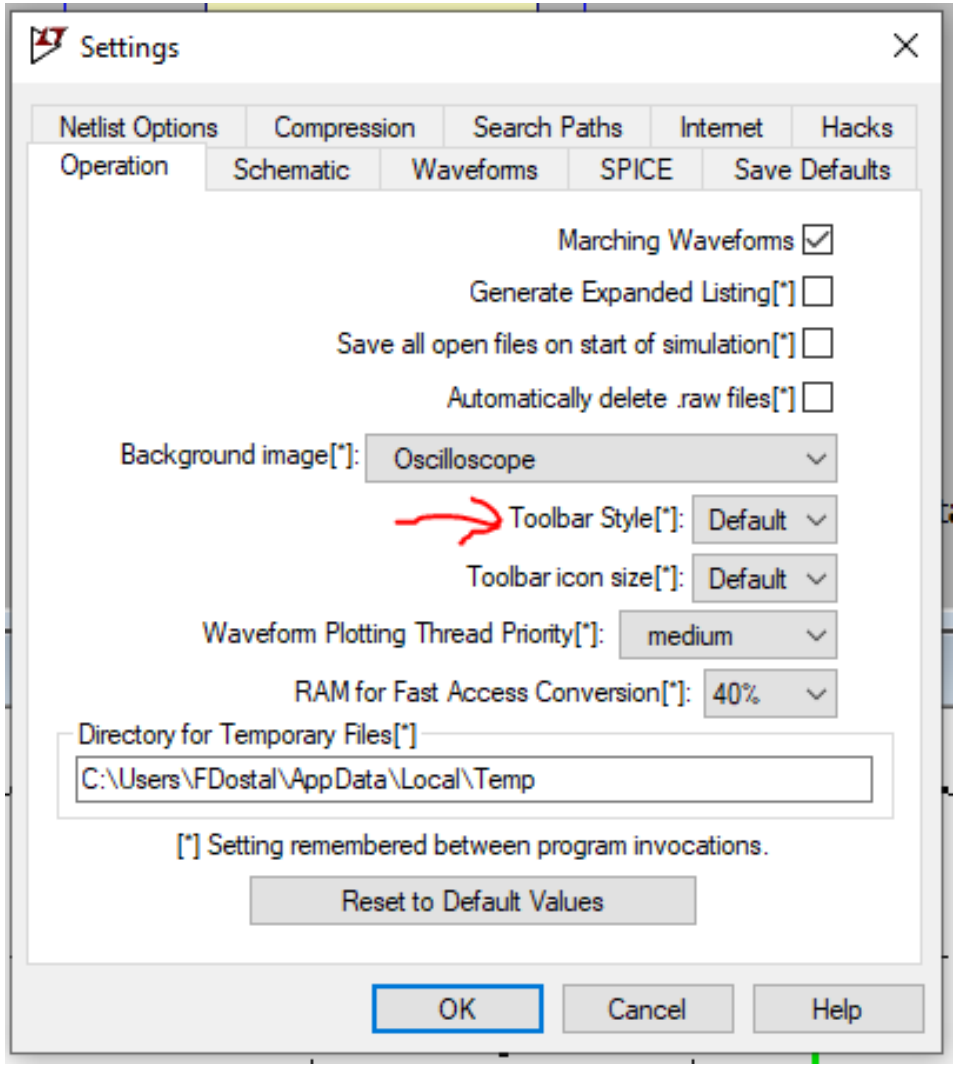
analog.com

LTspice 24 Refresh Overall Look and Feel



Revert back to classic toolbar style possible





Simulation Control

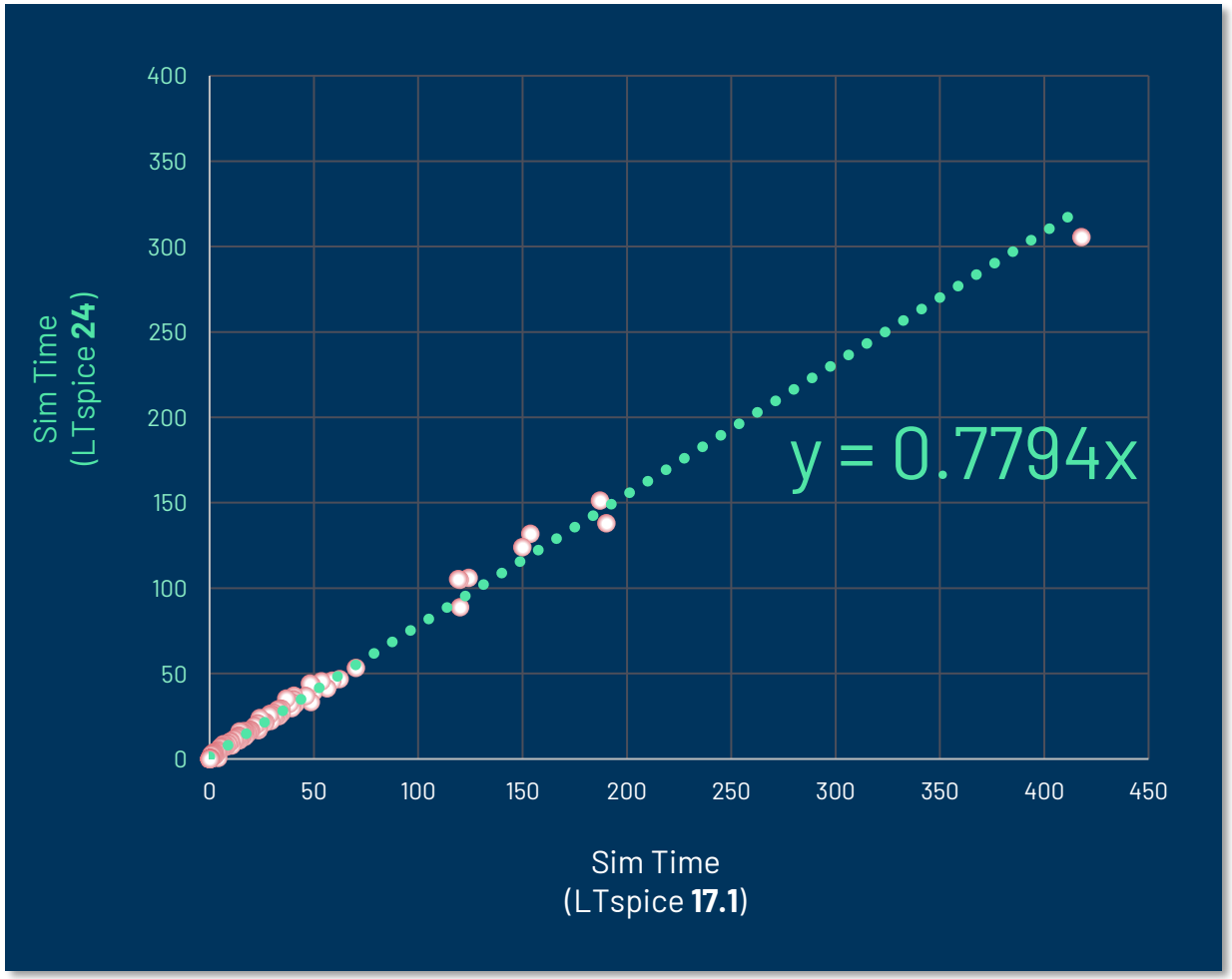
New **Configure Analysis** Toolbar Button and Shortcut ("A")

Improved Configure Analysis Dialog Functionality

- Captures all simulation commands on the schematic, *including comments*
- Populates tabs accordingly
- Automatically comment/uncomment schematic text

Shift + Left-Click toggles text between **directive** and **comment**

LTspice 24: Faster Simulations



- Improved simulation speed
  - Benchmarked ~200 popular MMP examples
  - ADI-standard Dell i7 Precision 5550 laptop
- Improved run-to-run consistency
- Changed default trtol to 2 for further improved performance

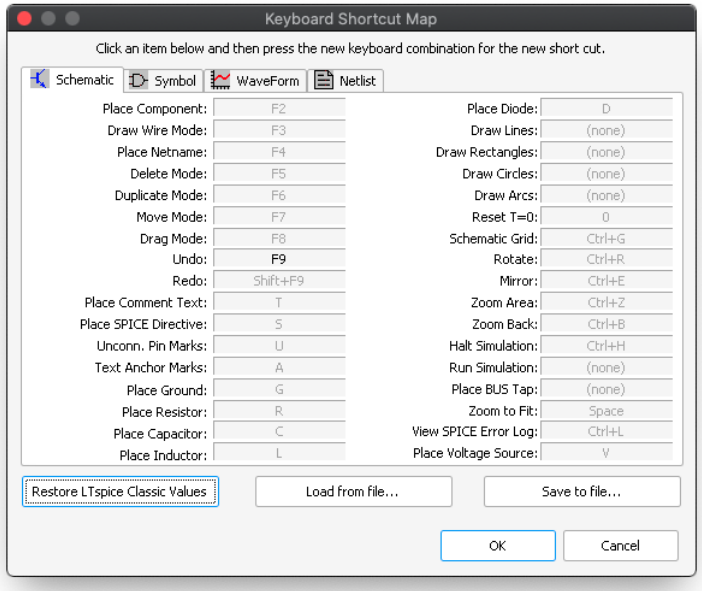
New Keyboard Shortcuts and Dynamic Cheat Sheet

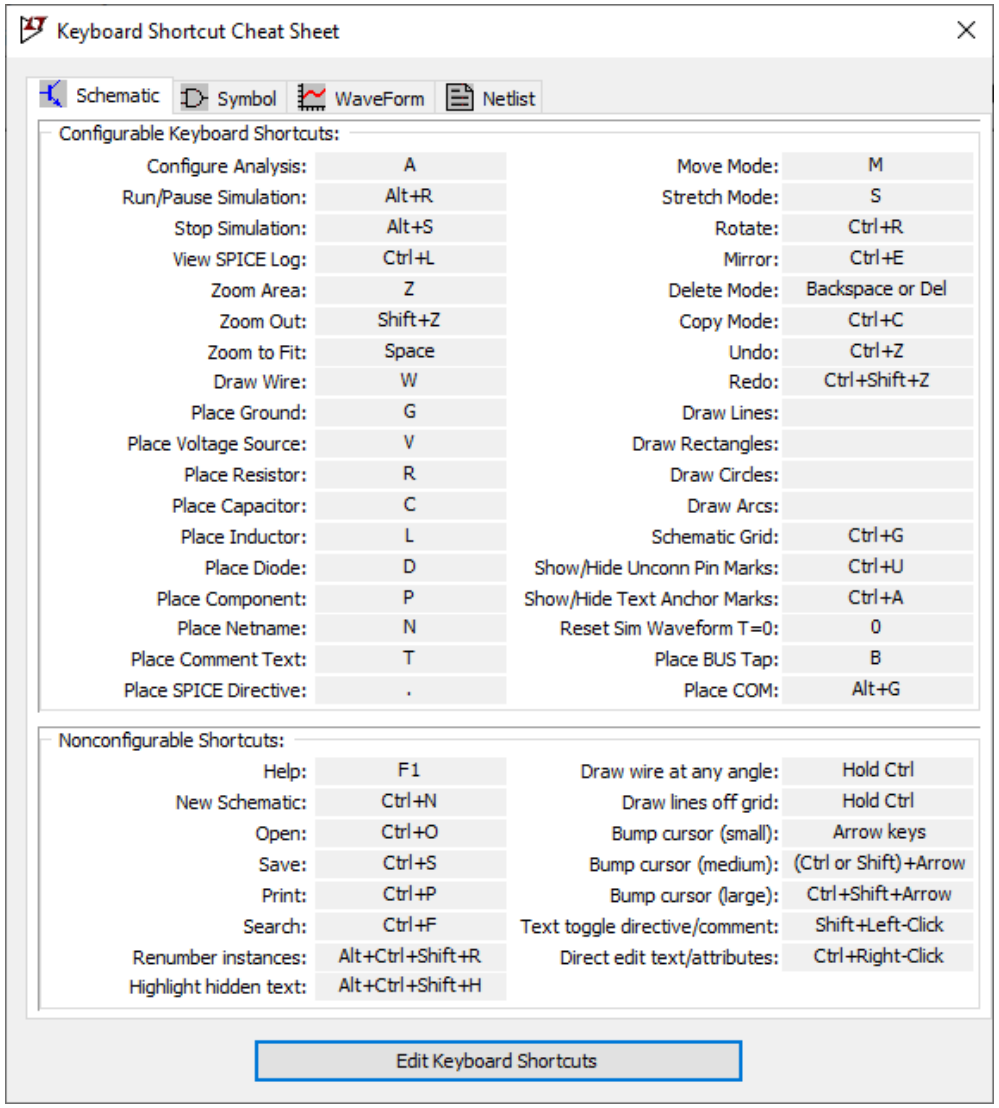
Customization-safe

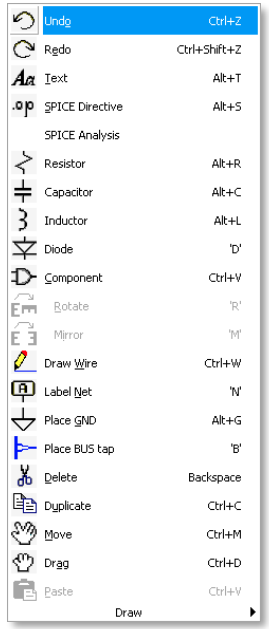
Return to old shortcuts via

Restore LTspice Classic Values

New Non-Modal, Floating Cheat Sheet Available from Help Menu







Frequency Response Analysis (FRA) Upgrades

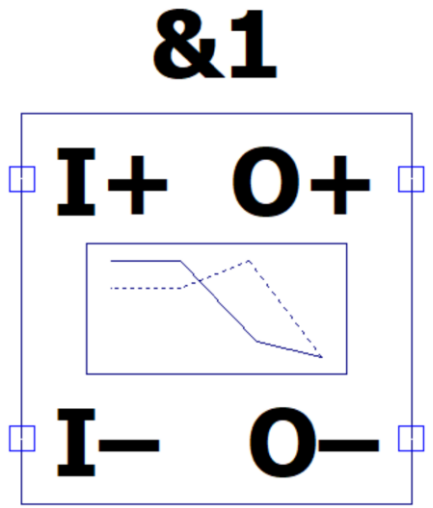
4-terminal Frequency Response Analyzer Probe

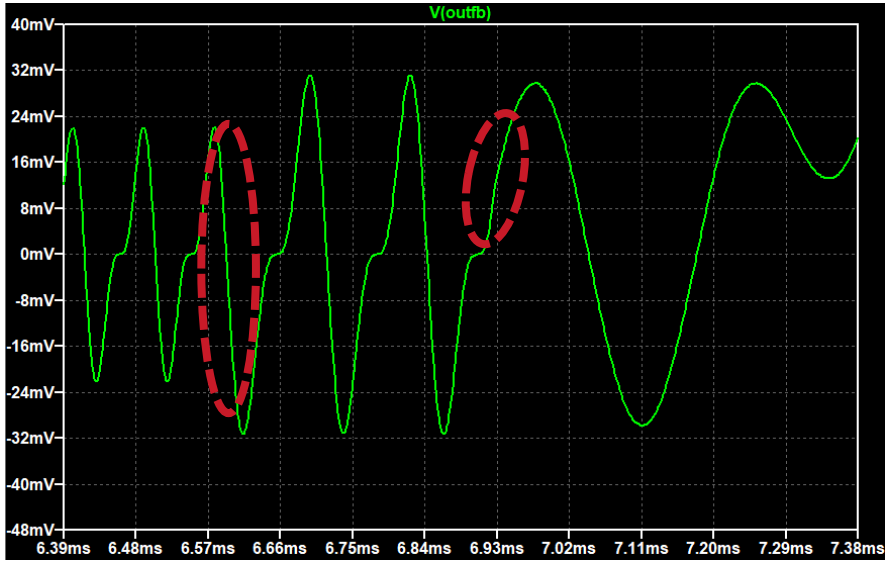
- Enables Bode plots of any part the loop
- Simplifies analysis of µModules with integrated top feedback resistors; negative outputs; and current feedback

Phase changed to represent phase margin (phase +180°)

Smooth stimuli transitions between frequencies

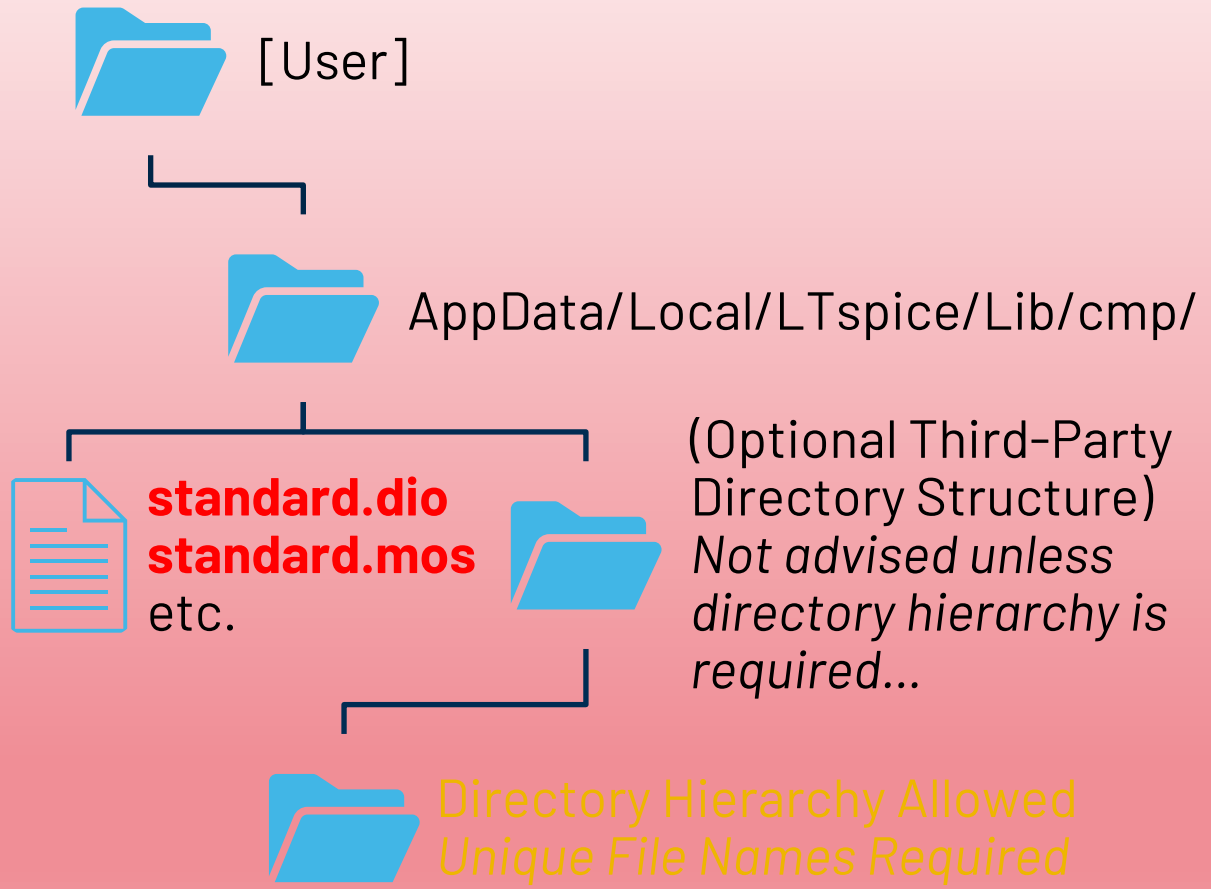
- Faster settling / improved accuracy



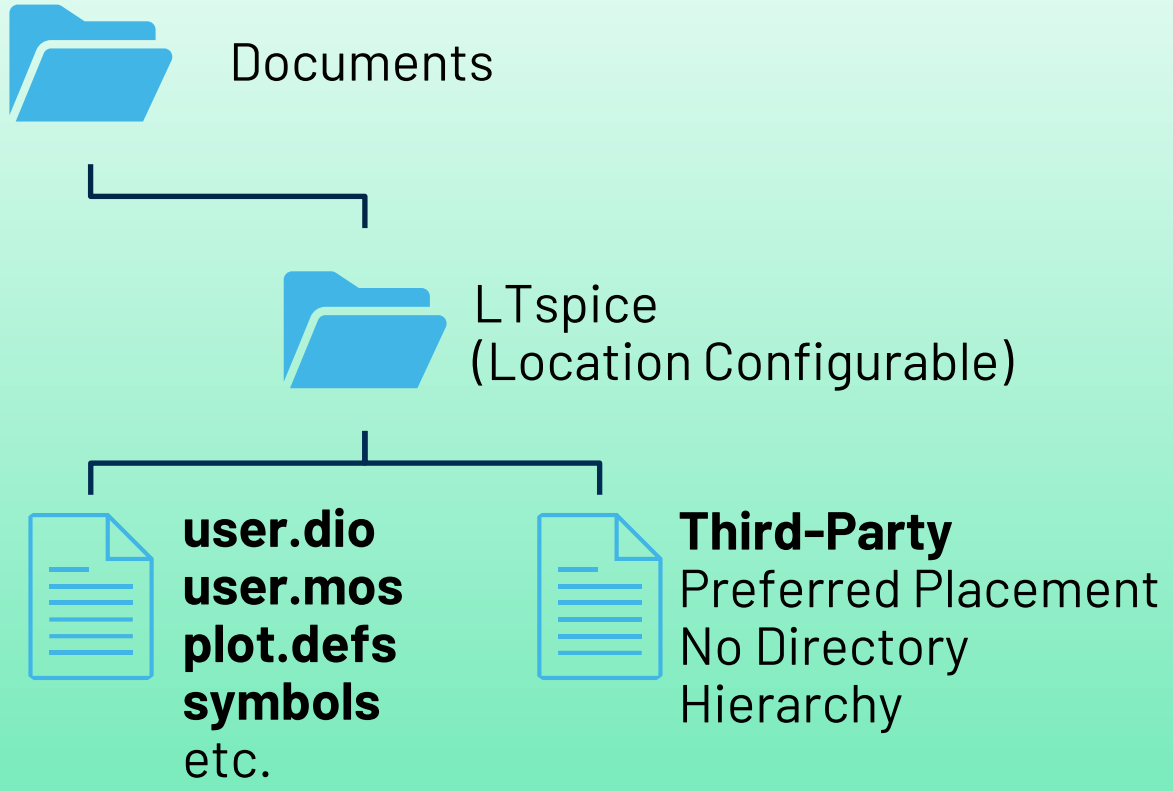


Component Libraries and AppData

LTspice Installs/Overwrites Files Here



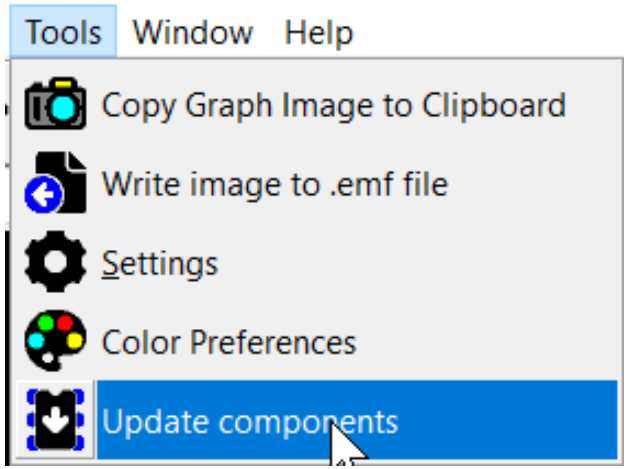
User Files Should be Placed Here



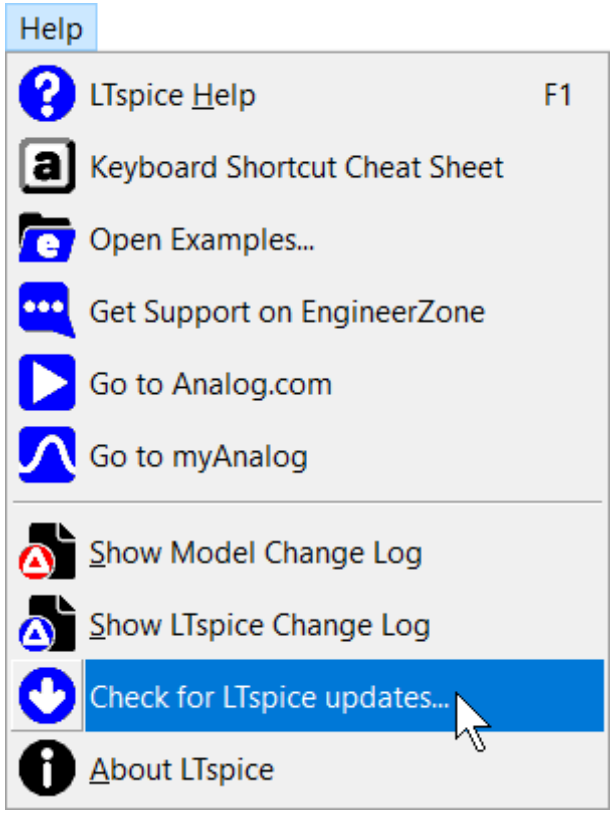
Components / Software may be separately updated

New since Ver. 24.

Update Components

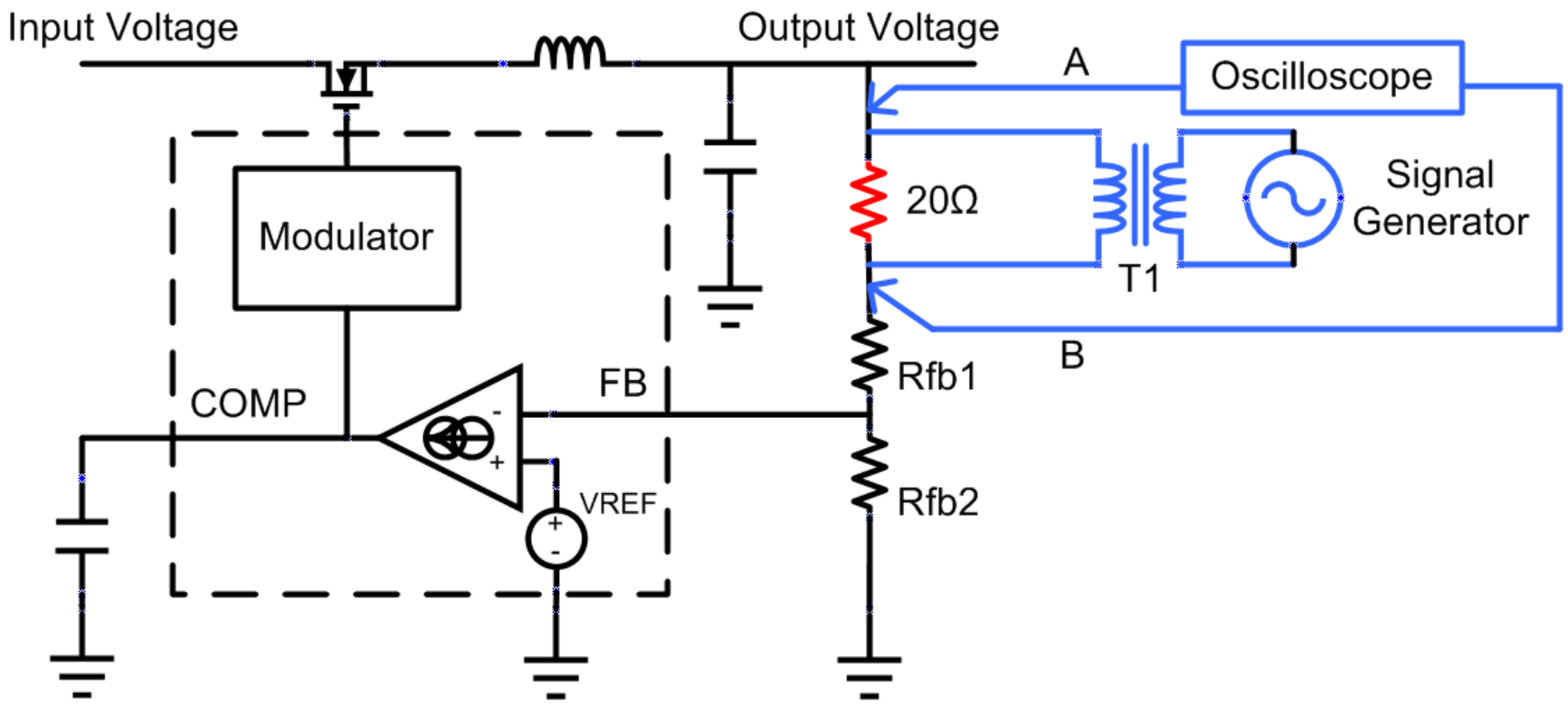


Update LTspice

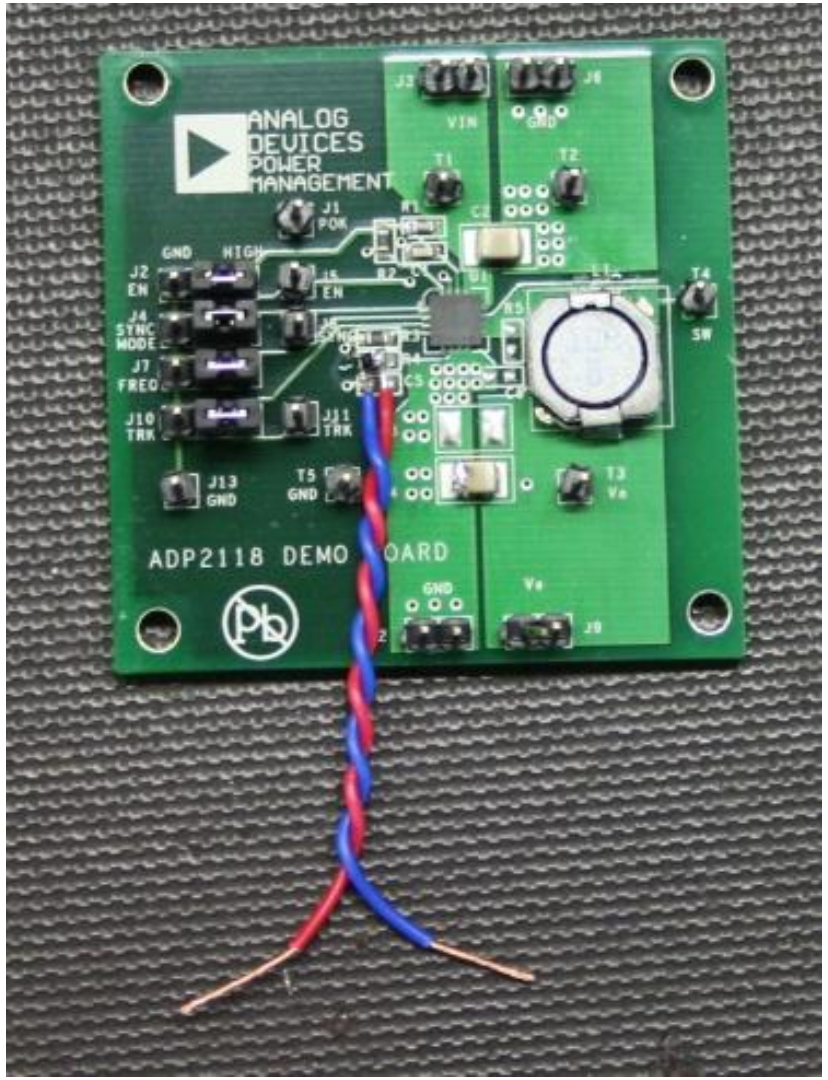


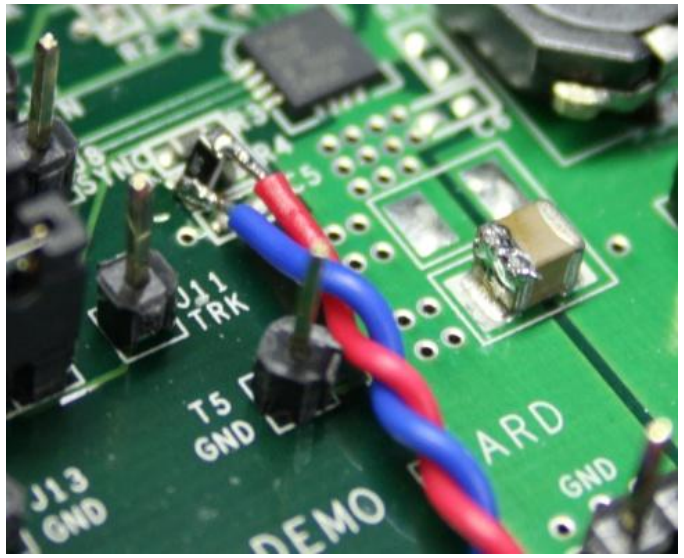
Simulating loop stability

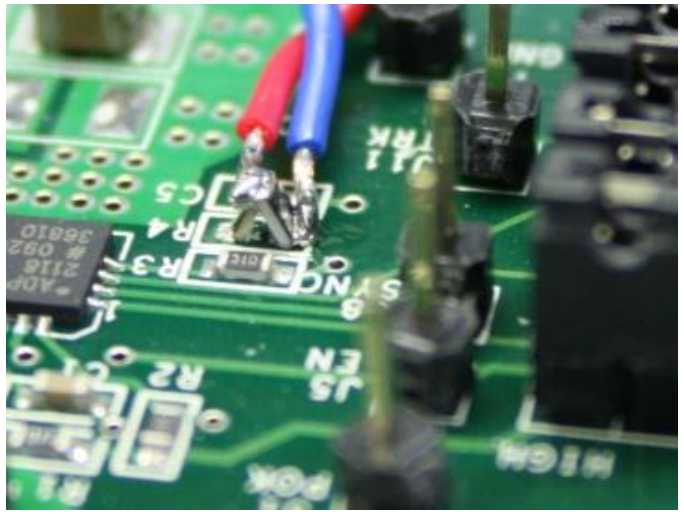
How to measure loop stability?



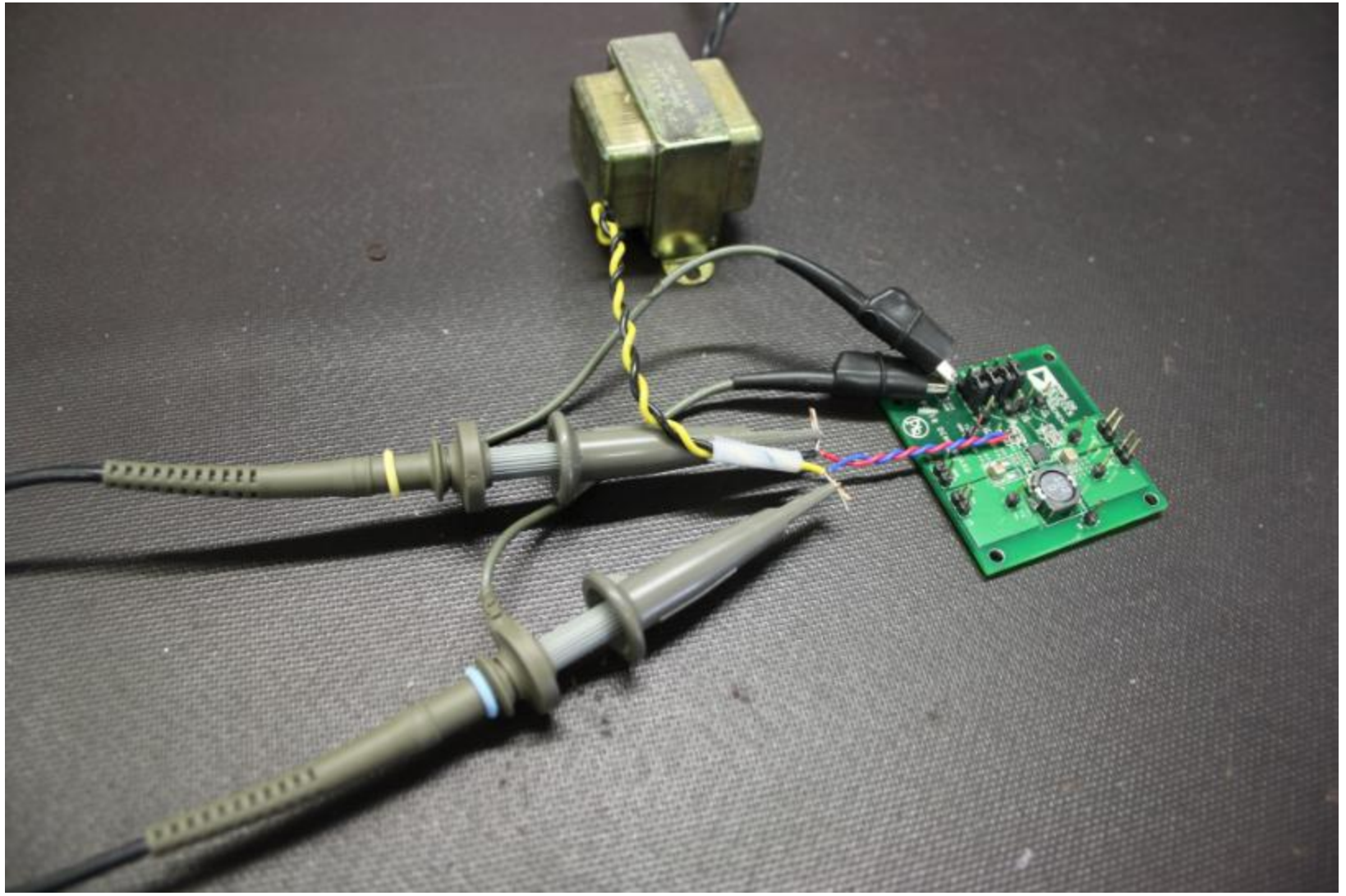
Practical Implementation



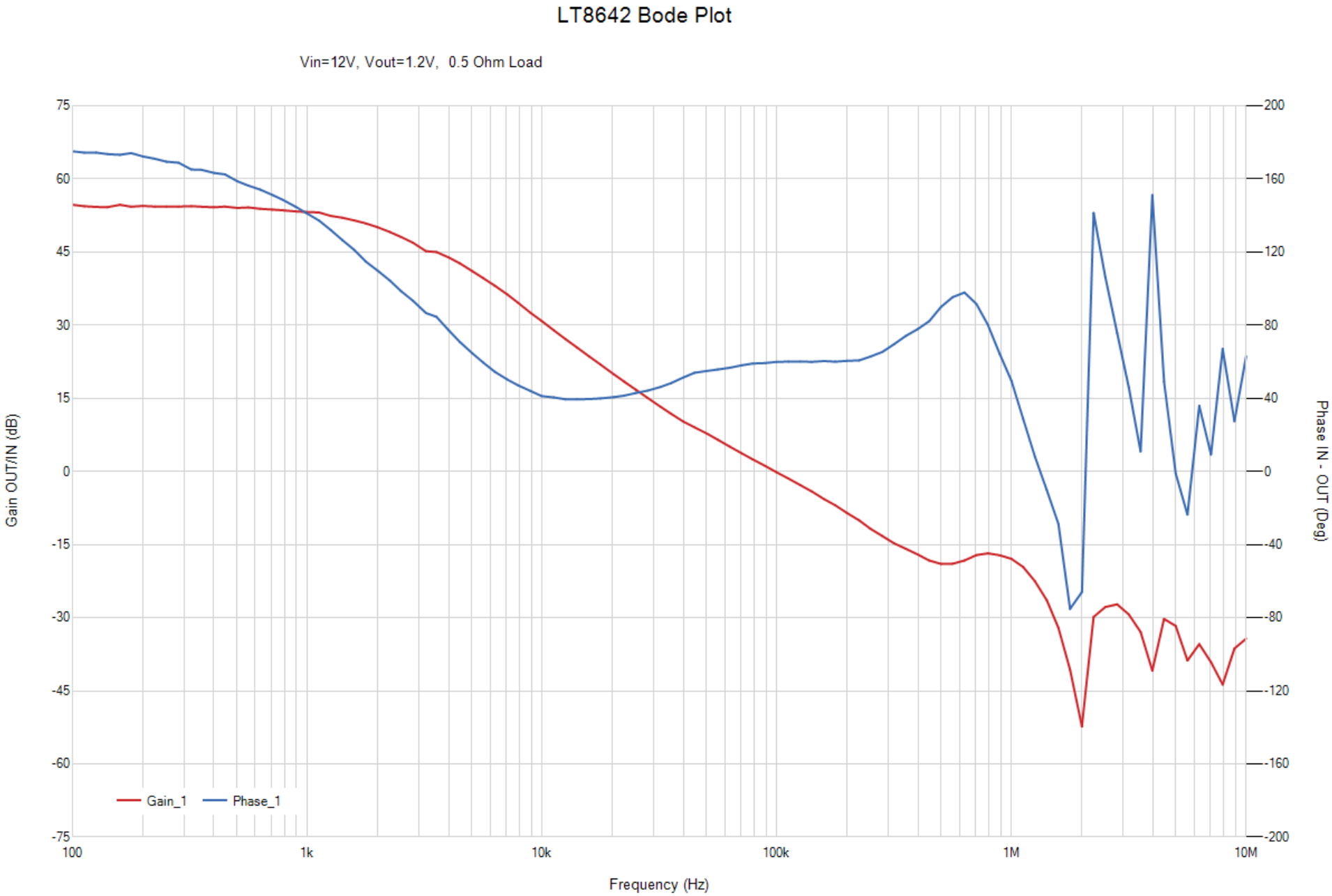




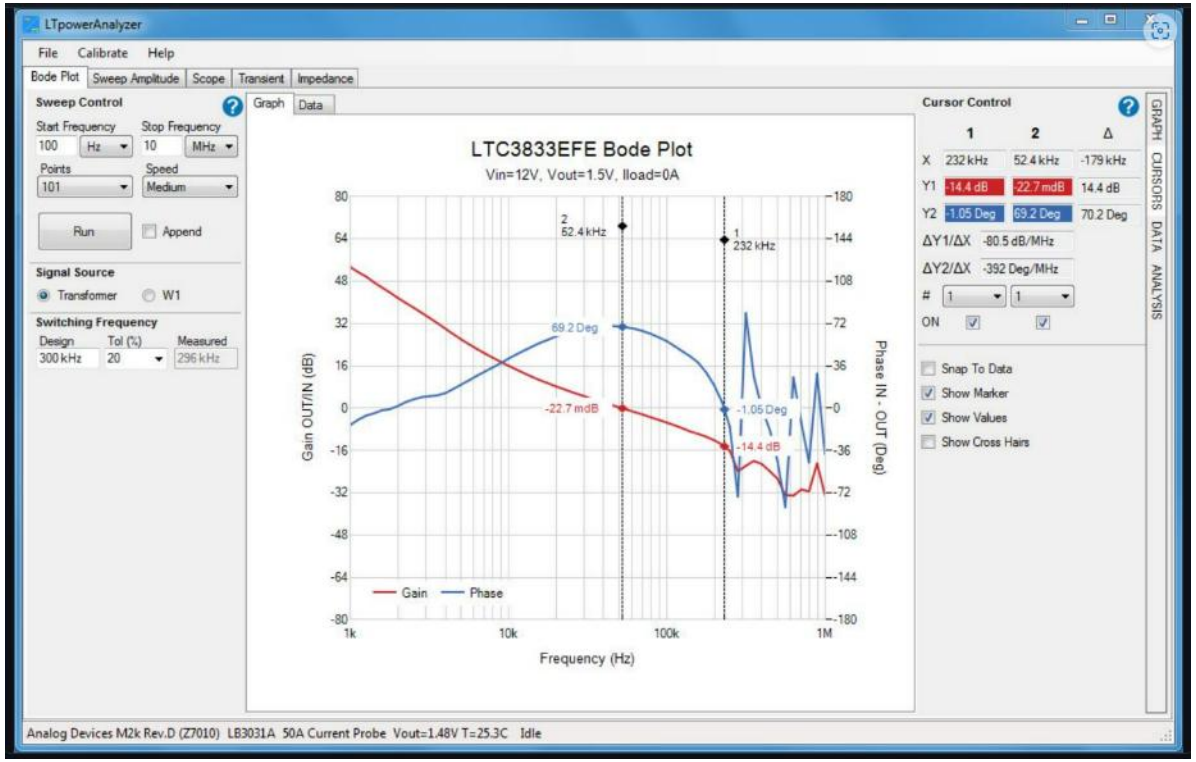
Practical Implementation



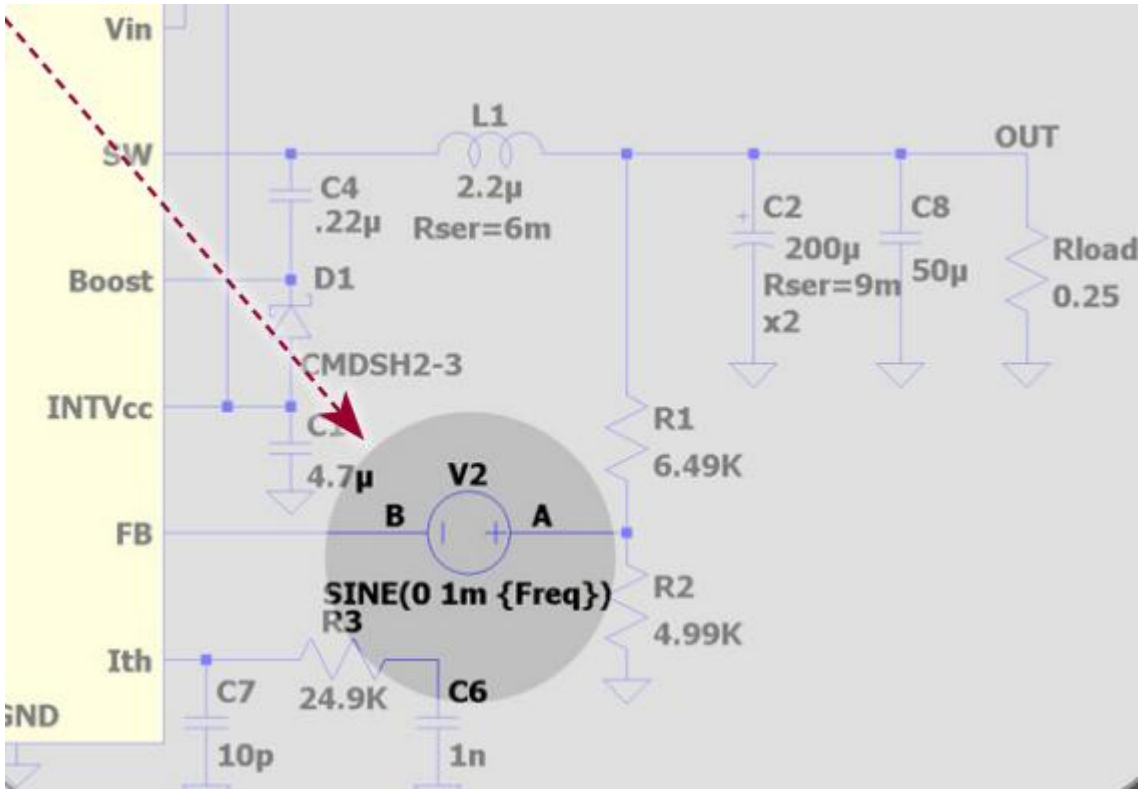
Bode Plot



LTpowerAnalyzer: Bode Plots On the Go!



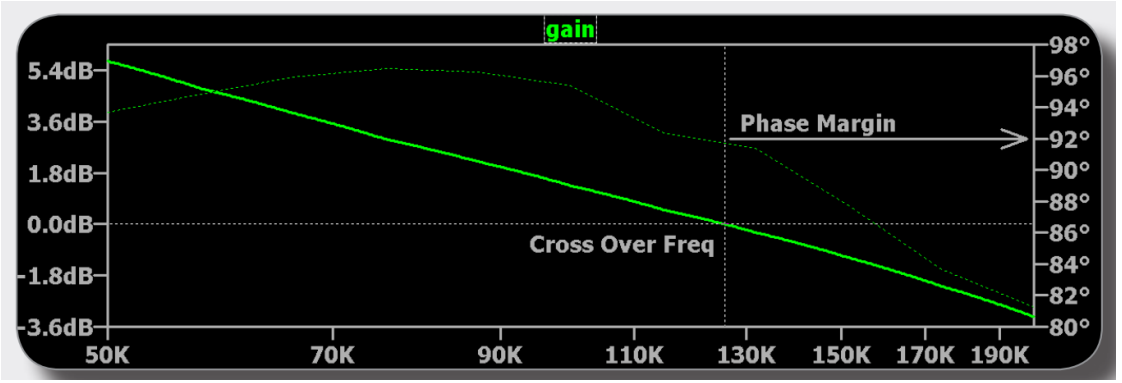
Bode Plot in old LTspice




```
.measure Aavg avg V(a)
.measure Bavg avg V(b)
.measure Are avg (V(a)-Aavg)*cos(360*time*Freq)
.measure Aim avg -(V(a)-Aavg)*sin(360*time*Freq)
.measure Bre avg (V(b)-Bavg)*cos(360*time*Freq)
.measure Bim avg -(V(b)-Bavg)*sin(360*time*Freq)
.measure GainMag param 20*log10(hypot(Are,Aim) / hypot(Bre,Bim))
.measure GainPhi param mod(atan2(Aim, Are) - atan2(Bim, Bre)+180,360)-180
```

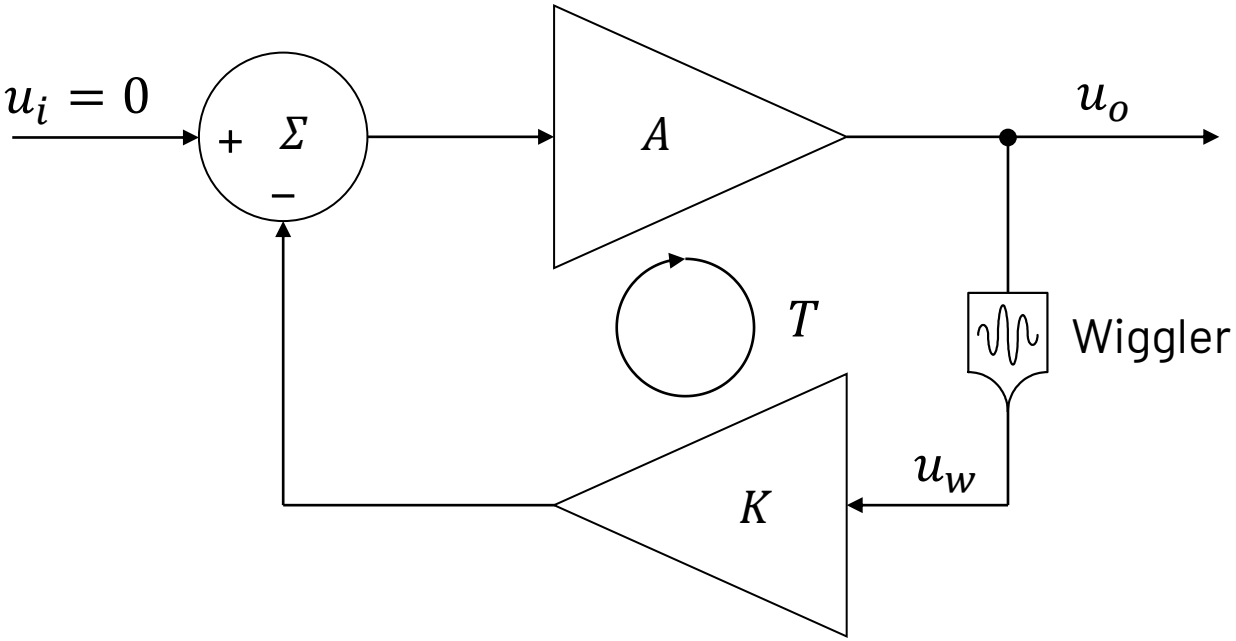
```
.param t0=.2m
.tran 0 {t0+25/freq} {t0}
```

```
.step oct param freq 5K 500K 5
.save V(a) V(b)
.option plotwinsize=0 numdgt=15
```

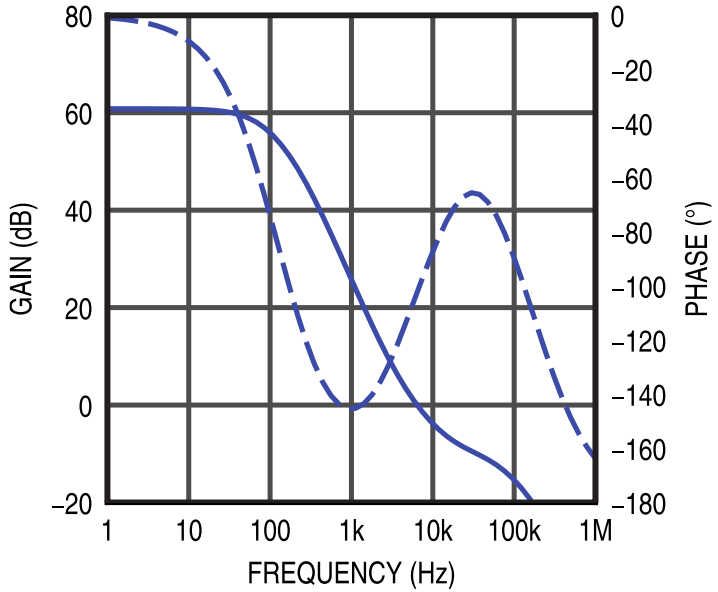


Stability Analysis, Small Signal

Power Supply: Input = Output = 0



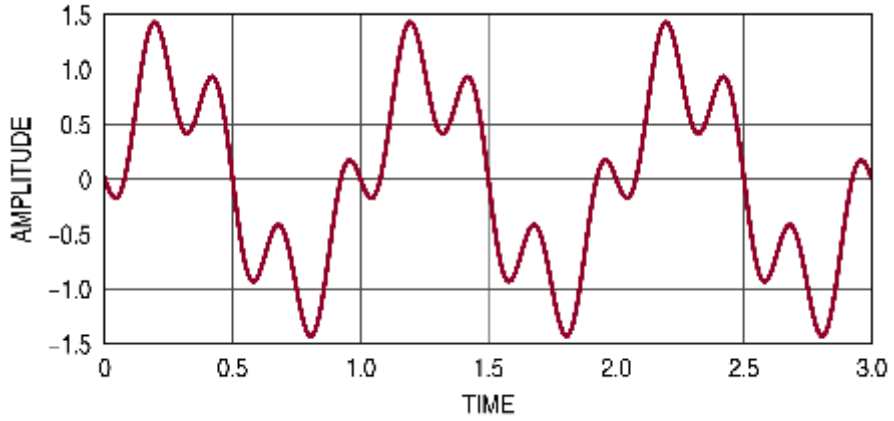
Sweep f

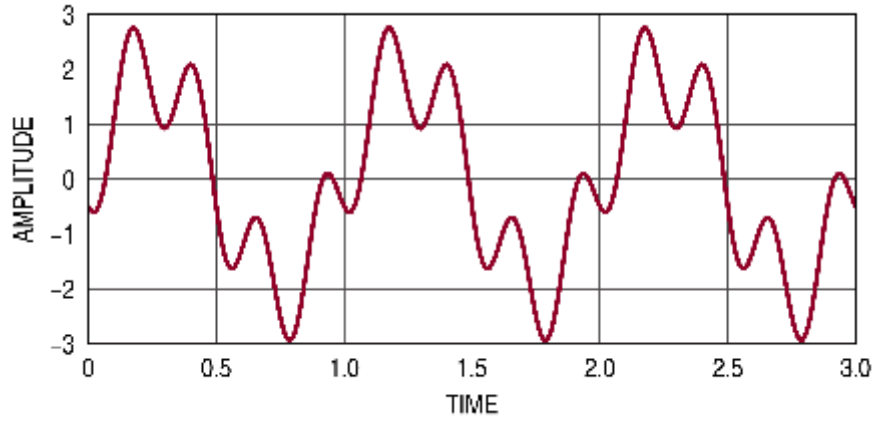


$$u_o = -Tu_w$$

Principle of Superposition

Superposition of Harmonics (Stimulus) → Linear Time-Invariant System → Superposition of Harmonics (Extraction)





$$s(t) = \sin(2\pi t) + \frac{1}{2}\sin(8\pi t + \pi)$$

Harmonics nf With $n = 2^k$ $(k \in \mathbb{N})$

Nonlinear Circuit: Keep Stimulus Sufficiently Small.

LTspice

File View Tools Help

Arrange windows so they overlap(+shift to also open iconized windows)

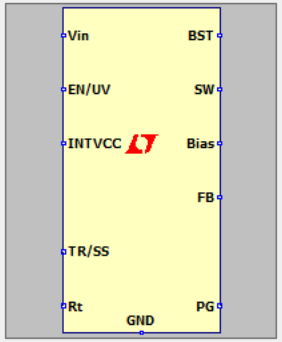
LTspice - [Draft1]

File Edit Hierarchy View Simulate Tools Window Help

Component

LT8618

High Efficiency 65V/100mA Synchronous Buck



Get LT8618 Info

Open Example Circuit

Top Directory:

C:\Users\FDostal\AppData\Local\LTspice\lib\sym

Search: lt8618

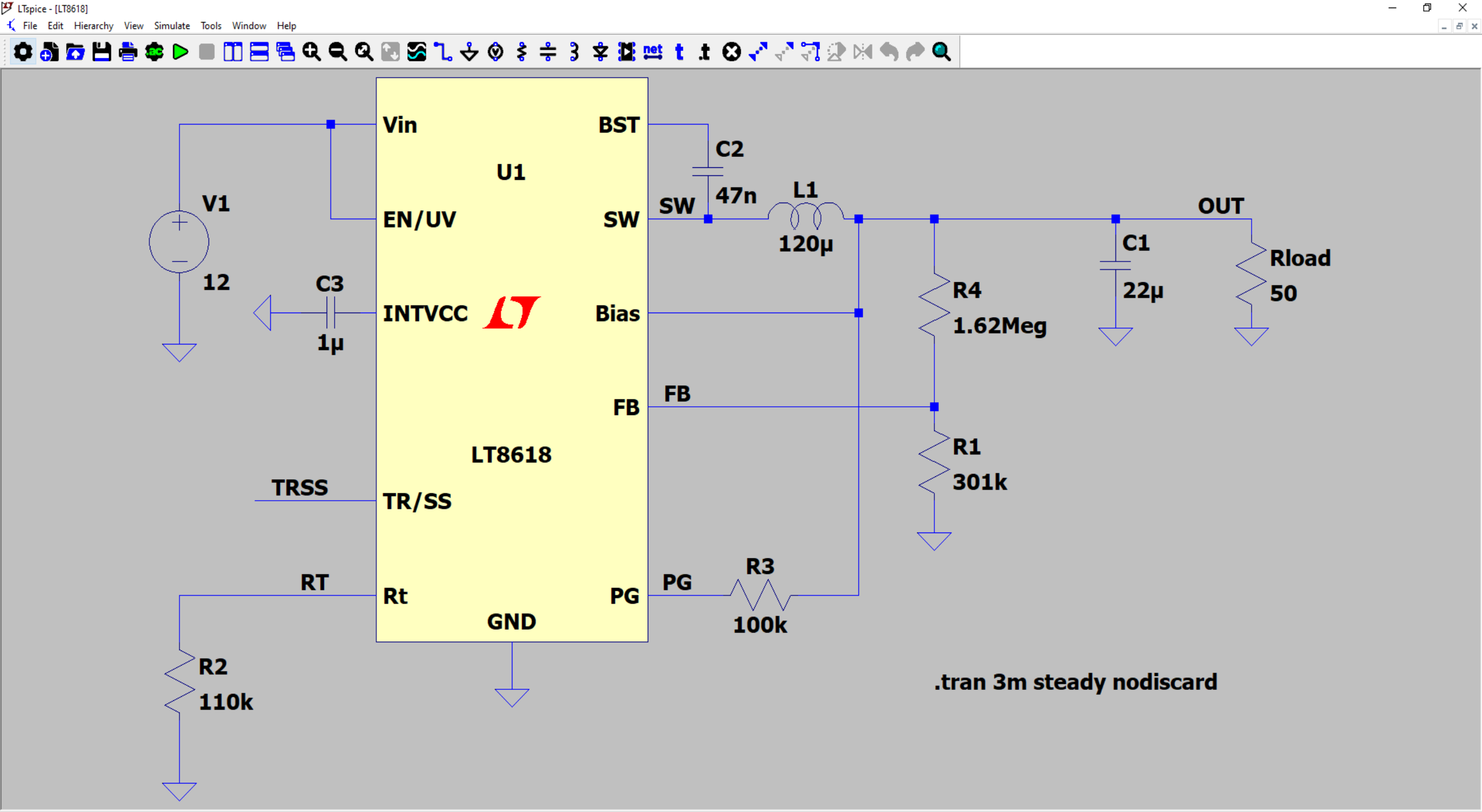
Go to analog.com

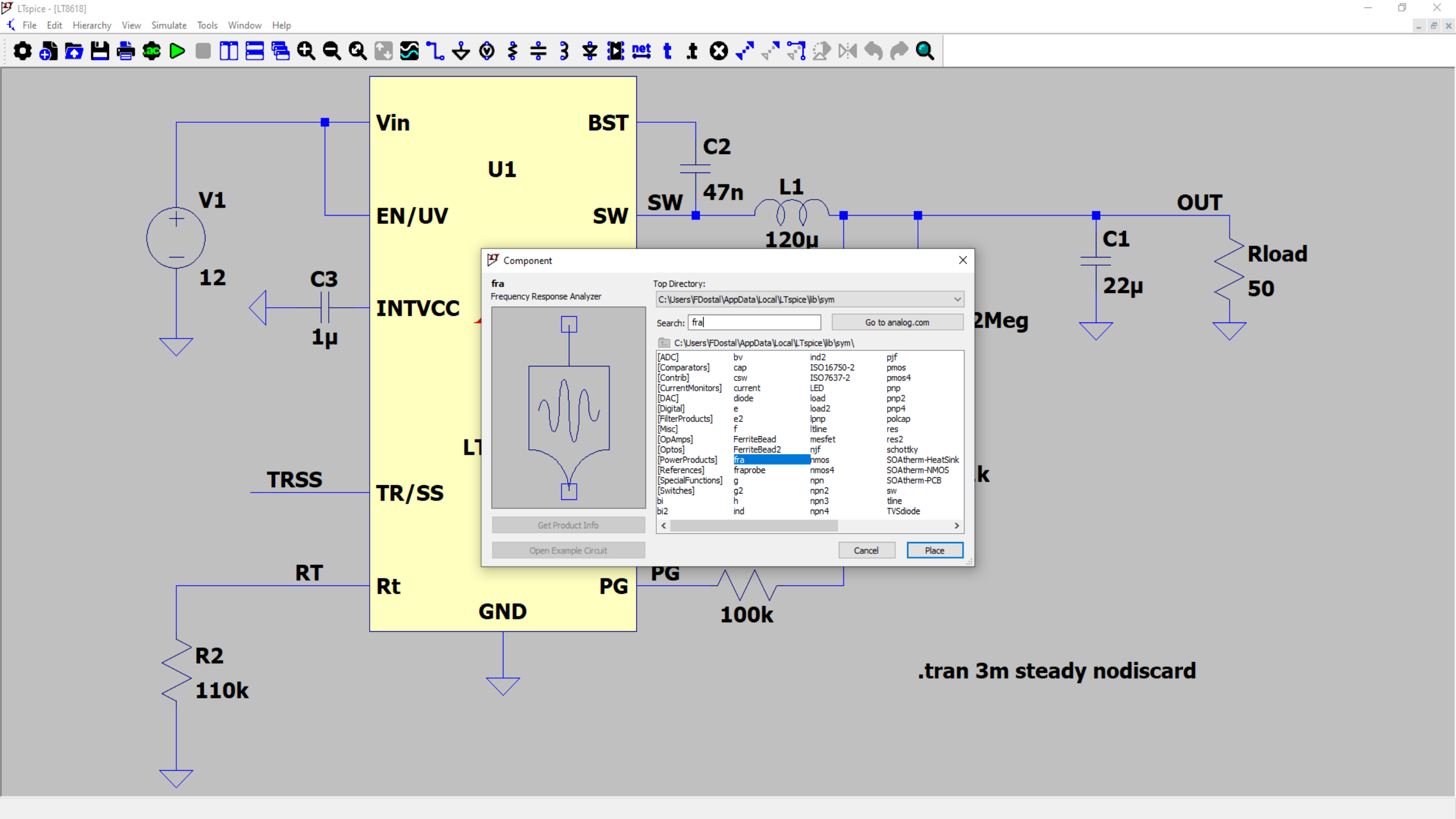
C:\Users\FDostal\AppData\Local\LTspice\lib\sym\PowerProducts\

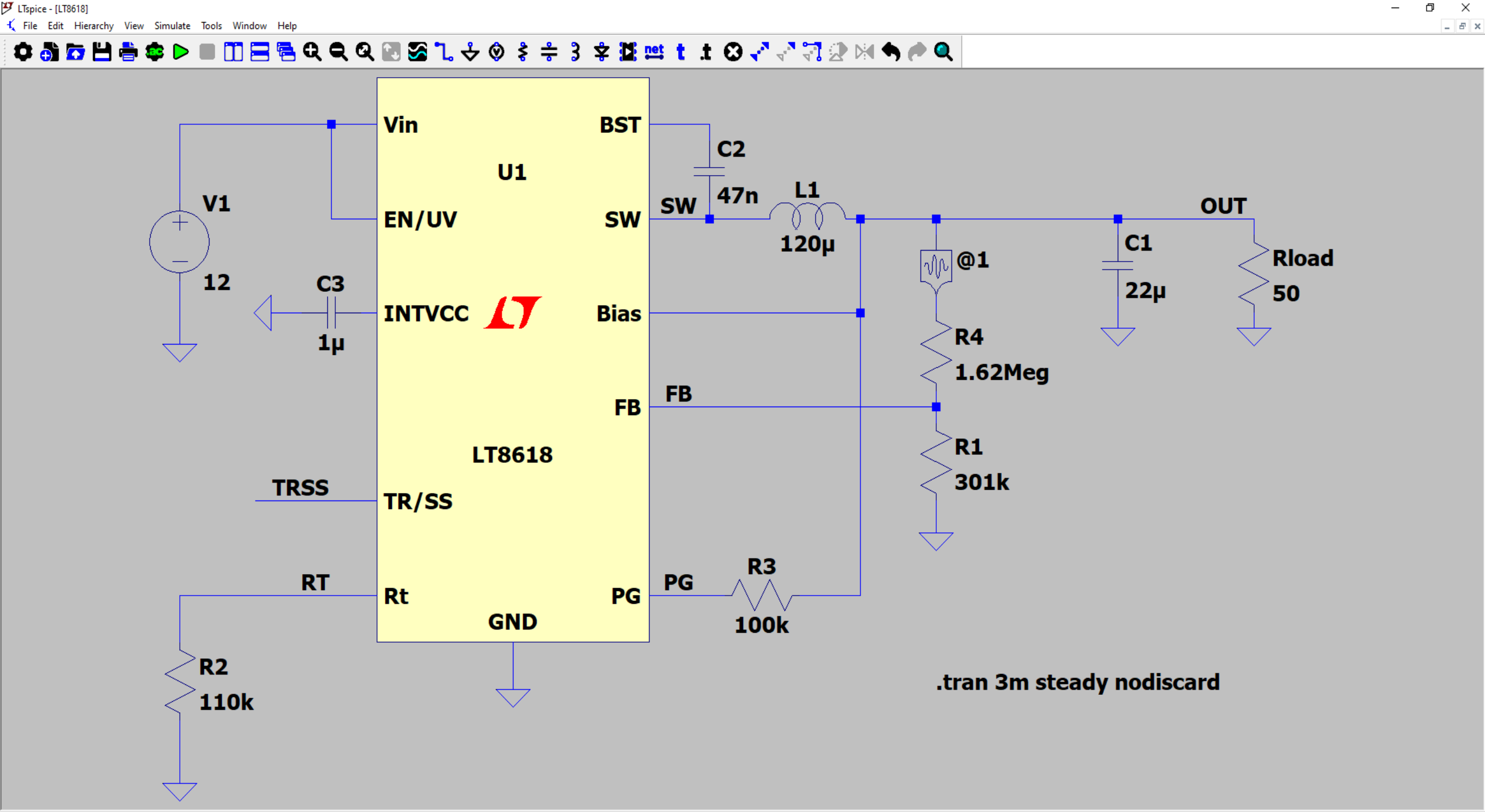
LT8361	LT8410-1	LT8604	LT8613
LT8362	LT8415	LT8604C	LT8614
LT8364	LT8418	LT8606	LT8616
LT8365	LT8471	LT8607	LT8618
LT8374	LT8494	LT8608	LT8618-3.3
LT8374-1	LT8495	LT8608S	LT8618C
LT8376	LT8550	LT8609	LT8619
LT8386	LT8551	LT8609A	LT8619-5
LT8390	LT8570	LT8609B	LT8620
LT8390A	LT8570-1	LT8609S	LT8630
LT8391	LT8580	LT8610	LT8631
LT8391A	LT8582	LT8610A	LT8636
LT8391D	LT8584	LT8610AB	LT8637
LT8392	LT8601	LT8610AC	LT8638S
LT8393	LT8602	LT8611	LT8640
LT8410	LT8603	LT8612	LT8640-1

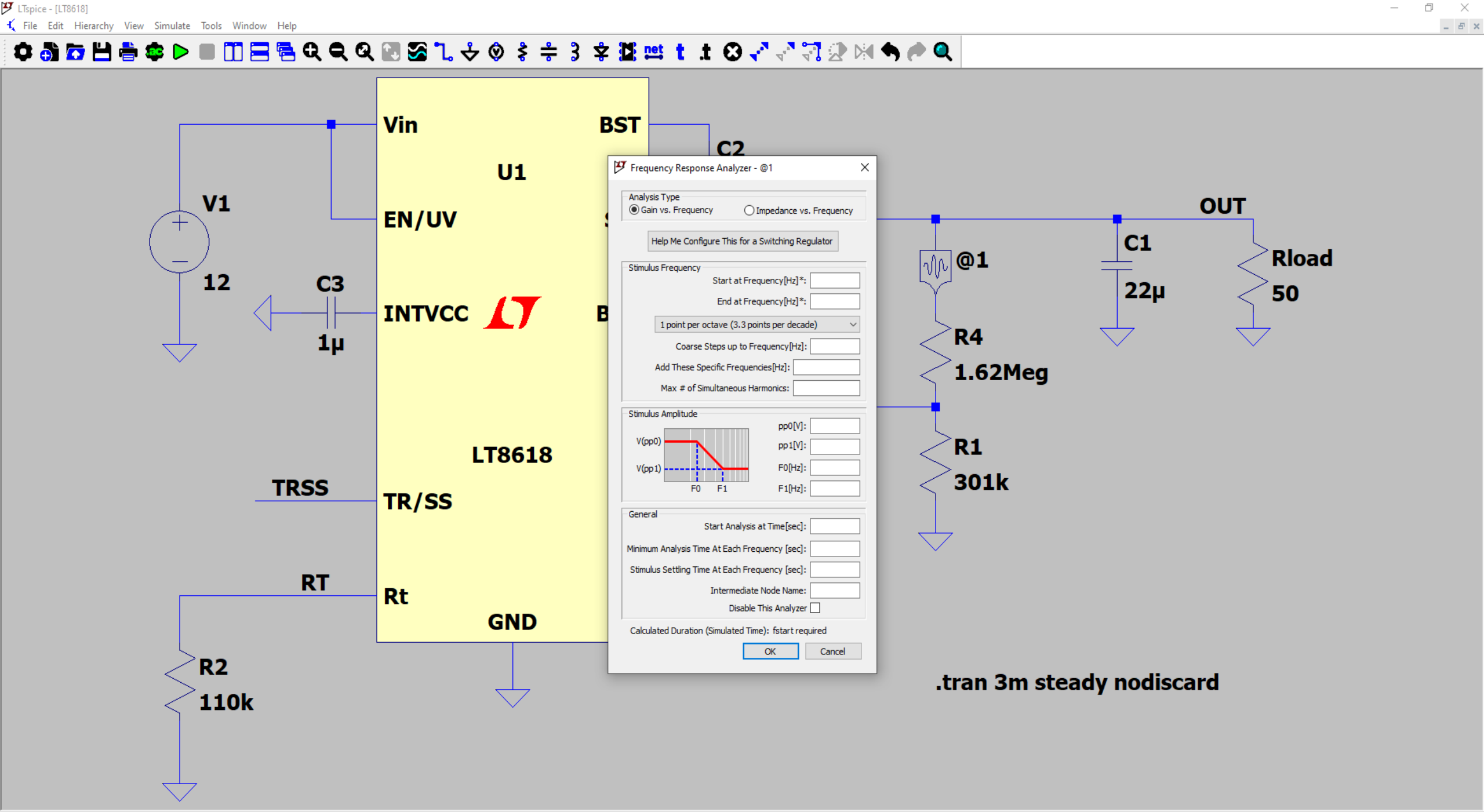
Cancel

Place

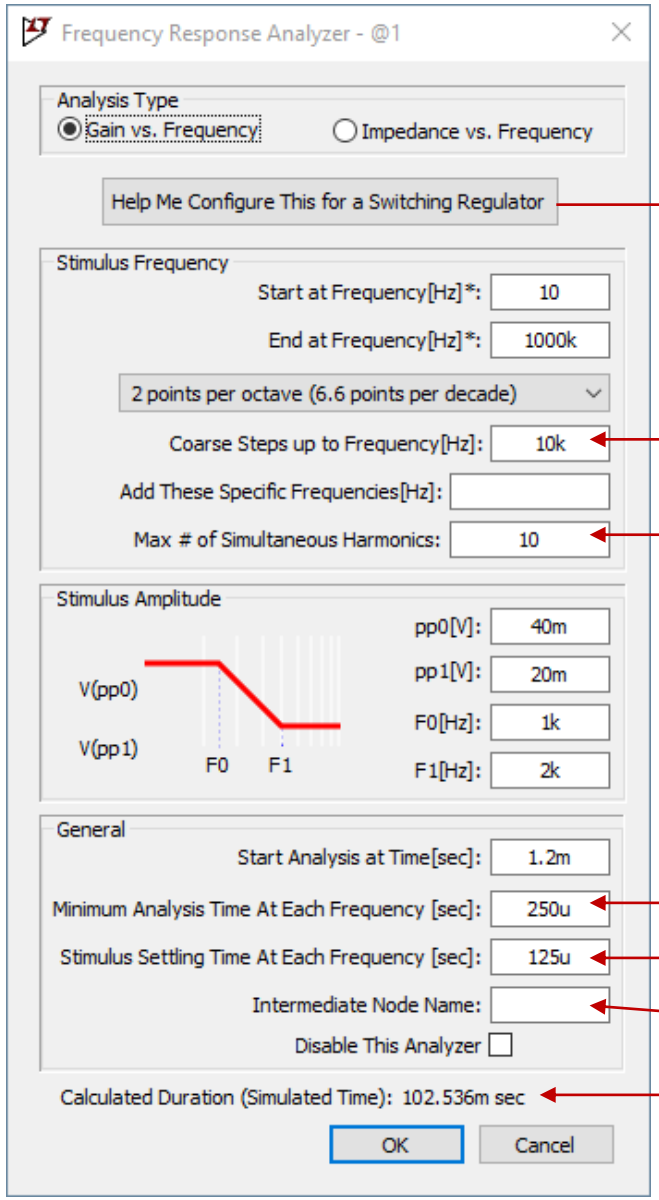

LTspice - [LT8618]
File Edit Hierarchy View Simulate Tools Window Help
Vin
BST
U1
EN/UV
SW
INTVCC
Bias
FB
LT8618
TR/SS
Rt
PG
GND
V1
12
C3
1µ
C2
47n
SW
L1
120µ
OUT
C1
22µ
Rload
50
R4
1.62Meg
R1
301k
FB
TRSS
RT
R2
110k
PG
R3
100k
.tran 3m steady nodiscard

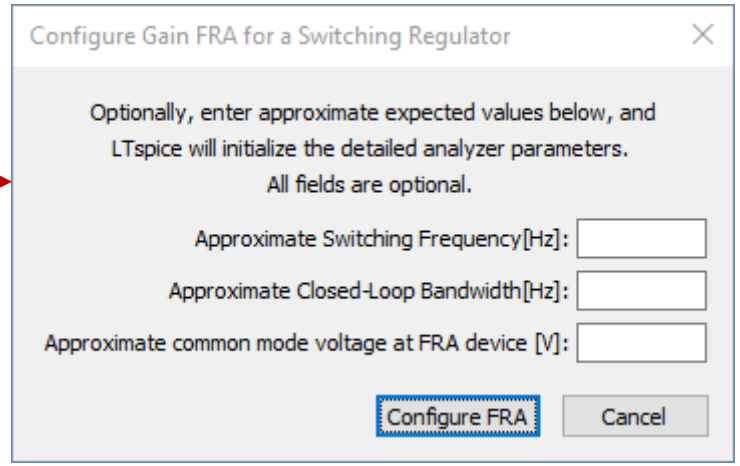

LTspice - [LT8618]
File Edit Hierarchy View Simulate Tools Window Help
Vin
BST
U1
EN/UV
SW
INTVCC
TRSS
TR/SS
RT
Rt
PG
GND
V1
12
C3
1µ
C2
47n
SW
L1
120µ
OUT
C1
22µ
Rload
50
2Meg
k
PG
100k
R2
110k
.tran 3m steady nodiscard
Component
fra
Frequency Response Analyzer
Top Directory:
C:\Users\FDostal\AppData\Local\LTspice\lib\sym
Search: fra
Go to analog.com
C:\Users\FDostal\AppData\Local\LTspice\lib\sym\
[ADC] [Comparators] [Contrib] [CurrentMonitors] [DAC] [Digital] [FilterProducts] [Misc] [OpAmps] [Optos] [PowerProducts] [References] [SpecialFunctions] [Switches]
bv cap csw current diode e e2 f FerriteBead FerriteBead2 fra fraprobe g g2 h ind
ind2 ISO16750-2 ISO7637-2 LED load load2 lpnp ltline mesfet njf nmos nmos4 npn npn2 npn3 npn4
pjf pmos pmos4 pnp pnp2 pnp4 polcap res res2 schottky SOAtherm-HeatSink SOAtherm-NMOS SOAtherm-PCB sw tline TVSdiode
bi bi2
Get Product Info
Open Example Circuit
Cancel
Place


LTspice - [LT8618]
File Edit Hierarchy View Simulate Tools Window Help
Vin
BST
U1
EN/UV
SW
INTVCC
Bias
FB
LT8618
TR/SS
Rt
PG
GND
V1
12
C3
1µ
C2
47n
SW
L1
120µ
OUT
@1
C1
22µ
Rload
50
R4
1.62Meg
FB
R1
301k
TRSS
RT
R2
110k
PG
R3
100k
.tran 3m steady nodiscard


LTspice - [LT8618]
File Edit Hierarchy View Simulate Tools Window Help
Vin
BST
U1
EN/UV
INTVCC
LT8618
TRSS
TR/SS
RT
Rt
GND
V1
12
C3
1µ
C2
@1
R4
1.62Meg
R1
301k
C1
22µ
OUT
Rload
50
R2
110k
.tran 3m steady nodiscard
Frequency Response Analyzer - @1
Analysis Type
Gain vs. Frequency
Impedance vs. Frequency
Help Me Configure This for a Switching Regulator
Stimulus Frequency
Start at Frequency[Hz]*:
End at Frequency[Hz]*:
1 point per octave (3.3 points per decade)
Coarse Steps up to Frequency[Hz]:
Add These Specific Frequencies[Hz]:
Max # of Simultaneous Harmonics:
Stimulus Amplitude
V(pp0)
V(pp1)
F0
F1
pp0[V]:
pp1[V]:
F0[Hz]:
F1[Hz]:
General
Start Analysis at Time[sec]:
Minimum Analysis Time At Each Frequency [sec]:
Stimulus Settling Time At Each Frequency [sec]:
Intermediate Node Name:
Disable This Analyzer
Calculated Duration (Simulated Time): fstart required
OK
Cancel
Editing component: @1

Settings





1 Point/Oct Below This Freq

Multiple Freqs at Once

Averaging

Settling

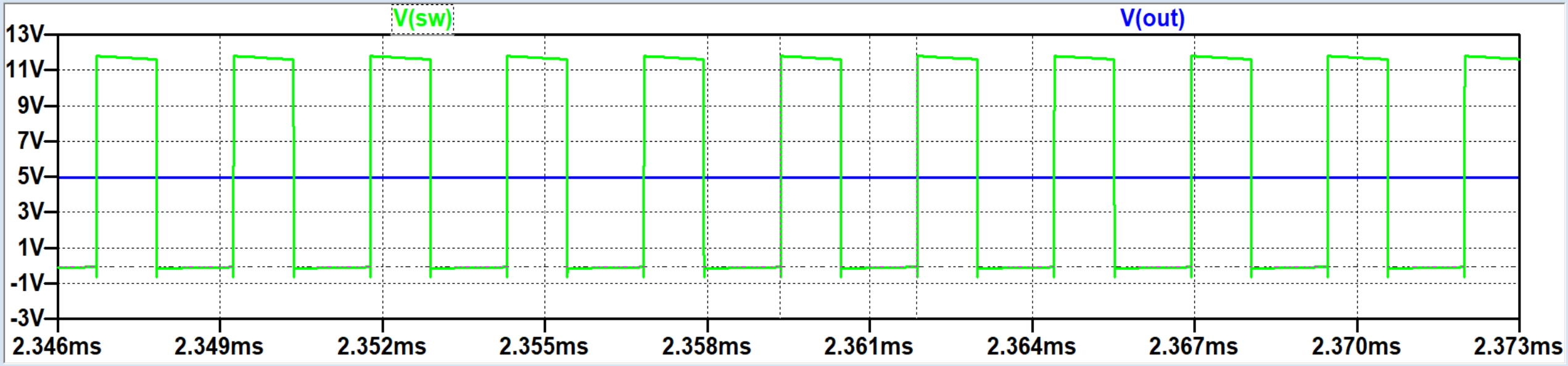
Required Simulated Time

LTspice - LT8618

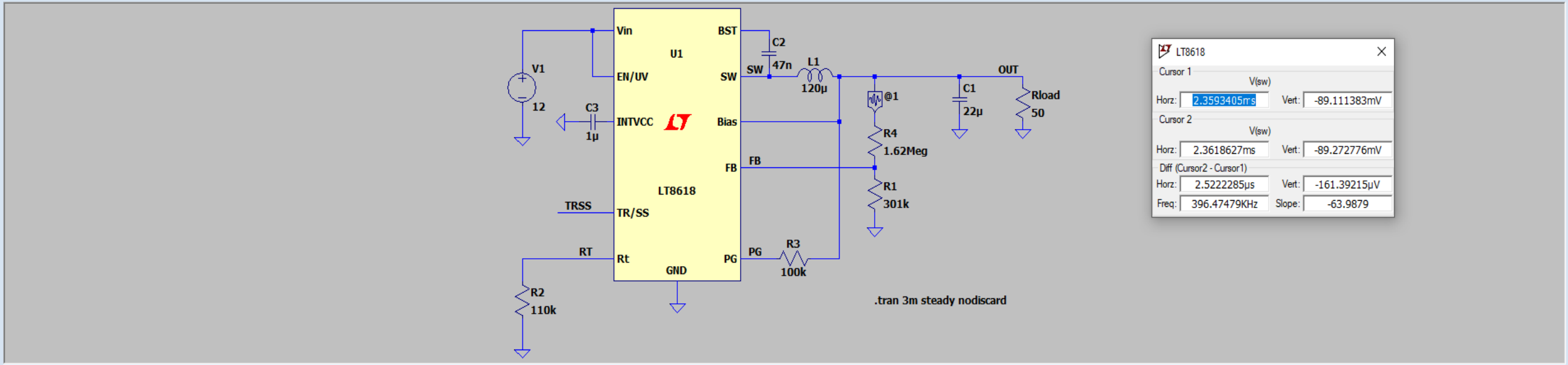
File View Plot Settings Simulation Tools Window Help

LT8618 LT8618

LT8618

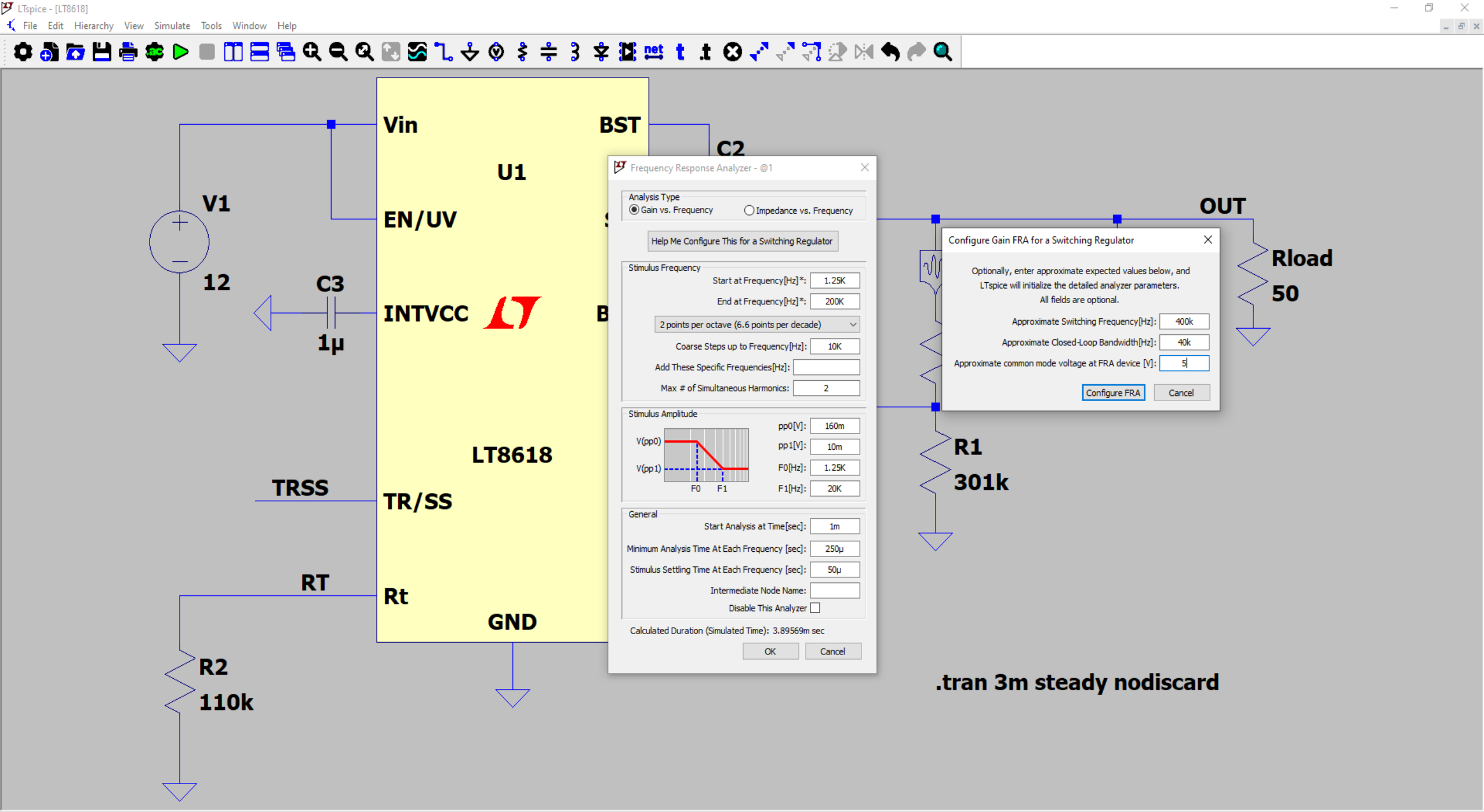


LT8618



LT8618

Cursor 1
V(sw)
Horz: 2.3593405ms Vert: -89.111383mV
Cursor 2
V(sw)
Horz: 2.3618627ms Vert: -89.272776mV
Diff (Cursor2 - Cursor1)
Horz: 2.5222285µs Vert: -161.39215µV
Freq: 396.47479KHz Slope: -63.9879

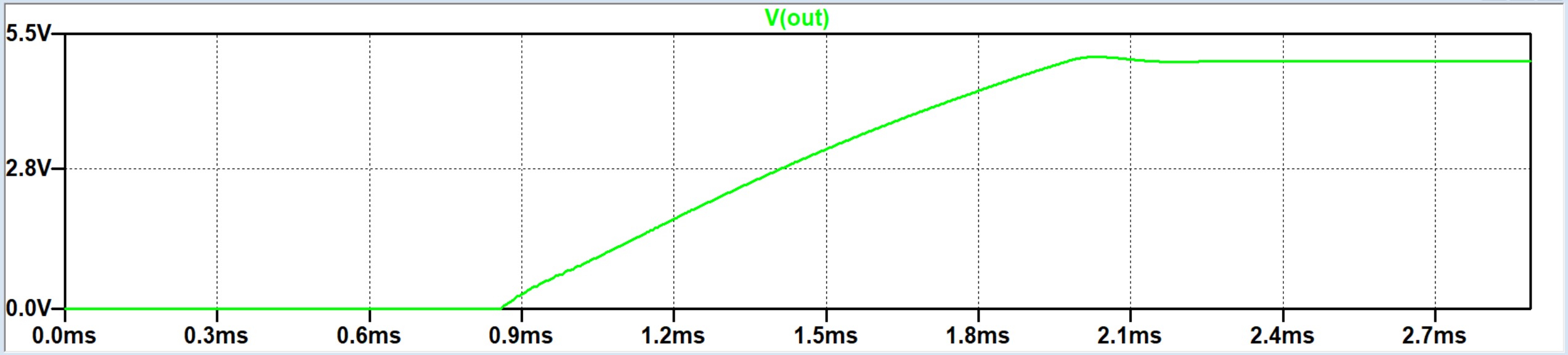

LTspice - [LT8618]
File Edit Hierarchy View Simulate Tools Window Help
Vin
BST
U1
C2
V1
12
EN/UV
C3
1µ
INTVCC
LT8618
TRSS
TR/SS
RT
Rt
GND
R2
110k
OUT
Rload
50
R1
301k
.tran 3m steady nodiscard
Frequency Response Analyzer - @1
Analysis Type
Gain vs. Frequency
Impedance vs. Frequency
Help Me Configure This for a Switching Regulator
Stimulus Frequency
Start at Frequency[Hz]*: 1.25K
End at Frequency[Hz]*: 200K
2 points per octave (6.6 points per decade)
Coarse Steps up to Frequency[Hz]: 10K
Add These Specific Frequencies[Hz]:
Max # of Simultaneous Harmonics: 2
Stimulus Amplitude
V(pp0)
V(pp1)
F0
F1
pp0[V]: 160m
pp1[V]: 10m
F0[Hz]: 1.25K
F1[Hz]: 20K
General
Start Analysis at Time[sec]: 1m
Minimum Analysis Time At Each Frequency [sec]: 250µ
Stimulus Settling Time At Each Frequency [sec]: 50µ
Intermediate Node Name:
Disable This Analyzer
Calculated Duration (Simulated Time): 3.89569m sec
OK
Cancel
Configure Gain FRA for a Switching Regulator
Optionally, enter approximate expected values below, and
LTspice will initialize the detailed analyzer parameters.
All fields are optional.
Approximate Switching Frequency[Hz]: 400k
Approximate Closed-Loop Bandwidth[Hz]: 40k
Approximate common mode voltage at FRA device [V]: 5
Configure FRA
Cancel
Editing component: @1

LTspice - LT8618

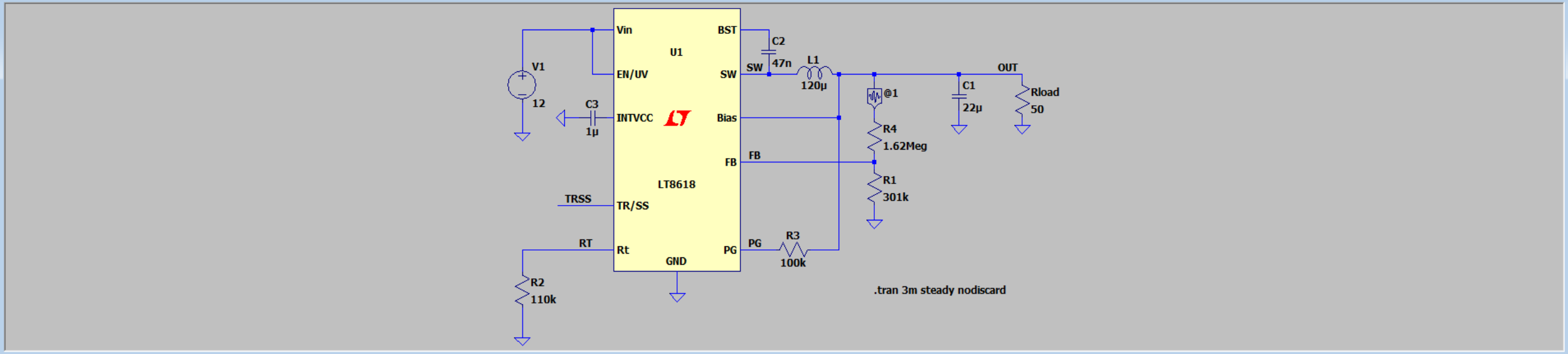
File Edit Hierarchy View Simulate Tools Window Help

LT8618 LT8618

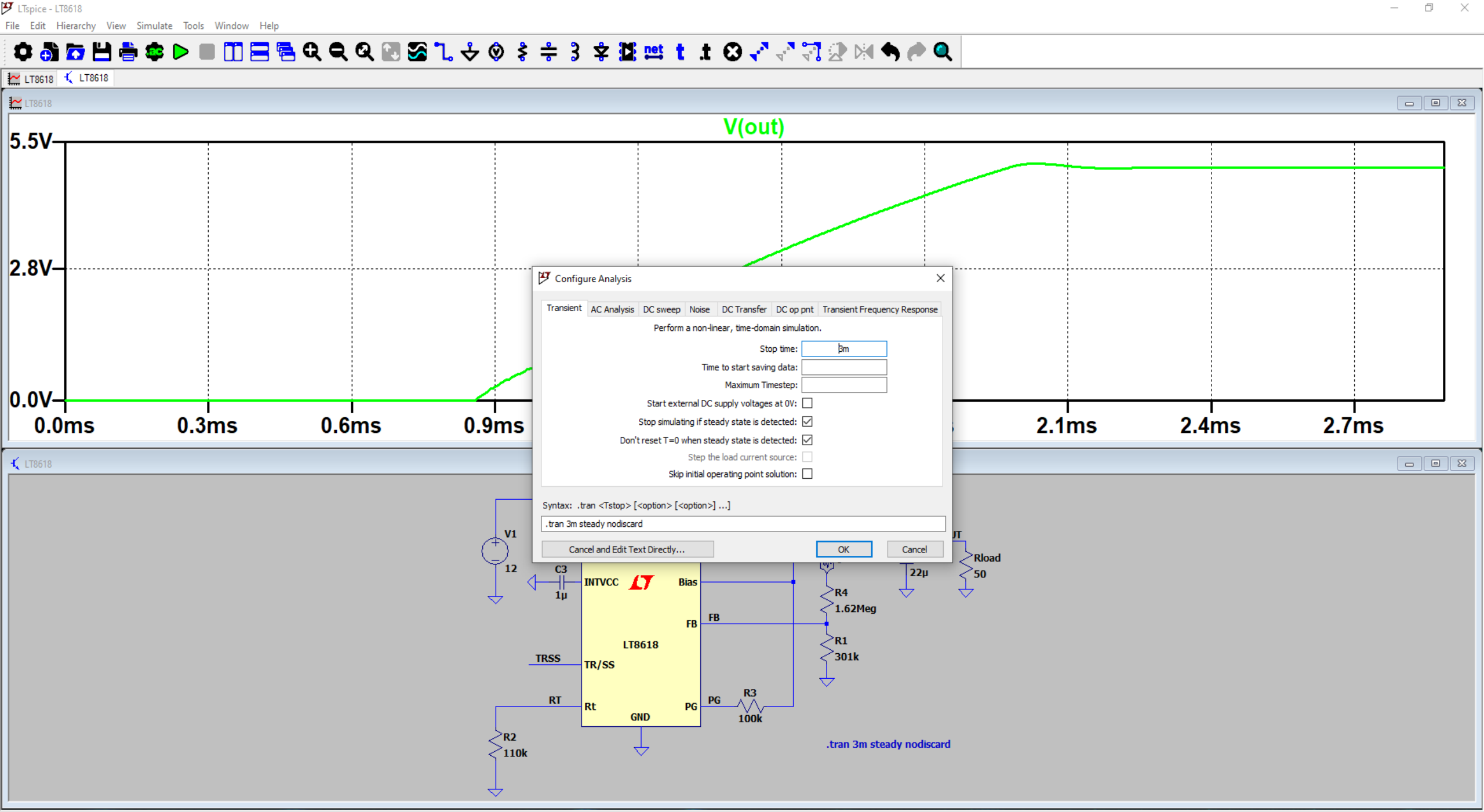
LT8618



LT8618



Start drafting a new schematic


LTspice - LT8618
File Edit Hierarchy View Simulate Tools Window Help
LT8618
LT8618
V(out)
5.5V
2.8V
0.0V
0.0ms
0.3ms
0.6ms
0.9ms
2.1ms
2.4ms
2.7ms
Configure Analysis
Transient
AC Analysis
DC sweep
Noise
DC Transfer
DC op pnt
Transient Frequency Response
Perform a non-linear, time-domain simulation.
Stop time:
3m
Time to start saving data:
Maximum Timestep:
Start external DC supply voltages at 0V:
Stop simulating if steady state is detected:
Don't reset T=0 when steady state is detected:
Step the load current source:
Skip initial operating point solution:
Syntax: .tran <Tstop> [<option> [<option>] ...]
.tran 3m steady nodiscard
Cancel and Edit Text Directly...
OK
Cancel
V1
12
C3
1µ
INTVCC
Bias
FB
LT8618
TRSS
TR/SS
RT
Rt
PG
GND
R2
110k
R3
100k
R4
1.62Meg
R1
301k
22µ
Rload
50
.tran 3m steady nodiscard
Right click to edit ".tran 3m steady nodiscard"

LTspice - LT8618.fra_1

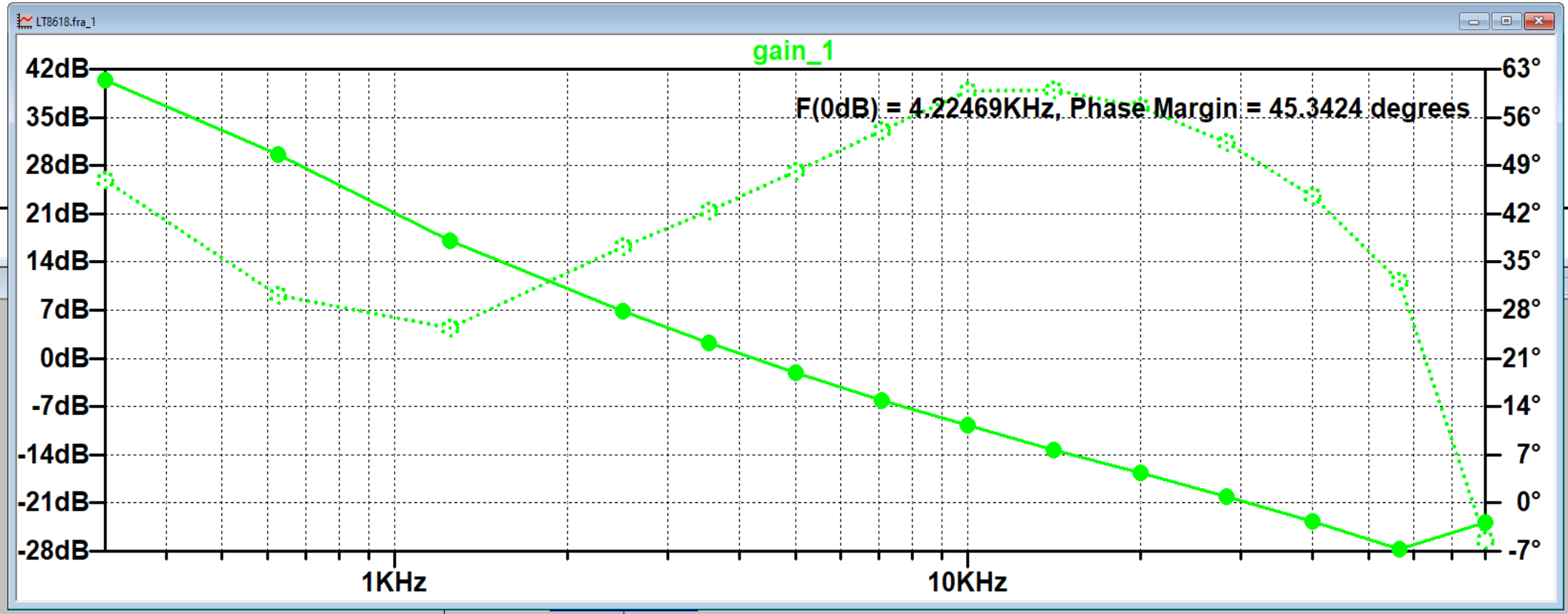
File View Plot Settings Simulation Tools Window Help

LT8618 LT8618 LT8618.fra_1

LT8618

5.5V
2.8V
0.0V
0ms
10ms

LT8618.fra_1



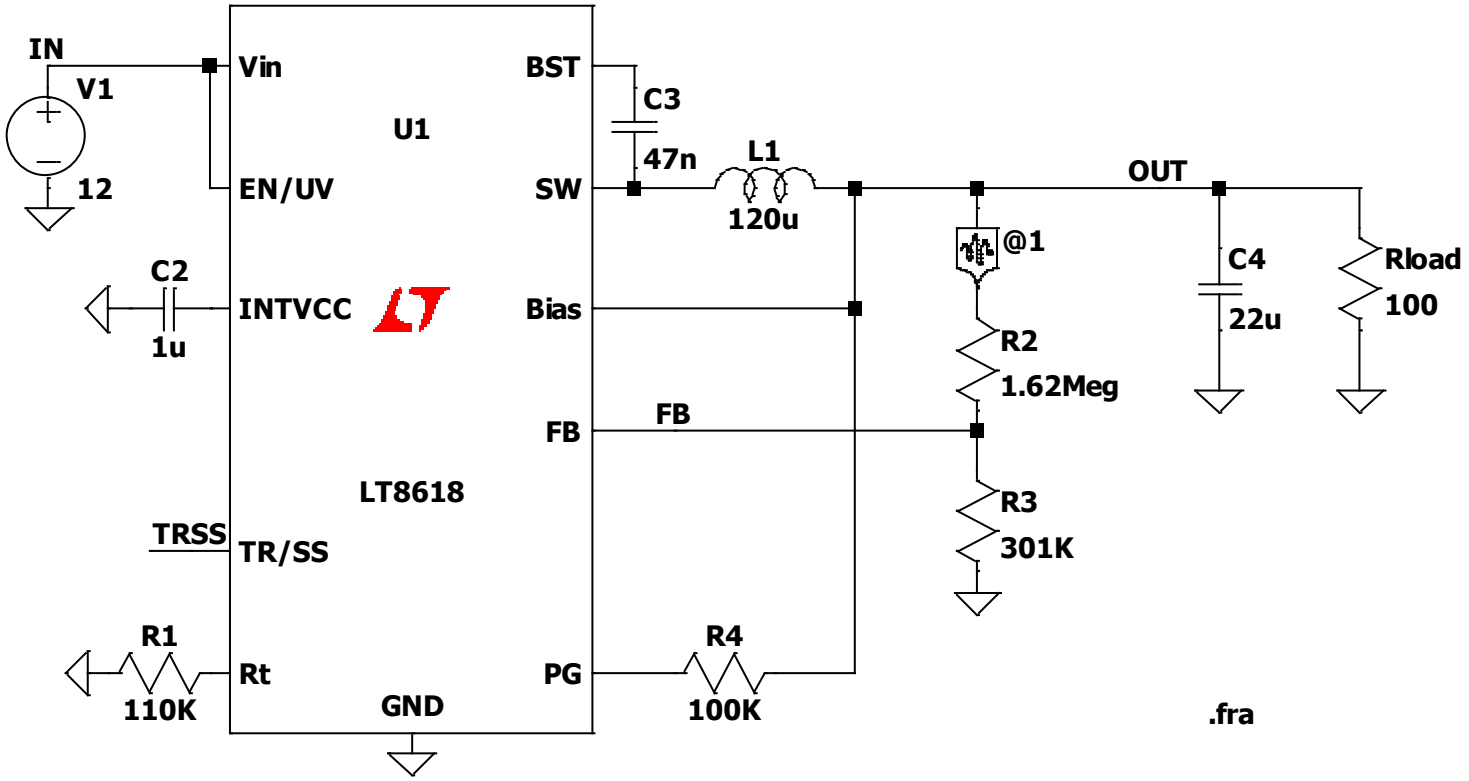
LT8618

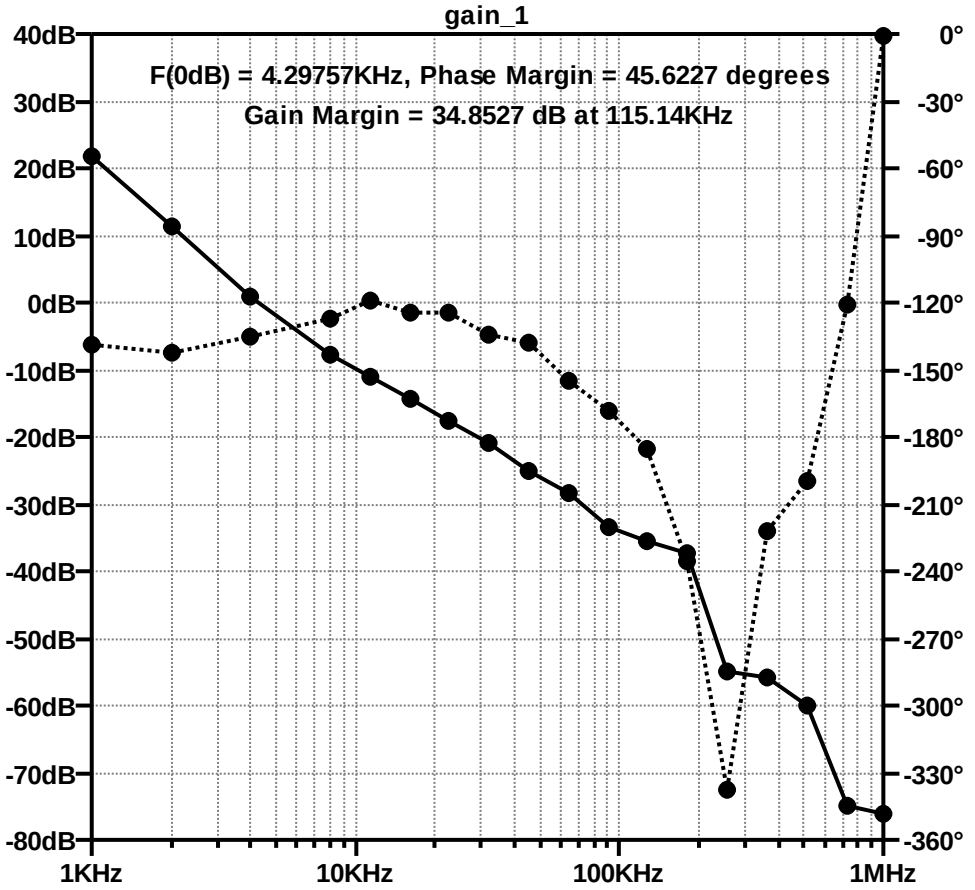
R2
110k

.tran 3m steady nodiscard
.fra

LT8618 (Buck)

100mA Synchronous Buck, f_{SW} = 400kHz, V_{OUT} = 5V

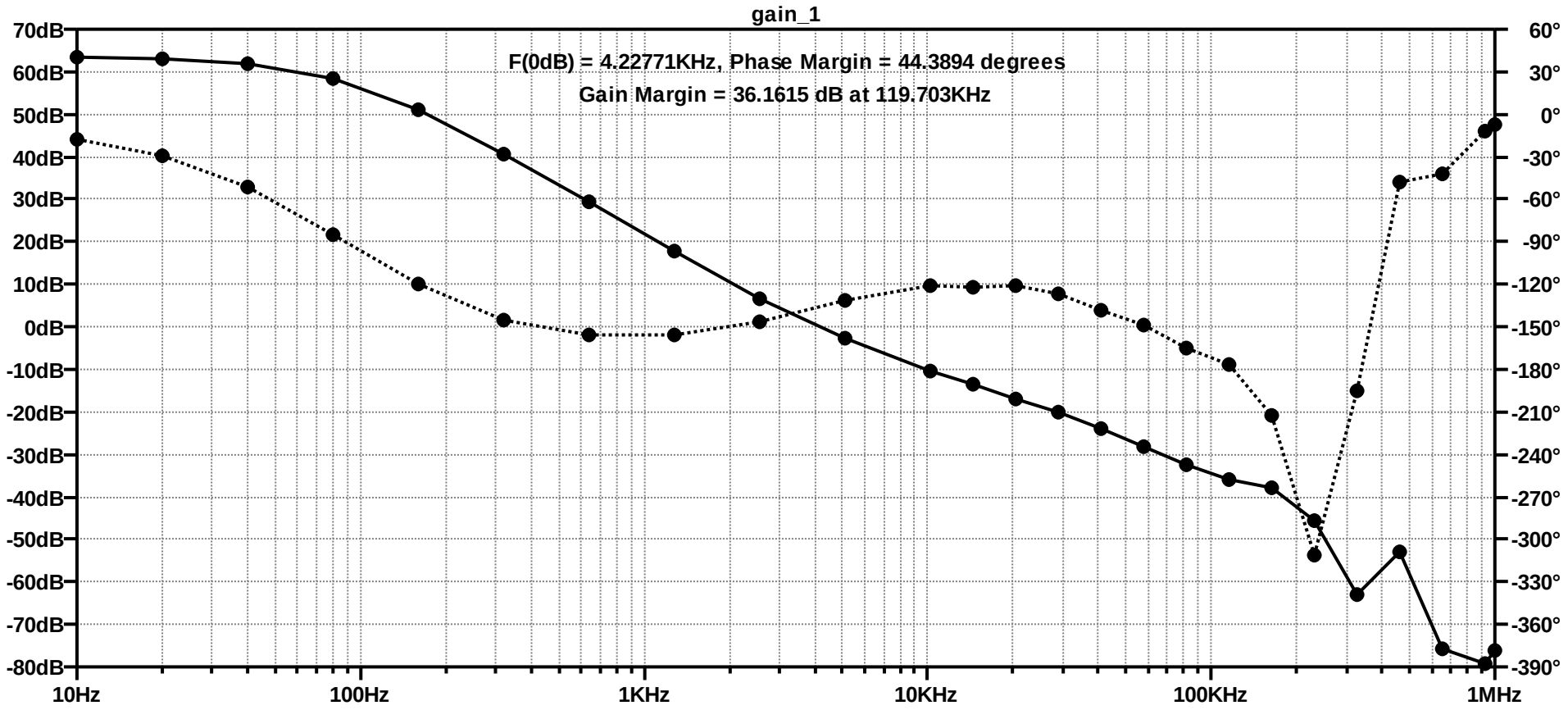




Run Time 14.7s (On 5 Years Old Intel Core i9 7920X)

LT8618 (Buck)

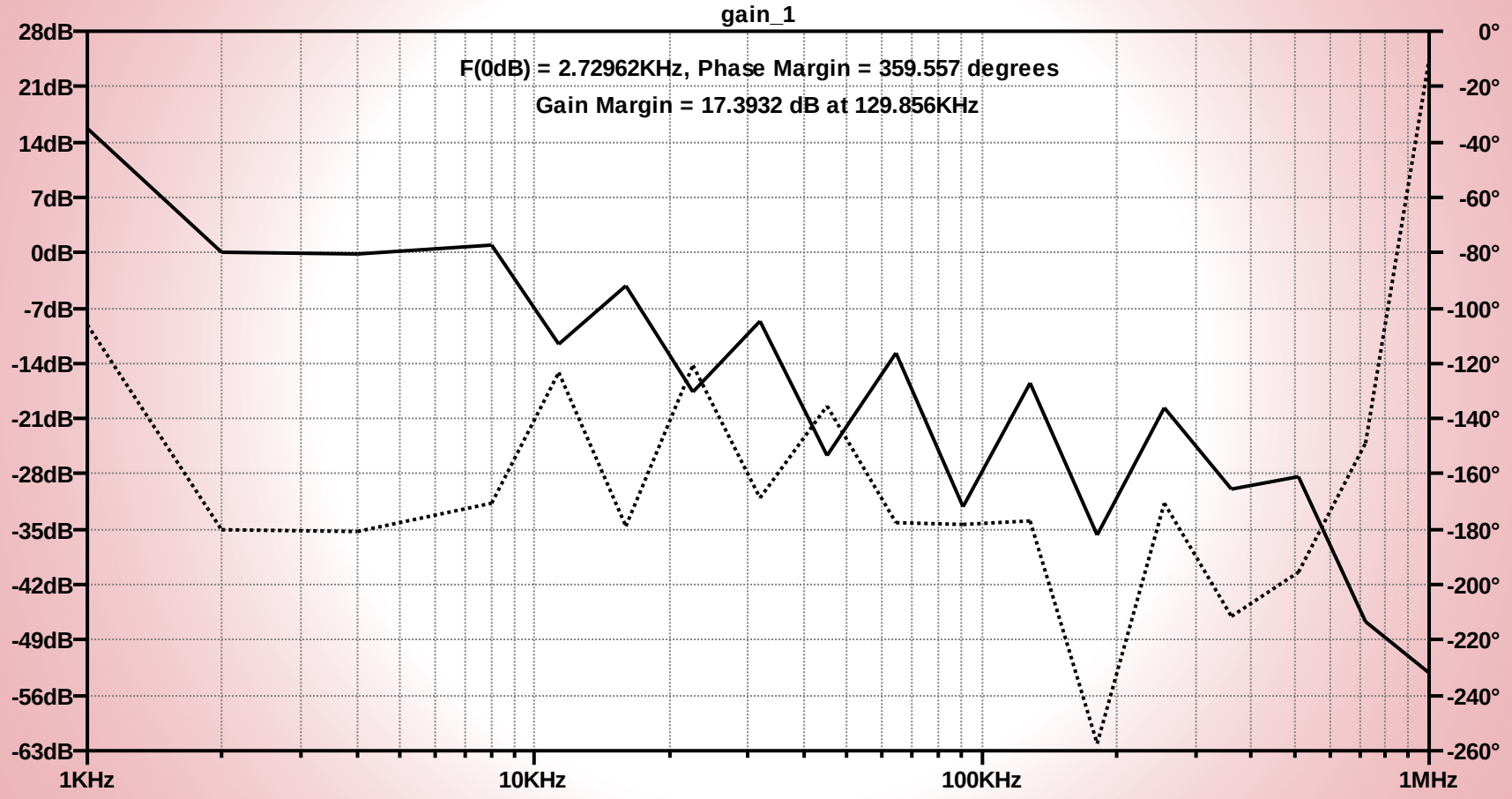
100mA Synchronous Buck, f_{SW} = 400kHz, V_{OUT} = 5V



Run Time 9min 12s

LT8618 (Buck)

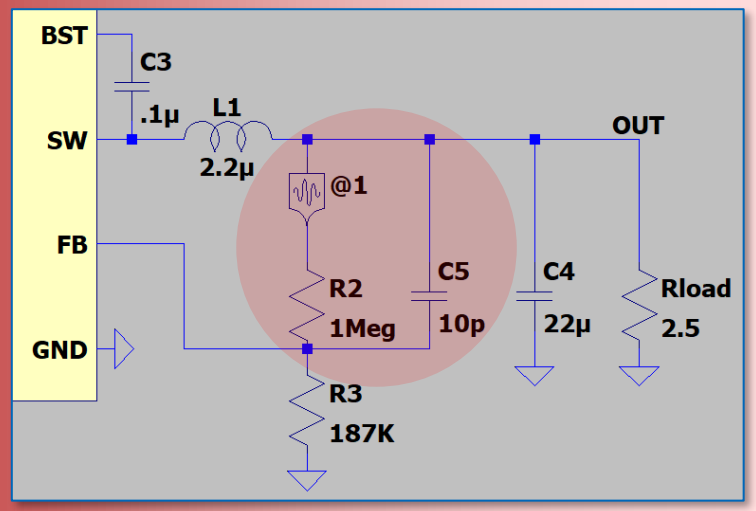
Stimulus Too Small



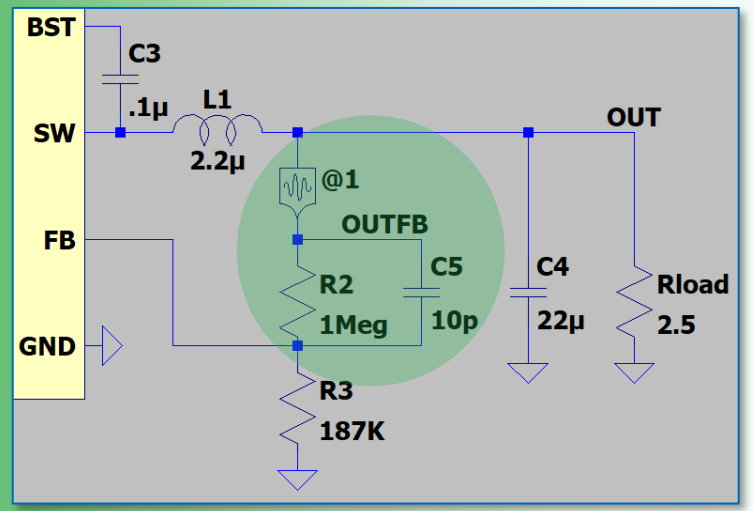
FAIL

Break the Loop

Incorrect



Correct



Criteria

- Interrupt **all** feedback paths
- FRA component must be point from **lower impedance (flat side)** to **higher impedance (pointy side)**

This requires engineering

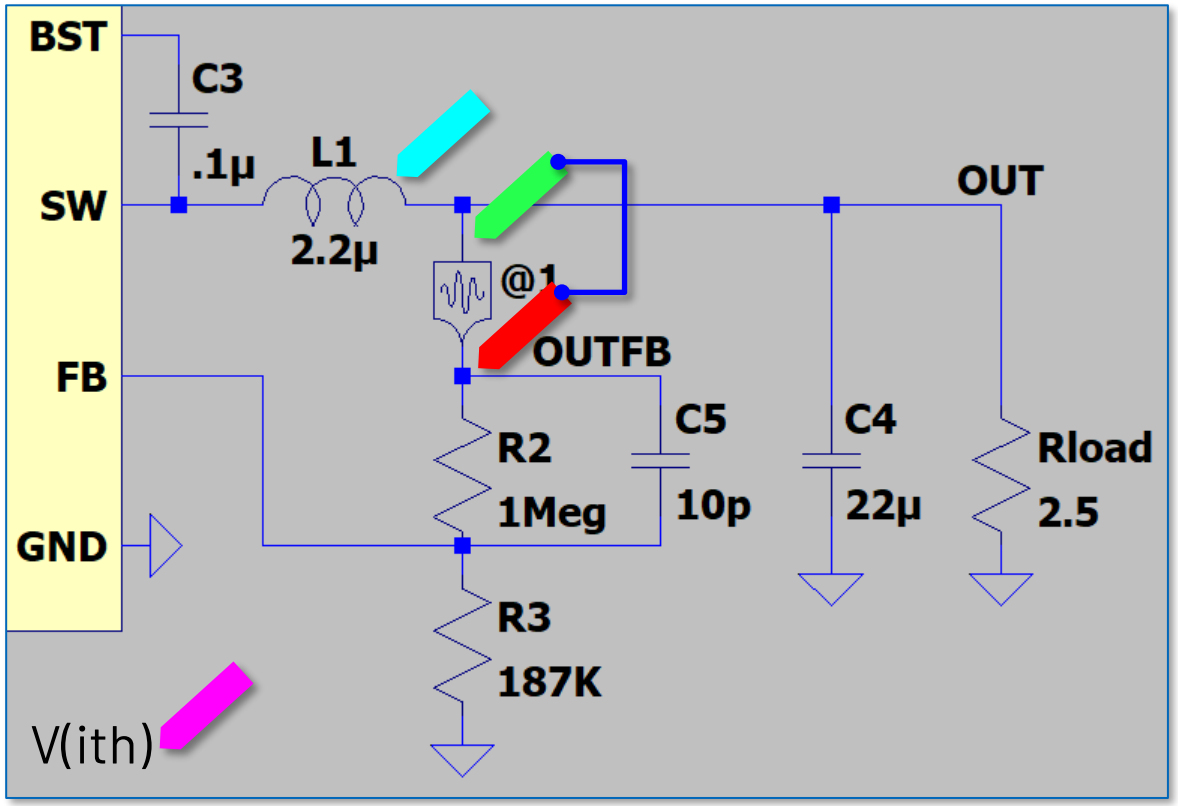
- LTspice does not know the correct placement
- Many circuits have multiple places where the loop can be broken—if in doubt, try two places and compare the results (adjust the stimulus amplitude appropriately)

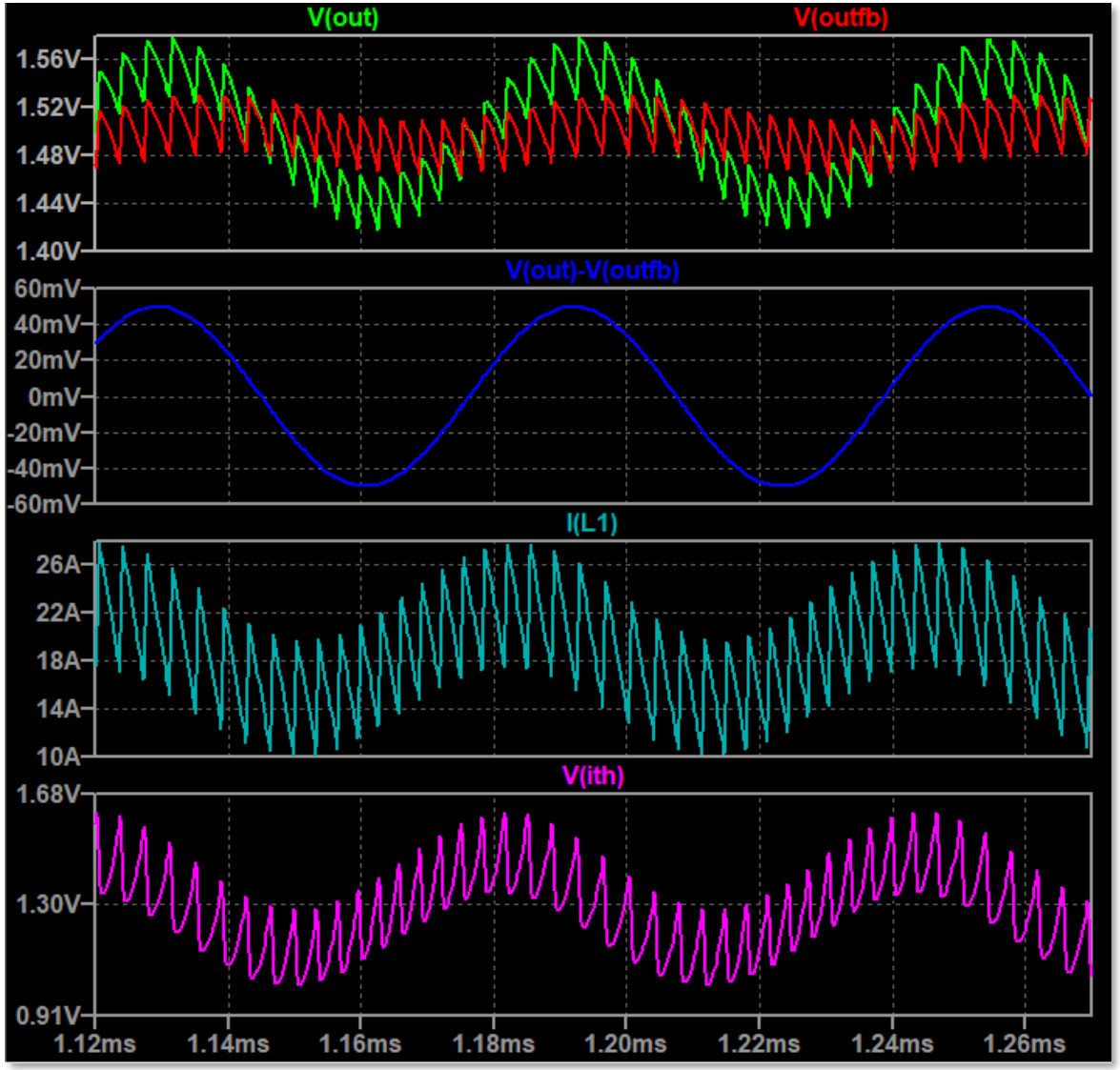
Inspect the FRA transient waveforms

Voltage at both FRA terminals, and the difference

Inductor current

Control voltage (if external)



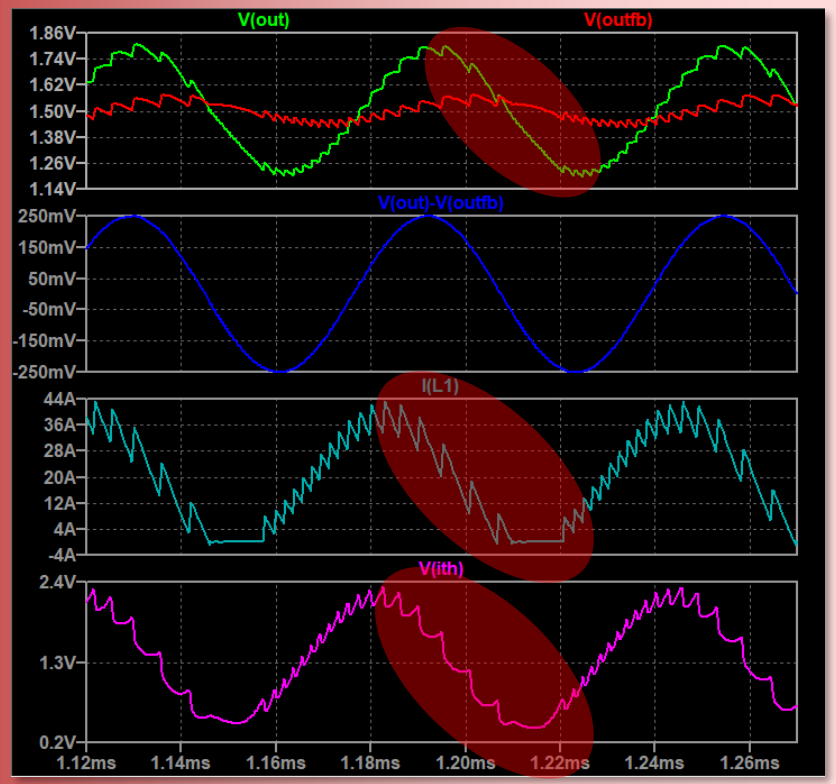


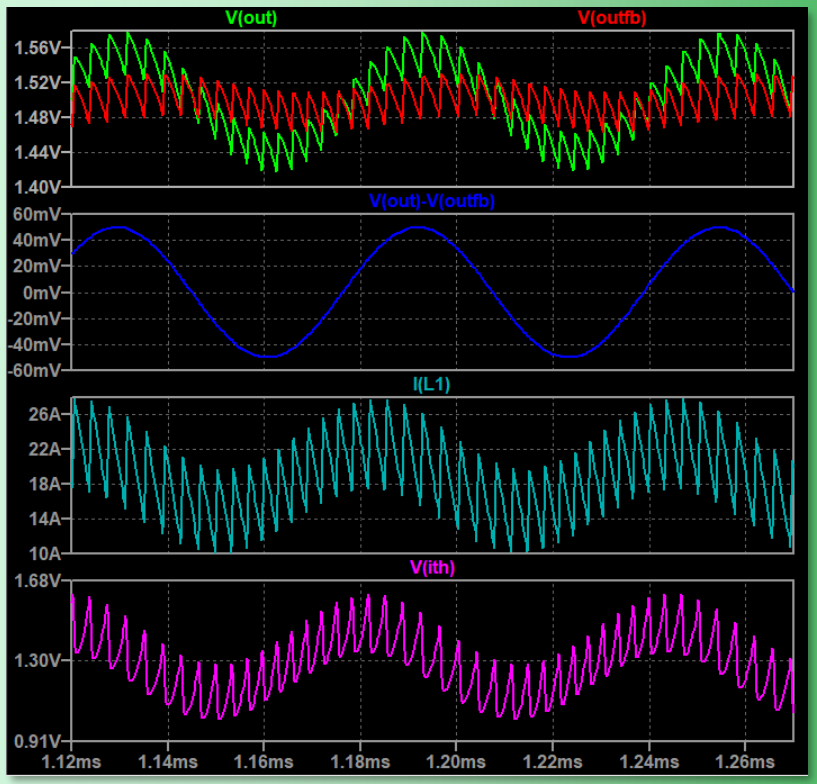
Inspect the FRA transient waveforms

Ideally, sinusoidal pattern should be evident and symmetric

- Look for signs of non-linearity, which would indicate stimulus amplitude too large
- Note that there are discontinuities when the frequency changes – these are expected

Bad
too much stimulus





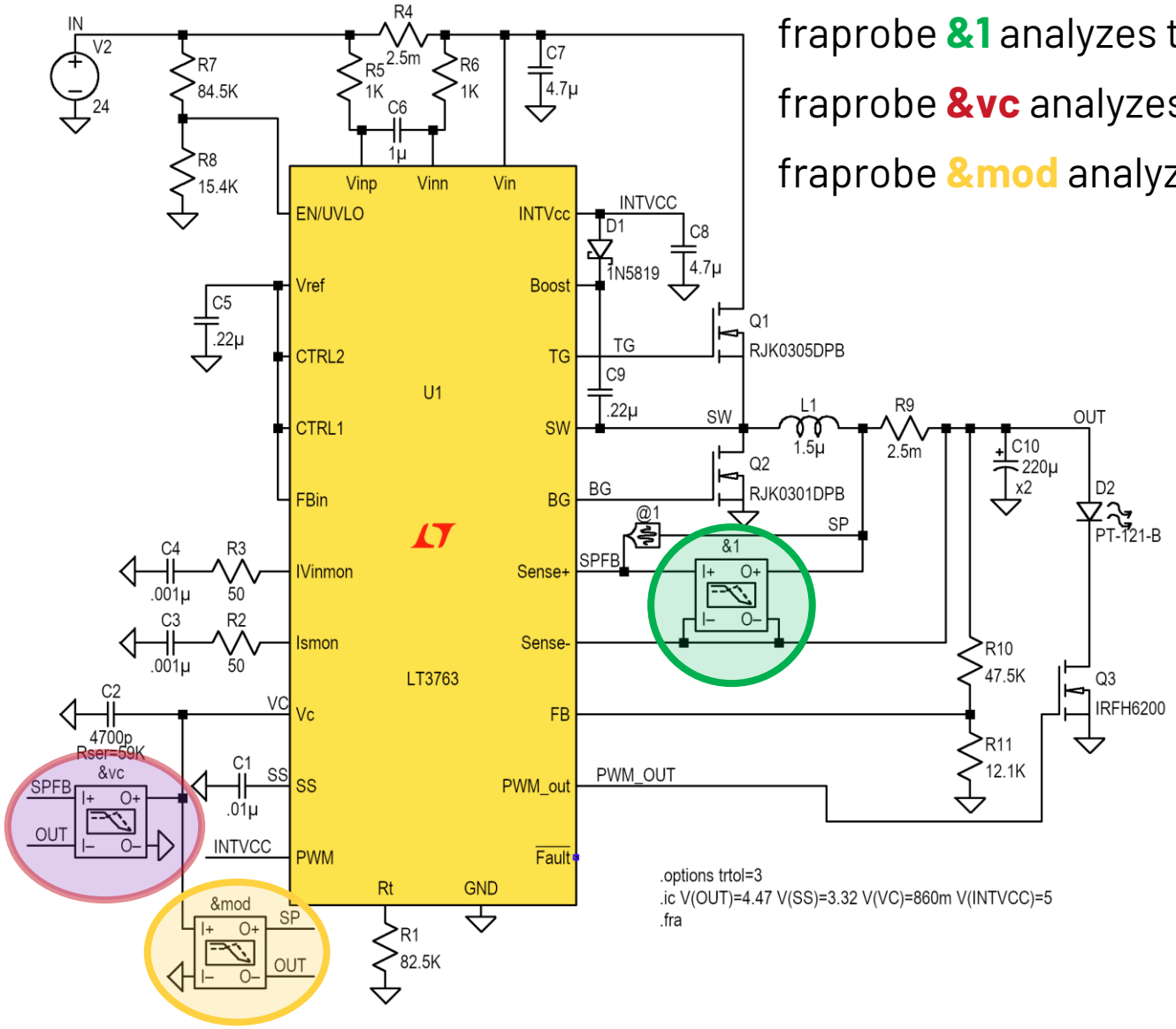
Good

Current Feedback and Partial Loop Analysis

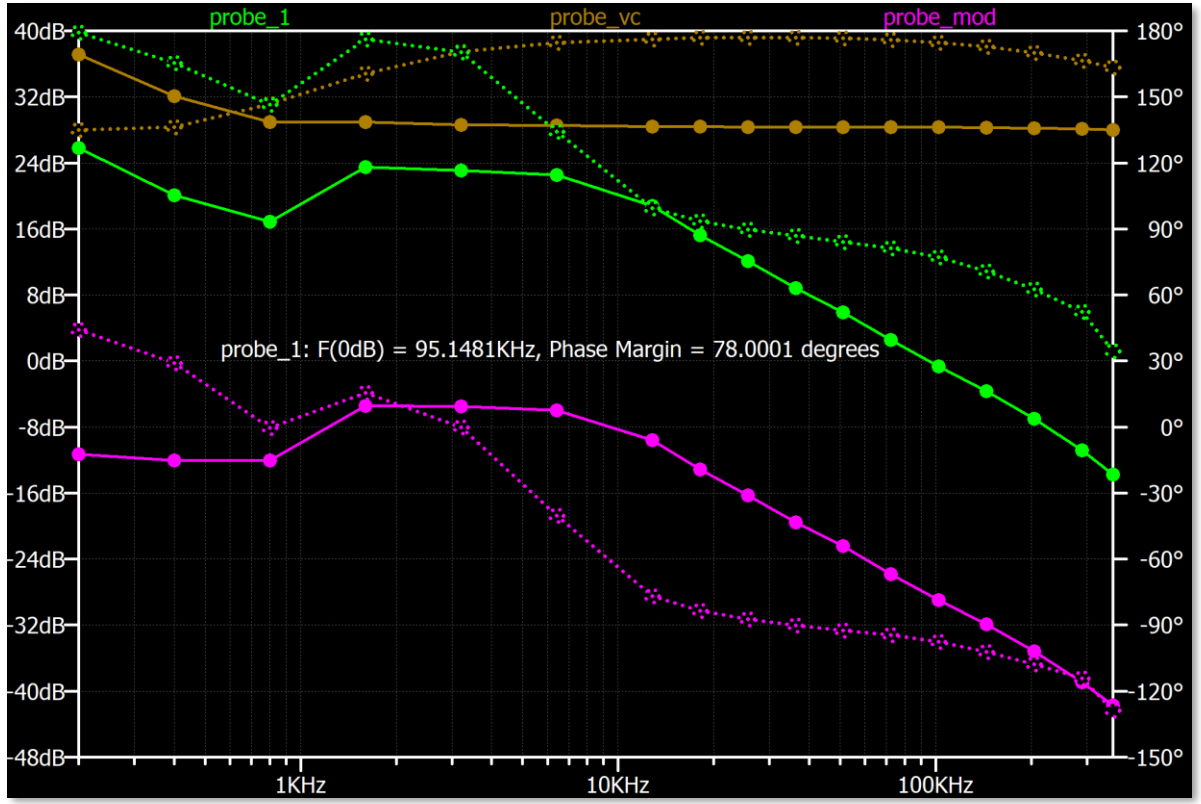
fraprobe **&1** analyzes the full loop differentially across the sense resistor R9

fraprobe **&vc** analyzes from current sense resistor to compensation point

fraprobe **&mod** analyzes from compensation point to current sense resistor




```
.options trtol=3
.ic V(OUT)=4.47 V(SS)=3.32 V(VC)=860m V(INTVCC)=5
.fra
```



Example: Stepping A Parameter

Easily Plot Phase And Gain Margin

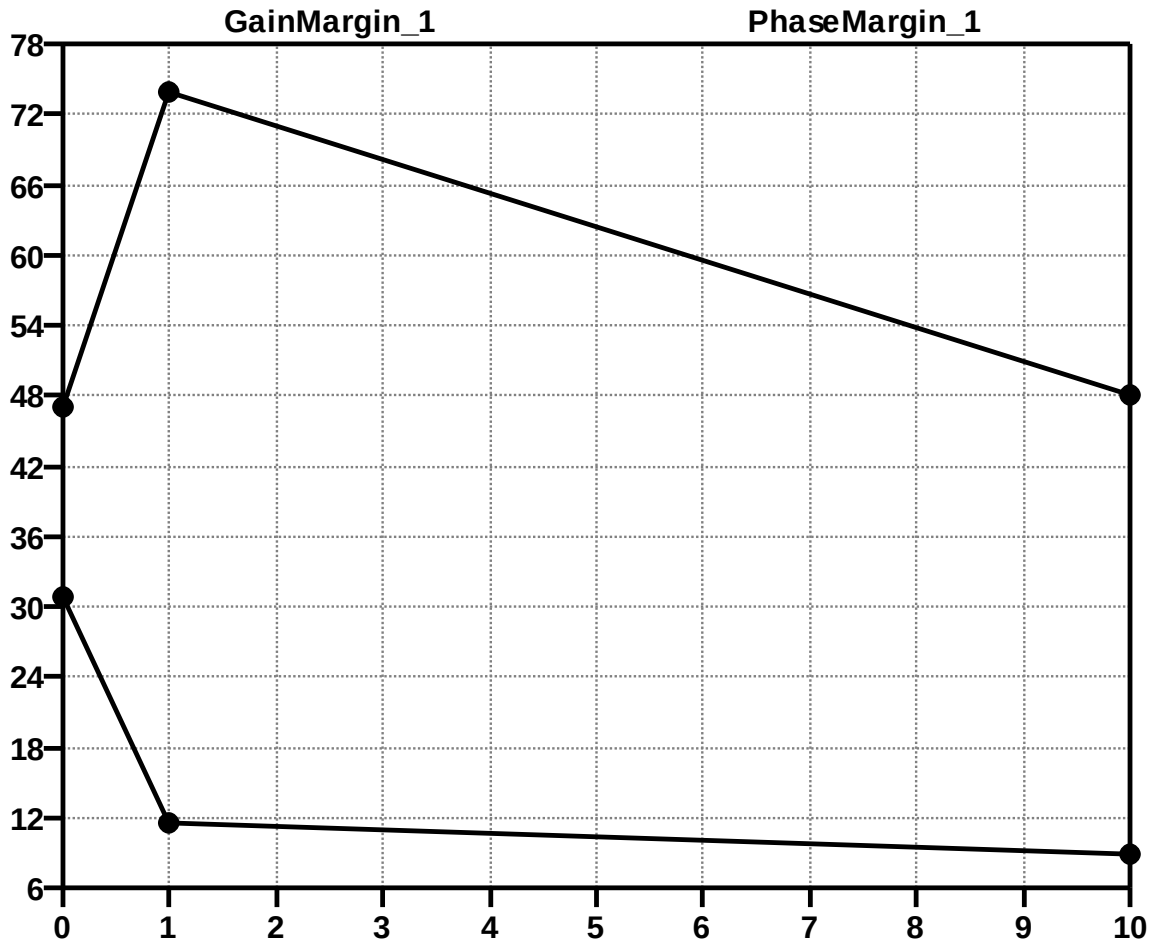
SPICE Error Log: fra_LT8648S.log

```
Measurement: PhaseMargin_1
  step              PhaseMargin          at
          1         47.0836°             46010.9
          2         73.9102°             206029
          3         48.0784°             234740

Measurement: GainMargin_1
  step              GainMargin           at
          1         30.7318dB            725478
          2         11.6137dB            582070
          3         8.96924dB            590198
```

Find Ctrl+F

Plot .step'ed .meas data

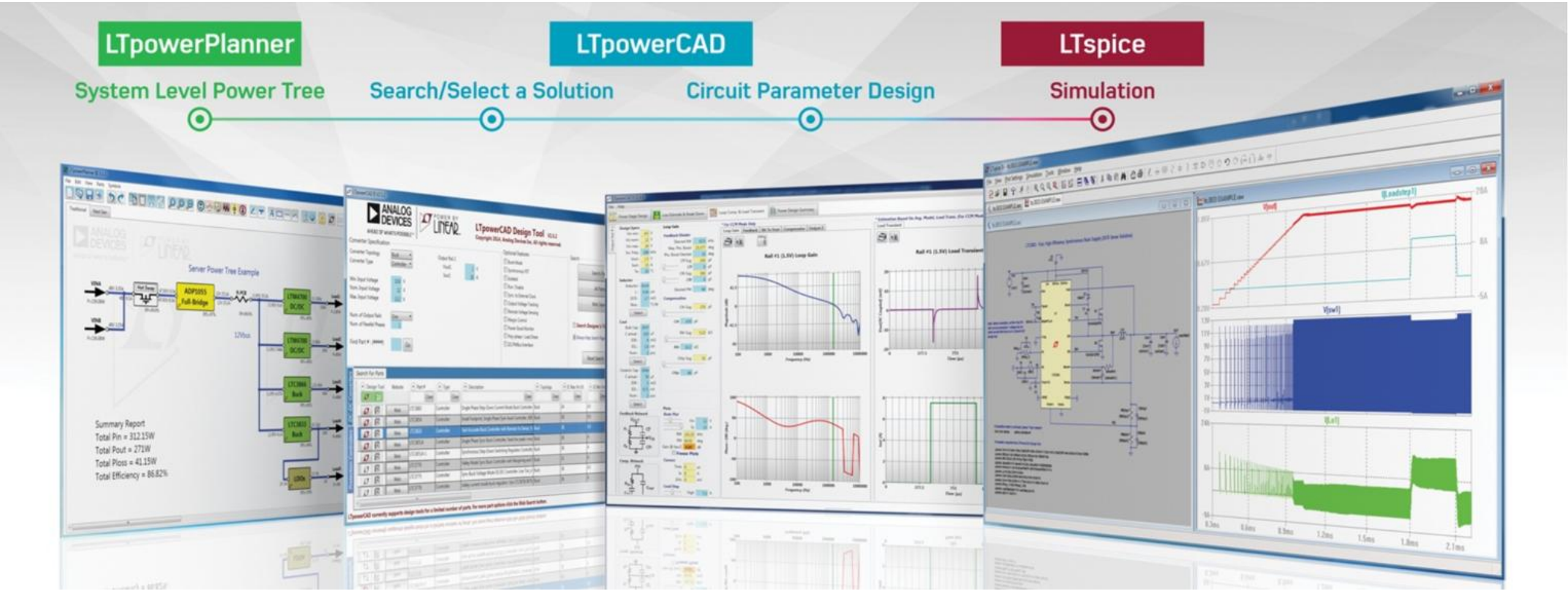
Close



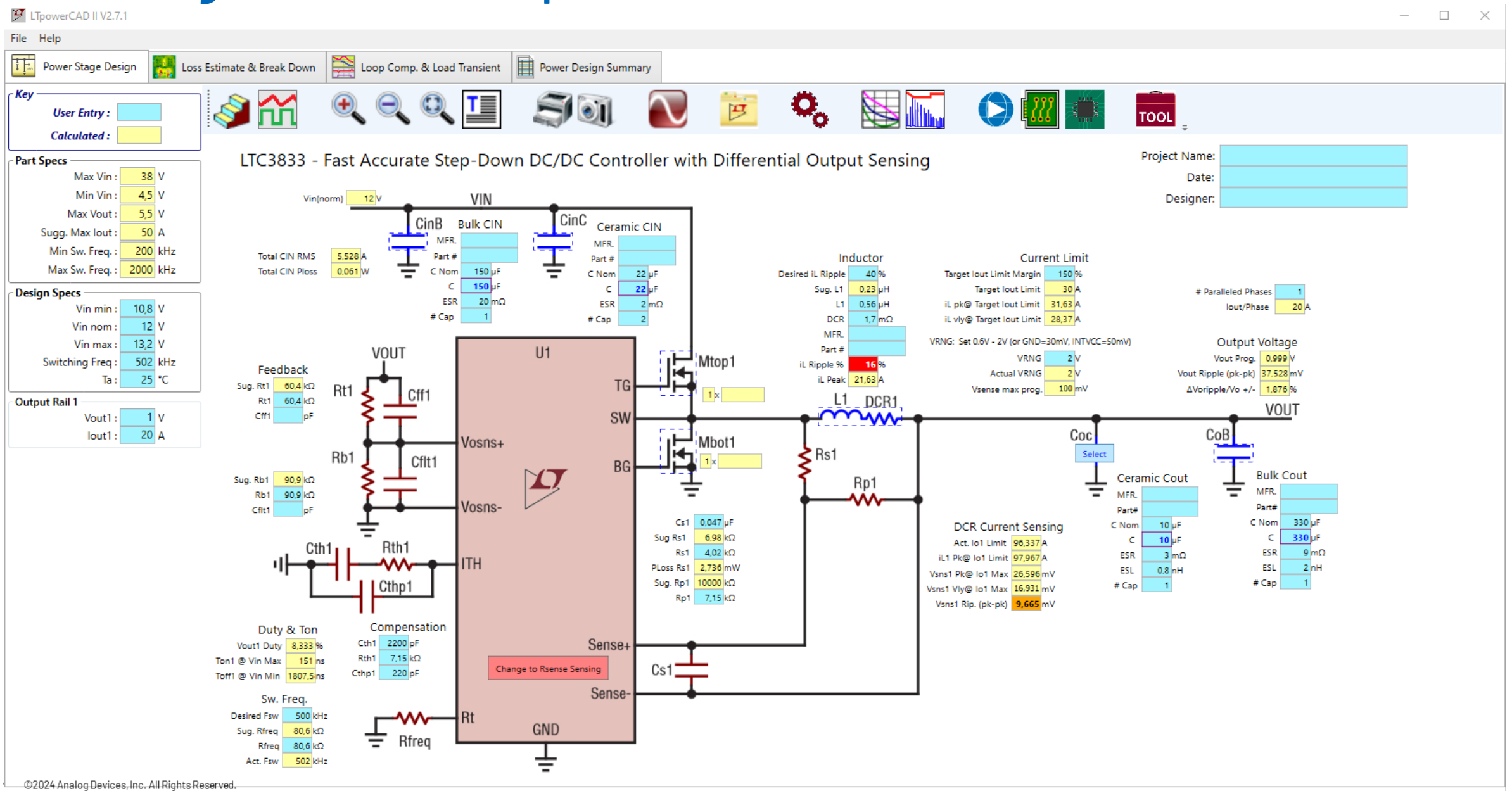
LTpowerCAD for loop analysis

analog.com

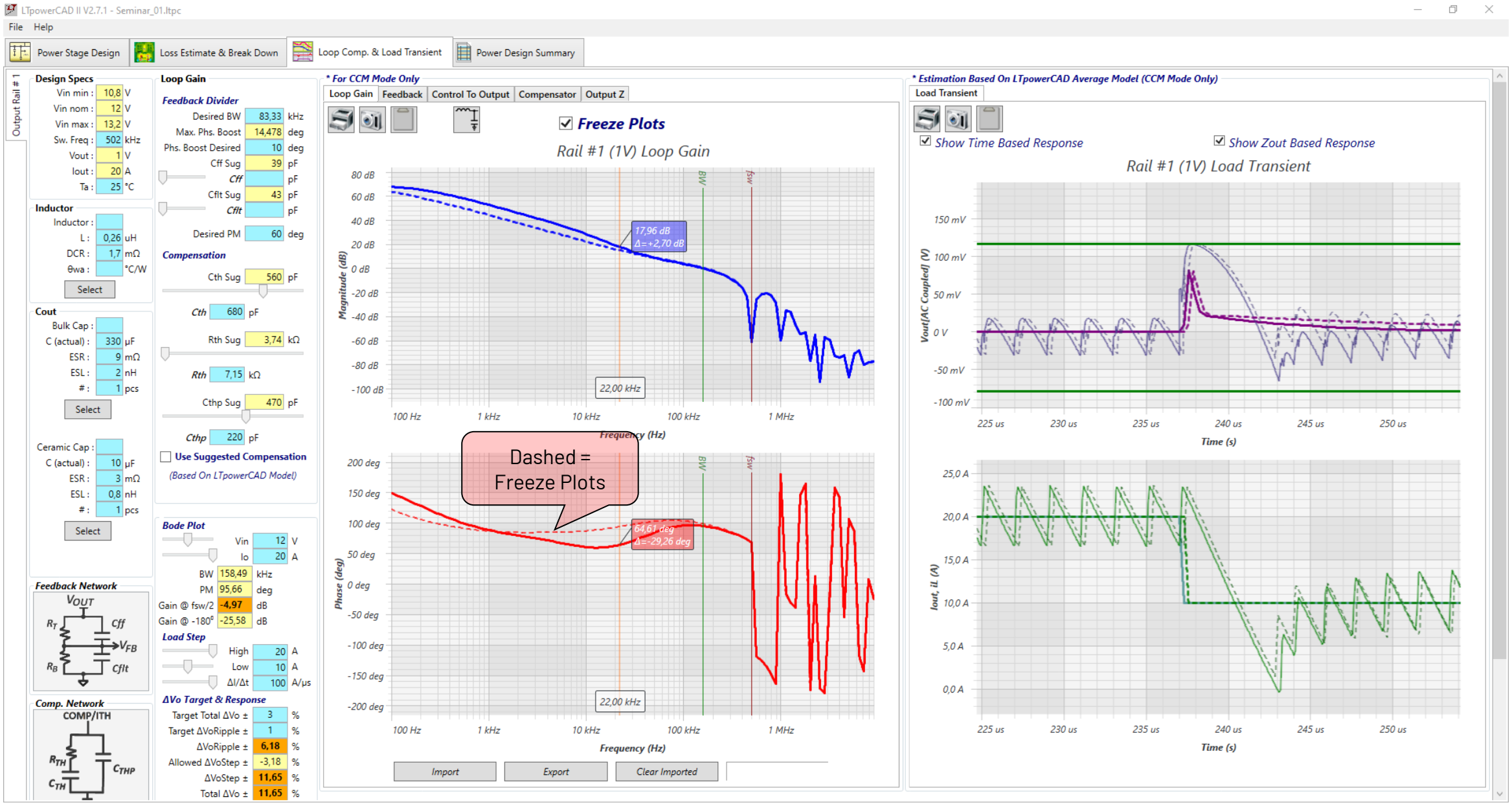
LTpowerCAD in the center



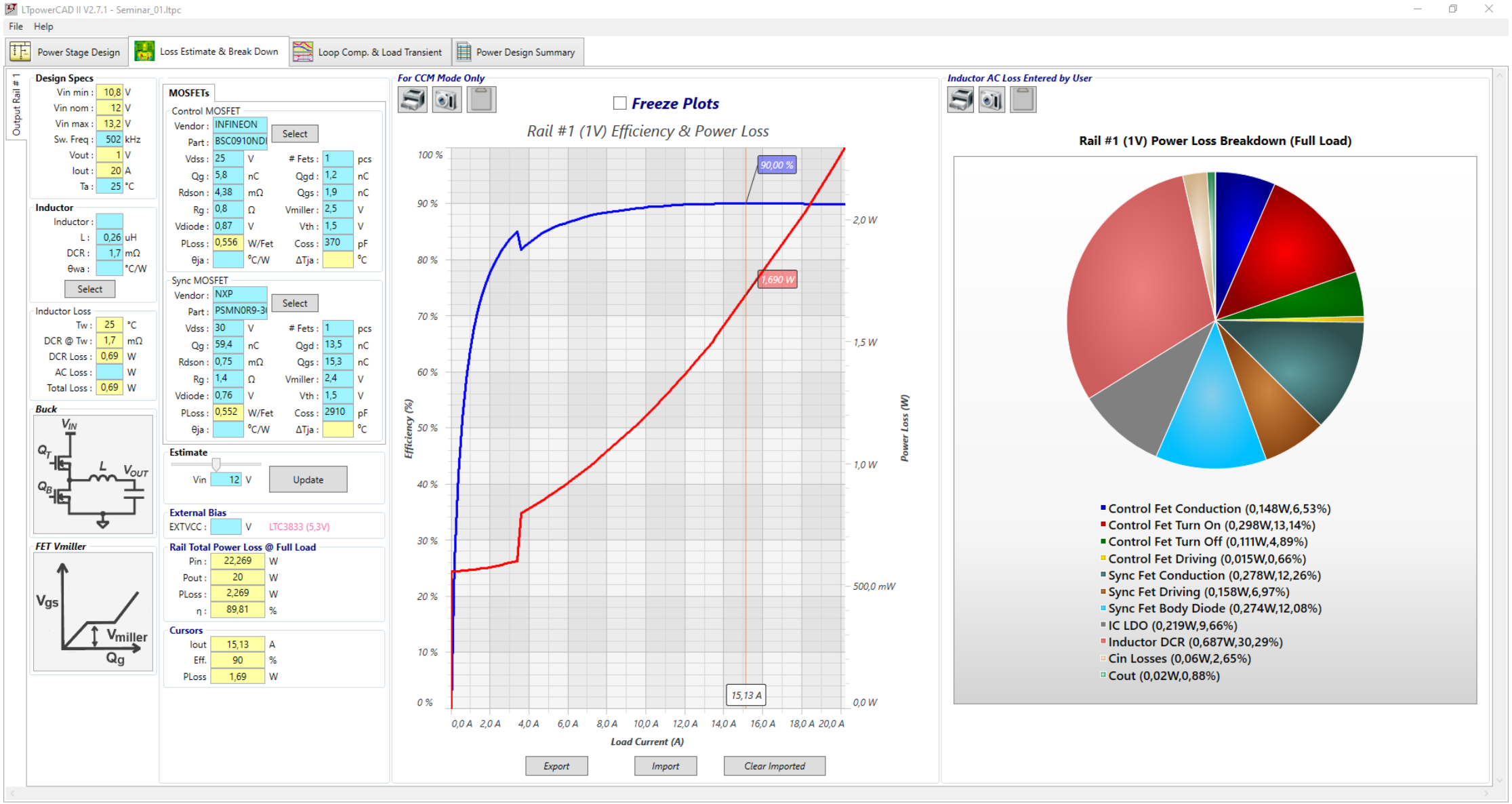
Selecting external components



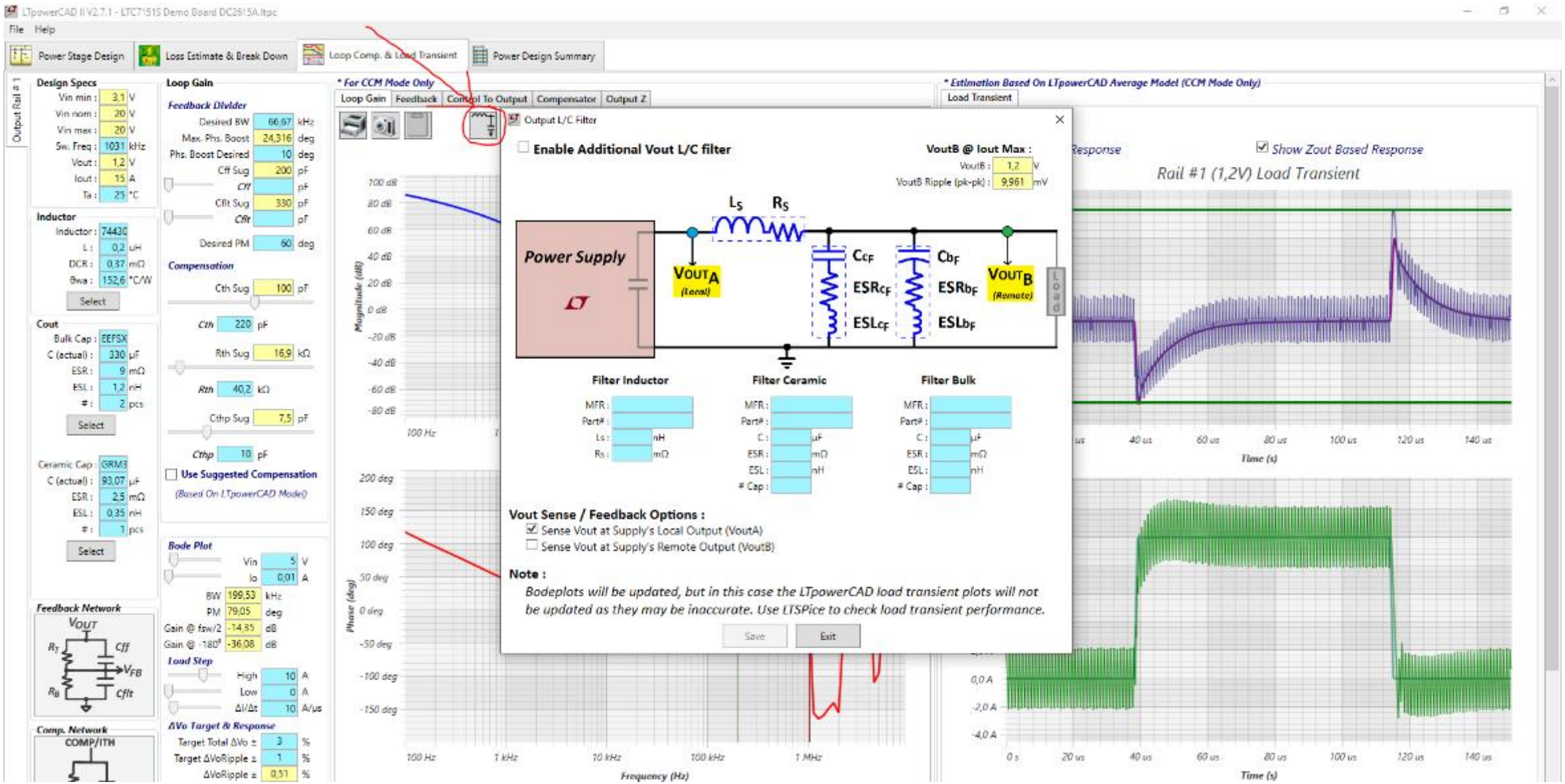
Feedback Loop & Transient Designs



Efficiency Optimization



Designing an output filter

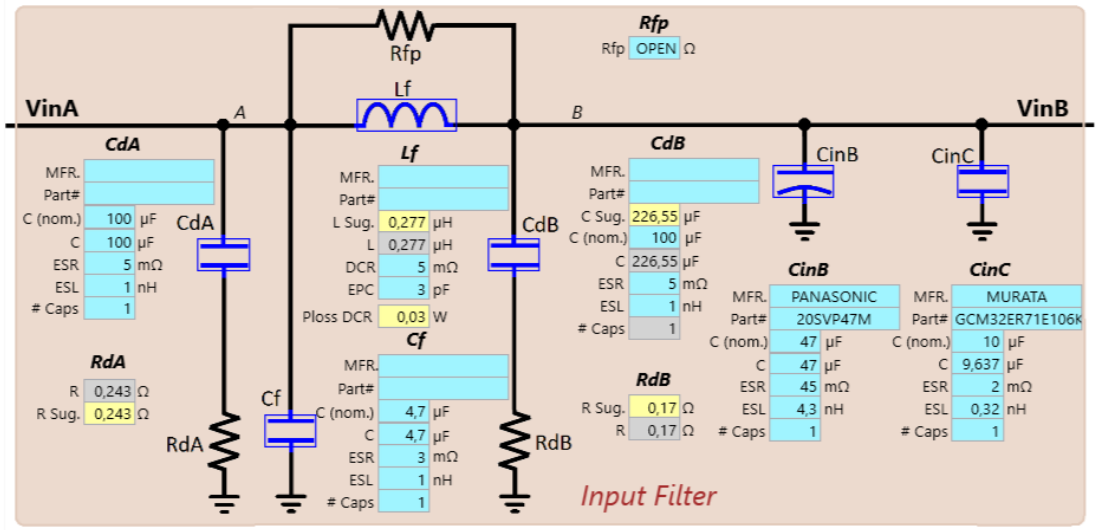


EMI Plot

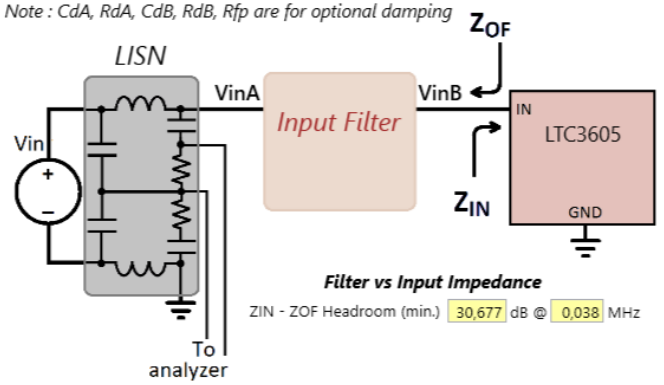
Input EMI Filter Design

Conducted (Differential Mode) EMI Filter Design

EMI Specification : CISPR22 | EMI Margin Desired : 0 dBµV | Use Suggested Values | Show EMI Without Input Filter | Cursor X : 77,40 kHz | Cursor Y : 39,38 dBµV



Note : CdA, RdA, CdB, RdB, Rfp are for optional damping



EMI vs. Specification

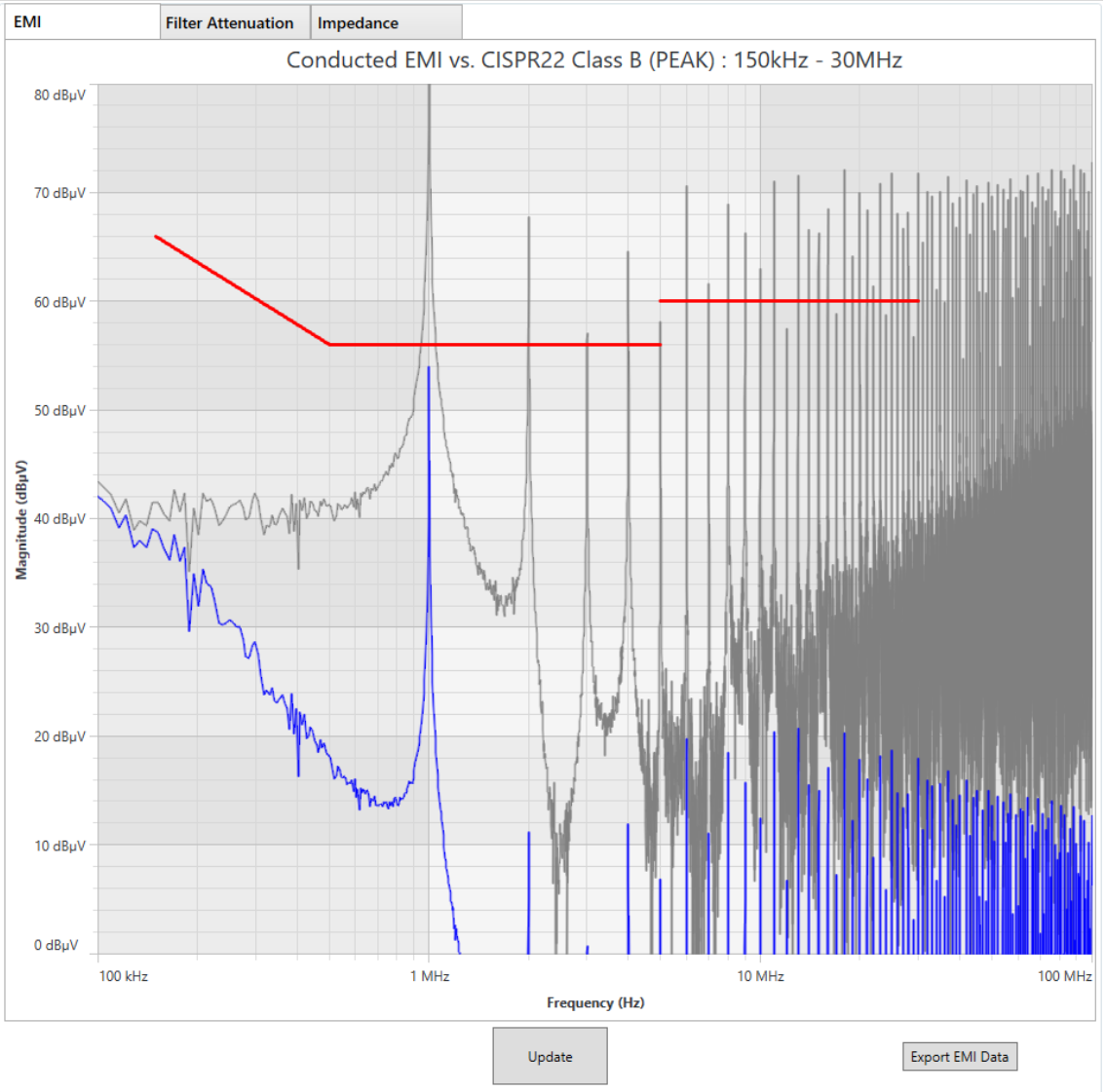
Actual EMI Margin (min.) 1,995 dBµV @ 1,001 MHz

Operating Conditions

Vin 6 V | Vout1 2,49 V | Iout1 5 A | Fsw 1000 kHz

Filter vs Input Impedance

ZIN - ZOF Headroom (min.) 30,677 dB @ 0,038 MHz



LISN...Line Impedance Stabilization Network

ANALOG DEVICES

Simulating Tollerances with Monte Carlo

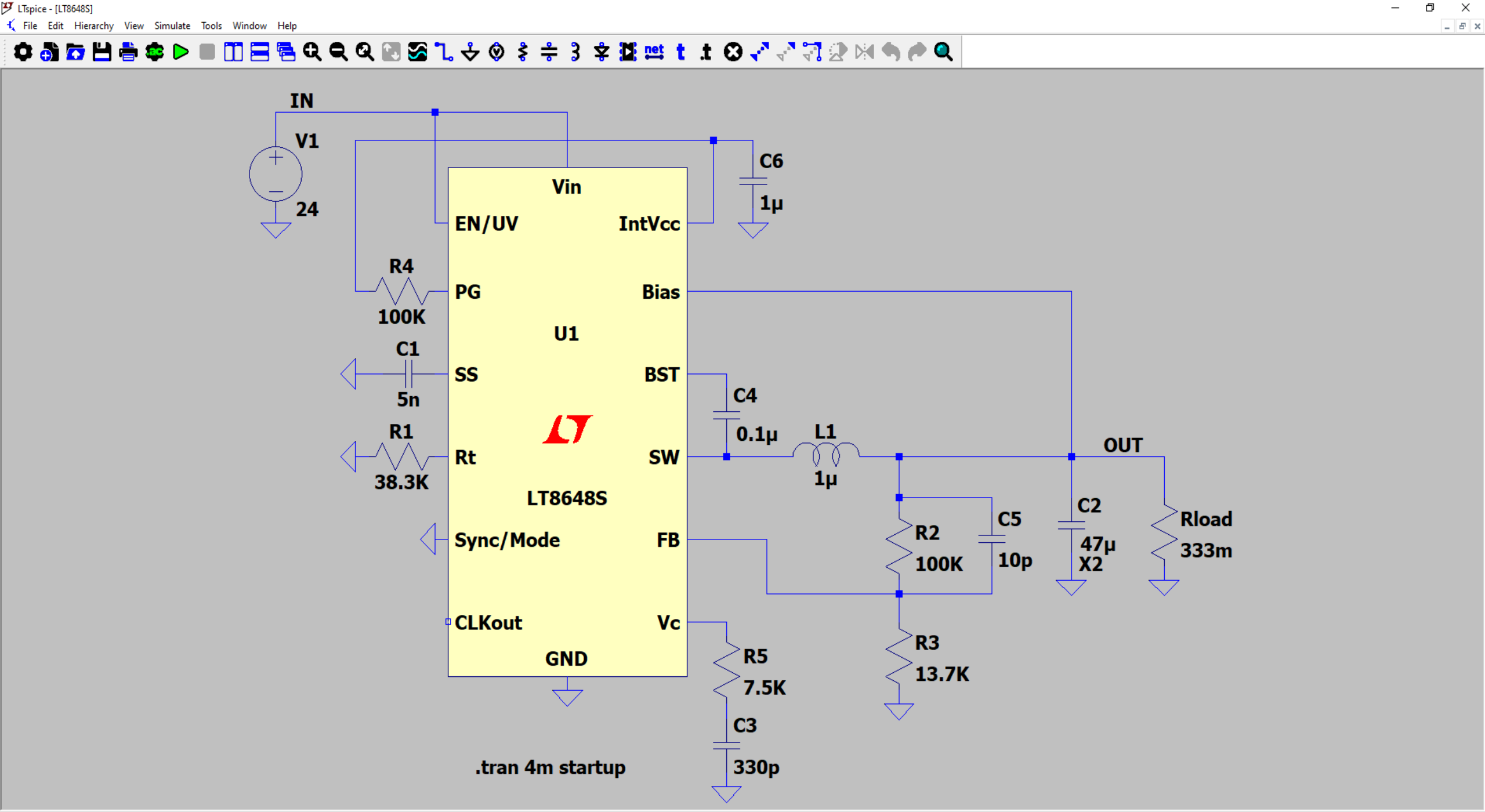
Monte Carlo Simulations: Statistical Functions

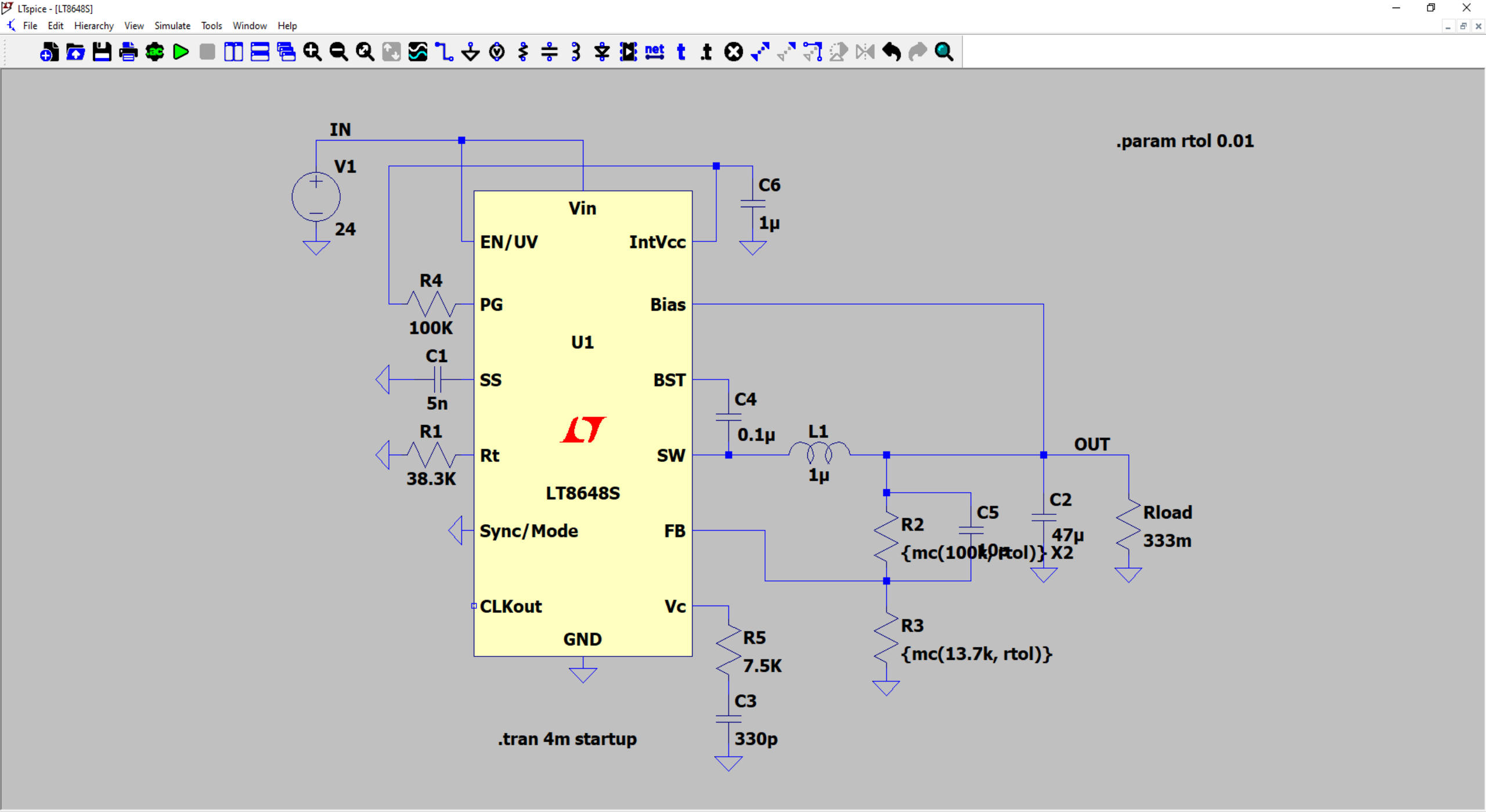
LTspice provides several statistical functions

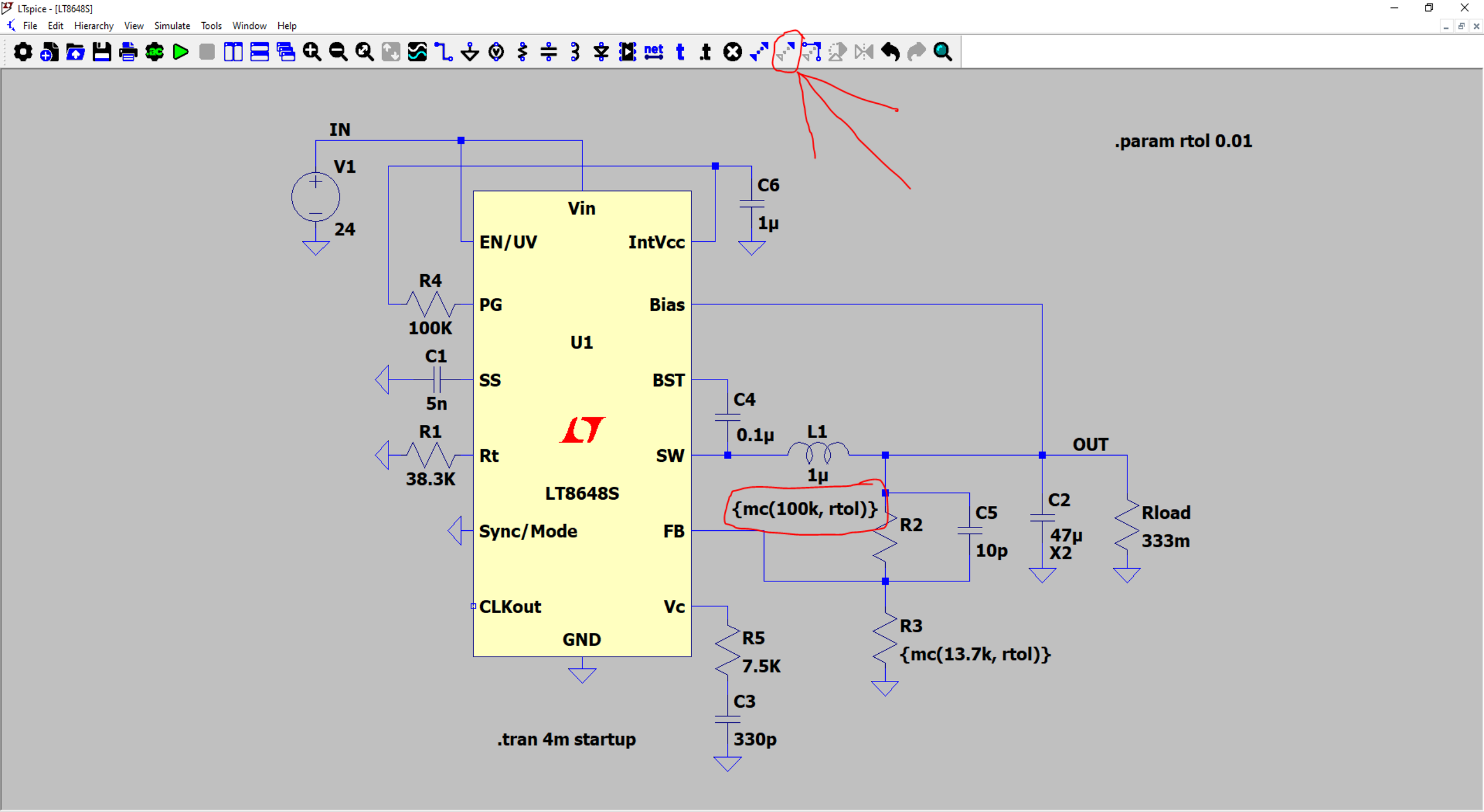
flat(x)	Random number between –x and x with uniform distribution
gauss(x)	Random number from Gaussian distribution with sigma of x.
mc(x,y)	A random number between x*(1+y) and x*(1-y) with uniform distribution.
rand(x)	Random number between 0 and 1 depending on the integer value of x.
random(x)	Similar to rand(), but smoothly transitions between values.

Most popular for Monte Carlo simulations:

- mc(x,y) for device parameters with target values not equal to zero
  - R, C, V, …
- flat(x) for parameters which are ideally 0
  - offset


LTspice - [LT8648S]
File Edit Hierarchy View Simulate Tools Window Help
IN
V1
24
C6
1µ
Vin
EN/UV
IntVcc
R4
100K
PG
Bias
U1
C1
5n
SS
BST
C4
0.1µ
L1
1µ
OUT
R1
38.3K
Rt
SW
LT8648S
R2
100K
C5
10p
C2
47µ
X2
Rload
333m
Sync/Mode
FB
R3
13.7K
CLKout
Vc
GND
R5
7.5K
C3
330p
.tran 4m startup


LTspice - [LT8648S]
File Edit Hierarchy View Simulate Tools Window Help
IN
V1
24
C6
1µ
Vin
EN/UV
IntVcc
R4
100K
PG
Bias
U1
C1
5n
SS
BST
C4
0.1µ
L1
1µ
OUT
R1
38.3K
Rt
SW
LT8648S
R2
{mc(100k, rtol)}
C5
10p
C2
47µ
X2
Rload
333m
Sync/Mode
FB
CLKout
Vc
GND
R5
7.5K
C3
330p
R3
{mc(13.7k, rtol)}
.param rtol 0.01
.tran 4m startup

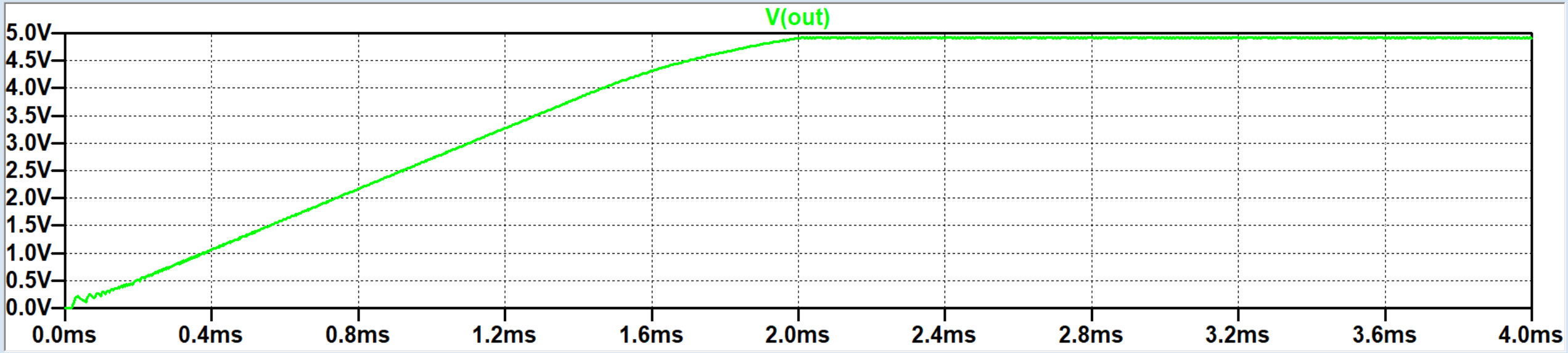

LTspice - [LT8648S]
File Edit Hierarchy View Simulate Tools Window Help
IN
V1
24
C6
1µ
Vin
EN/UV
IntVcc
R4
100K
PG
Bias
U1
C1
5n
SS
BST
C4
0.1µ
L1
1µ
OUT
R1
38.3K
Rt
SW
LT8648S
{mc(100k, rtol)}
R2
C5
10p
C2
47µ
X2
Rload
333m
Sync/Mode
FB
CLKout
Vc
GND
R5
7.5K
C3
330p
R3
{mc(13.7k, rtol)}
.tran 4m startup
.param rtol 0.01

LTspice - LT8648S

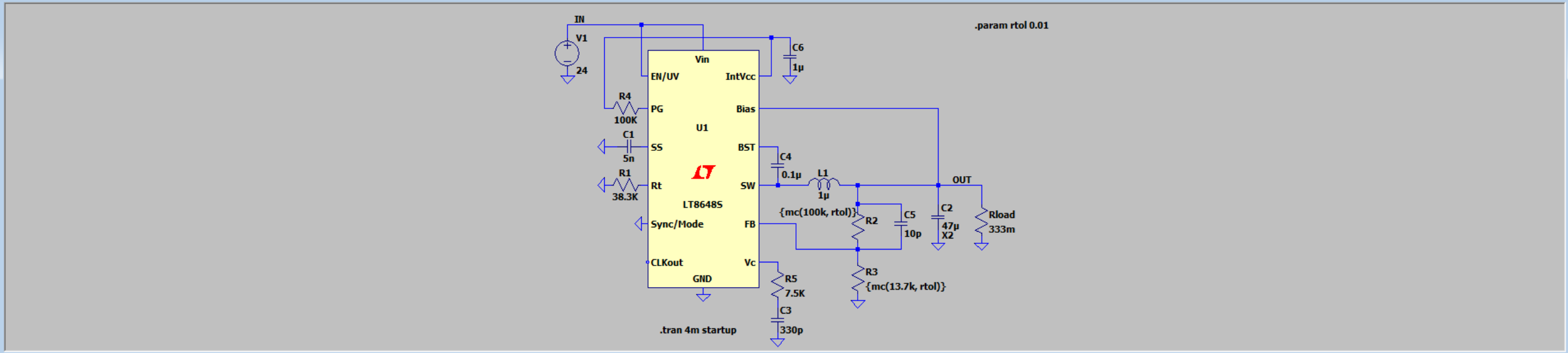
File Edit Hierarchy View Simulate Tools Window Help

LT8648S LT8648S

LT8648S



LT8648S

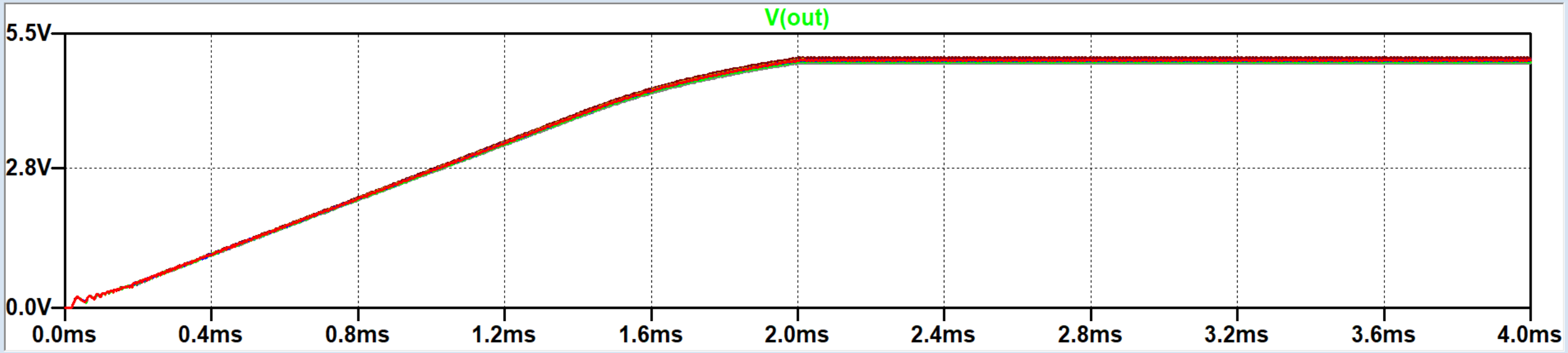


LTspice - LT8648S

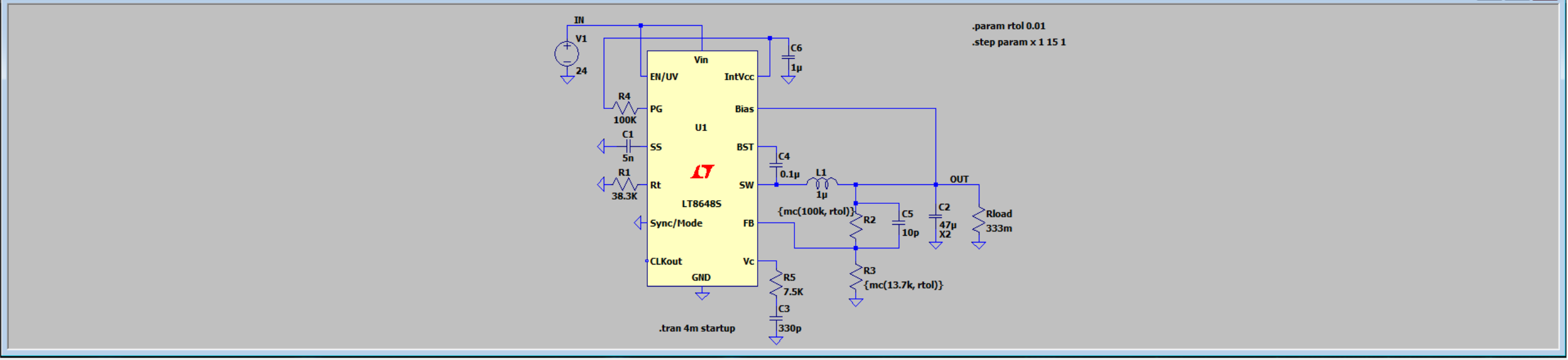
File Edit Hierarchy View Simulate Tools Window Help

LT8648S LT8648S

LT8648S



LT8648S

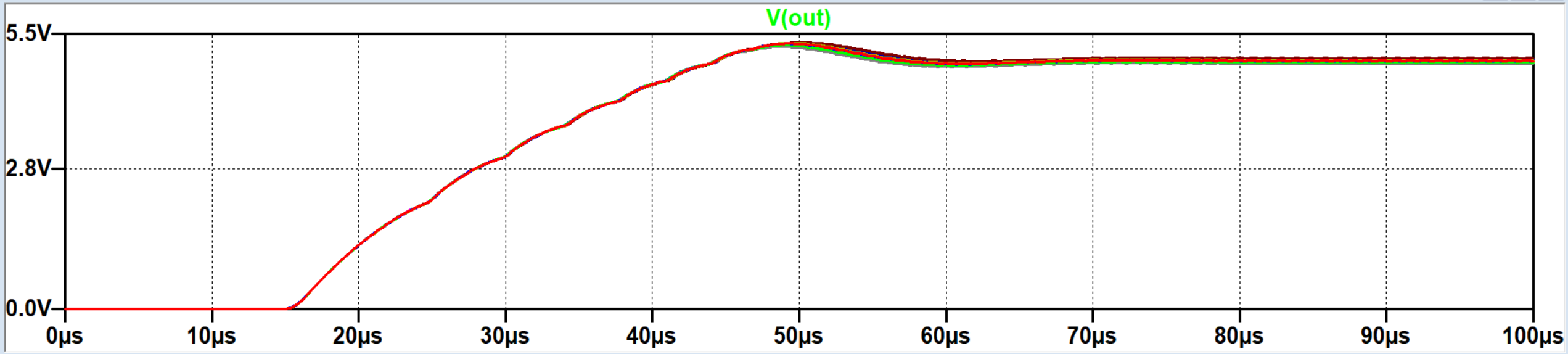


LTspice - LT8648S

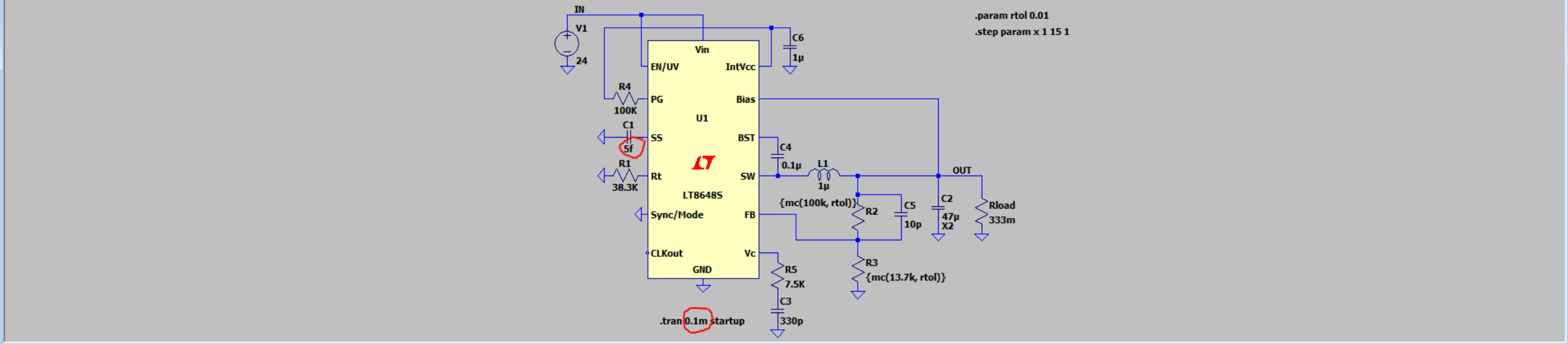
File Edit Hierarchy View Simulate Tools Window Help

LT8648S LT8648S

LT8648S



LT8648S



LTspice - LT8648S

File View Plot Settings Simulation Tools Window Help

LT8648S LT8648S

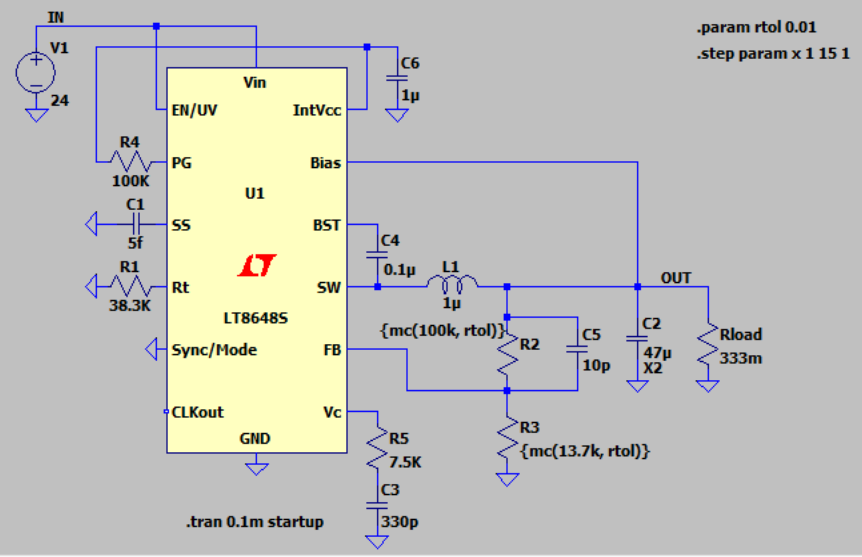
LT8648S

V(out)

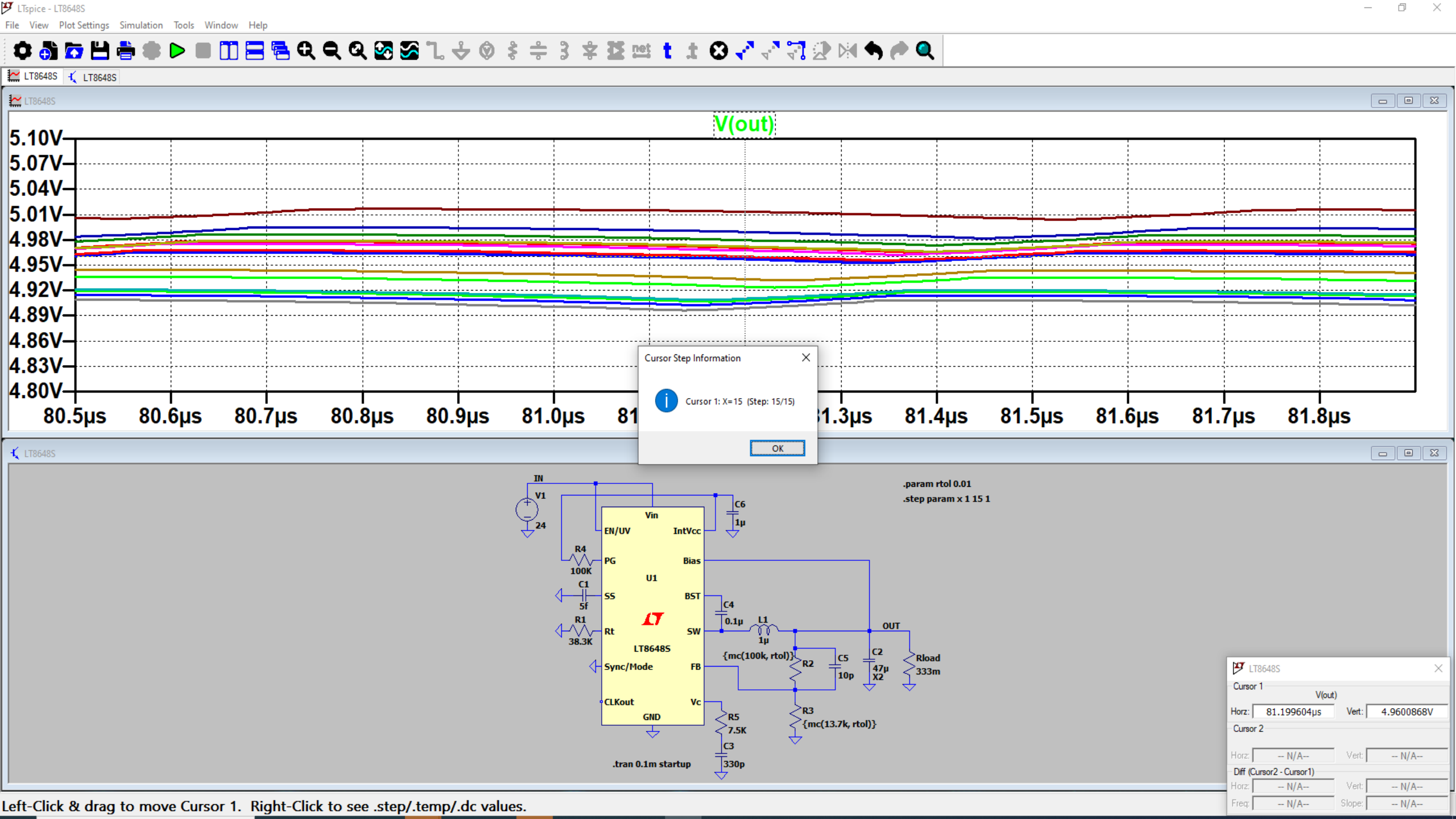
5.10V
5.07V
5.04V
5.01V
4.98V
4.95V
4.92V
4.89V
4.86V
4.83V
4.80V

80.5µs 80.6µs 80.7µs 80.8µs 80.9µs 81.0µs 81.1µs 81.2µs 81.3µs 81.4µs 81.5µs 81.6µs 81.7µs 81.8µs

LT8648S



Right-Click to manually enter Horizontal Axis Limits

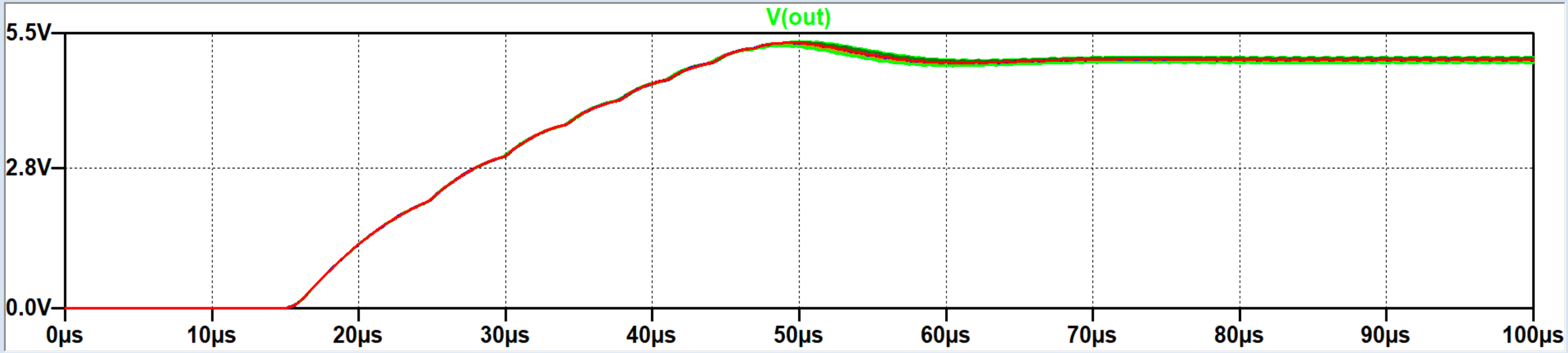

LTspice - LT8648S
File View Plot Settings Simulation Tools Window Help
LT8648S
LT8648S
V(out)
5.10V
5.07V
5.04V
5.01V
4.98V
4.95V
4.92V
4.89V
4.86V
4.83V
4.80V
80.5µs
80.6µs
80.7µs
80.8µs
80.9µs
81.0µs
81.3µs
81.4µs
81.5µs
81.6µs
81.7µs
81.8µs
Cursor Step Information
Cursor 1: X=15 (Step: 15/15)
OK
IN
V1
24
C6
1µ
Vin
EN/UV
IntVcc
R4
100K
PG
Bias
U1
C1
5f
SS
BST
C4
0.1µ
L1
1µ
R1
38.3K
Rt
SW
OUT
LT8648S
{mc(100k, rtol)}
R2
C5
10p
C2
47µ
X2
Rload
333m
Sync/Mode
FB
R3
{mc(13.7k, rtol)}
CLKout
Vc
R5
7.5K
GND
C3
330p
.tran 0.1m startup
.param rtol 0.01
.step param x 1 15 1
LT8648S
Cursor 1
V(out)
Horz: 81.199604µs
Vert: 4.9600868V
Cursor 2
Horz: -- N/A--
Vert: -- N/A--
Diff (Cursor2 - Cursor1)
Horz: -- N/A--
Vert: -- N/A--
Freq: -- N/A--
Slope: -- N/A--
Left-Click & drag to move Cursor 1. Right-Click to see .step/.temp/.dc values.

LTspice - LT8648S

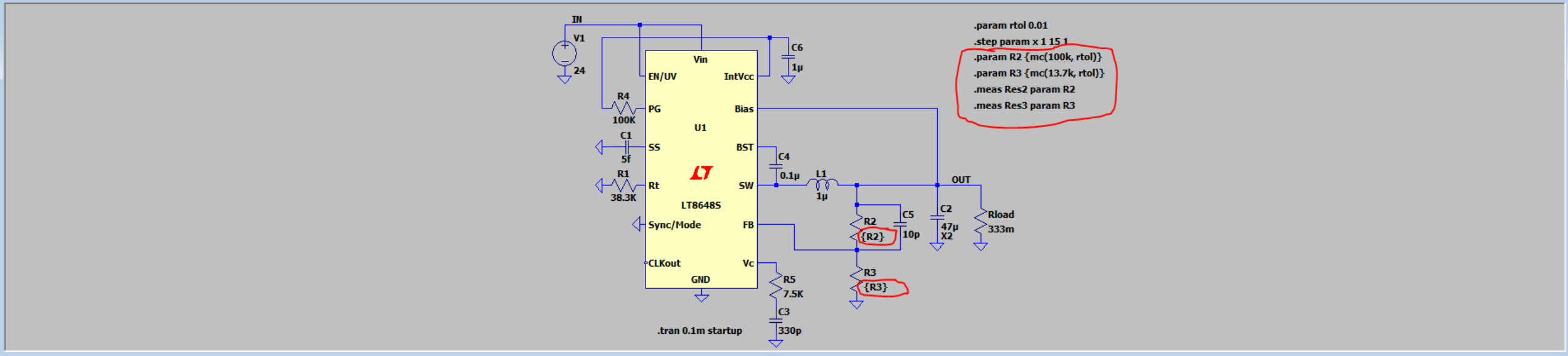
File Edit Hierarchy View Simulate Tools Window Help

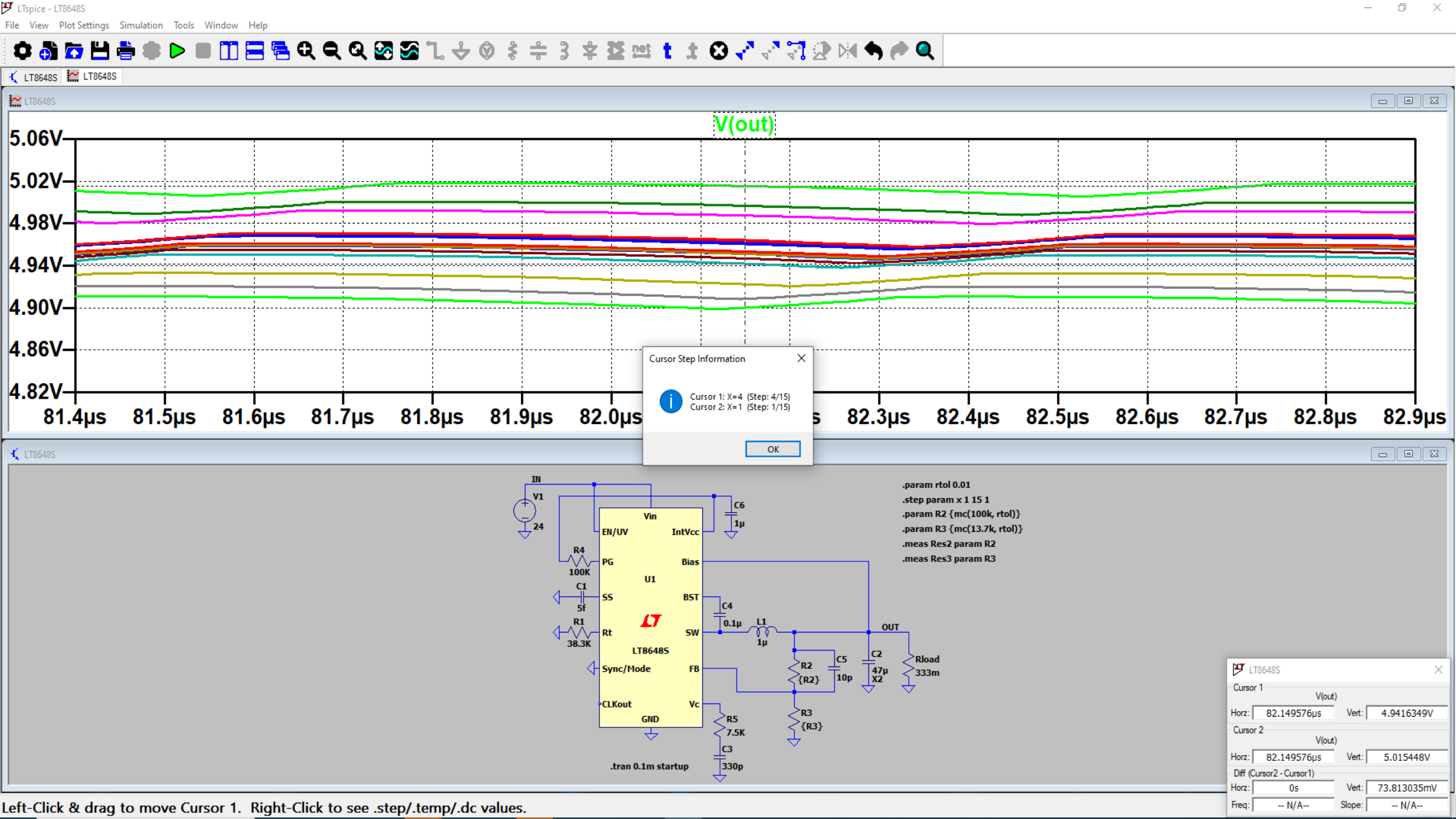
LT8648S LT8648S

LT8648S



LT8648S



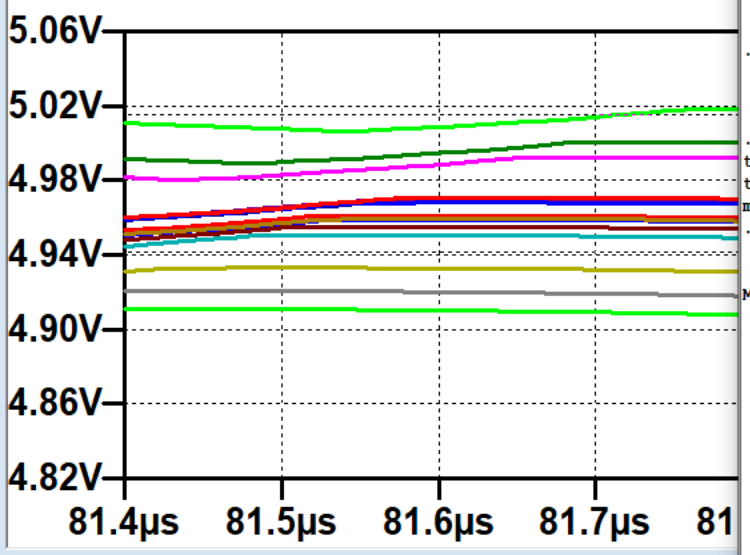

LTspice - LT8648S
File View Plot Settings Simulation Tools Window Help
LT8648S
LT8648S
V(out)
5.06V
5.02V
4.98V
4.94V
4.90V
4.86V
4.82V
81.4µs 81.5µs 81.6µs 81.7µs 81.8µs 81.9µs 82.0µs 82.3µs 82.4µs 82.5µs 82.6µs 82.7µs 82.8µs 82.9µs
Cursor Step Information
Cursor 1: X=4 (Step: 4/15)
Cursor 2: X=1 (Step: 1/15)
OK
IN
V1
24
C6
1µ
Vin
EN/UV
IntVcc
R4
100K
PG
Bias
U1
C1
5f
SS
BST
C4
0.1µ
L1
1µ
R1
38.3K
Rt
SW
OUT
LT8648S
Sync/Mode
FB
R2
{R2}
C5
10p
C2
47µ
X2
Rload
333m
CLKout
Vc
R3
{R3}
GND
R5
7.5K
C3
330p
.tran 0.1m startup
.param rtol 0.01
.step param x 1 15 1
.param R2 {mc(100k, rtol)}
.param R3 {mc(13.7k, rtol)}
.meas Res2 param R2
.meas Res3 param R3
LT8648S
Cursor 1
V(out)
Horz: 82.149576µs
Vert: 4.9416349V
Cursor 2
V(out)
Horz: 82.149576µs
Vert: 5.015448V
Diff (Cursor2 - Cursor1)
Horz: 0s
Vert: 73.813035mV
Freq: -- N/A--
Slope: -- N/A--
Left-Click & drag to move Cursor 1. Right-Click to see .step/.temp/.dc values.

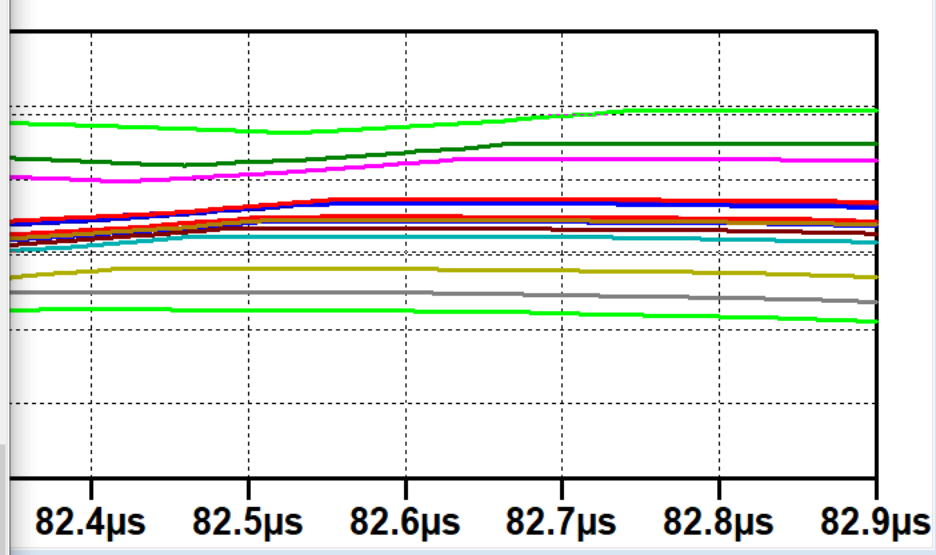
LTspice - LT8648S

File Edit Hierarchy View Simulate Tools Window Help

LT8648S LT8648S

LT8648S





LT8648S

m rtol 0.01
param x 1 15 1
m R2 {mc(100k, rtol)}
m R3 {mc(13.7k, rtol)}
s Res2 param R2
s Res3 param R3

oad
33m

SPICE Output Log: C:\Users\FDostal\AppData\Local\LTspice\examples\Applications\LT8648S.log

```
.step x=11


.step x=12


.step x=13


.step x=14
tnom = 27
temp = 27
method = modified trap
.step x=15


Measurement: res2
  step             r2
     1             100127
     2             99959.7
     3             100493
     4             100027
     5             99728.9
     6             99891.4
     7             99755.8
     8             100214
     9             99704.2
    10             100605
    11             100453
    12             99284.7
    13             99419.2
    14             100999
    15             99594.6

Measurement: res3
  step             r3
     1             13563.3
     2             13723.3
     3             13788.5
     4             13757.7
     5             13588
     6             13833.9
     7             13565.4
     8             13727.9
     9             13686.5
    10             13777.6
    11             13803
    12             13710.8
    13             13799.3
    14             13836.1
    15             13635.9

Total elapsed time: 22.236 seconds.
```

LT8648S

Cursor 1
V(out)
Horz: 82.149576µs Vert: 4.9416349V

Cursor 2
V(out)
Horz: 82.149576µs Vert: 5.015448V

Diff (Cursor2 - Cursor1)
Horz: 0s Vert: 73.813035mV
Freq: -- N/A-- Slope: -- N/A--

LTspice - LT8648S

File Edit Hierarchy View Simulate Tools Window Help

LT8648S LT8648S

SPICE Output Log: C:\Users\FDostal\AppData\Local\LTspice\examples\Applications\LT8648S.log

```
.step x=11


.step x=12


.step x=13


.step x=14
tnom = 27
temp = 27
method = modified trap
.step x=15


Measurement: res2
  step             r2
     1             100127
     2             99959.7
     3             100493
     4             100027
     5             99728.9
     6             99891.4
     7             99755.8
     8             100214
     9             99704.2
    10             100605
    11             100453
    12             99284.7
    13             99419.2
    14             100999
    15             99594.6

Measurement: res3
  step             r3
     1             13563.3
     2             13723.3
     3             13788.5
     4             13757.7
     5             13588
     6             13833.9
     7             13565.4
     8             13727.9
     9             13686.5
    10             13777.6
    11             13803
    12             13710.8
    13             13799.3
    14             13836.1
    15             13635.9

Total elapsed time: 22.236 seconds.
```

Find Ctrl+F

Plot .step'ed .meas data

Close

LT8648S

5.06V 5.02V 4.98V 4.94V 4.90V 4.86V 4.82V

81.4µs 81.5µs 81.6µs 81.7µs 81

82.4µs 82.5µs 82.6µs 82.7µs 82.8µs 82.9µs

m rtol 0.01
param x 1 15 1
m R2 {mc(100k, rtol)}
m R3 {mc(13.7k, rtol)}
s Res2 param R2
s Res3 param R3

oad
33m

LT8648S

Cursor 1
V(out)
Horz: 82.149576µs Vert: 4.9416349V

Cursor 2
V(out)
Horz: 82.149576µs Vert: 5.015448V

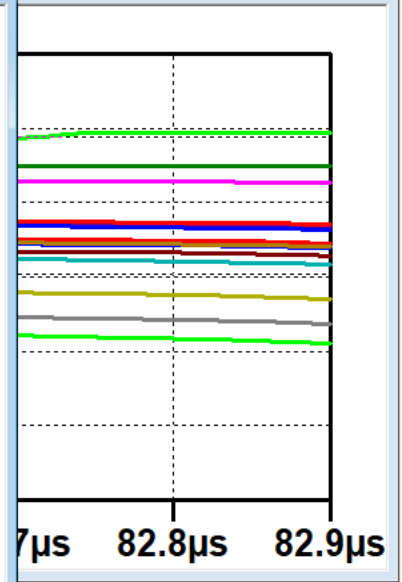
Diff (Cursor2 - Cursor1)
Horz: 0s Vert: 73.813035mV
Freq: -- N/A-- Slope: -- N/A--

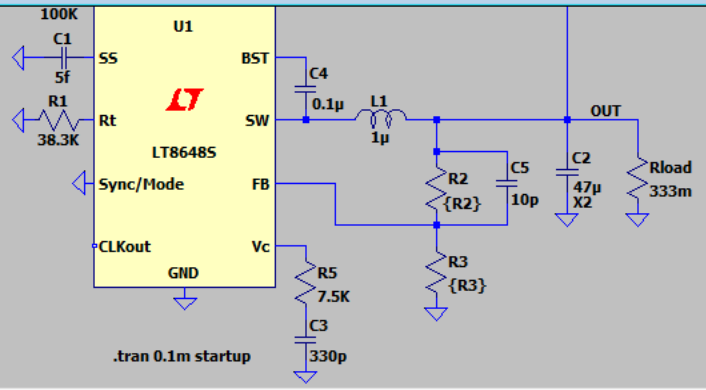
LTspice - LT8648S.log

File View Plot Settings Simulation Tools Window Help

LT8648S LT8648S LT8648S.log

LT8648S.log





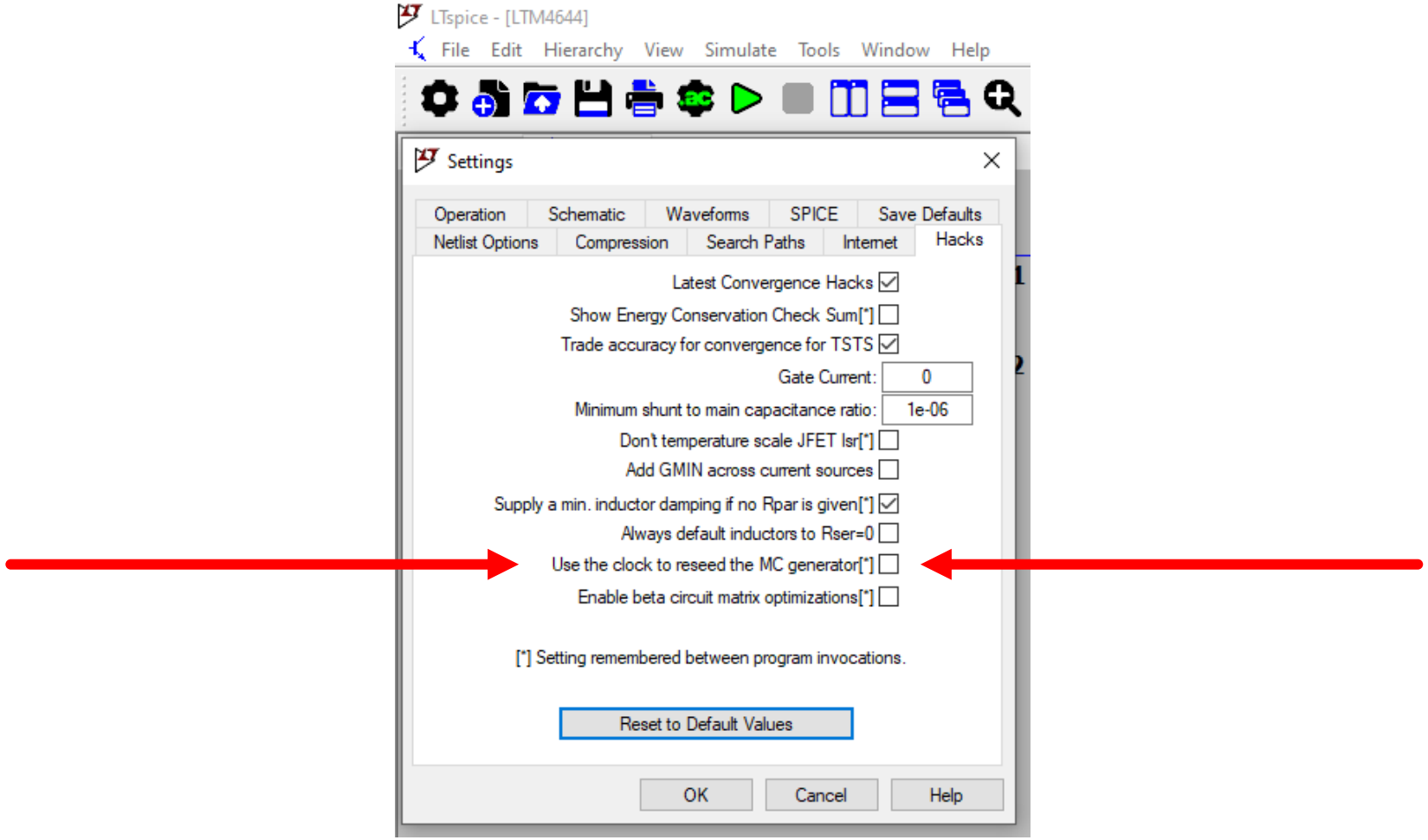
LT8648S

Cursor 1
V(out)
Horz: 82.149576µs Vert: 4.9416349V

Cursor 2
V(out)
Horz: 82.149576µs Vert: 5.015448V

Diff (Cursor2 - Cursor1)
Horz: 0s Vert: 73.813035mV
Freq: -- N/A-- Slope: -- N/A--

Setting LTspice to use real random numbers



Reason for fixed 'random' pattern: While developing a simulation, it is very useful when repeated runs of the simulation behave the same. This way you can compare them and observe the differences resulting from changes YOU made to the schematic or to other parameters.

Simulating behavior of a power switch

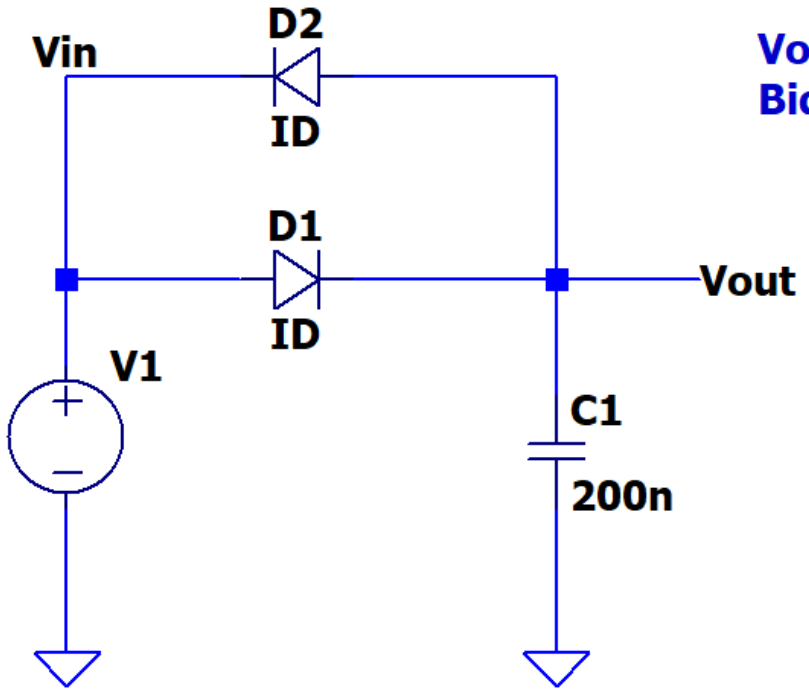
analog.com

Voltage Source Current Limited

Usecase:
Simulating output Stages to drive capacitive loads like MOSFETS, IGBTs, SIC

C1=Load

For proper adjustment to a real Gate-Drive you may add a serial resistance to V1.



Voltage Source with Current Limit Bidirectional

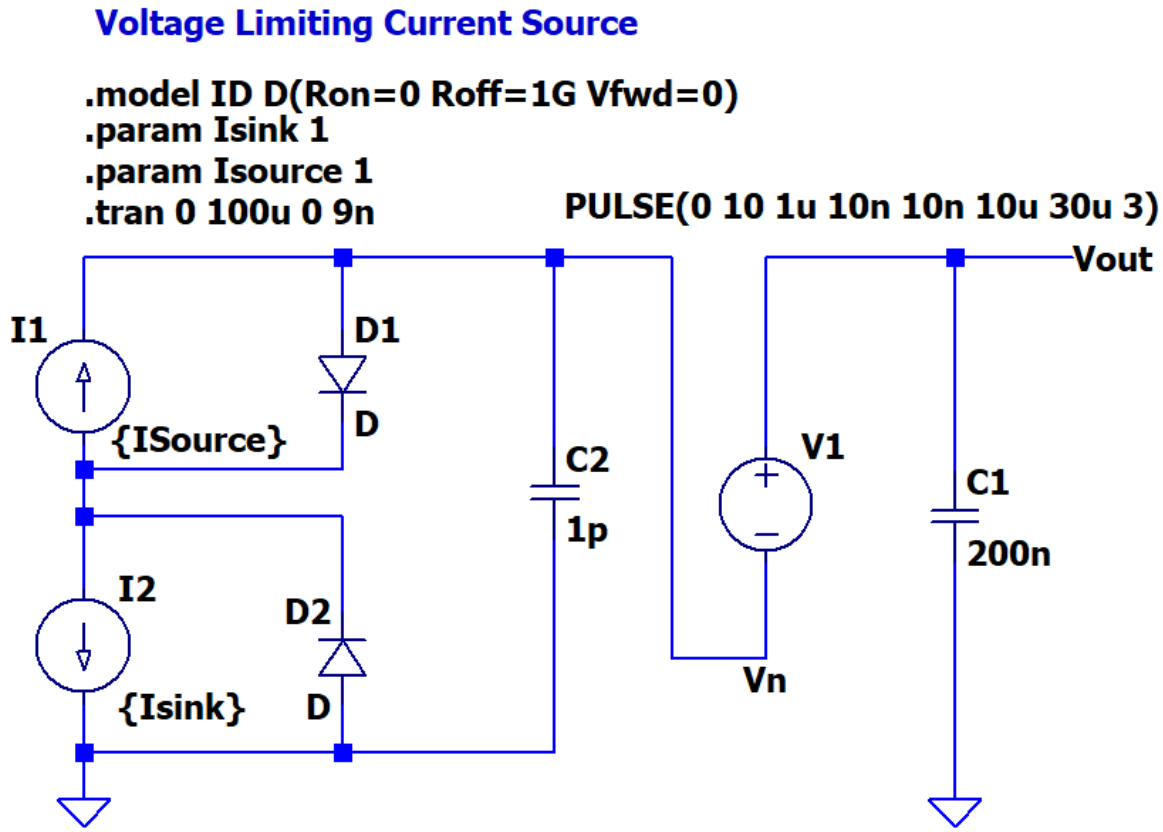
```
PULSE(0 10 1u 1n 1n 10u 20u 3)
.tran 100u

.model ID D(Ron=0 Roff=1G Vfwd=0 Ilimit=1)
```

Voltage Limiting Bidirectional I-Source

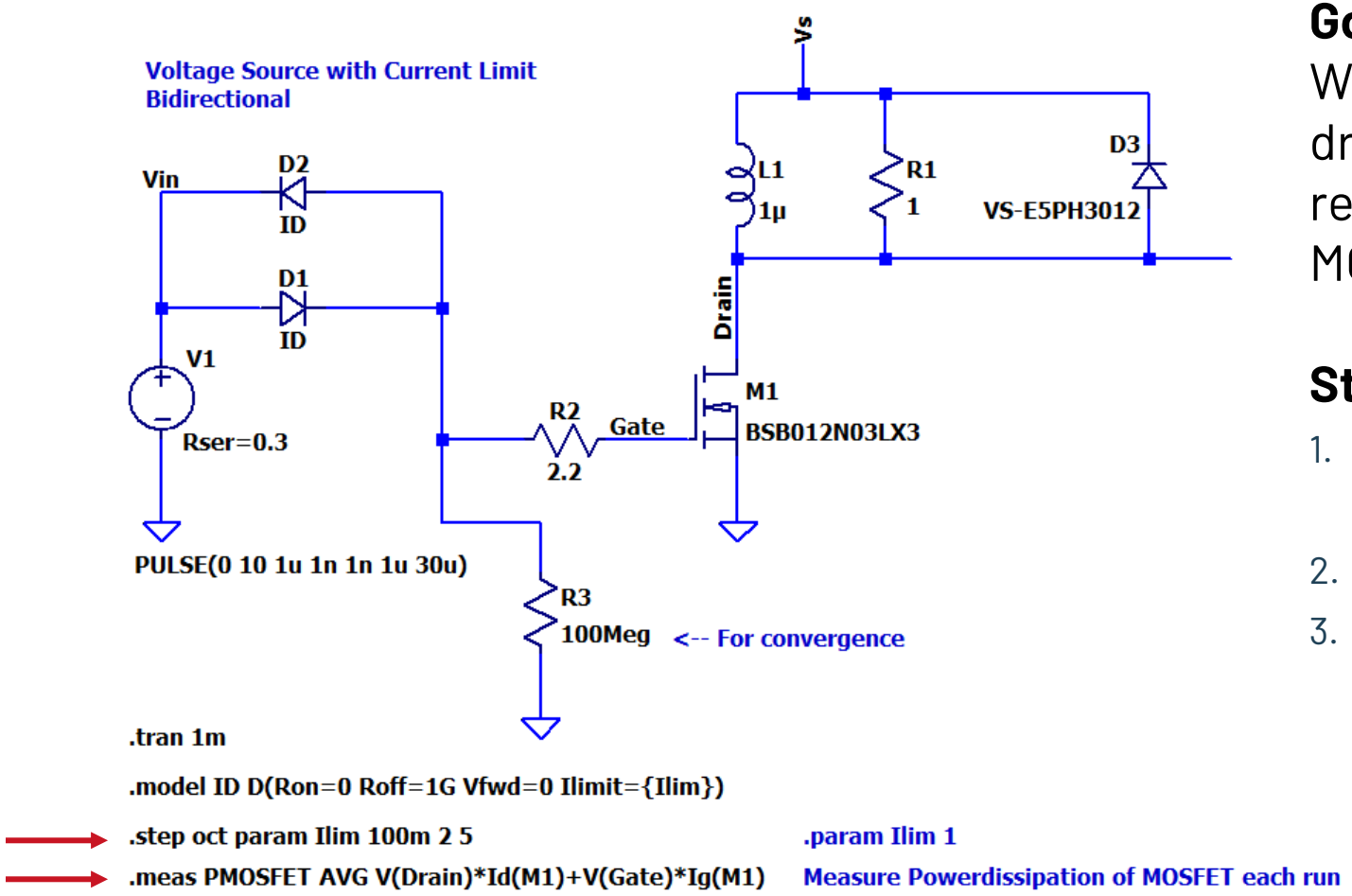
Use case: Driving power transistors (MOSFETS, SIC, IGBT) with large capacitive Gate.

D1, D2 are ideal Diodes
C2 is used to prevent high voltage spikes on Vn
C1 = Load

For proper adjustment to a real Gate-Drive you may add a serial resistance to V1.



Test Circuit to find minimum Drive-Current



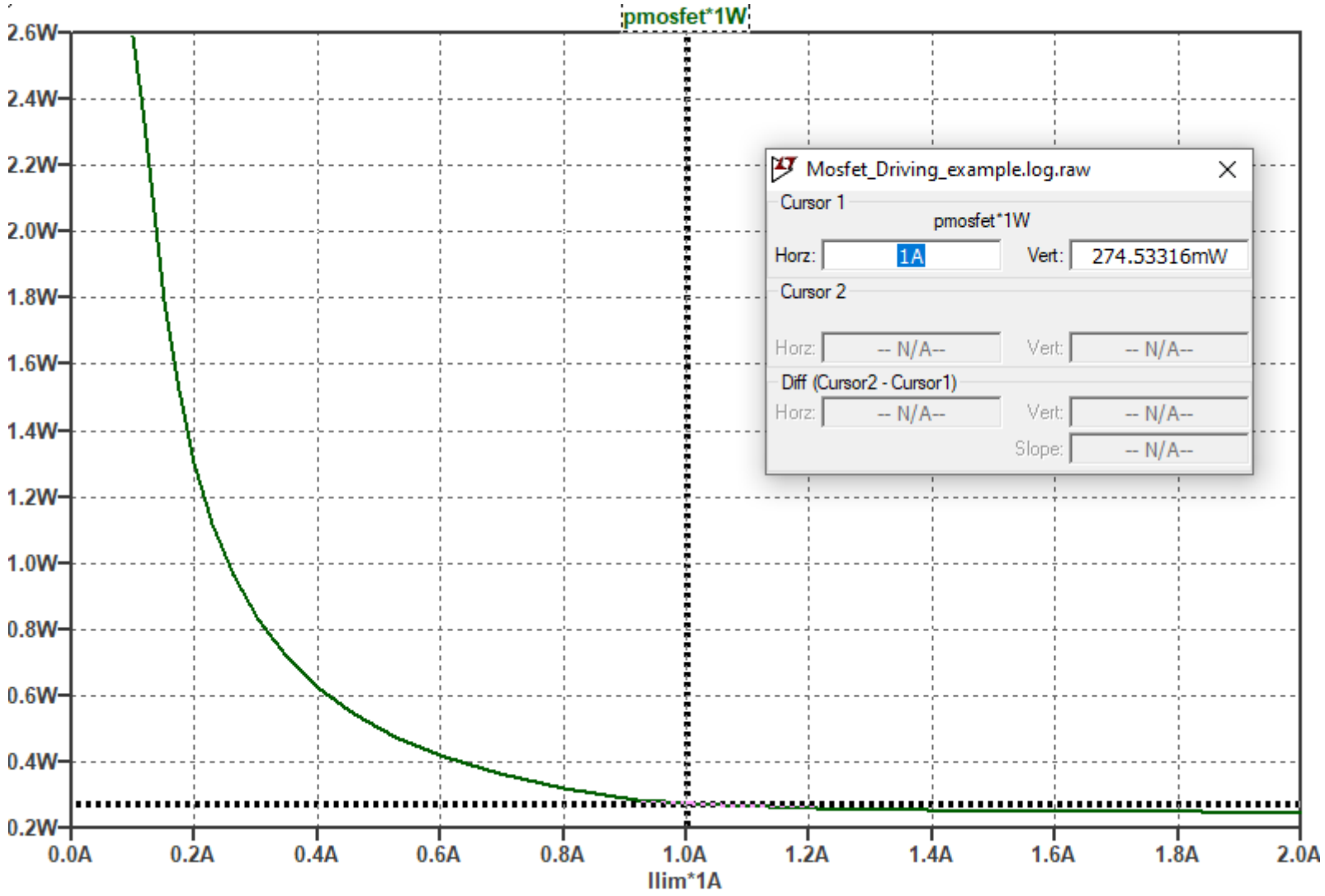
Goal:

We like to determine beyond which drive current there is no further reduction in the power-loss of the MOSFET

Steps to prepare:

1. Stepping the drive-current (`Ilim`)
2. Measure Power-Loss
3. Plot stepped meas. data
   1. Ctrl-L (log-file)
   2. Right click: Plot stepped measurement data

Powerdissipation at different Drive Current



Powerloss of the MOSFET vs. Drive peak current

Conclusion:
Beyond 1A peak drive current, there is no further reduction in Power-loss of the MOSFET.

AHEAD OF WHAT'S POSSIBLE

analog.com

ANALOG DEVICES