Index

To see the syntax of each of these three passive components in detail, refer to the corresponding chapters.

4.3 Procedures to access common or complex component models

In LTspice XVII, each component is represented by a common model.

A model is the mathematical representation of a component's behaviour. This representation is made on the basis of an equivalent schematic consisting of basic components (resistors, capacitors, inductors and sources). Each basic component is characterised by one or more numerical values which accurately define its behaviour.

LTspice XVII offers, for a certain number of components, **several models** of increasing complexity to represent more accurately the particular features of each component. It is down to you to choose the model that best satisfies the requirements of your system or its environment.

Let us look at an example. A resistor can be represented by a common model, with a limited resistance value, potentially the tolerance of this value and the power that this resistor can dissipate. In general, this is enough but if you wish to test your system as a function of temperature, you will need the temperature coefficient of this resistor. To introduce this new parameter, you must necessarily use a more complete resistor model which has this temperature coefficient as a parameter. On the other hand, it is most likely that this more complete model has many other parameters quantifying other aspects of resistor operation. If you are not interested in these characteristics or do not know their values, you do not need to enter them; LTspice XVII will replace these missing values with average values called "default parameters".

- **First procedure: the common model.** This procedure involves entering standard values of a component represented by its common model.
- **Second procedure: the more complete models.** This procedure lets you access less standard values. You can enter these more numerous parameters in the **attribute editor**.

Each component has its own models and dedicated parameters. In a subsequent chapter, we have dedicated an entire section to the detailed description of each component's models.

4.3.1 Modifying a component's current values

Certain components have a common model that offers the ability to use a quick-input window such as that of a resistor (see this section).

Two examples of a monolithic power MOSFET:

- `M1 Nd Ng Ns 0 MyNMOSFET`
  `.model MyNMOSFET NMOS (KP=.001)`
- `M1 Nd Ng Ns Nb MyPMOSFET`
  `.model MyPMOSFET PMOS (KP=.001)`

This model uses the reserved keywords NMOS and PMOS to specify that a monolithic MOSFET uses an N or P channel.

Another generic VDMOS sub-model is used for the double vertical power distribution MOSFET (refer to the next section).

CAUTION

MOSFETs include many **generic sub-models**, and this makes them quite difficult to understand. Each **generic sub-model** is adapted to the **MOSFET** component it represents. The choice of sub-model is made by the manufacturer during the SPICE model production phase. It is automatically recognised by LTspice based on the parameters entered in the model, and the process is fully transparent to the user.

The **generic sub-model** of the monolithic **MOSFET** has three or four output terminals according to its reference: **Nd, Ng, Ns,** and **Nb** respectively for the **drain**, the **gate**, the **source** and the **substrate** (or **bulk**).

L and **W** are the channel length and width in meters.

Ad and **As** are the drain and source diffusion areas respectively, in square meters.

If any of the four parameters **L, W, Ad** or **As** is not specified, the default value is automatically added, as with all other generic sub-models.

Pd and **Ps** are the **drain** and **source** junction perimeters, in metres.

Nrd and **Nrs** are the equivalent number of squares of the drain and source diffusions respectively; these values are the multipliers of the sheet resistance **Rsh** in the model.

Pd and **Ps** have a default value of 0, whereas **Nrd** and **Nrs** are equal to 1.

Off indicates an initial condition on a DC simulation device. Initial conditions can be specified with the command **.ic = VDS, VGS, VBS** when the **UIC** option is active (transient simulation). This occurs when a **.tran** simulation starts with a value other than **t = 0**.

20 SOAtherm: thermal model for MOSFET with heatsink

20.1 SOAtherm for LTspice XVII

The ability to insert or remove SMPS cards when hot requires the use of a MOSFET, which has both a **low R_{on} resistance** and a safe operating area (**SOA**), especially for high-temperature transients. In fact, it is common to find **MOSFETs** optimised for **low R_{on} resistance**, but which have proved unsuitable for use with high-temperature transients (**SOA**).

For applications with high-temperature transients (**Hot Swap**) that allow a card to be directly inserted and removed hot from a backplane with safety, the **SOAtherm model** is a valuable tool. The safe operating area (SOA) of the **MOSFET** is guaranteed by the manufacturers for **Hot Swap** applications (high-temperature transients). Twenty-four MOSFET models of this type are available in the LTspice XVII database.

A thermal model called SOAtherm was developed based on the **Cauer model** by **Dan Eddleman**, an engineer specialised in analogue electronics who has more than 15 years of experience at Linear Technology as designer of integrated circuits, manager of the integrated circuit design centre of Singapore and application engineer.

The **SOAtherm model** is included in LTspice XVII. In circuit simulations, it makes it possible to verify that the **safe operating area (SOA)** of a MOSFET is not exceeded, thus avoiding many design errors which cause failures in pulse circuits and SMPSs.

Several examples illustrate the advantages of using the SOAtherm model to verify the correct use of MOSFETs.

20.2 How to use the SOAtherm model with LTspice XVII

If you installed LTspice XVII before 18 January 2019, you have the symbol **SOAtherm-NMOS** on the list of available models, as was the case in LTspice IV, but don't be surprised to find that it doesn't work, because it was deactivated on this date. On the other hand, if you installed LTspice XVII after this date, this model no longer appears on the list of available symbols because new methods have been implemented to achieve SOAtherm functionality.

Today, with LTspice XVII, the procedure for **activating the SOAtherm model** is radically different. The functionality and the result of the simulations are exactly the same as they were in LTspice IV, but we must change our working habits to continue to take advantage of the full power of the **SOAtherm model**.

A circuit designer can use the **SOAtherm model** to verify that the **SOA** of a MOSFET is suitable for one of the many applications involved. The **SOA** corresponds to the **temperature safe operating area of a MOSFET chip**.

No additional heat sink or model of thermal dissipation through the copper surface of an electronic card is required to use this model. However, in certain applications, particularly during power transients of more than 10 milliseconds, it may be desirable to add a means of removing heat. This is why the **SOAtherm** model has two other models which can be used to either add a manufactured heat sink when the power is high (**SOAtherm-HeatSink**) or use a copper-plated surface of the PCB as a heat sink when the power is low (**SOAtherm-PCB**).