ICeGaN® in LLC Converters

Unlocking performance beyond Silicon for Next-Gen Power Systems

October 2025

AGENDA

CGD

GaN vs SI

ICeGaN®

LLC and the benefits of ICeGaN

3kW LLC experimental results

Dare to innovate
differently

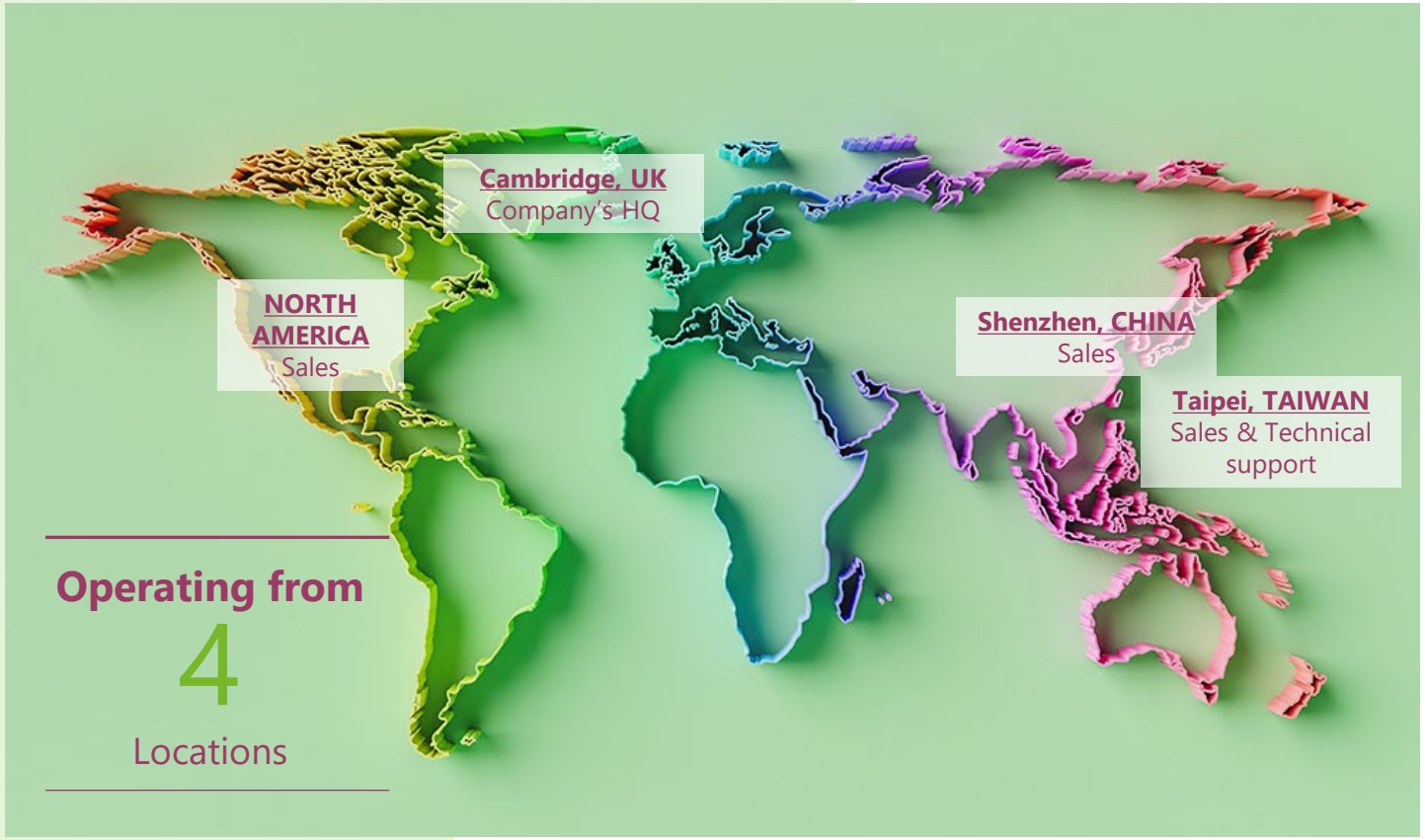
Cambridge GaN Devices at a Glance

The Fast-paced Scaleup Making Green Electronics Possible

A fabless semiconductor company designing, developing and commercialising **energy-efficient GaN-based power transistors and ICs**

Innovation
110+
Patent applications

Employees
~60
And growing...



Operating from
4
Locations

Company Focus

MOBILE and OTHER CONSUMER SMPS

Reduced weight/size

More efficient

Fast charging

INDUSTRIAL

Volume reduction

High efficiency

DATACENTRE and TELECOM

OPEX reduction by >10%

CAPEX reduction up to 10%

AUTOMOTIVE

Faster charging

50% smaller OBCs and DCDC converters

Why GaN?

GaN outperforms Si

Silicon
14
Si
28.086

Traditional Si-based Devices

SLOW SWITCHING

HIGHER DRIVING LOSS

LESS SUSTAINABLE

Less Efficient, Less Sustainable

Gallium	Nitrogen
31	7
Ga	**N**
69.723	14.007

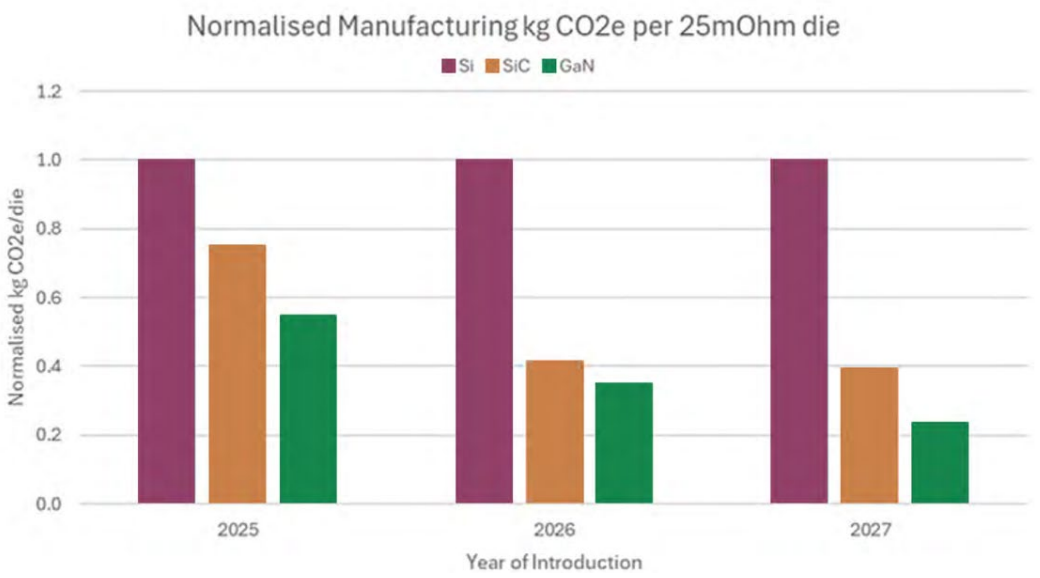
GaN-based Devices

- ✓ **LOWER Q_{OSS}**
- ✓ **10x LOWER Q_G**
- ✓ **NO REVERSE RECOVERY (Q_{RR})**
- ✓ **LOWER R_{DSON} PER AREA**
- ✓ **MORE SUSTAINABLE MANUFACTURING PROCESS**

More Efficiency, More Power Density

Why GaN?

More Sustainable



GaN HEMT fabrication avoids high-carbon-emission processes

- × No High-energy implantation
- × No Long thermal diffusion
- × No Gate oxidation

GaN devices achieve **lower per-device carbon emissions** compared

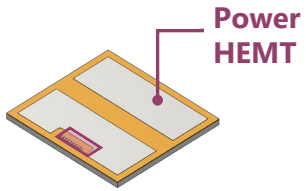
Why ICeGaN ?

What makes ICeGaN Devices Beneficial for High-Power LLC?

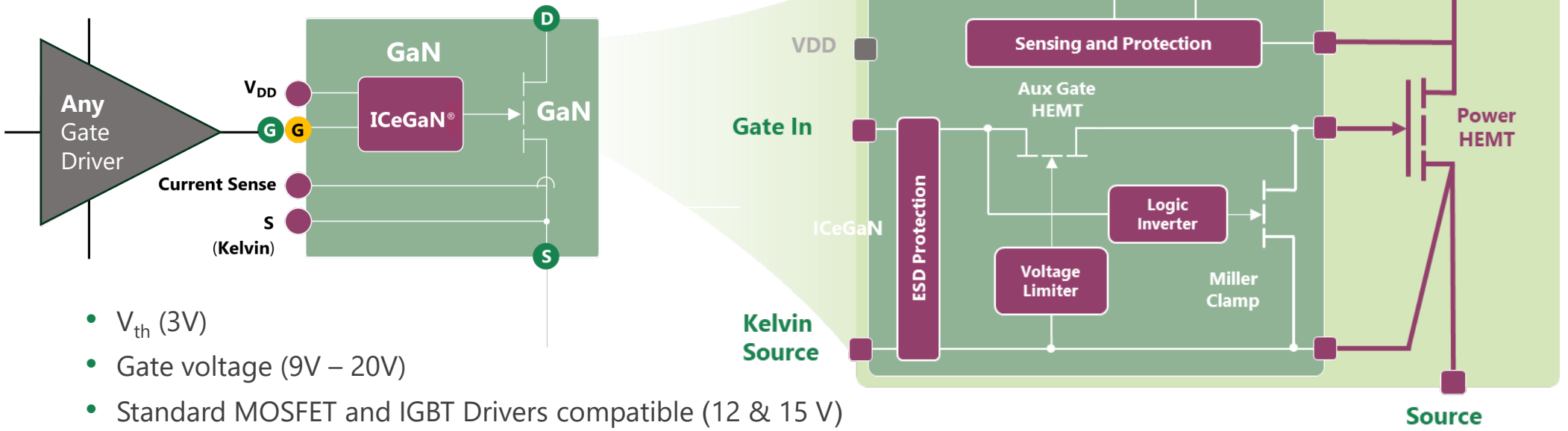
1. GaN switch **faster than Si**
2. Achieve **higher power density** by increasing the switching frequency.
3. ICeGaN is GaN HEMT that is **easy to drive**

ICeGaN Power IC

All-In-One Monolithic GaN Chip



ICeGaN (Integrated Circuit eMode GaN)



- V_{th} (3V)
- Gate voltage (9V – 20V)
- Standard MOSFET and IGBT Drivers compatible (12 & 15 V)
- Internal Miller Clamp for high dv/dt and 0 V turn-off
- Improved robustness – 2 kV ESD all pins, high transient rating on the gate
- Withstands >80 V dynamic voltage overshoots on the gate pin

ICeGaN Product Portfolio for High Power

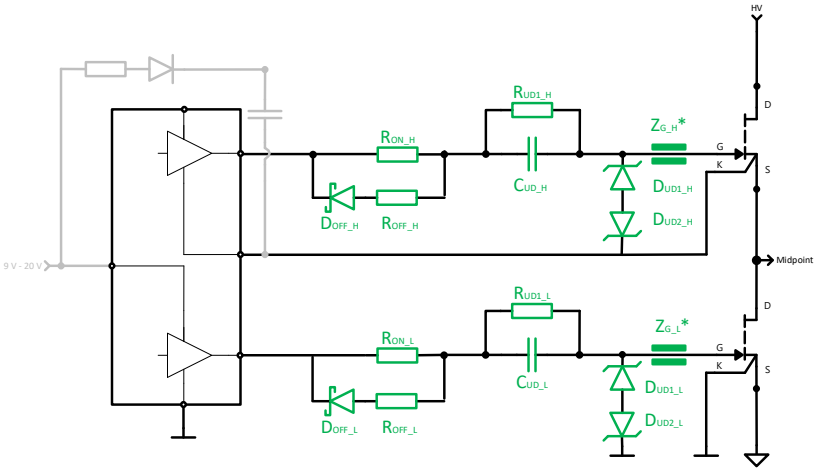
	PN	$R_{DS(on)}$ typ (mΩ)	Current Rating (A)	Package	Features	Preferred Gate Driver	Status
P2 Series	CGD65C025SP2	25	60	BHDFN-9-1	ICeGaN	Any MOSFET, IGBT or SiC driver	Available Today
	CGD65C055SP2	55	27	BHDFN-9-1	ICeGaN		Available Today
H2 Series	CGD65A055SH2	55 mΩ	27	DFN 8x8	ICeGaN		Available Today
	CGD65A130SH2	130 mΩ	12	DFN 8x8	ICeGaN		
	CGD65B130SH2	130 mΩ	13	DFN 5x6	ICeGaN		
	CGD65B240SH2	240 mΩ	7	DFN 5x6	ICeGaN		

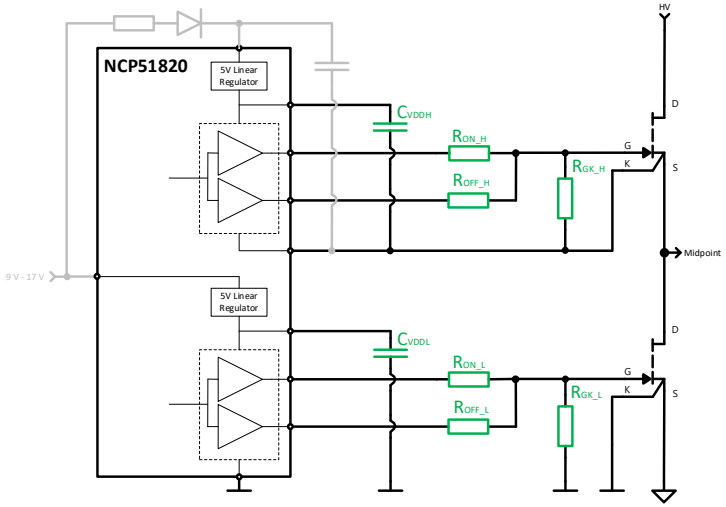
BHDFN:
Enhanced Thermal Bottom-Side Cooled

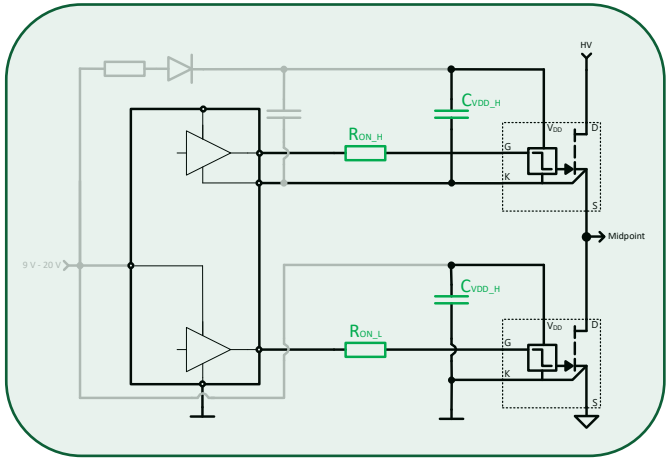
DFN 8x8 & 5x6
Bottom-Side Cooled

ICeGaN is Easy to Drive

Comparison with Discrete GaN







Discrete GaN Driving

- ↓ Require **negative drive** to avoid unwanted turn-on events during start-up, dynamic load, overload or light-load conditions where soft-switching operation might lose soft-switching operation
- ↓ **Poor voltage regulation on the high side** (additional clamping/LDO required) using bootstrap

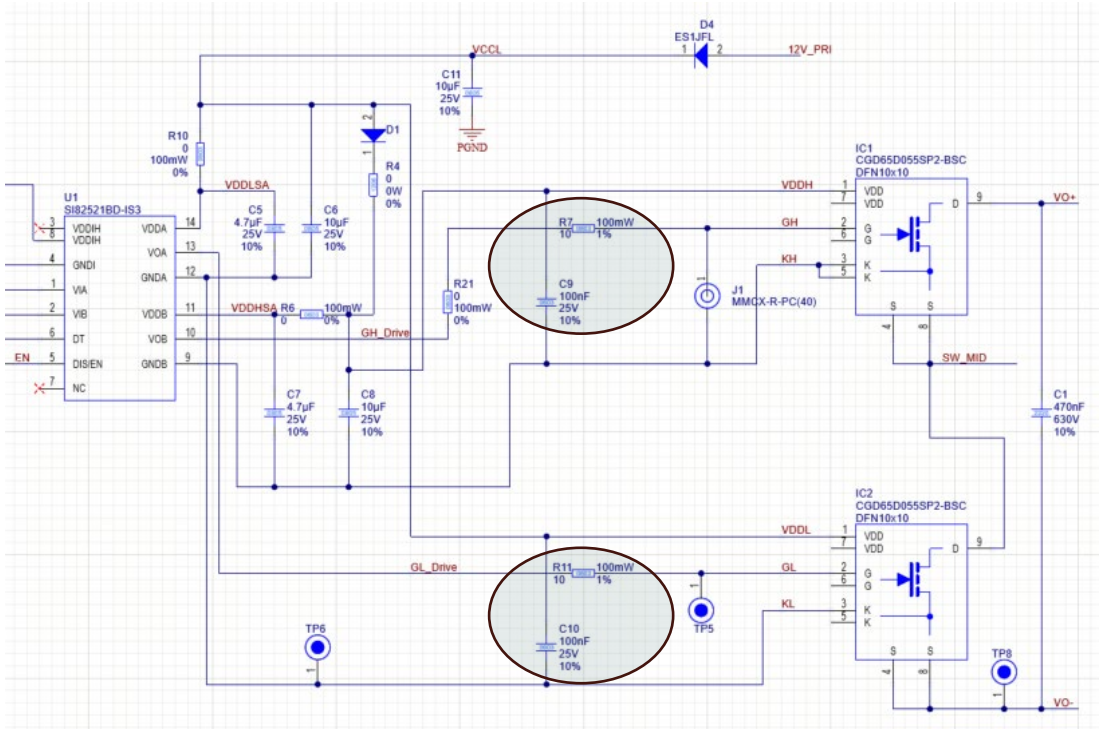
- ↓ More external components
- ↓ More complexity
- ↓ Tighter PCB layout
- ↓ Higher reverse voltage Vsd
- ↓ More switching losses
- ↓ Possible UVLO issue (not always)

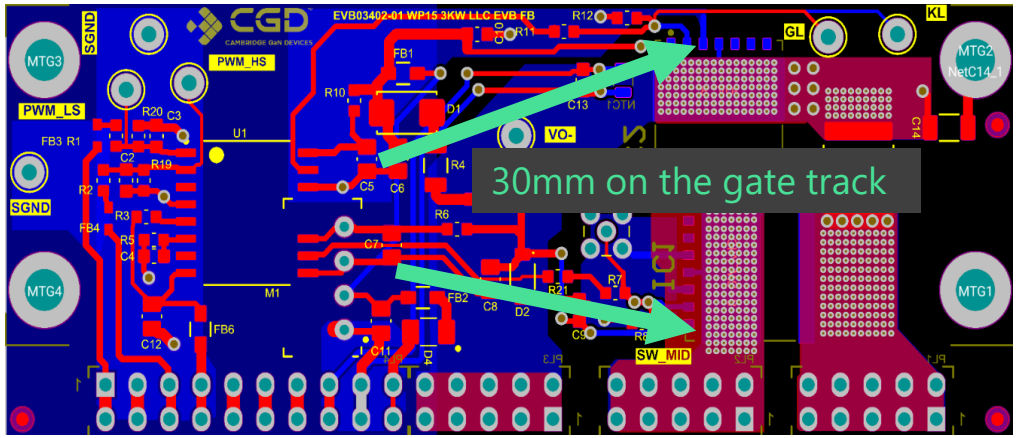
ICeGaN Driving

- ✓ **Only 1 resistor and 1 capacitor per device**
- ✓ **No negative drive No need for specific gate drive voltage**
- ✓ **More PCB space for cooling the device**
- ✓ **Bootstrap no OVP or UVLO issues**

ICeGaN is Easy to Drive

Example



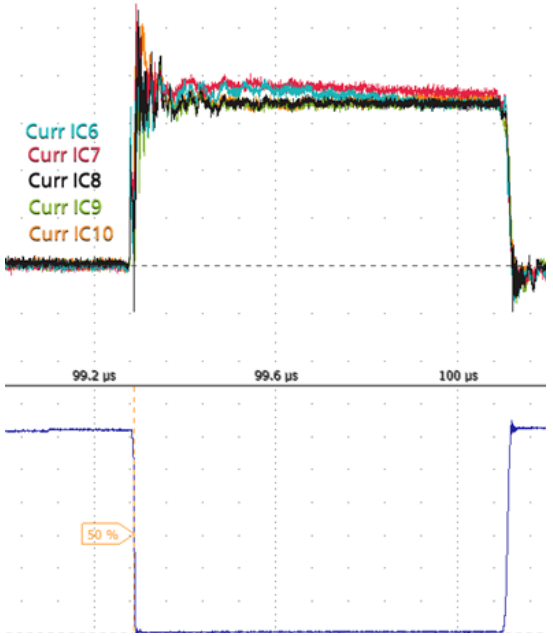


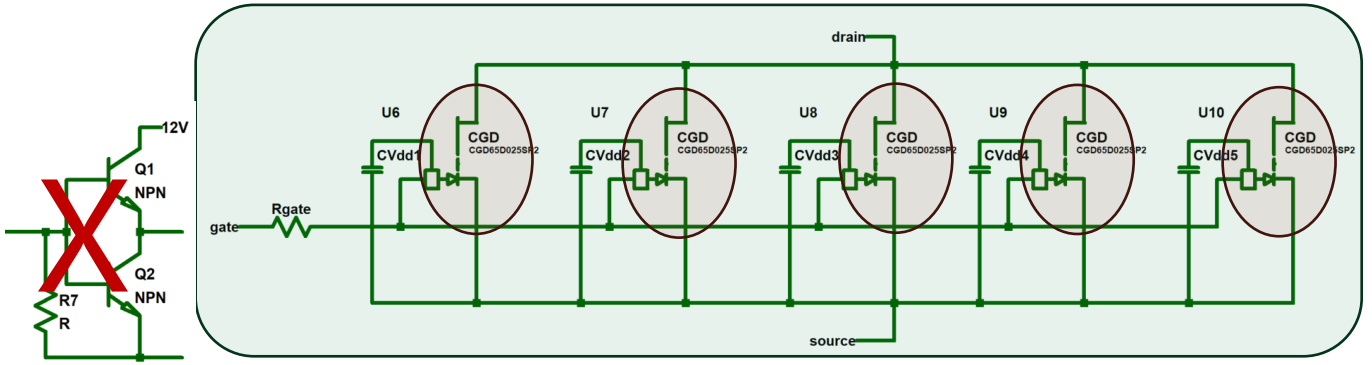
HB daughter card for LLC converter: 400V/50V – 3kW – 570 kHz

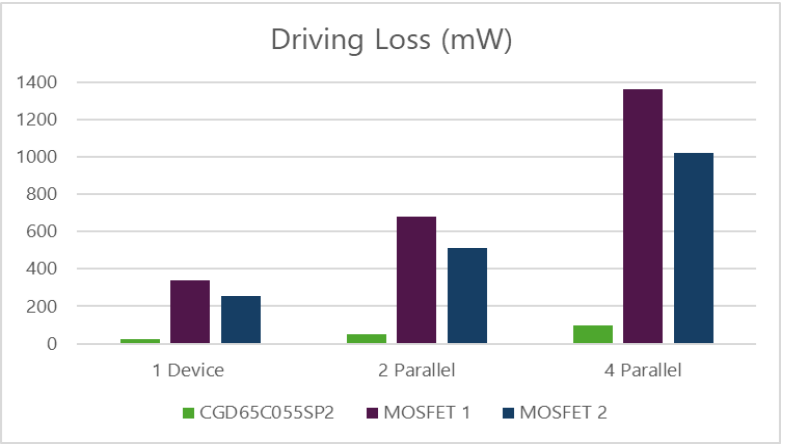
ICeGaN is Easy to Drive

Easy to Drive + Easy to Parallel

10 times lower Low Q_G and Paralleling ICeGaN is easy and straightforward





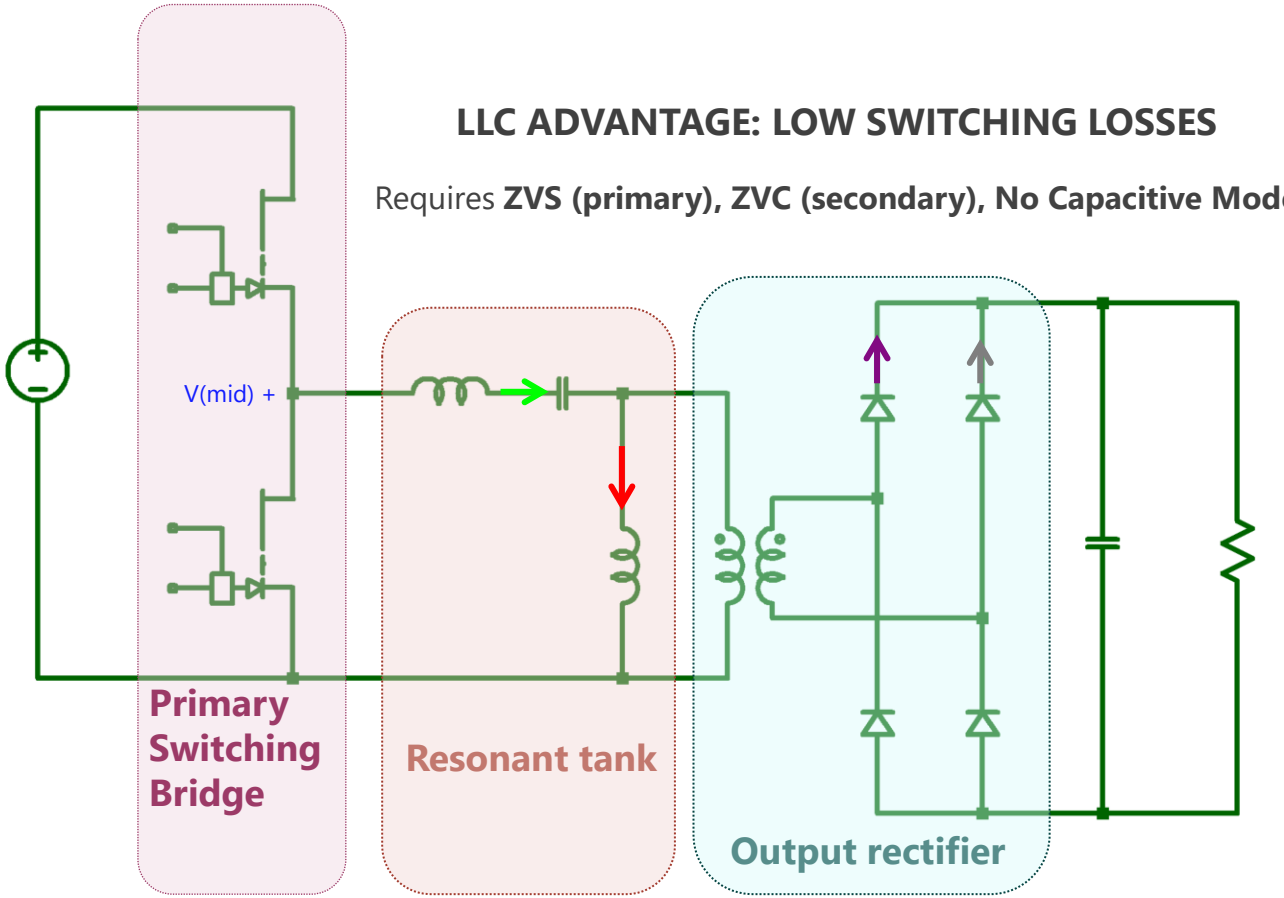


$$P_G = Q_G \cdot V_G \cdot f_{SW}$$

For high power and high frequency applications driving is easy, no extra additional components

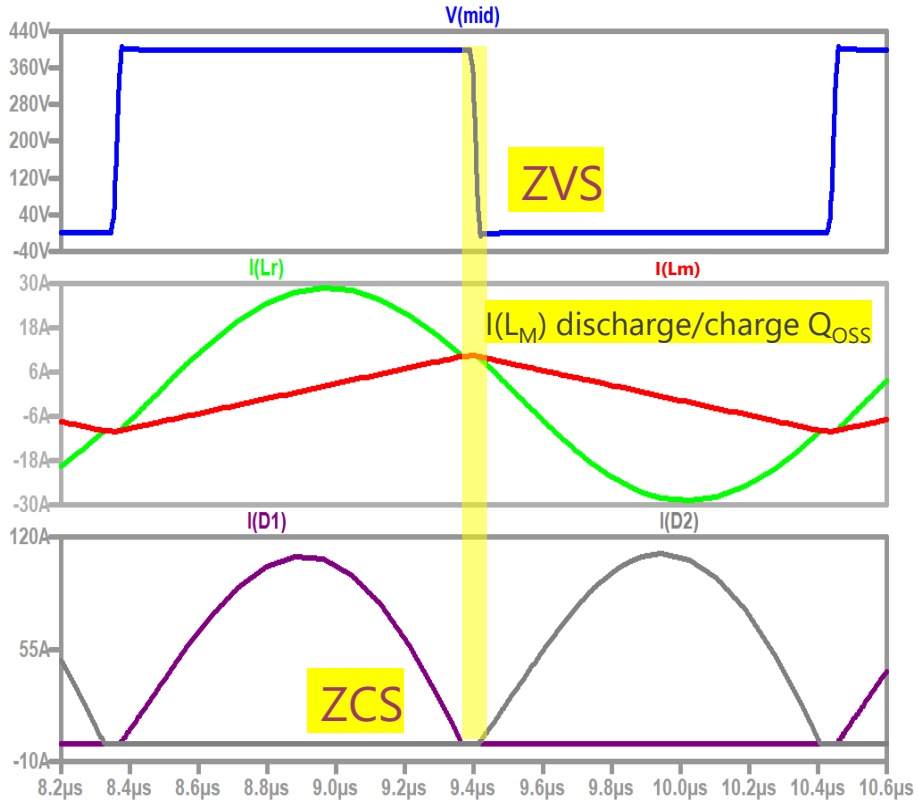
LLC

Fundamental principle



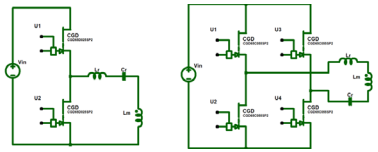
LLC ADVANTAGE: LOW SWITCHING LOSSES

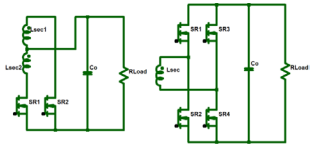
Requires **ZVS (primary), ZVC (secondary), No Capacitive Mode**

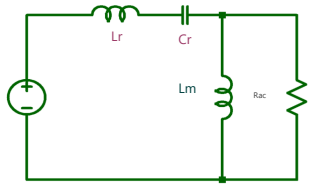


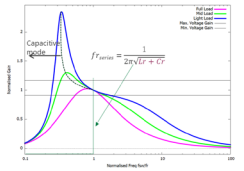
LLC

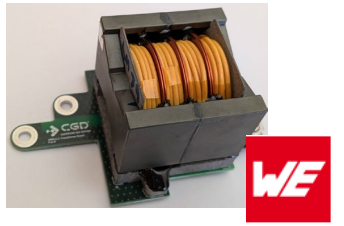
Design Process











Specs

Vin

Vout

Po

Size

Topology

Voltage Gain Range

Frequency optimization

Conduction Loss estimation -> (R_{DSON})

Select Transformer N ratio

Tank Design - FHA

Ensure ZVS -> Lm & C_{OTR}

Chose m ratio:
- Ensure Voltage gain
- Reduce Lr

Adjust Q voltage gain curve
- Ensure ZVS and control

Simulation

Magnetics

Core Size

Core Loss

Winding Loss

Maybe different design path and iterations depending on the specs and the targets

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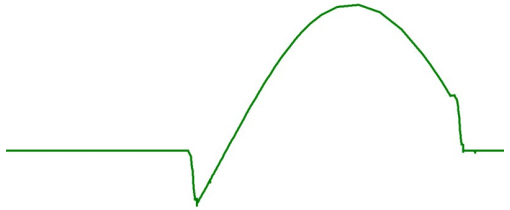
Estimate Switches Conduction Loss

With ZVS sorted conduction loss in the primary Bridge dominates $P_{cond} = I_{RMS}^2 \cdot R_{DSON}$



We can use a quick simulation to get the RMS through the switches

400V – 50V – 3kW Example

	CGD65C055SP2	CGD65C055SP2	CGD65C025SP2
Topology	Full-Bridge	Full-Bridge	Half-Bridge
R_{DSON} at 25 °C (mΩ)	55	25	25
R_{DSON} at 100 °C (mΩ)	110	50	50
I_{RMS} (A)	7	7	14
Conduction Loss (W)	5.39	2.45	9.8
Bridge Total Loss	22.8	11.1	19.6

Depending on your design goals, you might want to take in consideration the conduction loss to select the primary bridge topology

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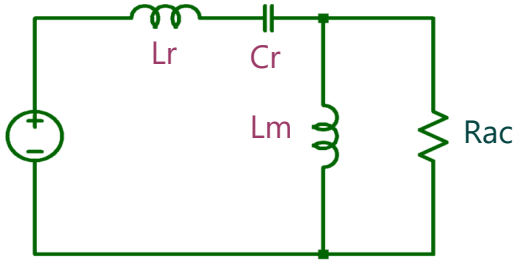
Resonant Tank Design

First Harmonic Approximation (FHA) Strong non-linear gain vs. voltage and load PWM averaging techniques don't work

FHA assumes pure sinusoidal currents



$$R_{AC} = \frac{8}{\pi} \cdot N \cdot R_{load}$$

$$fr = \frac{1}{2\pi\sqrt{Lr + Cr}}$$

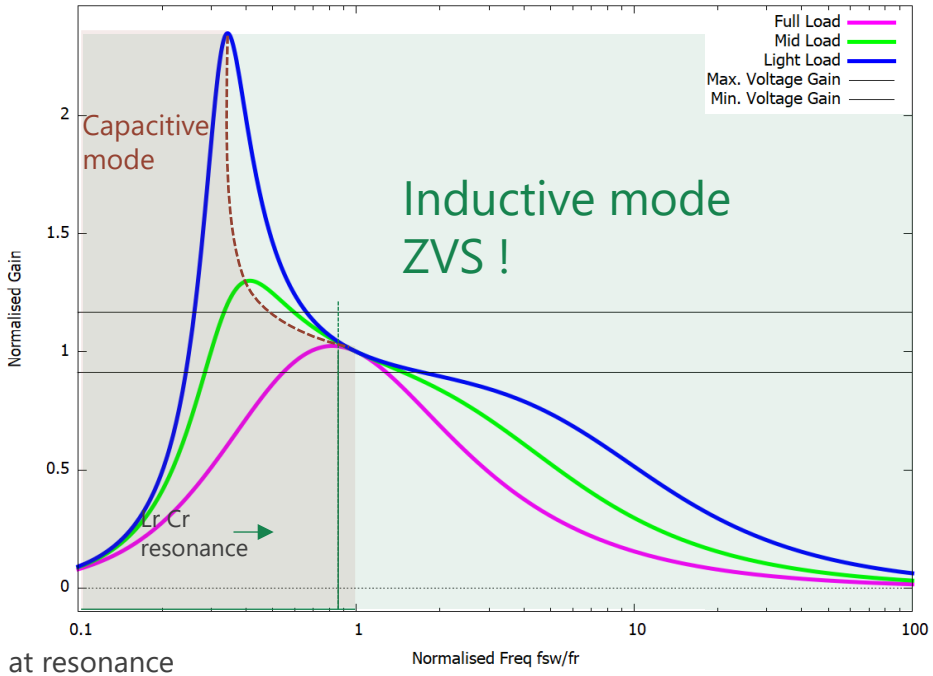
$$F_N = fSW/fR$$

$$Q = \sqrt{\frac{Lr}{Cr}} \cdot R_{AC}$$

$$m = \frac{Lr + Lm}{Lr}$$

Cannot be solved analytically but graphically

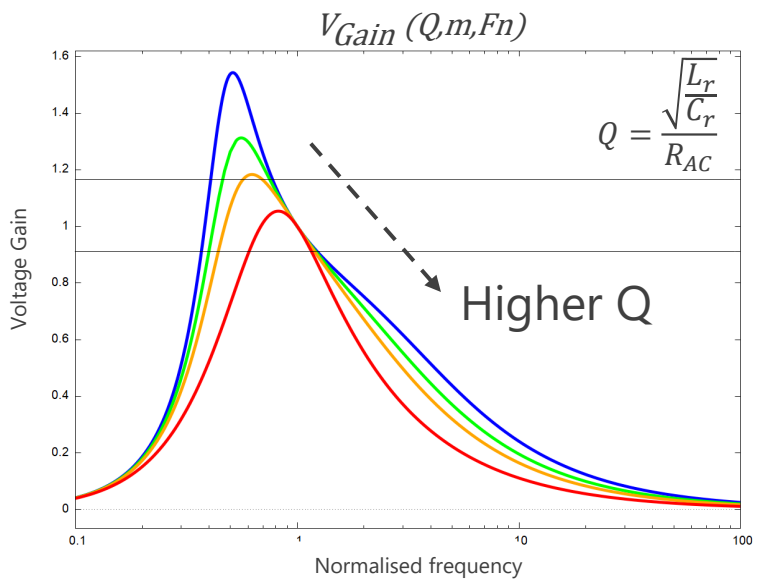
$$V_{Gain}(Q,m,Fn) = \frac{Vo(s)}{Vin(s)} = \frac{F_n^2 \cdot (m-1)}{\sqrt{(m \cdot F_n^2 - 1)^2 + F_n^2 (F_n^2 - 1)(m-1)^2 Q^2}}$$

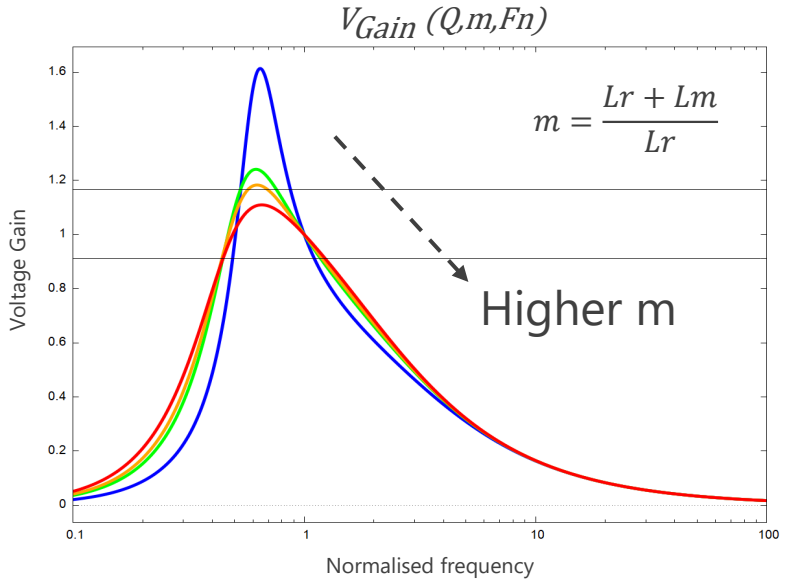


Best efficiency is at resonance

LLC

Increasing the resonant frequency…





You need to tune *Q* and *m* to operate at full load within the voltage gain range

Increasing the frequency and keeping *Q* and m constant, we can reduce L_r and L_m
We can adjust *Q* and m to increase L_m to reduce circulating current because GaN Q_{OSS} is much smaller -> less energy storage in the inductances

LLC

...can lead to smaller magnetics

$$E = \frac{1}{2}LI^2$$

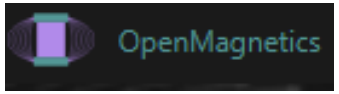
Inductor design is all about energy storage

$$B_s n A_e > L I_p$$ (*)

If we reduce L same keep n and B_S we can reduce A_e, hence size
If we reduce I_{MAG} we can also reduce I_p a bit too

Magnetic design is challenging and full of trade-offs. Ultimately depends on your design goals

- Smaller volume → less surface area for cooling
- Higher frequency → more core and ac losses

Iterate to find the balance between size, loss and thermal management 

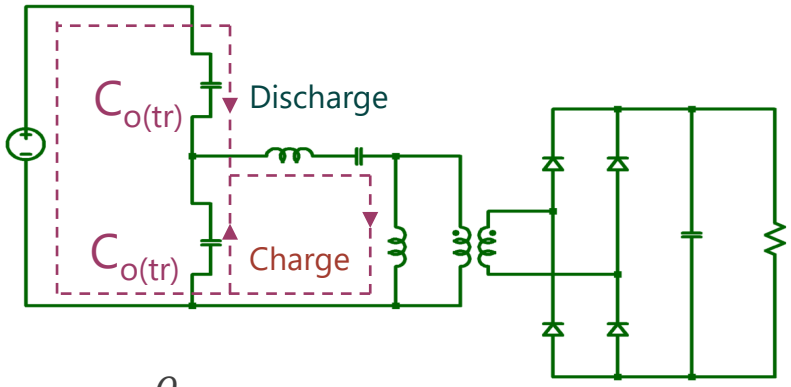
(*) https://ridleyengineering.com/design-center-ridley-engineering/39-magnetics/271-102-custom-inductors-%E2%80%93-one-design-equation.html

Prelimary tank design considerations

Lower $C_{O(TR)}$, Faster ZVS

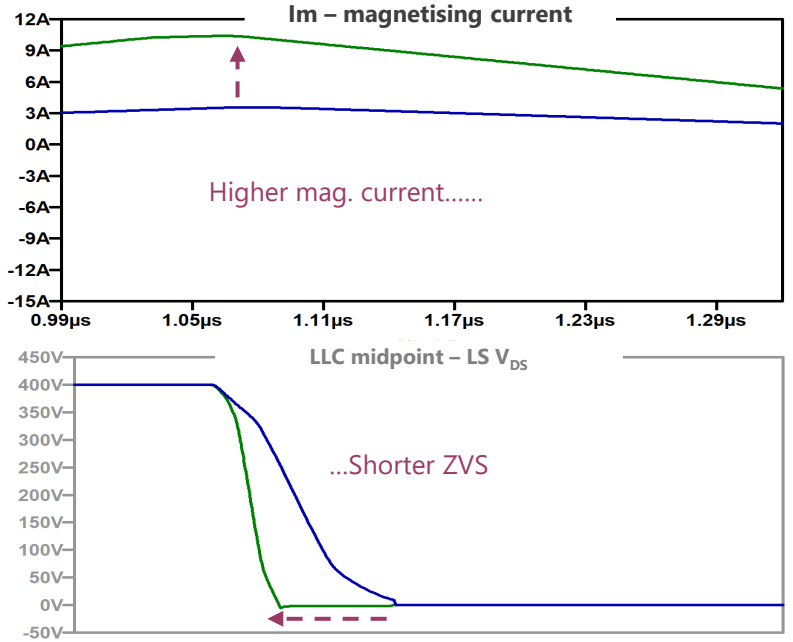
x Don't use C_{OSS} value to estimate ZVS

✓ **$C_{O(TR)}$ represents the drain-source charge (**usually at 400V**)**



$$C_{OTR} = \frac{Q_{OSS}}{V_{DS}}$$

$$dead\ timemin = 16 \cdot C_{OTR} \cdot f_{SW} \cdot L_M$$



Magnetizing current must be high enough to maintain ZVS and shorter dead times, but low enough to avoid excessive losses

ICeGaN

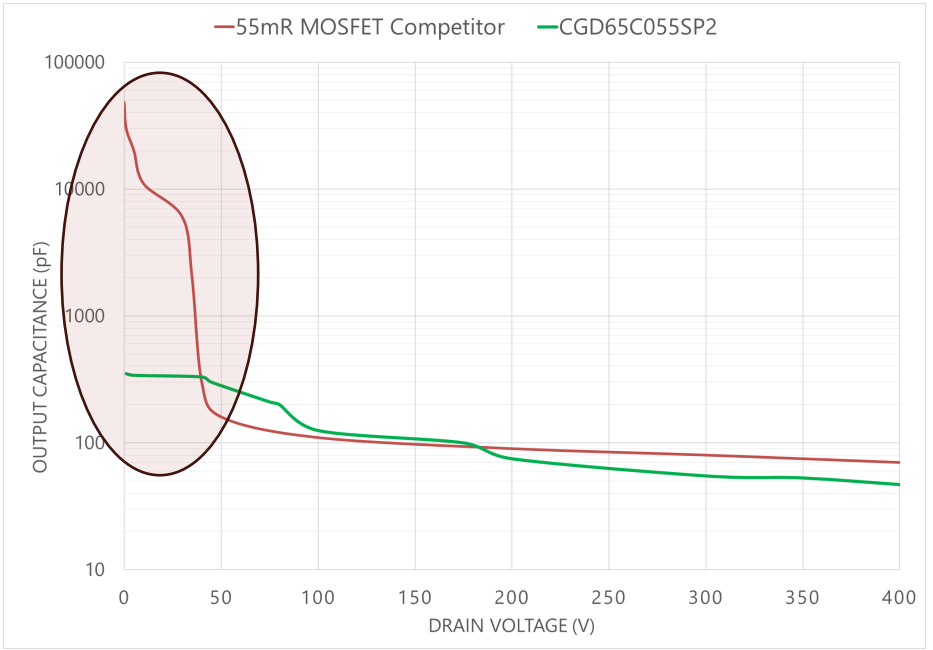
✓ Lower C_{OTR}
✓ Faster ZVS transitions
✓ No R_{DSON} compromise

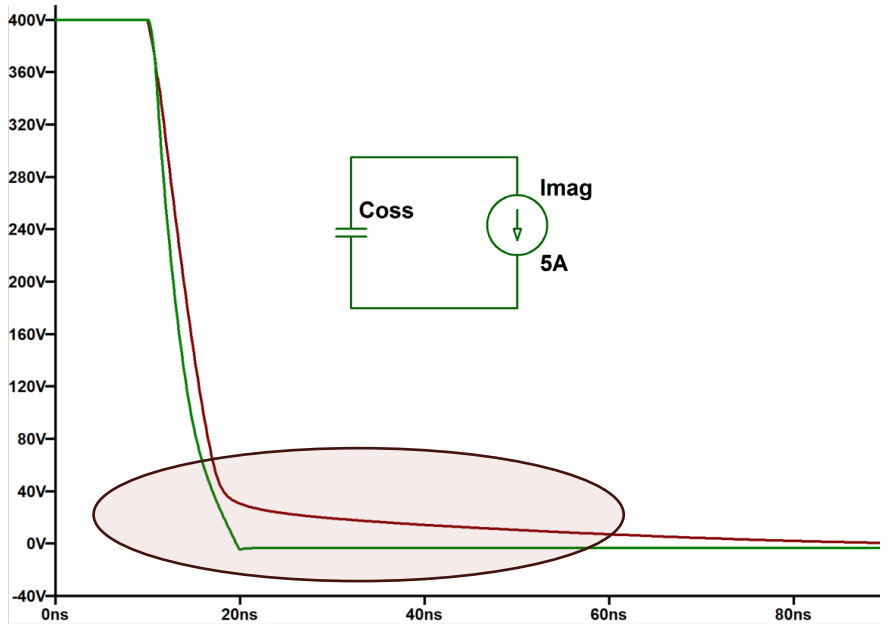
MOSFET has larger FOM: R_{DSON} x C_{OTR}

× Lower R_{DSON} MOSFETS selection limit by Q_{OSS}
× High C_{OTR} limit switching frequency operation
× More conduction losses and heat

Faster ZVS Transitions with ICeGaN

MOSFETS are Slower





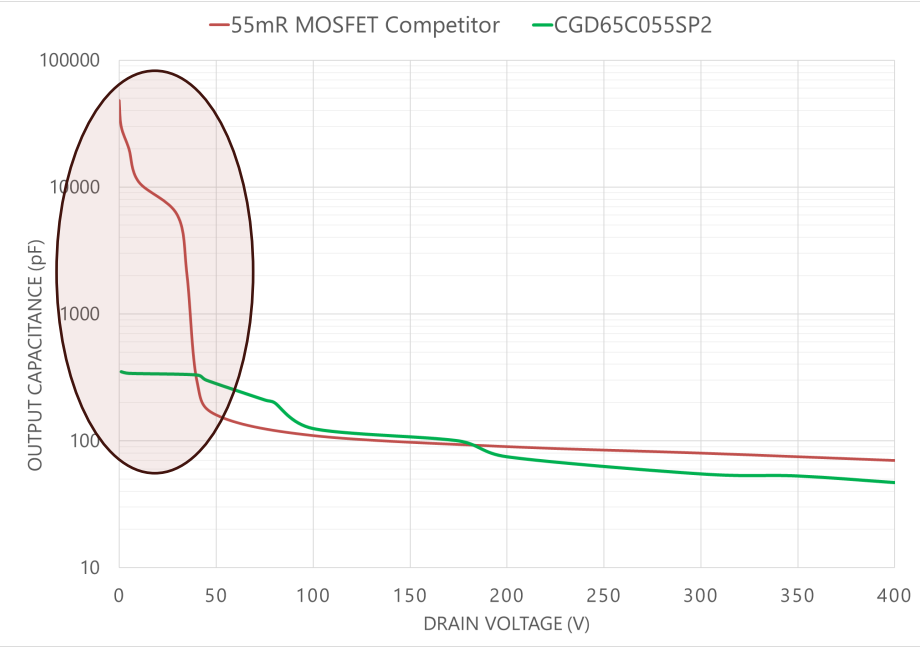
	55mR MOSFET	CGD65C055SP2
Coss (pf)	90	47
Cotr (pf)	1035	120

ICeGaN Lower C_{OTR} Faster!!

MOSFET V_{DS} discharge is significantly slower at Low Voltage

Faster ZVS Transitions with ICeGaN

MOSFETS are slower



But some of the latest SJ MOSFET achieve very low C_{OSS}

DON'T BE FOOLED

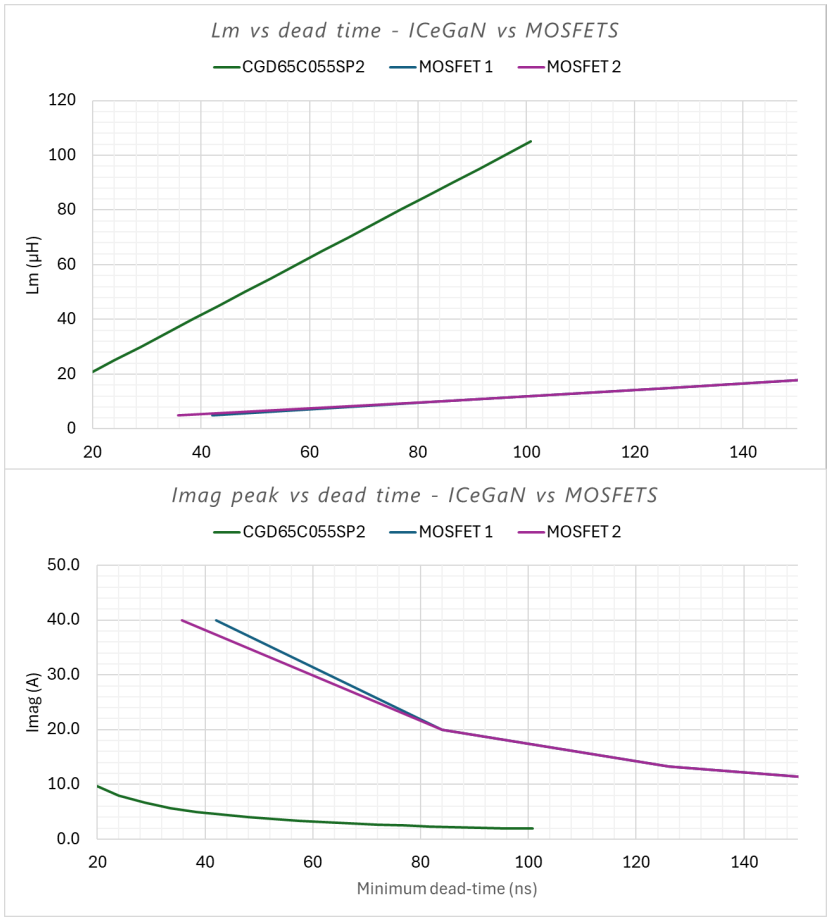
	25mR MOSFET	CGD65C055SP2
Coss (pf)	90	134
Cotr (pf)	1932	325

STILL ICeGaN has 7 times less C_{OTR}

MOSFET V_{DS} discharge is significantly slower at Low Voltage

ZVS ICeGaN vs MOSFET

Analysis on 55 mΩ devices at 500kHz switching frequency



	CGD65C055P2	MOSFET1	MOSFET2
R_{DSON} (mΩ)	55	52	52
C_{OTR} (pf) @400V	120	1035	894

$$L_M = \frac{dead\_timemin}{16 * c_{OTR} * f_{SW}}$$

ICeGaN has ~9 times lower C_{OTR}

Example
dead time = 100 ns

ICeGaN
I_{MAG} = 2 A
P_{IMAG} = 0.3W

MOSFET
I_{MAG} = 18 A
P_{IMAG} =3W

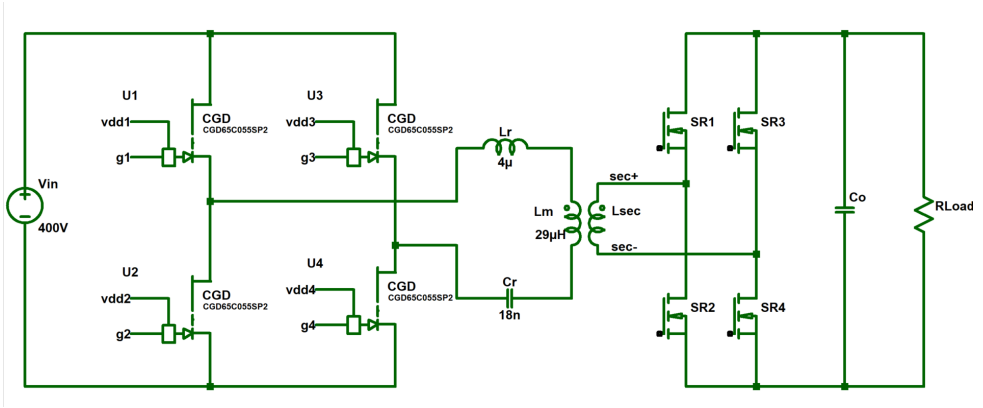
Shorter time to archive ZVS

Less magnetising current losses

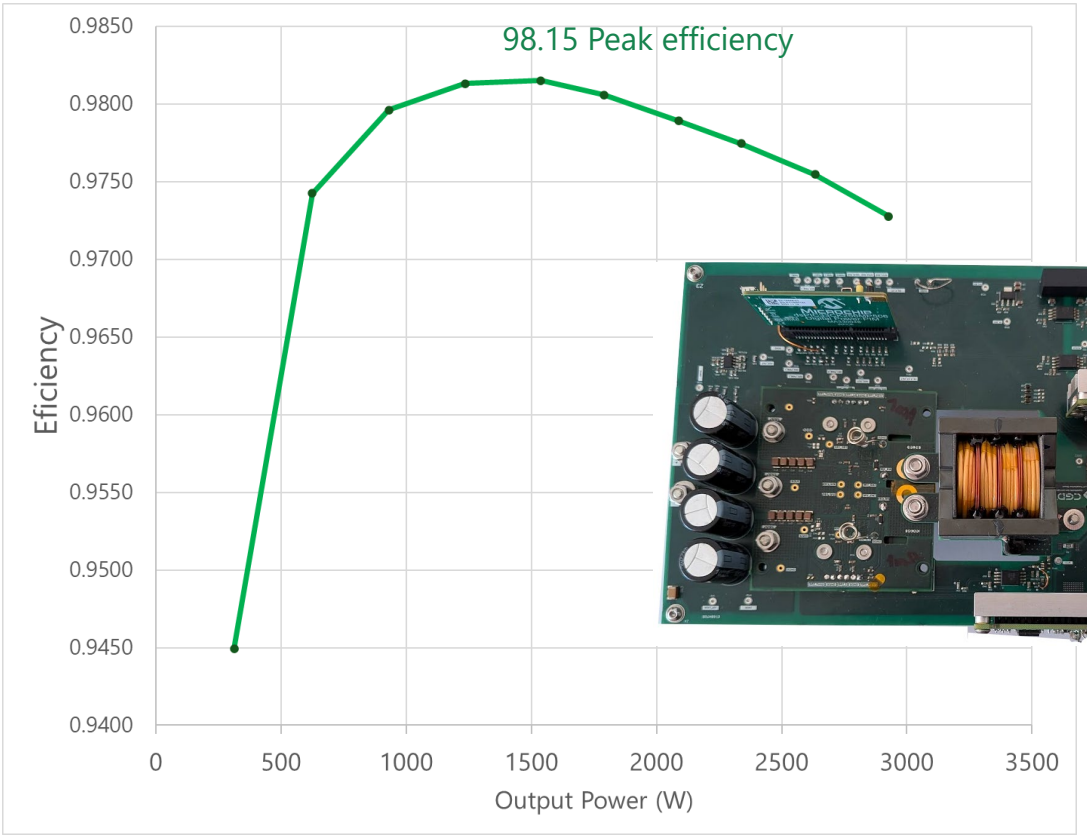
Less energy storage in the L_m

3kW 570kHz LLC Experimental Results

Open Loop Prototype



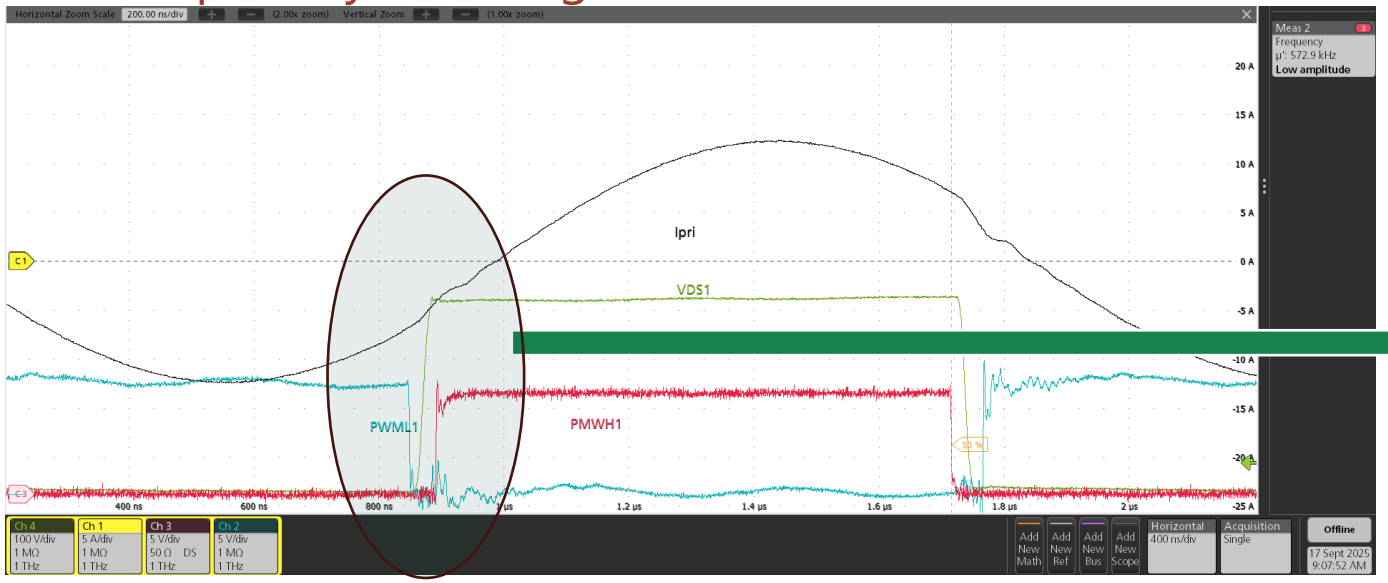
3kW LLC Specification	
Input LLC Voltage (nominal)	400V
Output Voltage (nominal)	50V
Nominal output power full load	3000W
Output current (nominal)	60A
Switching frequency (Full load nominal conditions)	500kHz
Steady-State Ripple (max.)	± 500mV
Target Efficiency at nominal conditions 400V input / 50V	
- 100% load	97%
- 50% load	98%
- 20% load	97%
- 10% load	94%
Cooling	Forced air (external FAN)

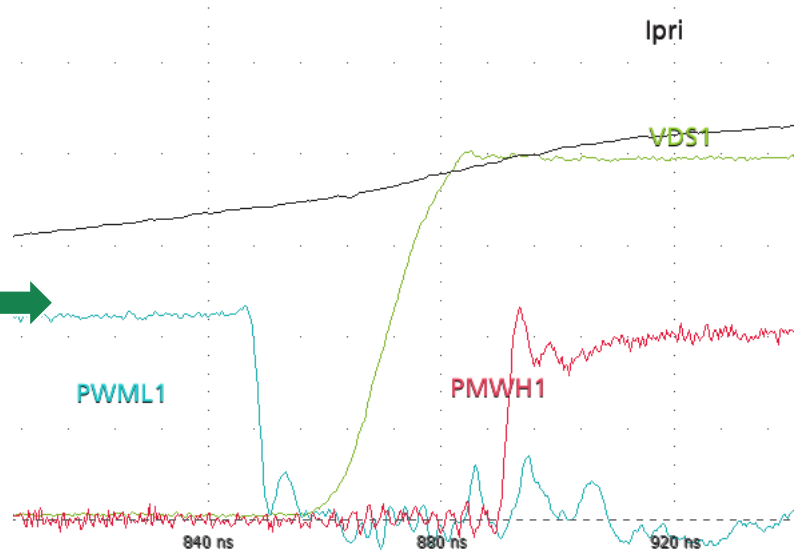


FB-FB Open Loop Prototype
PCB can be greatly optimized
PQ4040 Magnetic can be optimized
SR 2x1mR EPC GaN

3kW 570kHz LLC Experimental Results

55mΩ primary full-bridge waveforms





L_M = 29uH

Fsw = 570kHz

ZVS = 30ns

Dead time = 50ns

ICeGaN loss estimation = 4.6W → We were conservative in our preliminary estimation (>5W)

ICeGaN FB calculation =18.6W

Summary of ICeGaN in LLC Topologies

Fast switching | Low loss | Simple driving

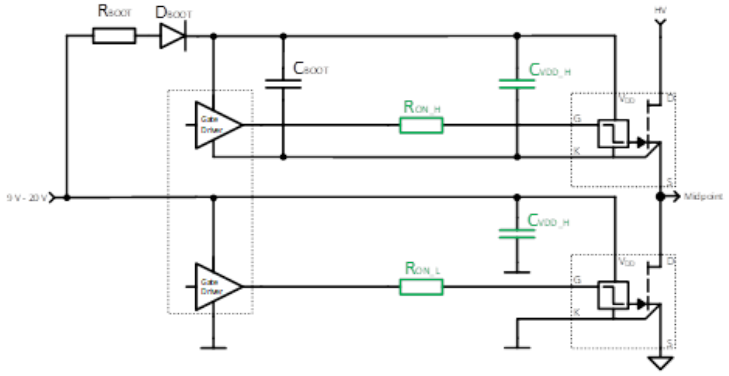
FAST SWITCHING → Shorter dead times, higher frequency operation, higher power density

SIMPLE DRIVING → No negative gate, no turn-off path**,** relaxed layout

MINIMAL COMPONENTS → Only 2 SMDs per device

EASY PARALLELING → Scales to high power

ROBUST → Excellent gate protection



Dare to innovate differently

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