FILTER FOR UNISOLATED DC/DC-CONVERTERS

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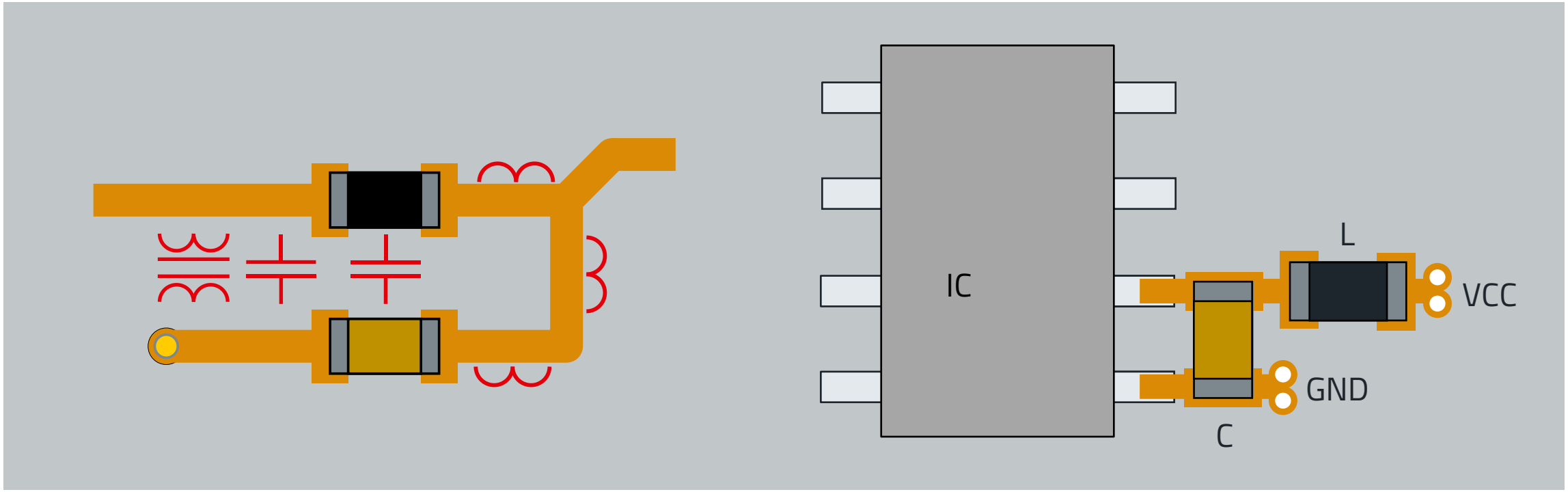
WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

- Filter placement
- Transmission modes
- DM noise source
- Filter topologies
- DM filter
- Measures against radiated noise

FILTER PLACEMENT

Filter Arrangement

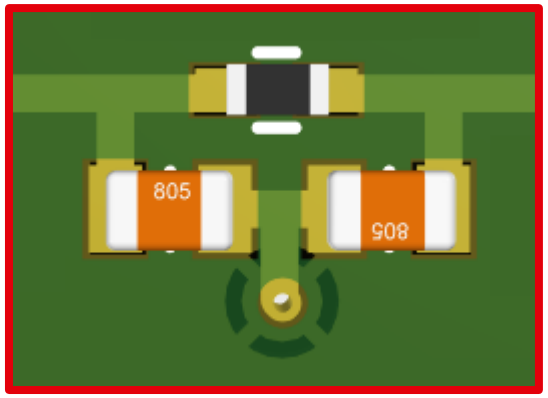
- 1nH per 1mm
- 0.5nH per Via



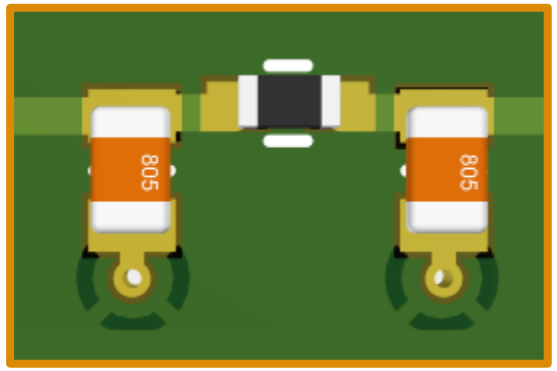
WE eiSos

Filter Arrangement

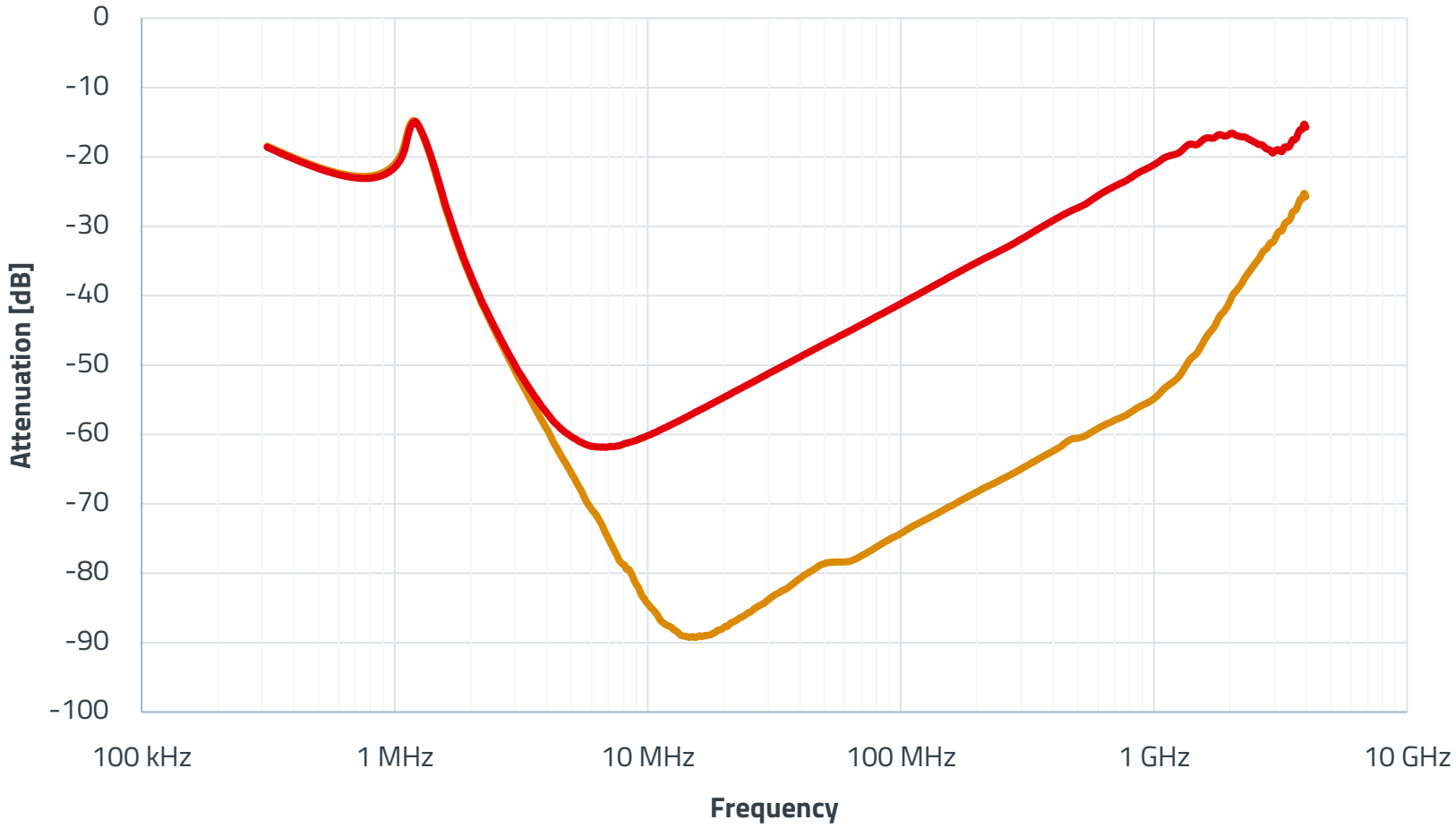
Layout: Influence on Insertion Loss



0805, Bad Layout

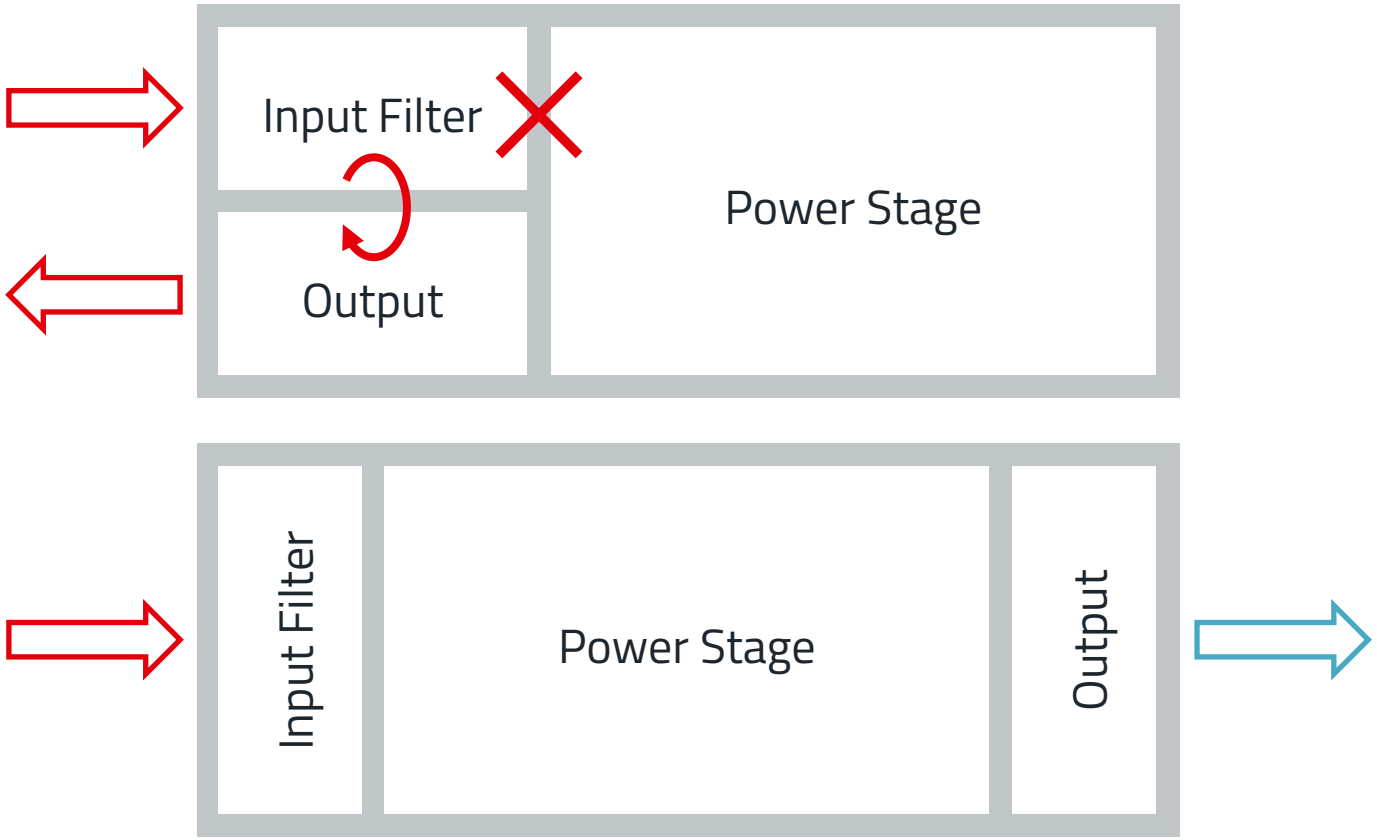


0805, Good Layout



Filter Placement

Example: Line Filter

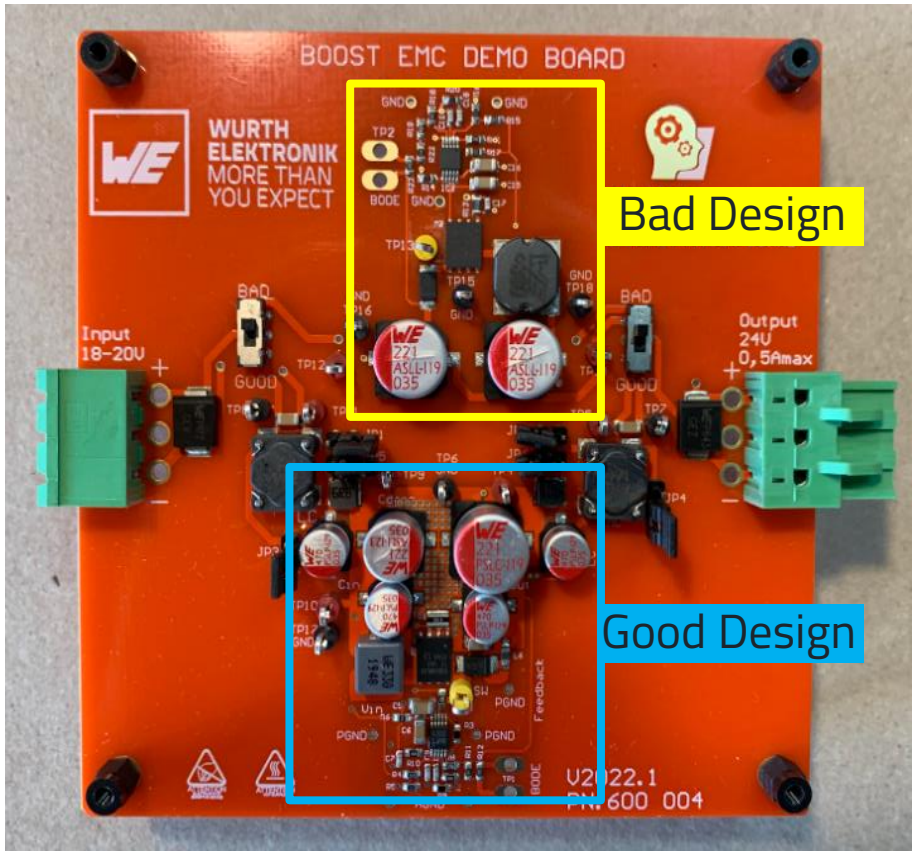


Avoid parallel structures and coupling of input/output

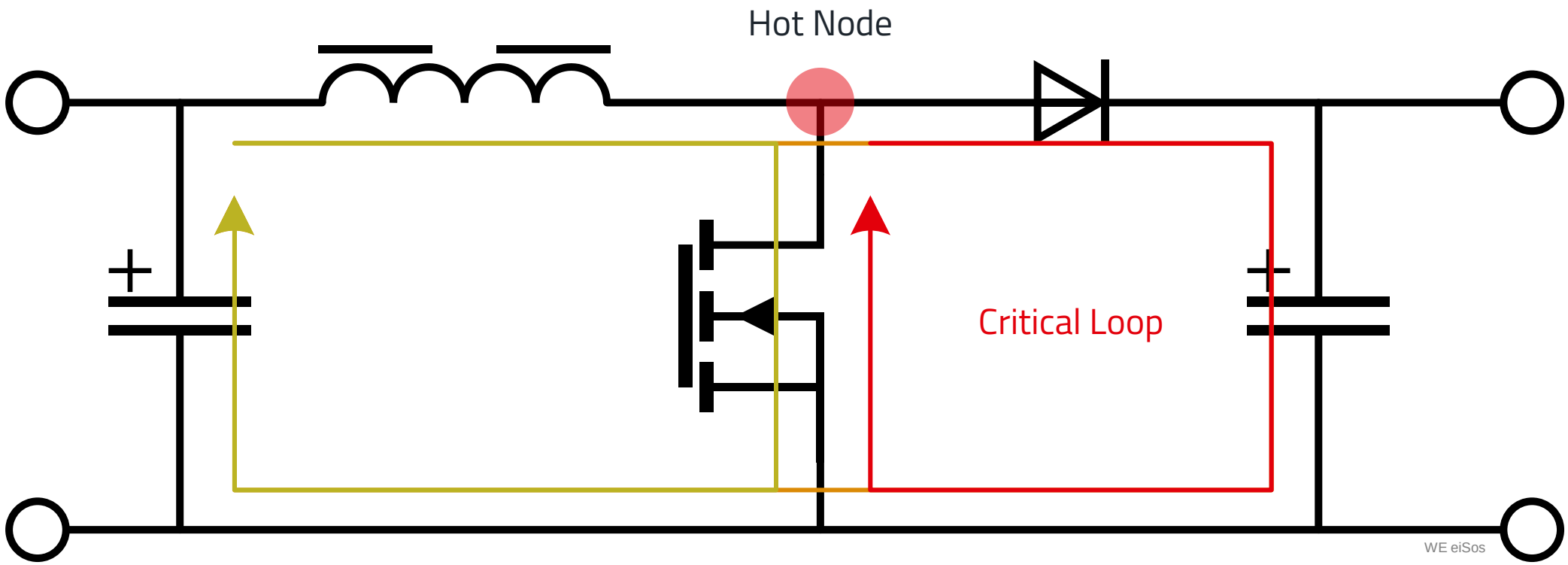
Objective of the Good and Bad Layout

Keypoints

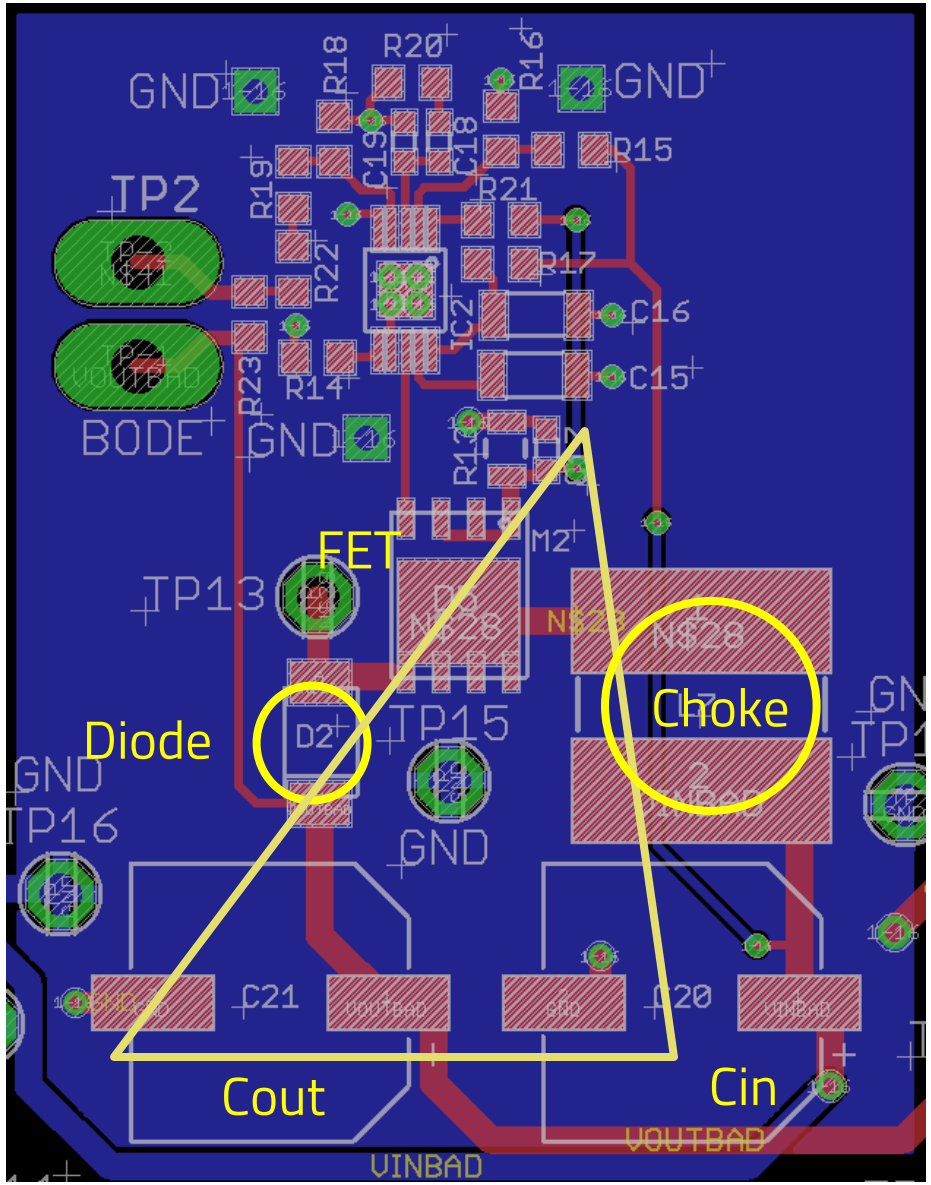
- Single Point PGND vs. big PGND Loop
- Correct vs. Wrong Capacitor Position
- Same Semiconductors, different Passives
- Shielded Choke vs. Unshielded Choke
- Alu-Electrolyte vs. Polymer Caps
- Filter @ I/Os vs. No Filter at all
- Ferrite in the Power Loop of a DCDC



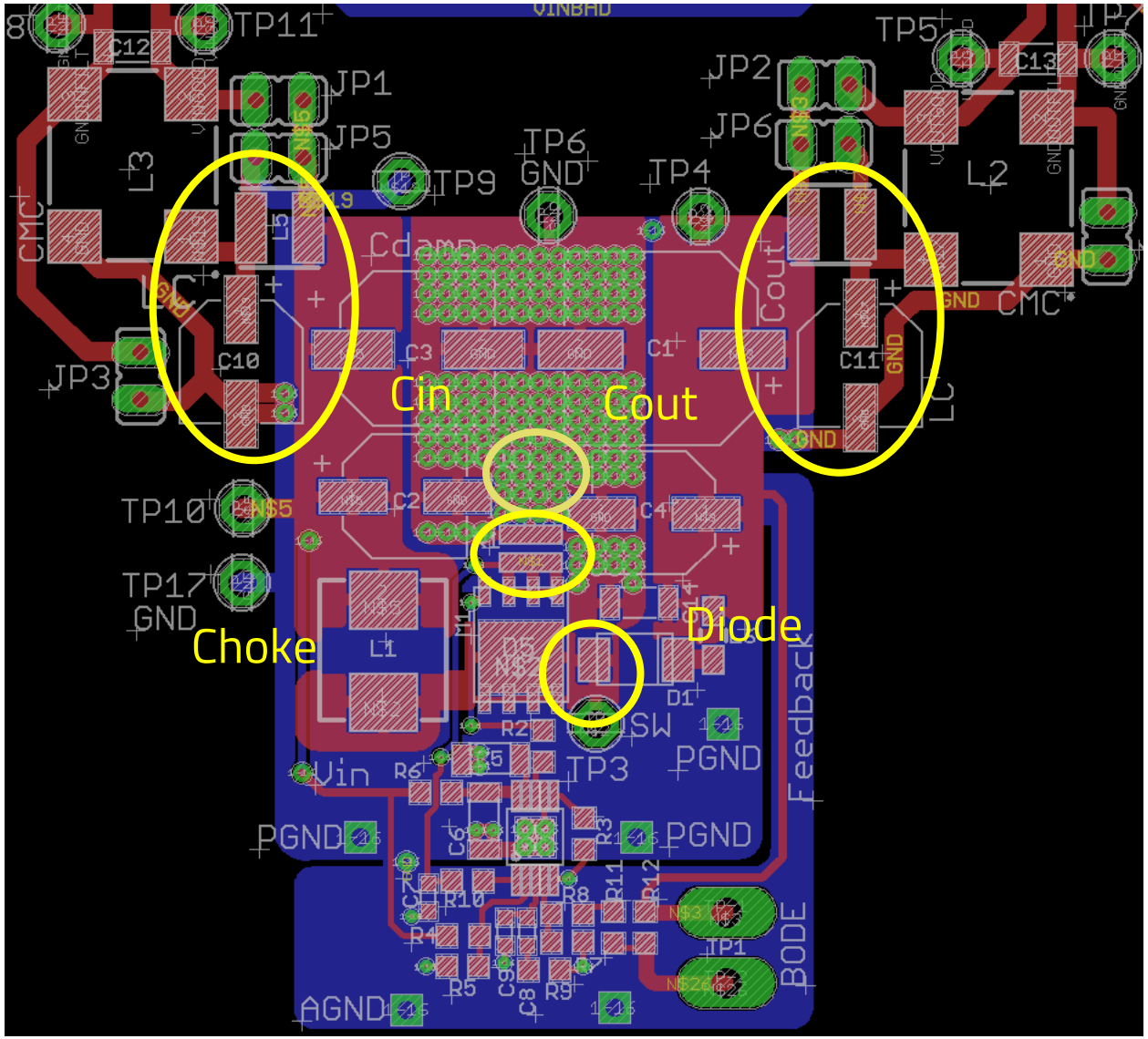
Noise sources with the Boost Converter



PCB Layout - Bad Design

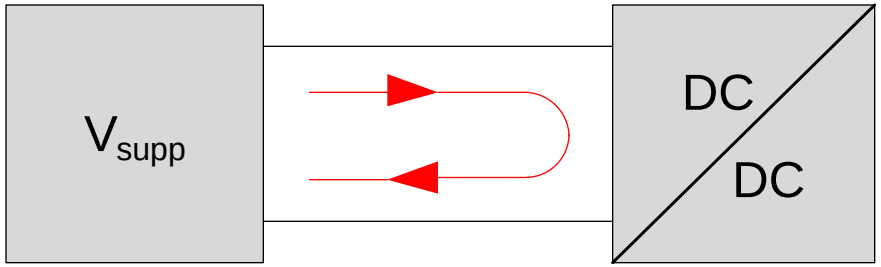


PCB Layout - Good Design

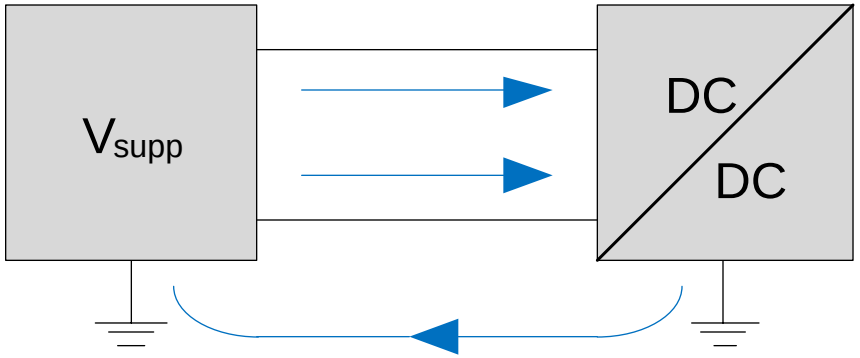


TRANSMISSION MODES

Transmission modes



Differential Mode



Common Mode

Transmission mode noise

- **Differential mode currents**
  - Current path as in circuit diagram
  - Easy to follow paths
  - Return current path very close
  - Relatively large currents
  - Filters with LC, π, T topologies
  - Conducted EMI problem
- **Common mode currents**
  - Current path unexpected
  - Current via parasitic paths
  - Return current path very large
  - Relatively small currents (µA)
  - Filtering with CMC and Y-Caps
  - Radiated & conducted EMI problem

EMC: How can *WE* help you ?

Over the limit ?
Susceptibility?

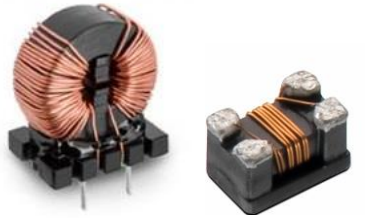
Overvoltage?

Surge :

ESD :

Conducted

Common mode



Differential mode

Y capacitor

X Cap

Radiated

Shielding Material

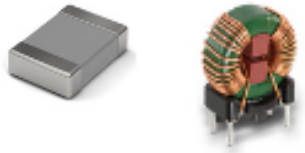
30MHz ~ 20GHz

Tracks

30MHz ~ 3GHz

Ferrite

Capacitor

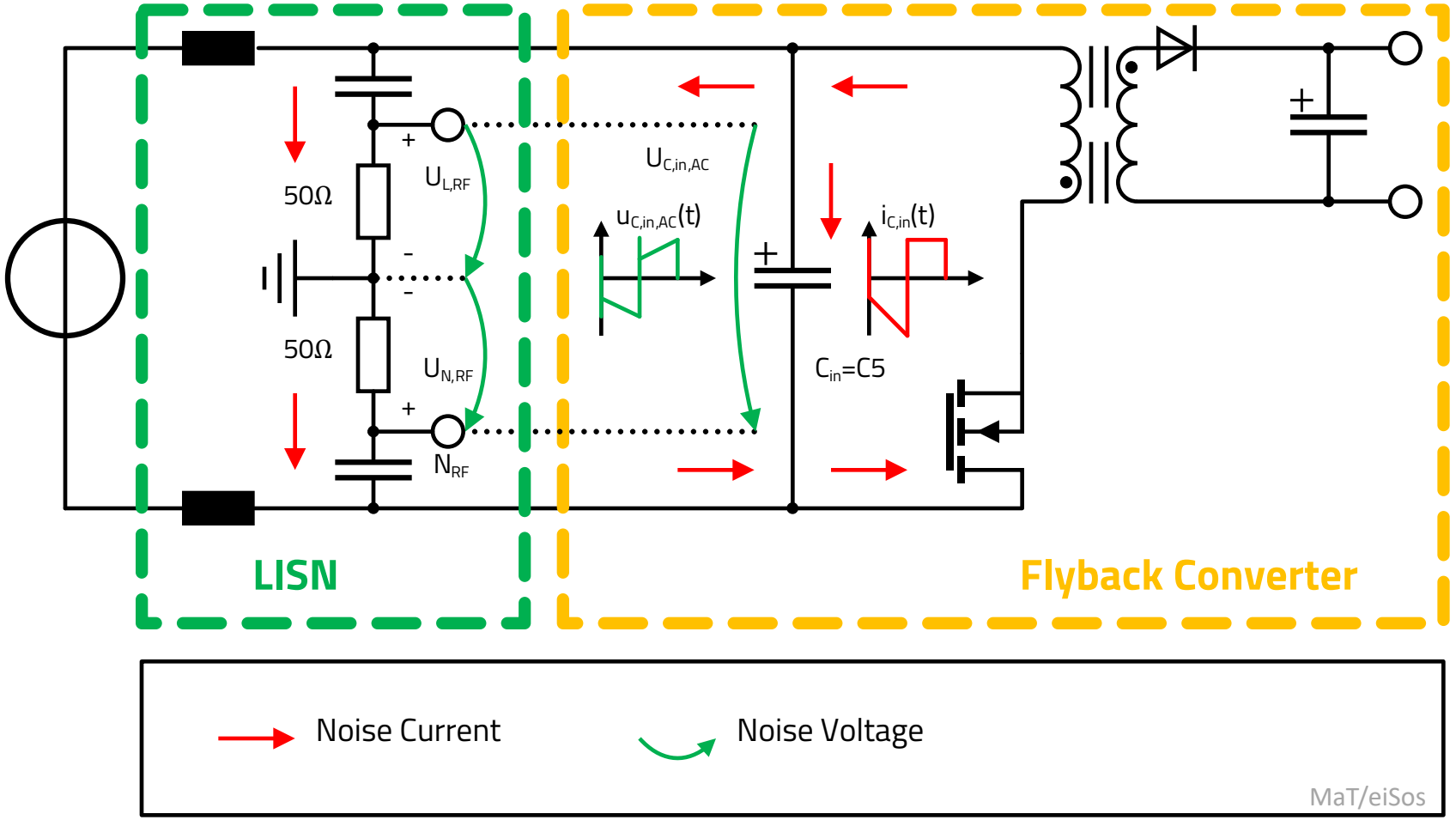


Cables

30 ~ 100MHz

Differential mode noise

Theory: Conducted emissions measurement - Symmetrical LISN



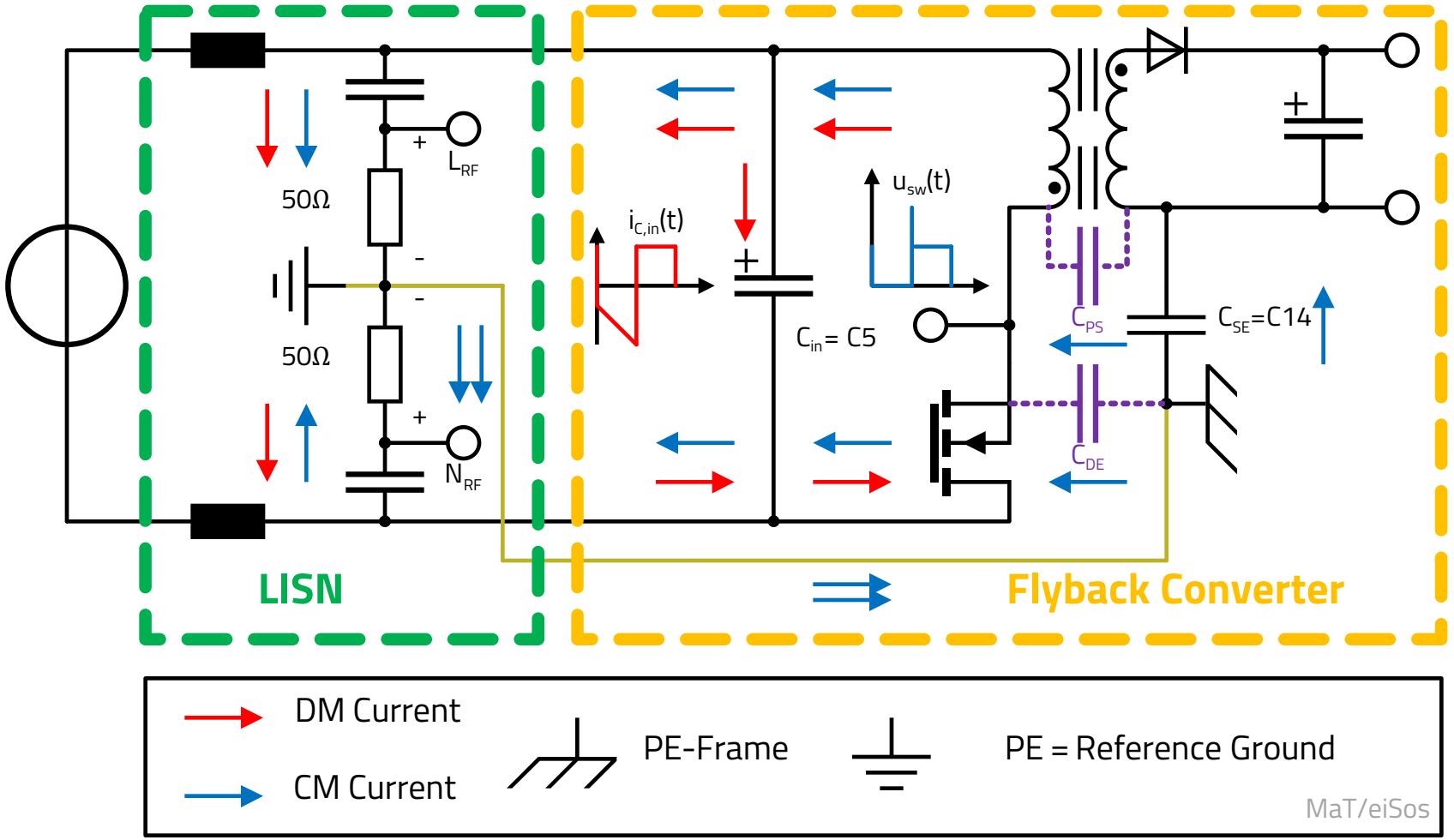
$$U_{\mathrm{L,RF}} = U_{\mathrm{N,RF}} = \frac{U_{\mathrm{C,in,AC}}}{2}$$

$$20 \cdot \log\left(\frac{1}{2}\right) \approx -6dB$$

$$\boldsymbol{k = 1:}$$
$$\left|\widetilde{U}_{L,RF}\right| = \left|\widetilde{U}_{C,in}\right| - 6dB$$

Recognizing the transmission mode

Theory: DM and CM noise path in a flyback converter



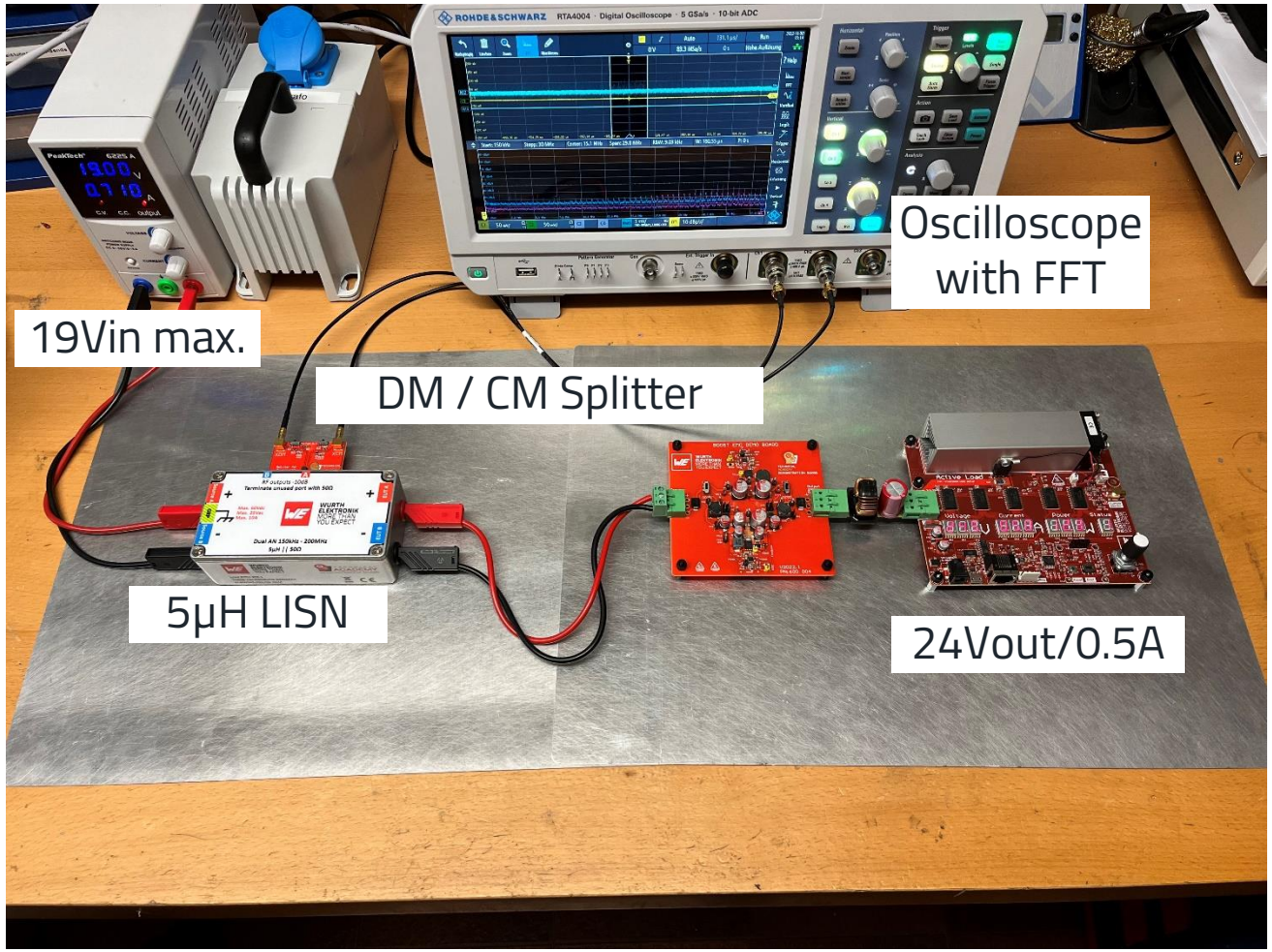
$$U_{\mathrm{L,RF}} = U_{\mathrm{CM}} + U_{\mathrm{DM}}$$

$$U_{\mathrm{N,RF}} = U_{\mathrm{CM}} - U_{\mathrm{DM}}$$

$$U_{\mathrm{DM}} = \frac{U_{\mathrm{L,RF}} - U_{\mathrm{N,RF}}}{2}$$

$$U_{\mathrm{CM}} = \frac{U_{\mathrm{L,RF}} + U_{\mathrm{N,RF}}}{2}$$

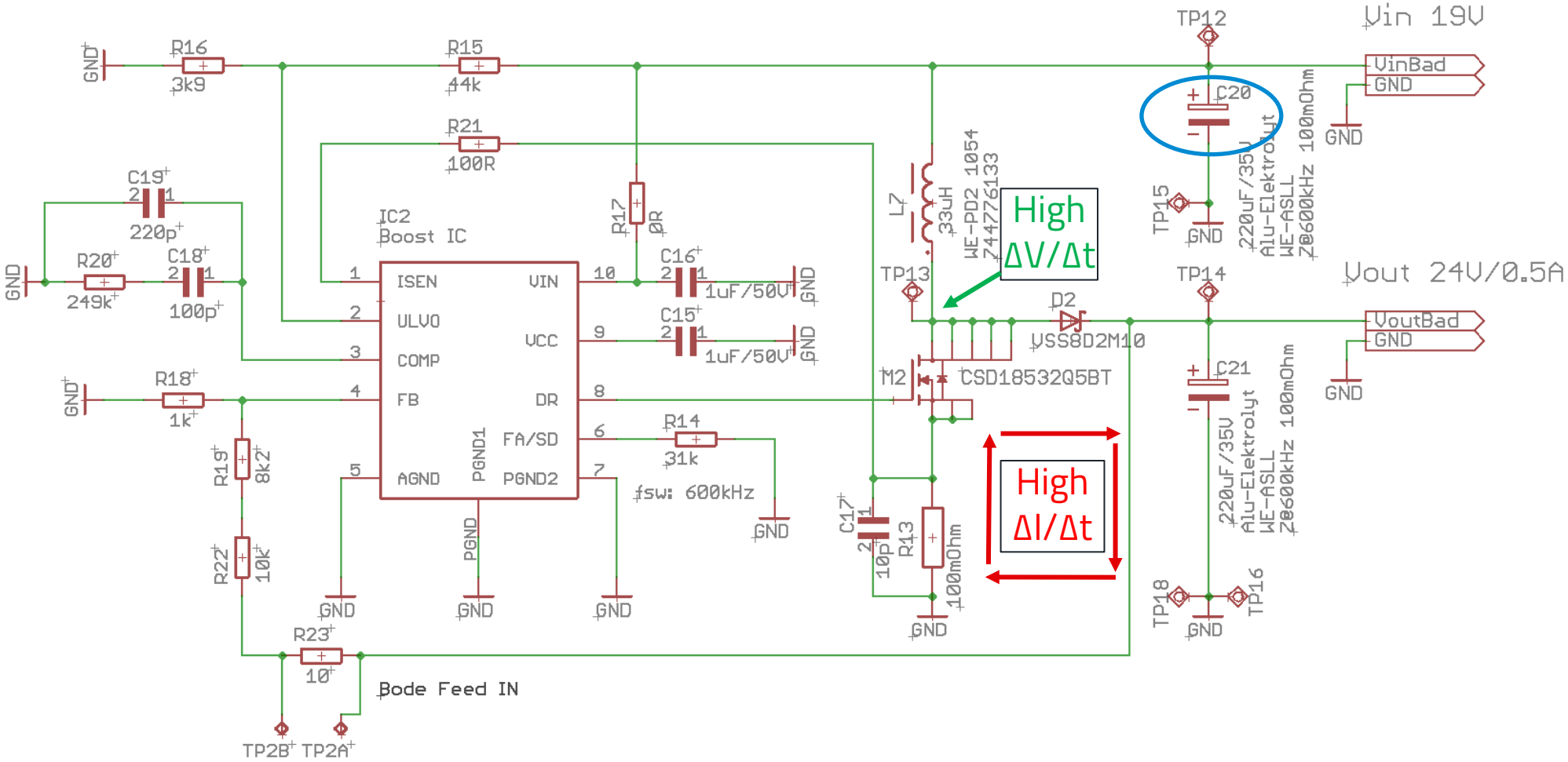
Setup


ROHDE&SCHWARZ RTA4004 · Digital Oscilloscope · 5 GSa/s · 10-bit ADC
Oscilloscope with FFT
19Vin max.
DM / CM Splitter
5µH LISN
24Vout/0.5A

DM NOISE SOURCE

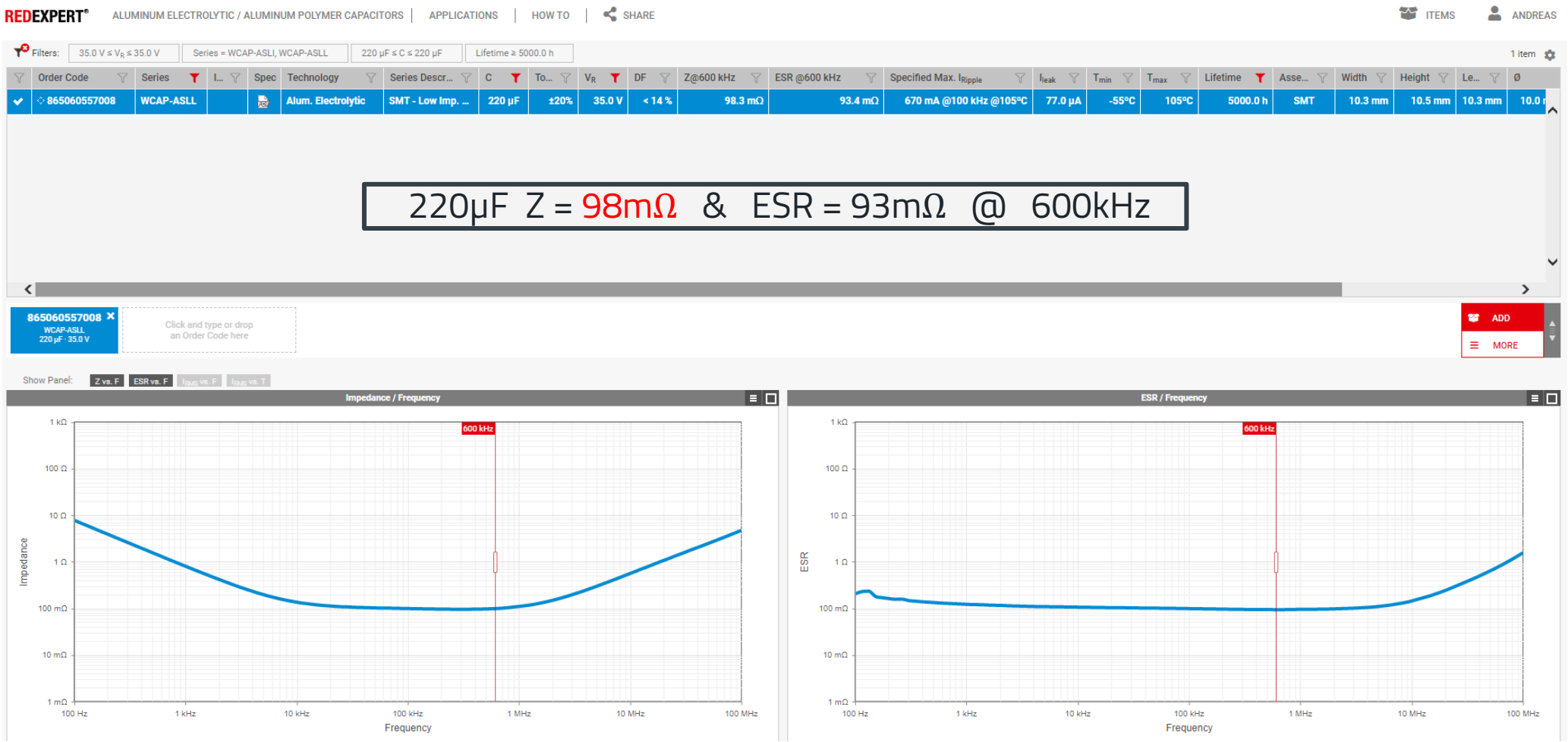
Schematic - Bad Design

19V → 24V/0,5A



Input capacitor - Bad Design

Redexpert Alu Cap Selection for Fsw 600kHz



Conducted EMI Calculation with 220µF Elko Cin - Bad Design

Triangular approximation (differentail mode only):

$$D = \frac{U_{out} - U_{in} + U_d}{U_{out} + U_d} = \frac{24V - 19V + 0{,}5V}{24V + 0{,}5V} = 0{,}224$$

$$\Delta I = \frac{U_{in}}{L \cdot f_{sw}} \cdot D = \frac{19V}{33\mu H \cdot 600kHz} \cdot 0{,}224 = 0{,}21A$$

$$|I_{cin}[600kHz]| = \frac{\Delta I}{\sqrt{2} \cdot \pi^2 \cdot D \cdot (1 - D)} \cdot |\sin(\pi \cdot D)| = \frac{0{,}21A}{\sqrt{2} \cdot \pi^2 \cdot 0{,}224 \cdot (1 - 0{,}224)} \cdot |\sin(\pi \cdot 0{,}224)| = 56mA$$

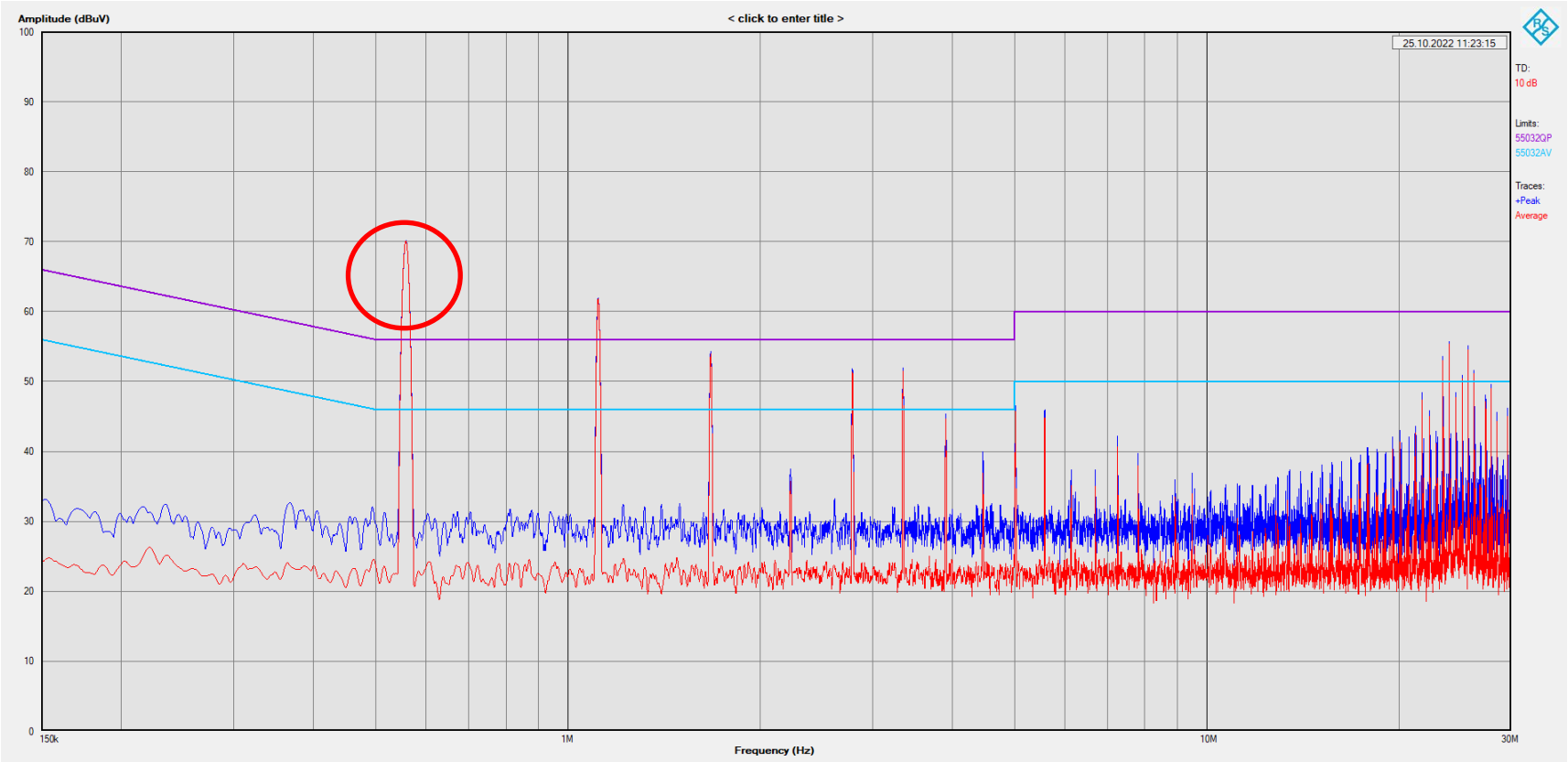
$$|U_{cin}(600kHz)| = |Z_{cin}(600kHz)| \cdot |I_{cin}(600kHz)| = 98m\Omega \cdot 56mA = 5{,}49mV$$

$$5{,}49mV \rightarrow 20\log\left(\frac{5{,}49mV}{1\mu V}\right) = 74{,}8dB\mu V \; - 6dB(LISN\ Voltage\ Divider) = 68{,}8dB\mu V$$

Limit CISPR32 Class B is 46dBµV → approx. 33dB Damping is necessary

Verification of the triangular approximation - Bad Design

DM noise on input with DM/CM splitter



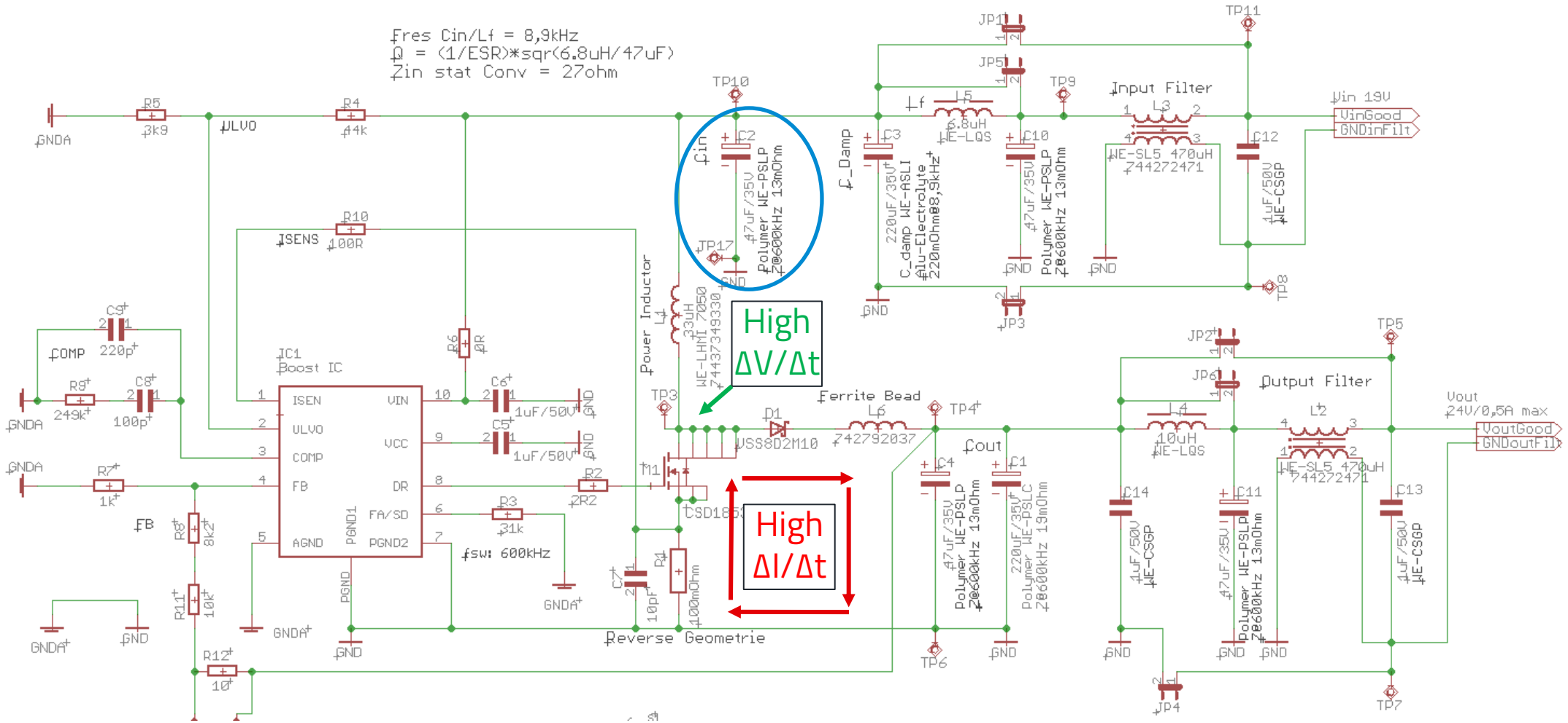
69dBµV as calculated

Input capacitor - Good Design

Redexpert Polymer Cap Selection for Fsw 600kHz

Schematic - Good Design

19V → 24V/0,5A



Conducted EMI Calculation with 47µF Polymer Cin

Triangular approximation (differential mode only):

$$D = \frac{U_{out} - U_{in} + U_d}{U_{out} + U_d} = \frac{24V - 19V + 0{,}5V}{24V + 0{,}5V} = 0{,}224$$

$$\Delta I = \frac{U_{in}}{L \cdot f_{sw}} \cdot D = \frac{19V}{33\mu H \cdot 600kHz} \cdot 0{,}224 = 0{,}21A$$

$$|I_{cin}[600kHz]| = \frac{\Delta I}{\sqrt{2} \cdot \pi^2 \cdot D \cdot (1 - D)} \cdot |\sin(\pi \cdot D)| = \frac{0{,}21A}{\sqrt{2} \cdot \pi^2 \cdot 0{,}224 \cdot (1 - 0{,}224)} \cdot |\sin(\pi \cdot 0{,}224)| = 56mA$$

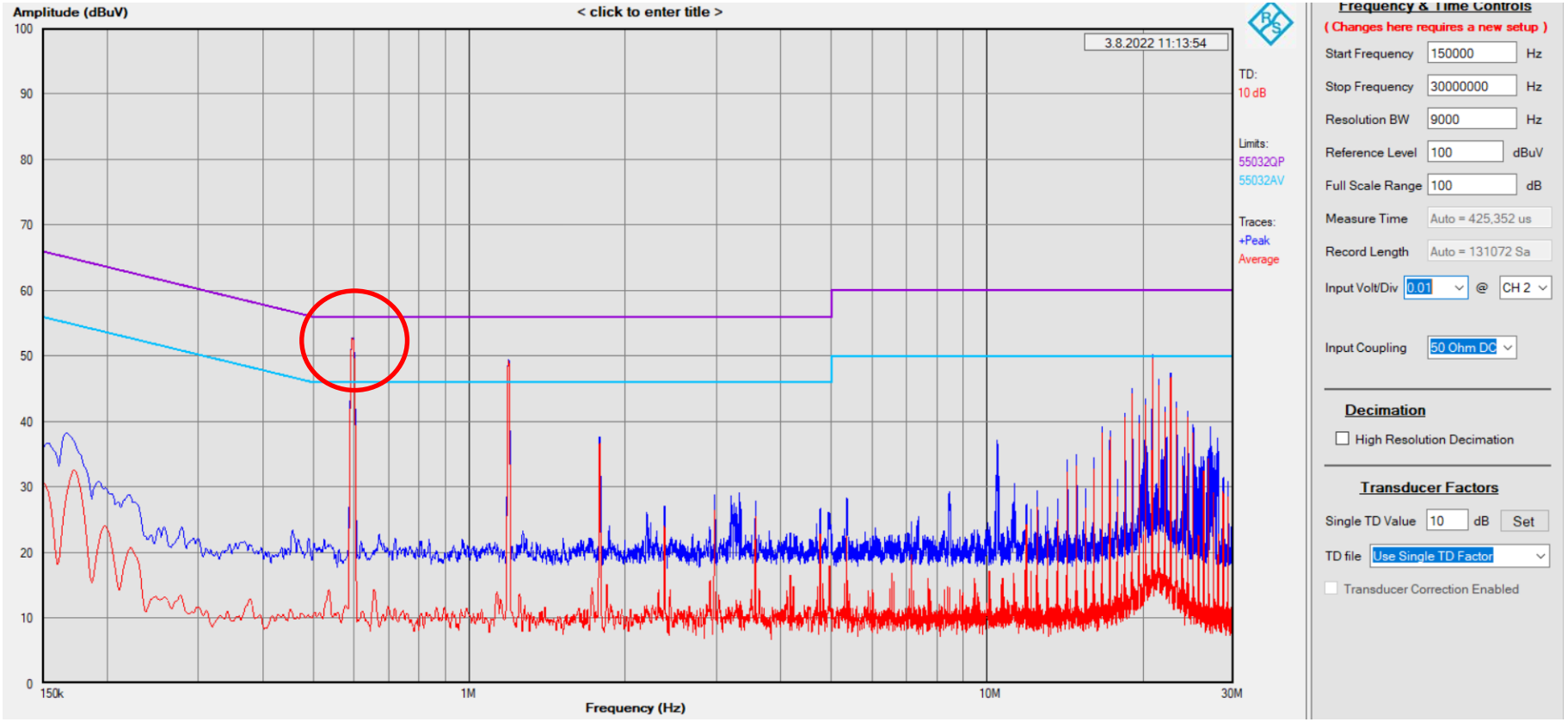
$$|U_{cin}(600kHz)| = |Z_{cin}(600kHz)| \cdot |I_{cin}(600kHz)| = 14m\Omega \cdot 56mA = 784\mu V$$

$$784\mu V \rightarrow 20\log\left(\frac{784\mu V}{1\mu V}\right) = 57{,}9dB\mu V \; - 6dB(LISN\ Voltage\ Divider) = 51{,}9dB\mu V$$

Limit CISPR32 Class B is 46dBµV → approx. 16dB Damping is necessary

Verification of the triangular approximation - Good Design

DM noise on input without Filter



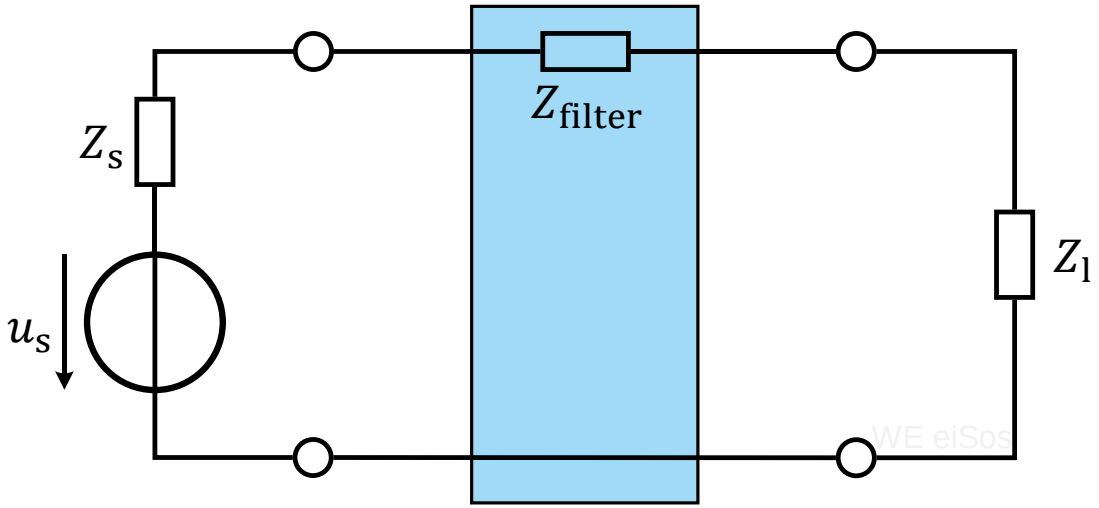
52dBµV as calculated

FILTER TOPOLOGIES

Dimensioning of a filter choke

- A filter choke in series connection forms a **first-order low-pass**.
- **Differential-mode insertion loss** in decibel:

$$A_{\mathrm{dm}} = 20 \cdot \log \left| 1 + \frac{Z_{\mathrm{filter}}}{Z_{\mathrm{s}} + Z_{\mathrm{l}}} \right| \mathrm{dB}$$



- Minimum required filter impedance Z_{filter} at a noise frequency f_{n}:

$$|Z_{\mathrm{filter}}|_{f_{\mathrm{n}}} \geq |Z_{\mathrm{s}} + Z_{\mathrm{l}}|_{f_{\mathrm{n}}} \cdot \left(10^{\frac{A_{\mathrm{dm}}(f_{\mathrm{n}})}{20}} - 1 \right)$$

- For an exact calculation the source and load impedance for each noise frequency would have to be known.

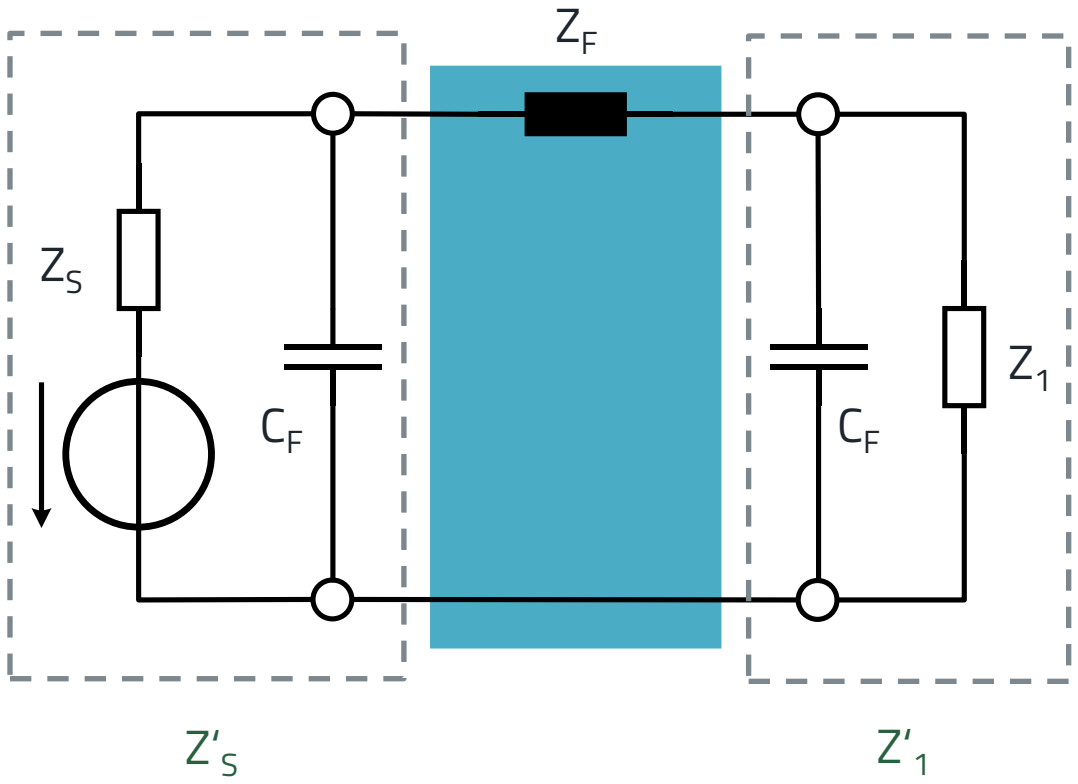
Dimensioning of a Filter

Adjusting the Operating Point with Capacitors

- Parallel Capacitors decrease System Impedance

$$A_{\mathrm{dm}} = 20 \cdot \log \left| 1 + \frac{Z_{\mathrm{F}}}{Z'_{\mathrm{s}} + Z'_{\mathrm{l}}} \right| \mathrm{dB}$$

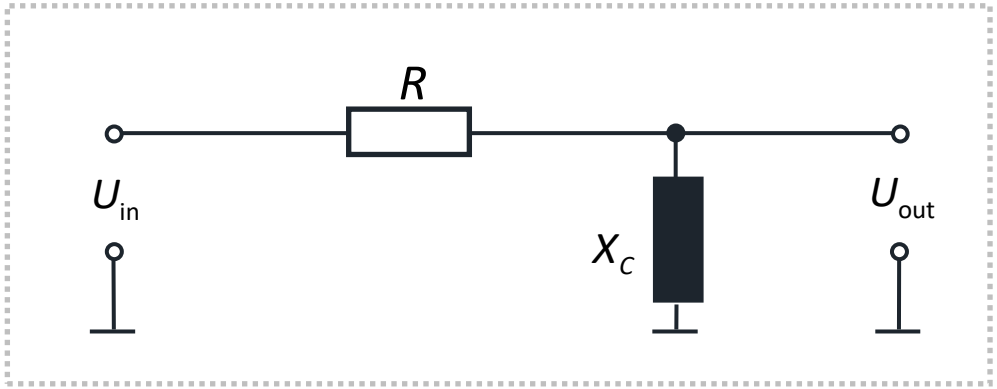
- Caps will also work as an RF Short to Ground
- Pay Attention to SRF of the Components
- 2nd order Filter Topologies can be adjusted to system impedances



Filter order

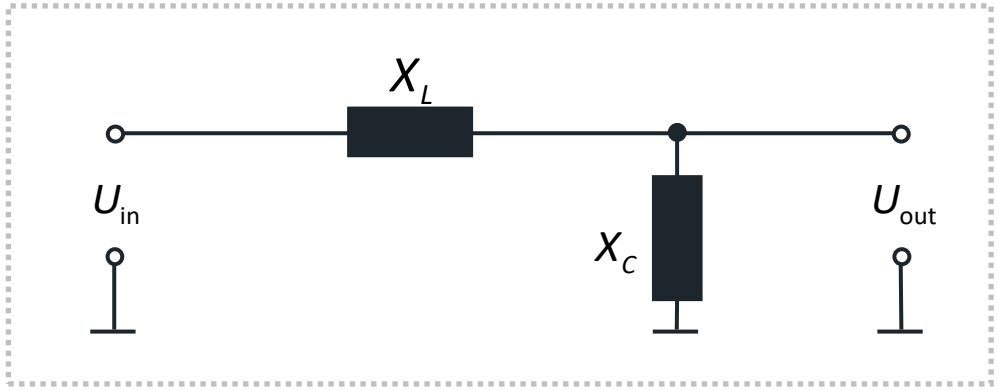
- The filter order is determinded by the number of energy storage elements (*L* & *C*).

Low-pass example: first order



$$f \uparrow \rightsquigarrow X_C = -\frac{1}{\omega C} \downarrow$$

Low-pass example: second order



$$f \uparrow \rightsquigarrow X_L = \omega L \uparrow$$

$$f \uparrow \rightsquigarrow X_C = -\frac{1}{\omega C} \downarrow$$

Filter calculation by hand

- Amount of the transfer function of the low-pass filter:

$$\left|\frac{u_{\text{sup}}}{u_{\text{in}}}\right| = \frac{|X_C|}{X_L + X_C}$$

- Reactance:

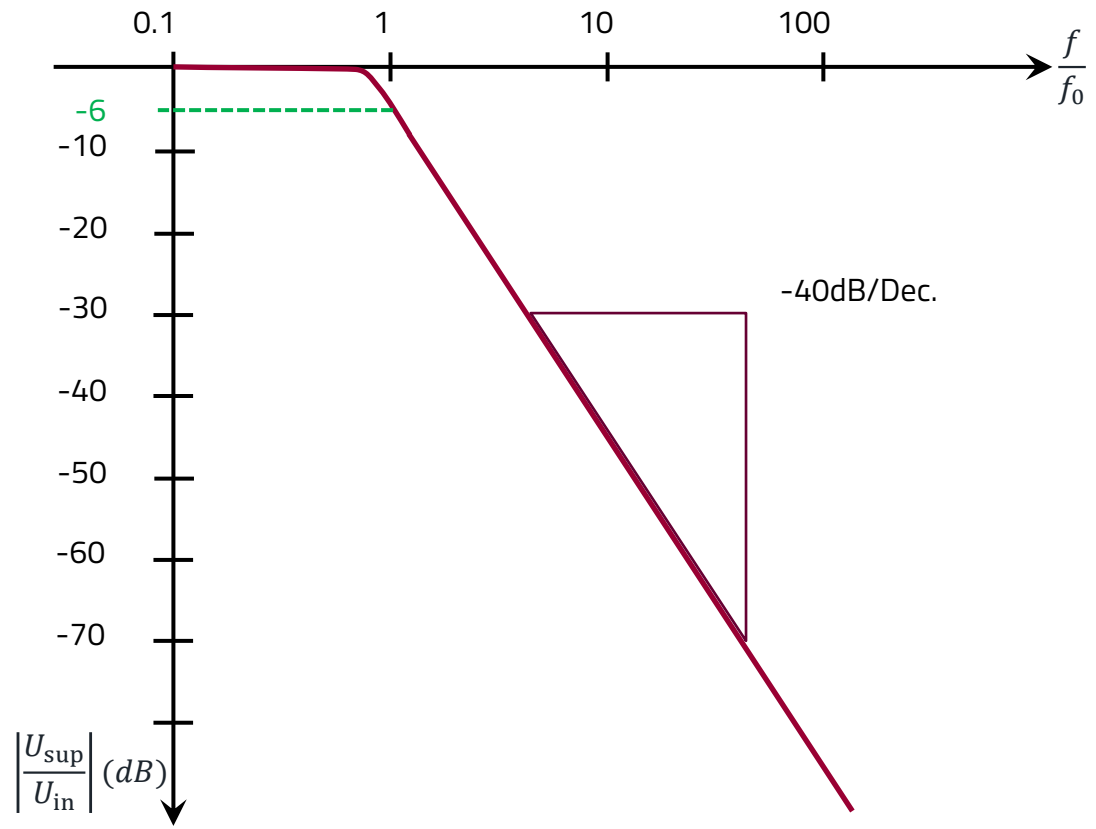
$$X_L = 2\pi \cdot f \cdot L_{\text{F}}$$

$$X_C = -\frac{1}{2\pi \cdot f \cdot C_{\text{F}}}$$

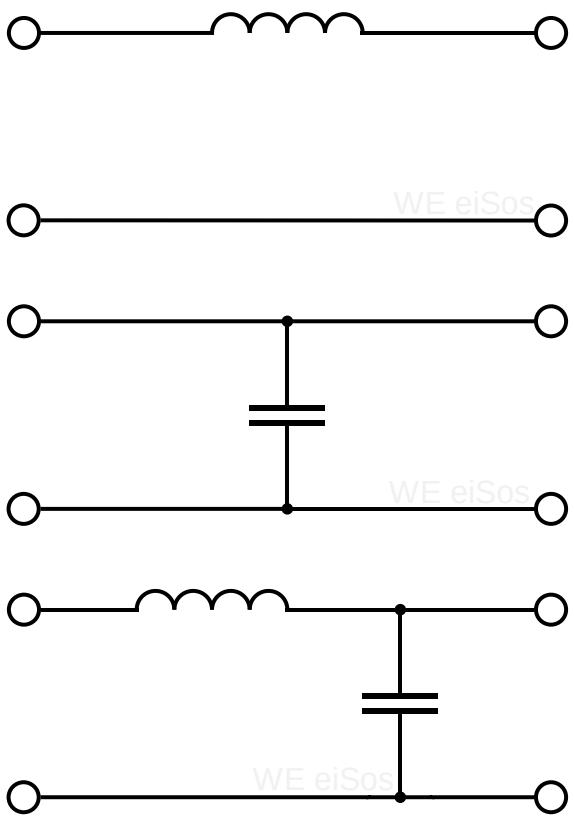
- -6dB cutoff frequency:

$$f_{\text{c}} = \frac{1}{2\pi \cdot \sqrt{L_{\text{F}} \cdot C_{\text{F}}}}$$

Gain Plot 2nd Order LC Filter

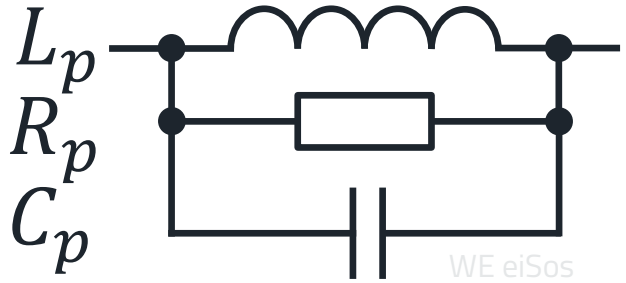


Filter topologies – Overview

Input	Topology	Output
$\lvert Z_s \rvert_{f_n} < \lvert Z_L \rvert_{f_n}$		$\lvert Z_l \rvert_{f_n} < \lvert Z_L \rvert_{f_n}$
$\lvert Z_s \rvert_{f_n} > \lvert Z_C \rvert_{f_n}$		$\lvert Z_l \rvert_{f_n} > \lvert Z_C \rvert_{f_n}$
$\lvert Z_s \rvert_{f_n} < \lvert Z_L \rvert_{f_n}$		$\lvert Z_l \rvert_{f_n} > \lvert Z_C \rvert_{f_n}$

Filter topologies – inductance vs. SMD-ferrite

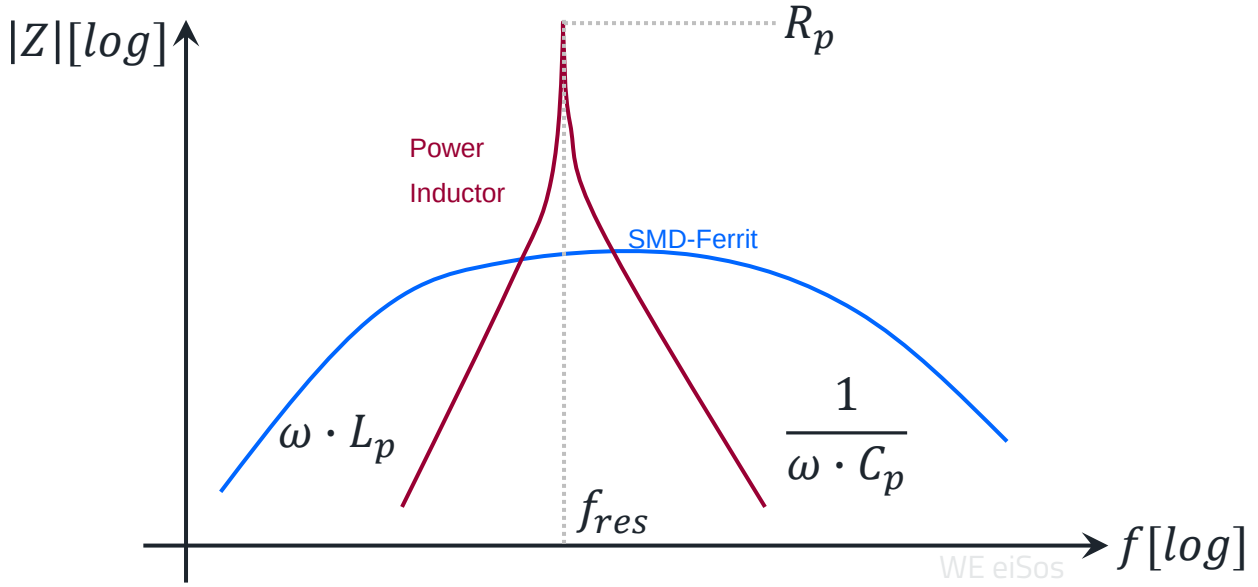
- Parasitic capacitance C_p:
  - → Power inductor: 10pF ... 500pF
  - → SMD-ferrite: 5fF ... 5pF



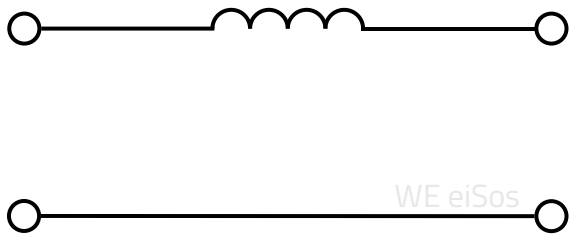
- Loss resistance R_p:
  - → Power inductor: < 30kΩ
  - → SMD-ferrite: 10Ω ... 3kΩ

$$f_{res} = \frac{1}{2 \cdot \pi \cdot \sqrt{L_p \cdot C_p}}$$

$$|Z(f_{res})| = R_p$$



L-filter

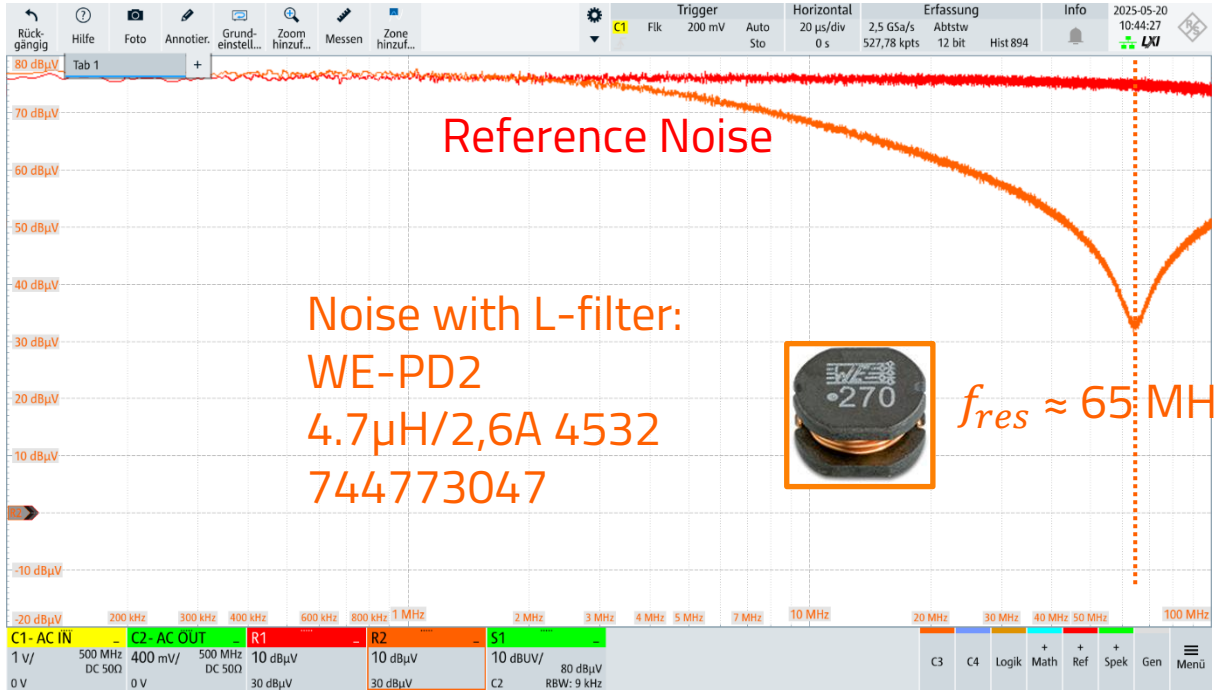


- Insertion loss for $Z_s = Z_l = 50\Omega$:

$$A_{\mathrm{dm},50} = 20 \cdot \log \left| 1 + \frac{Z_L}{100\Omega} \right| \mathrm{dB}$$

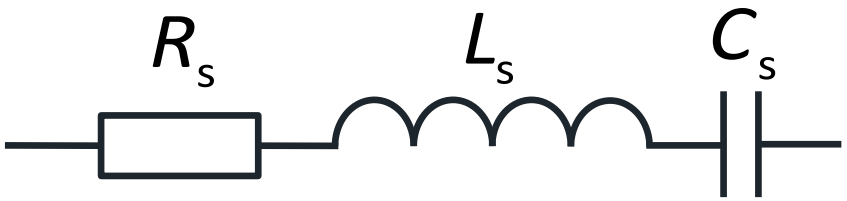
- General insertion loss:

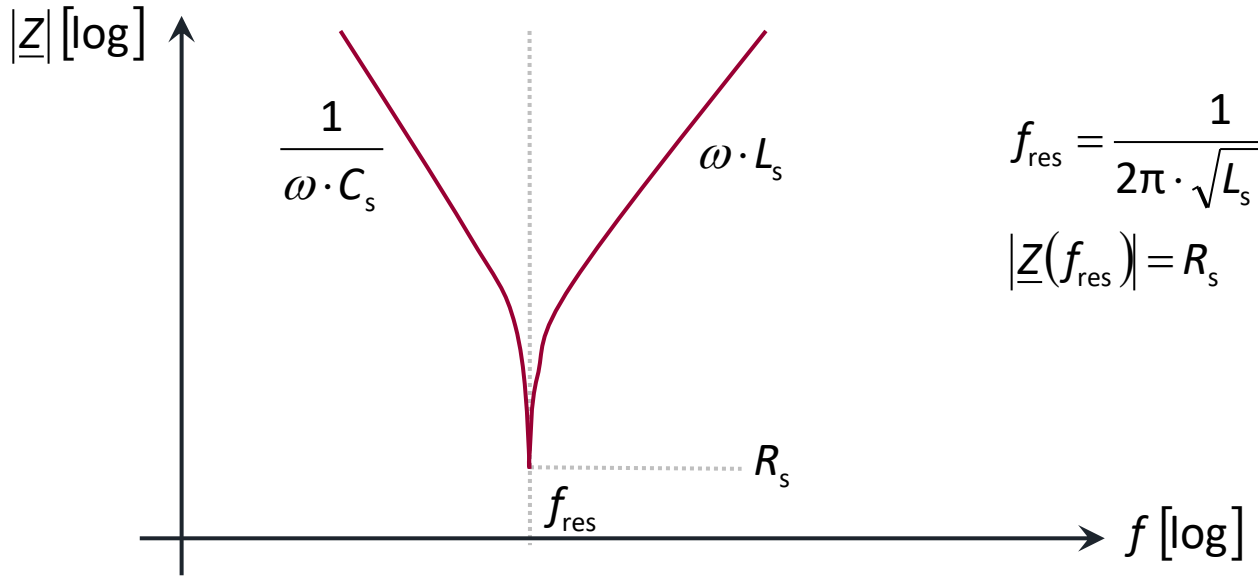
$$A_{\mathrm{dm}} = 20 \cdot \log \left| 1 + \frac{1}{Z_s + Z_l} \cdot \sum_n Z_{L,n} \right| \mathrm{dB}$$



Filter elements – Capacitance

- Extension of the L-filter with another frequency-dependent element:
  - Capacitor / capacitance
- Series inductance Ls:
  - SMD type: 1nH ... 5nH
- Series resistance Rs:
  - SMD type: 20mΩ ... 300mΩ (1Ω)

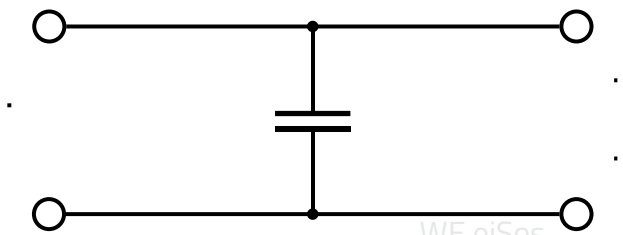




$$f_{res} = \frac{1}{2\pi \cdot \sqrt{L_s \cdot C_s}}$$

$$|\underline{Z}(f_{res})| = R_s$$

C-filter

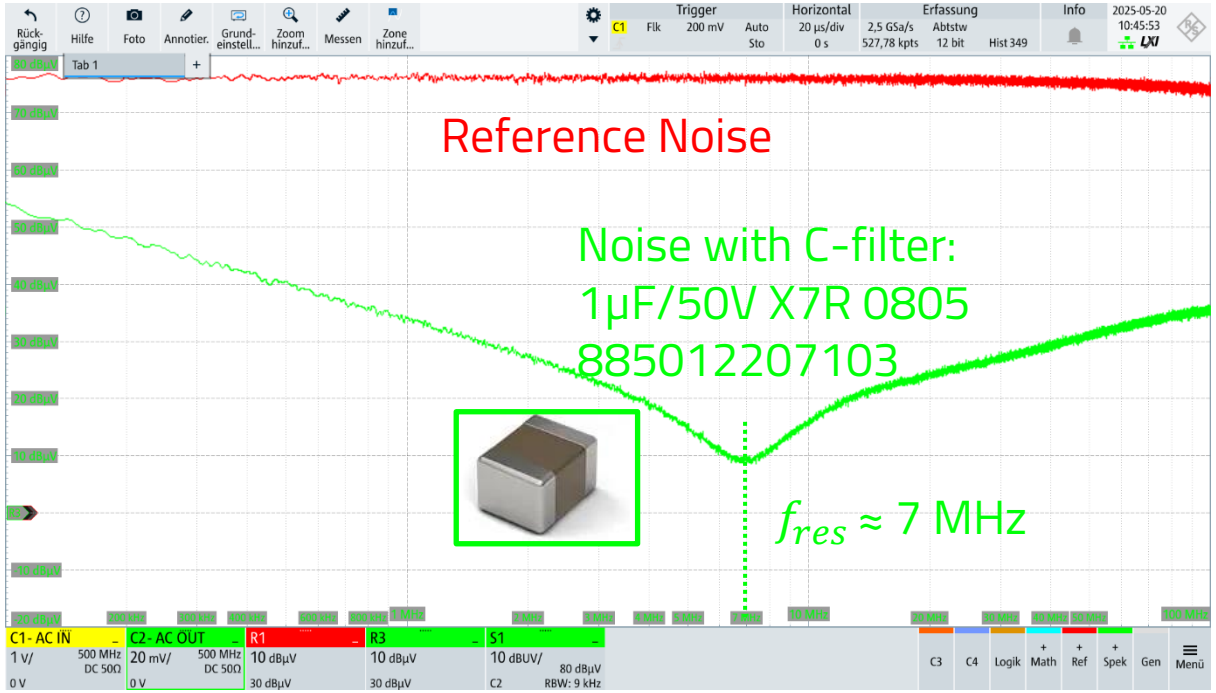


- Insertion loss for $Z_s = Z_l = 50\Omega$:

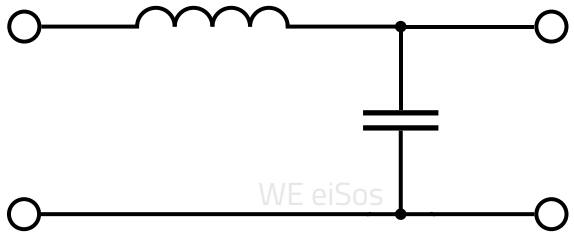
$$A_{\mathrm{dm},50} = 20 \cdot \log|1 + 25\Omega \cdot Y_{C1}|\ \mathrm{dB}$$

- General insertion loss:

$$A_{\mathrm{dm}} = 20 \cdot \log\left|1 + \frac{1}{Y_s + Y_l} \cdot \sum_n Y_{C,n}\right|\ \mathrm{dB}$$



LC-filter (Unshielded filter choke)

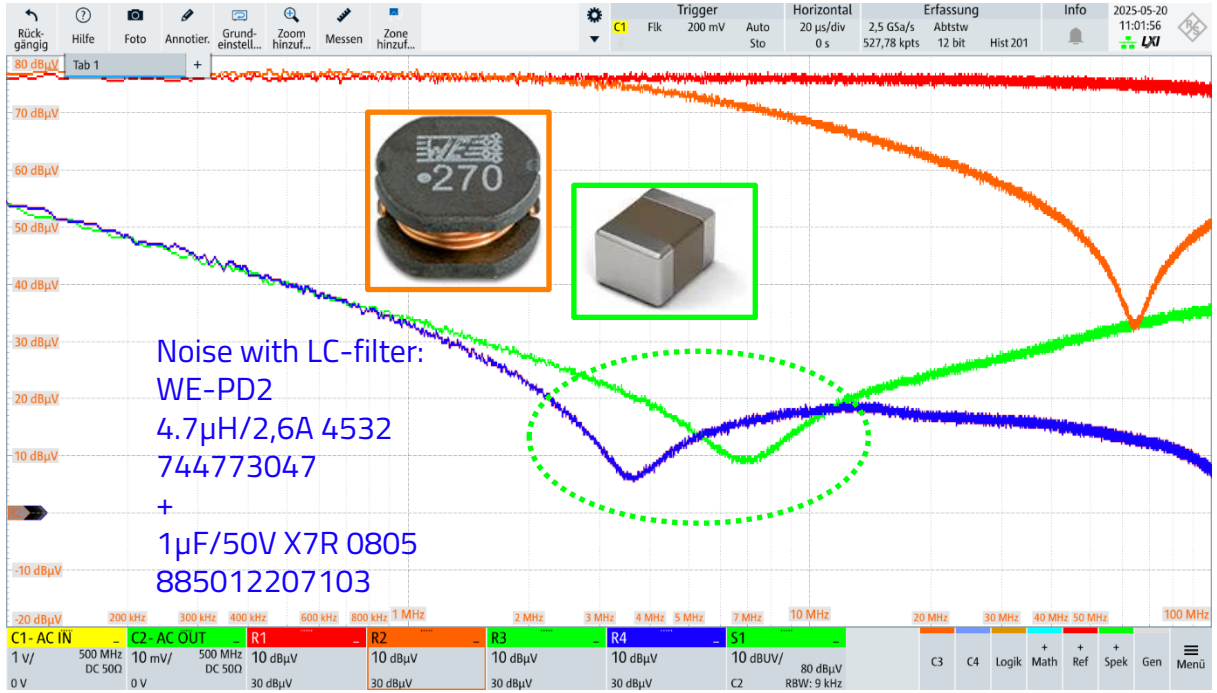


- Insertion loss for $Z_s = Z_l = 50\Omega$:

$$A_{\mathrm{dm},50} = 20 \cdot \log \left| 1 + 25\Omega \cdot Y_C + \frac{Z_L}{100\Omega} + \frac{Z_L \cdot Y_C}{2} \right| \mathrm{dB}$$

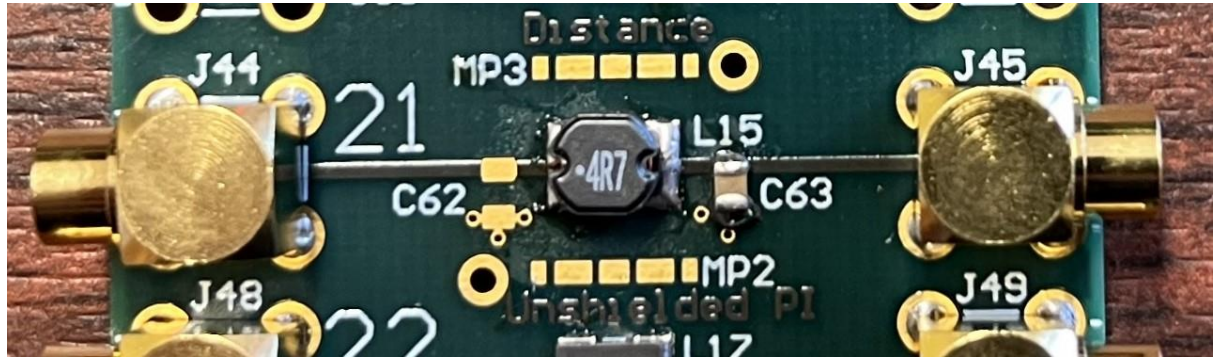
- General insertion loss:

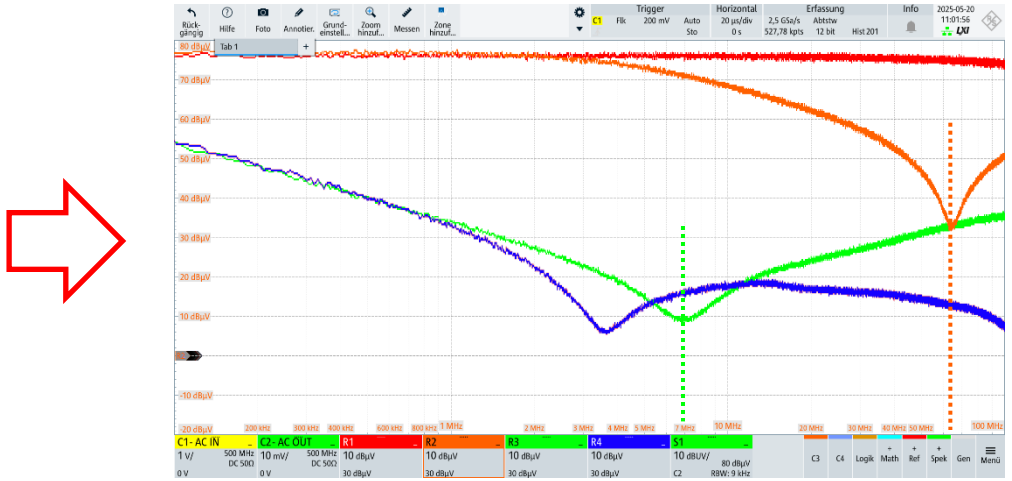
$$A_{\mathrm{dm}} = 20 \cdot \log \left| 1 + \frac{Z_l \cdot Y_C \cdot (Z_L + Z_s) + Z_L}{Z_s + Z_l} \right| \mathrm{dB}$$

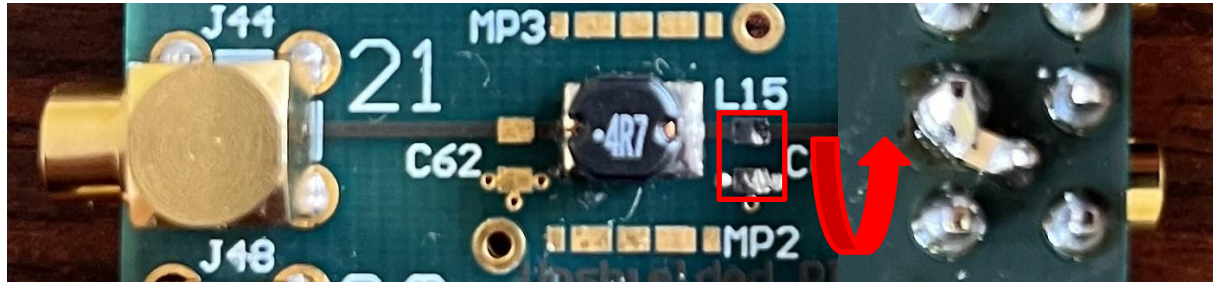


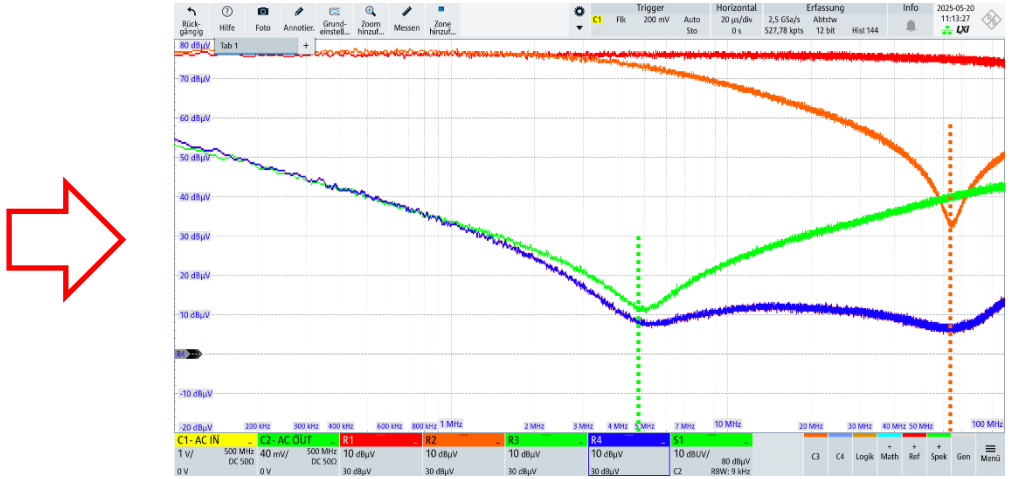
Filter Arrangement

Filter capacitor position (Top / Bottom)





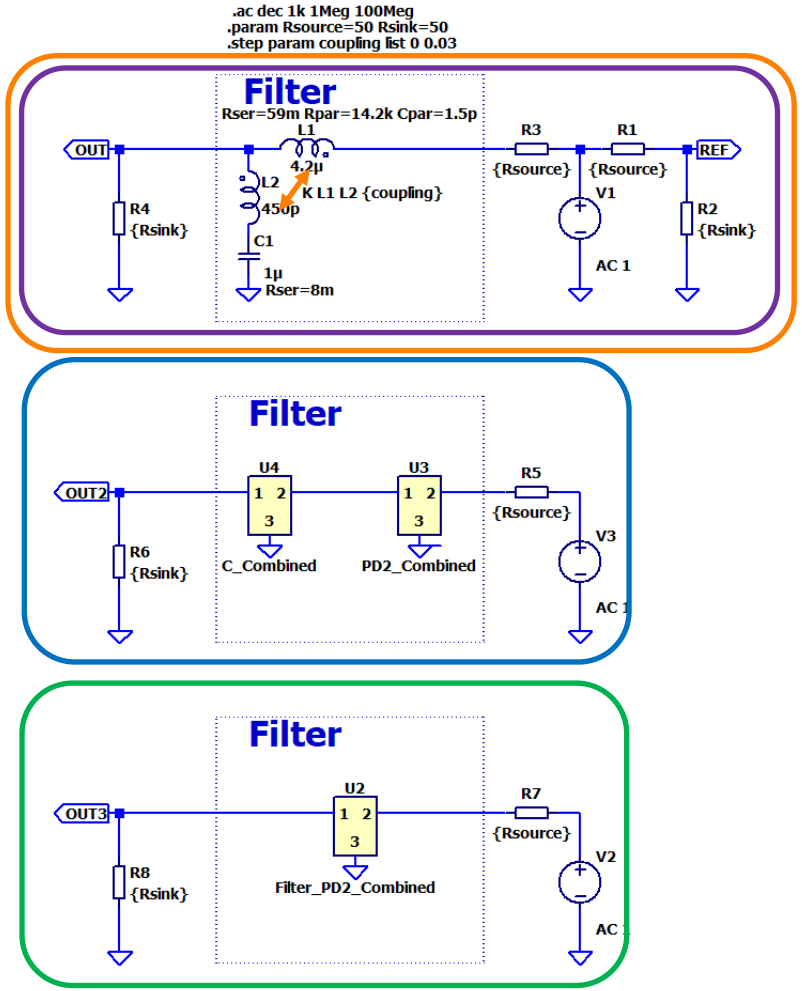




Filter Arrangement

LTspice simulation - Filter PD2 (unshielded) – capacitor on top

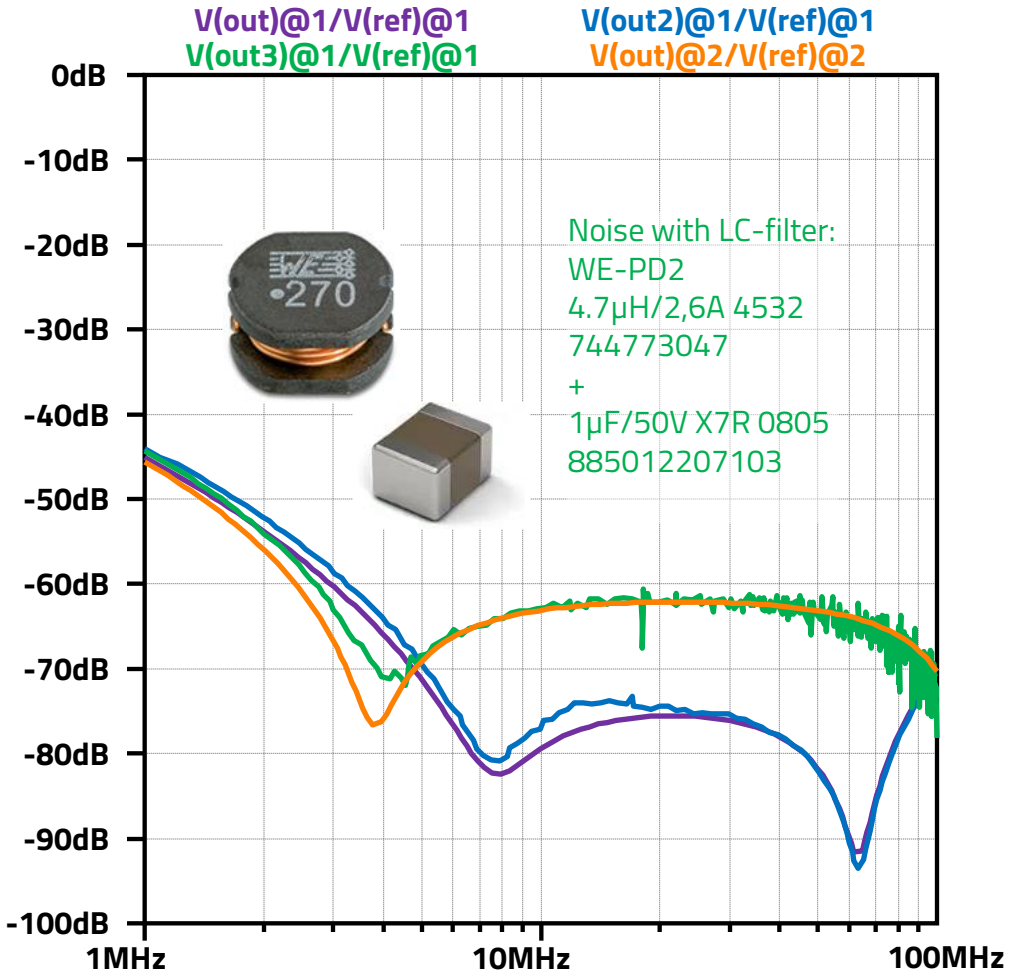
Link to LTspice simulation



Fitted equivalent circuit model with coupling coeffcient (0.03)

s-parameter single component

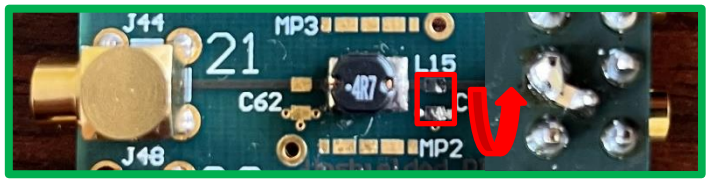
s-parameter entire filter



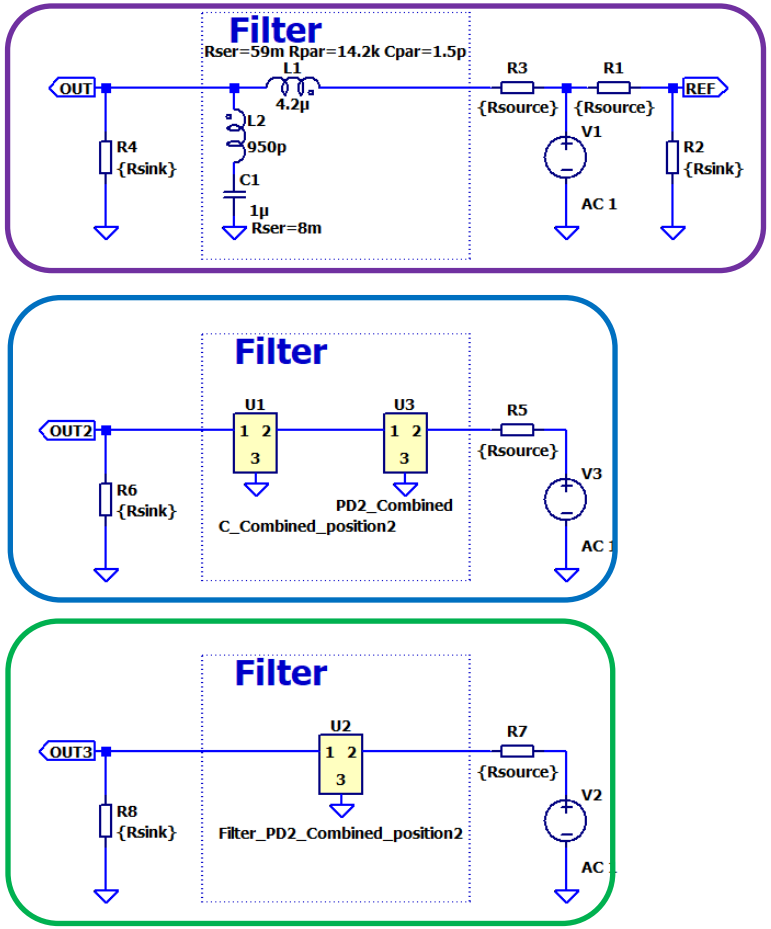
Filter Arrangement

LTspice simulation - Filter PD2 (unshielded) – capacitor on bottom

Link to LTspice simulation



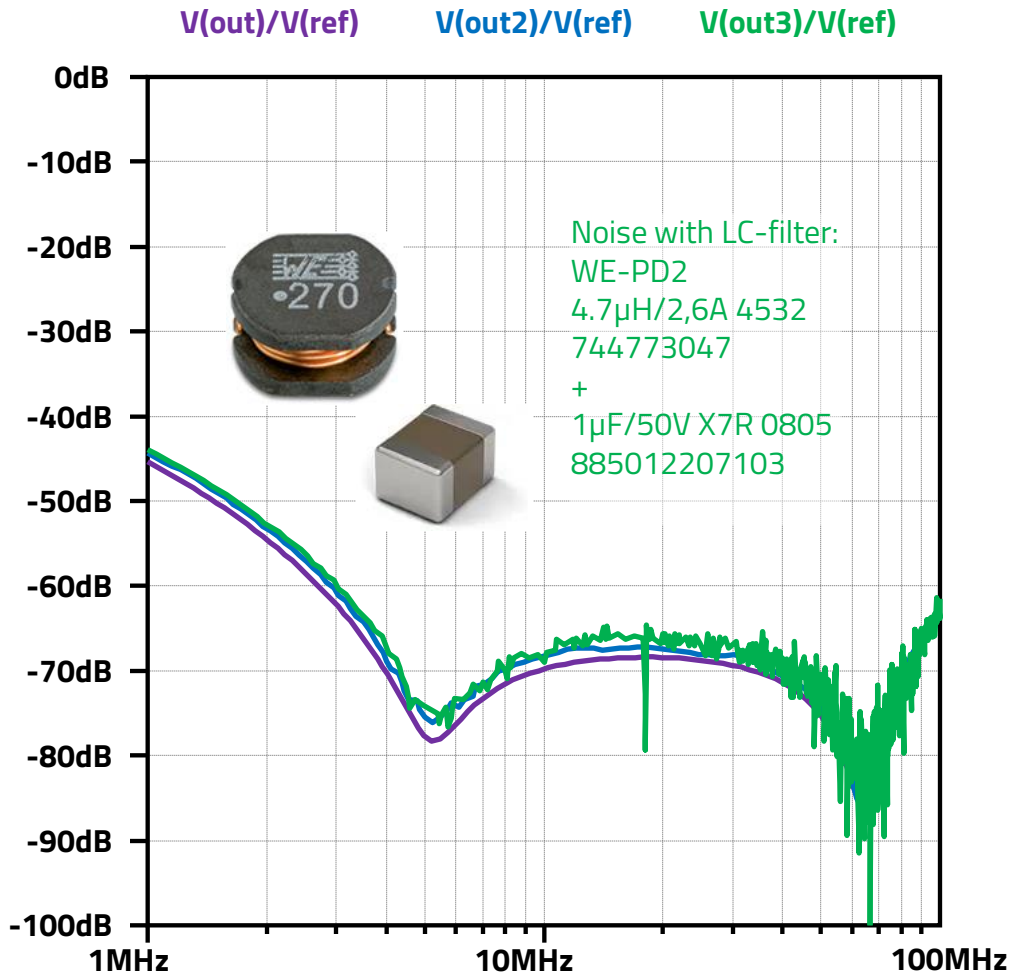
.ac dec 1k 1Meg 100Meg
.param Rsource=50 Rsink=50



Fitted equivalent circuit model

s-parameter single component

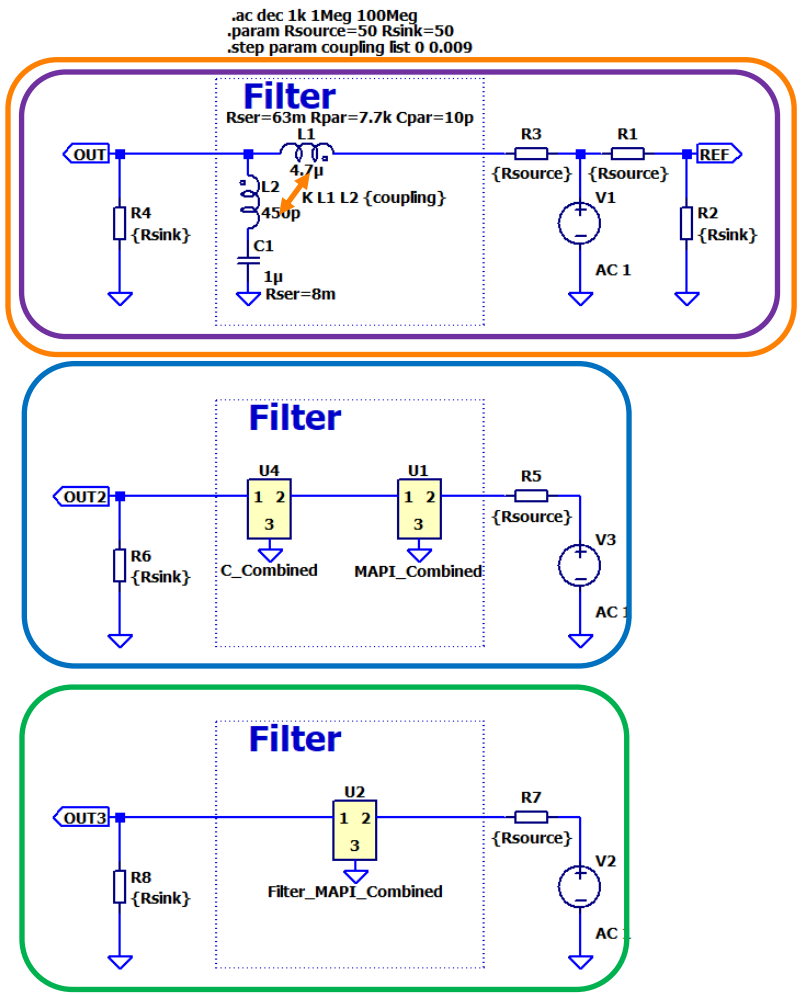
s-parameter entire filter



Filter Arrangement

LTspice simulation - Filter MAPI (molded) – capacitor on top

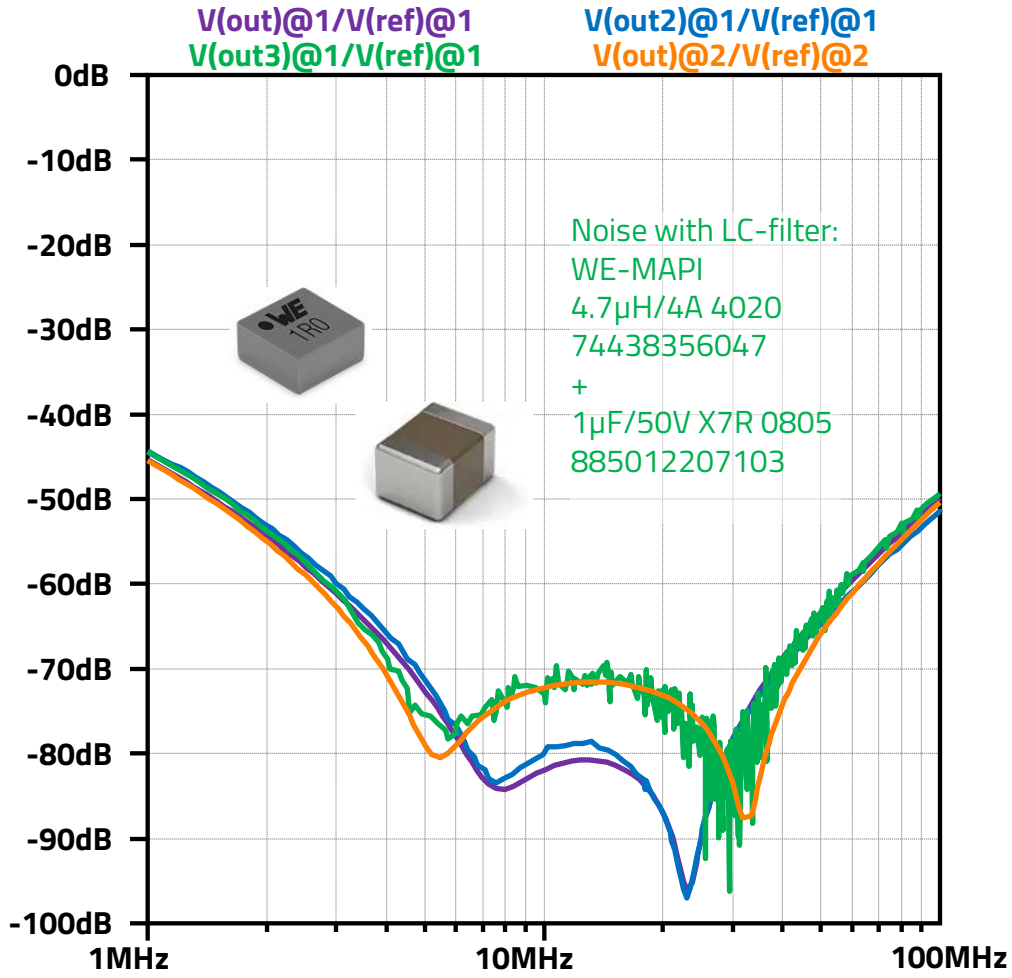
Link to LTspice simulation



Fitted equivalent circuit model with coupling coeffcient (0.009)

s-parameter single component

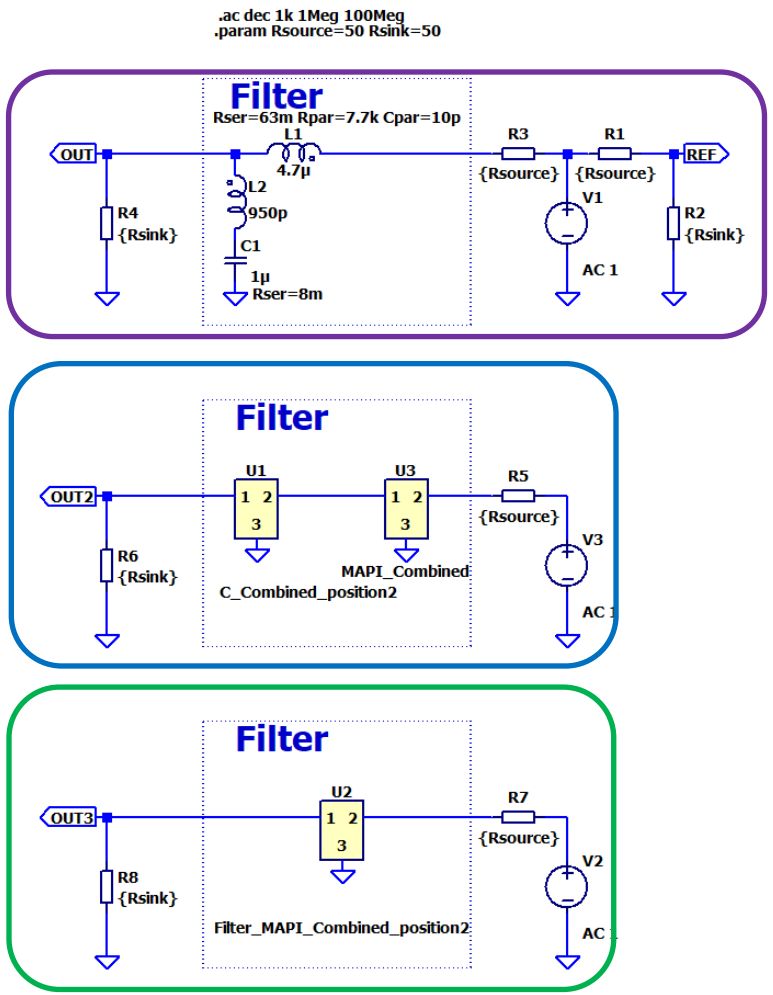
s-parameter entire filter



Filter Arrangement

LTspice simulation - Filter MAPI (molded) – capacitor on bottom

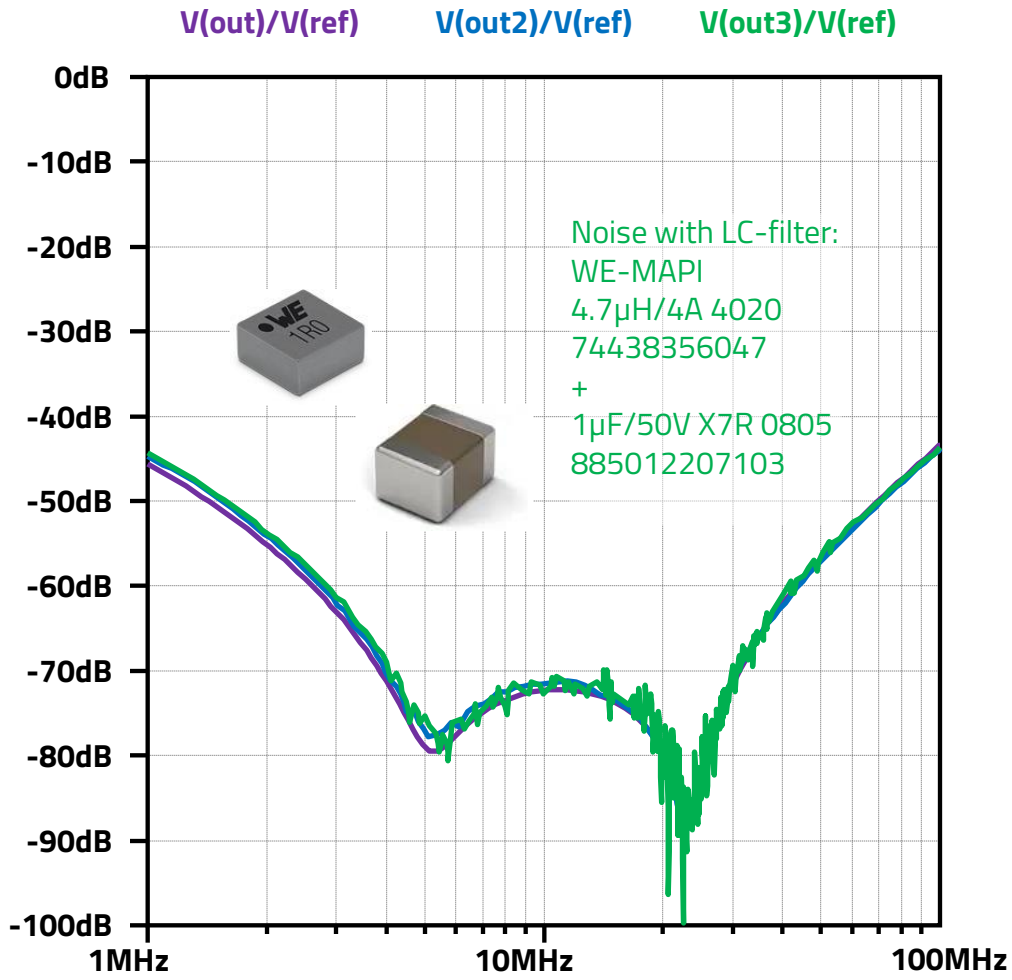
Link to LTspice simulation



Fitted equivalent circuit model

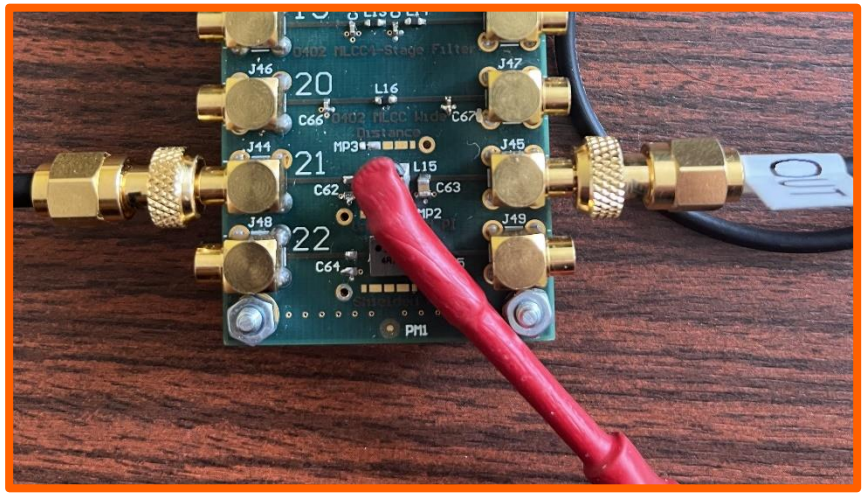
s-parameter single component

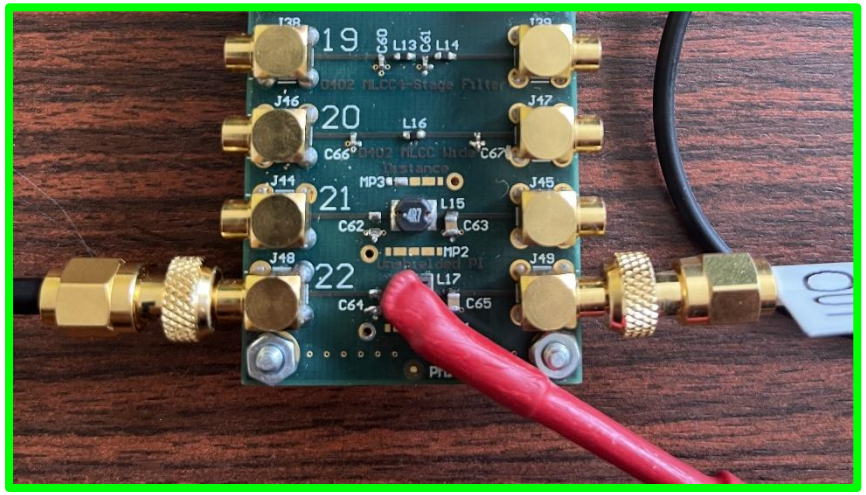
s-parameter entire filter

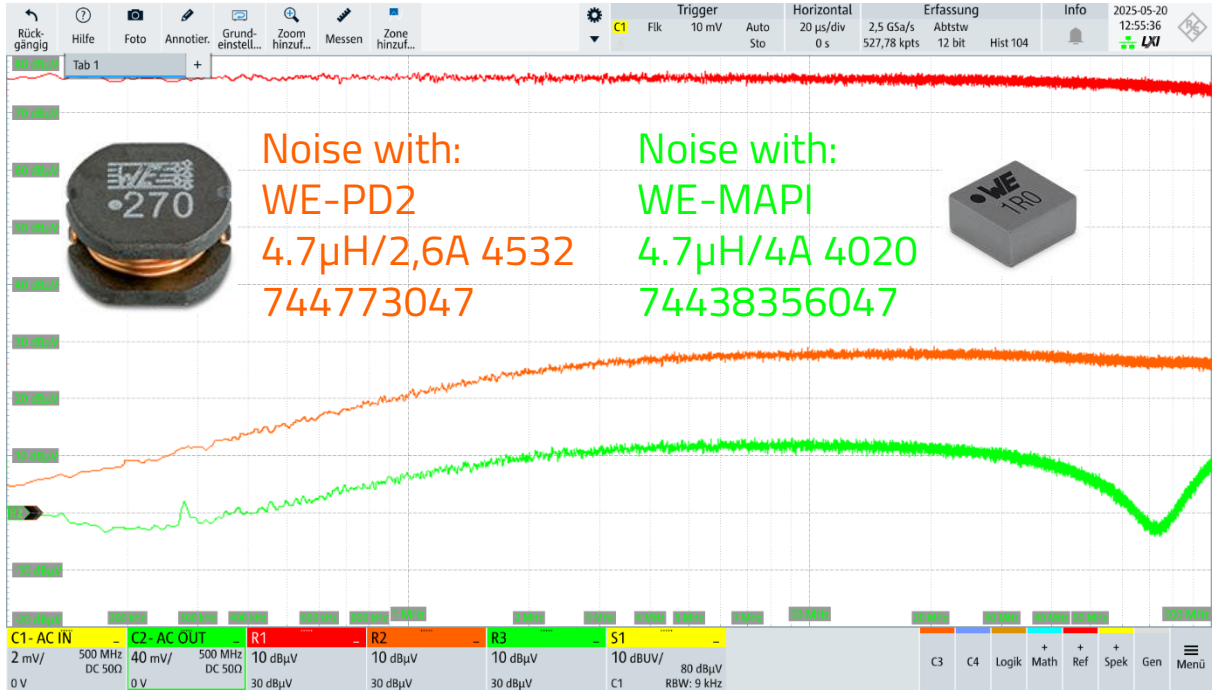


Near field (H-field)

Unshielded vs. molded filter choke



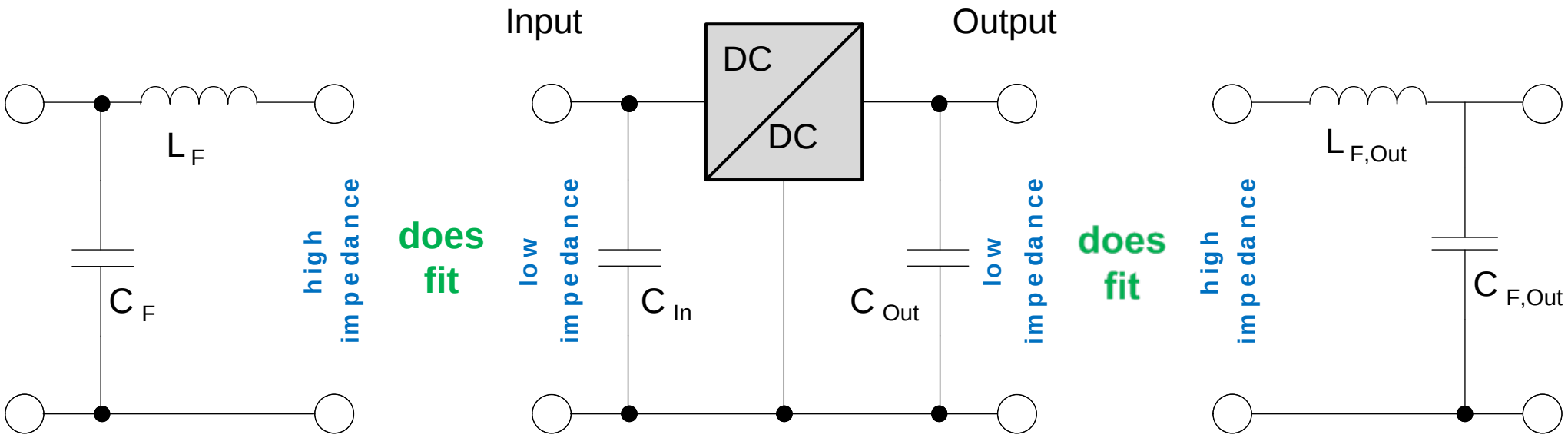




DM FILTER

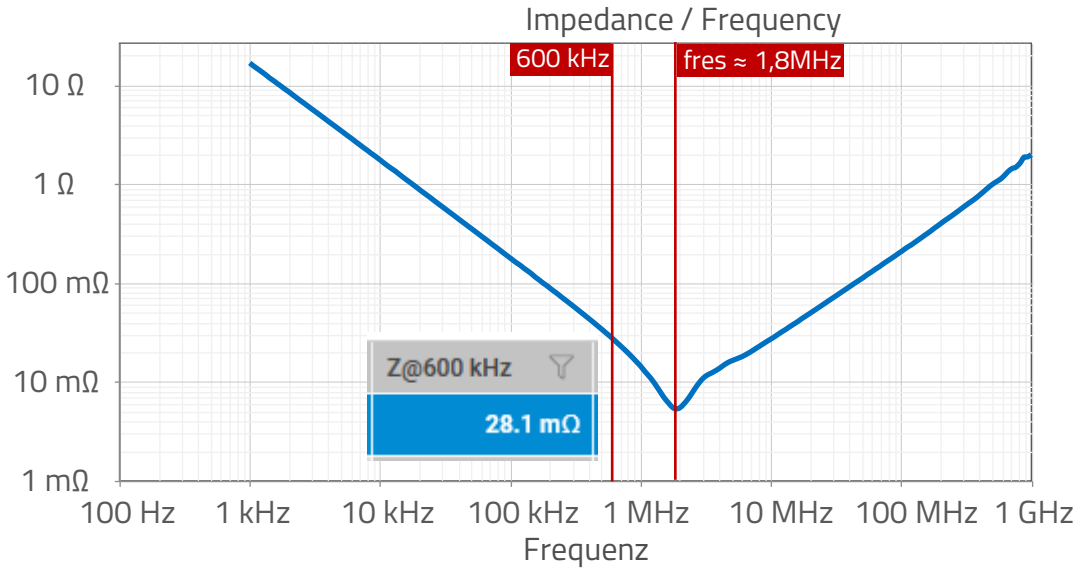
I/O Filter Arrangement for DCDC

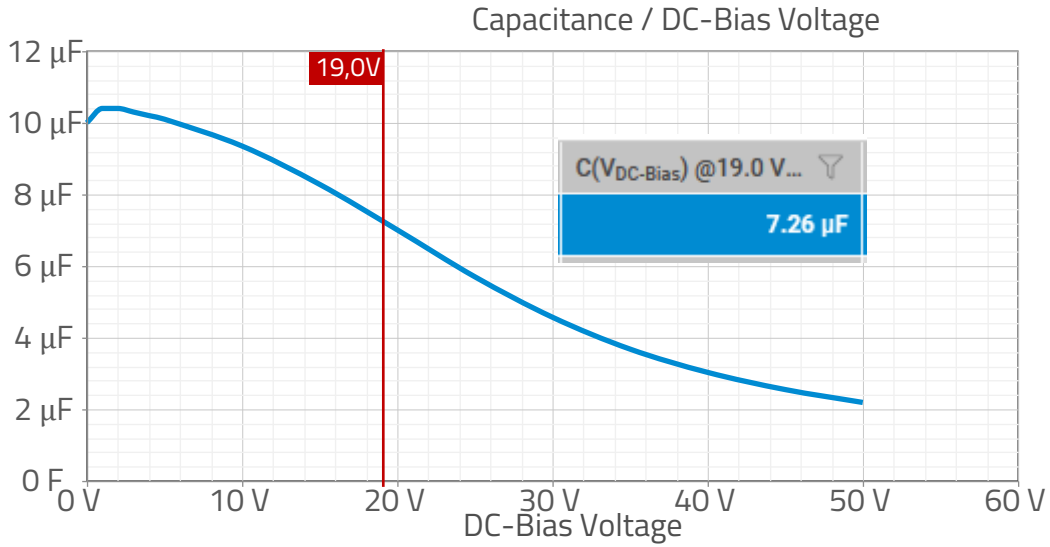
2nd order LC filter to filter differential mode conducted EMI



Filter calculation by hand

1. Selection of the filter capacitor with REDEXPERT (https://we-online.com/re/5sH1x8Bx):
   - C>1µF with low ESR and ESL: MLCC (MLCC with DC-Bias consideration!), Film, Polymer or Polymer Hybrid
   - and $f_{r,Cin} > f_{sw}$ (Switching frequency) is a good choice
   - ➢ 10µF/50V 1210 X7R - 885012209073





Filter calculation by hand

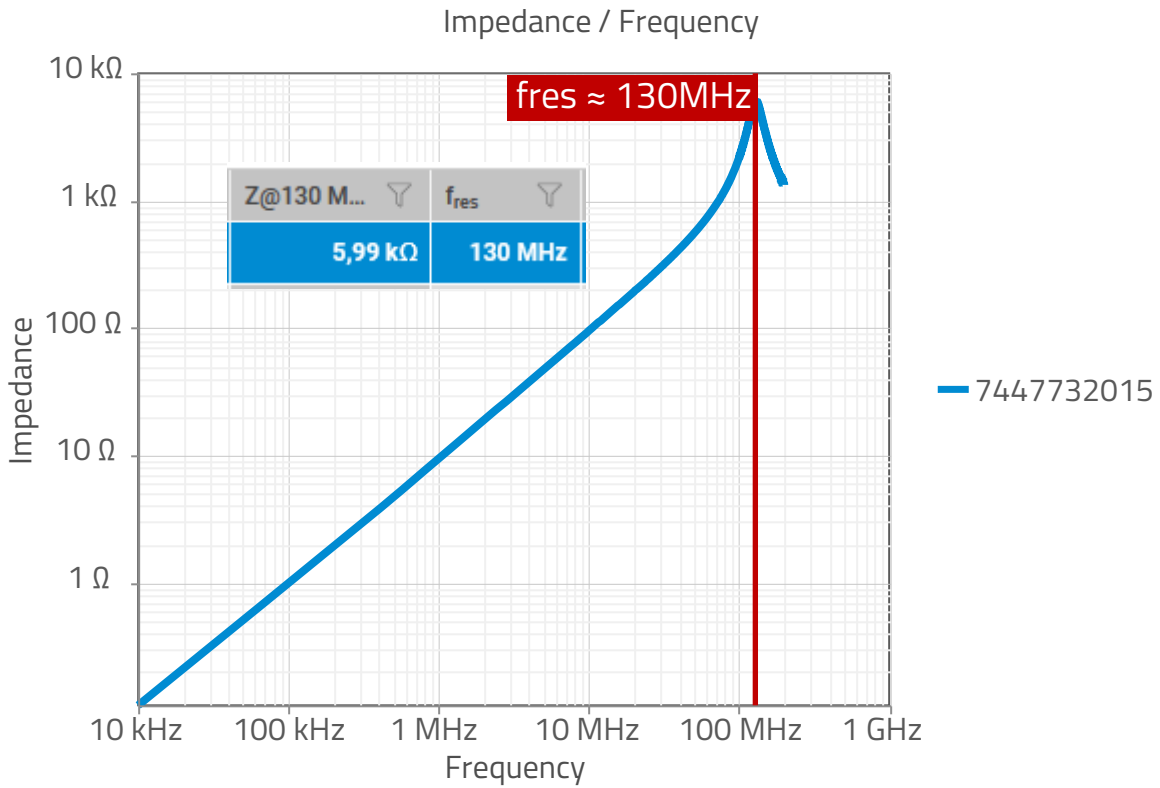
2. Select corner frequency of the input filter max. 1/10 of the switching frequency of the switching regulator for min. 40dB attenuation at the switching frequency

3. Calculation of filter inductance:

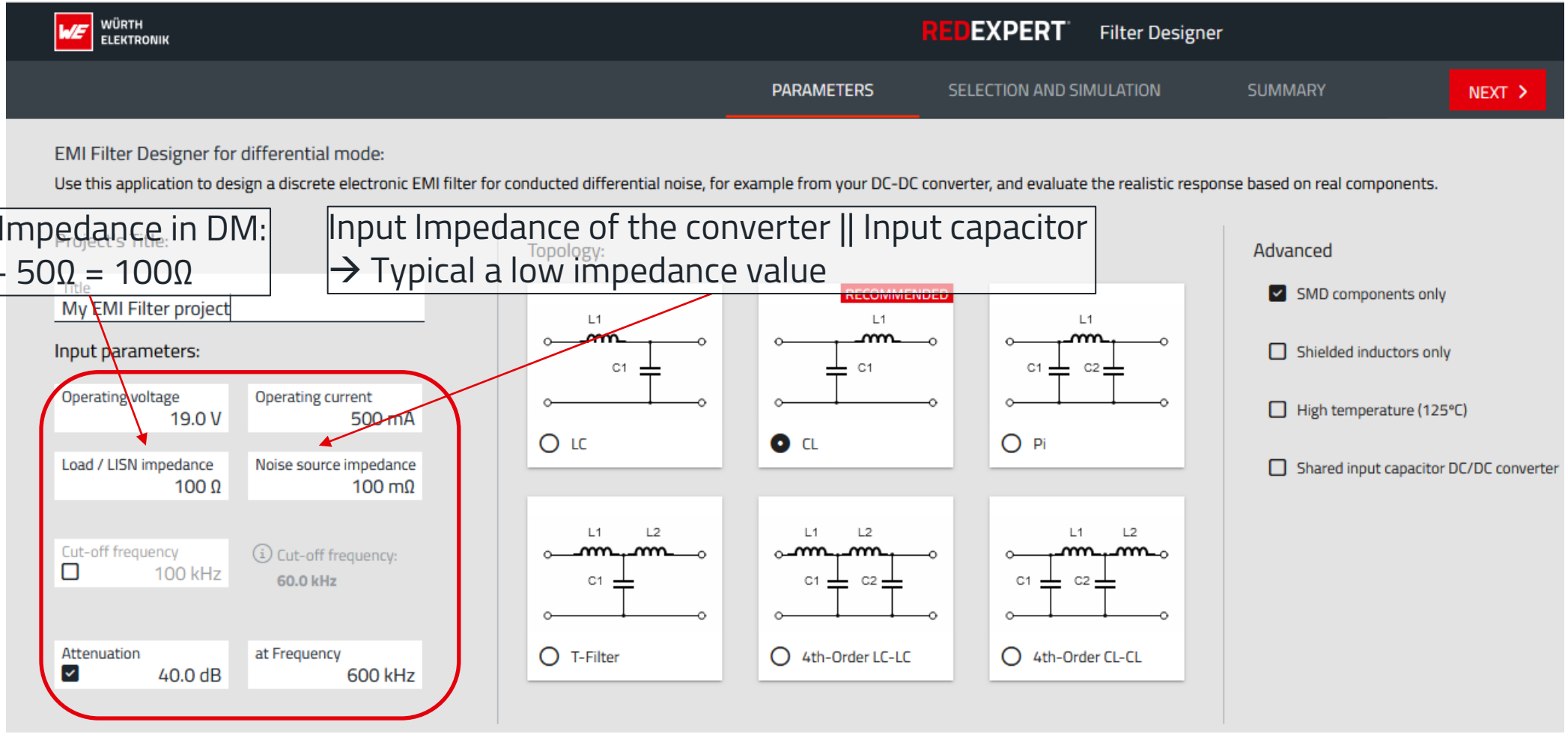
$$f_c = \frac{1}{2\pi\sqrt{LC}} \rightarrow L_F = \frac{1}{(2\pi\frac{1}{10}f_{sw})^2 \cdot C_F}$$

$$= \frac{1}{(2\pi\frac{1}{10}600kHz)^2 \cdot 7{,}26\mu F} \approx 1\mu H$$

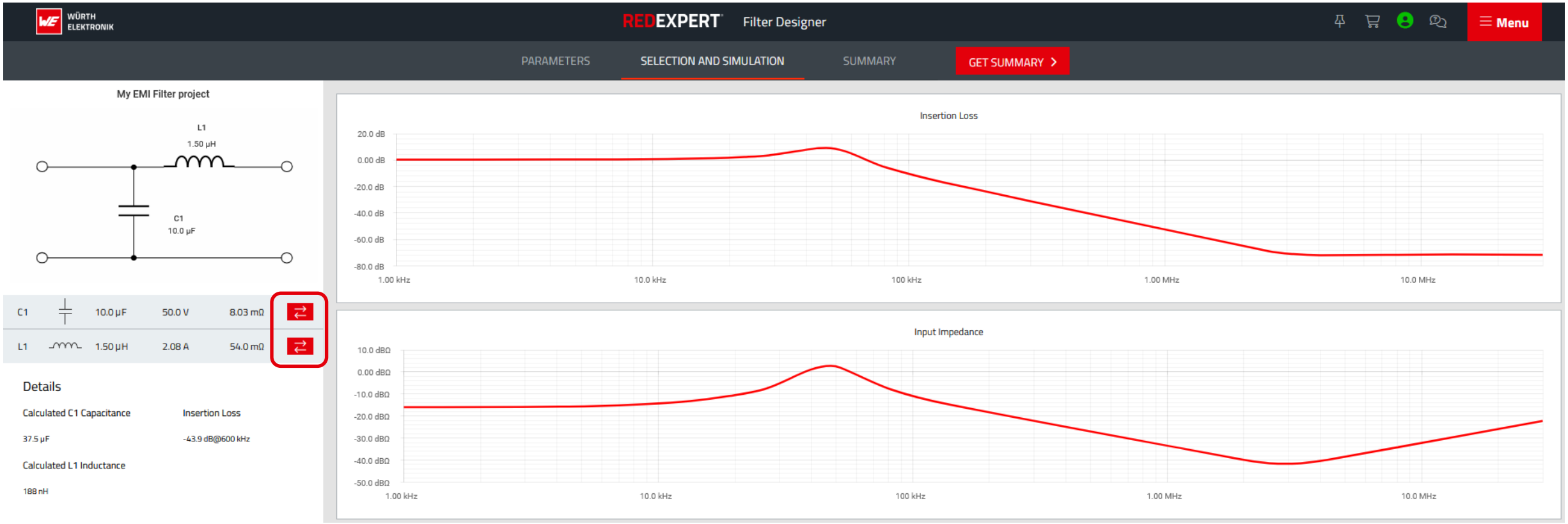
4. Selection of the next largest inductance value
   - 1,5µH e.g. 1,5µH/2,08A PD2 3512 – 7447732015
   - SRF of the inductor ideally more than 30MHz



Filter Simulation with REDEXPERT Filter Designer



Filter Simulation with REDEXPERT Filter Designer



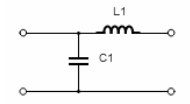
Filter Simulation with REDEXPERT Filter Designer

WÜRTH ELEKTRONIK

REDEXPERT Filter Designer

PARAMETERS | SELECTION AND SIMULATION | SUMMARY

Circuit Schematic



Specifications Edit

"My EMI Filter project"

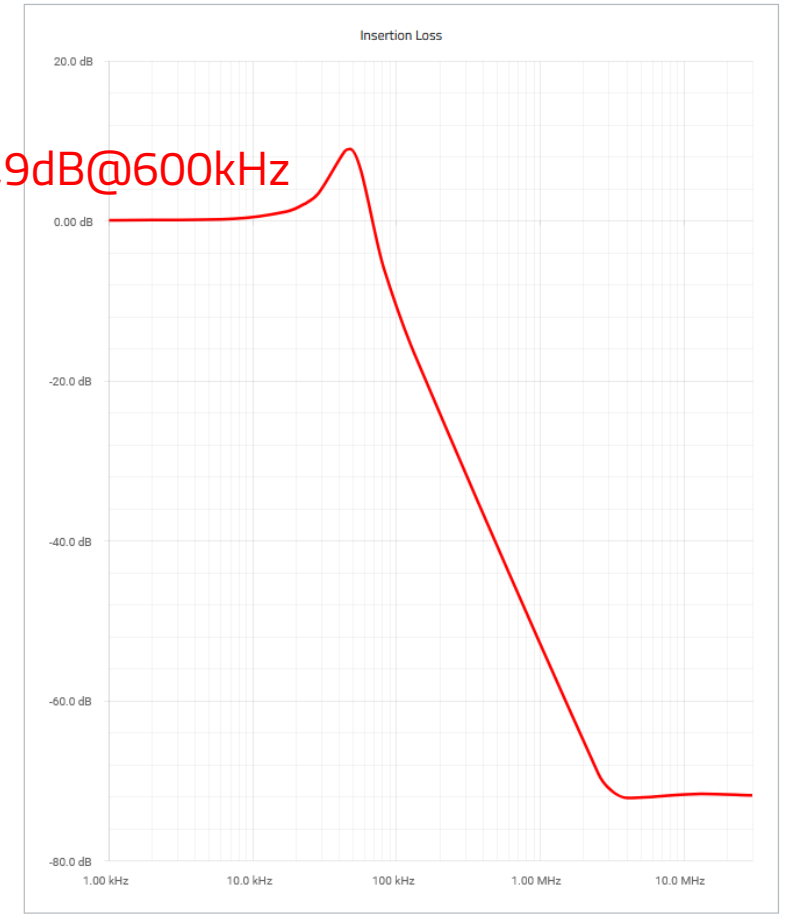
TYPE: CL
V_{op}: 19.0 V
I_{op}: 500 mA
LOAD / LISN IMPEDANCE: 100 Ω
NOISE SOURCE IMPEDANCE: 100 mΩ
ILOSS -43.9 dB@600 kHz

-43,9dB@600kHz

Bill Of Materials ADD

#	N...	Order Code	Value	Properties	Qty
1.	C1	885012209073	10.0 µF	Capacitance = 10.0 µF Footprint = 8.00 mm² Rated Voltage = 50.0 V Height = 2.50 mm Type = X7R	1
2.	L1	7447732015	1.50 µH	Footprint = 8.40 mm² Inductance = 1.50 µH Rated Current = 2.08 A DC Resistance = 54.0 mΩ	1

Simulation Responses



Filter Simulation with LTSpice

Download, installation paths

- Download from the Analog Devices website → https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html
- Current version (11/2024): **24.0.12**
- Previous version: **17.0.42**

- Installation paths:
  - Version 17.0.42
    - Program → C:\Program Files\LTC\LTspiceXVII
    - User directory → C:\Users \ <*name*> \Documents\LTspiceXVII
  - Version 24.0.12
    - Program → C:\Users \ <*Name*> \AppData\Local\Programs\ADI\LTspice
      User directory → C:\Users \ <*Name*> \AppData\Local\LTspice

Filter Simulation with LTSpice

Folder structure

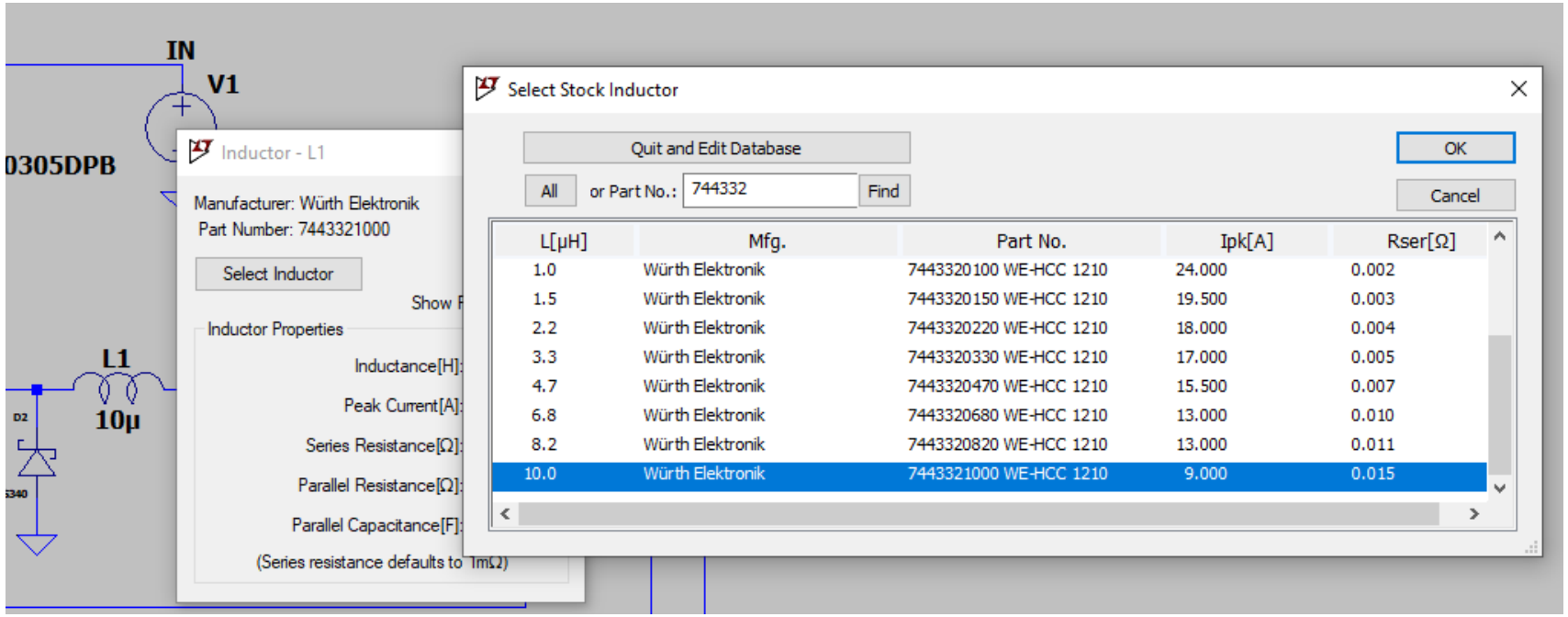
- Example circuits → C :\Users\ <*Name*> \ AppData\Local\LTspice\examples\
  - **Applications**
  - **Educational**
- Libraries → C:\Users\ <*Name*> \ AppData\Local\LTspice\lib\
  - **cmp** → standard components (.bead, .bjt, .cap, .dio, .ind, .jft, .mos, .res)
  - **sub** → Subcircuits (Linear Technology, Analog Devices, Maxim Integrated) with subfolders for other manufacturers, e.g. Würth Elektronik (\Contrib\Wurth)
  - **sym** → circuit symbols, also with "\Contrib" subfolder

Filter Simulation with LTSpice

- Würth Elektronik components are contained in the following standard libraries:
  - standard.bead
  - standard.cap
  - standard.ind
- Further components → C :\Users \ <*Name*> \AppData\Local\LTspice\lib\sym\Contrib\Wurth\
  - Automotive → common mode chokes, HF coils
  - Capacitors\MLCC → Ceramic capacitors (NP0, X5R, X7R) with DC bias modeling
  - EMC components → common mode chokes, line filter modules
  - Optoelectronics → IR LEDs, UV LEDs, laser diode, colored LEDs, white LEDs, optocouplers
  - PowerMagnetics → Coupled inductors, audio filter inductors, PFC chokes, power transformers, current transformers
  - Signal → HF inductors, signal transformers

Filter Simulation with LTSpice

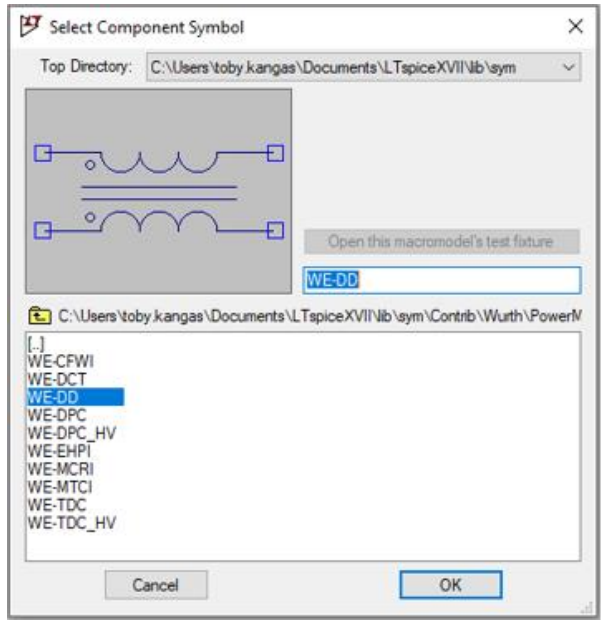
Built-in standard component libraries

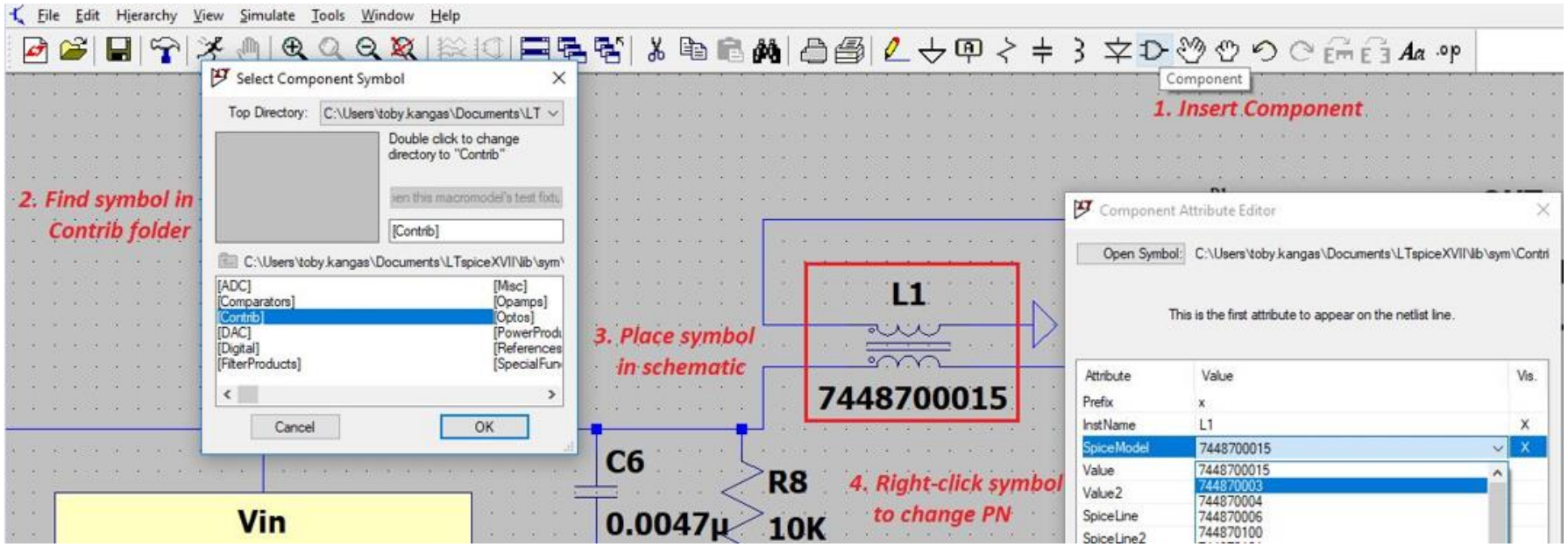


- For simple component models, LTspice offers standard libraries for capacitors, inductors, ferrite beads, as well as resistors, diodes, mosfets, and BJTs. These models use the standard equivalent circuit for that component. These models guarantee the highest simulation speed.

Filter Simulation with LTSpice

Components „Contrib“ directory

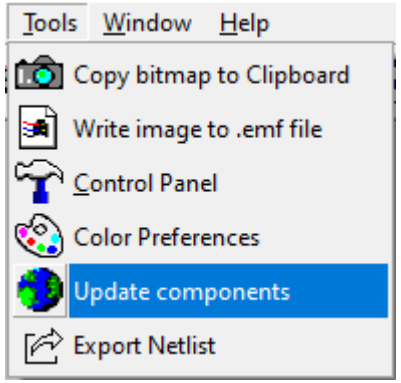




- The “Contrib” directory in the LTspice components library is a place for contributors to include their models directly in LTspice. It is sorted by manufacturer, and within our Wurth folder, the organization is structured by product type to make it easy to find the model you need. For most products, there is one symbol per series. The specific part number is chosen by right-clicking the symbol after it is placed in the schematic.

Filter Simulation with LTSpice

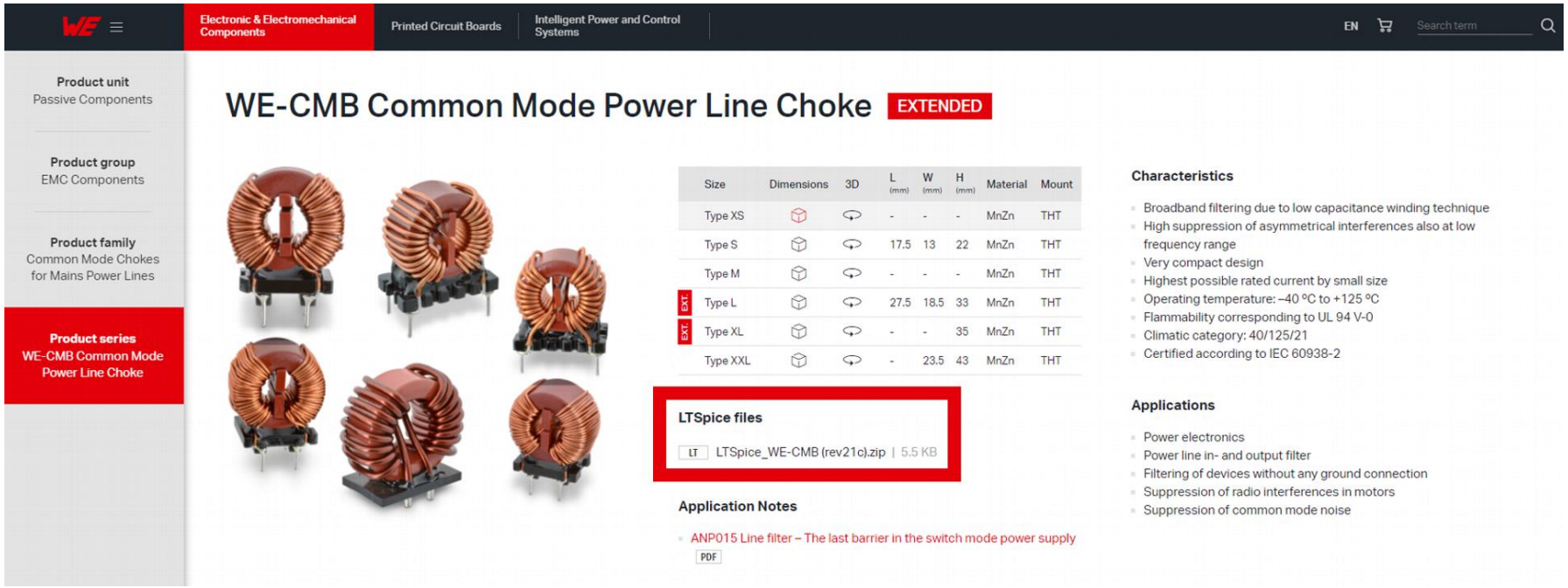
Library updates



- We have most of our component libraries in LTspice directly, and will continue to add models there. To update the LTspice libraries, select “Update Components” from the Tools menu to update your LTspice program and libraries (or “Sync Release” in older LTspice versions).

Filter Simulation with LTSpice

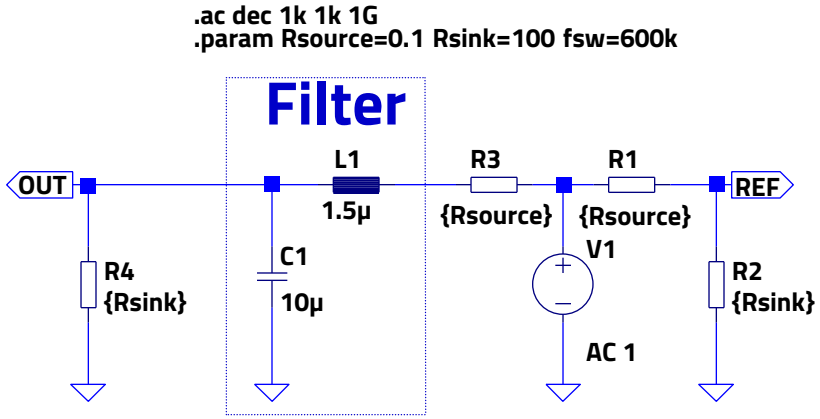
LTspice models are also available on the WE website



- Our model libraries can still be downloaded from our website if you are unable to use the “Update Components” feature (or “Sync Release” in older LTspice versions) due to your company’s IT security policies or because of other technical issues. Please also check our website if you do not find the model installed directly in LTspice. For model installation and usage instructions, please refer to the document “Using the LTspice Model Libraries” below.

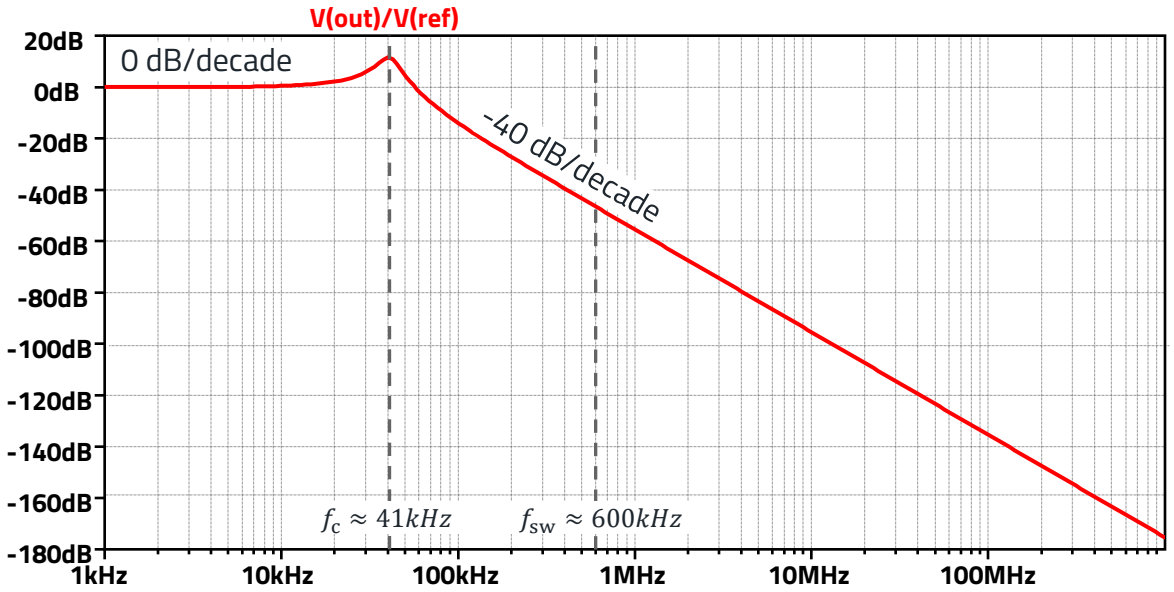
Filter Simulation with LTSpice

Ideal components



[Link to LTspice simulation]

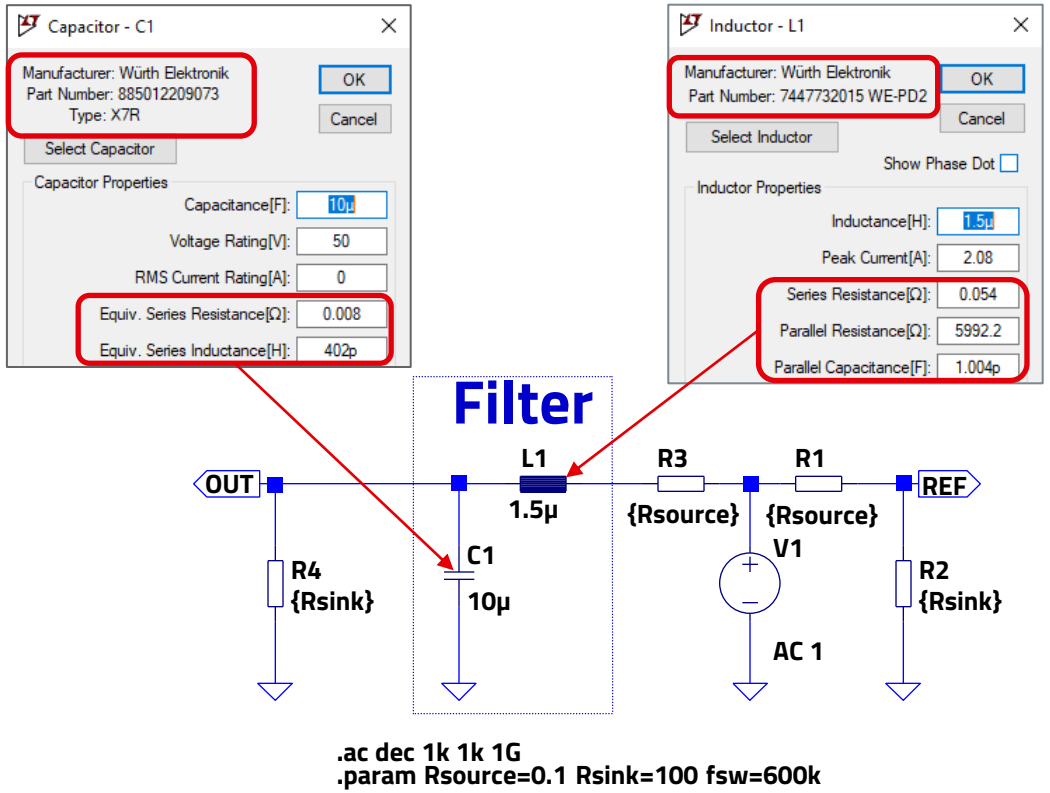
LTSpice schematic



Simulation result

Filter Simulation with LTSpice

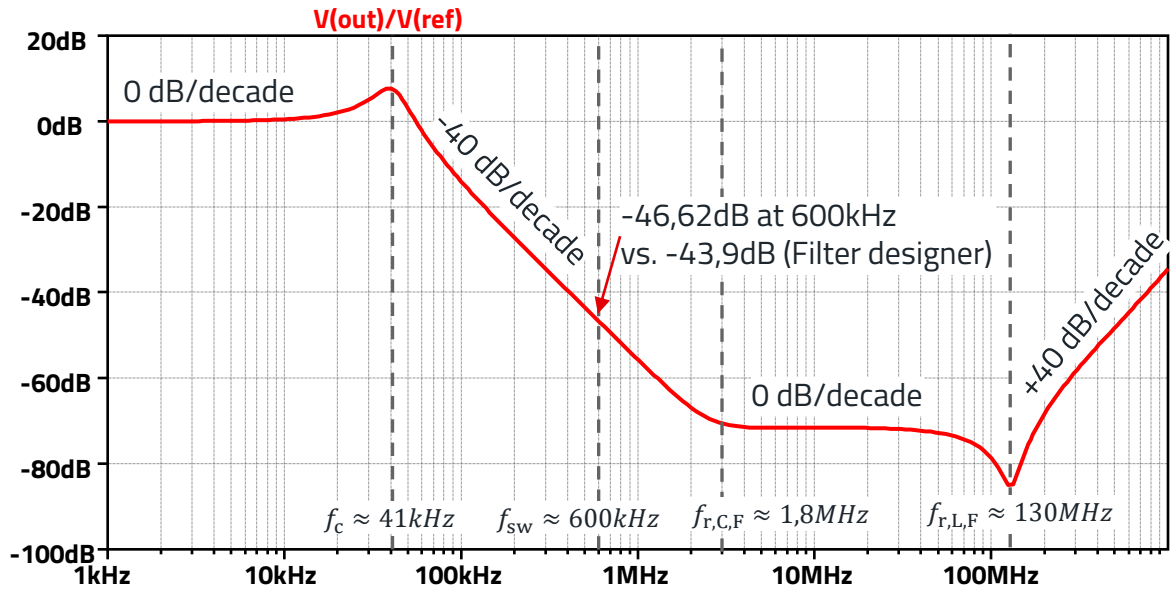
Real components



.ac dec 1k 1k 1G
.param Rsource=0.1 Rsink=100 fsw=600k

[Link to LTspice simulation]

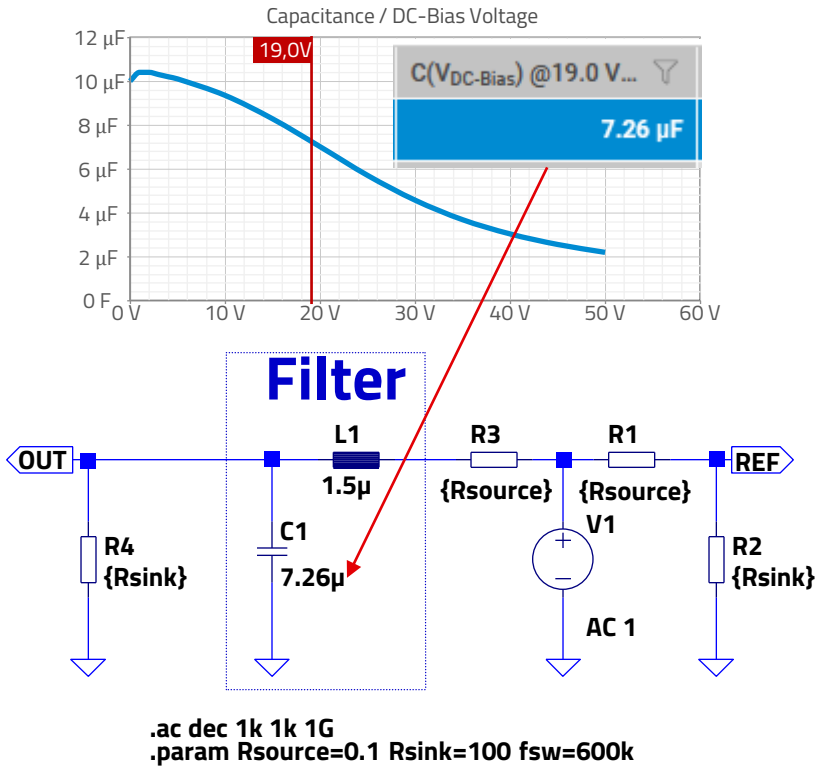
LTSpice schematic



Simulation result

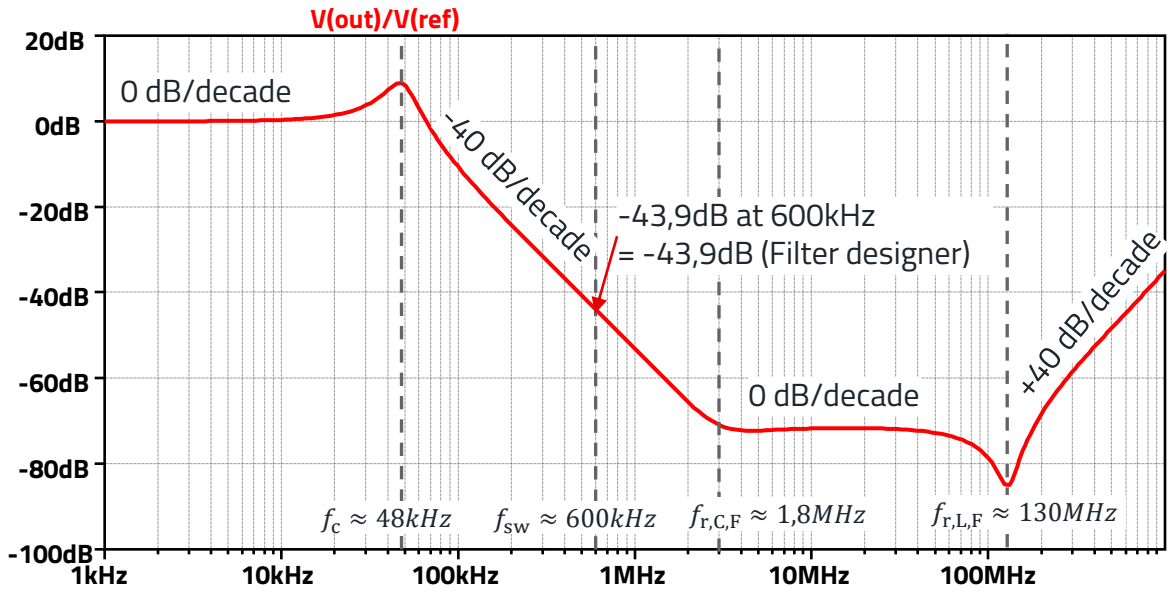
Filter Simulation with LTSpice

Real components with DC-Bias



Link to LTspice simulation

LTSpice schematic

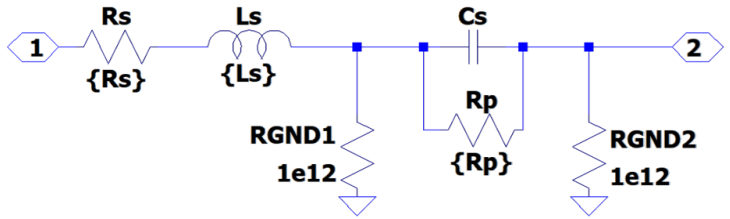


Simulation result

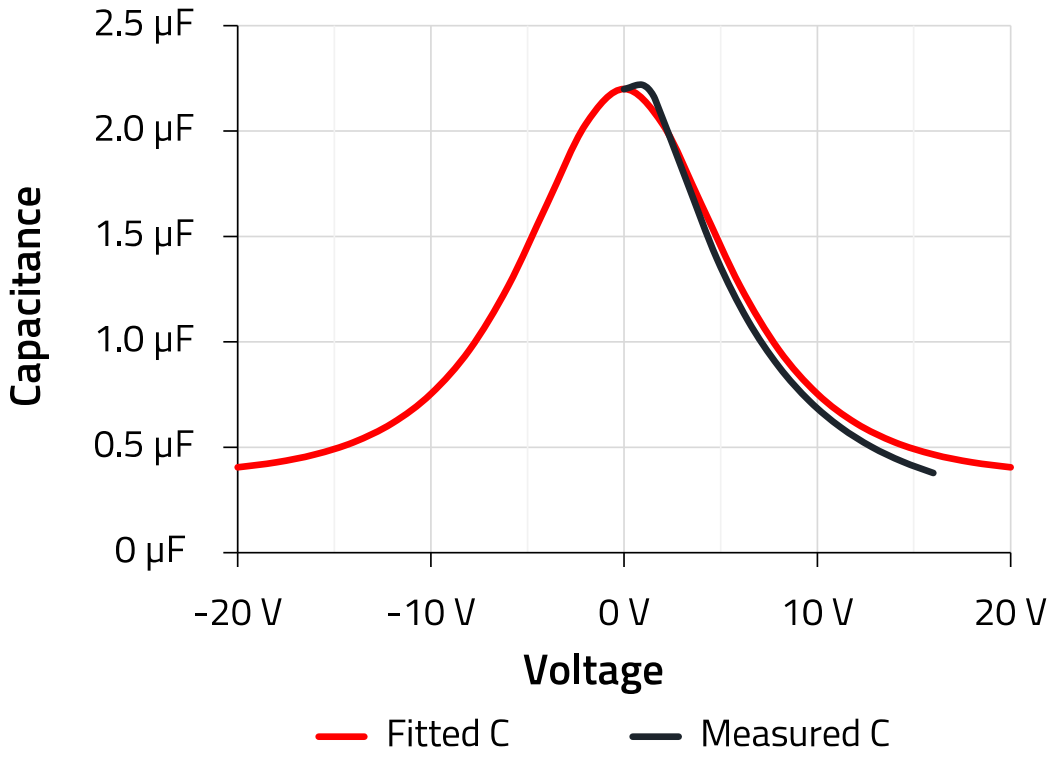
Filter Simulation with LTSpice

LTSpice Würth Elektronik - LTspice MLCC DC-bias model

- The new Würth Elektronik MLCC DC-Bias models are already integrated in LTspice 24.x
- Path:\Contrib\Wurth\Capacitors\MLCC
- Voltage vs. capacitance implementation:
  - $C = (C_0 - C_{SAT}) \cdot \operatorname{sech}\left(\frac{V}{V_{th}}\right) + C_{SAT}$
    - sech() = Hyperbolic secant



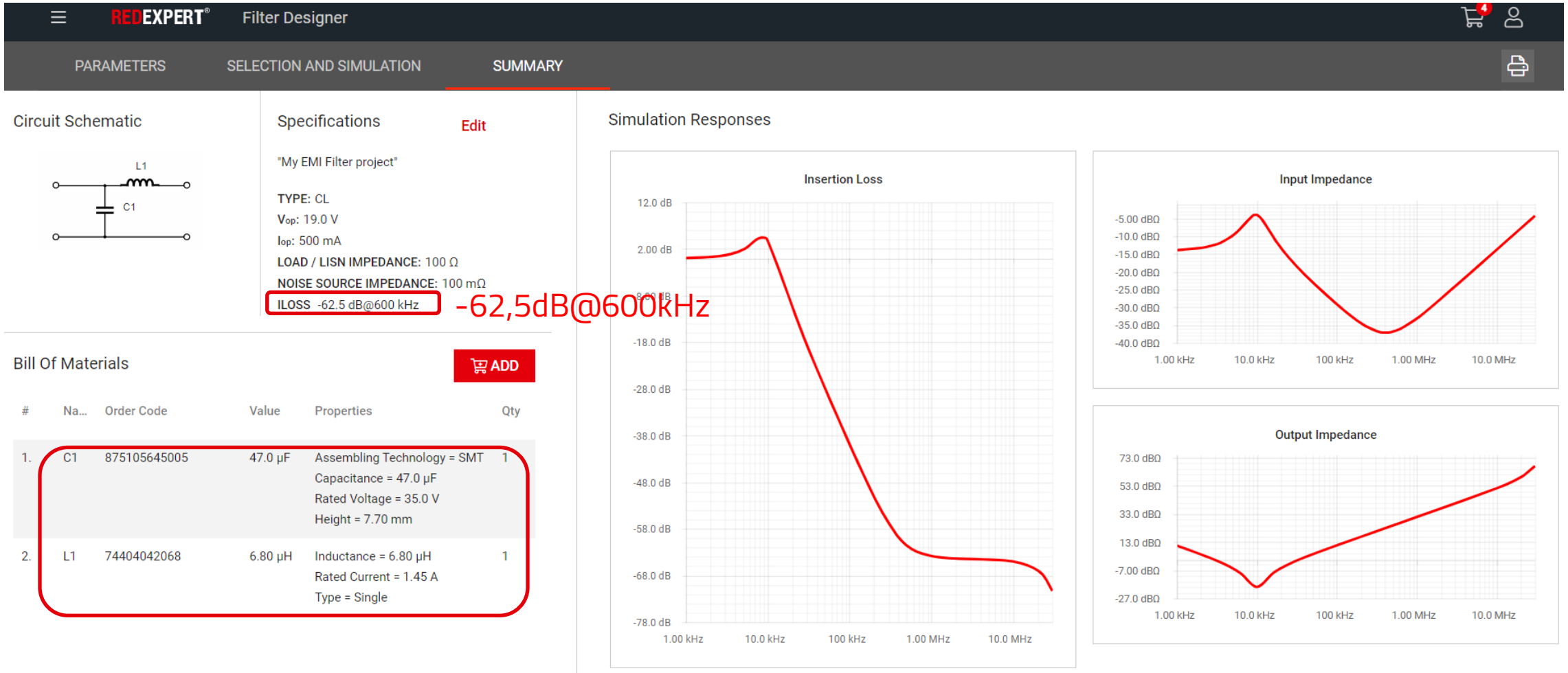
Q=(x*{Csat})+({C0}*{Vth}*arctan(sinh(x/{Vth})))-({Csat}*{Vth}*(arctan(sinh(x/{Vth}))))
.param Rs=2.2E-6 Ls=2.59E-10 Rp=5e7 C0=2.2E-6 Csat=3.62E-7 Vth=4.49



Measured and fitted voltage dependent behavior of capacitance.
Part number: 885012106018, C: 2.2µF, Matchcode: WCAP-CSGP, Size: 0603, Material: X5R, V_R: 16 V.

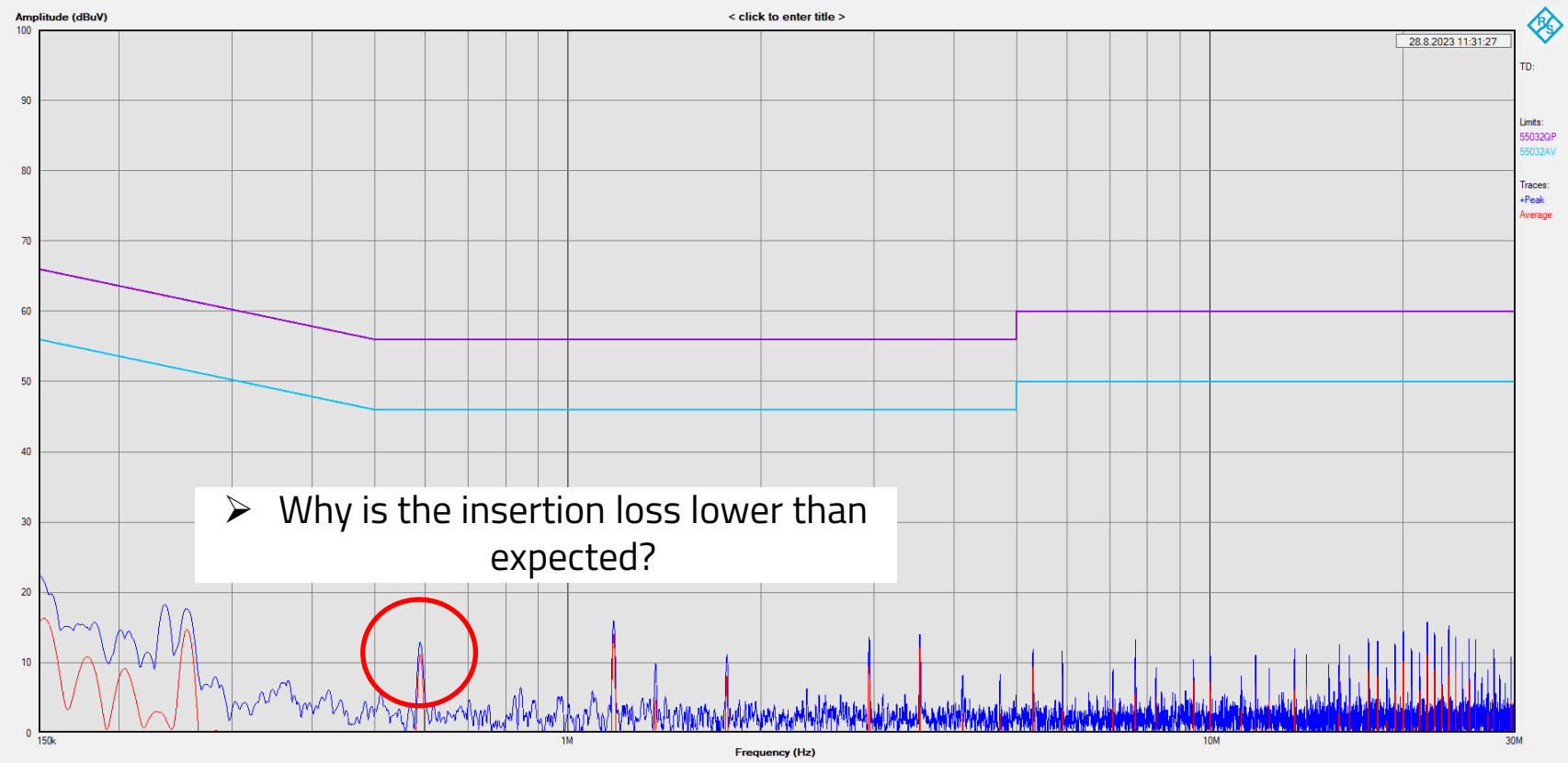
Filter Simulation with REDEXPERT Filter Designer - Good Design

Good choice to filter the range from 150kHz to 30MHz



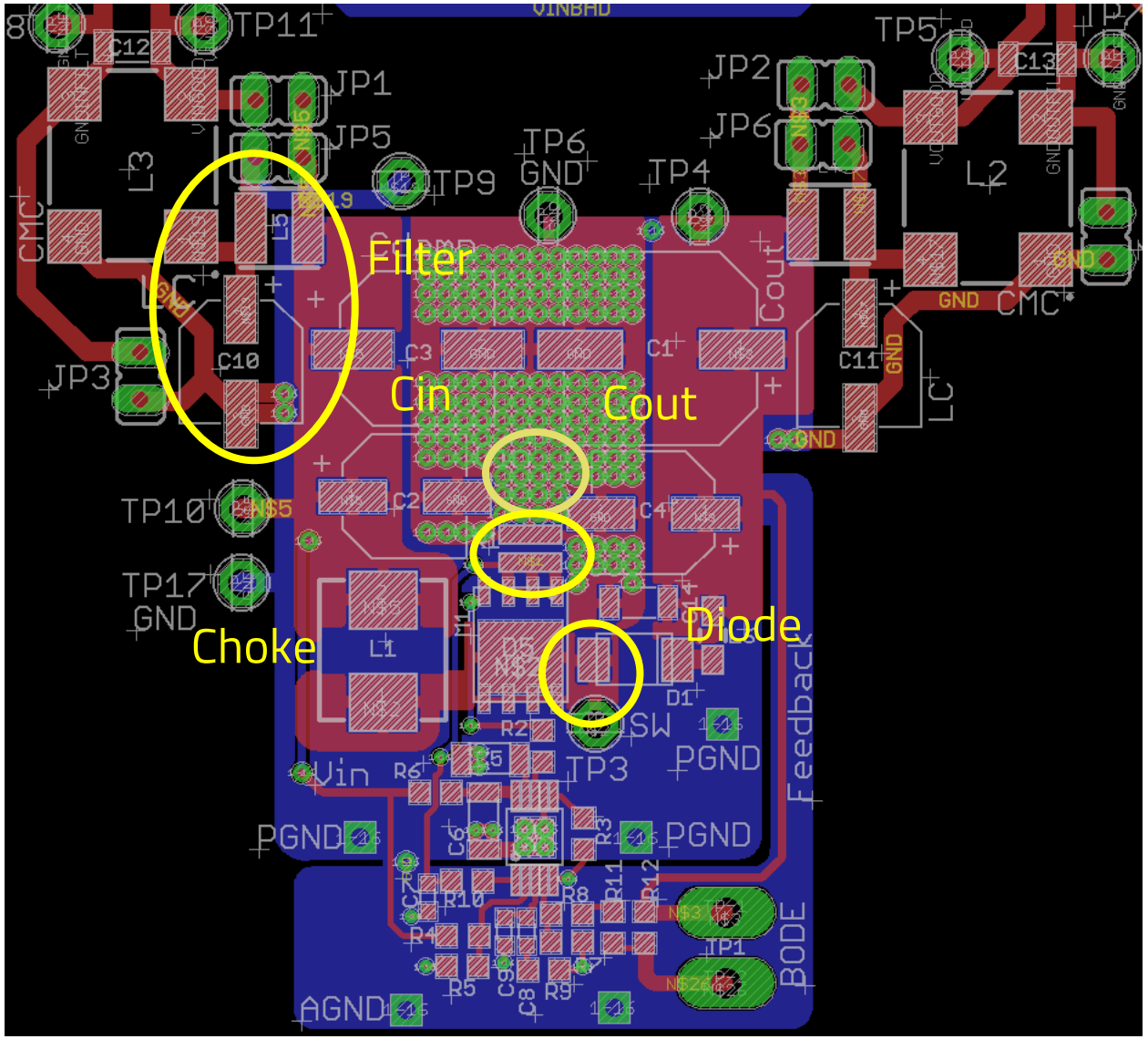
Verification of the filter effect - Good Design

DM noise on input with Filter



Insertion loss around 40dB (but 62.5dB calculated with REDEXPERT)

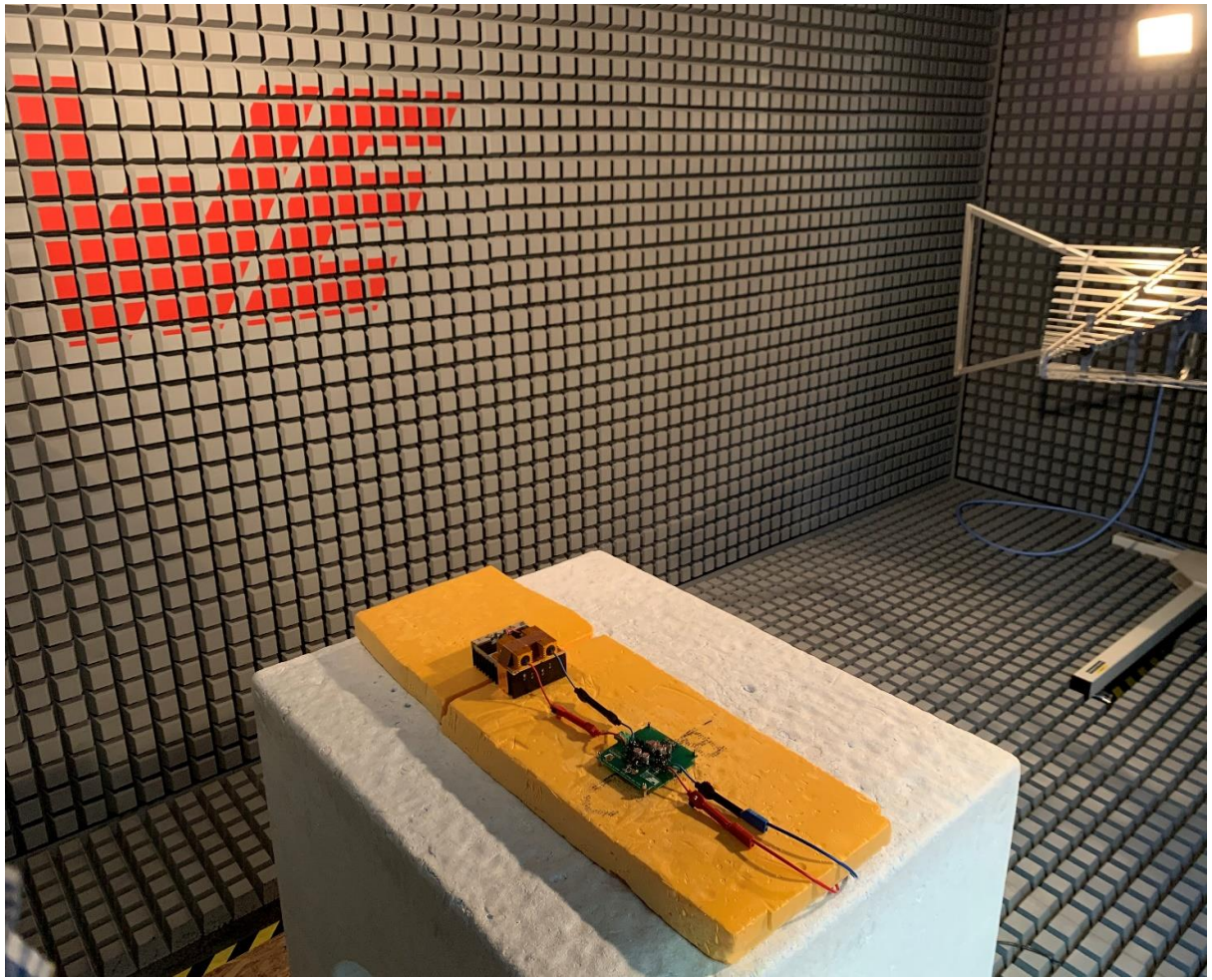
PCB Layout - Good Design

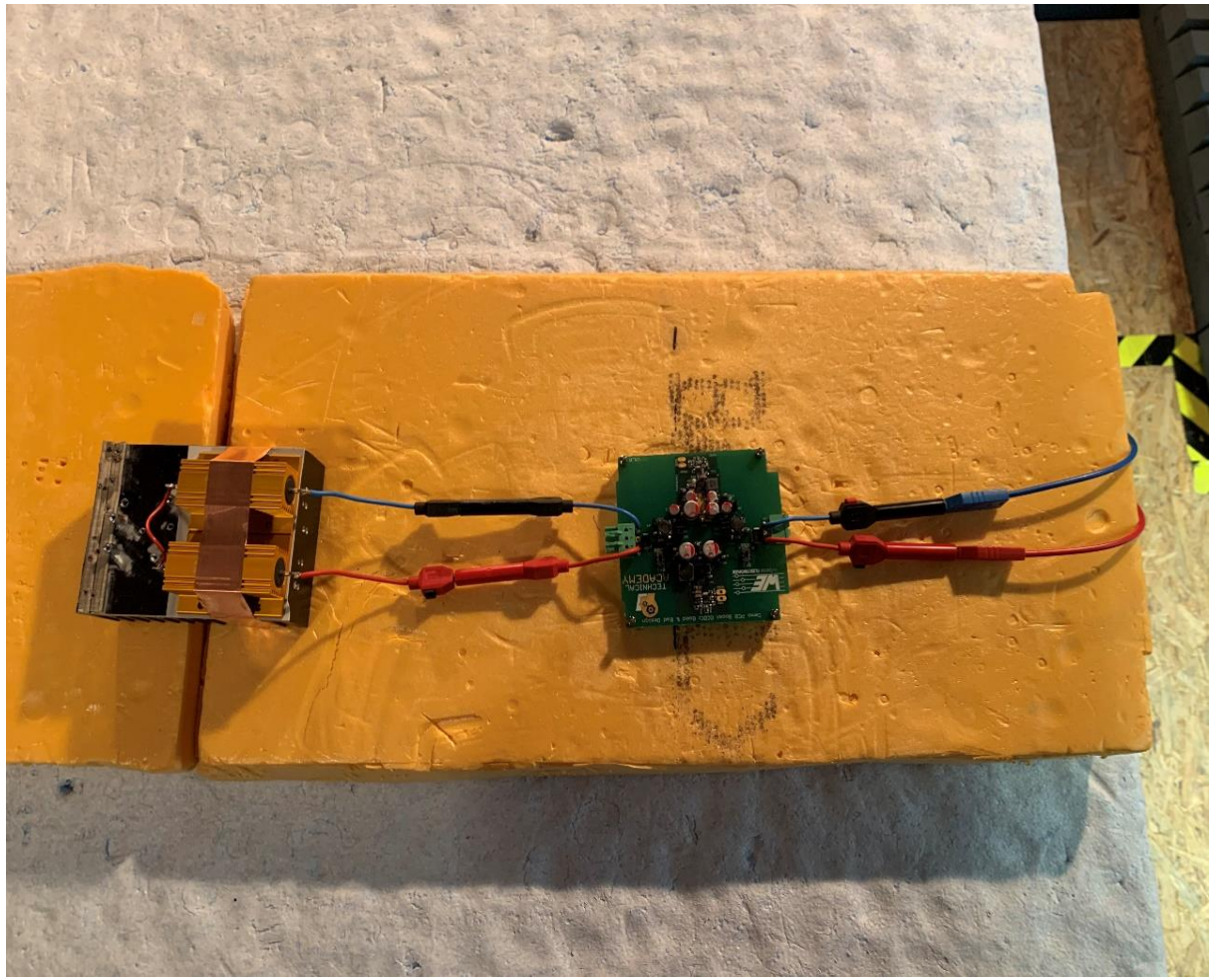


MEASURES AGAINST RADIATED NOISE

EMC Test Lab

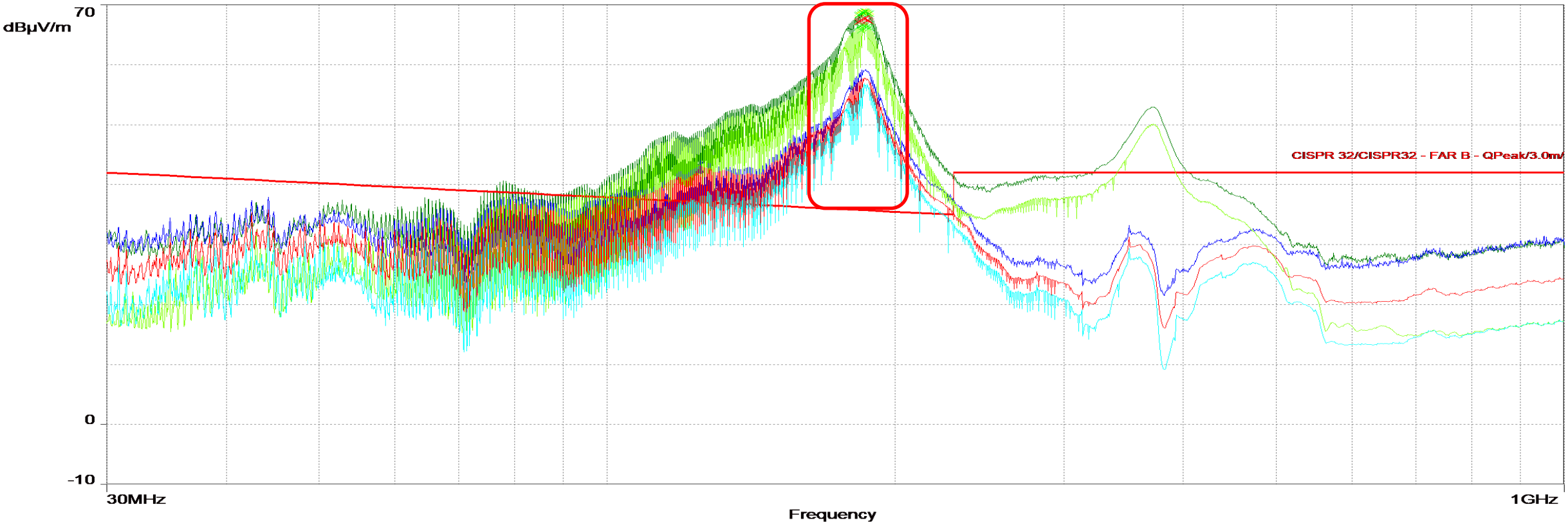
CISPR32 Radiated Emission





EMC Test Lab - Bad Design

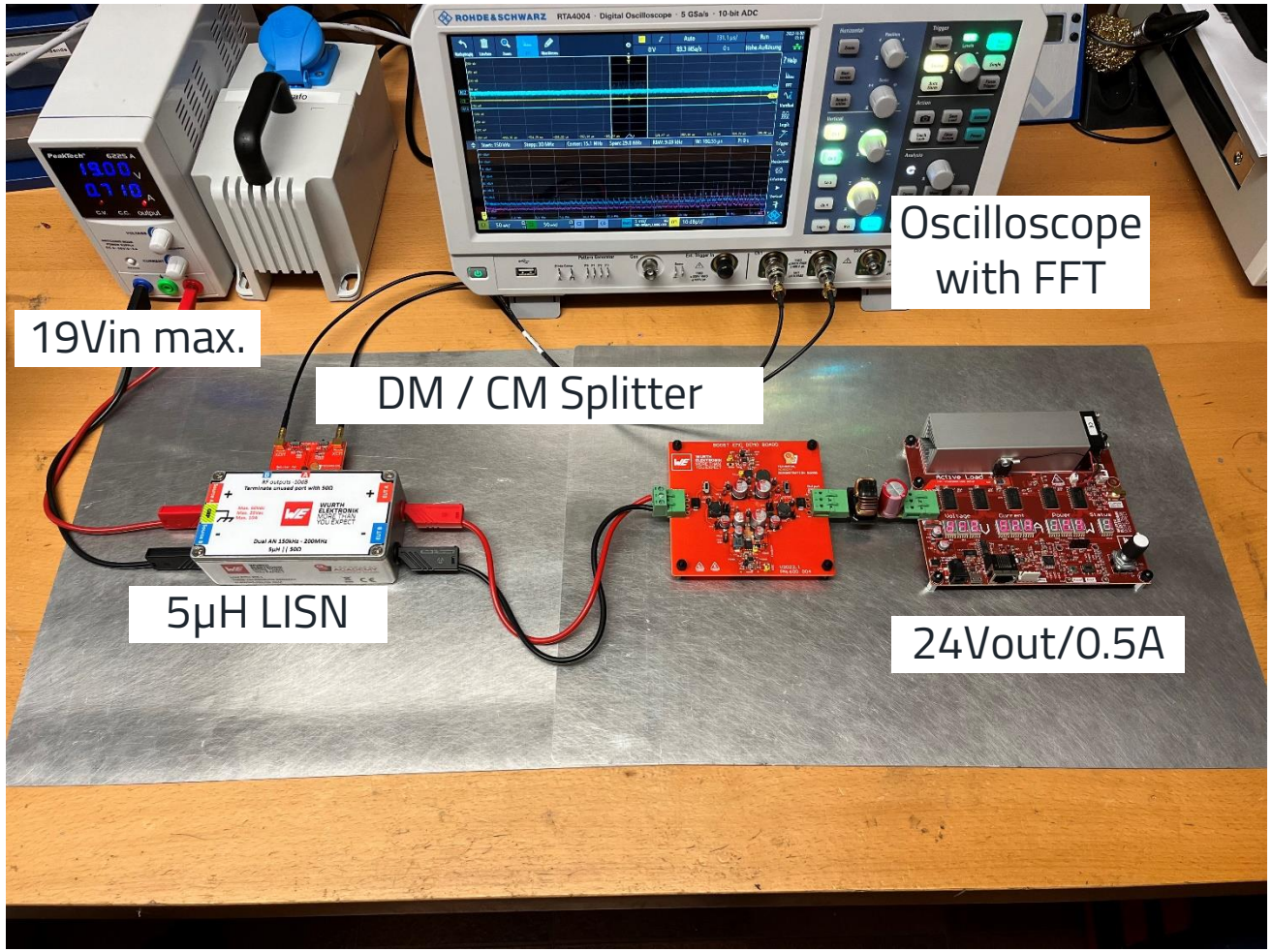
CISPR32 Radiated Emission



Bad Design

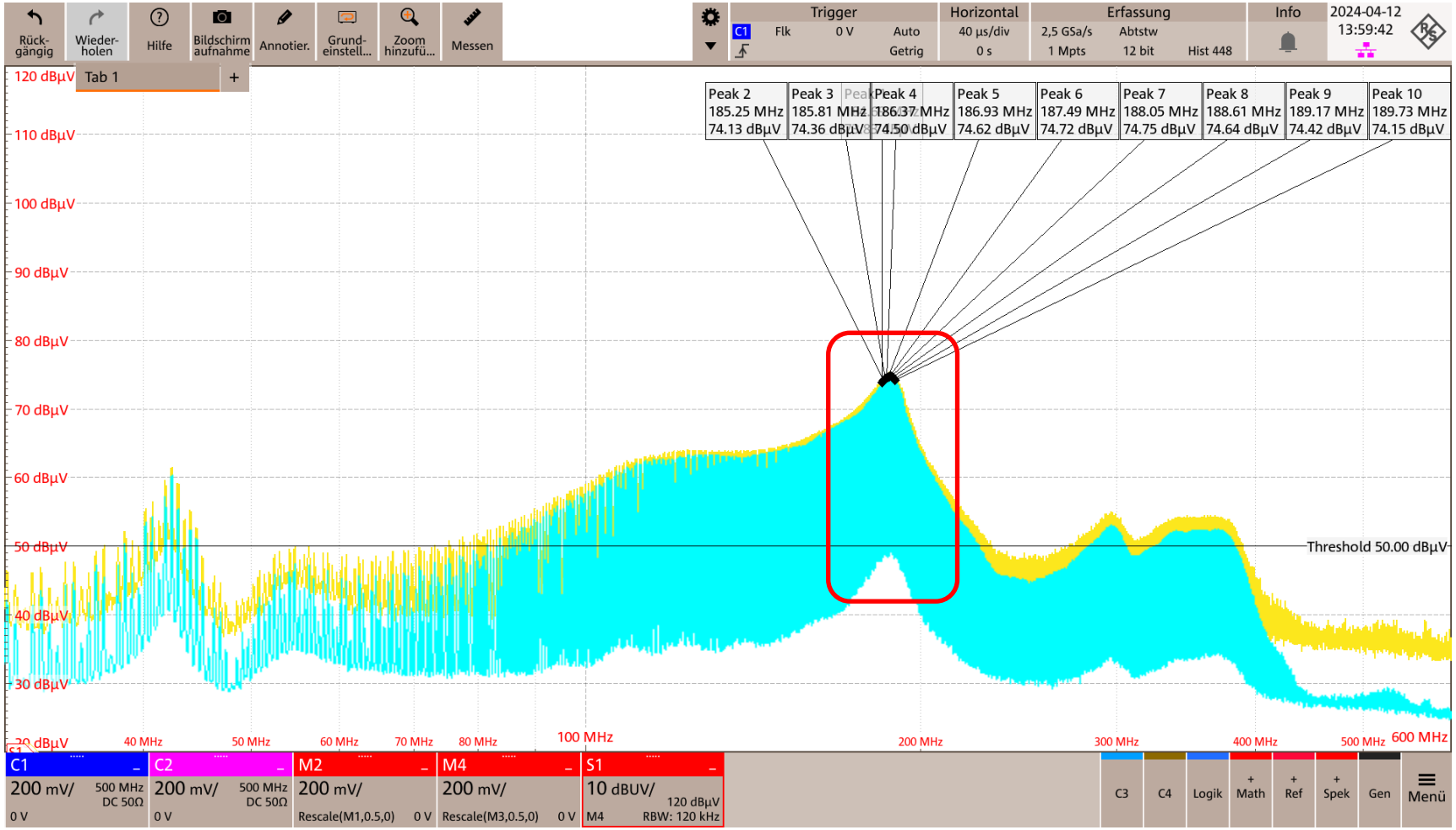
EMC Measurement Conducted up to 600MHz

Setup

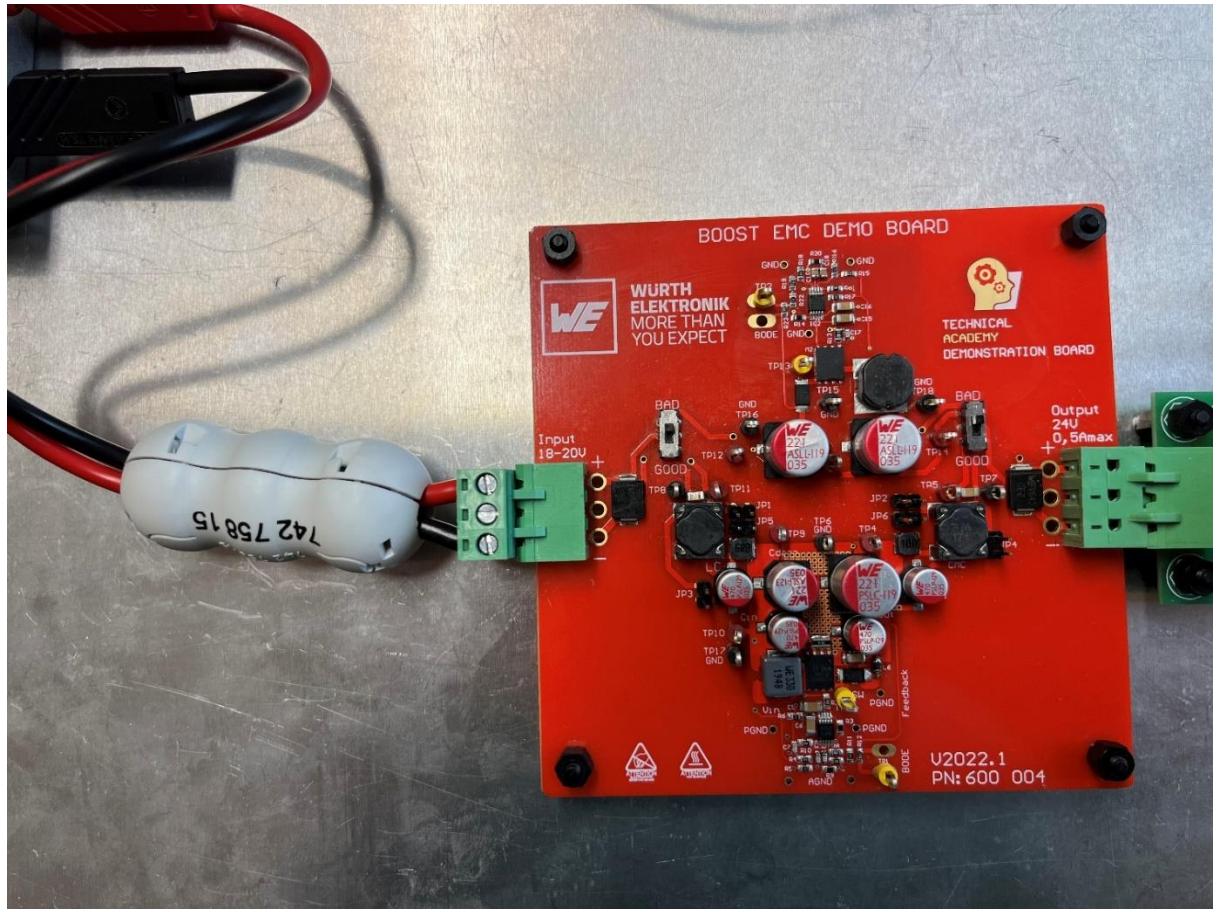


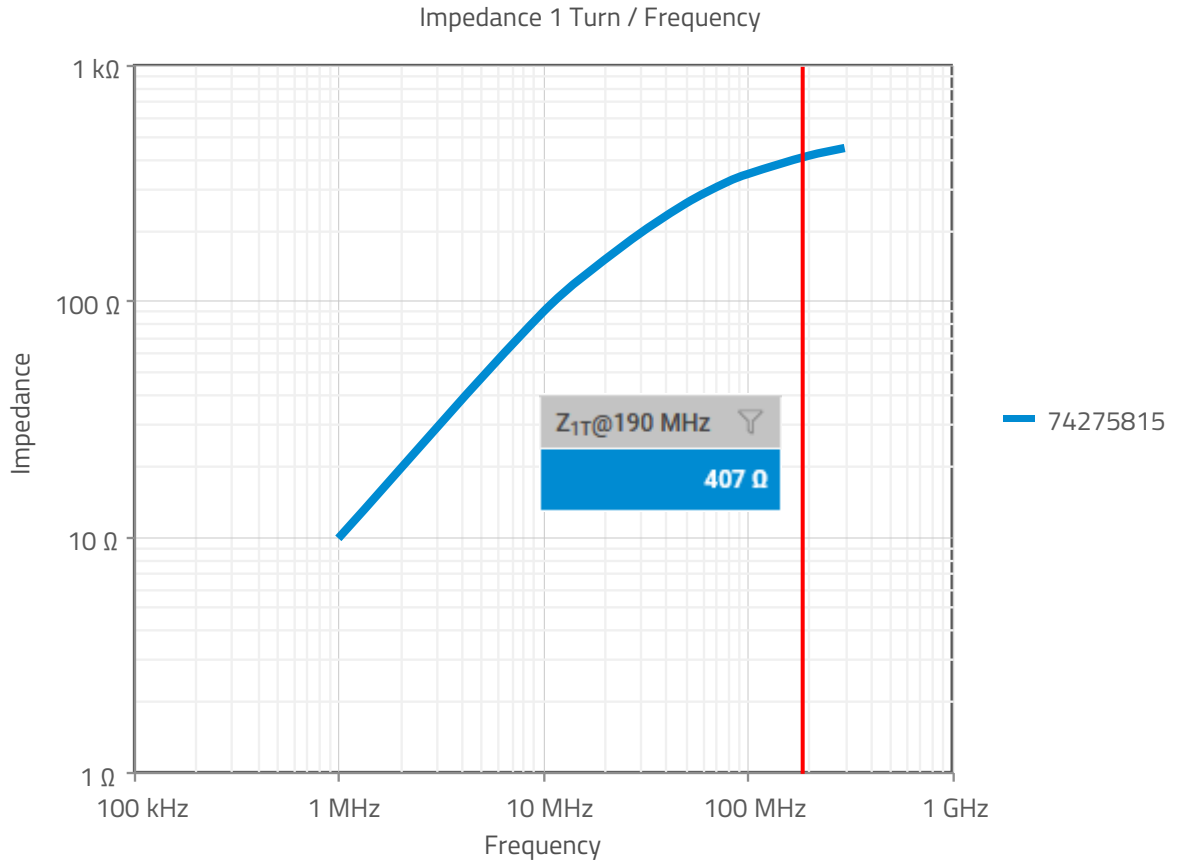
EMC Measurement Conducted up to 600MHz - Bad Design

FAE Equipment Bad Design CM



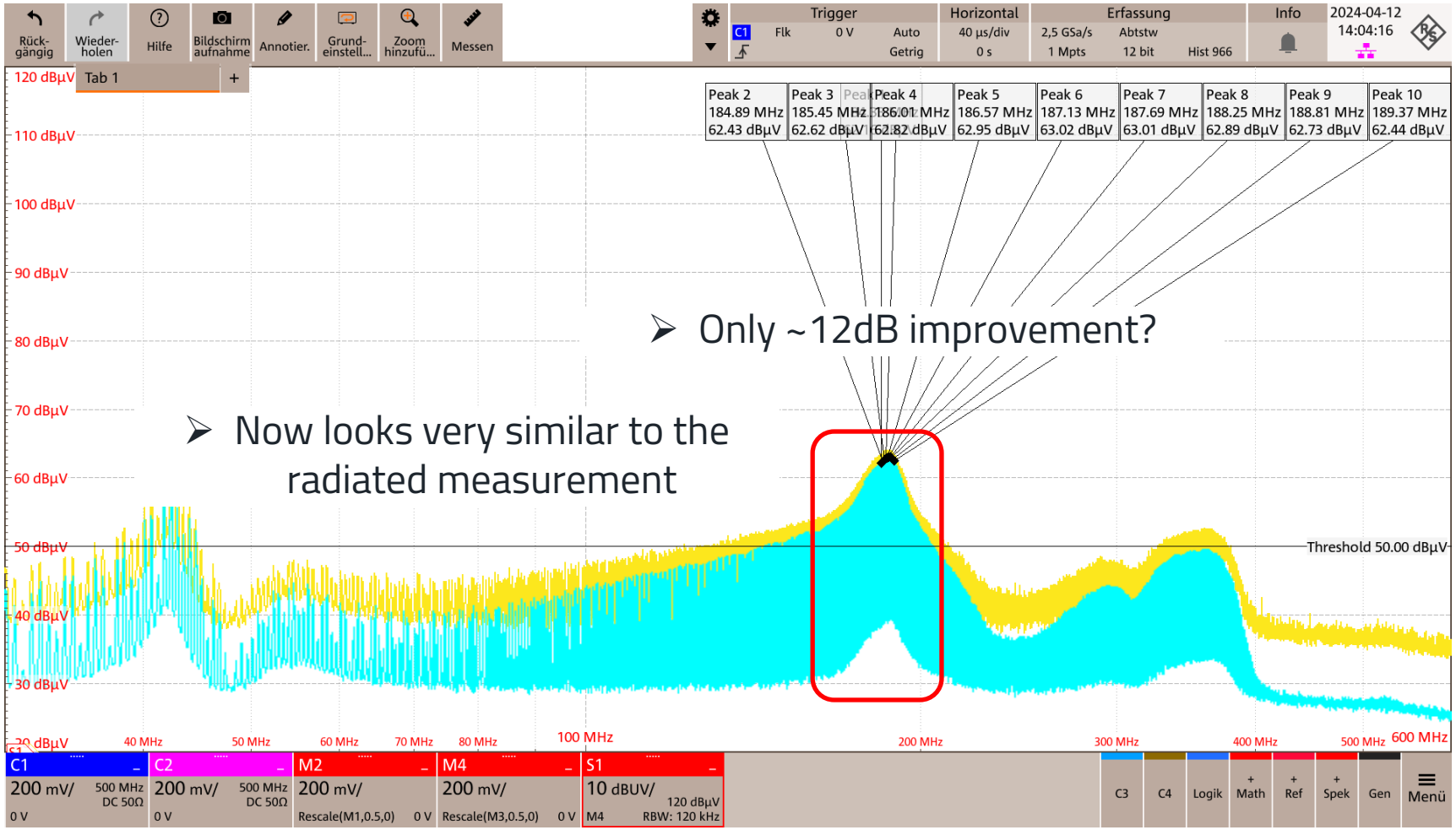
Setup with cable ferrite (74275815)





EMC Measurement Conducted up to 600MHz with cable ferrite (74275815)

FAE Equipment - Bad Design CM



Dimensioning of a cable ferrite

Impedance vs. Attenuation

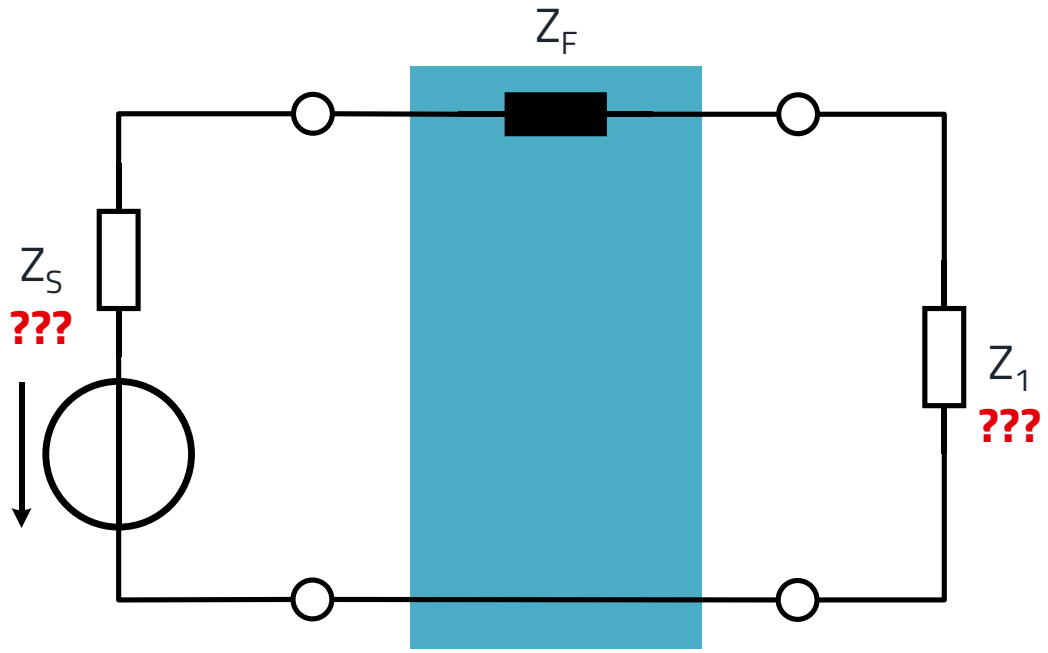
- A cable ferrite in series connection forms a **first-order low-pass Filter**
- **Insertion loss** in decibel:

$$A_{\mathrm{dm}} = 20 \cdot \log \left| 1 + \frac{Z_{\mathrm{F}}}{Z_{\mathrm{s}} + Z_{\mathrm{l}}} \right| \mathrm{dB}$$

- Minimum **filter impedance** at a noise frequency

$$Z_{\mathrm{filter}} = |Z_{\mathrm{s}} + Z_{\mathrm{l}}|_{f_{\mathrm{n}}} \cdot (10^{\frac{A_{\mathrm{cm}}(f_{\mathrm{n}})}{20}} - 1)$$

- For an exact calculation the source and load impedance for each noise frequency would have to be known.



Dimensioning of a cable ferrite

System impedance

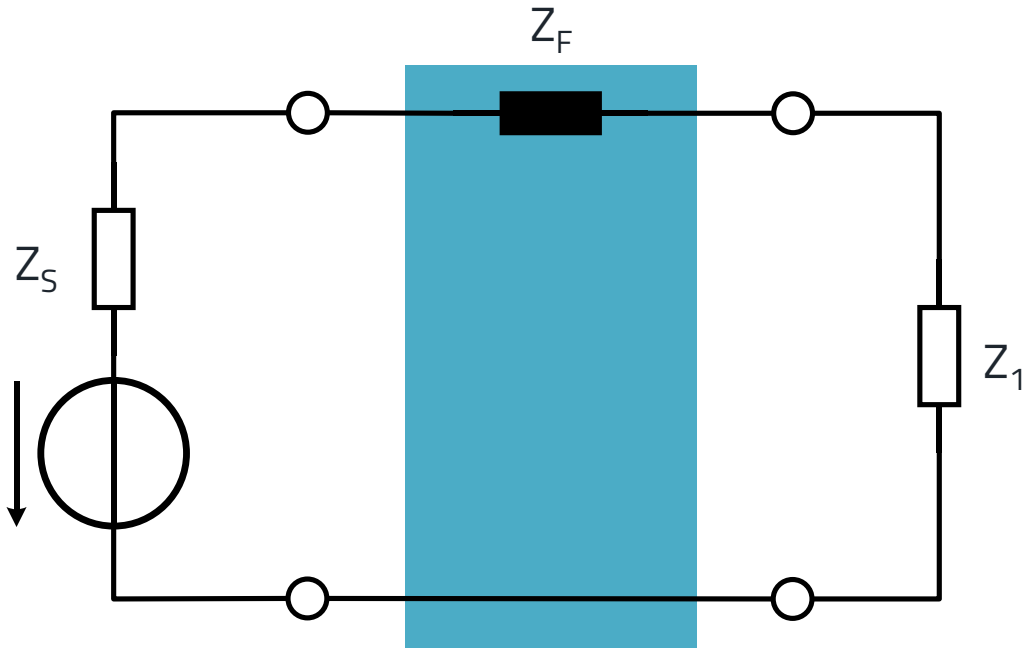
- **System impedance** at a noise frequency
  - $|Z_s + Z_l|_{f_n} = \frac{Z_{\text{filter}}}{\left(10^{\frac{A_{cm}(f_n)}{20dB}} - 1\right)}$

➢ For 12dB attenuation with a 409Ω cable ferrite @ 190Mhz

  - $|Z_s + Z_l|_{f_n} = \frac{409\Omega}{\left(10^{\frac{12dB}{20dB}} - 1\right)} \approx 137\Omega$

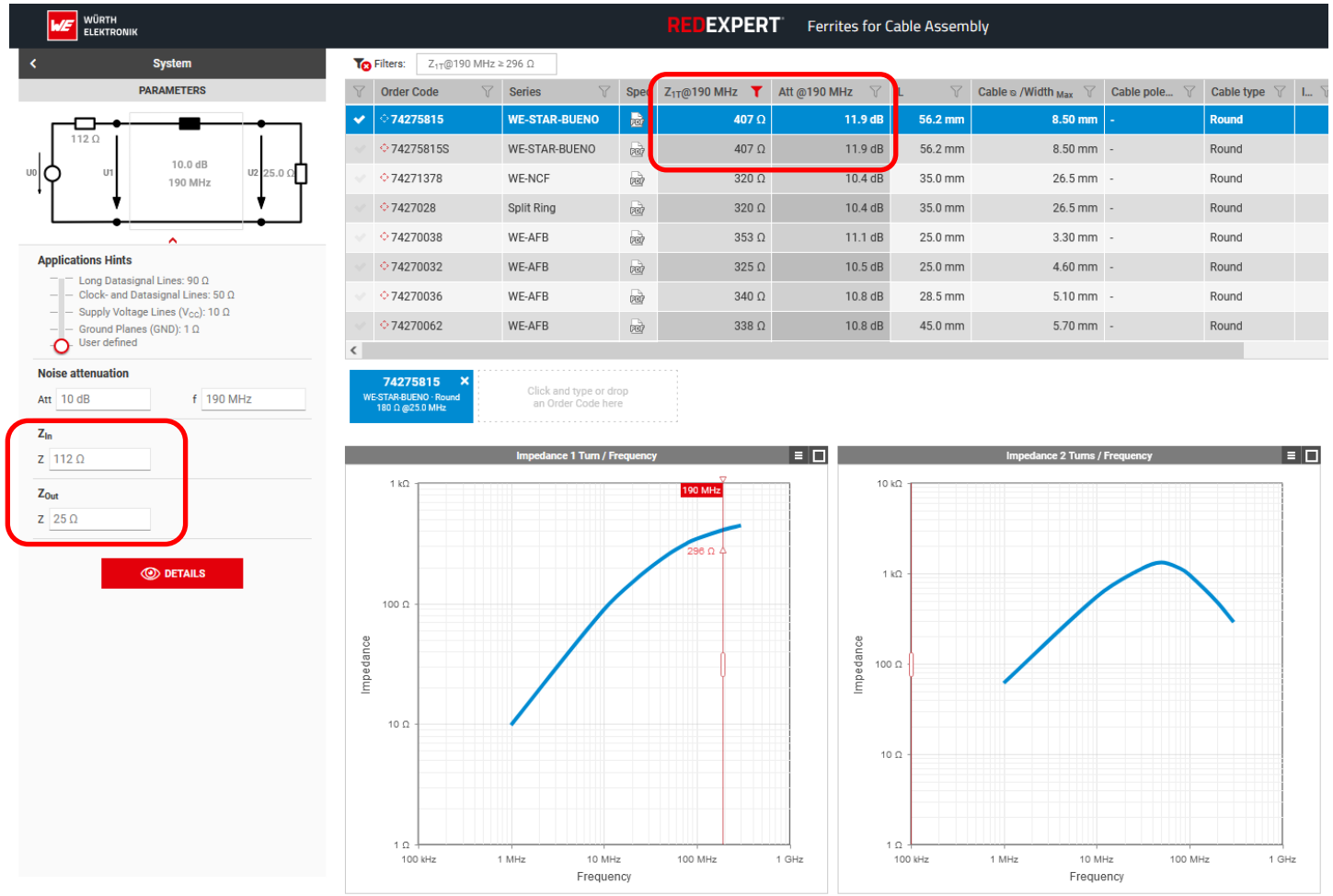
  ➢ Z_1 is known / Z_1 = 25Ω = CM-Impedance of the LISN
    ➢ Z_S = 112Ω
  ➢ High impedance system
  ➢ Inductive coupling may be the source of the noise

    ➢ Let's try an h-field probe to find the source



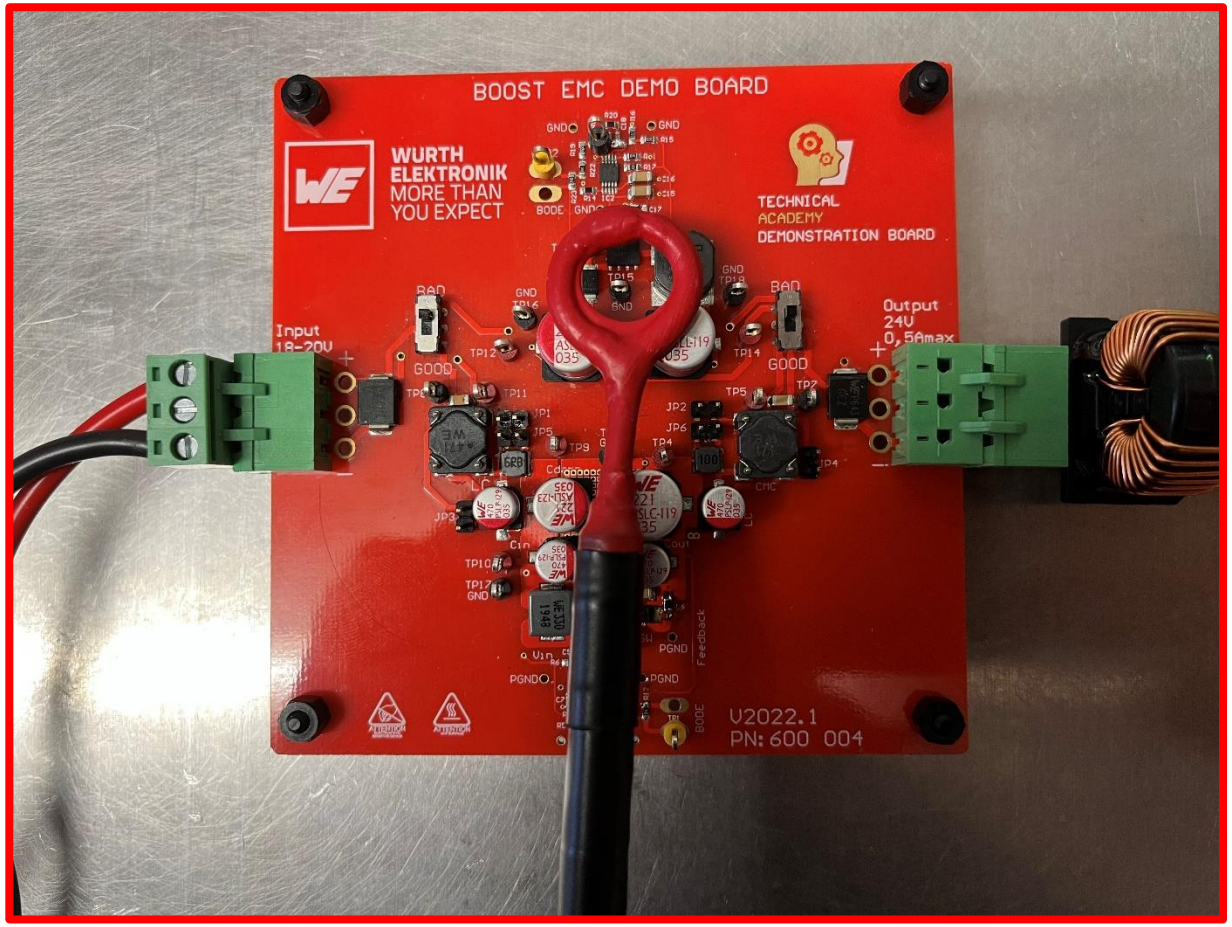
Dimensioning of a cable ferrite with REDEXPERT

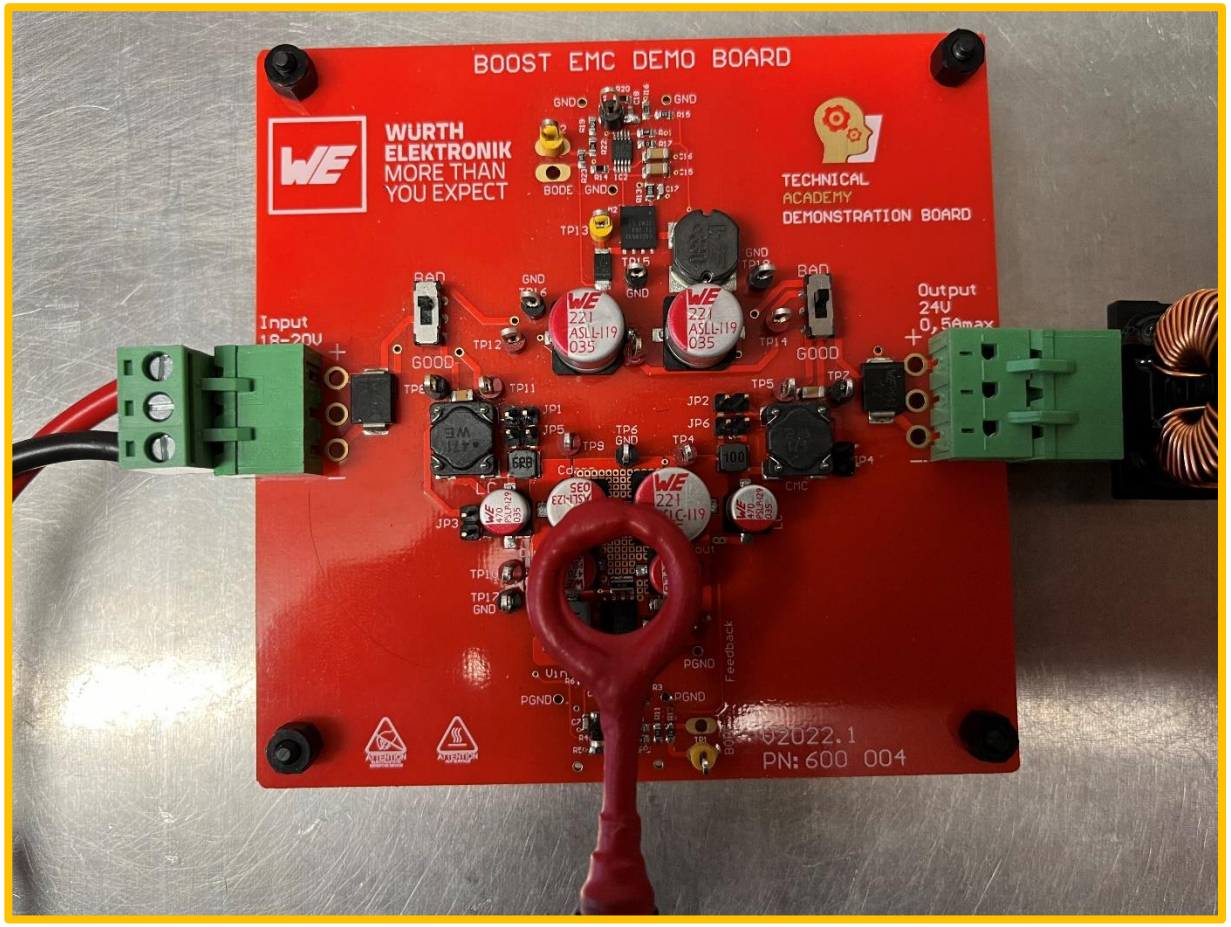
https://we-online.com/re/5sHwSLa5He



Near Field 1GHz (H-Field Probe - Big Loop)

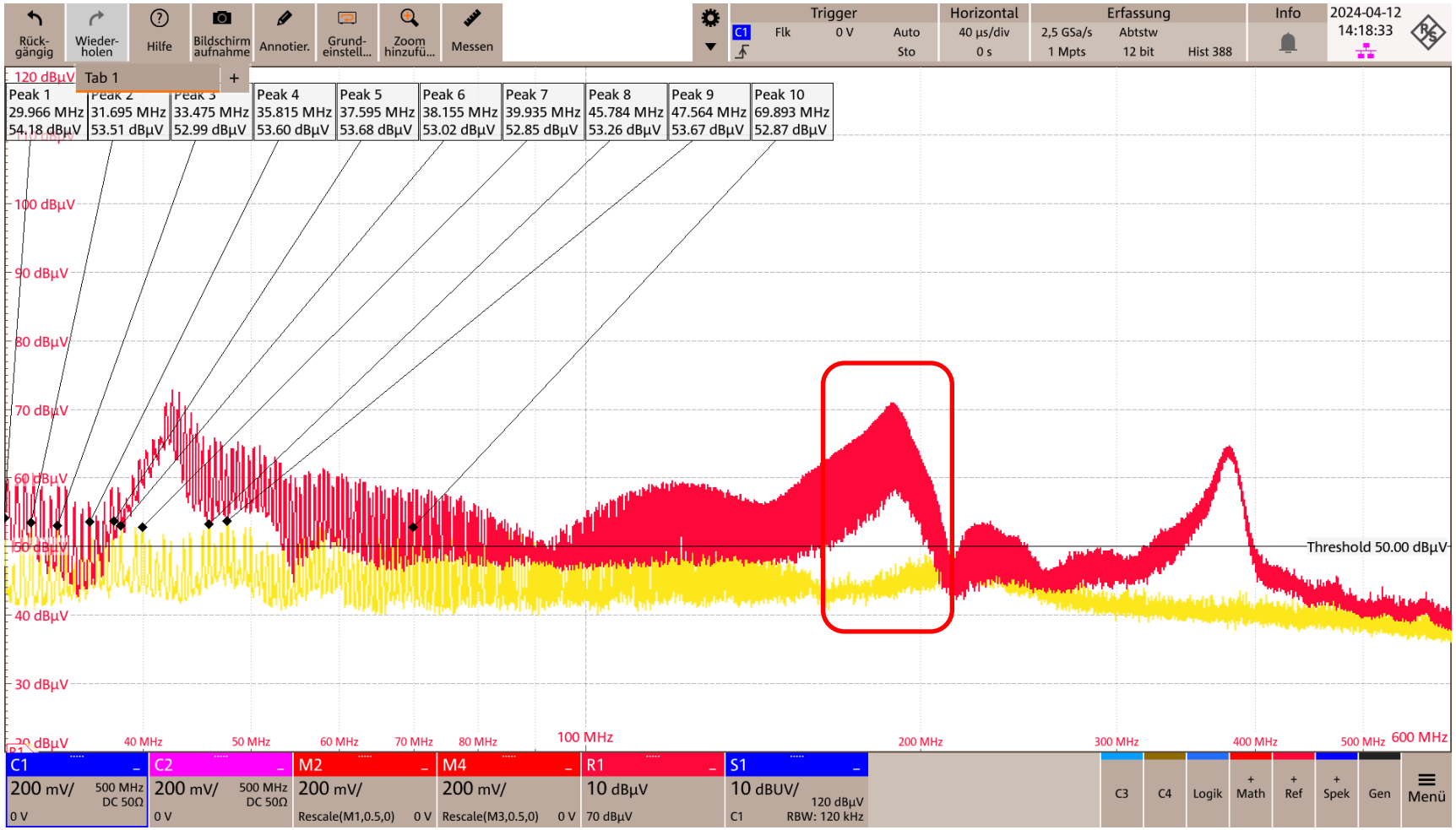
Bad vs. Good





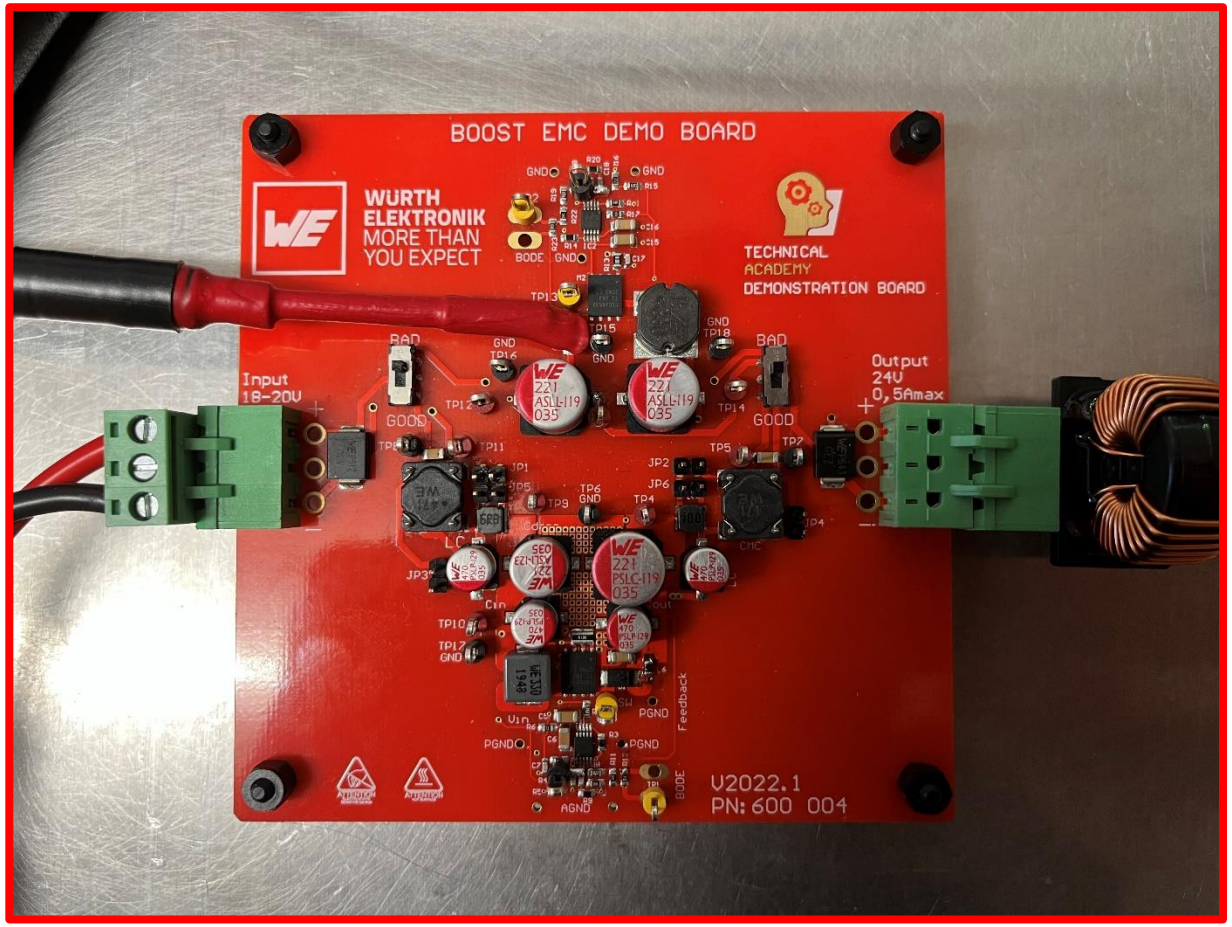
Near Field 1GHz (H-Field Probe - Big Loop)

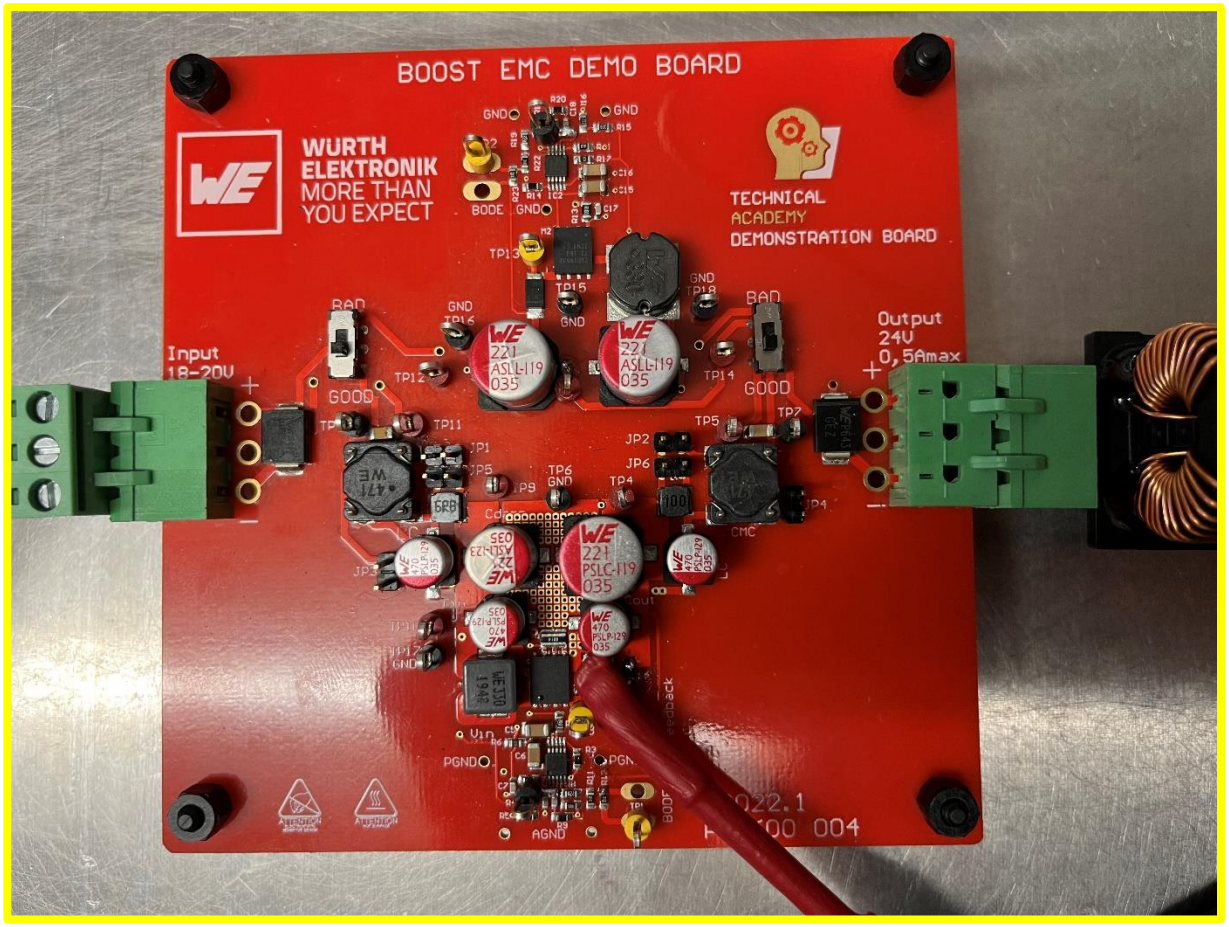
Bad vs. Good



Near Field 1GHz (H-Field Probe - Small Loop - Schottky Diode)

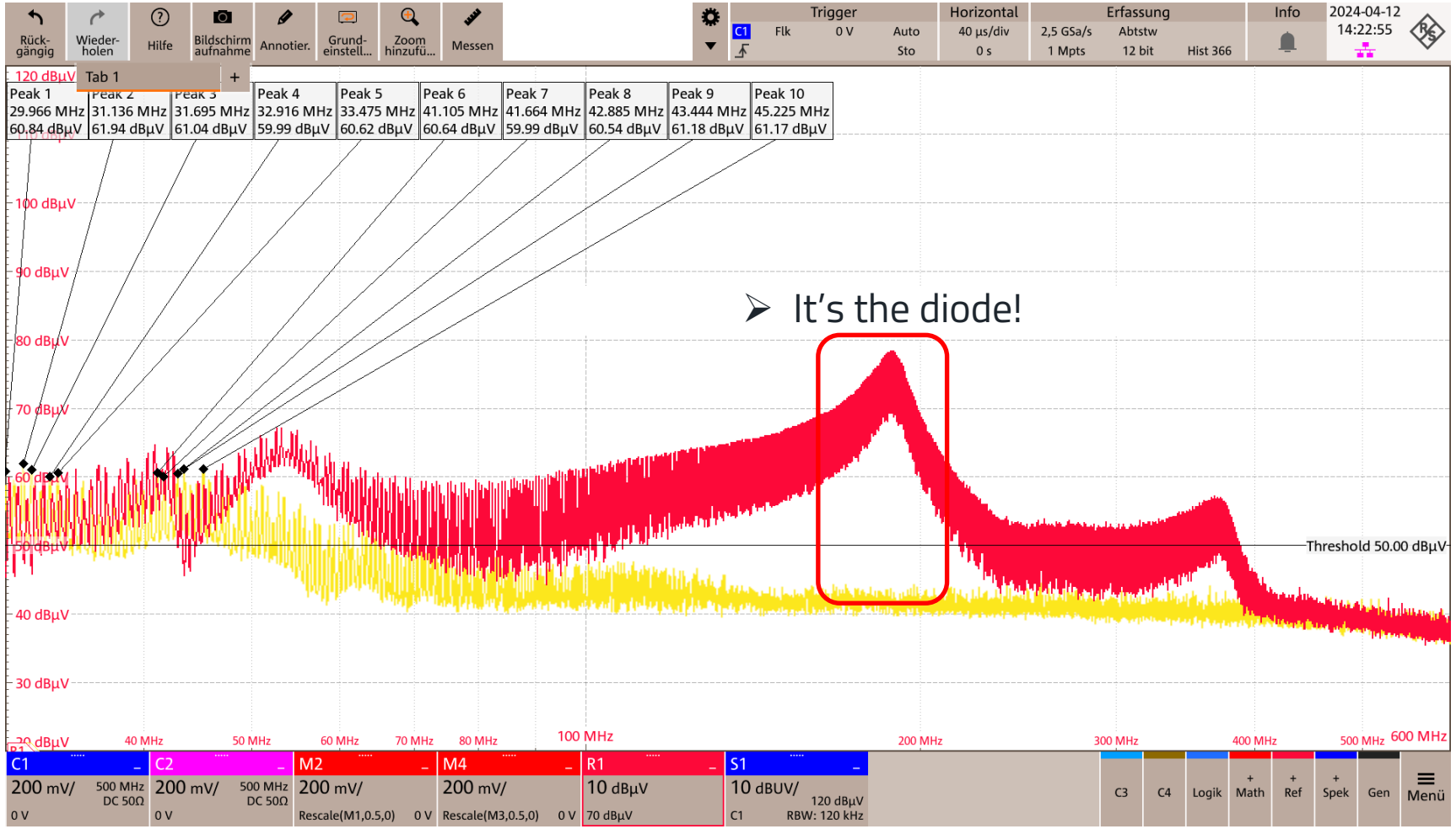
Bad vs. Good





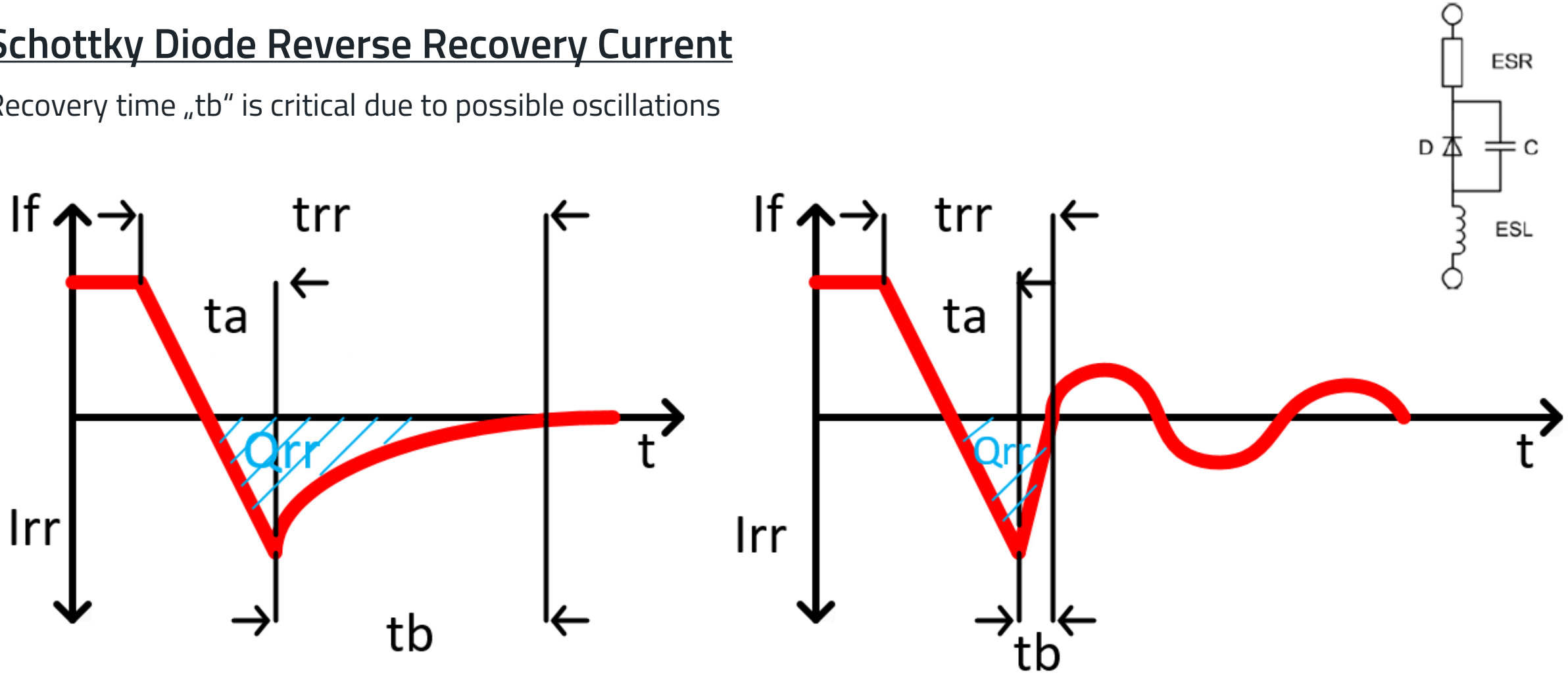
Near Field 1GHz (H-Field Probe - Small Loop - Schottky Diode)

Bad vs. Good



Schottky Diode Reverse Recovery Current

Recovery time „tb“ is critical due to possible oscillations



The softer the recovery, the lower the RF EMI noise but the higher the losses „Qrr“ in the diode

Schottky Diode Reverse Recovery Current

- $Recovery\ Softness\ Faktor$:

  $RSF = {t_b}/{t_a}$

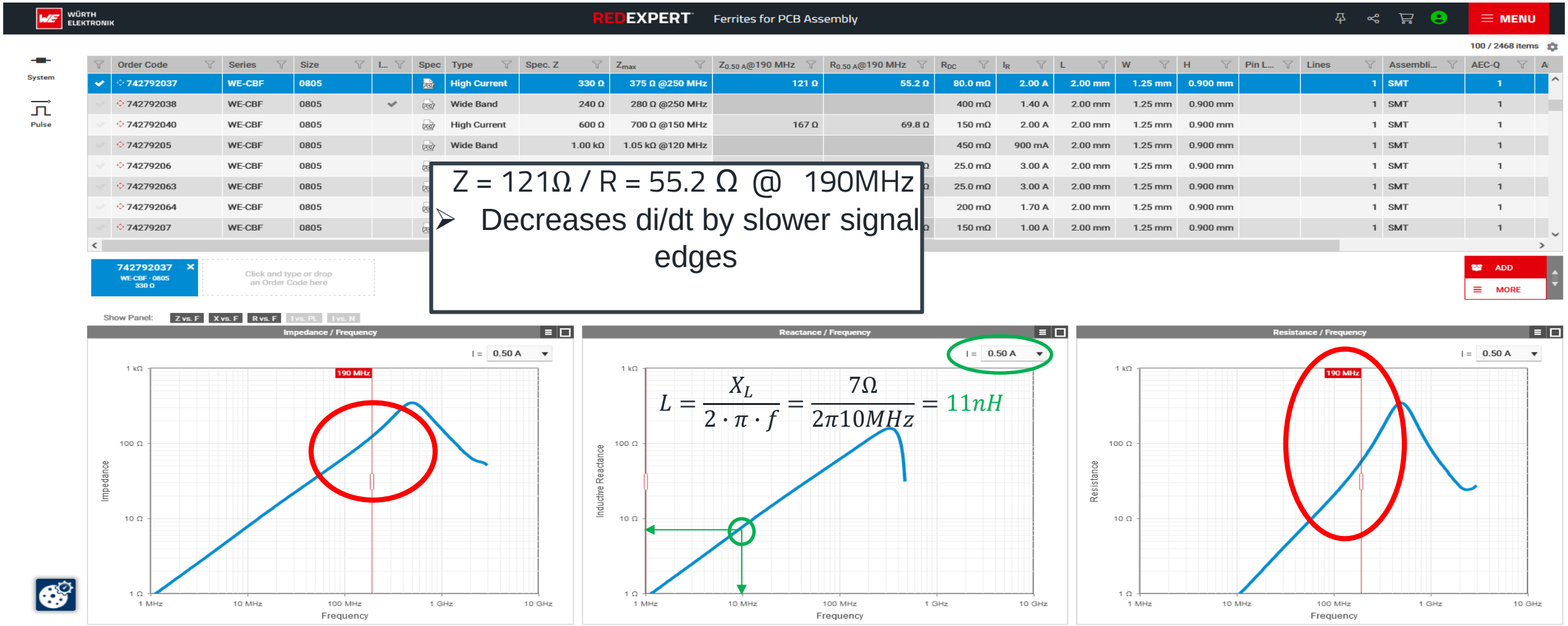
  the larger the value, the "softer"

  - I_{RR} and t_{rr} are strongly temperature-dependent values! (does not apply to SiC/GaN)

    ➢ You could use a soft recovery diode or solve the problem by extending t_b with a ferrite

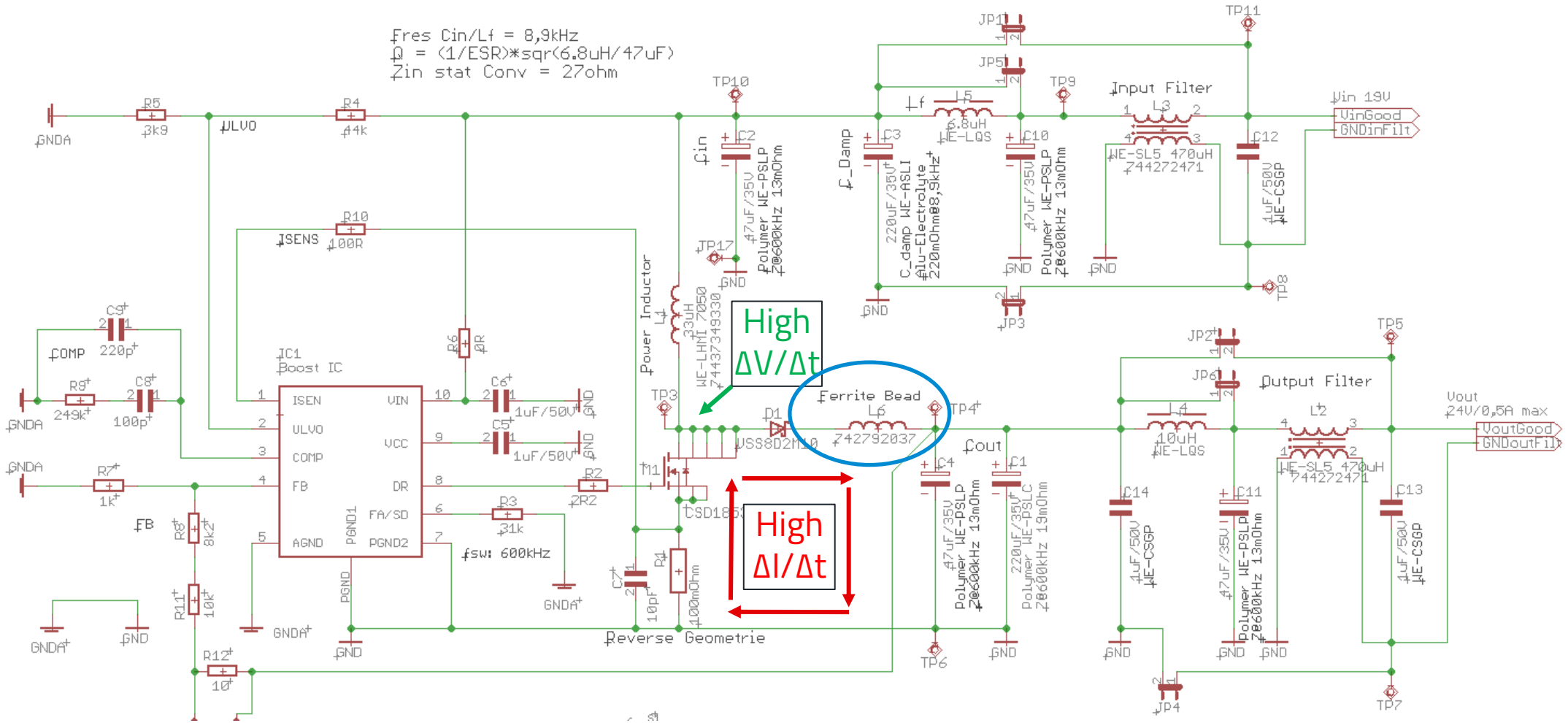
Redexpert (https://we-online.com/re/5oUl3TFk)

Chip Bead Selection @ 0,5A Iout and 190MHz → Reactance XL under 10MHz as low as possible!



Schematic Good Design

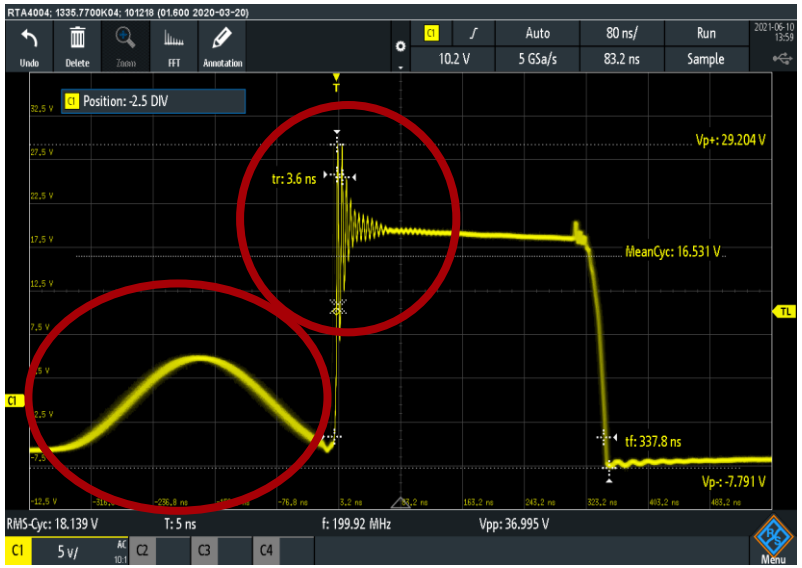
19V → 24V/0,5A

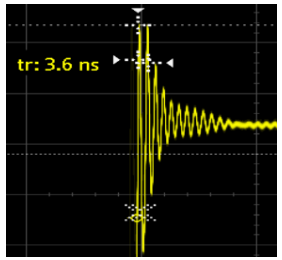


Time Domain Measurements

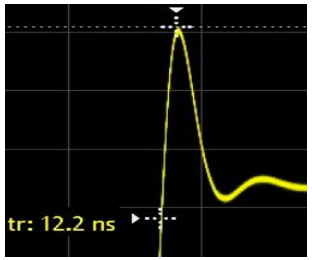
Voltage over Schottky Diode

Bad Design

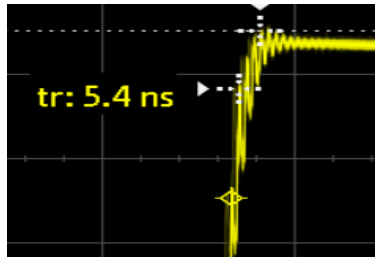




Good Design with Ferrite

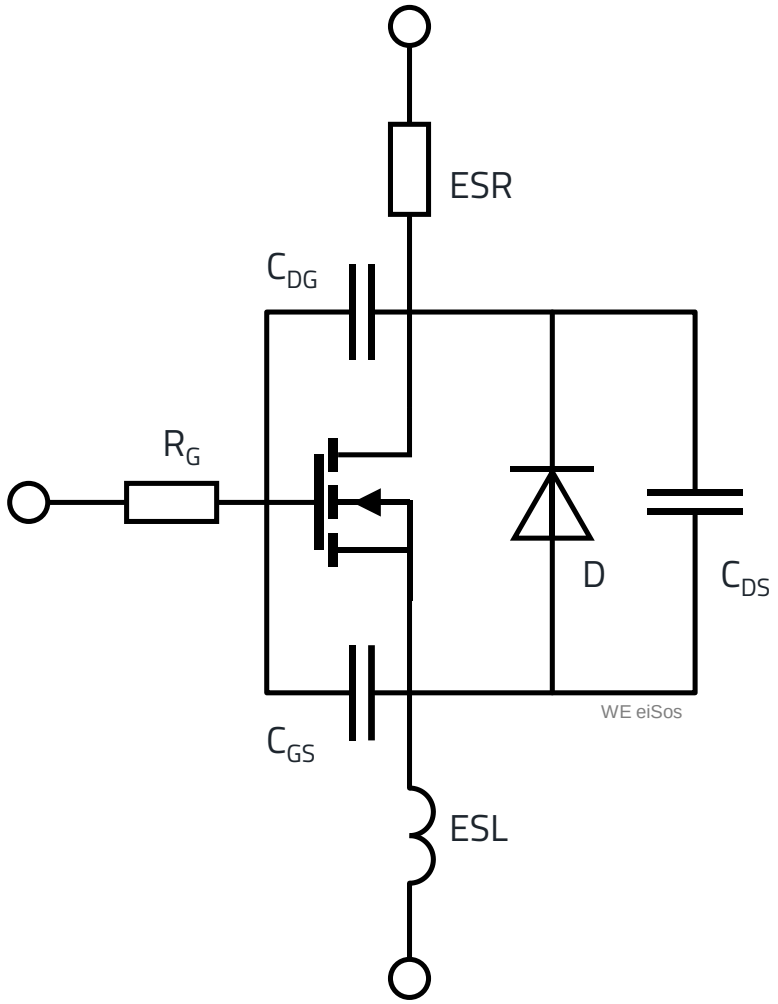


Good Design no Ferrite



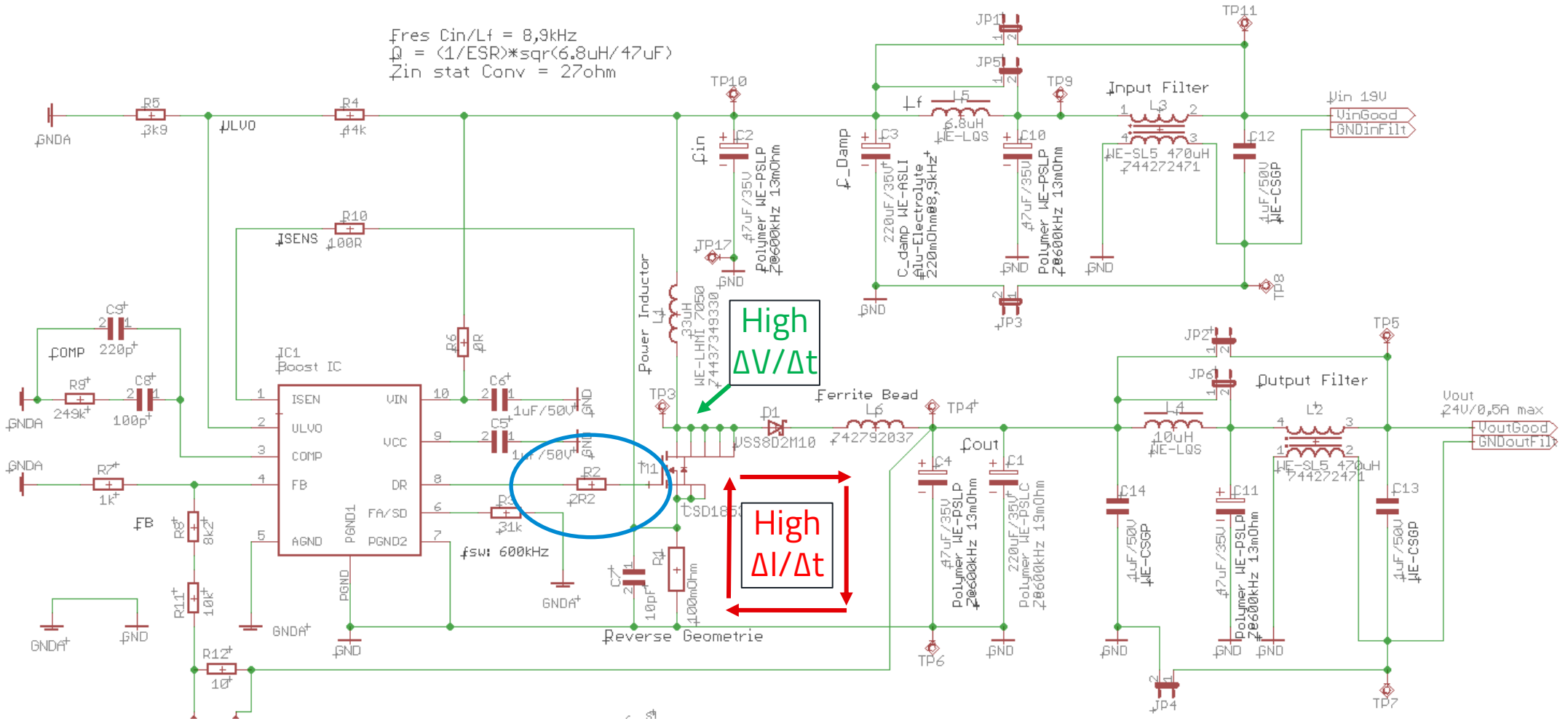
Noise from the FET

- Oscillations are caused by parasitic component effects (also in combination with the layout)
- Choose an MOSFET with a small drain/source capacitance
  - ➢ MOSFET fixed for this bad/good comparison
- Choose an MOSFET with moderate on/off slope
  - ➢ MOSFET fixed for this bad/good comparison
  - ➢ However, the slope can also be slowed down by gate resistance



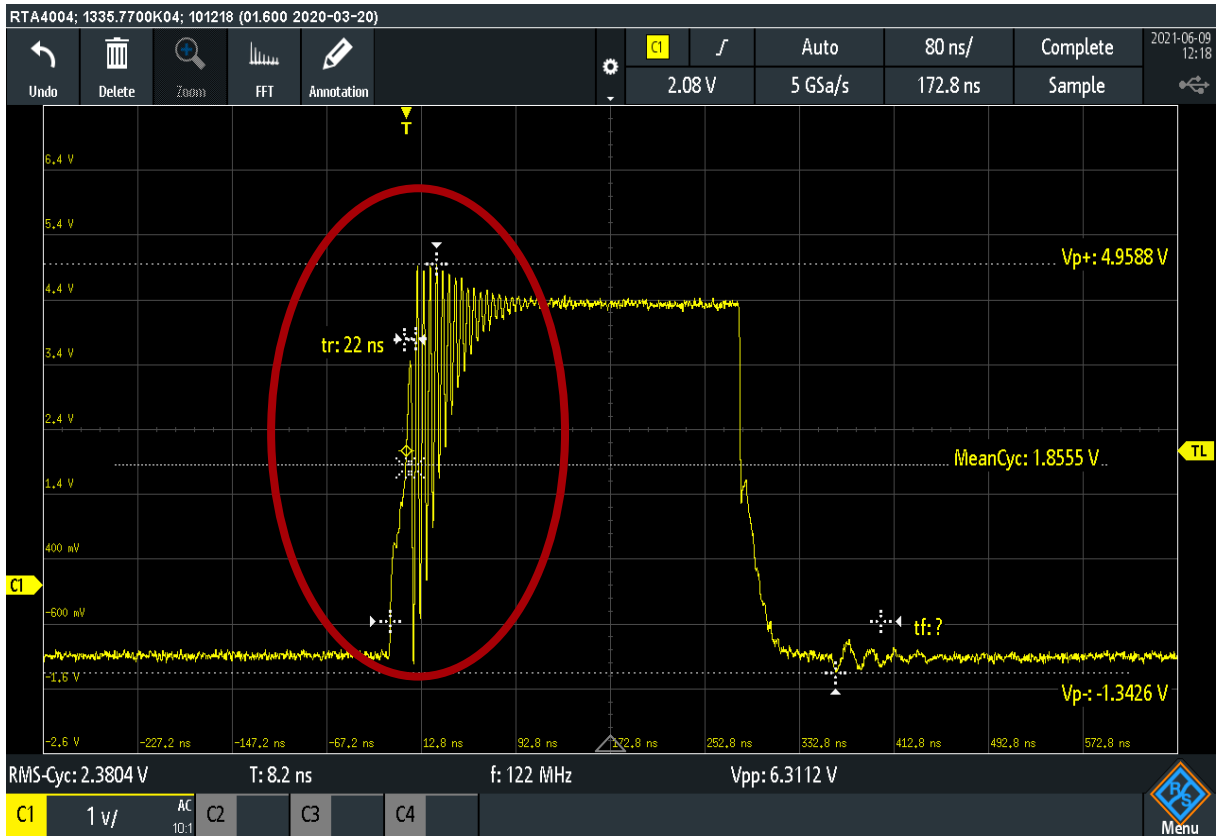
Schematic Good Design

19V → 24V/0,5A

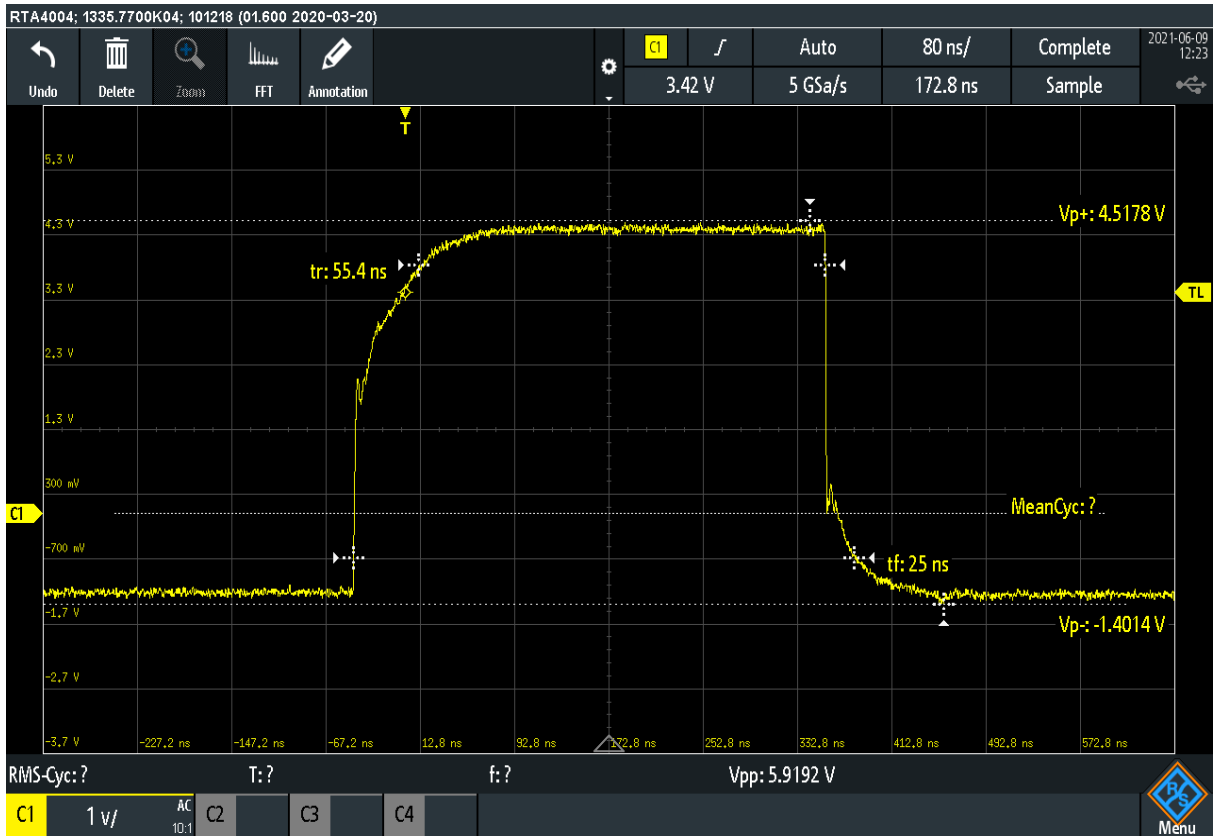


Time Domain Measurements

FET Gate Source Voltage



Bad Design Vgs MOSFET

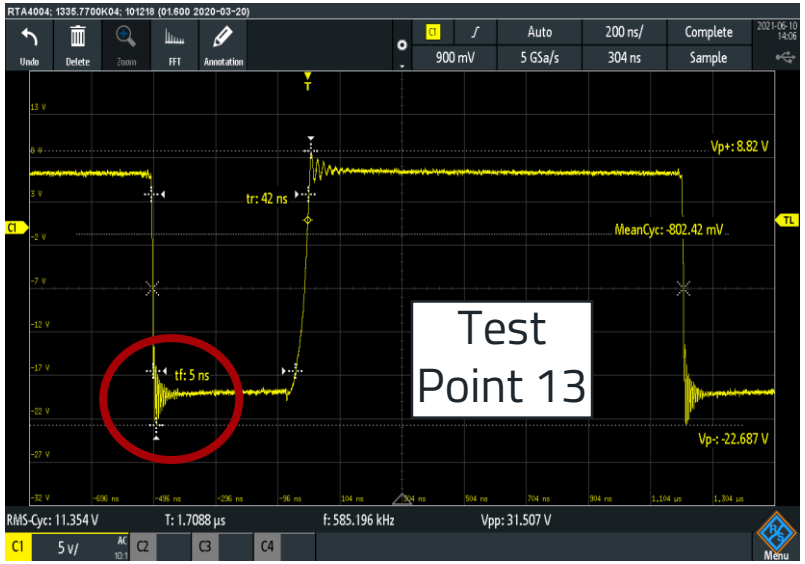


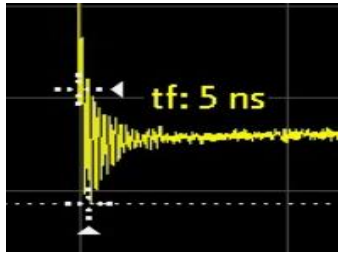
Good Design Vgs MOSFET

Time Domain Measurements

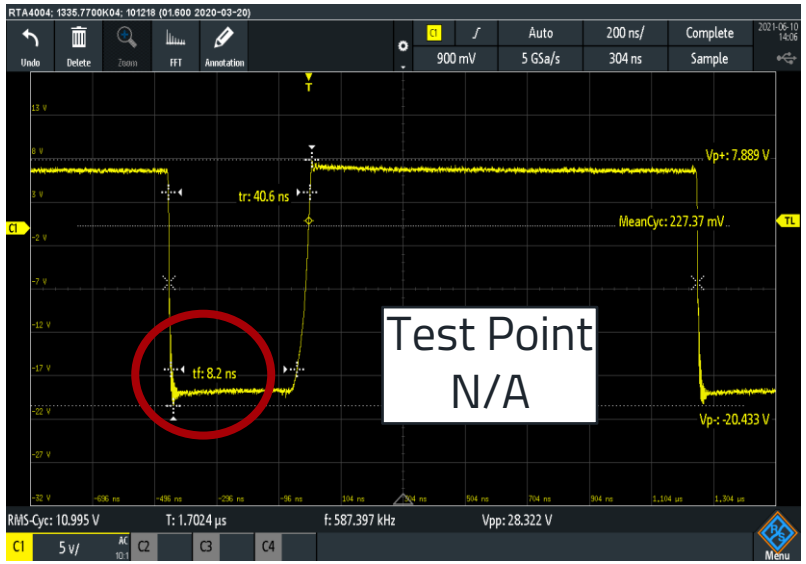
Switch Node Voltage

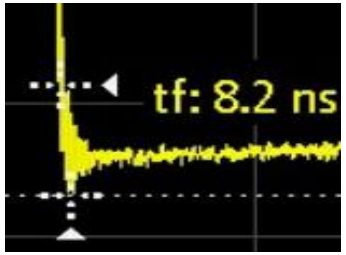
Bad Design



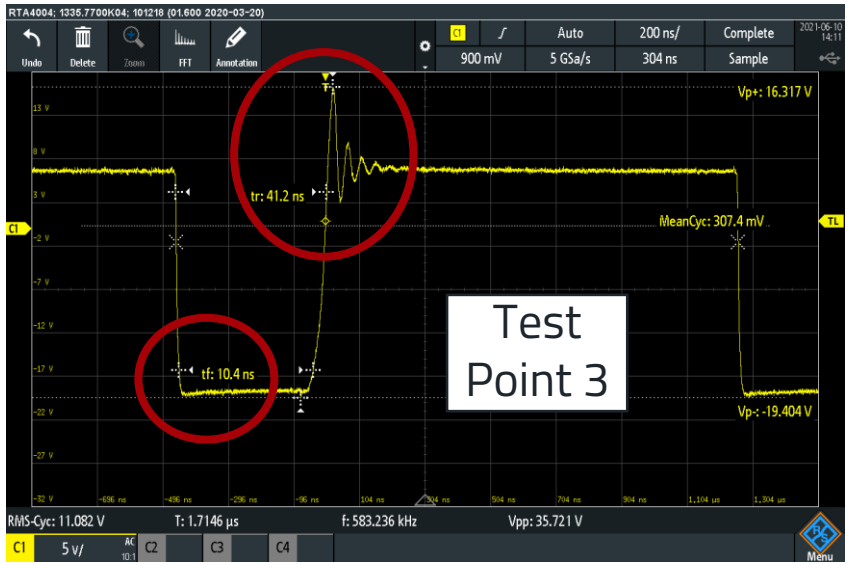


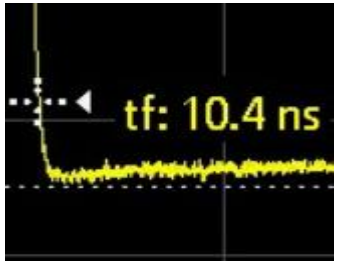
Good Design no Ferrite

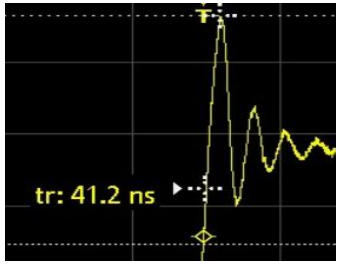




Good Design with Ferrite

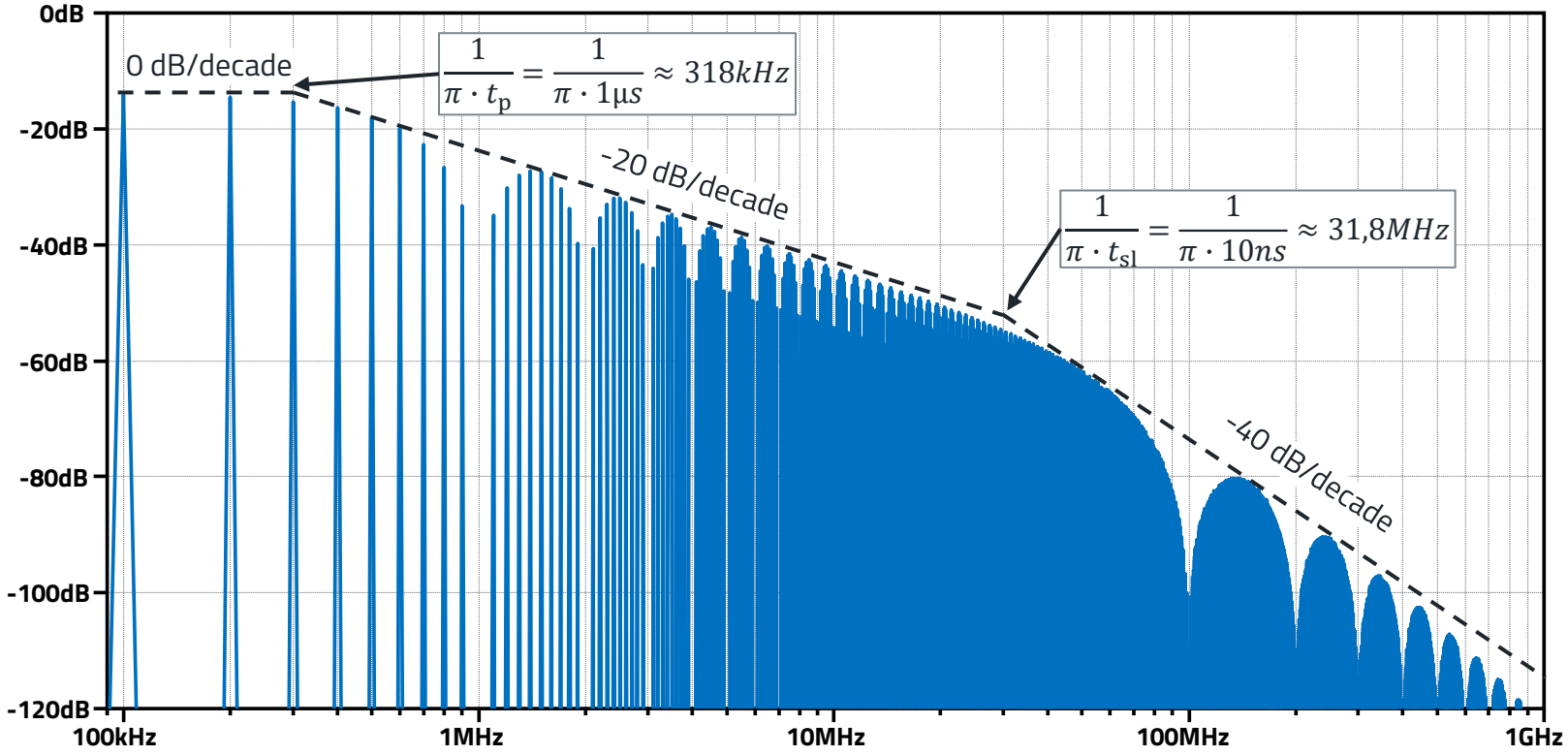






Noise from the Diode/FET

Spectrum of a trapezoidal voltage/current waveform



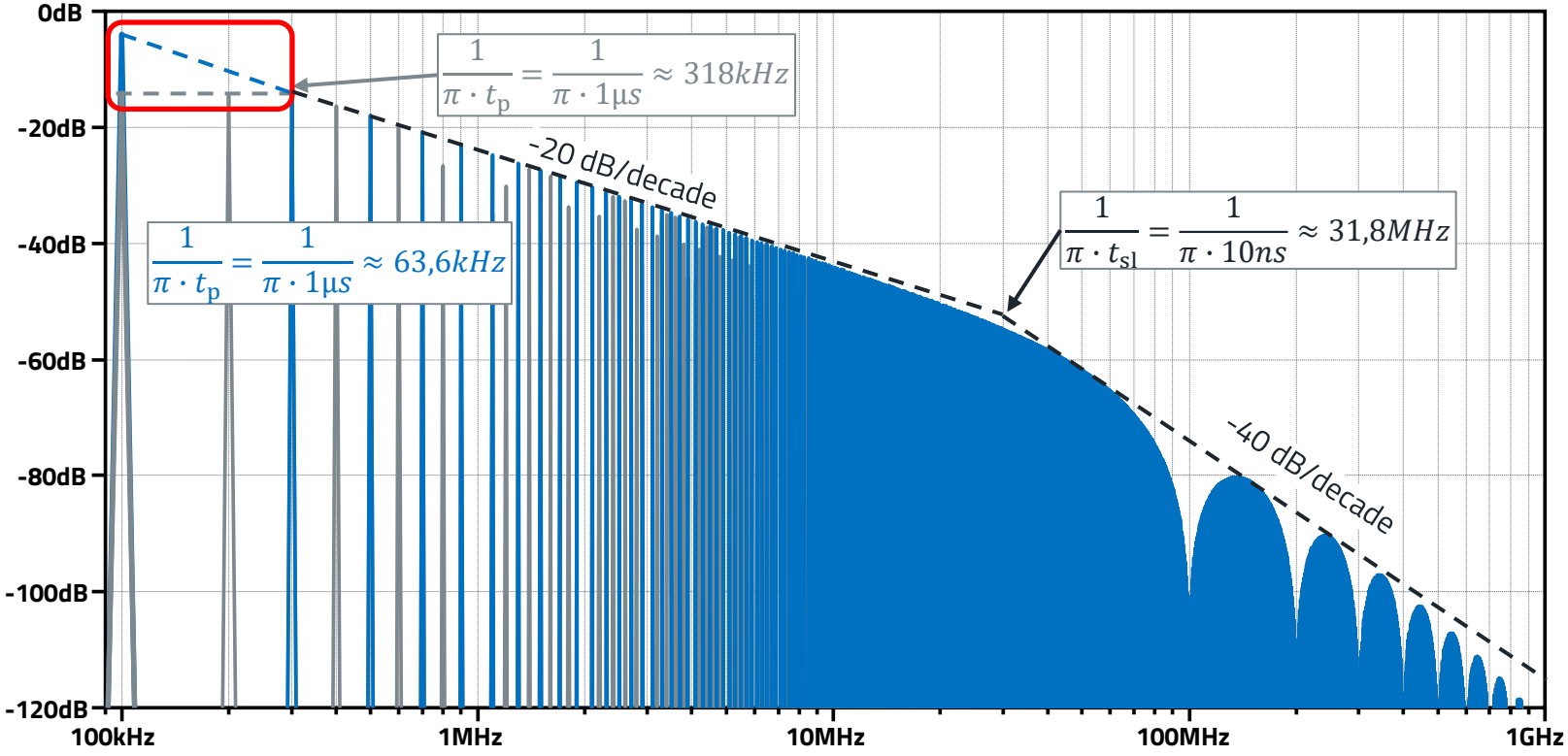
$\widehat{U} = \sqrt{2}$ / f = 100kHz / t_r = t_f = t_{sl} = 10ns / D = 10% or. D = 90%

Link to LTspice simulation

- t_p: pulse width
  - $t_p = D \cdot T$ or
  - $t_p = (1 - D) \cdot T$
  - ➢ whichever is smaller
  - ➢ whereby:
    - D: duty-cycle
    - $T = \frac{1}{f}$: period-time
    - f : frequency
- t_{sl}: slope-time
  - $t_{sl} \approx t_r$ or
  - $t_{sl} \approx t_f$
  - ➢ t_{sl} dominated by t_r or t_f whichever is smaller
  - ➢ whereby:
    - t_r: rise-time
    - t_f: fall-time

Noise from the Diode/FET

Spectrum of a trapezoidal voltage/current waveform depending on duty-cycle



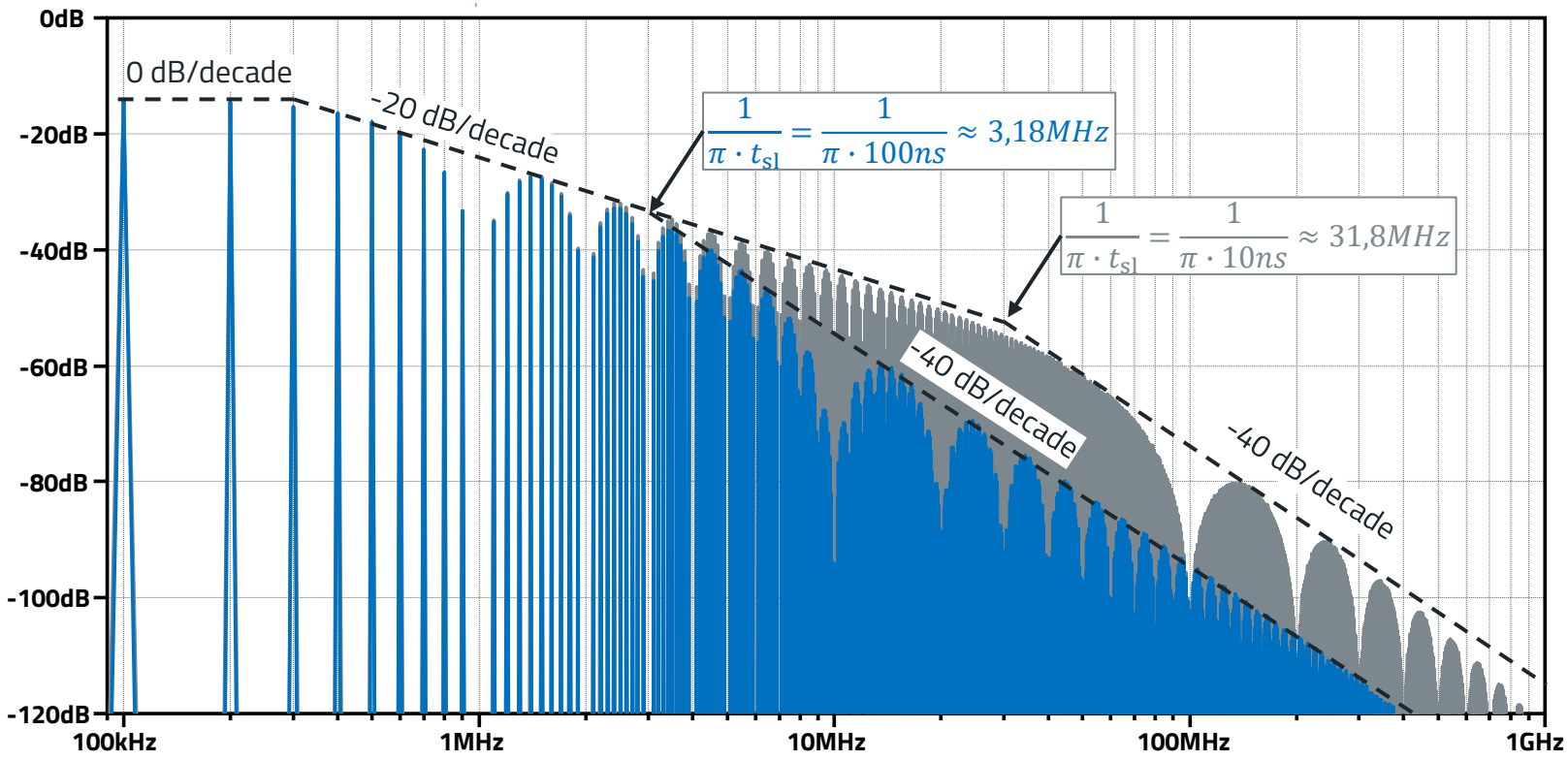
$\hat{U} = \sqrt{2}$ / f = 100kHz / t_{sl} =10ns / D = 10% or. 90% vs. 50%

Link to LTspice simulation

- A waveform with 50% duty cycle only has odd harmonics
- A clock signal with 50% duty cycle has a greater amplitude of the first harmonic than a 10% or even a 90% duty cycle signal
  - However a 90% clock signal has more power than a 10% or 50% clock signal, but this power adds to the DC component only (0 Hz)

Noise from the Diode/FET

Spectrum of a trapezoidal voltage/current waveform depending on slope-time (rise-/fall-time)



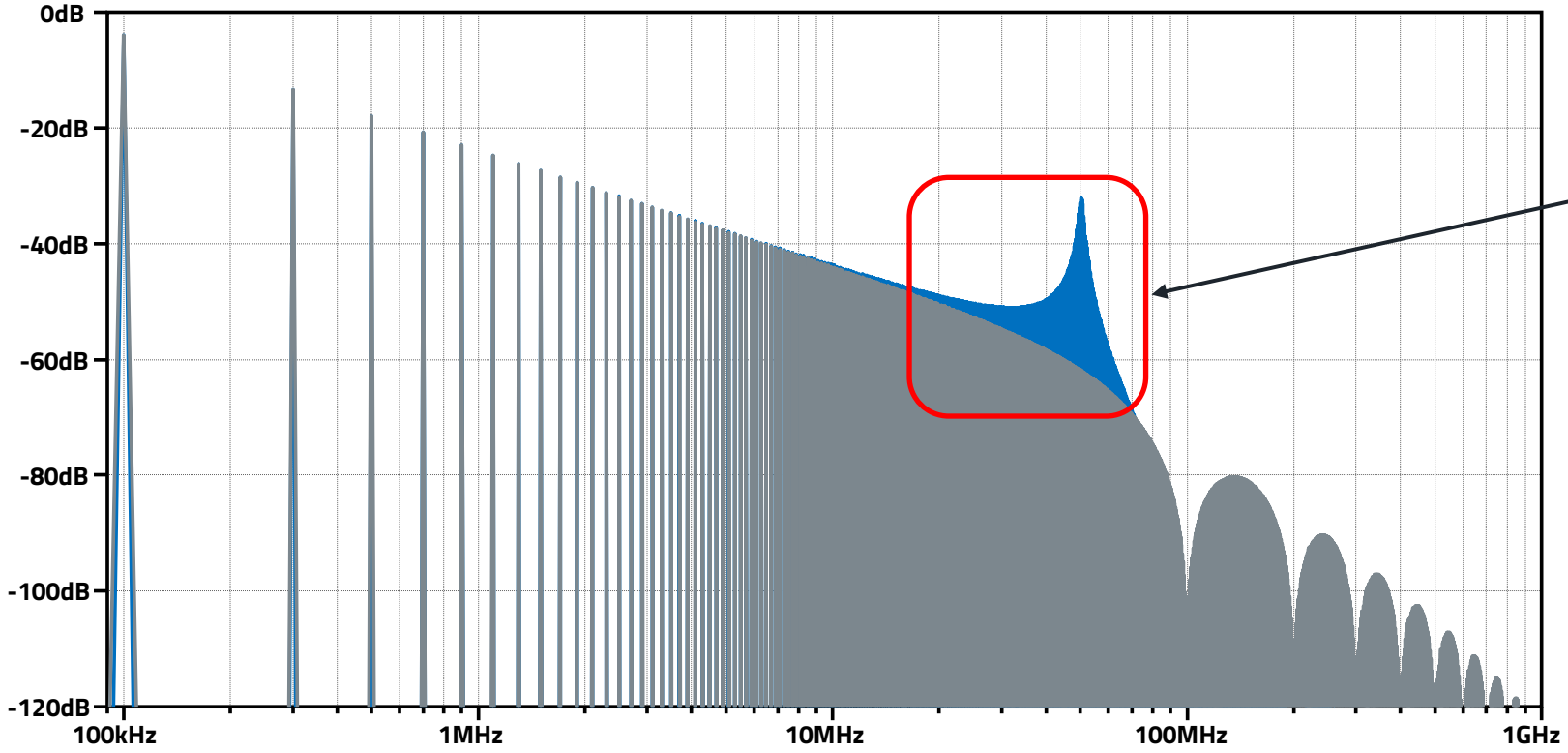
$\hat{U} = \sqrt{2}$ / f = 100kHz / t_{sl} = 10ns vs. 100ns / D = 10% or. D = 90%

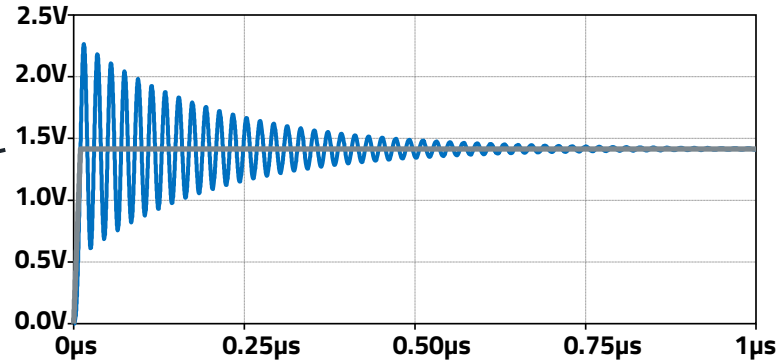
Link to LTspice simulation

- The frequency response begins to drop significantly at frequencies that are higher than the frequency determined by the rise- and/or fall-time (=slope-time)
- An increase of the rise- and fall-time by factor 10 reduces the amplitude of the high-frequency harmonics also by factor 10 (-20 dB)

Noise from the Diode/FET

Spectrum of a trapezoidal voltage/current waveform depending on ringing





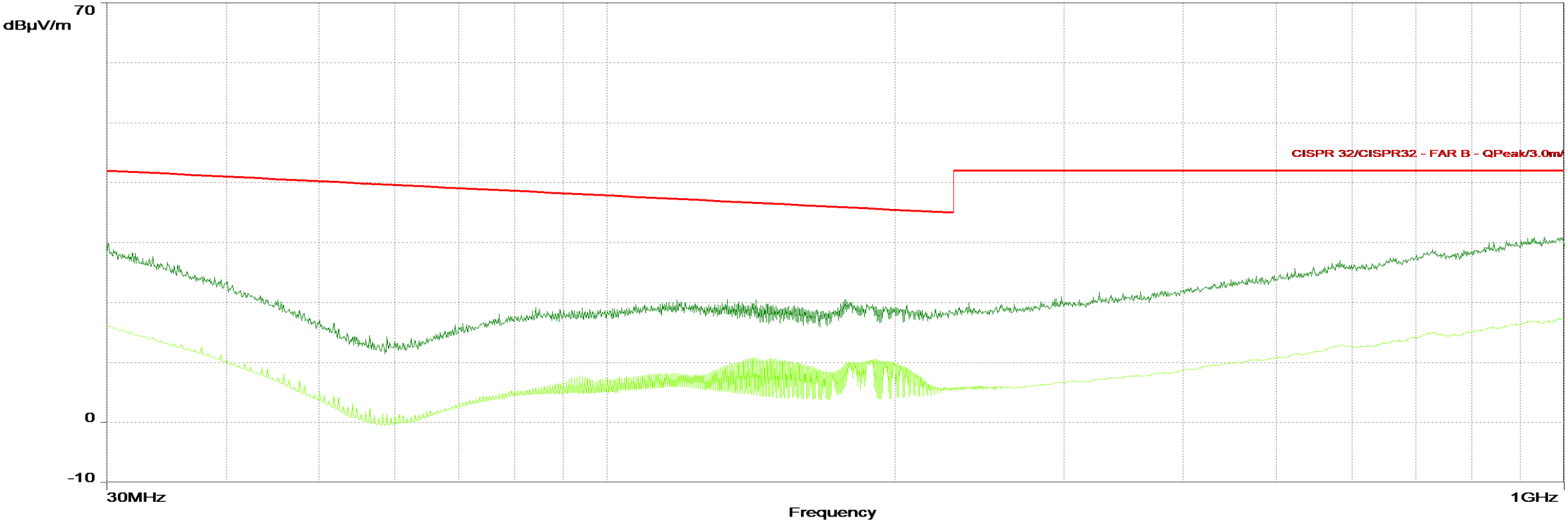
- The ringing introduces higher-frequency components (harmonics)
- In the example, the harmonics around 50MHz (resonance frequency) are about 30dB (32x) higher in comparison with the signal without ringing
- It is possible that the trace on which the signal propagates acts as an efficient (resonant) antenna at these higher frequencies

$\hat{U} = \sqrt{2}$ / f = 100kHz / t_{sl} =10ns / D = 50% / 50MHz ringing vs. No ringing

Link to LTspice simulation

EMC Test Lab - Good Design

CISPR32 Radiated Emission



Good Design: With all Filters and Chip Bead Ferrite after Schottky Diode

EMC Measurement Conducted up to 600MHz - Good Design

FAE Equipment - Good Design CM