EMC DESIGN TIPS

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FAE

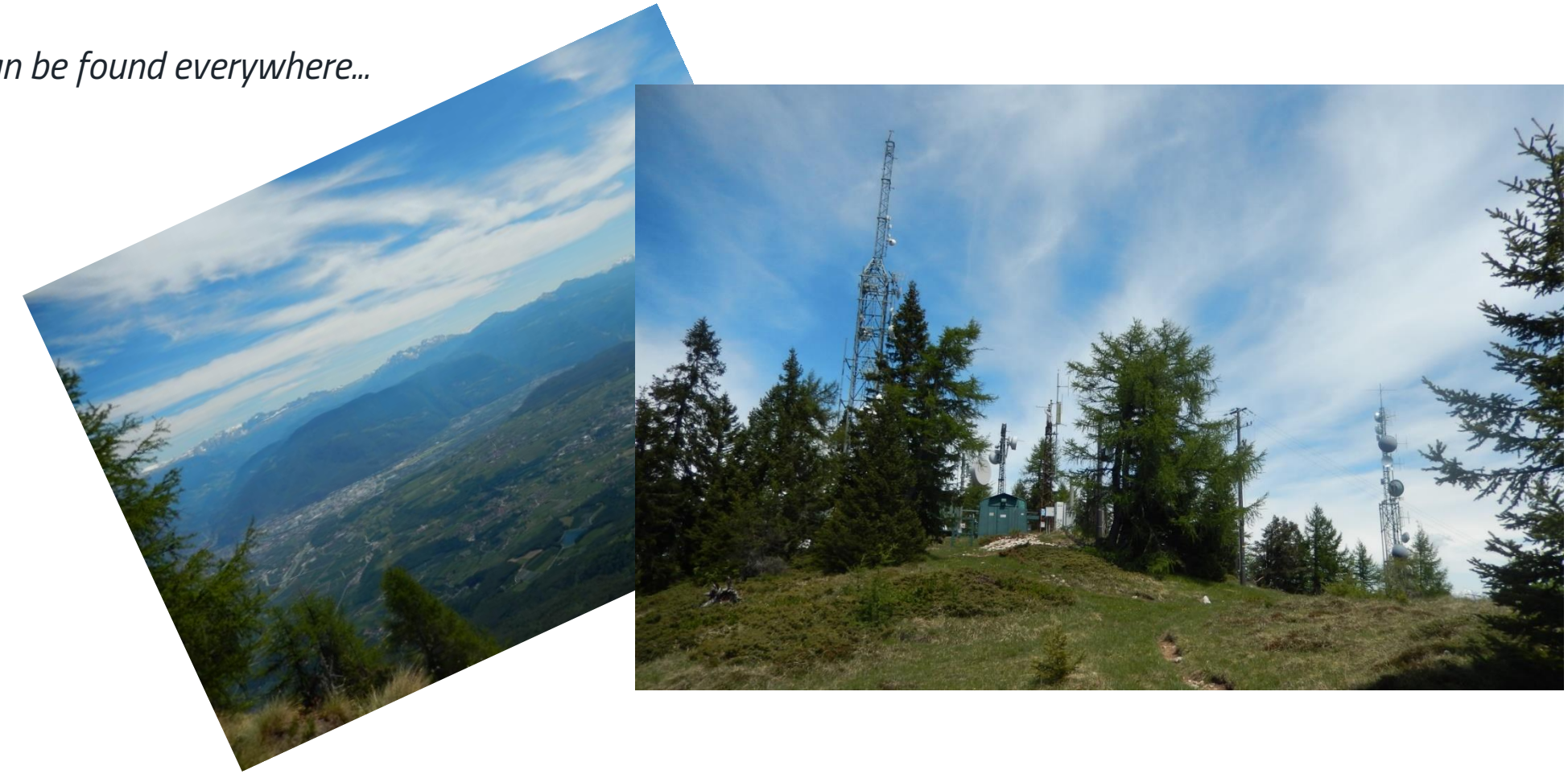
WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

Agenda

- Coupling paths
  - Shielding demonstration
  - Coupling demonstration
- Ground Concept
- Power Integrity
- Layer Stack
- Arrangement of Traces & Vias
- Filter Placement
- Grounding
- Layout Considerations
  - Power Inductors
  - Crystals & Oscillators

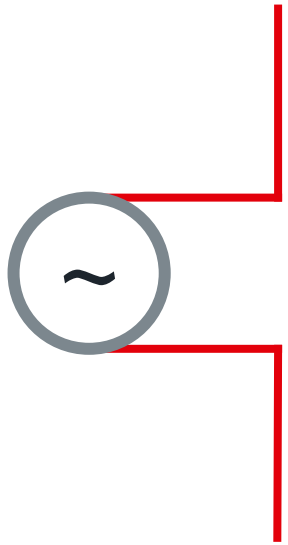
EMI

EMI and HF can be found everywhere...

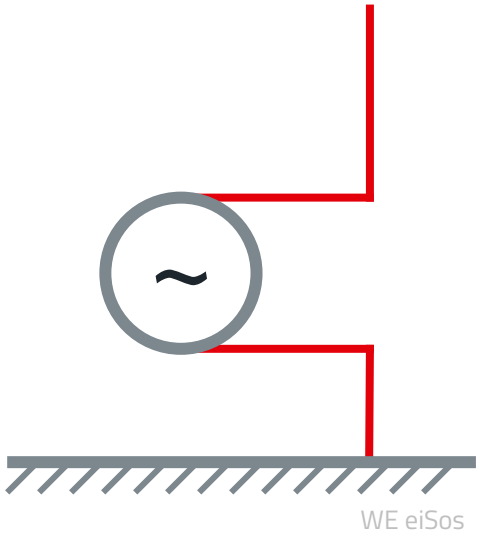


COUPLING PATHS

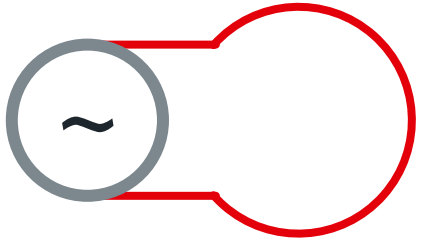
Everything is an Antenna



Electric Dipole Antenna



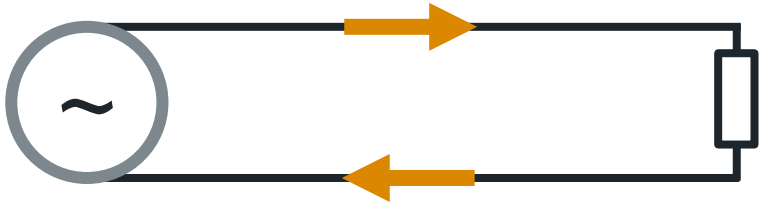
Electric Monopole Antenna



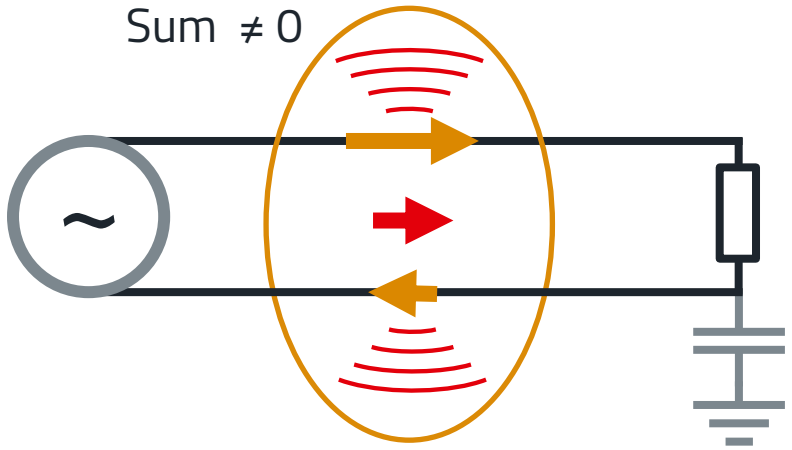
Magnetic Loop Antenna

Everything is an Antenna

...even if there is no Antenna



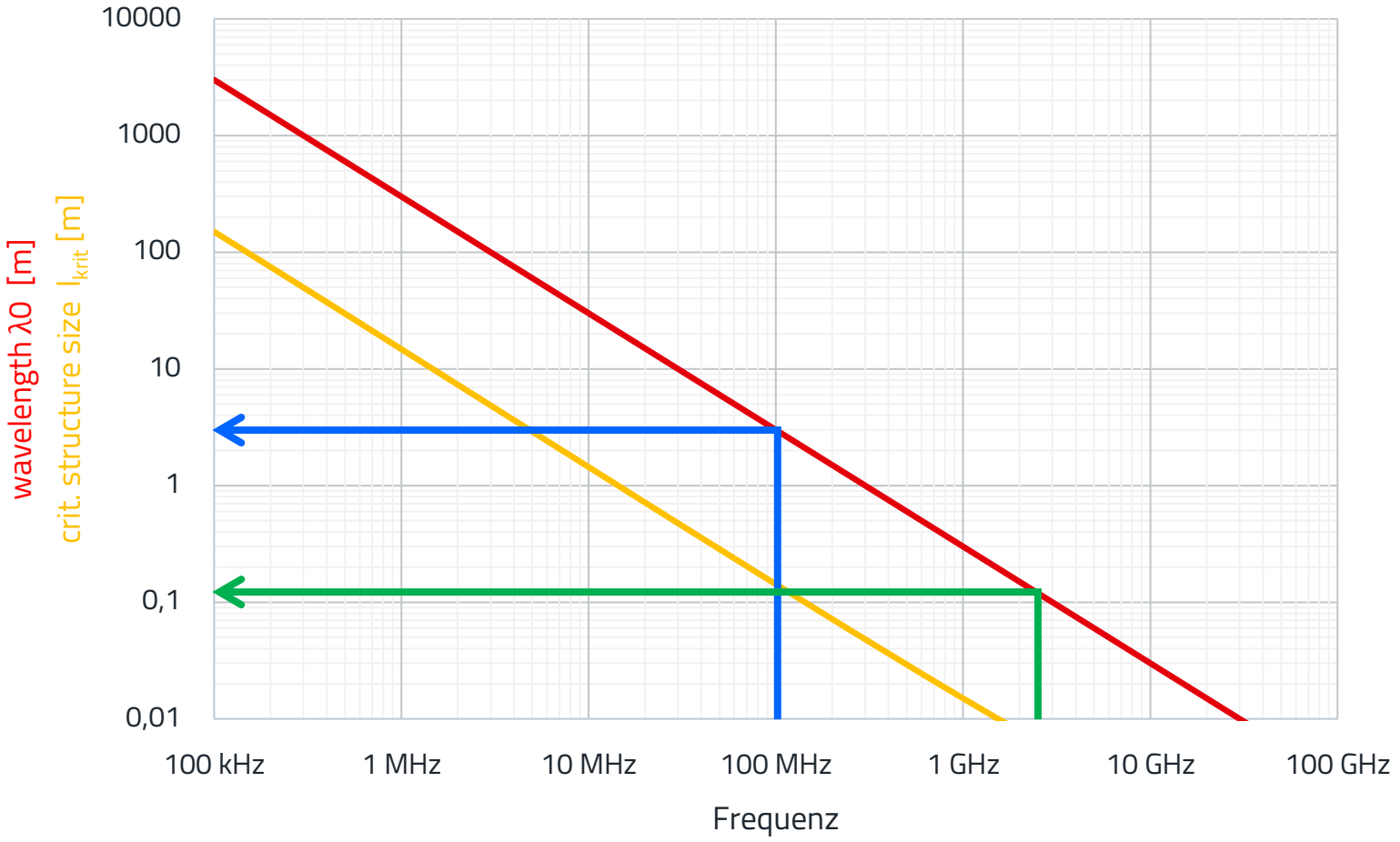
Differential Mode



Common Mode

Radiated coupling

Frequency, wavelength



- Vacuum

$$\lambda_0 = \frac{c_0}{f} = \frac{1}{f \cdot \sqrt{\varepsilon_0 \cdot \mu_0}}$$

$c_0 = 299792458\text{m} \cdot \text{s}^{-1}$

$$\lambda_0 \approx \frac{300}{f\ [MHz]}$$

- Critical wavelength
  - ➢ Structures that tend to radiate into the far field

$$l_{\text{krit}} \approx \frac{\lambda_0}{10} \ldots \frac{\lambda_0}{20}$$

- Medium

$$\lambda = \frac{1}{f \cdot \sqrt{\varepsilon_0 \cdot \mu_0} \cdot \sqrt{\varepsilon_r \cdot \mu_r}}$$

1) FM-Radio @ 100MHz

- $\lambda_0 = 3\text{m}; \frac{\lambda_0}{4} = 75\text{cm}; \frac{\lambda_0}{20} = l_{\text{krit}} = 15\text{cm}$

2) WiFi @ 2,4GHz

- $\lambda_0 = 12{,}5\text{cm}; \frac{\lambda_0}{4} = 3{,}13\text{cm}; \frac{\lambda_0}{20} = l_{\text{krit}} = 6{,}25\text{mm}$

Radiation emissions

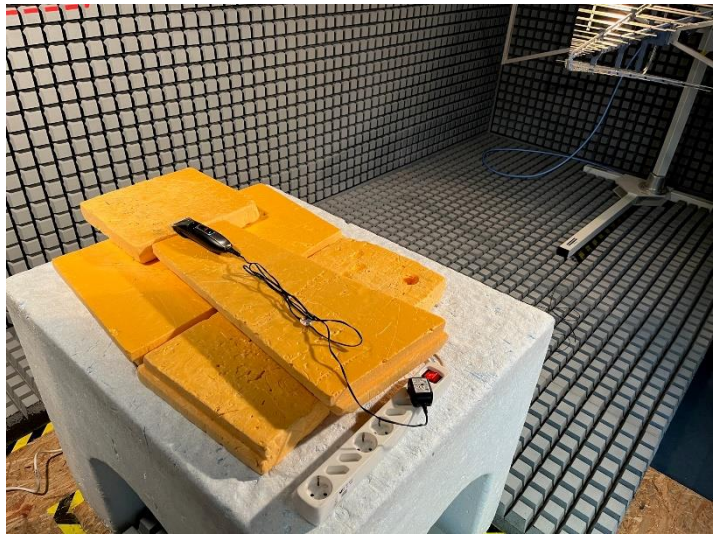
Measurement setup

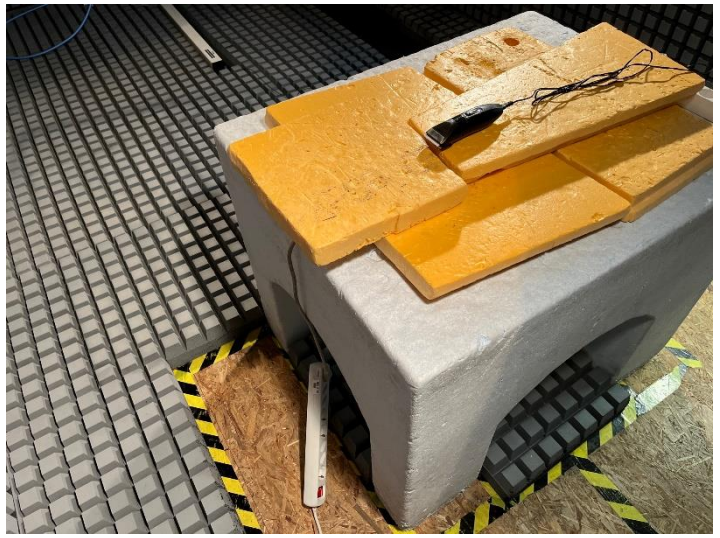
- Fully Anechoic Chamber (FAC):
  - Absorbers also on the floor – no superposition of direct and reflected ray: no height Scan.
  - No change in the setup between emissions and immunity – easy to handle for labs..
  - The DUT needs to be in the height of the antenna tip – FAC is made for table top equipment and not for floor
  - standing Equipment.

Radiated emissions

Example - electric shaver

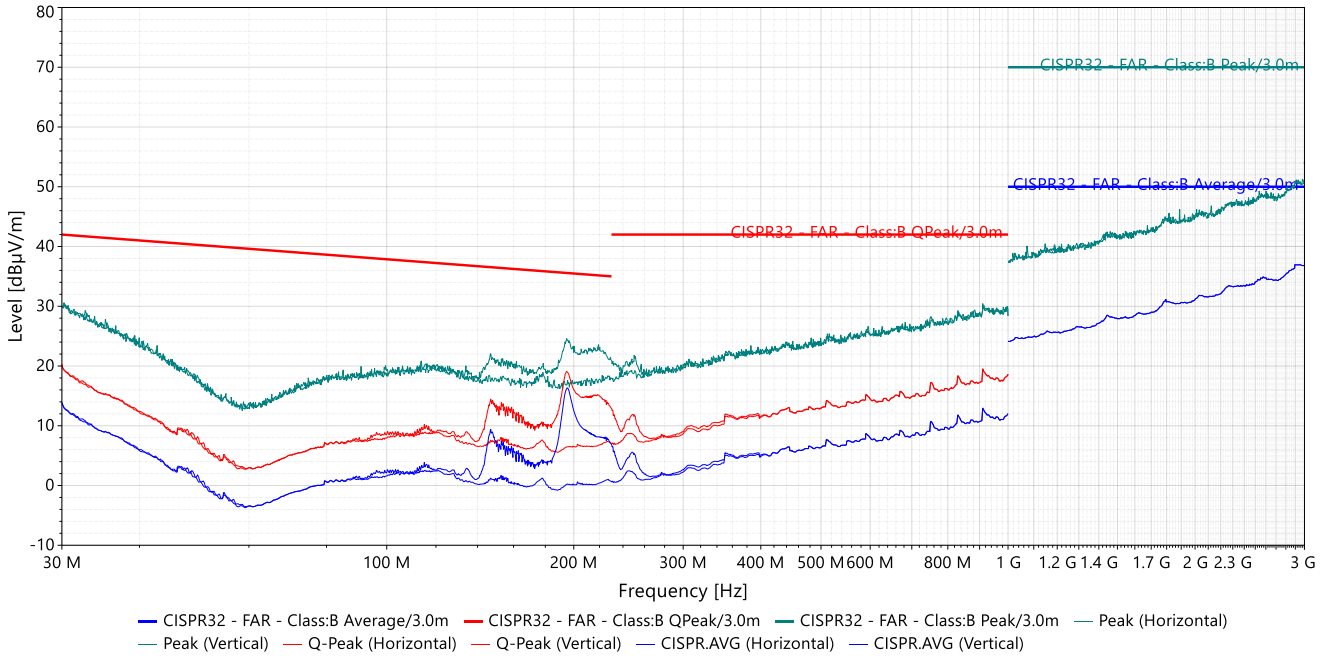
- Charging mode:
  - Charger is part of the DUT
- Shaving mode:
  - Battery powered without cable
- Using it wrong?
  - Shaving mode with cable





Radiated emissions

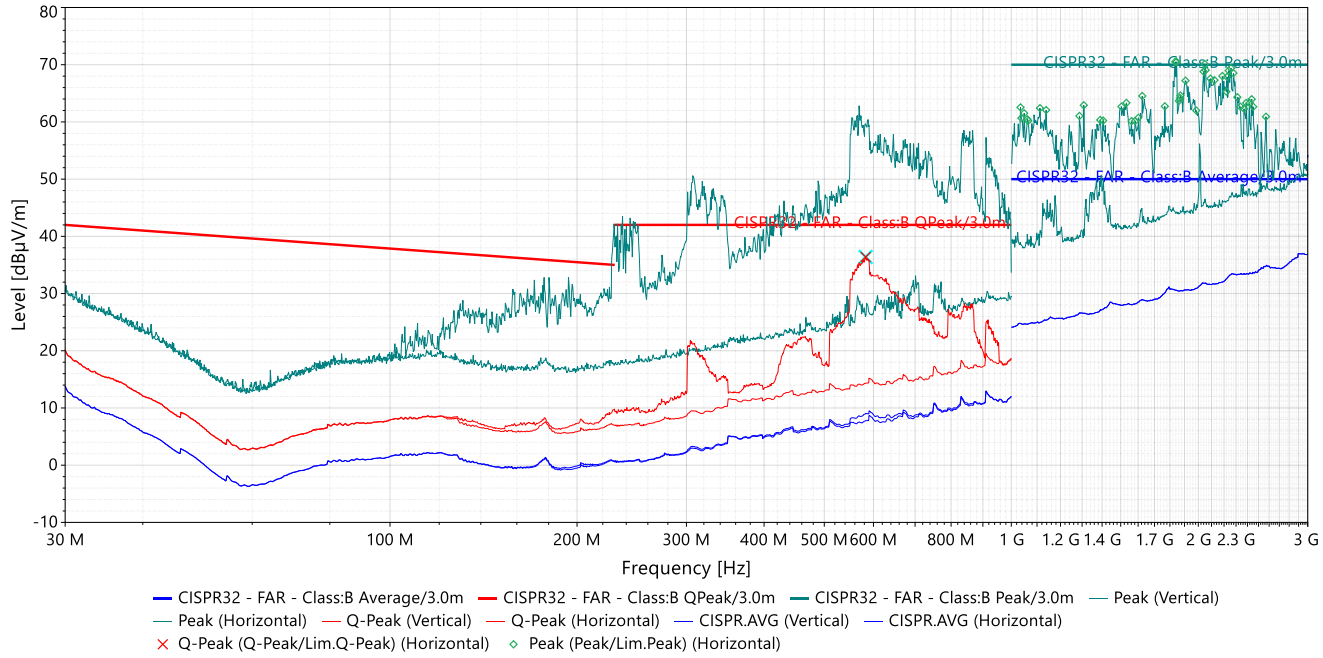
Example - electric shaver: Charging mode



Radiated emissions

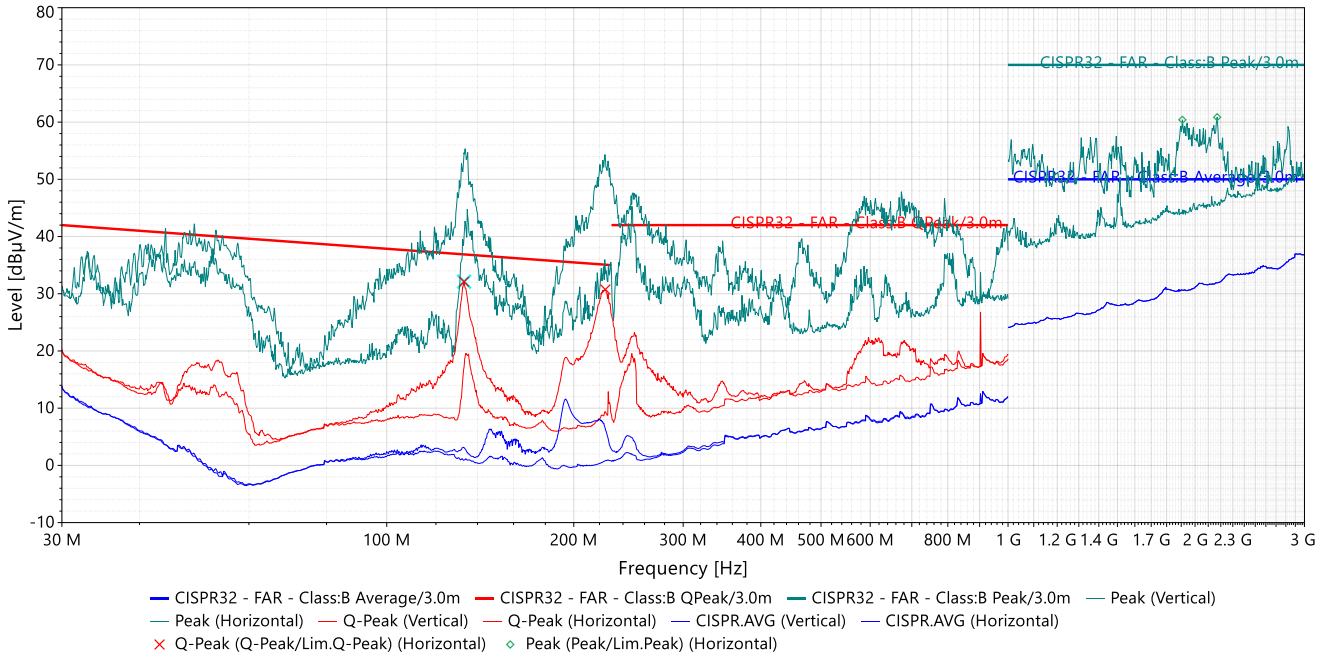
Example - electric shaver: battery powered working mode

- High peak detector:
  - Brushed motor
  - Motor bursts
- CISPR 14-1-1:
  - No Limits above 1 GHz



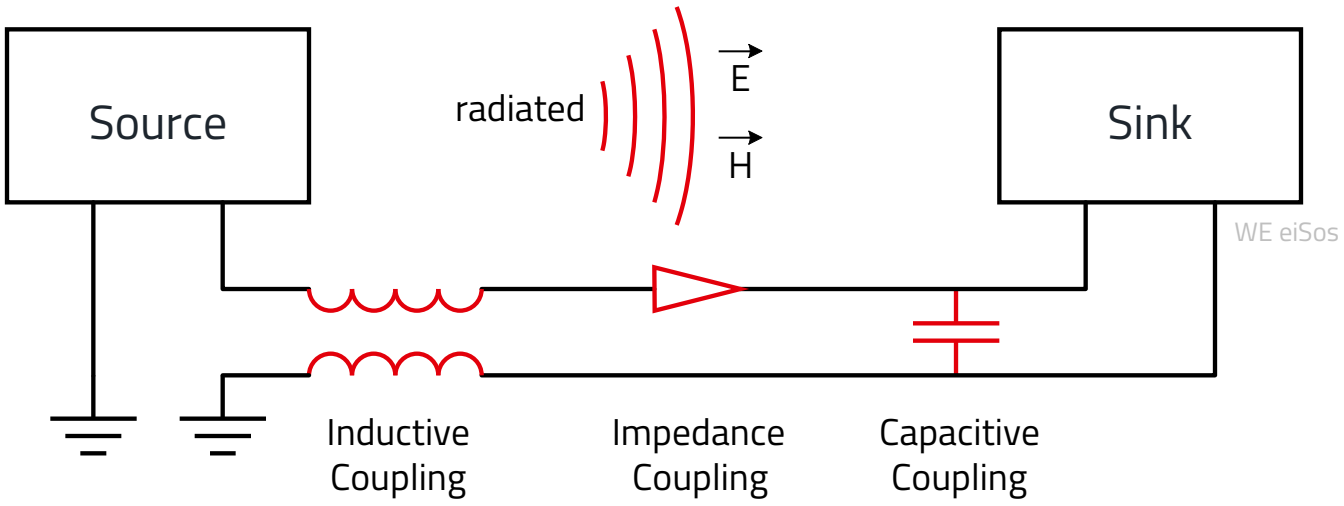
Radiated emissions

Example - working mode with cable



Reducing EMI

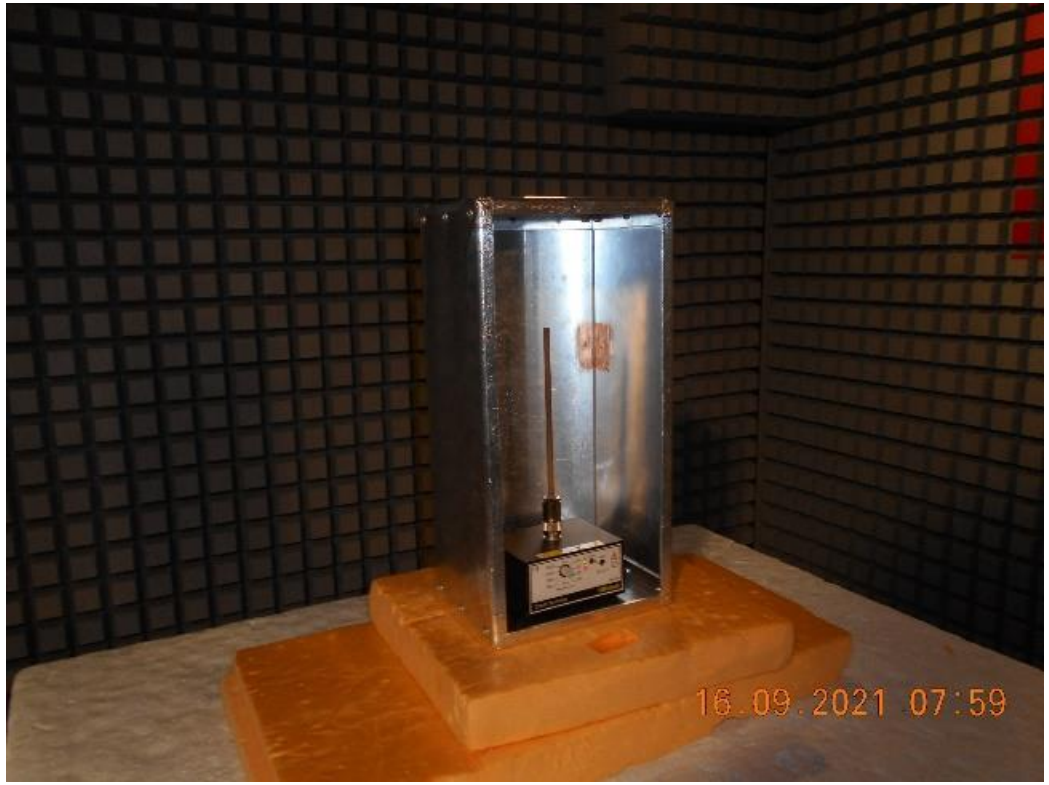
- Sufficient EMC can be achieved by suited measures at the noise source, coupling path or sink.
  - **Primary Measure** Reduce emission from noise source
  - **Secondary Measure** Break coupling paths
  - **Tertiary Measure** Increase immunity of the sink

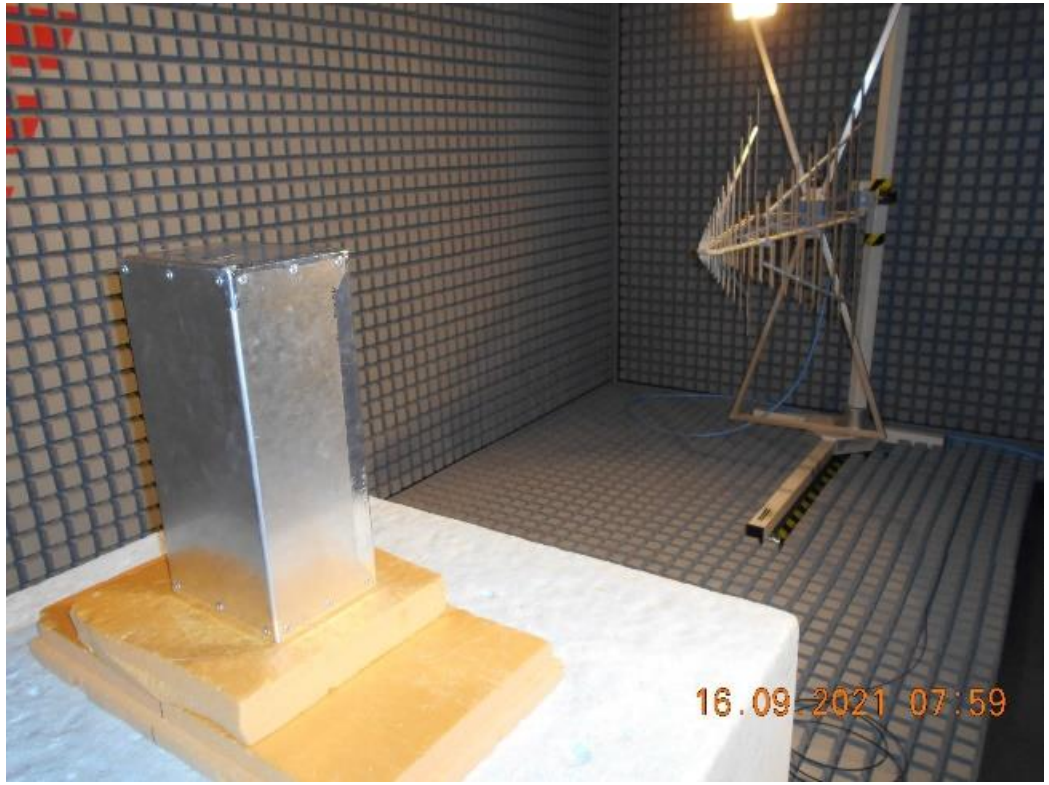


SHIELDING DEMONSTRATION

Shielding Demonstration

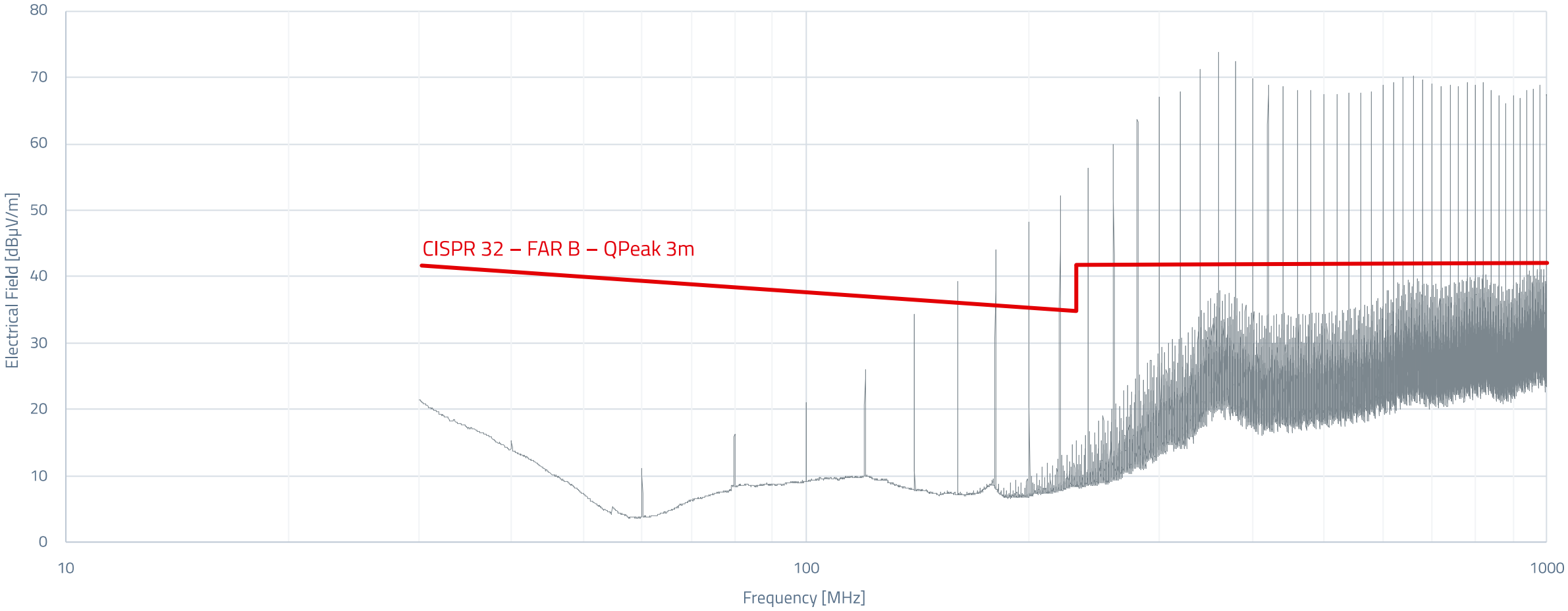
DUT: Comb generator with 20 MHz harmonics





Shielding Demonstration

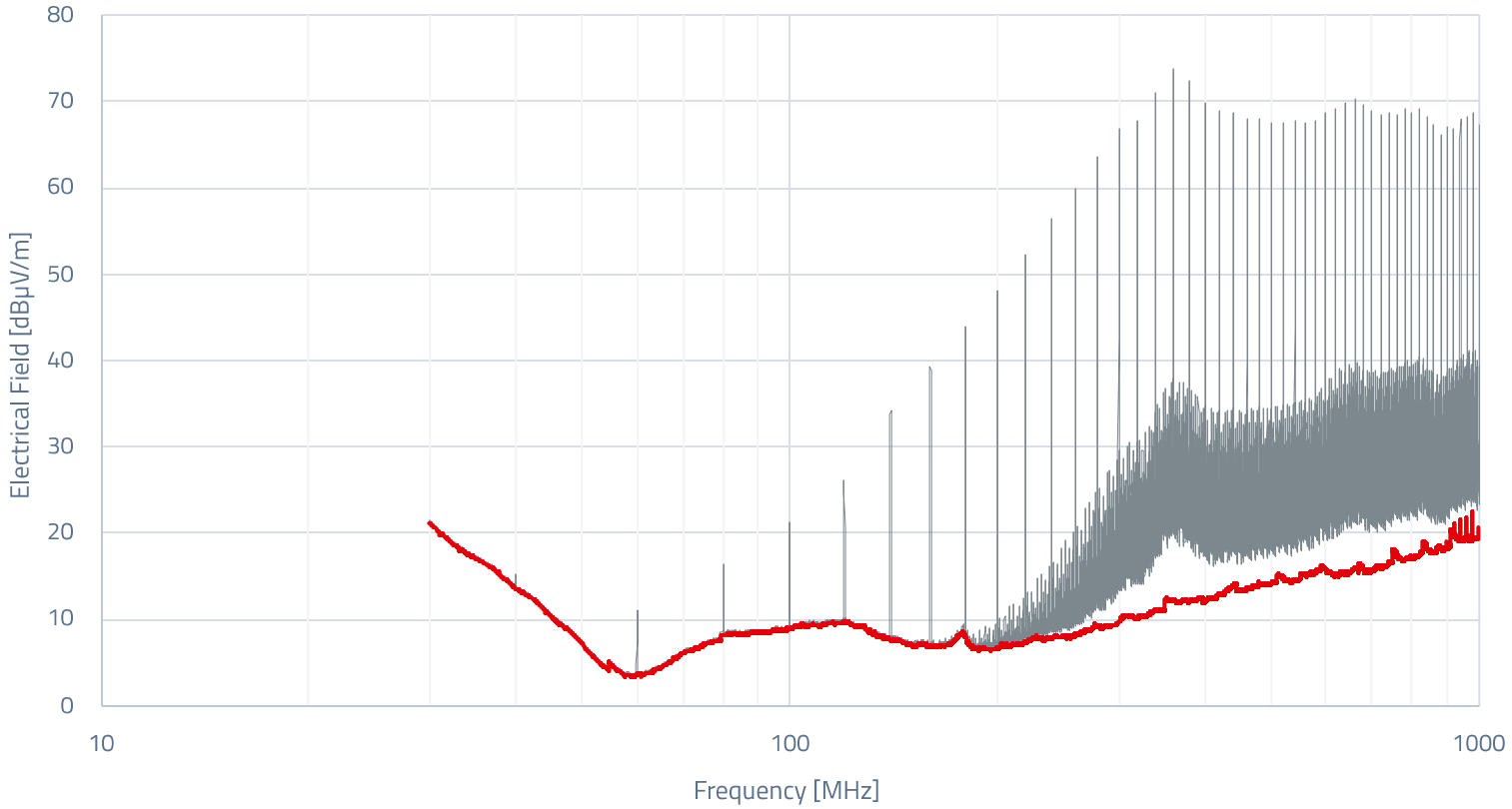
Unshielded Noise source for Reference



Shielding Demonstration

Fully Shielded Box

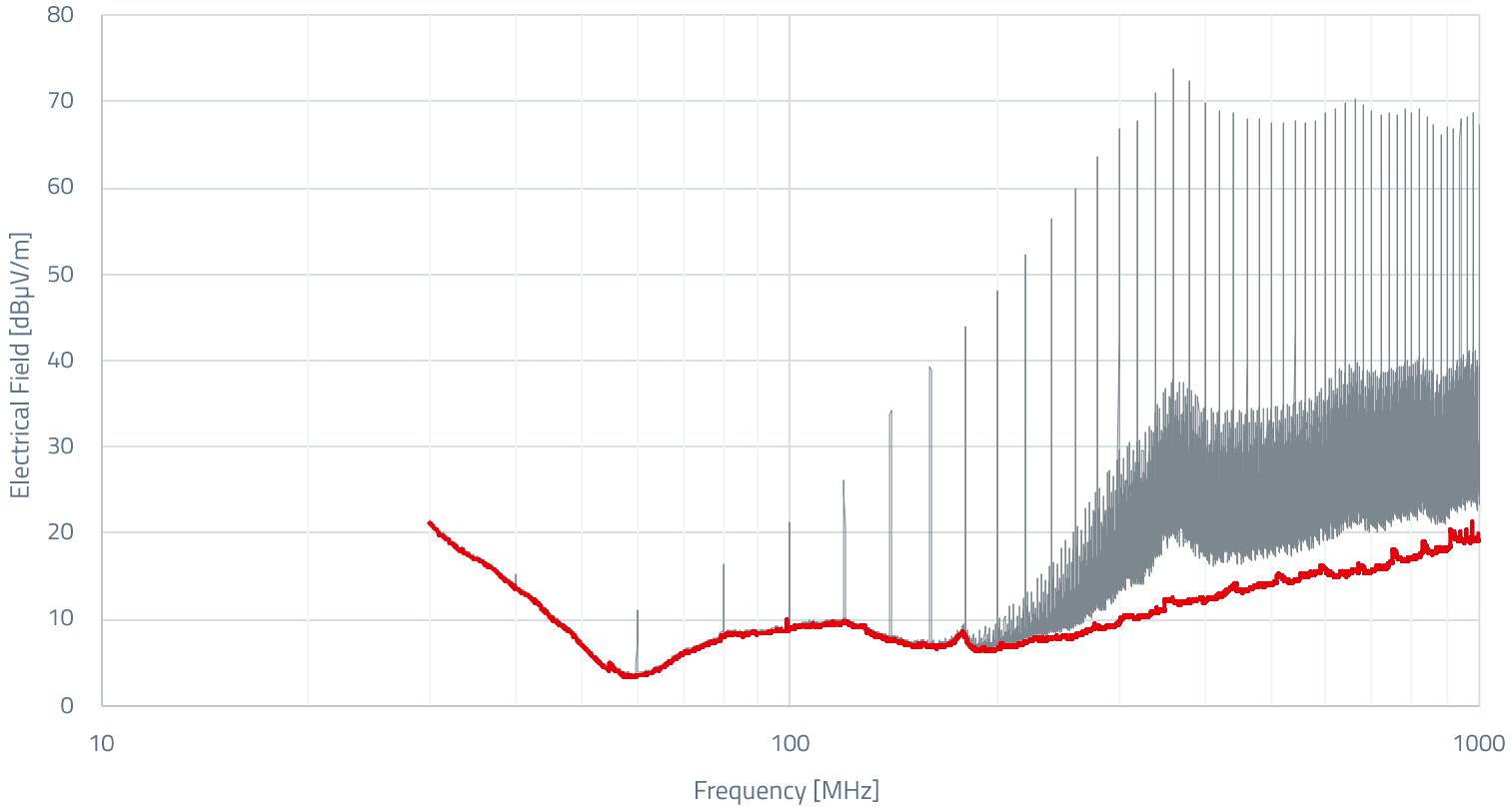
- DUT in the Box, Sealed with tinfoil and copper tape
- 60 dB Attenuation @ 360 MHz.

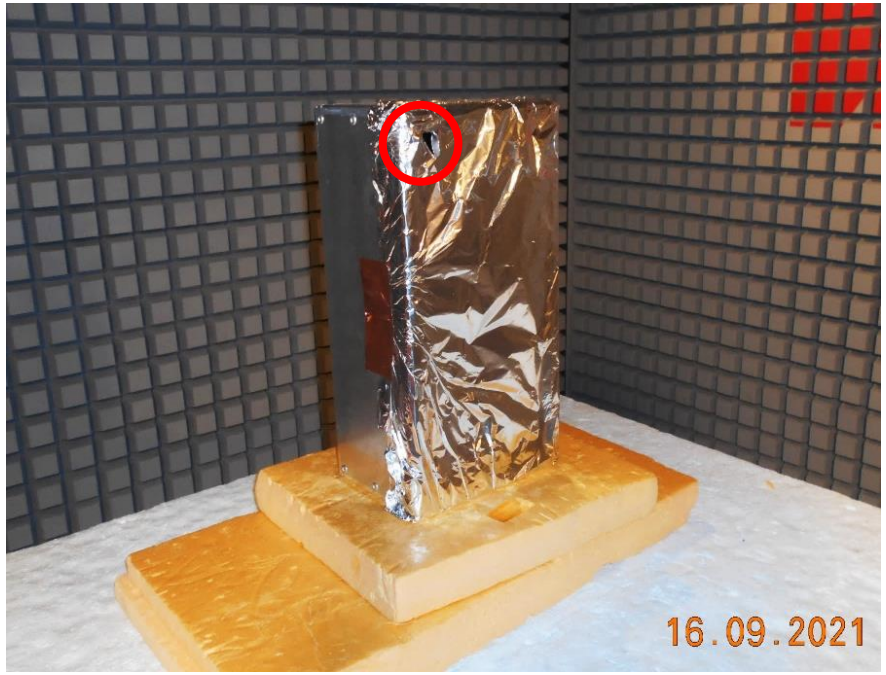


Shielding Demonstration

Shielded Box, 20mm hole

- Completely sealed housing can rarely be realized
  - Interfaces, Cooling, Maintanance

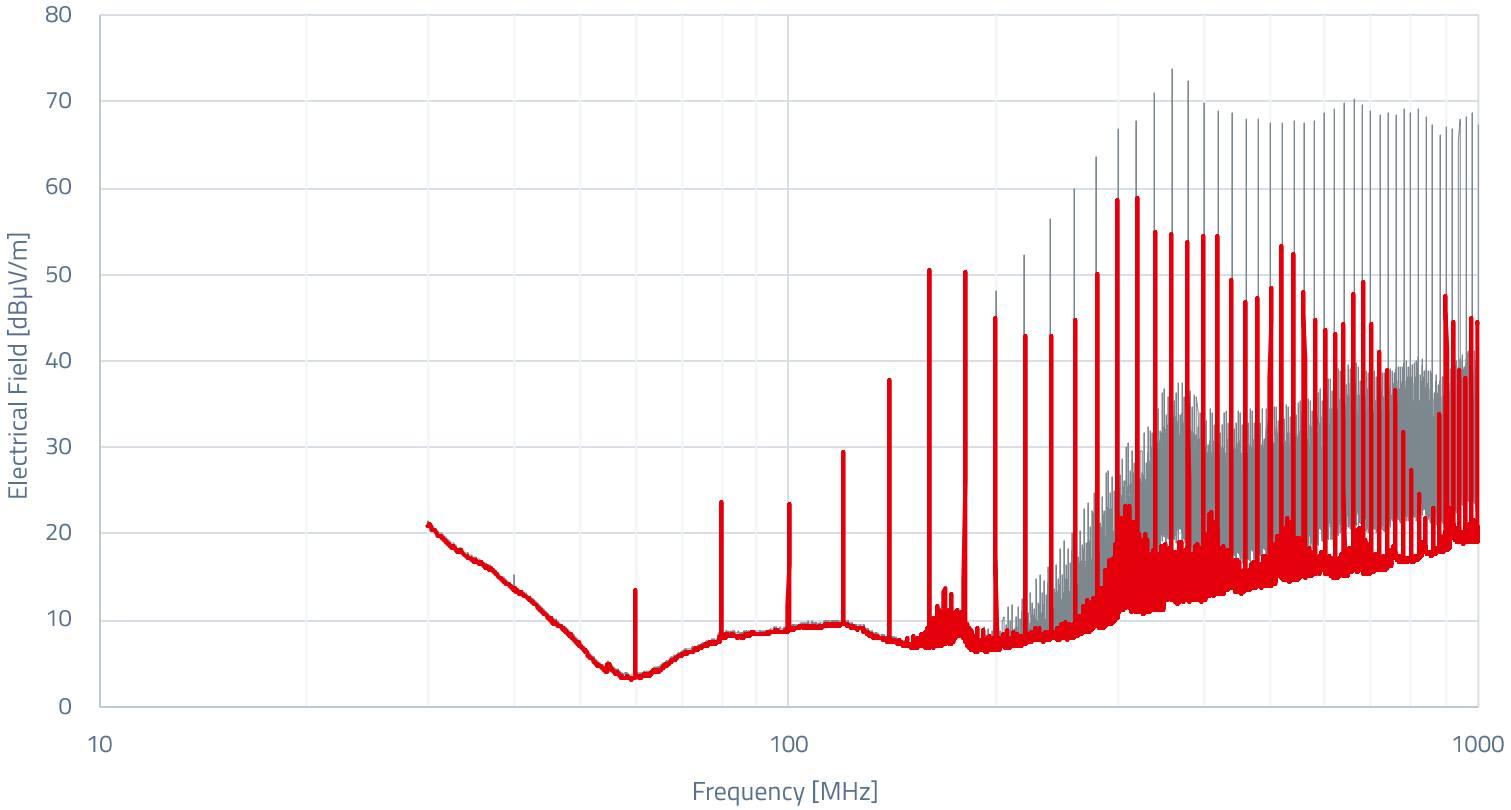


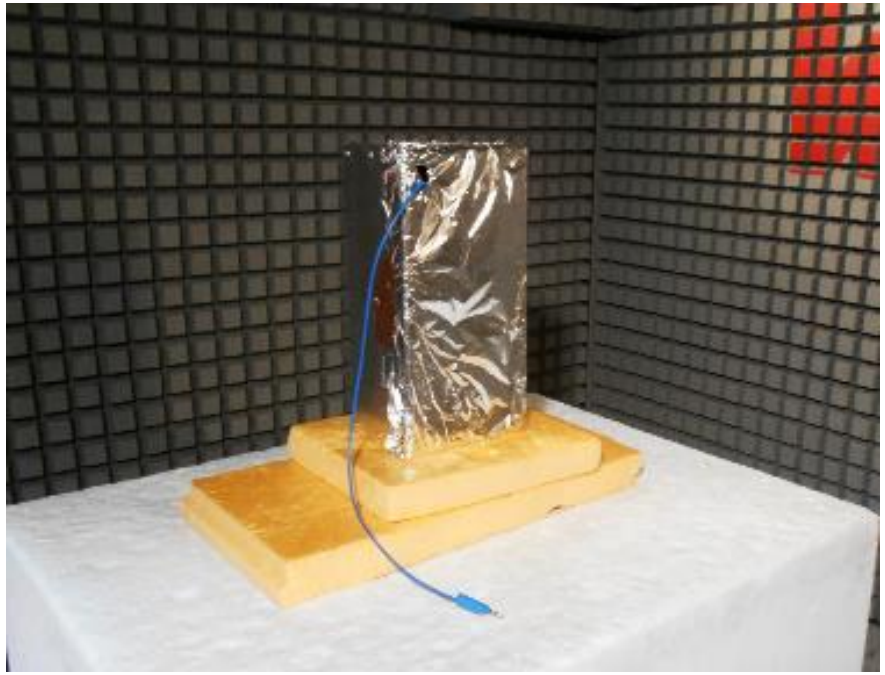


Shielding Demonstration

Shielded Box, 20mm hole and 50cm Cable

- Completely sealed housing can rarely be realized, e.g. due to Interfaces
- The Cable is **not connected** to the noise source

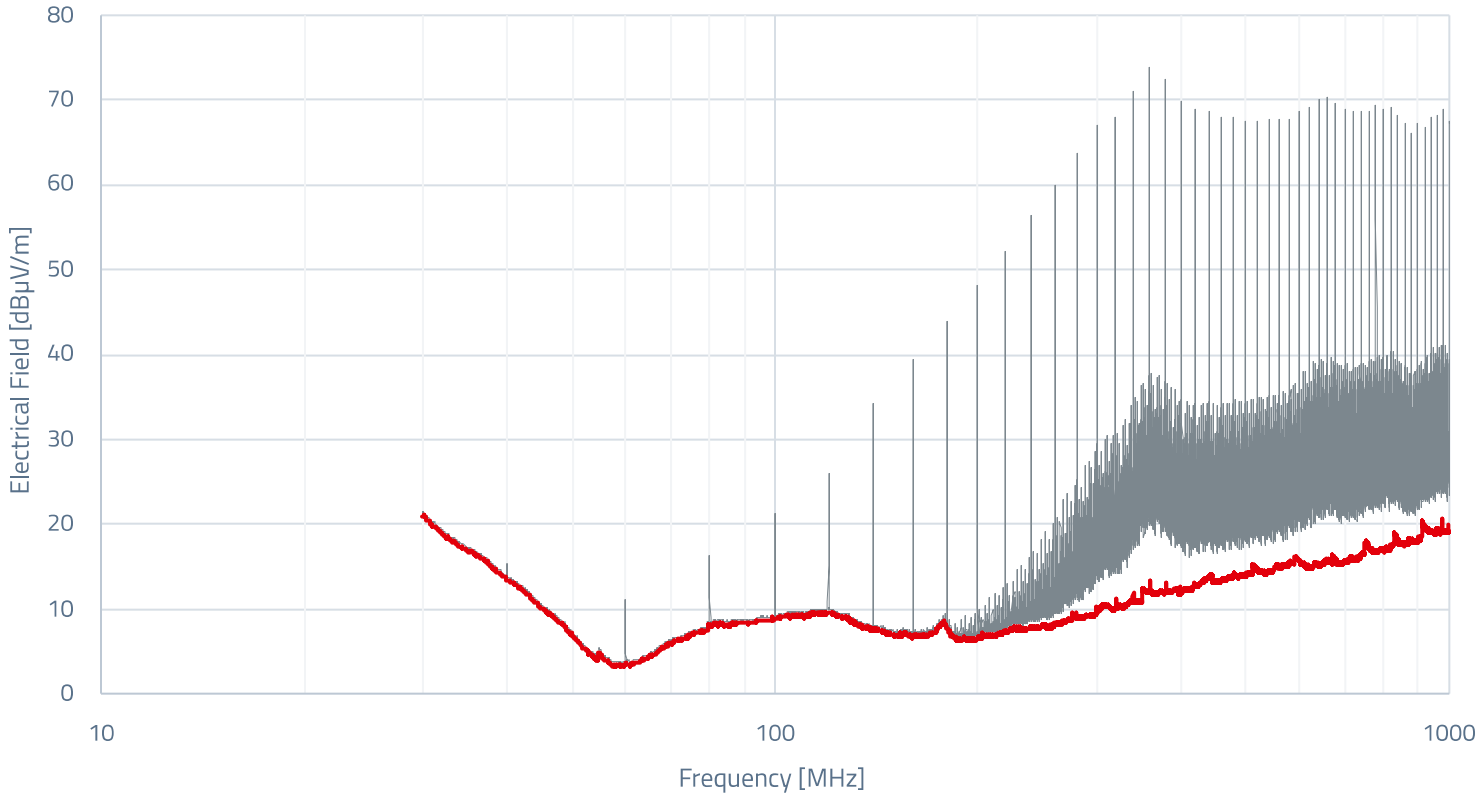




Shielding Demonstration

Shielded Box, several small holes

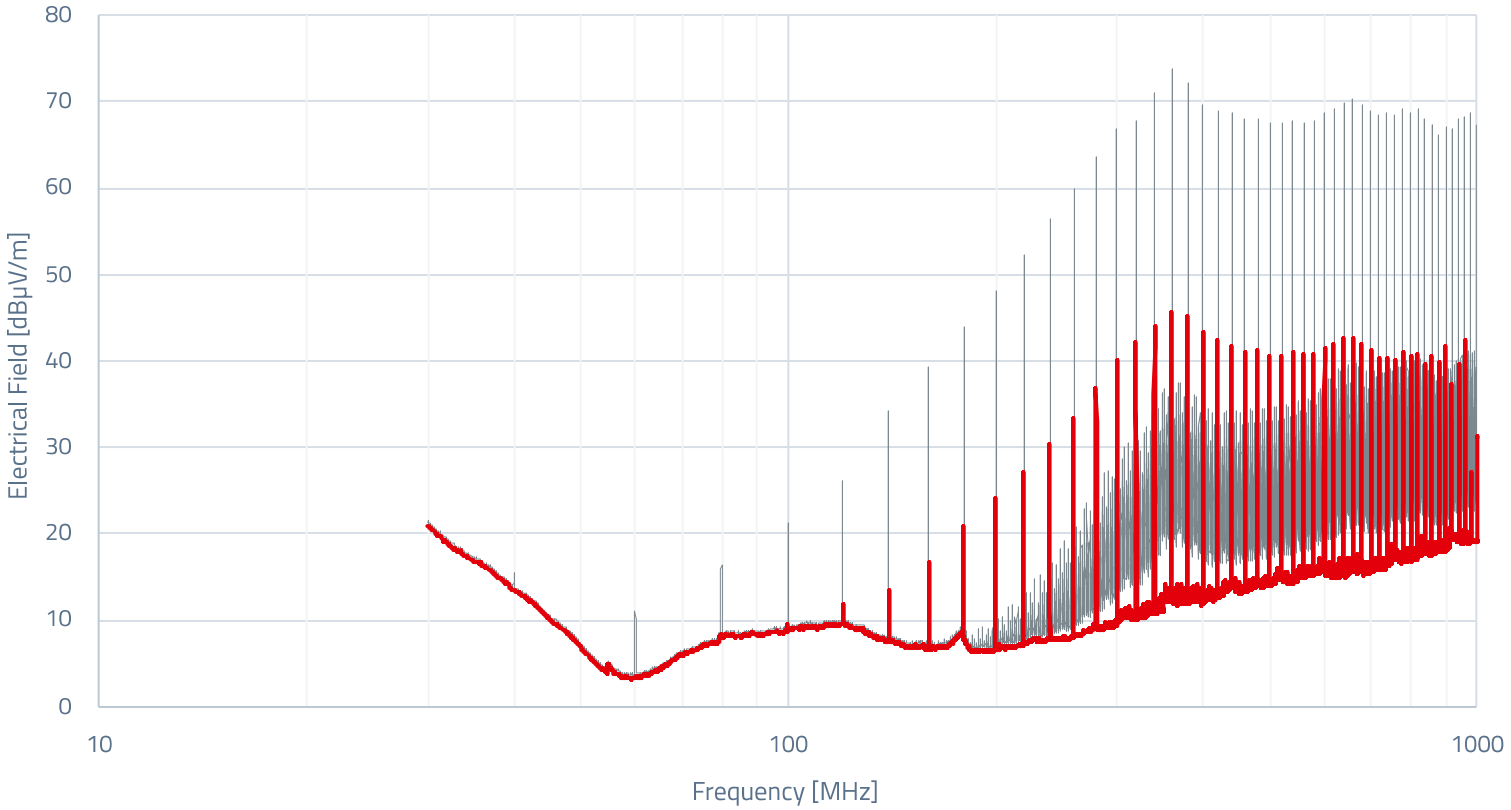
- Completely sealed housing can rarely be realized, e.g. due to cooling
- A grid of small holes emulates ventialation gilles



Shielding Demonstration

Shielded Box, several 20cm slits

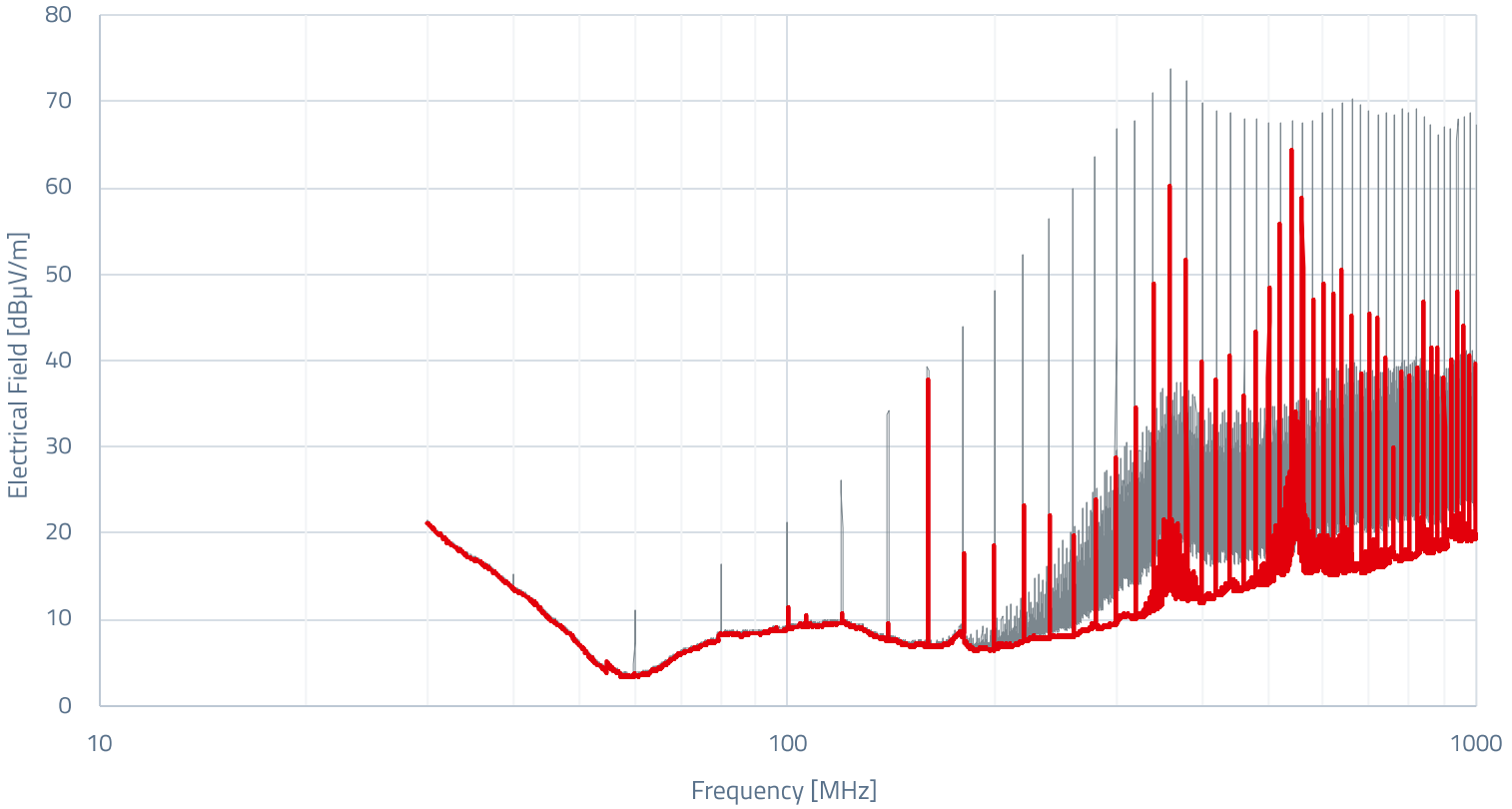
- Completely sealed housing can rarely be realized, e.g. due to cooling
- Sometimes slits are used for ventilation

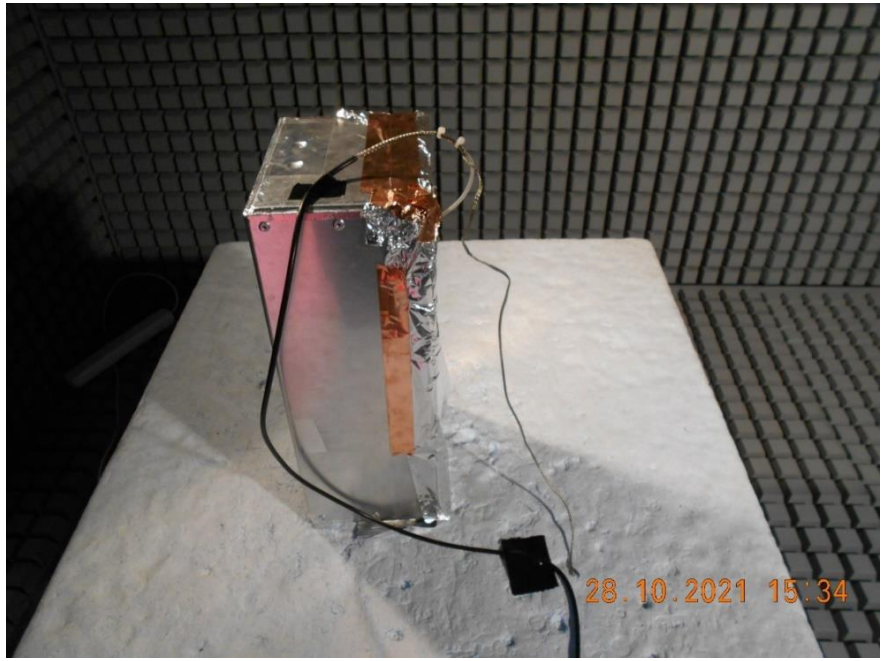


Shielding Demonstration

Shielded Box, 20mm hole, BNC-Cable, Shield is not connected

- Inside the box, the shield is stripped from the cable
- The Shield is **not connected** to the Box

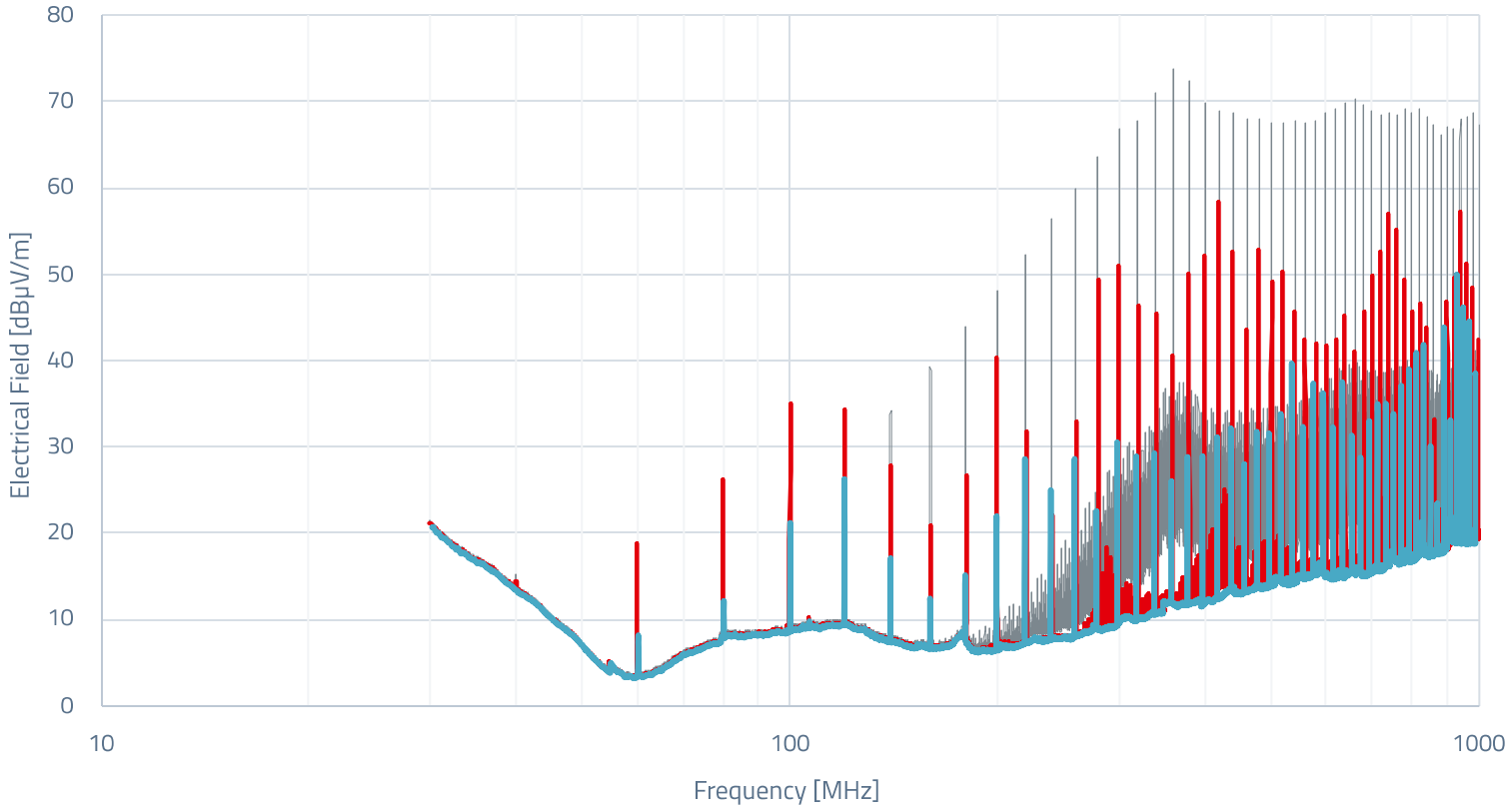


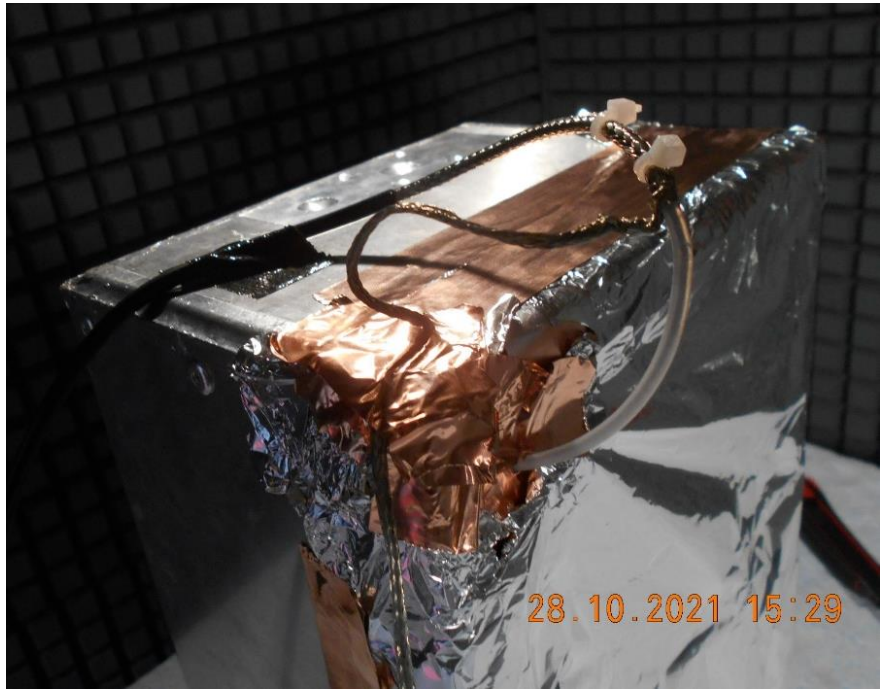


Shielding Demonstration

Shielded Box, BNC-Cable, Shield connected by pigtail

- Inside the box, the shield is stripped from the cable
- The Shield is **connected** to the Box by a **10 cm Pigtail** / by a **2 cm Pigtail**

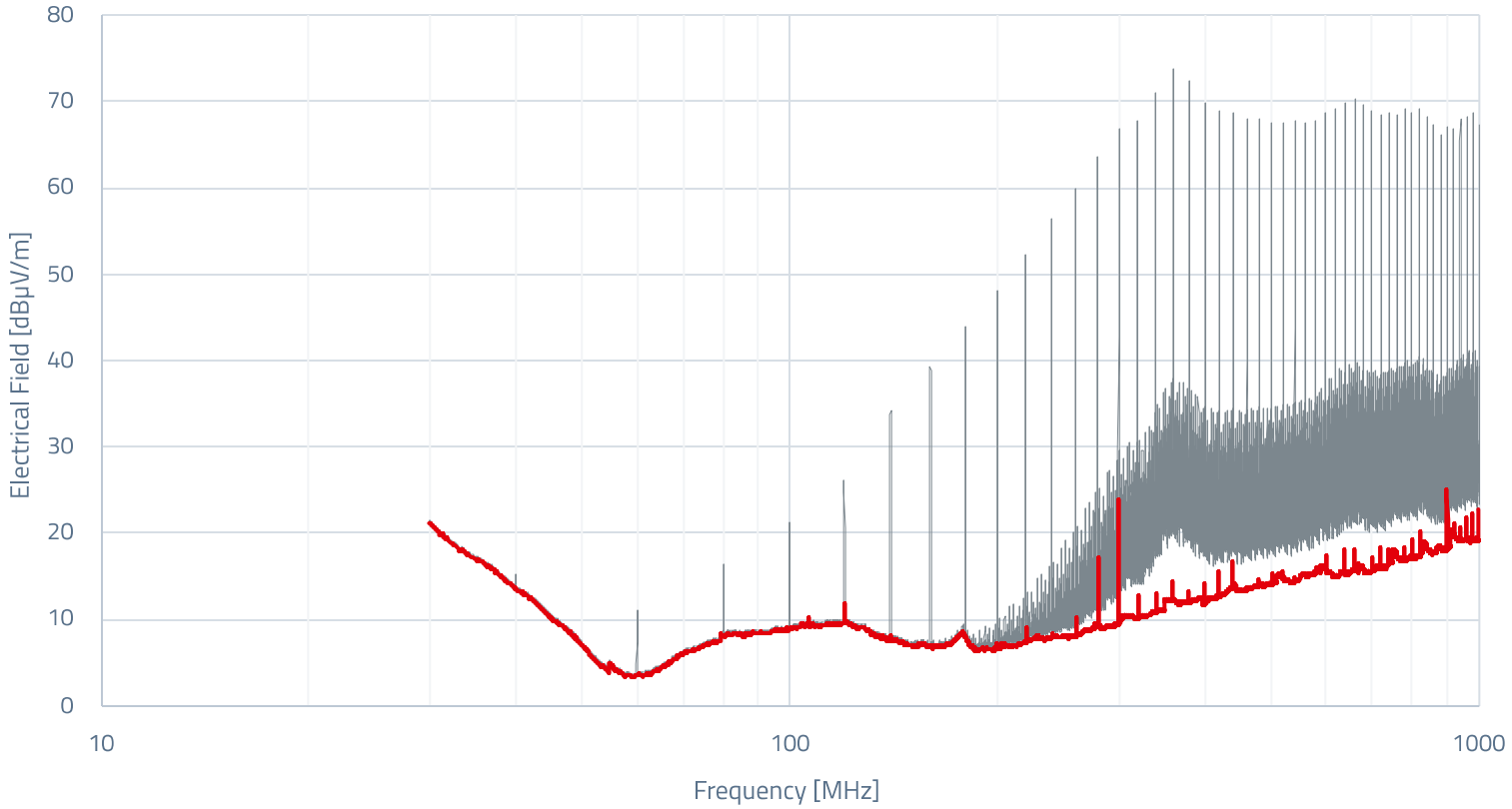


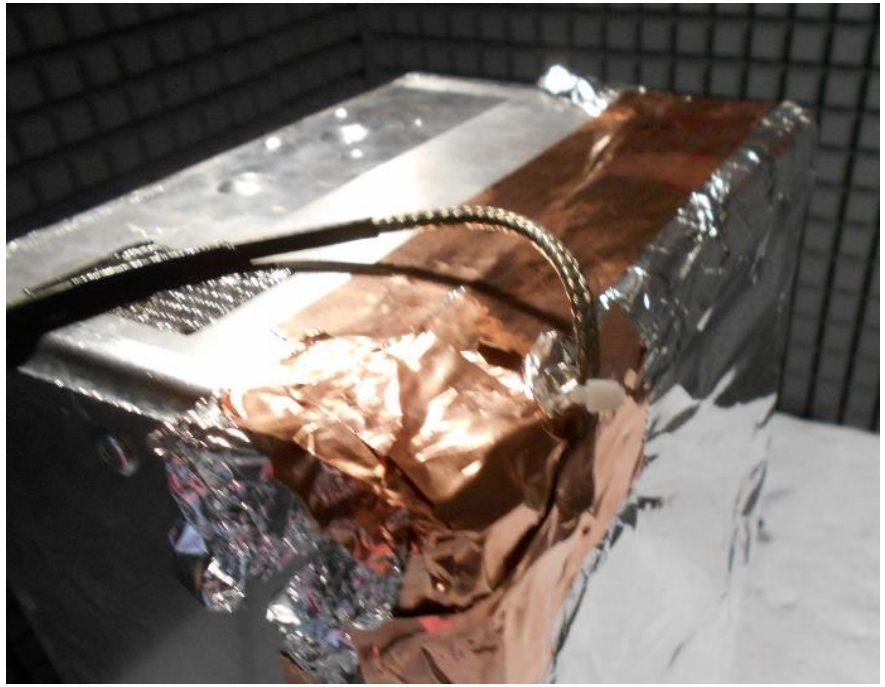


Shielding Demonstration

Shielded Box, BNC-Cable, Shield properly connected

- Inside the box, the shield is stripped from the cable
- The Shield is **connected** to the Box **360° with copper tape** (*not flawless*)





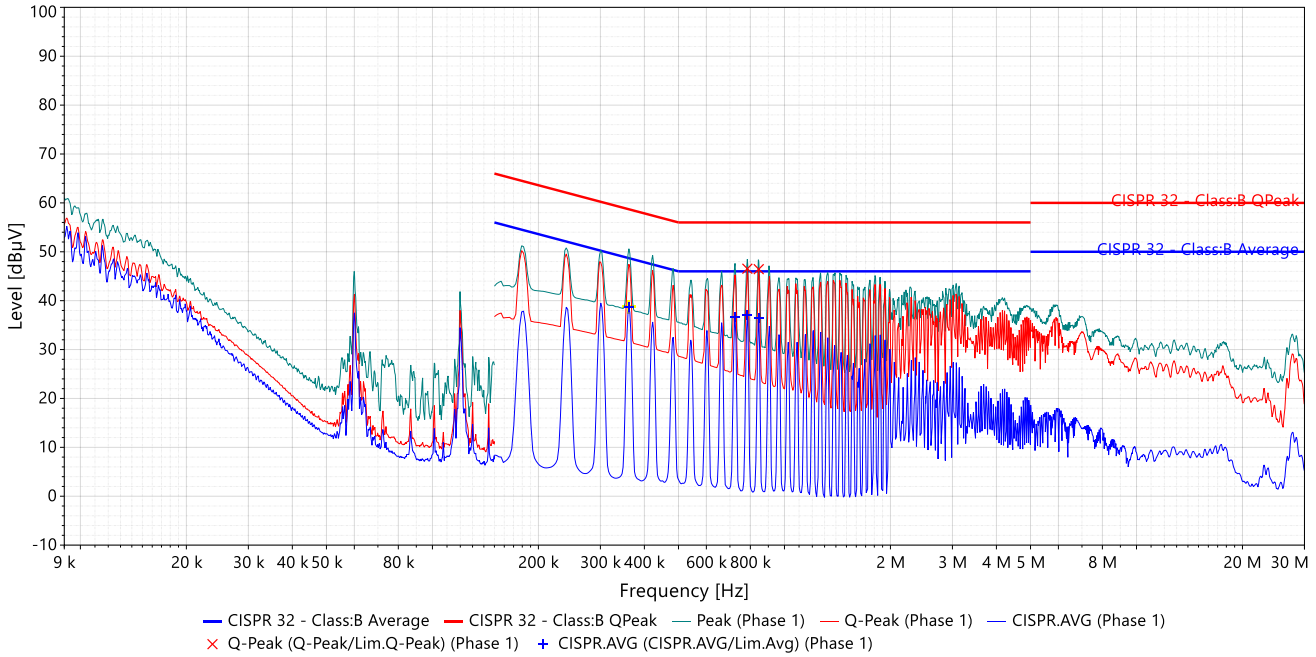
COUPLING PATHS

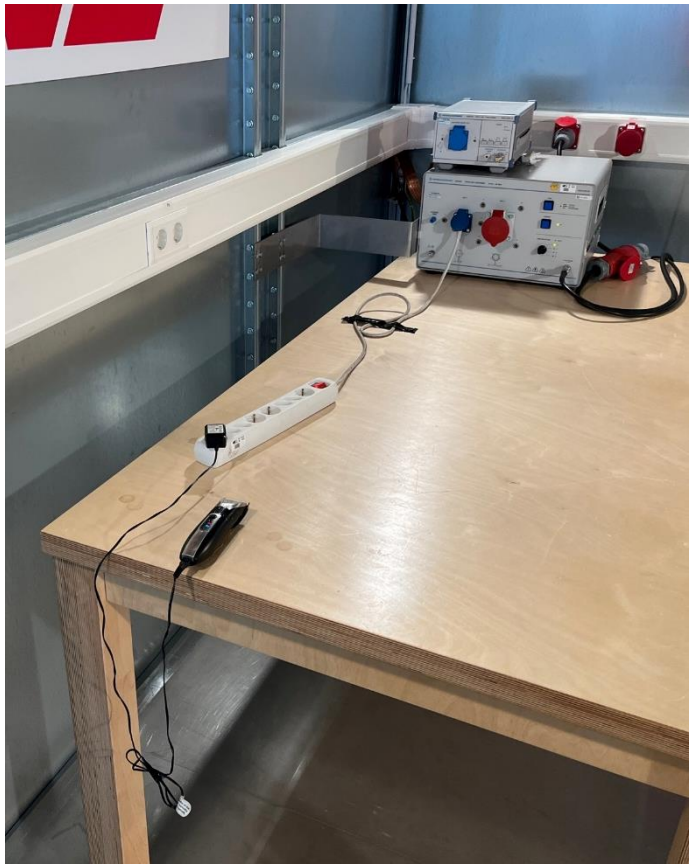
Conducted coupling

- Physical coupling path formed by a direct contact
- DUT and LISN (Noise Sink) are directly connected via a cable
  - Reduction of the noise source impedance due to low-impedance components (e.g. a low-impedance input capacitor in a DC/DC converter)
  - LC filter to interrupt the coupling path

Conducted emissions

Electric shaver emission test – charging mode

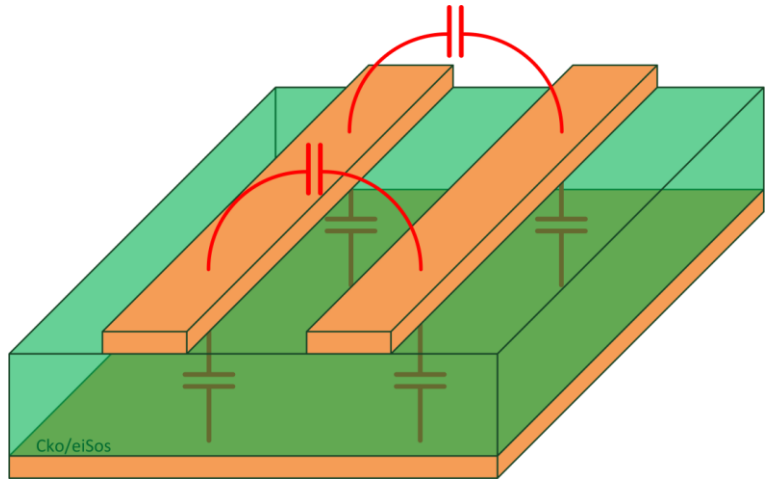




Capacitive Coupling

Origins

- Originates from high dU/dt
- Parallel conductors form a parasitic capacitance
- Coupling capacitance is directly proportional to the length of the parallel trace run



Isolating Components	typ. Coupling Capacitance
Optocoupler	0,5…5 pF
Solid State Relay	0,5…10 pF
Gate Drive Transformer	2…10 pF
Electromechanical Relay	10…100 pF
Digital Isolator	100…200 pF
Digital Isolator (int. SMPS)	300…600 pF
Transformers in SMPS	Up to 1000 pF

Capacitive Coupling

Effects

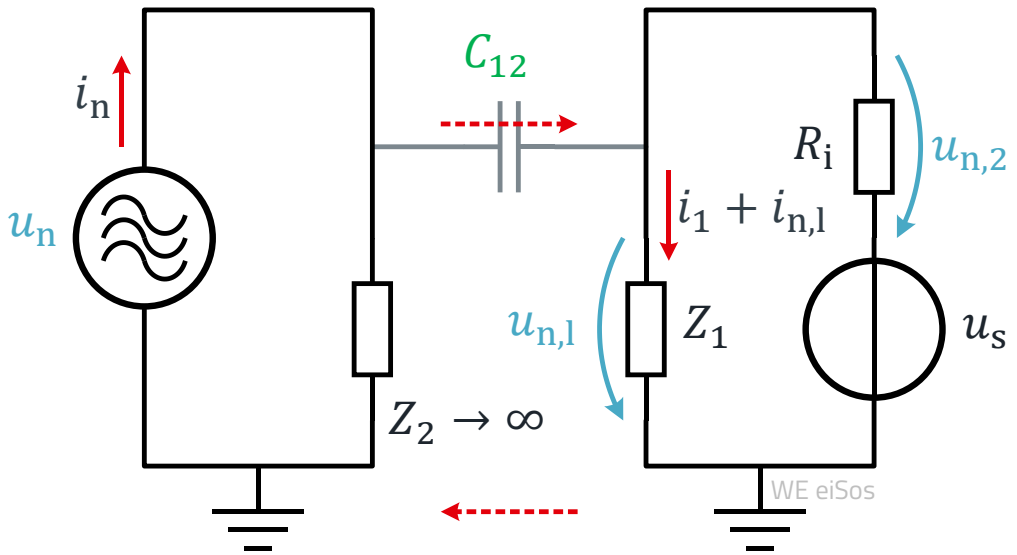
- Voltage interference at the load:

$$u_{\mathrm{n,l}} = i_{\mathrm{n}} \cdot \frac{R_{\mathrm{i}} \cdot Z_1}{R_{\mathrm{i}} + Z_1} = C_{12} \cdot \frac{\mathrm{d}u_{\mathrm{n}}}{\mathrm{d}t} \cdot \frac{R_{\mathrm{i}} \cdot Z_1}{R_{\mathrm{i}} + Z_1}$$

  - Laplace made easy: replace $\frac{\mathrm{d}}{\mathrm{d}t}$ by $j\omega$

$$U_{\mathrm{n,l}} = U_{\mathrm{n}} \cdot j\,\omega\, C_{12} \cdot \frac{R_{\mathrm{i}} \cdot Z_1}{R_{\mathrm{i}} + Z_1}$$

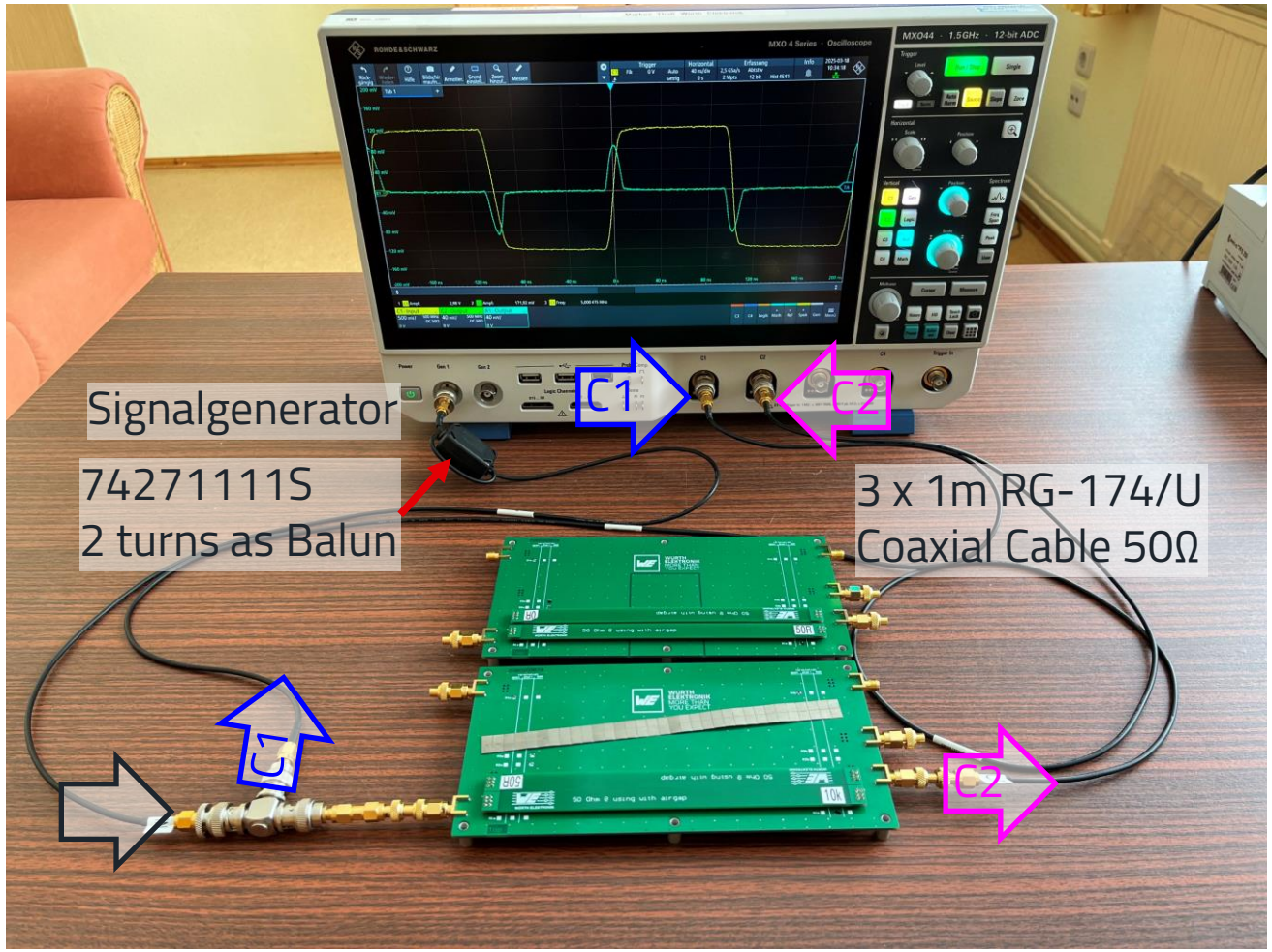
$$C_{12} = \varepsilon \cdot \frac{A}{d}$$



- Doubling the frequency doubles the crosstalk (+6 dB)
- Doubling the sink impedance (Ri||Z1) doubles the crosstalk

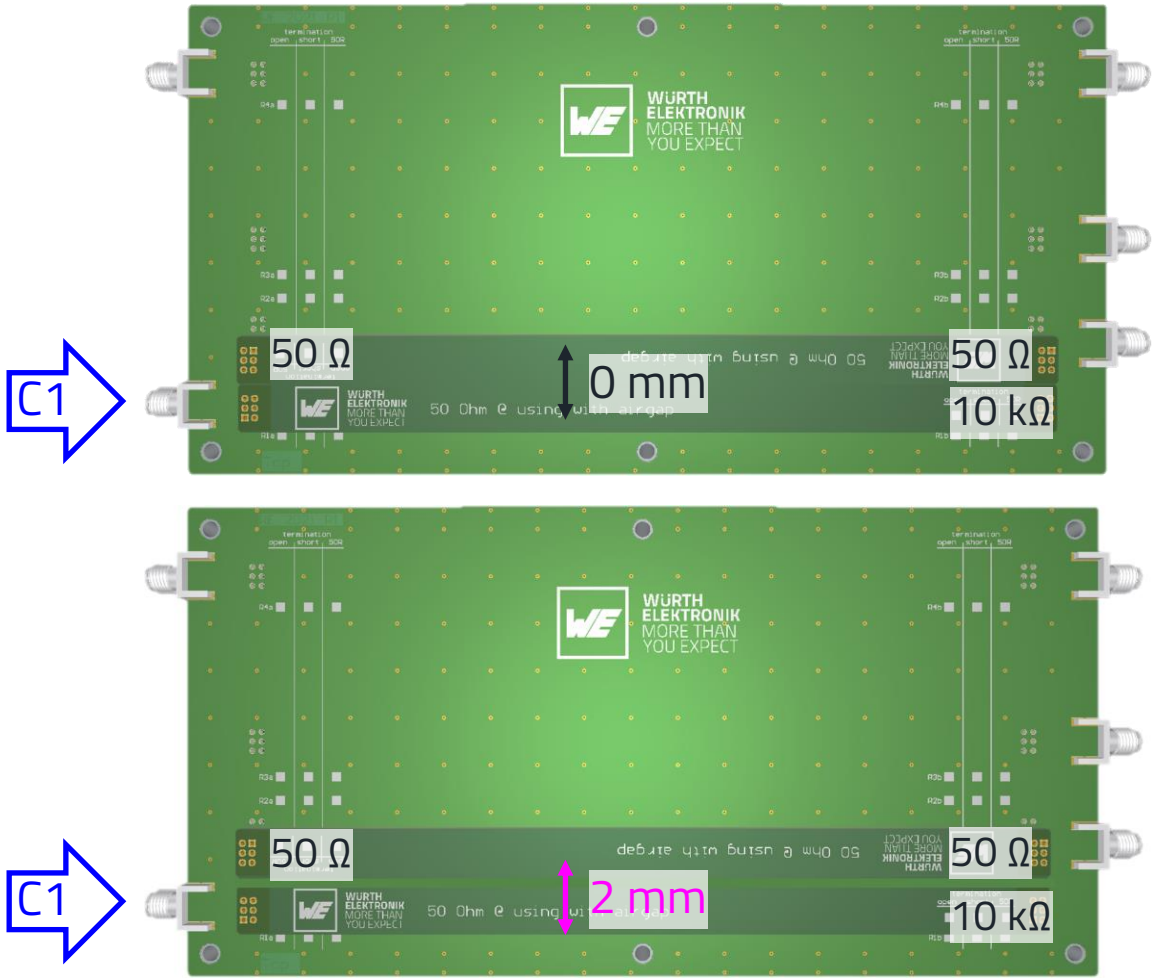
Coupling experiment

Testsetup



Capacitive Coupling

Experiment - 10 kΩ load resistance - 0 / 2 mm distance

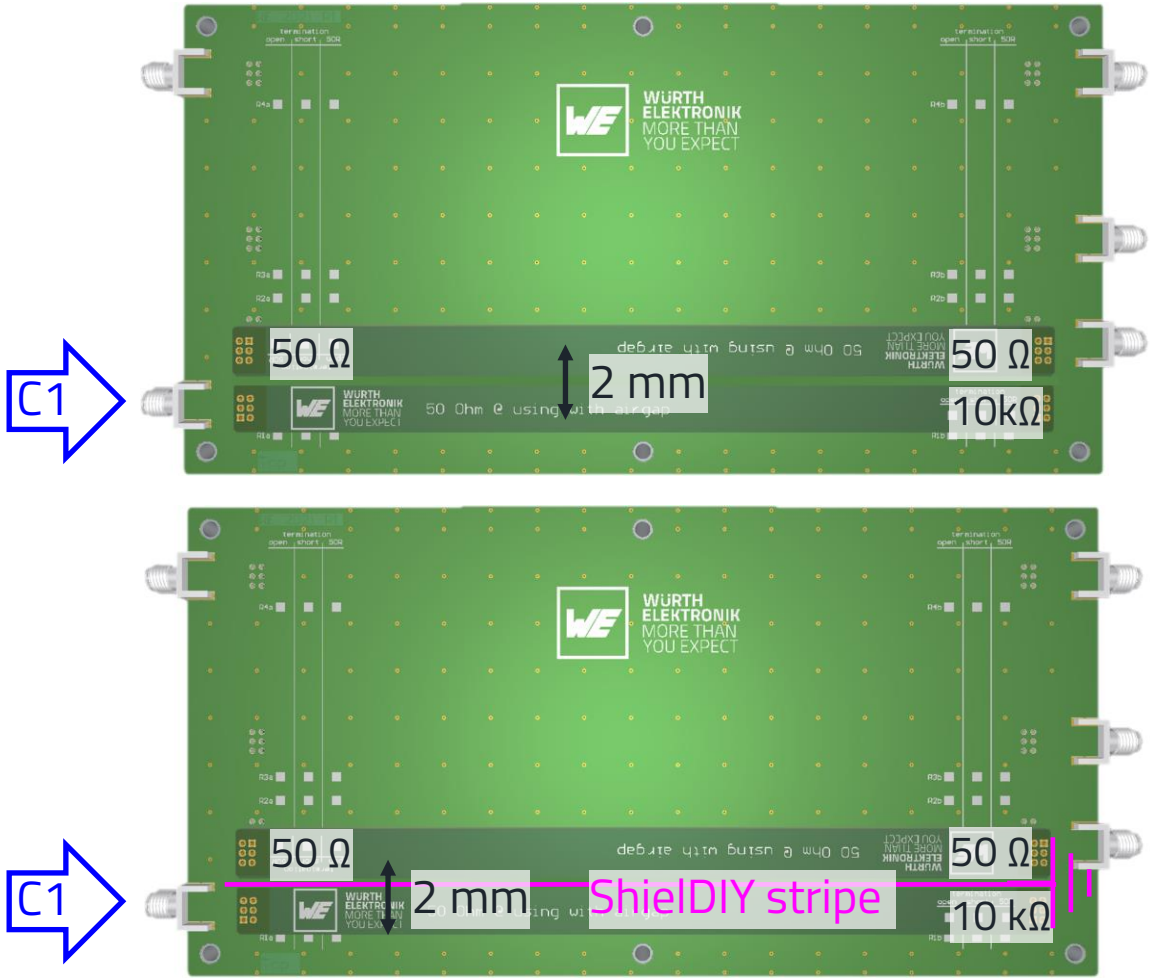


Input: Square wave / 3 Vpp / 5 MHz

- Crosstalk decreases with C12 (increased distance)

Capacitive Coupling

Experiment - 10 kΩ load resistance - 2 mm distance - grounded ShielDIY stripe (one side)



R1

C2

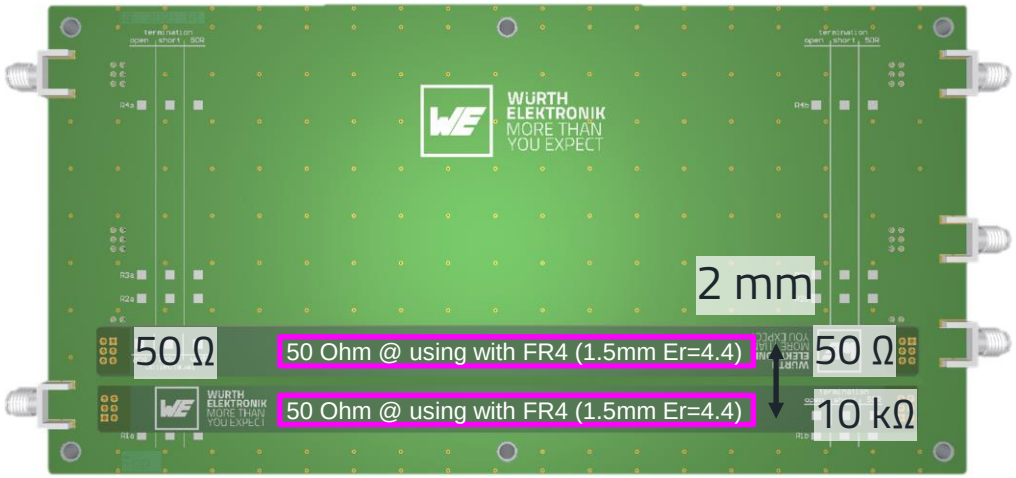
Input: Square wave / 3 Vpp / 5 MHz

- E-field can be easily shielded using a shield plate grounded on one side

Capacitive Coupling

Experiment - 10 kΩ load resistance - 2 mm distance - capacitance to the GND plane

C1



C1

R1

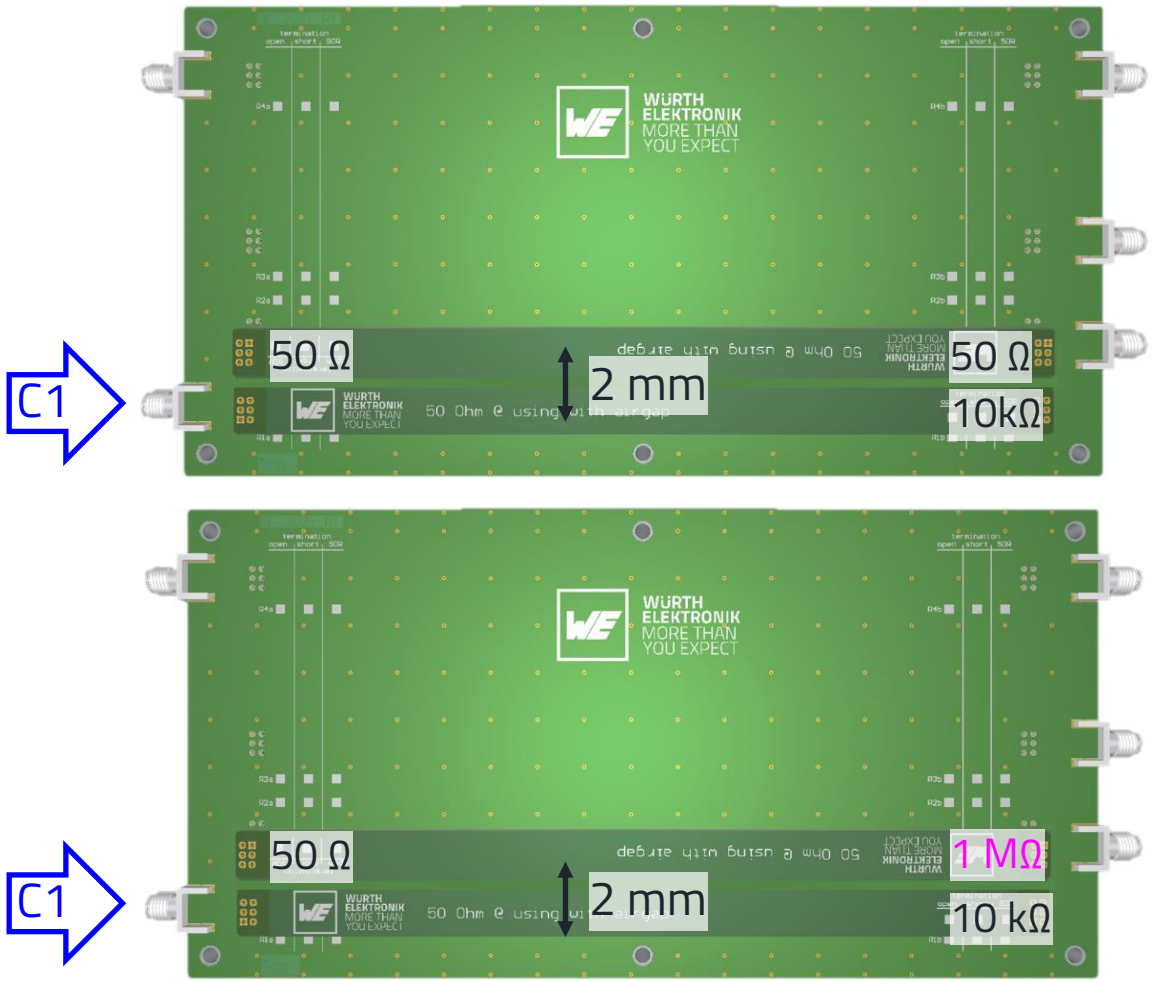
C2

Input: Square wave / 3 Vpp / 5 MHz

- Increasing the capacitance to the GND plane minimizes crosstalk

Capacitive Coupling

Experiment - 10 kΩ load resistance - 2 mm distance - 1 MΩ far end termination



R1

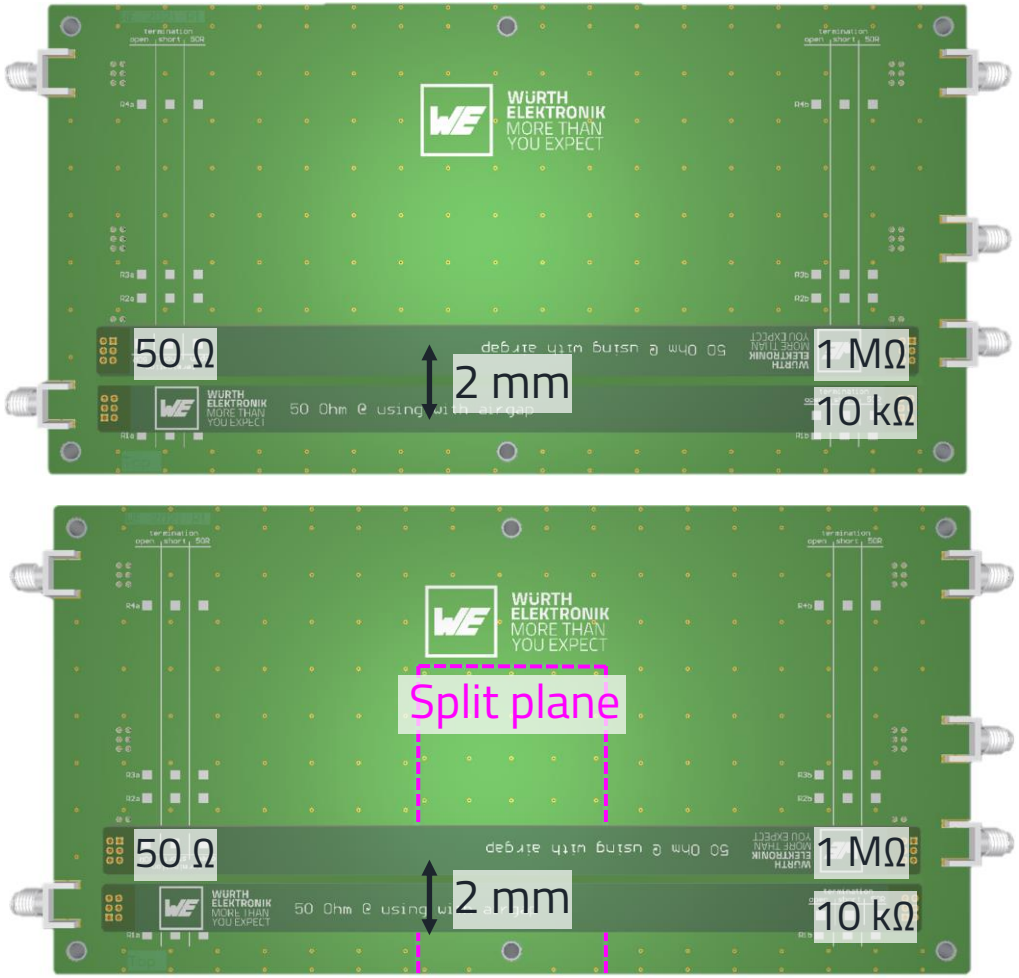
C2

Input: Square wave / 3 Vpp / 5 MHz

➢ Doubling the sink impedance (Ri||Z1) doubles the crosstalk

Capacitive Coupling

Experiment - 10kΩ load resistance - 2 mm distance - 1 MΩ Far end termination - Split plane



Input: Square wave / 3 Vpp / 5 MHz

- More parasitic coupling capacitance due GND-split

Capacitive Coupling

Measures to decrease coupling

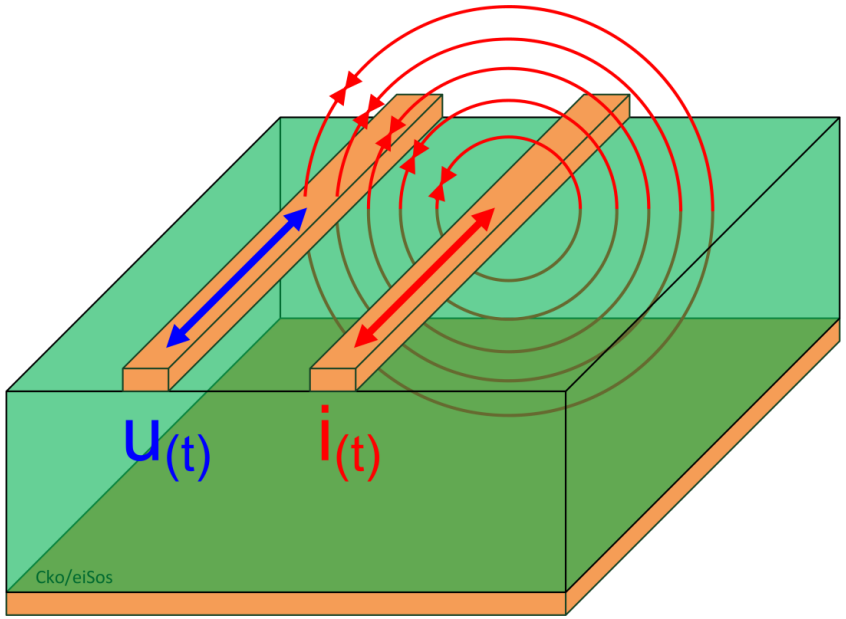
- **Primary Measure**
  - Decrease dU/dt by selecting a slower signal edges
  - A Low pass filter to take off the edges

- **Secondary Measure**
  - Shorten/avoid parallel trace runs
  - Small areas for switched polygons (e.g. DC/DC switch node)
  - Increase distance between affected paths
  - Electrical shielding (Cable, PCB, Housing)

Inductive Coupling

Origins

- Originates from high dI/dt
- Parallel traces form a parasitic transformer
- Mutual Inductance increases with shorter distance



Inductive Coupling

Effects

- Voltage interference at the load (Z1 = Near End):

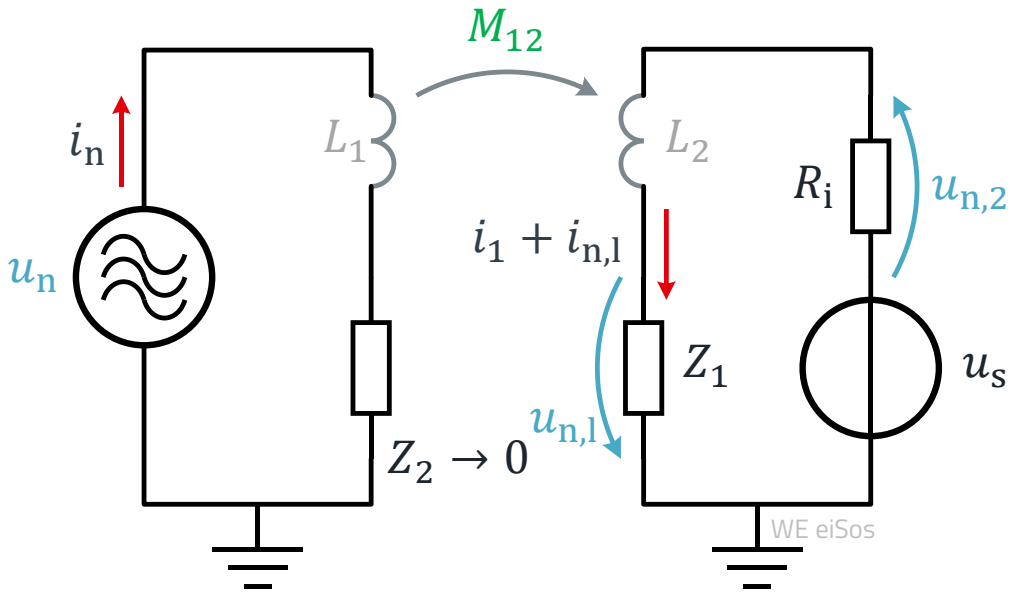
$$u_{\mathrm{n,l}} = M_{12} \cdot \frac{\mathrm{d}i_{\mathrm{n}}}{\mathrm{d}t} \cdot \frac{Z_1}{R_{\mathrm{i}} + Z_1}$$

  - Lapace made easy: replace $\frac{\mathrm{d}}{\mathrm{d}t}$ by $j\,\omega$

$$U_{\mathrm{n,l}} = I_{\mathrm{n}} \cdot j\,\omega\,M_{12} \cdot \frac{Z_1}{R_{\mathrm{i}} + Z_1}$$

$$M_{12} = \mu \cdot N_1 N_2 \cdot \frac{A}{l}$$

- Doubling the frequency doubles the crosstalk (+6 dB)
- Crosstalk increases with inductive loop dimensions

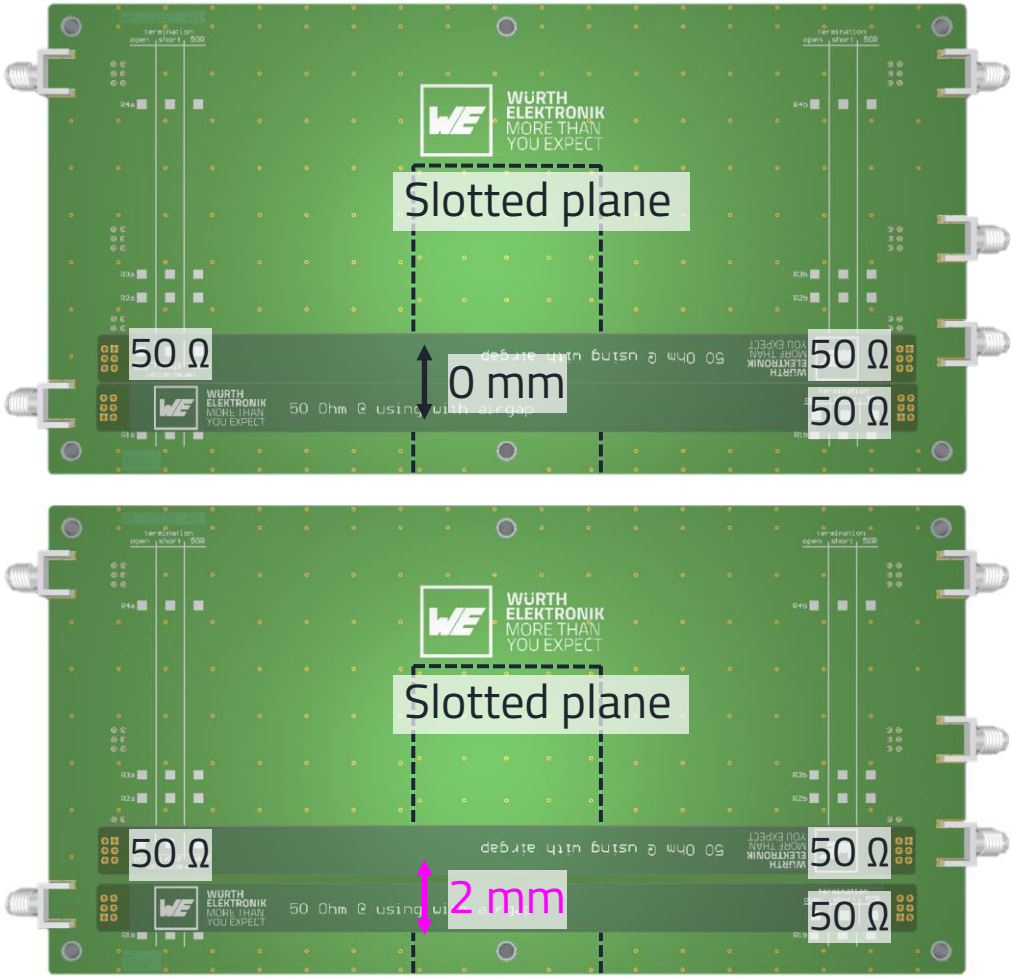


- Phase reversal of the induced current can be observed at the far end
- Voltage interference at the source (Ri = Far End):

$$U_{\mathrm{n,2}} = -I_{\mathrm{n}} \cdot j\,\omega\,M_{12} \cdot \frac{R_{\mathrm{i}}}{R_{\mathrm{i}} + Z_1}$$

Inductive (dominant) vs. Capacitive Coupling

Experiment - 50 Ω load resistance - slotted plane - 0 / 2 mm distance



R1

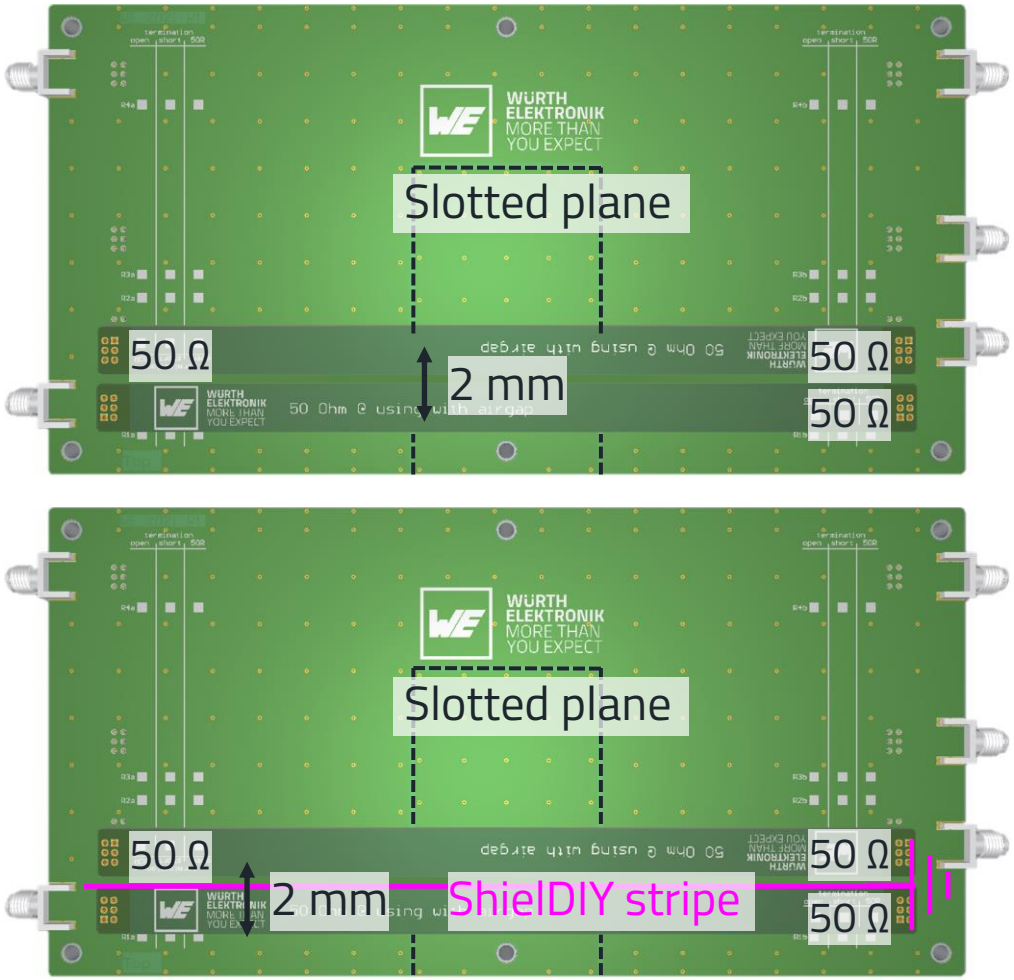
C2

Input: Square wave / 3 Vpp / 5 MHz

- Capacitive coupling counteracts the inductive coupling at the far end (inductive coupling dominates)

Inductive (dominant) vs. Capacitive Coupling

Experiment - 50 Ω load resistance - 2 mm distance - slotted plane - grounded ShielDIY stripe (one side)



R1

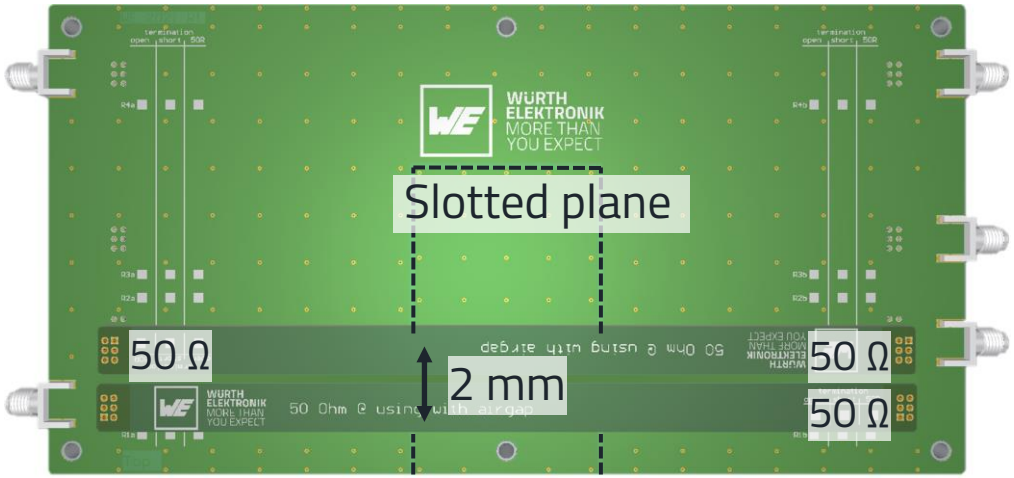
C2

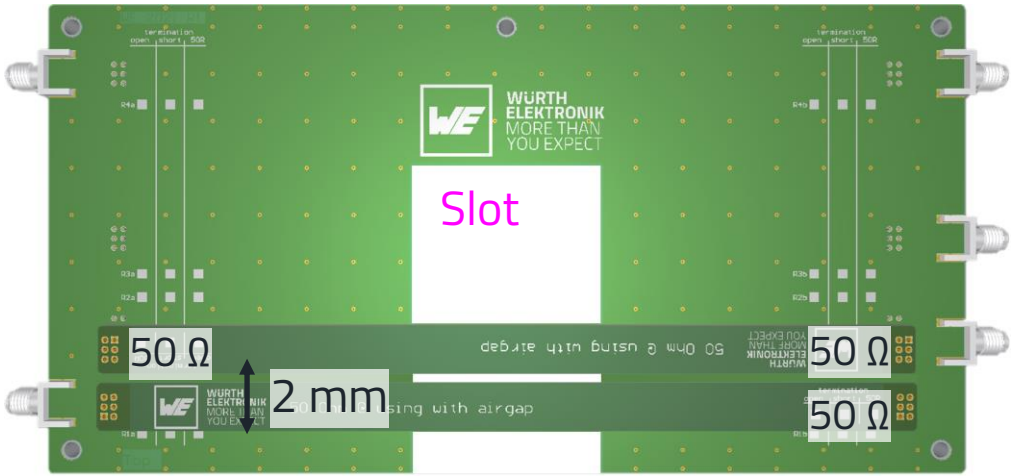
Input: Square wave / 3 Vpp / 5 MHz

- Capacitive coupling counteracts the inductive coupling at the far end
  - less capacitive coupling (shielded) → more overall crosstalk

Inductive (dominant) vs. Capacitive Coupling

Experiment - 50 Ω load resistance - 2 mm distance - slotted plane vs. slot

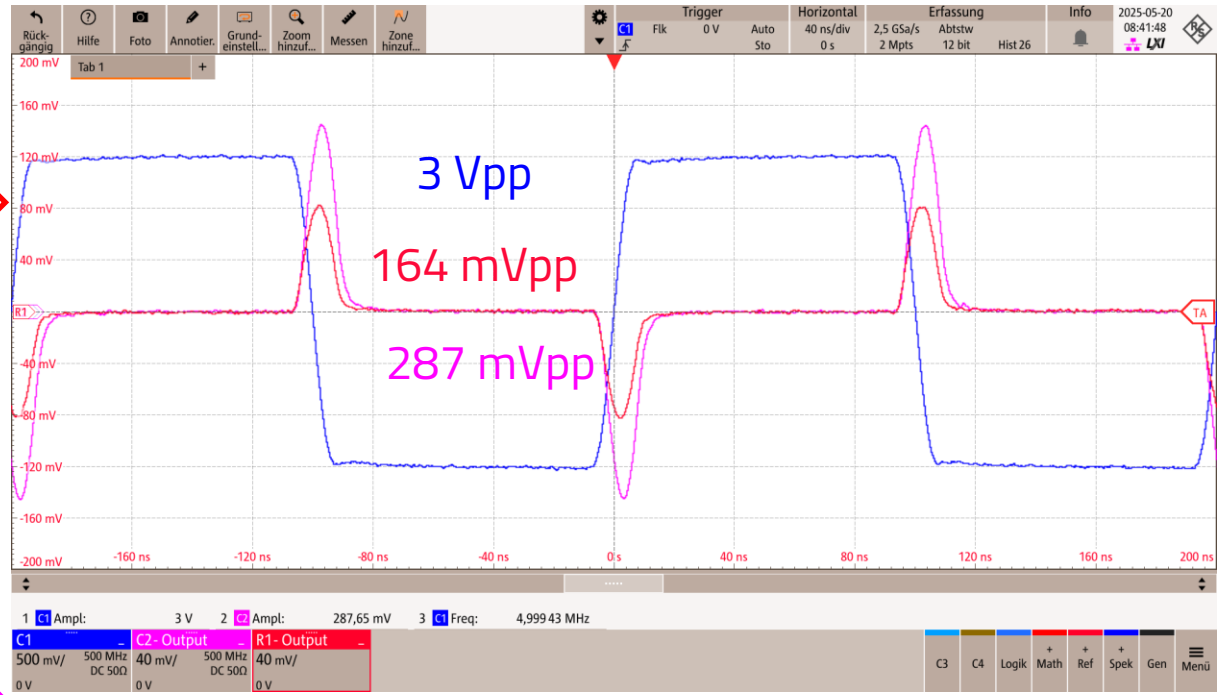




R1

C2

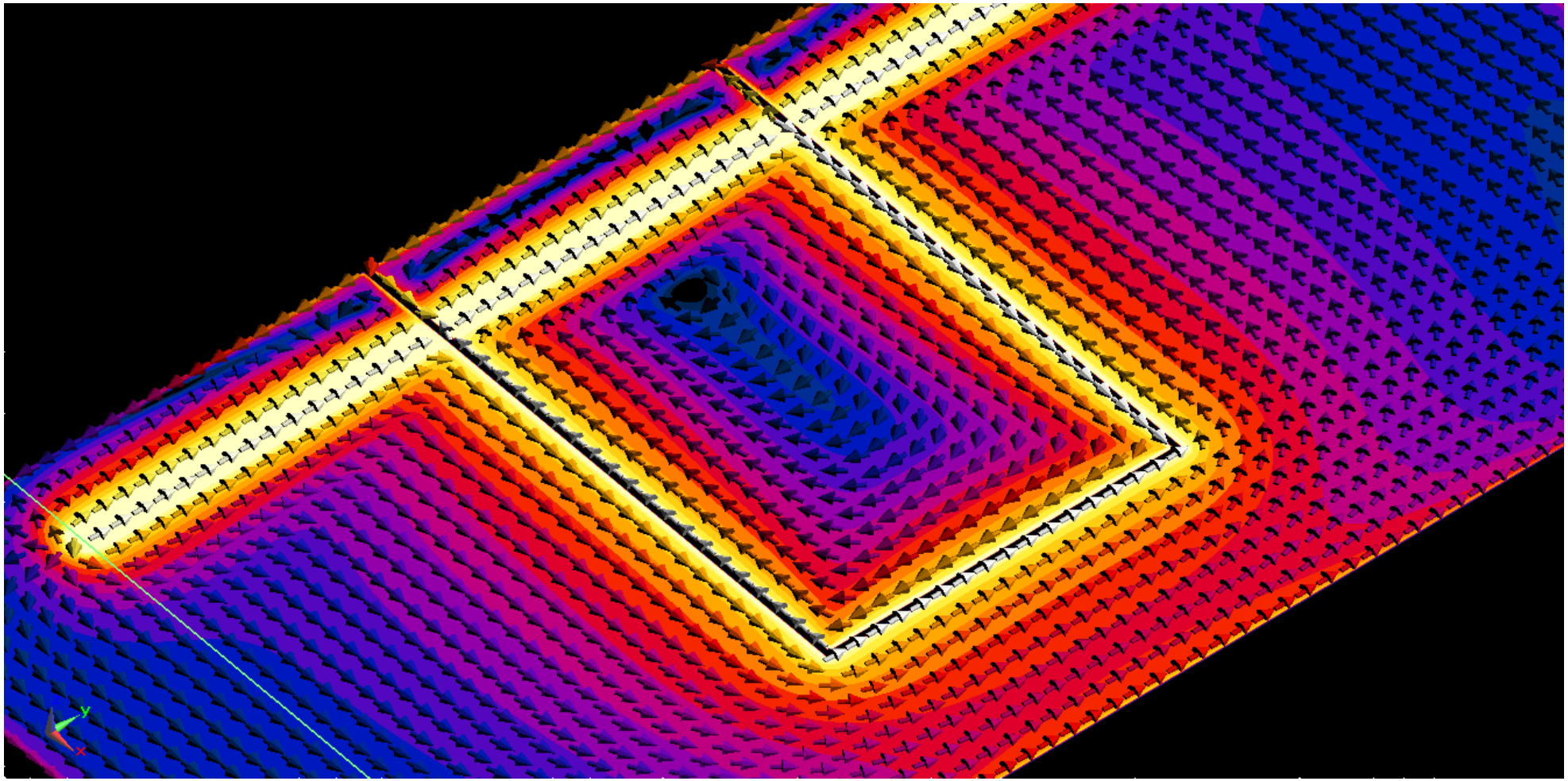
Input: Square wave / 3 Vpp / 5 MHz



- Countercurrent in the slotted floating plane compensates the effect of inductive coupling

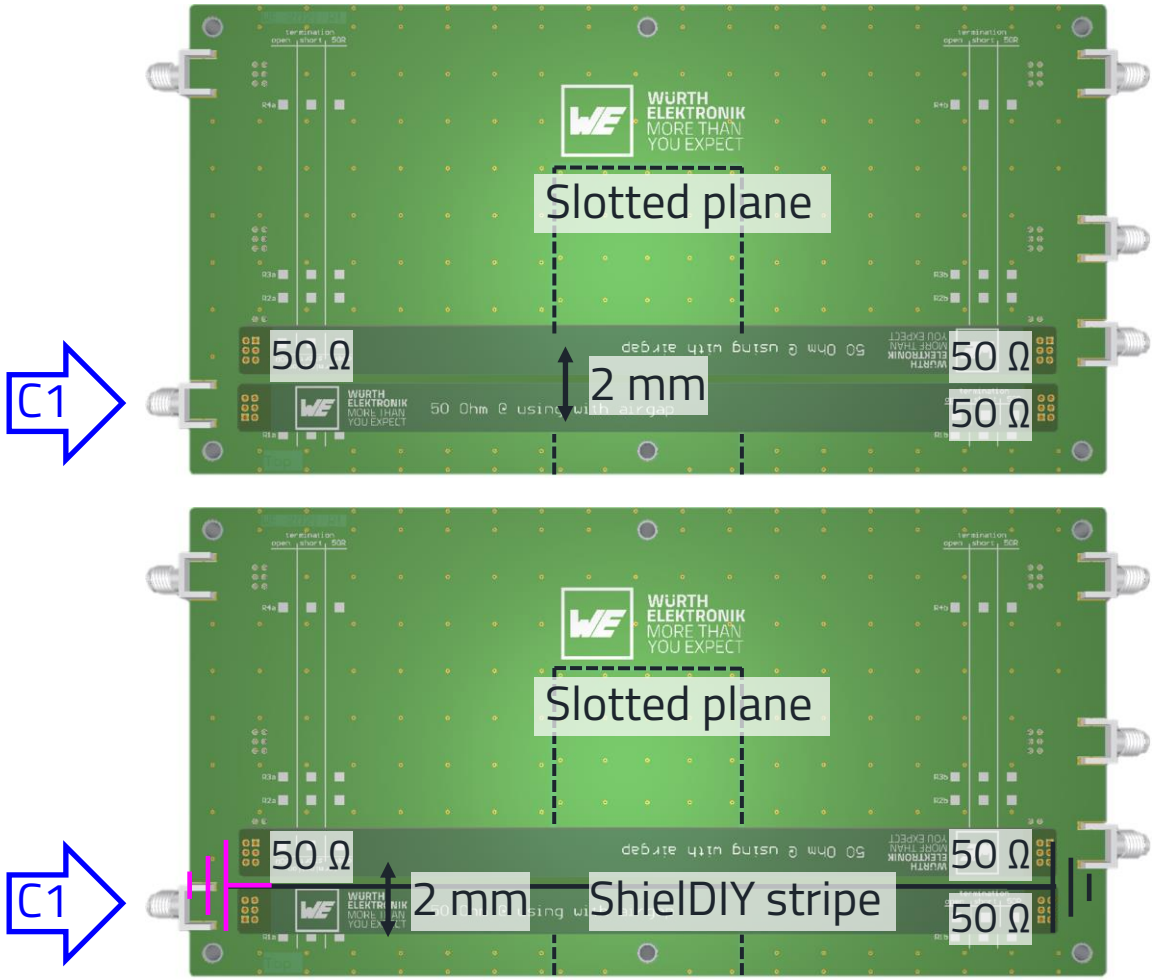
Inductive Coupling

Simulation: Return Path on slotted GND plane



Inductive Coupling

Experiment - 50 Ω load resistance - 2 mm distance - slotted plane - grounded ShielDIY stripe (both sides)



R1

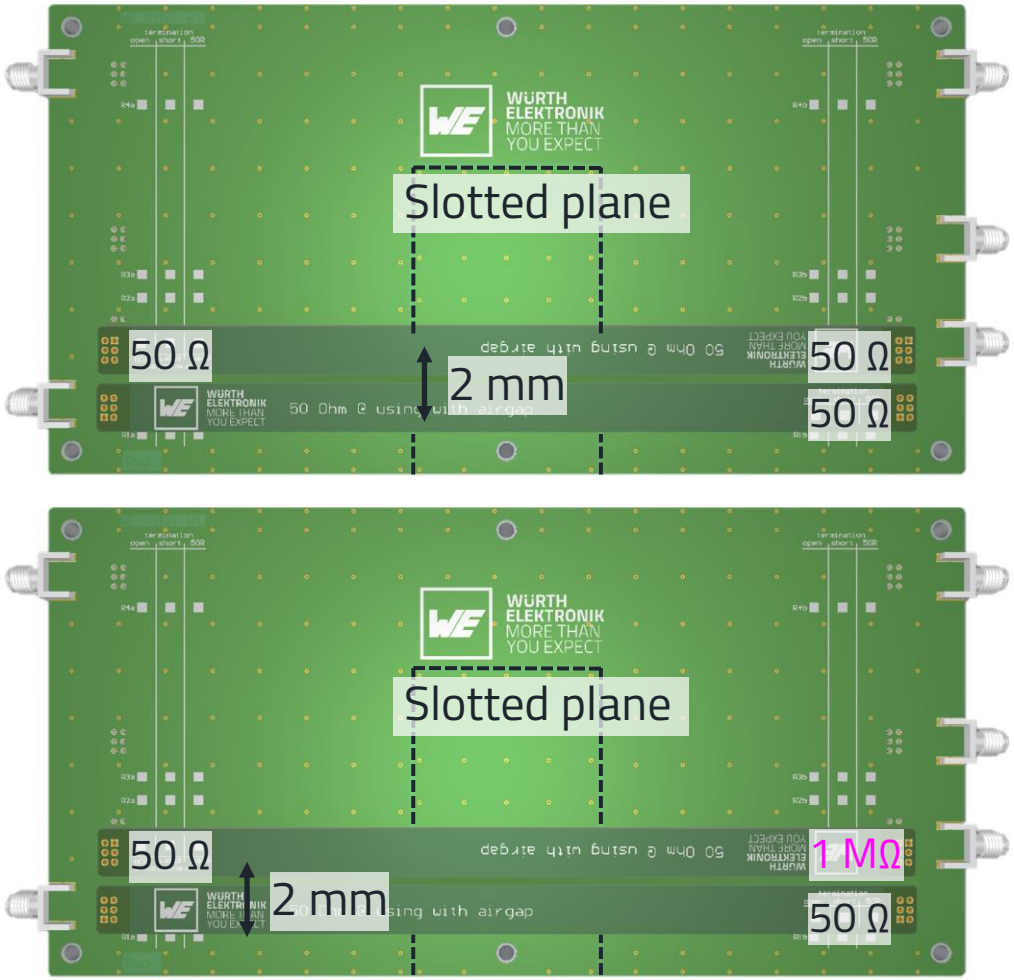
C2

Input: Square wave / 3 Vpp / 5 MHz

- Short return path over ShielDIY stripe (E-Field + H-Field shielding)
  - less inductive coupling, but still some coupling due vertical loops

Inductive Coupling

Experiment - 10 kΩ load resistance - 2 mm distance – slotted plane - 1 MΩ far end termination



R1

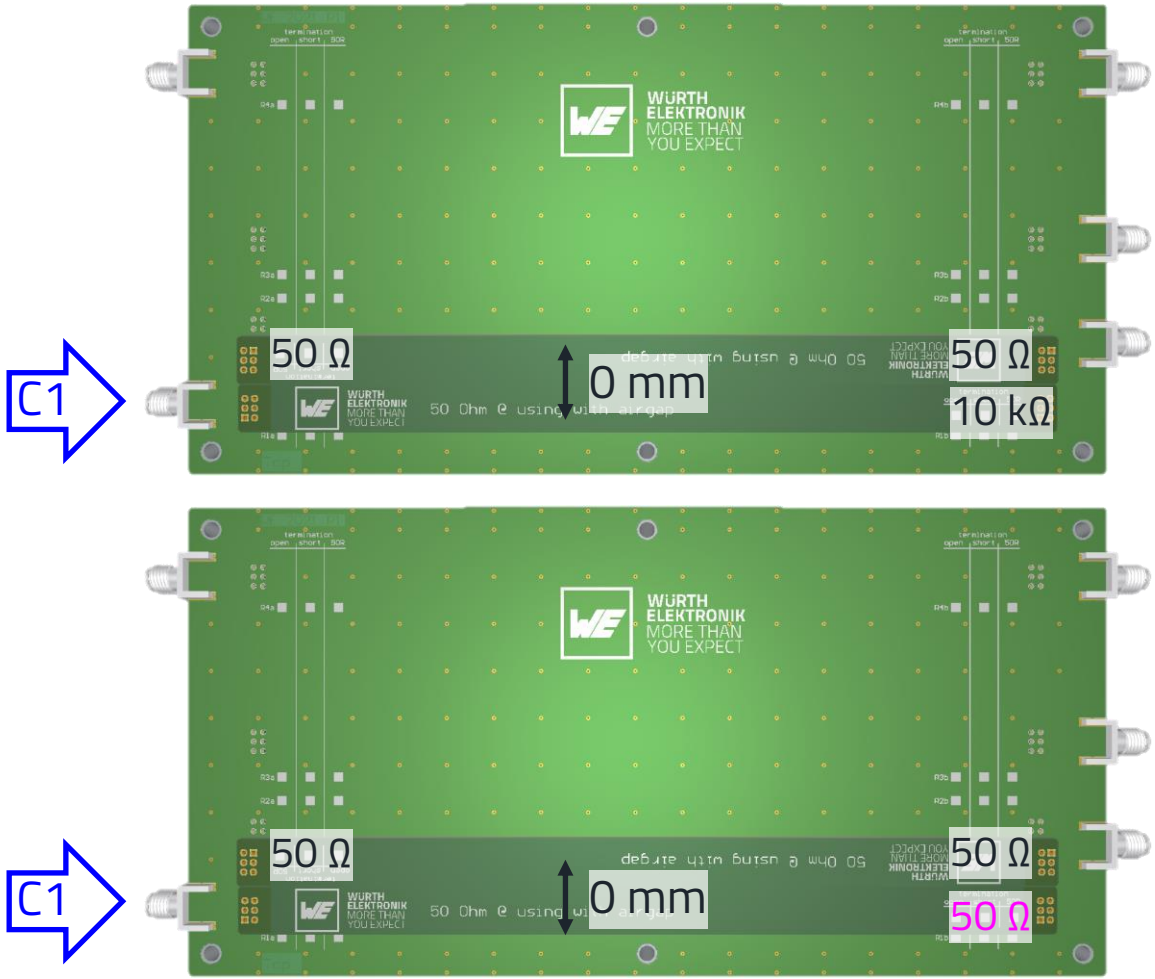
C2

Input: Square wave / 3 Vpp / 5 MHz

- With a one side high-impedance termination of the affected circuit, the open load voltage of the parasitic transformer is obtained

Inductive vs. Capacitive Coupling (dominant)

Experiment - 10 kΩ / 50 Ω load resistance - 0 mm distance

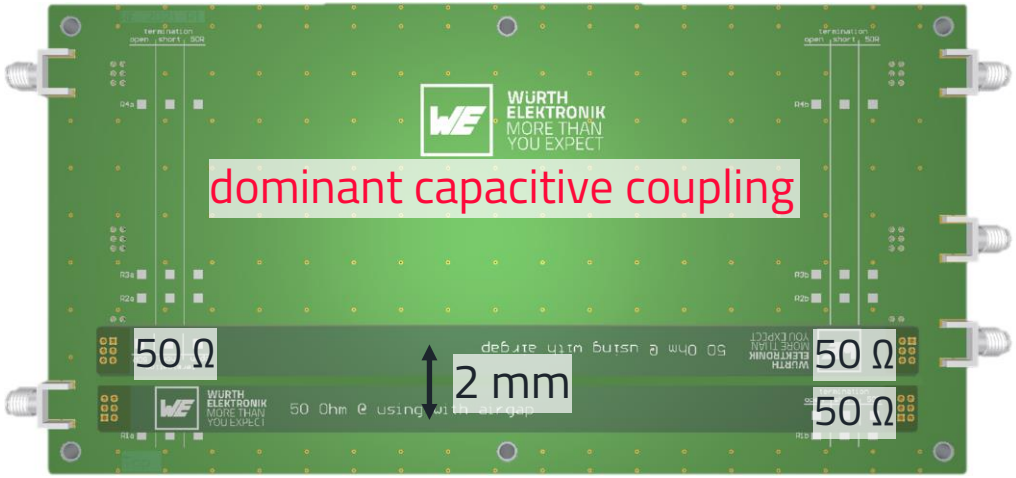


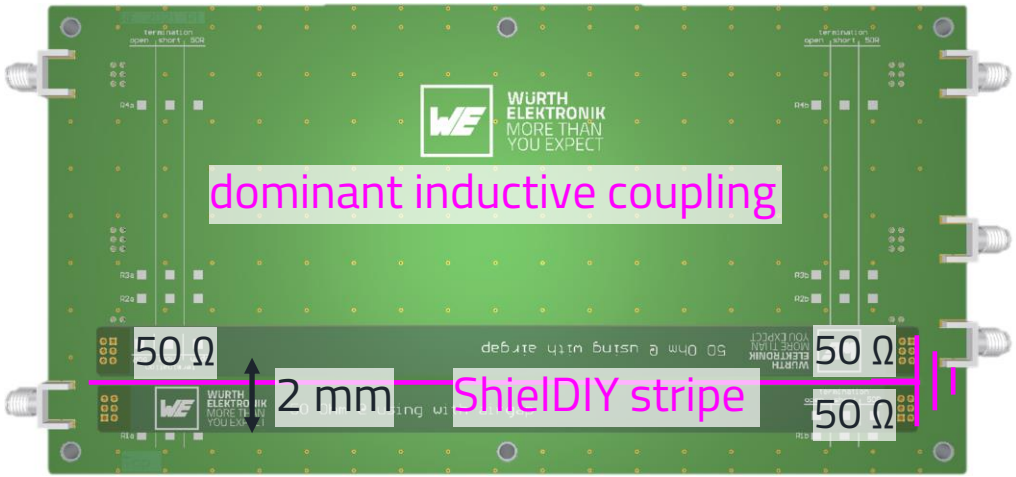
Input: Square wave / 3 Vpp / 5 MHz

- Inductive coupling (due 50 Ω load) counteracts the capacitive coupling at the far end (capacitive coupling dominates)

Capacitive vs. Inductive Coupling

Experiment - 50 Ω load resistance - 2 mm distance - grounded ShielDIY stripe (one side)

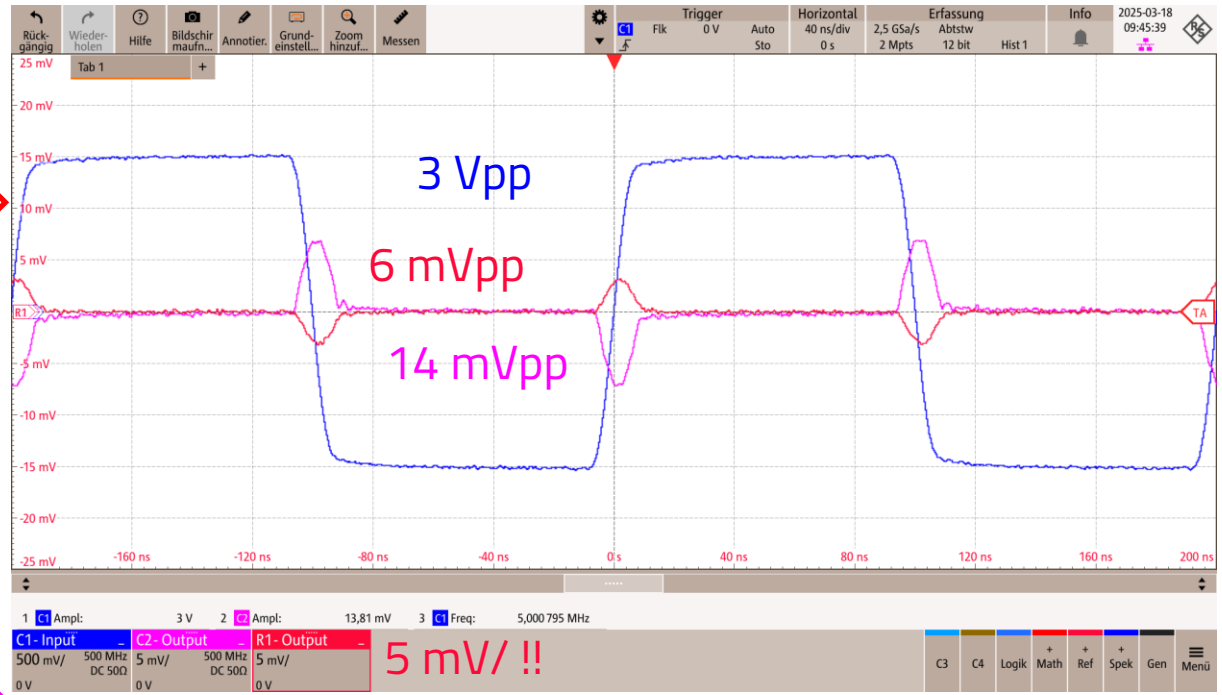




R1

C2

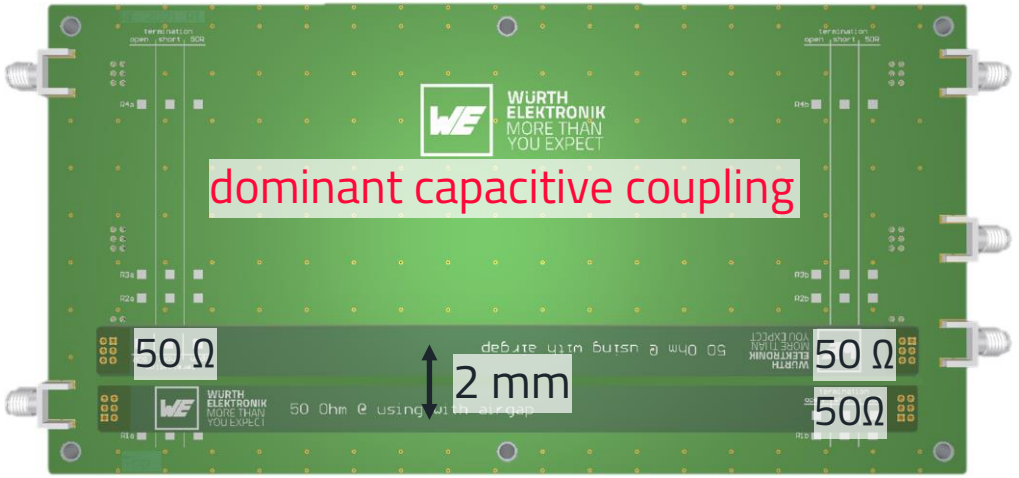
Input: Square wave / 3 Vpp / 5 MHz

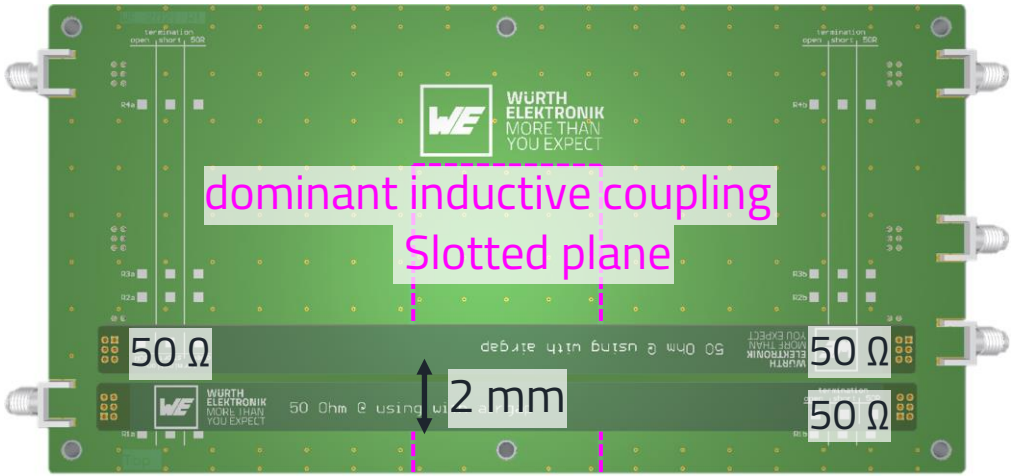


- Capacitive coupling counteracts the inductive coupling at the far end
  - capacitive coupling shielded → inductive coupling over vertical loops remains

Capacitive vs. Inductive Coupling

Experiment - 50 Ω load resistance - 2 mm distance - solid gnd-plane vs. slotted plane



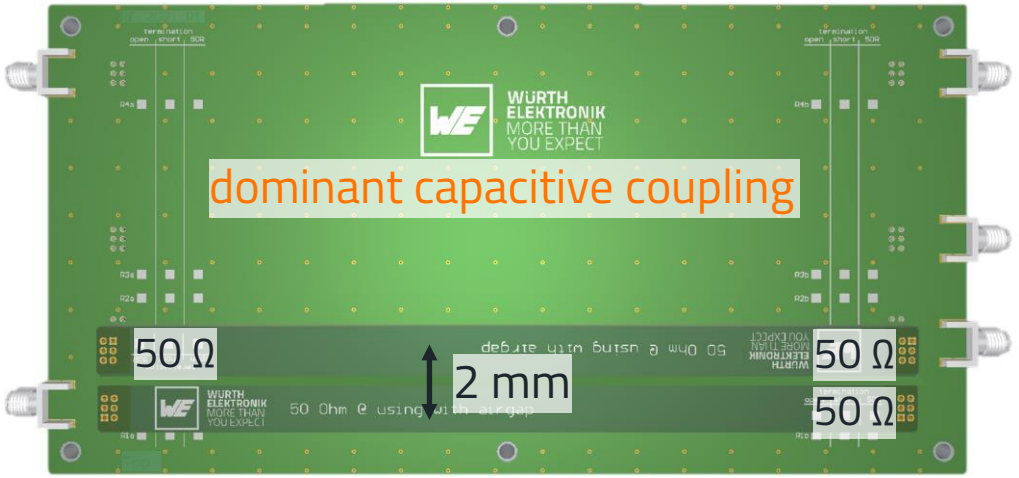


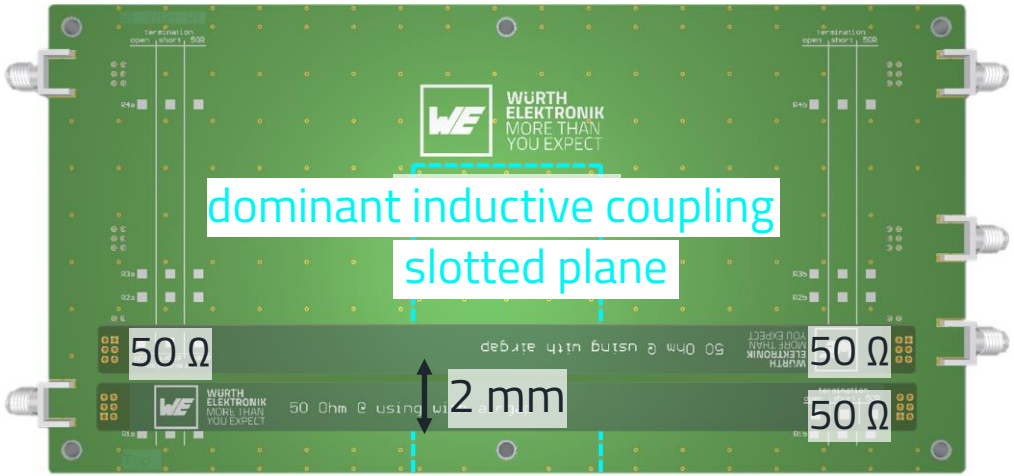
Input: Square wave / 3 Vpp / 5 MHz

- PCB with split plane (inductive coupling dominates) shows significantly more crosstalk (Factor 23)

Capacitive vs. Inductive Coupling

Experiment - 50 Ω load resistance - 2 mm distance - solid gnd-plane vs. slotted plane

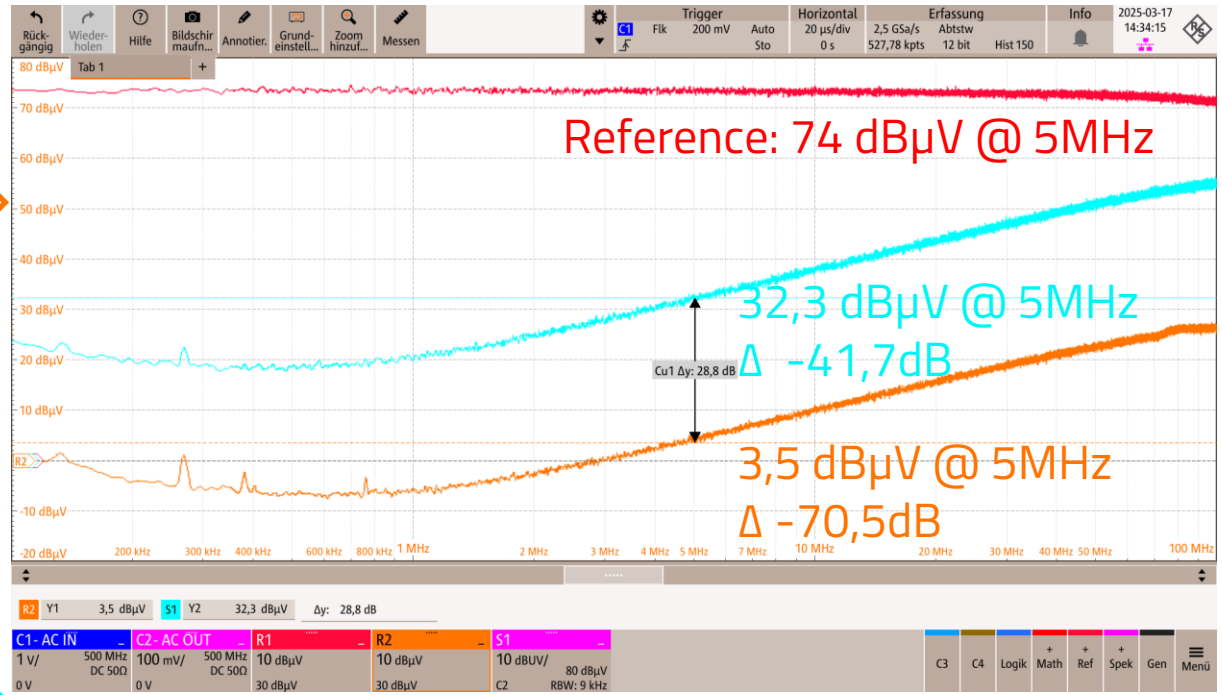




R1

S1

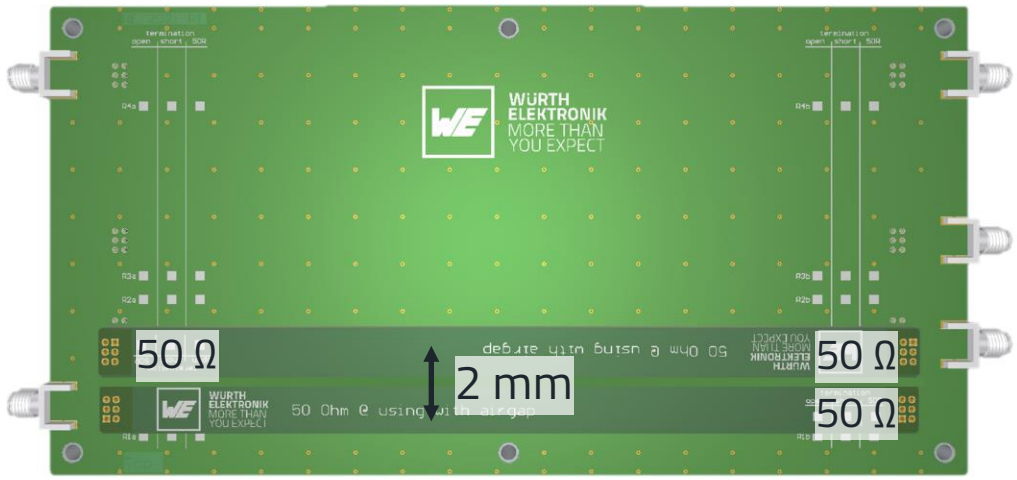
Input: Wideband Noise (74 dBµV)



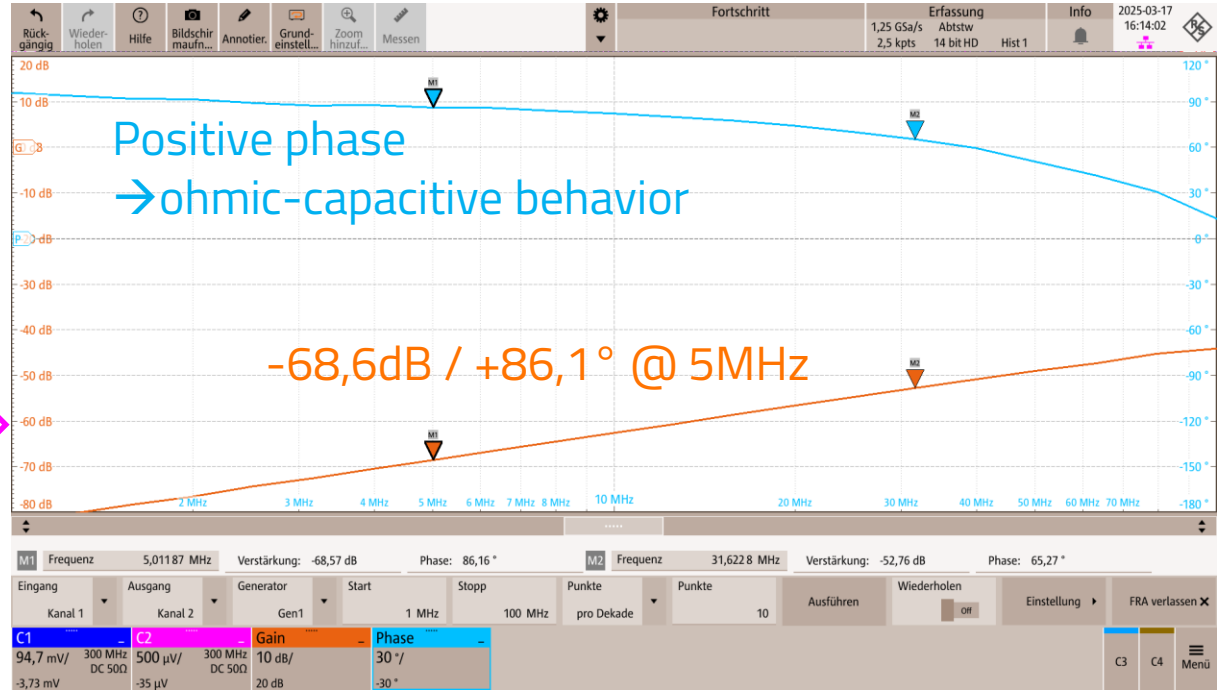
- PCB with split plane (inductive coupling dominates) shows 28,8dB (with noise measurement) or 27,2dB (with FRA) (Factor 27,5 or 22,9) more crosstalk

Capacitive Coupling (dominant)

Frequency response analysis (FRA) - 50 Ω load resistance - 2 mm distance – solid gnd plane



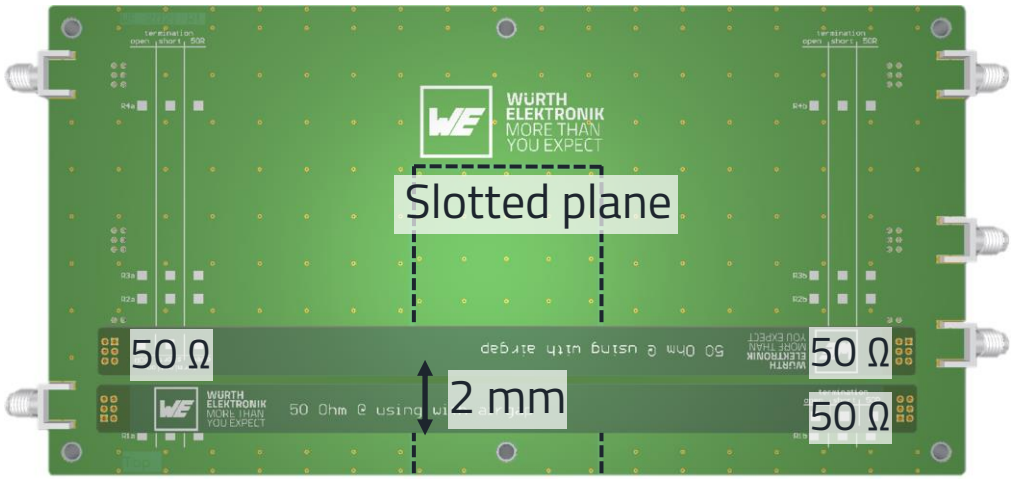
C2

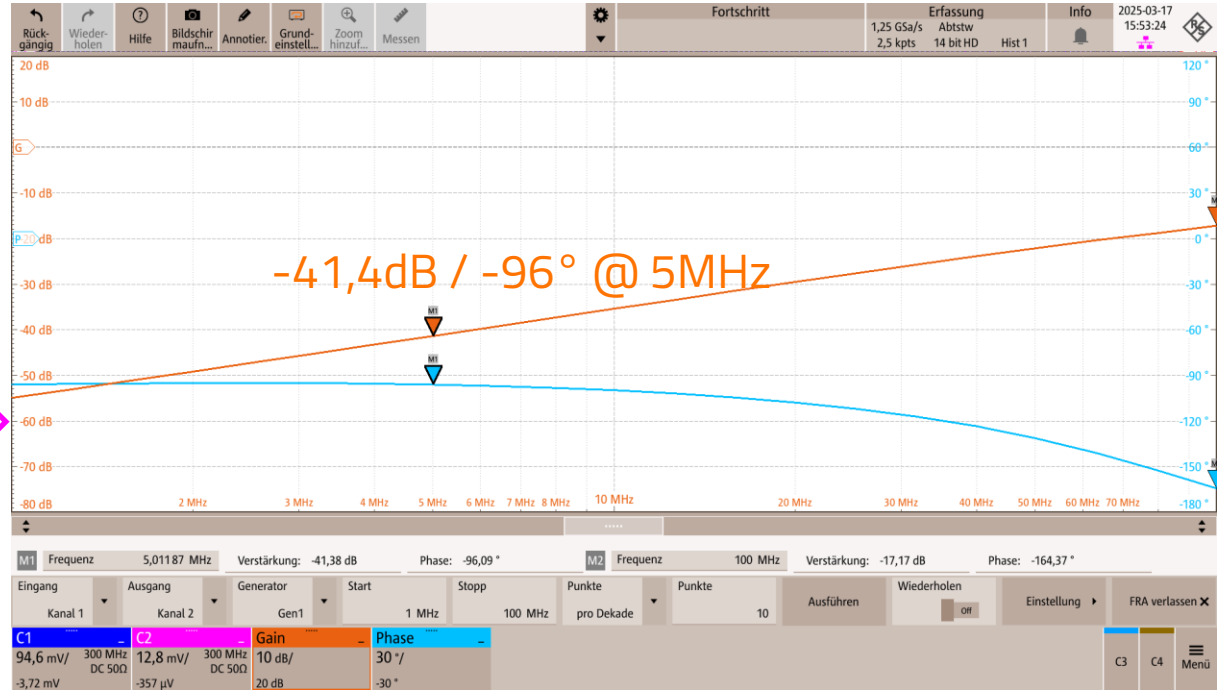


- Doubling the frequency doubles the crosstalk (+6 dB)
- In circuits with primarily capacitive loads, current leads the voltage (ideally +90 °)

Inductive Coupling (dominant)

Frequency response analysis (Frau) - 50 Ω load resistance - 2 mm distance - slotted plane





- Doubling the frequency doubles the crosstalk (+6 dB)
- phase at the far end differs from capacitive coupling (ideally -90°)

Inductive Coupling

Measures to decrease coupling

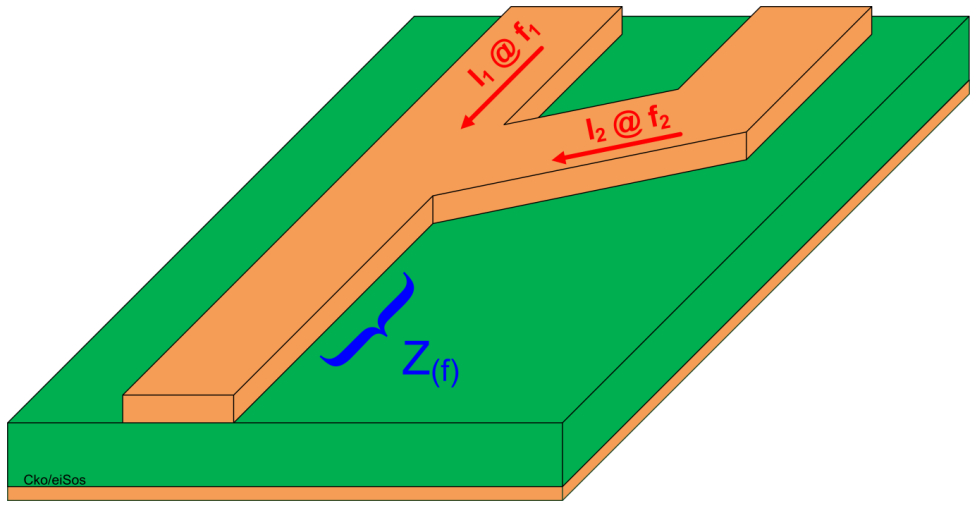
- **Primary Measure**
  - Decrease dI/dt by selecting a lower switching frequency and slower signal edges
  - A filter Inductor/Ferrite to take off the edges

- **Secondary Measure**
  - Decrease magnetic loop area
  - Increase distance between affected circuits
  - Orthogonal component placement
  - Magnetic shielding with ferrite materials (soft permeability, high μ_r)

Impedance Coupling

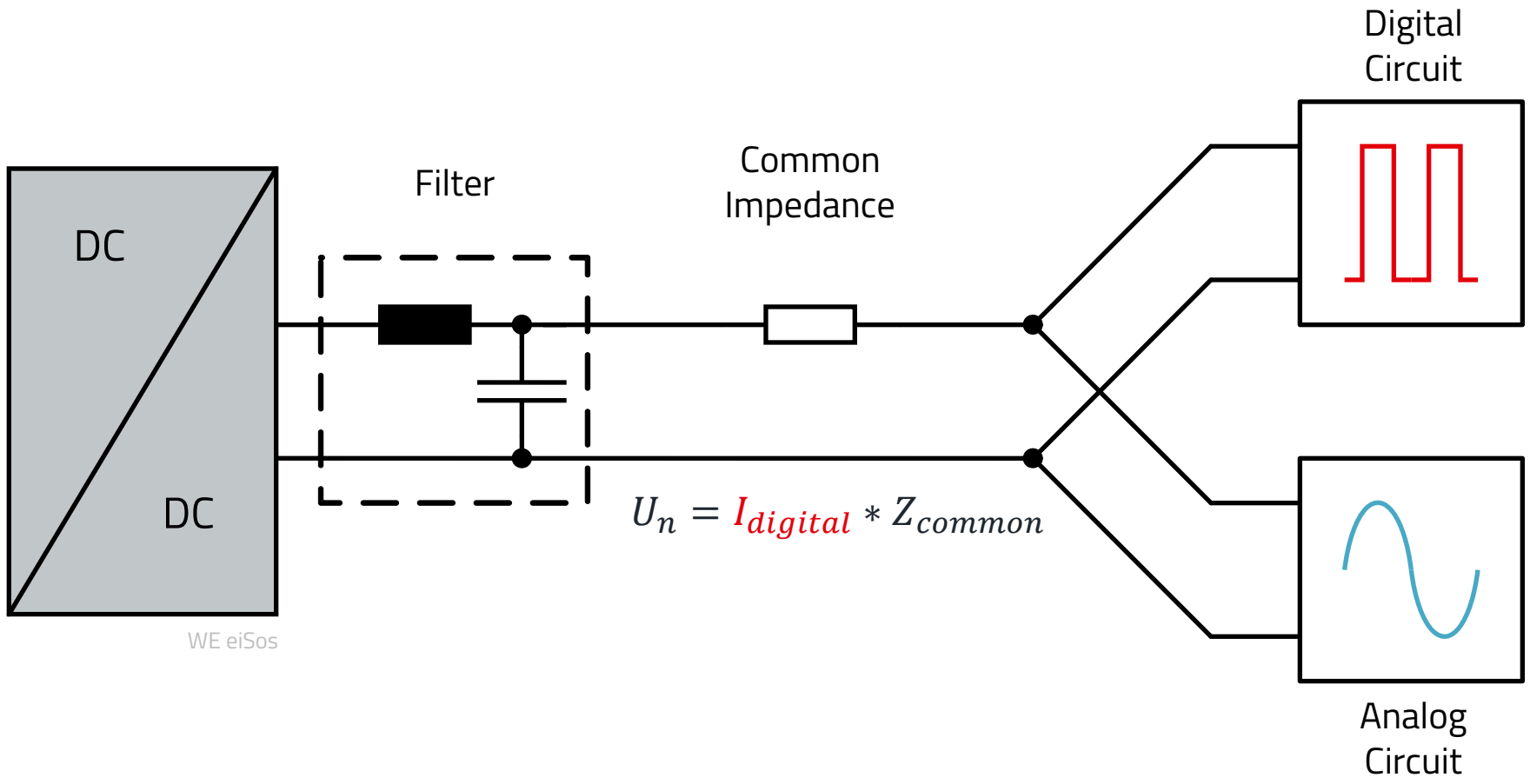
Origins

- Interference affects circuits with a mutual traces
- Circuits share an impedance and therefore the voltage across that impedance
- Main cause for high mutual impedances is self-inductance across copper traces

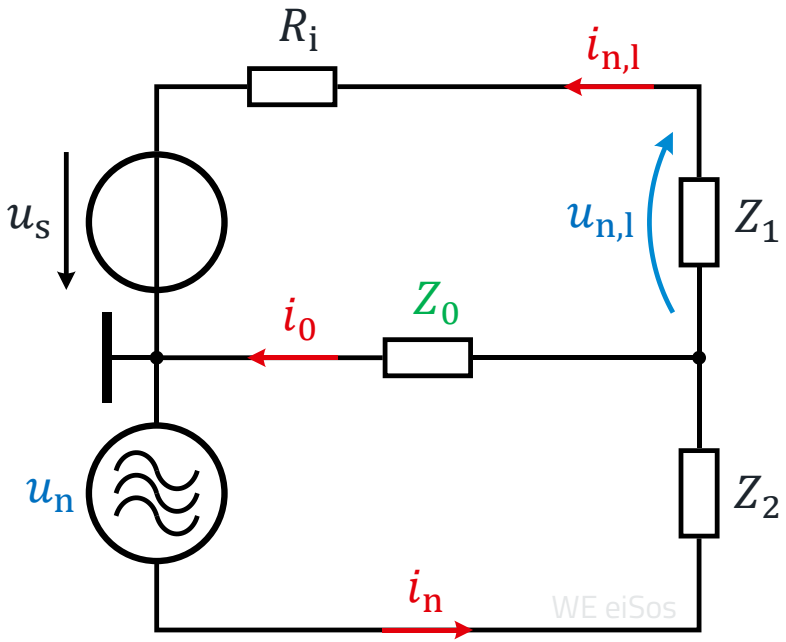


Impedance Coupling

A closer look



Impedance Coupling



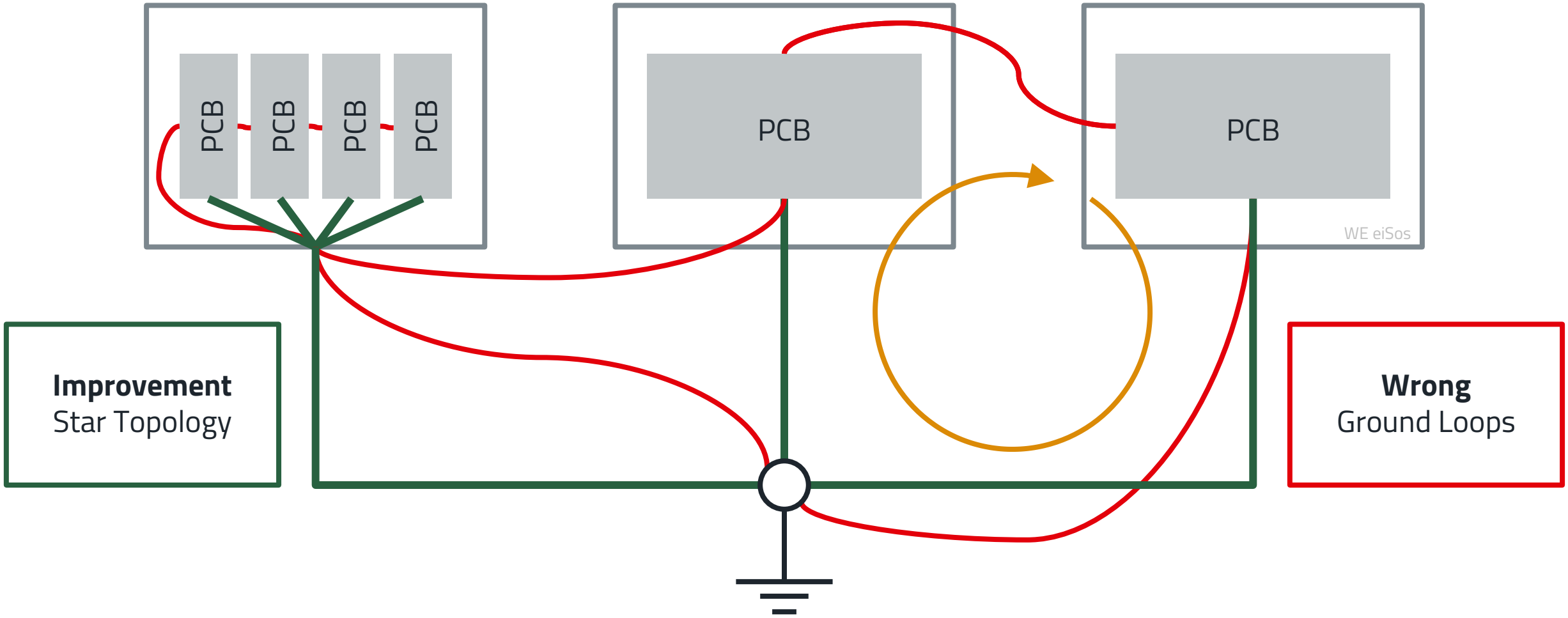
- Coupling impedance: $\underline{Z_0} = R_0 + \mathrm{j}\omega L_0$
- Interference voltage at the load:

$$u_{\mathrm{n,l}} = \frac{u_\mathrm{n}}{Z_2 + (R_\mathrm{i} + Z_1) \| Z_0} \cdot \frac{Z_1 \cdot Z_0}{R_\mathrm{i} + Z_1 + Z_0}$$

GROUND CONCEPT

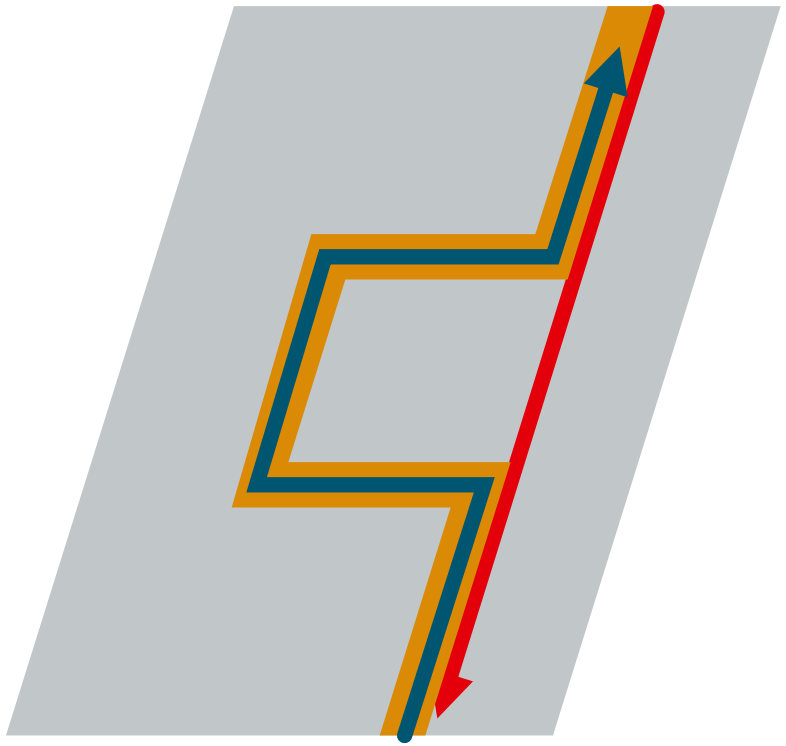
Ground Concept

Distribution across multiple PCBs

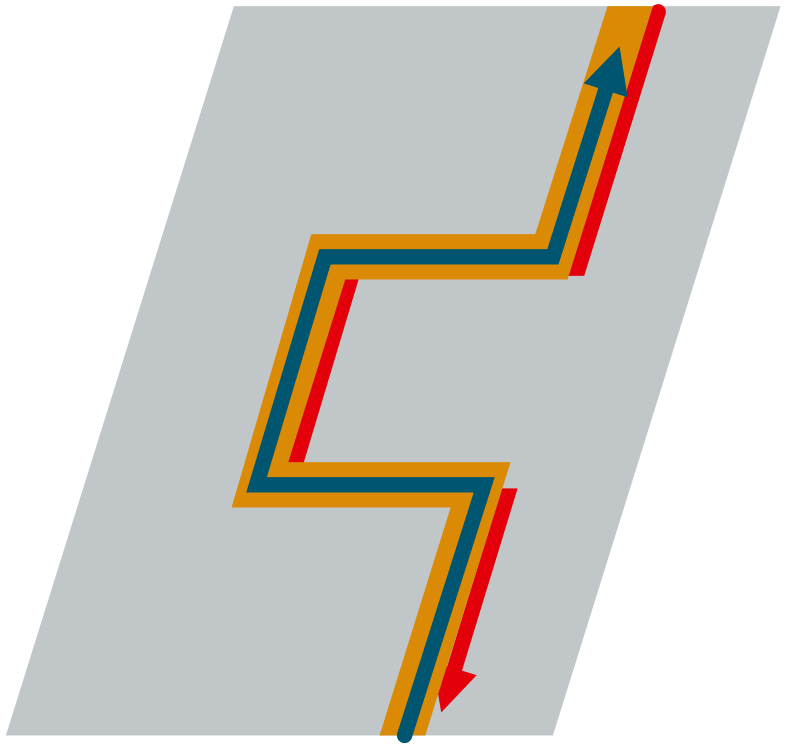


Path of least Impedance

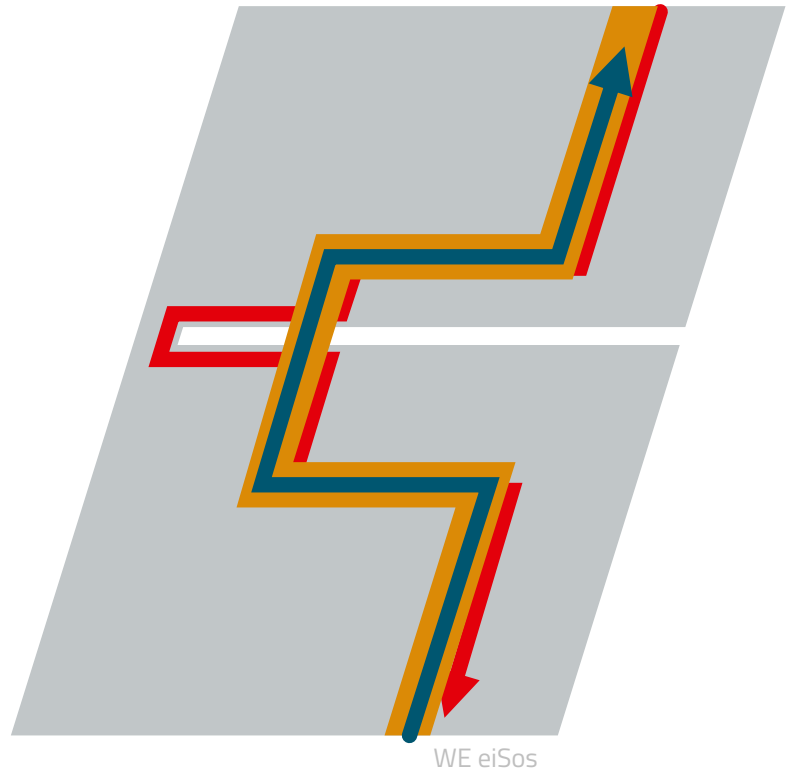
Return Path for AC and DC currents



DC Return Path



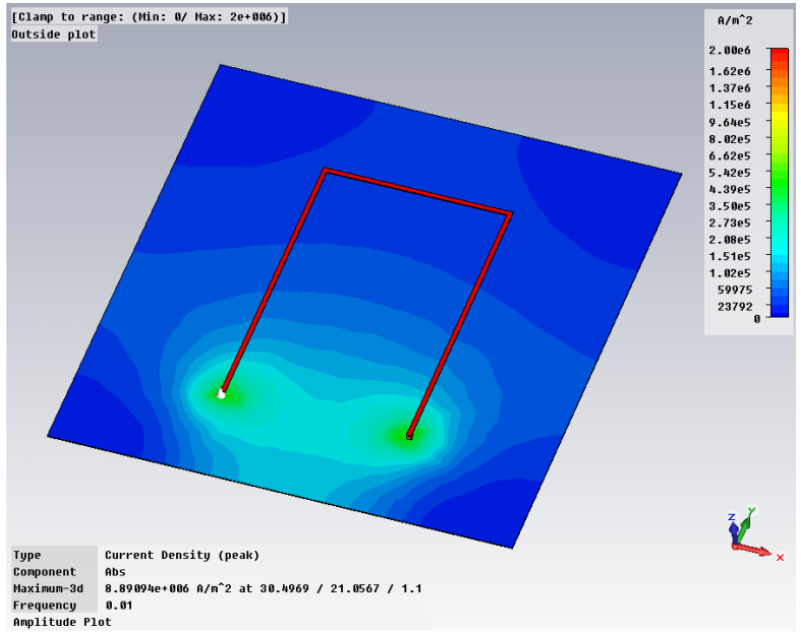
AC Return Path



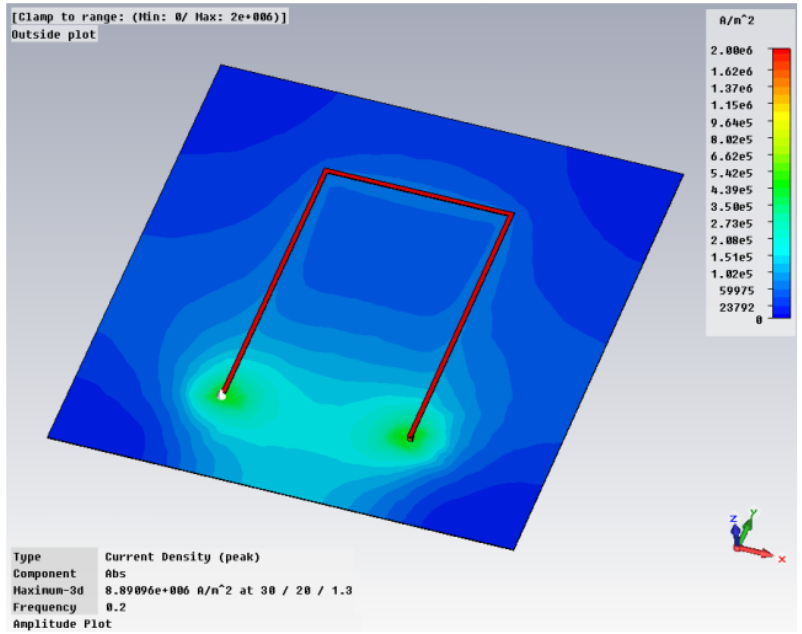
Slotted AC Return Path

Path of least Impedance

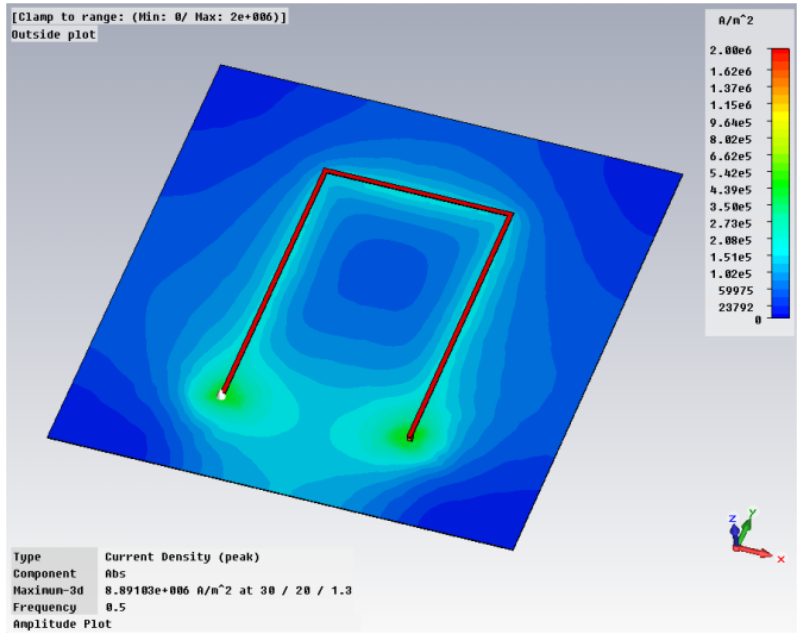
Simulation: Return Path depending on Frequency



10 Hz



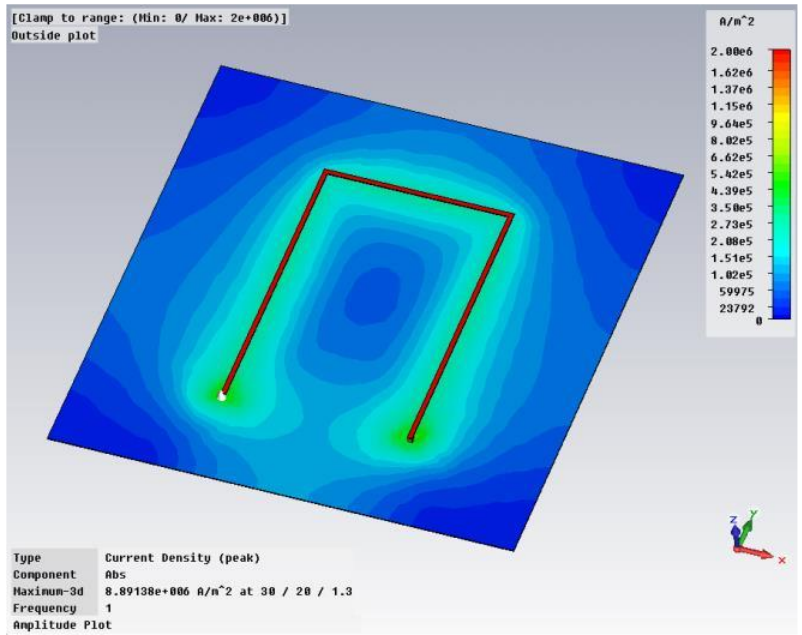
200 Hz



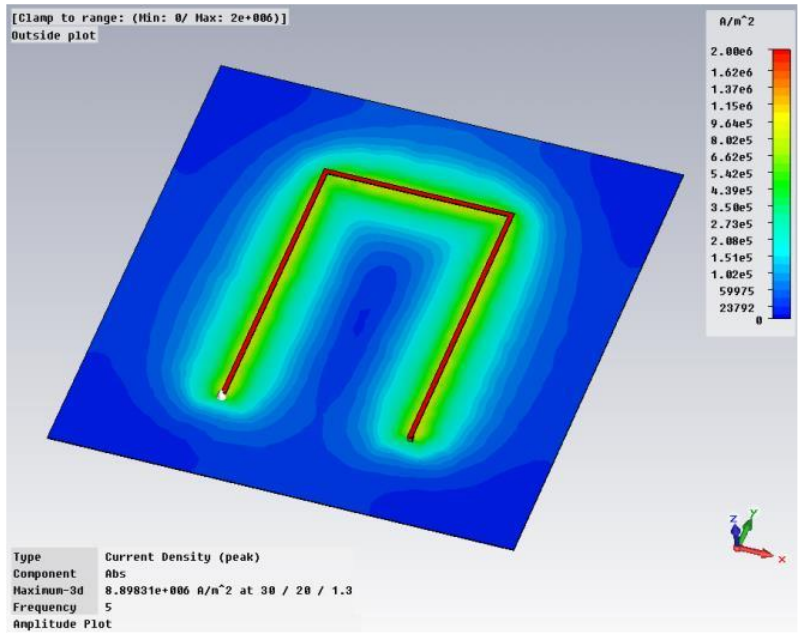
500 Hz

Path of least Impedance

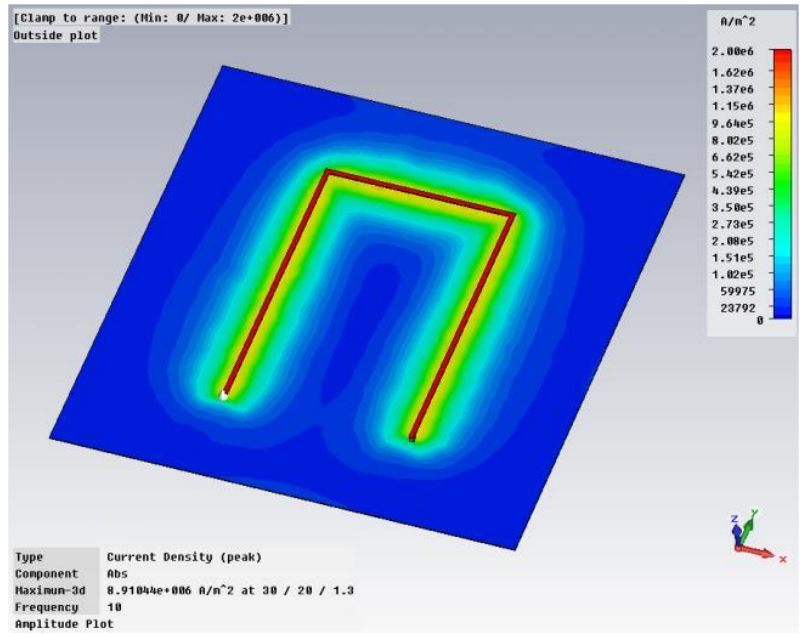
Simulation: Return Path depending on Frequency



1 kHz



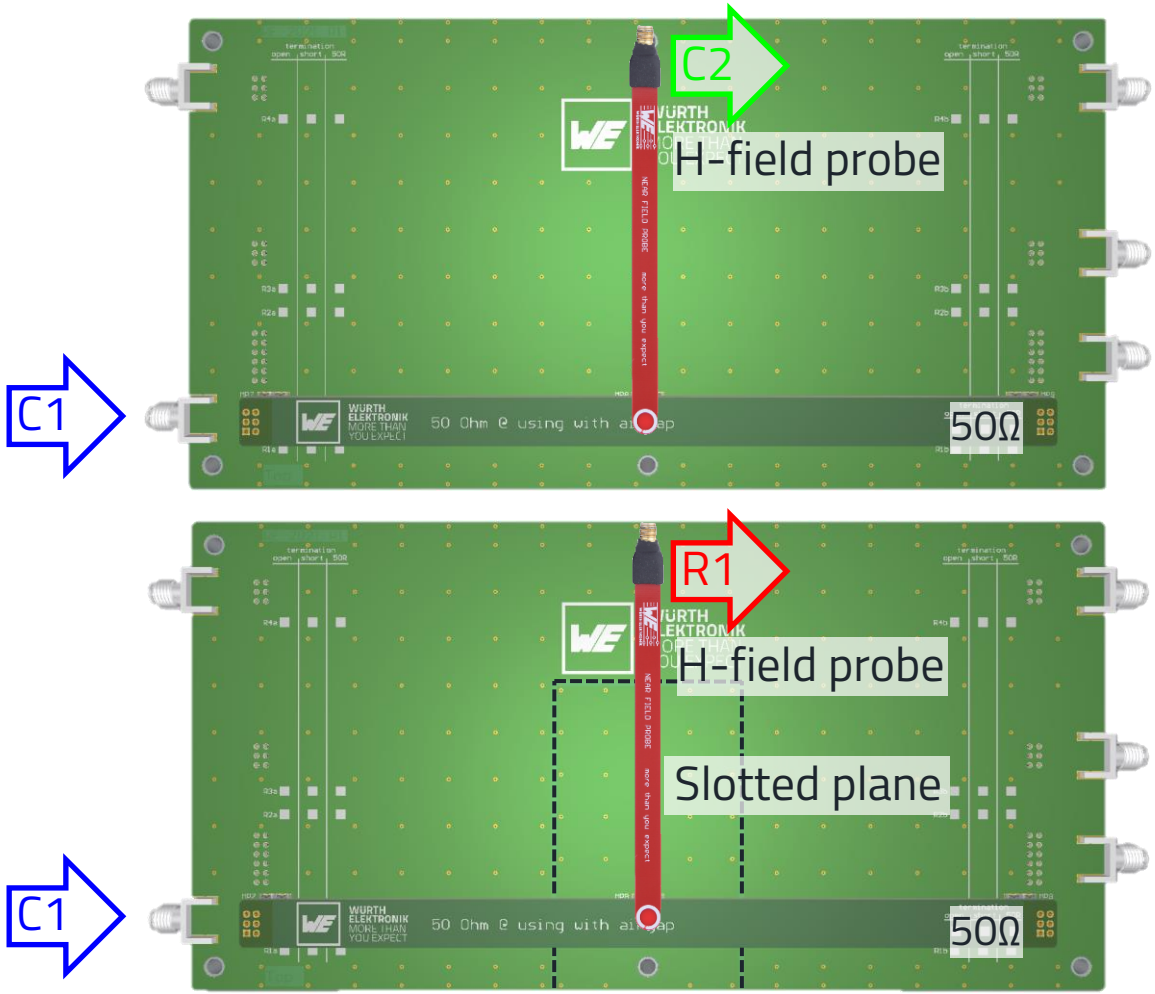
2 kHz

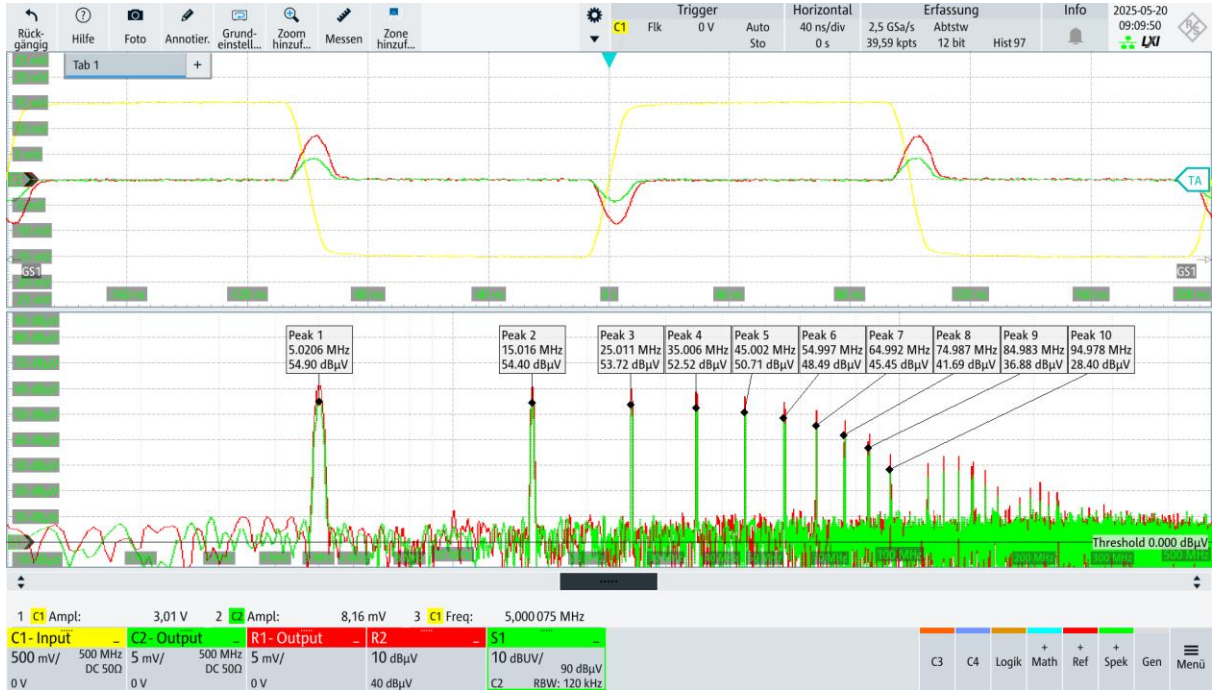


10 kHz

Path of least Impedance

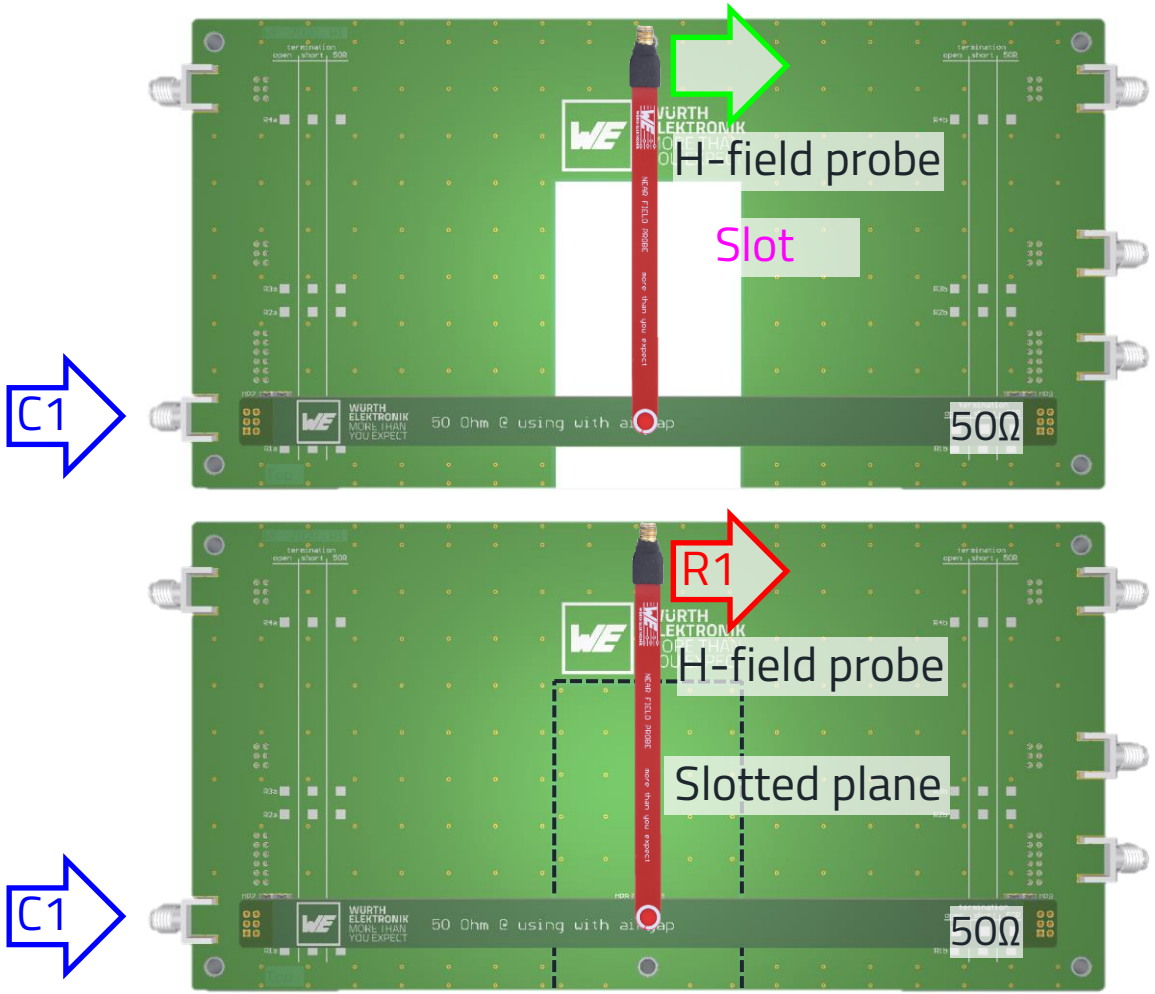
Measurement: Return Path on slotted GND plane

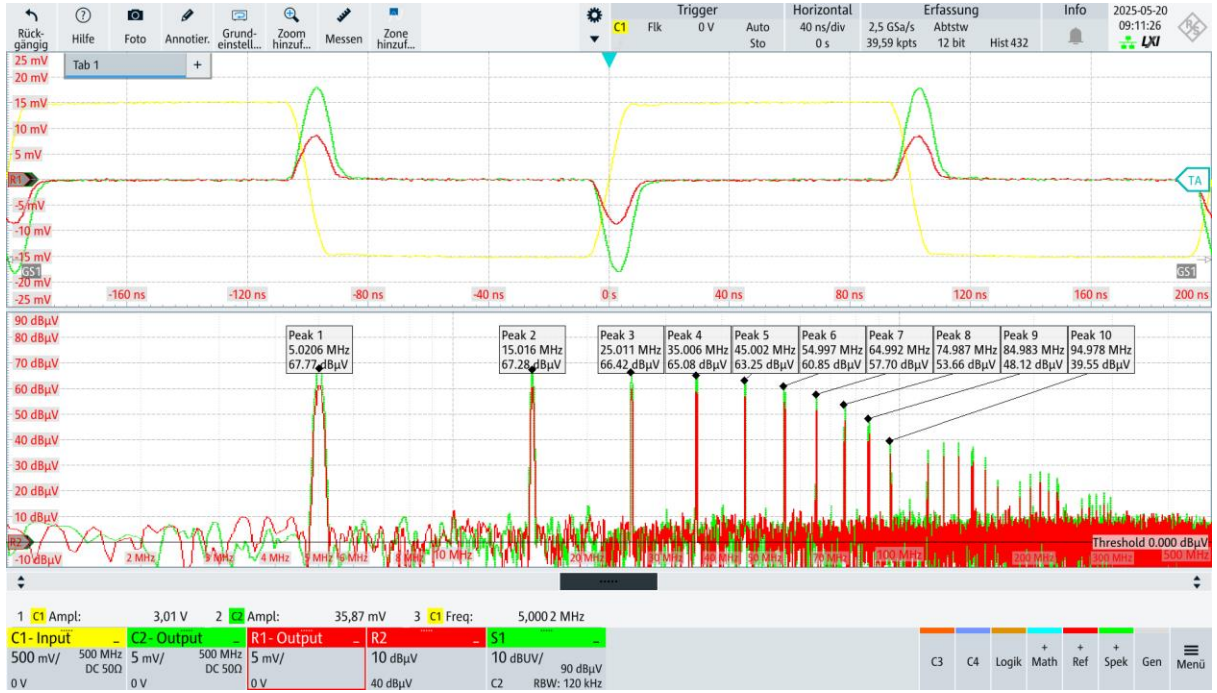




Path of least Impedance

Measurement: Return Path on slotted GND plane

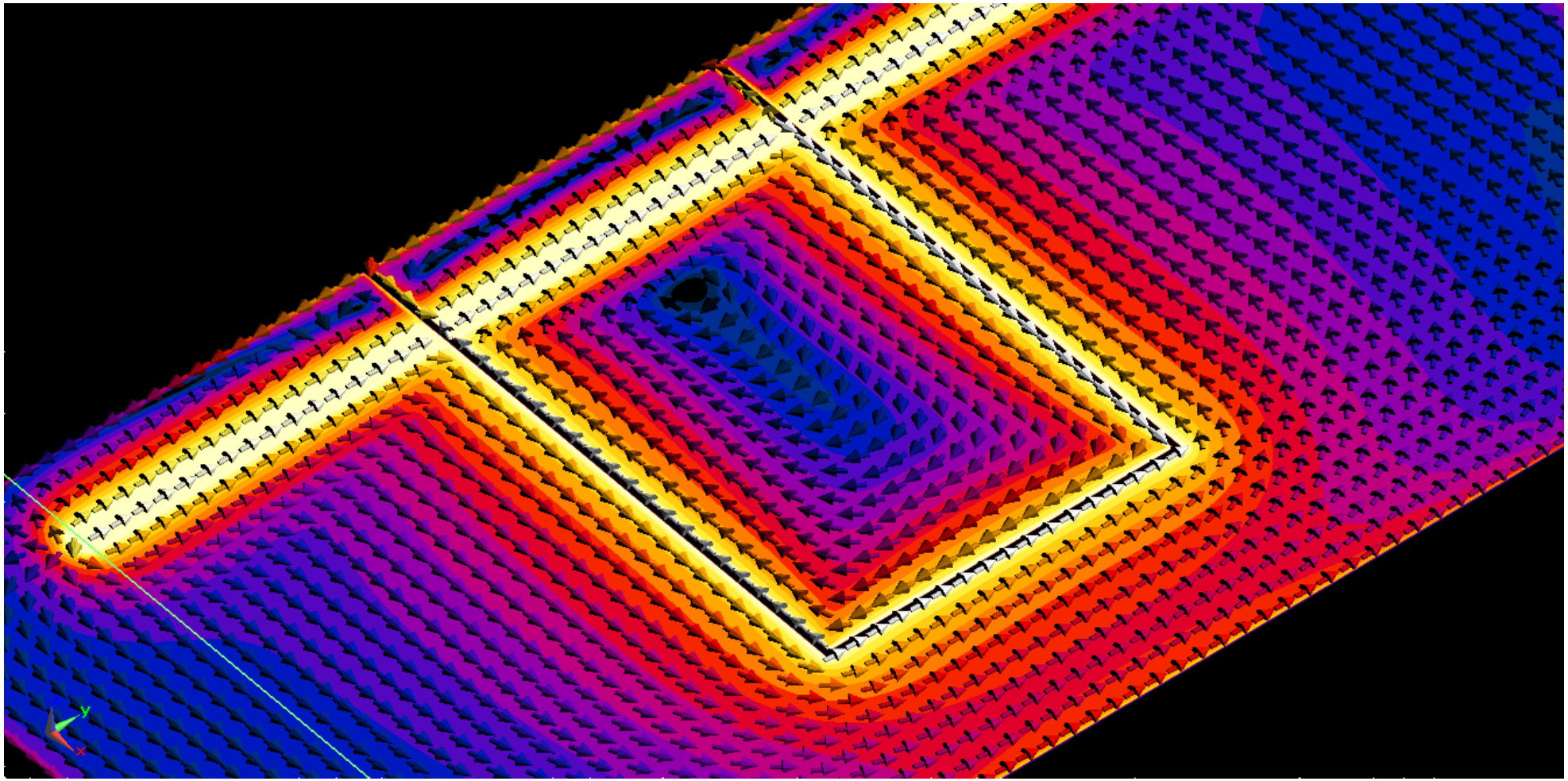




Path of least Impedance

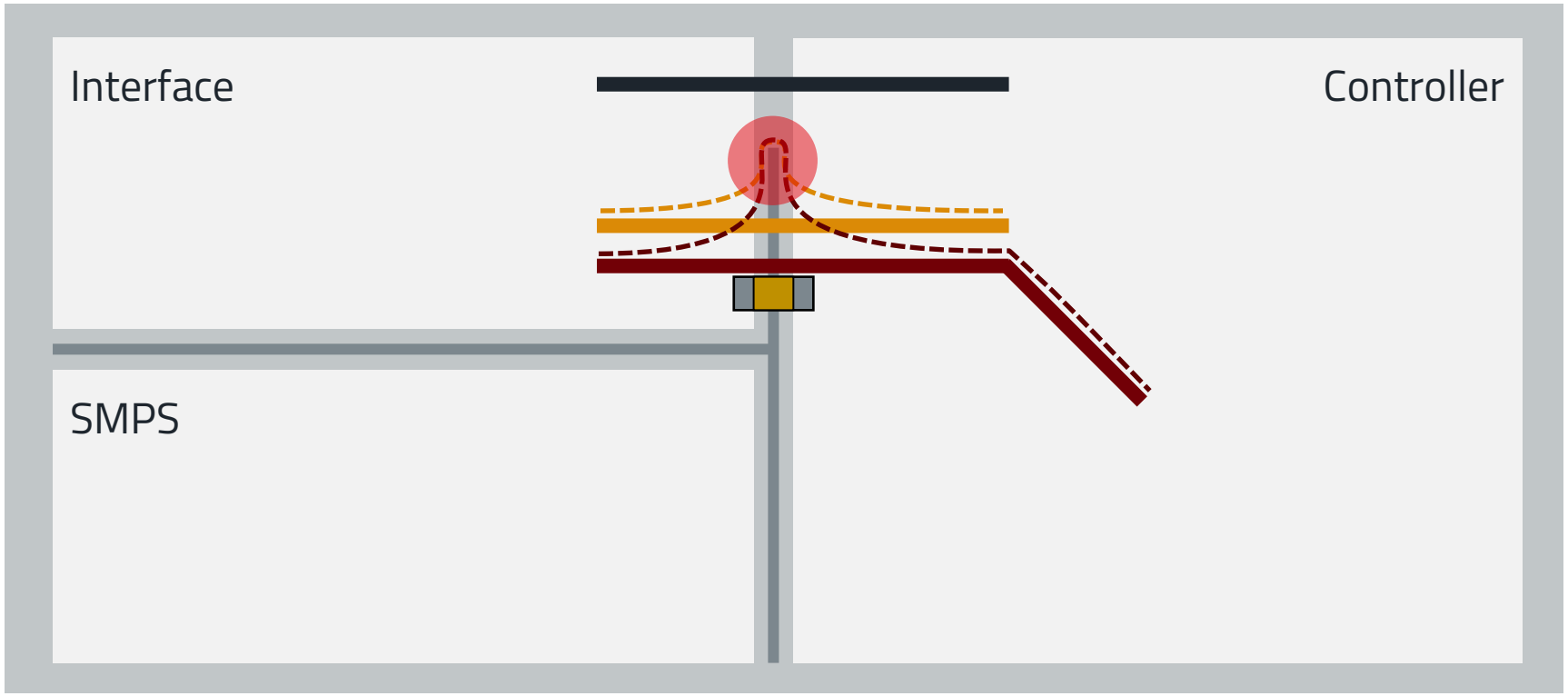
Simulation: Return Path on slotted GND plane

SEIBERSDORF LABORATORIES



Seperating functional blocks

Splitting GND?

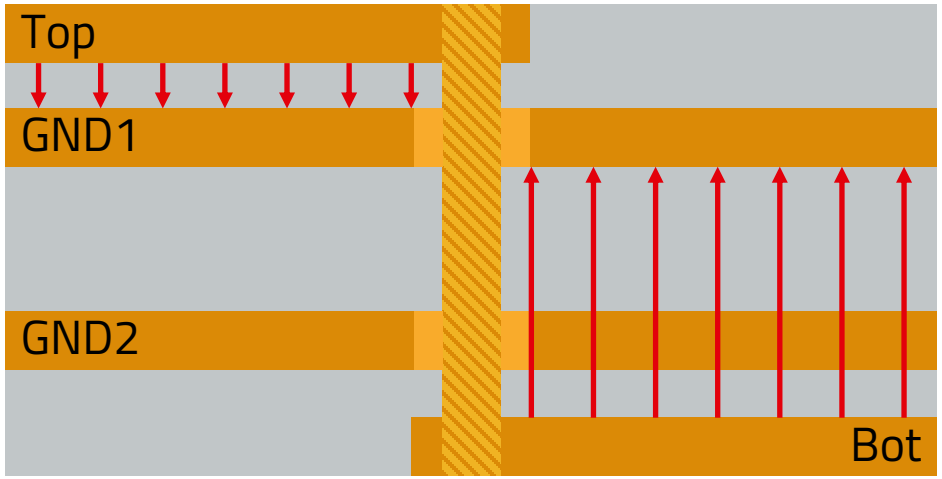


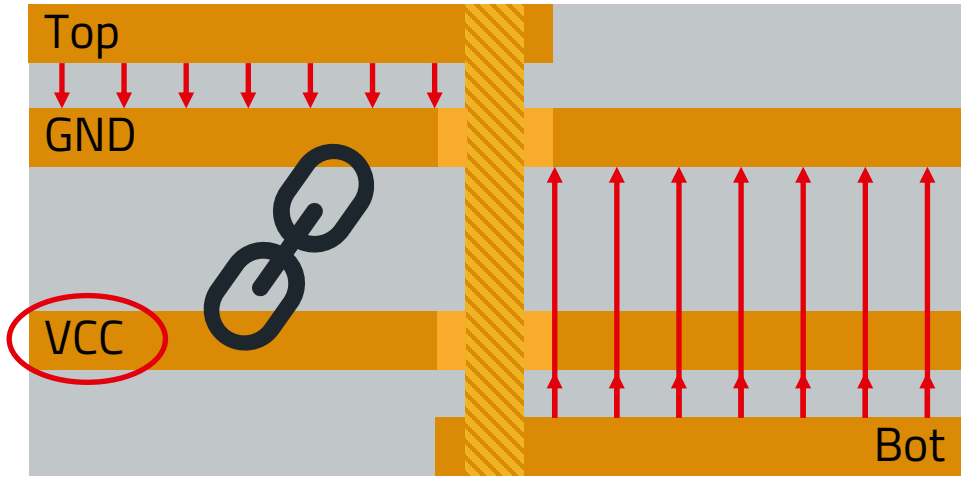
WE eiSos

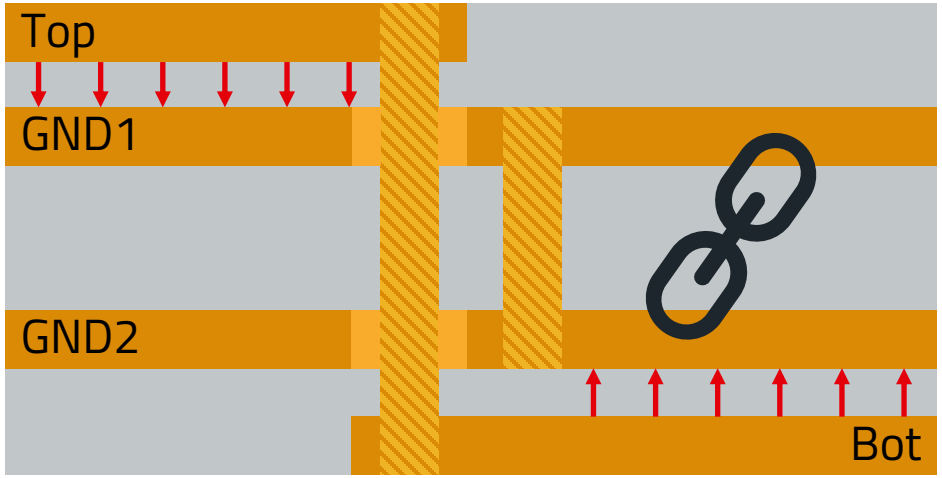
Slotting the GND Plane to form seperate reference points (AGND, DGNG, PGND)

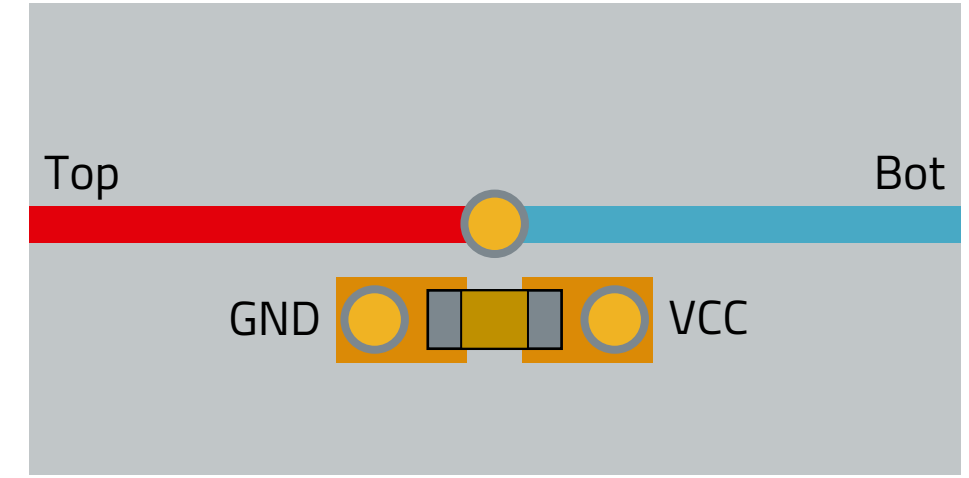
Routing the Return Path

Layer Jumps in Critical Signals









POWER INTEGRITY

Power Integrity

Voltage Drops caused by Peak Currents

- Digital Systems usually allow for a 5…10% voltage ripple

$$\Delta u(t) = \underbrace{R * [i_{Gate1}(t) + i_{Gate2}(t) + \cdots]}_{\text{DC-Drop}} + \underbrace{L * \frac{d}{dt}[i_{Gate1}(t) + i_{Gate2}(t) + \cdots]}_{\text{Noise}}$$

In the 90s

- U = 5 V
- I = 1 A
- R = 5 Ω
- P = 5 W

Z_{target} = 5 Ω / 10
= 0.5 Ω

Industry Standard

- U = 3,3 V
- I = 3 A
- R = 1 Ω
- P = 10 W

Z_{target} = 1 Ω / 10
= 0.1 Ω

State of the Art

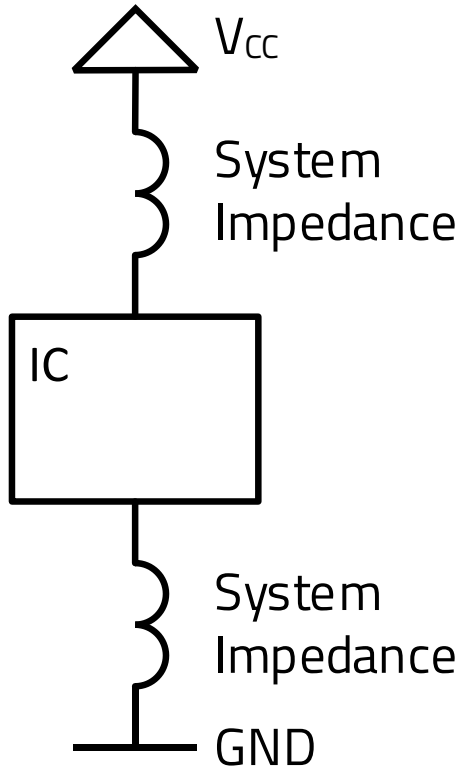
- U = 1 V
- I = 10 A
- R = 0.1 Ω
- P = 10 W

Z_{target} = 0.1 Ω / 10
= 0.01 Ω

Power Integrity

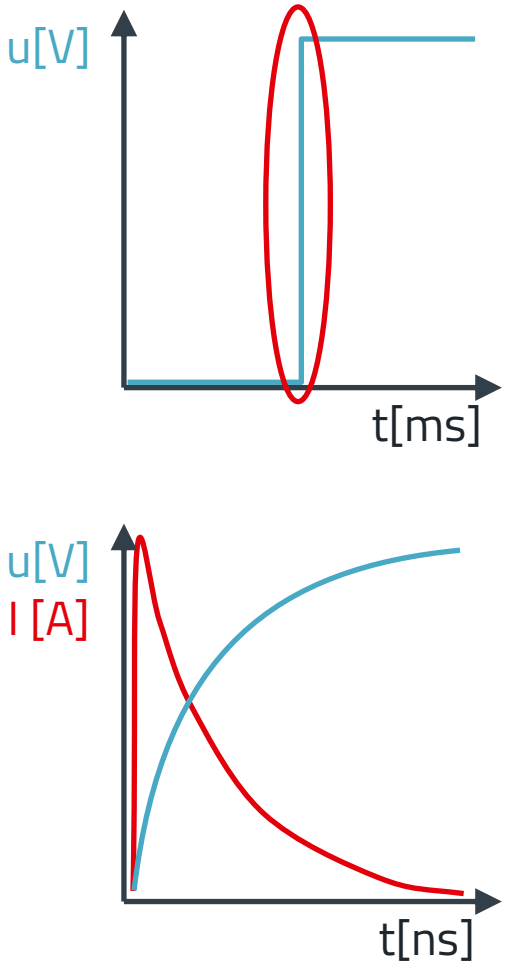
Defintion

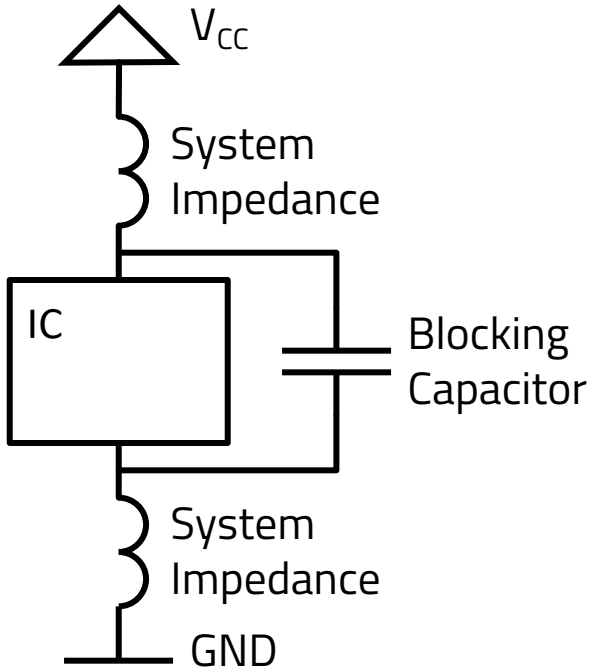
- Keep the voltage ripple lower than the specification
  - Stable Supply for all depending Systems
- Control Ground Bounce
  - Stable Reference throughout the PCB
- Maintain Electromagnetic Compatibilty
  - Avoid Interference with other Components/Systems

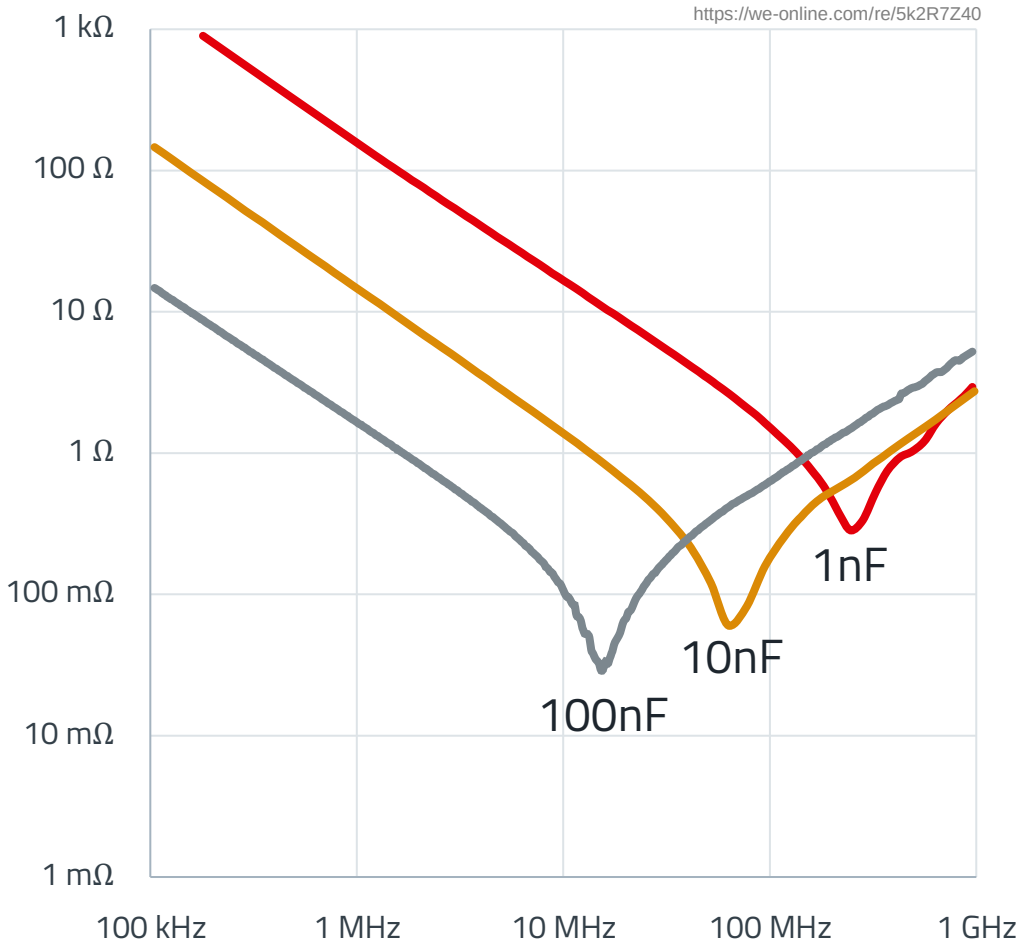


Blocking Capacitors

Mode of Operation and Selection Criteria

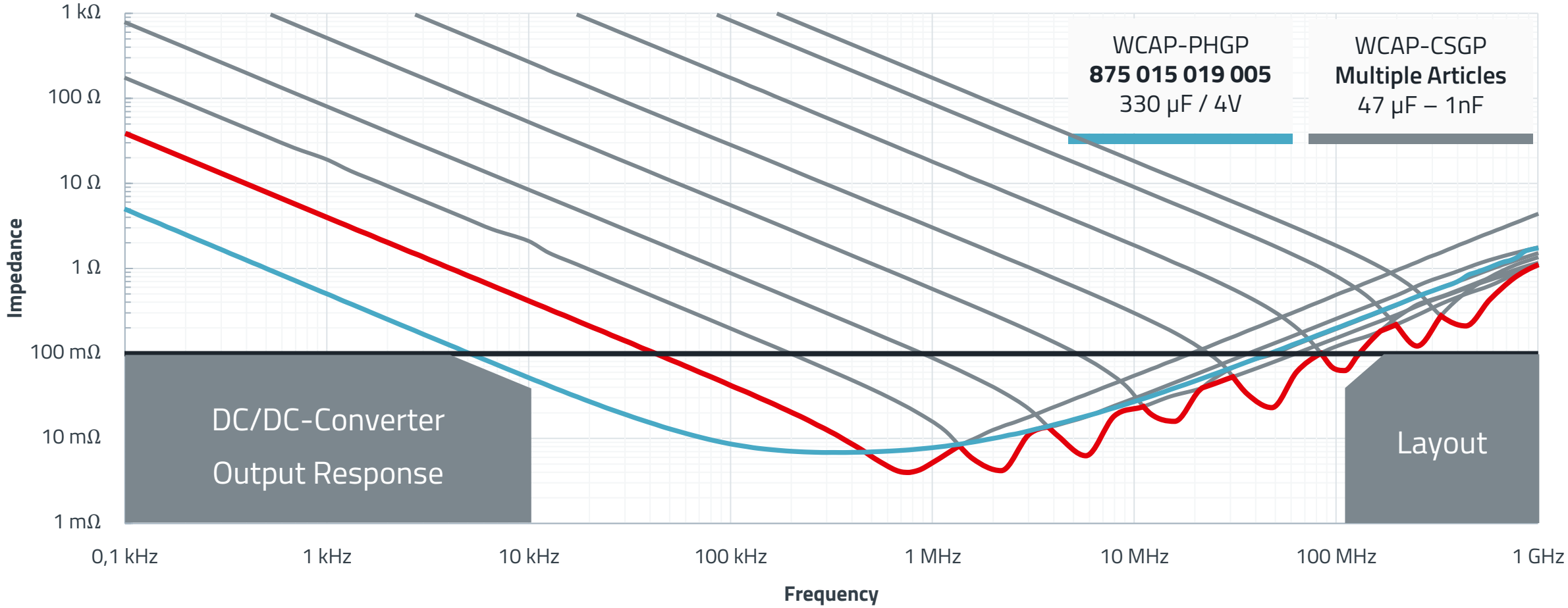






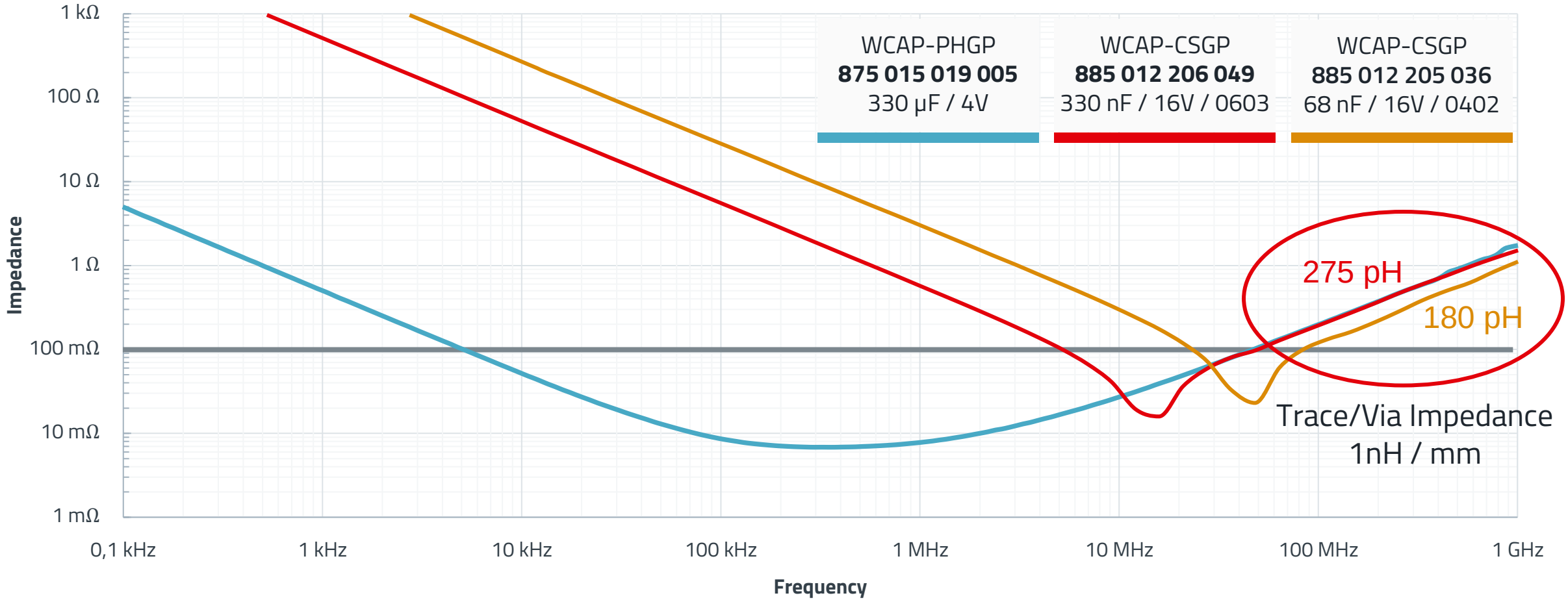
Power Integrity

Effect of Multiple Caps on System Impedance



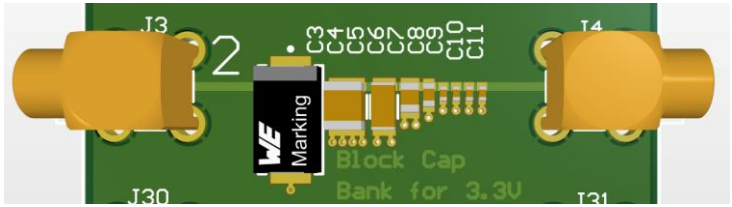
Power Integrity

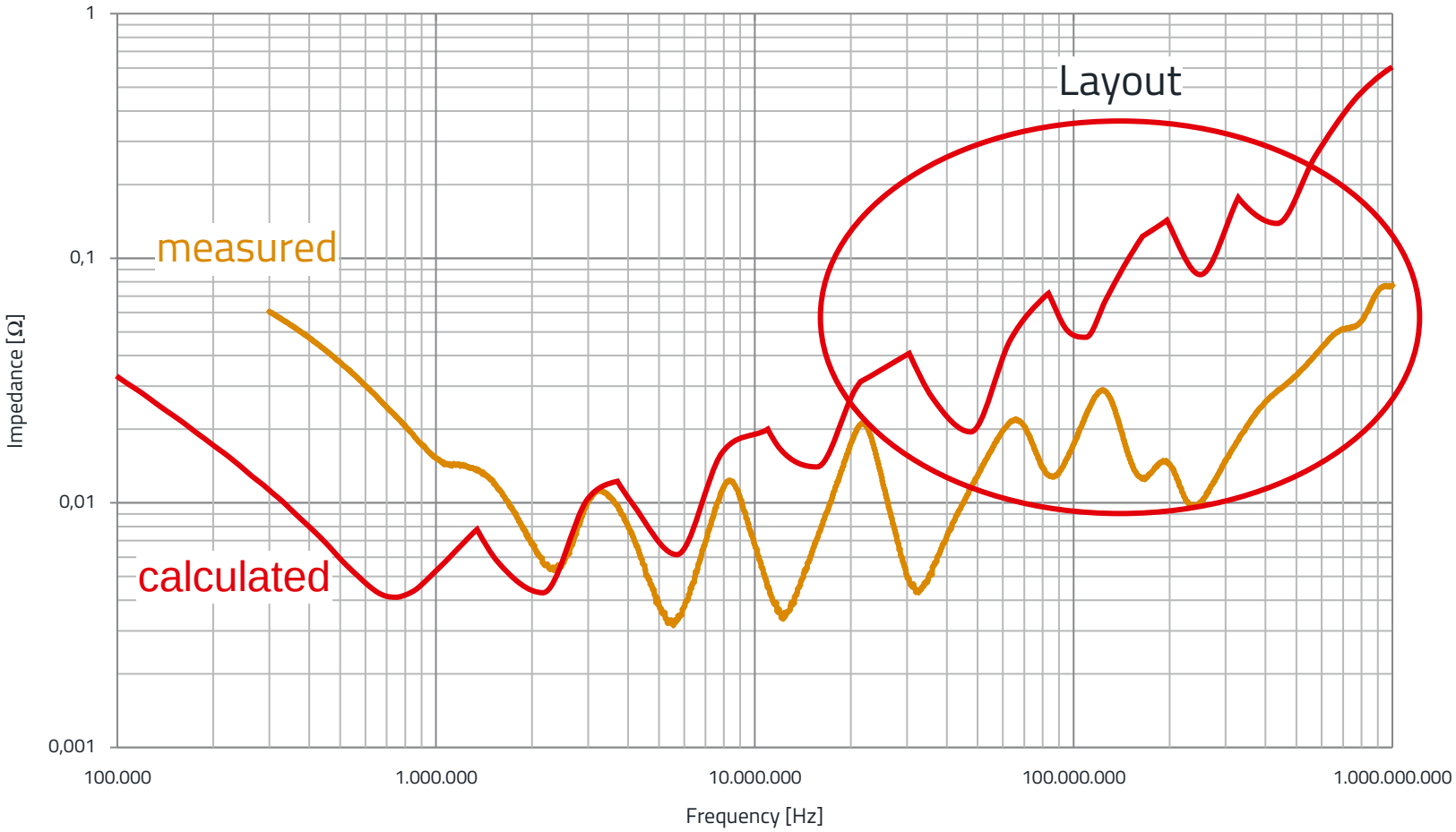
Optimiziation of Caps in Design



Blocking Caps

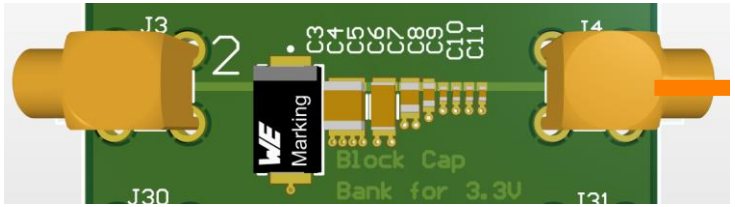
Combined Characteristics vs. Measurement

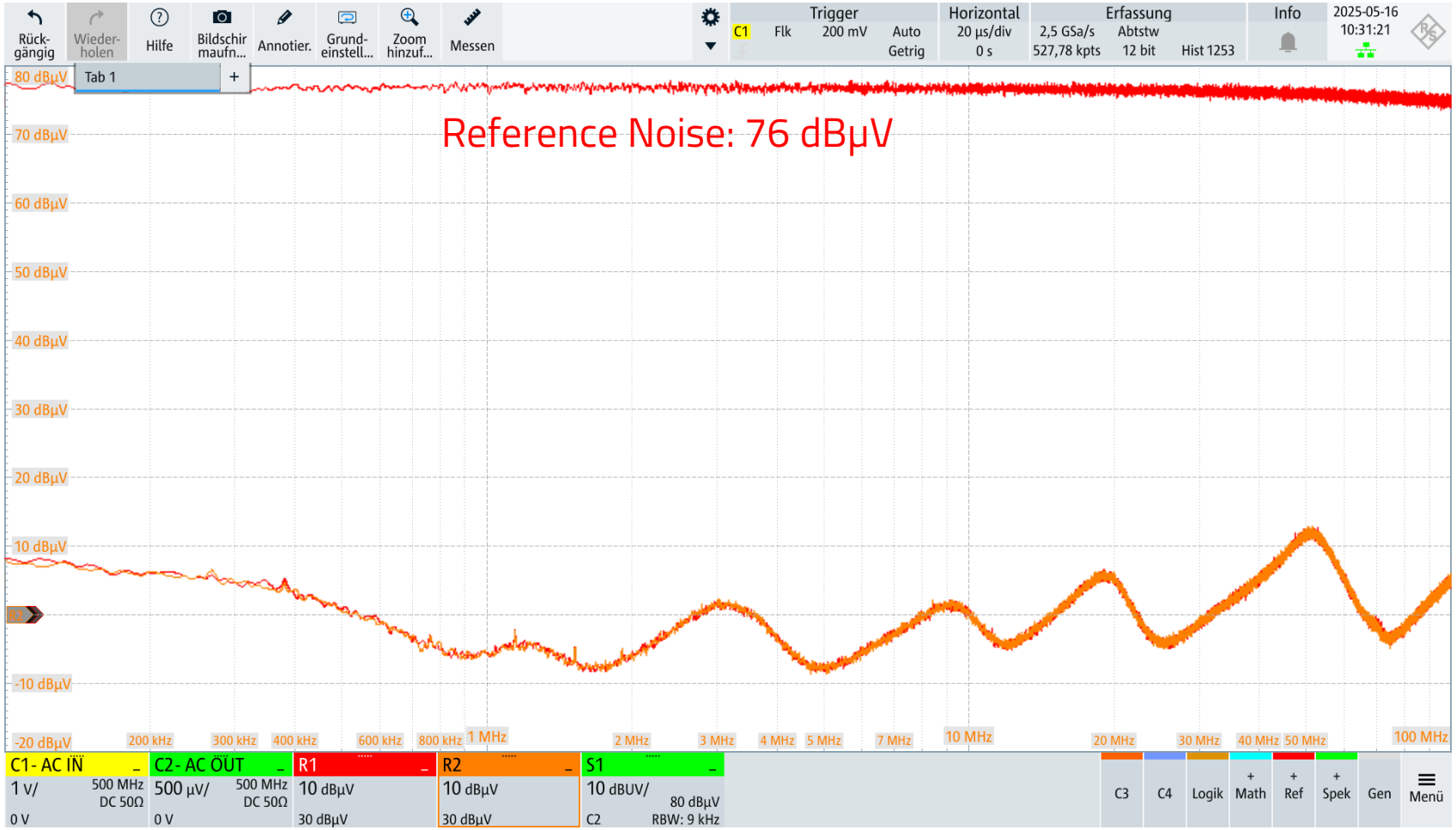




Blocking Caps

Insertion Loss Measurement with Oscilloscope

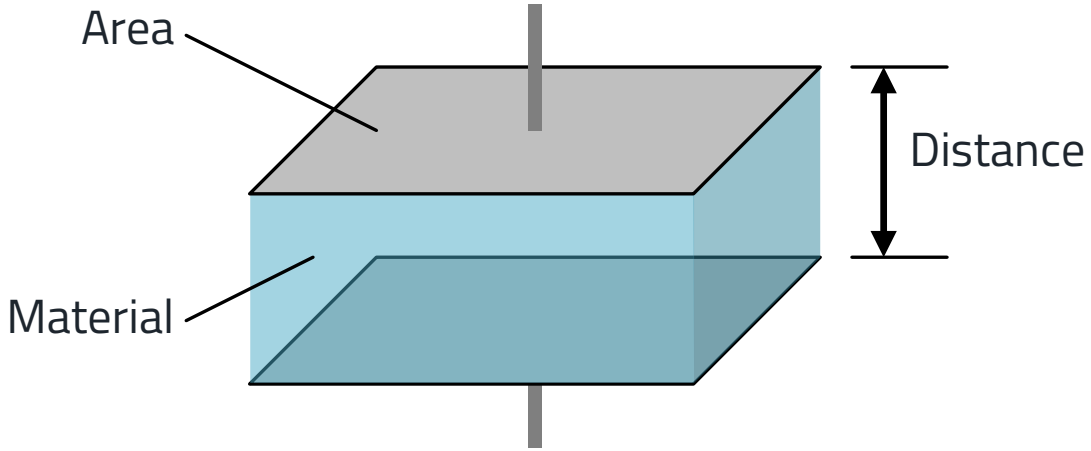




LAYER STACK

Impedance of a VCC/GND Layer System

PCB Layers as Parallel-plate Capacitor



$$C = \varepsilon * \frac{A}{d} = \varepsilon_0 * \varepsilon_r * \frac{A}{d}$$

- C Capacitance [F]
- A Area [m²]
- D Distance [m]
- ε_r Relative Permitivity: FR4 ca. 4.2
- ε_0 Vacuum Permittivity: $8{,}85 \times 10^{-12} \frac{As}{Vm}$

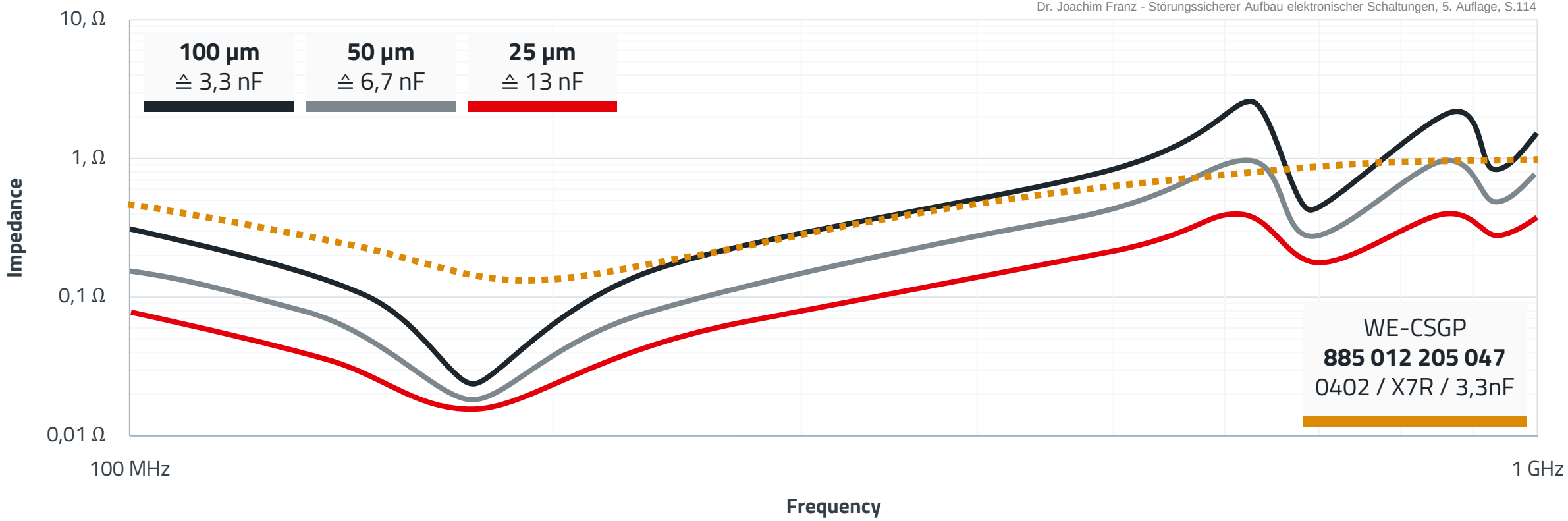
Example PCB 112x80 mm (d = 100 µm):

$$C = \frac{0{,}009m^2}{100 \times 10^{-6}m} \times 8{,}85x10^{-12} \times 4.2 = \mathbf{3{,}3nF}$$

Impedance of a VCC/GND Layer System

PCB Layers as two-dimensional conductor planes

https://we-online.com/re/5s1ByXKX
Dr. Joachim Franz - Störungssicherer Aufbau elektronischer Schaltungen, 5. Auflage, S.114

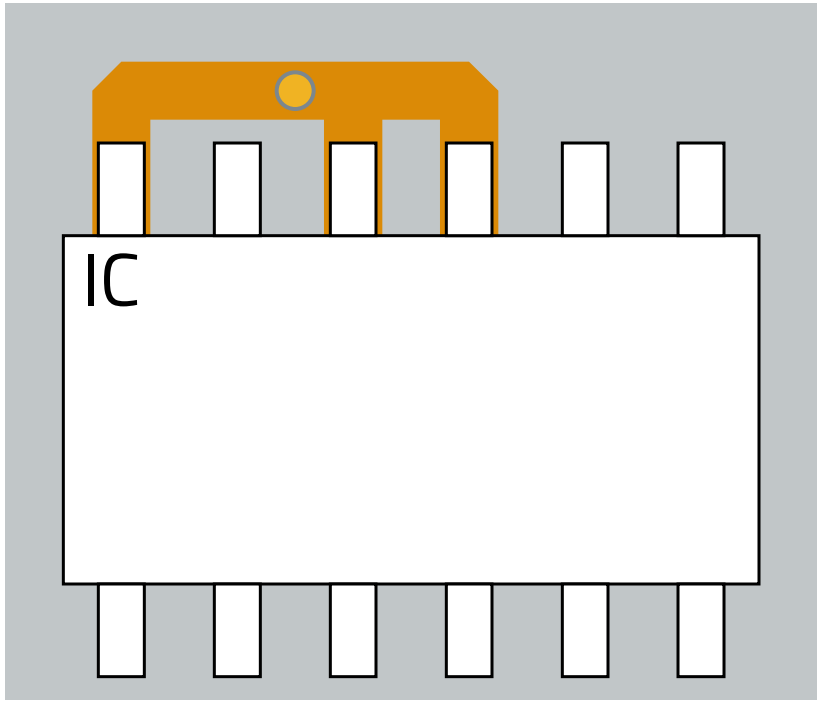


Simulated Impedance of the Vcc/GND System of a PCB 112mmx80mm

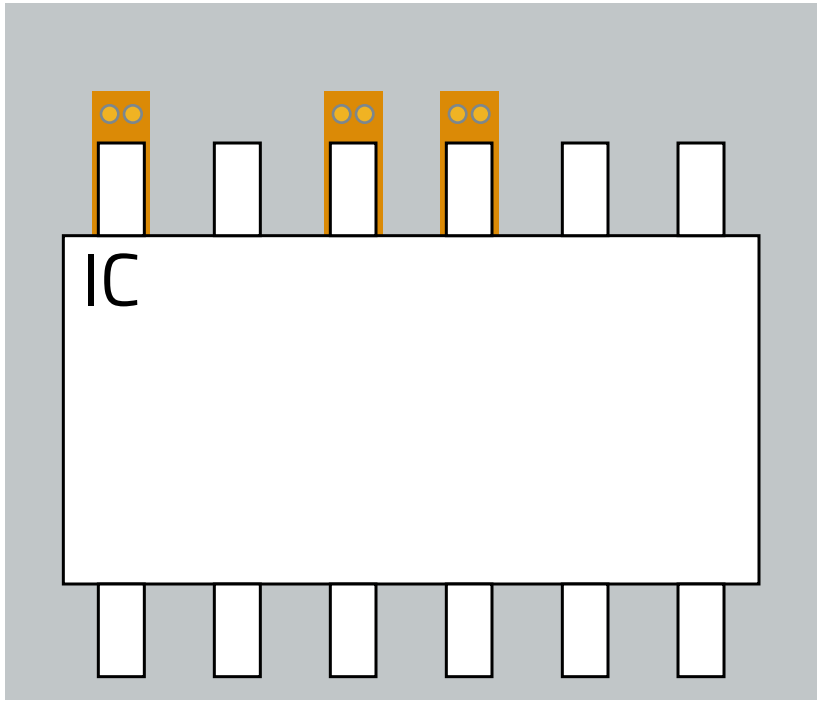
ARRANGEMENT OF TRACES & VIAS

Single Vias vs Grouped Vias

Ground Connection @ IC Pins



Bad



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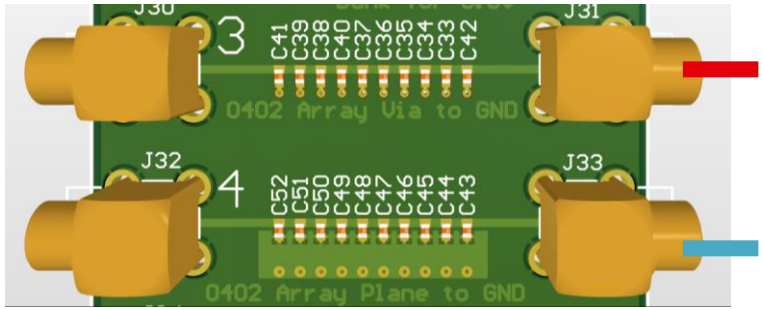
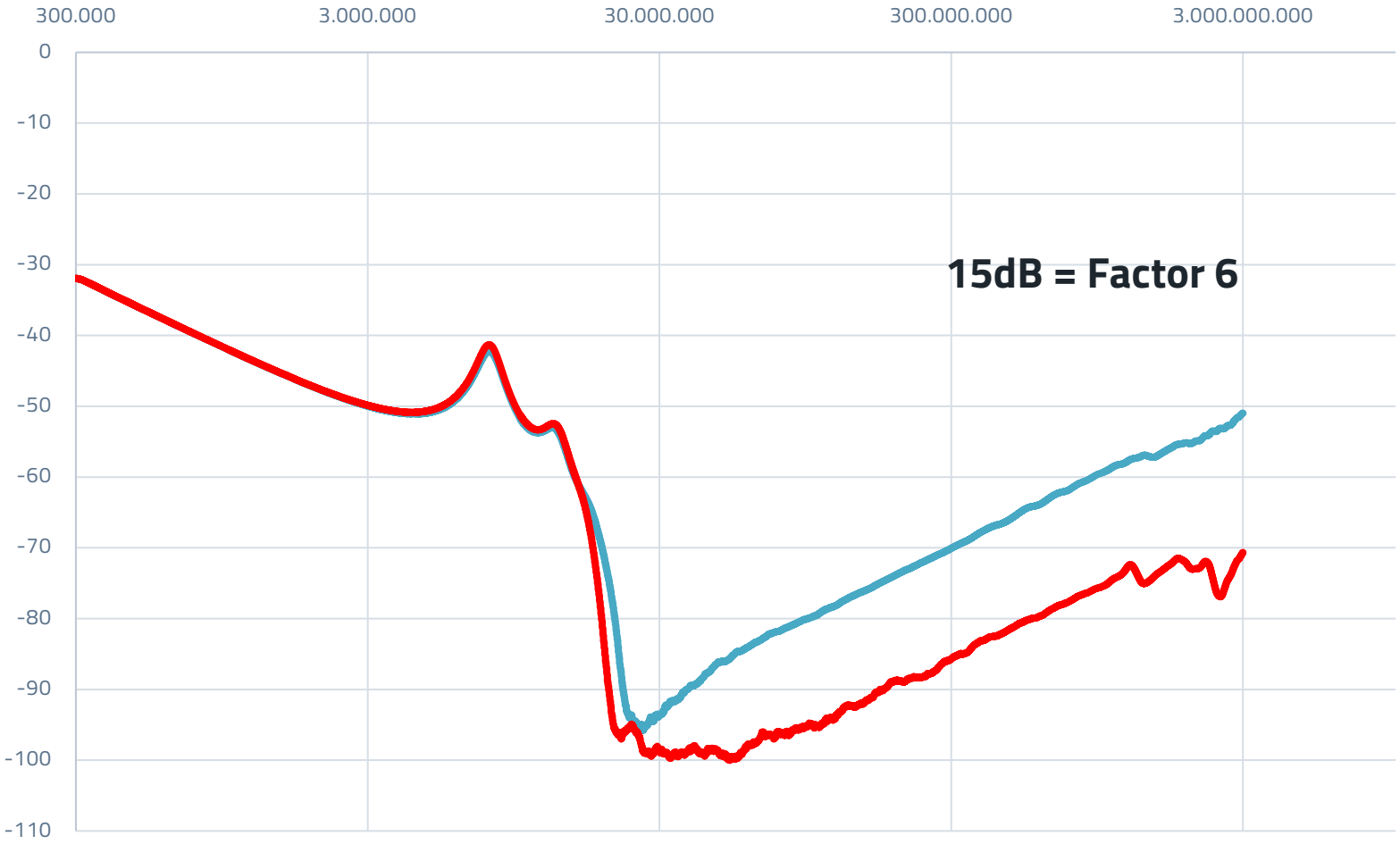
Better

Single Vias vs Grouped Vias

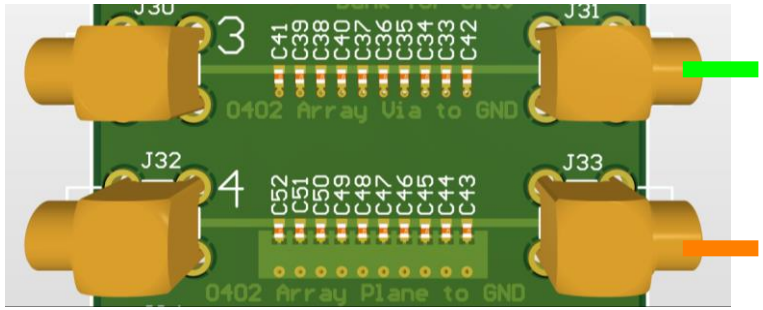
Example: 10x 100nF MLCCs, VNA Measurement

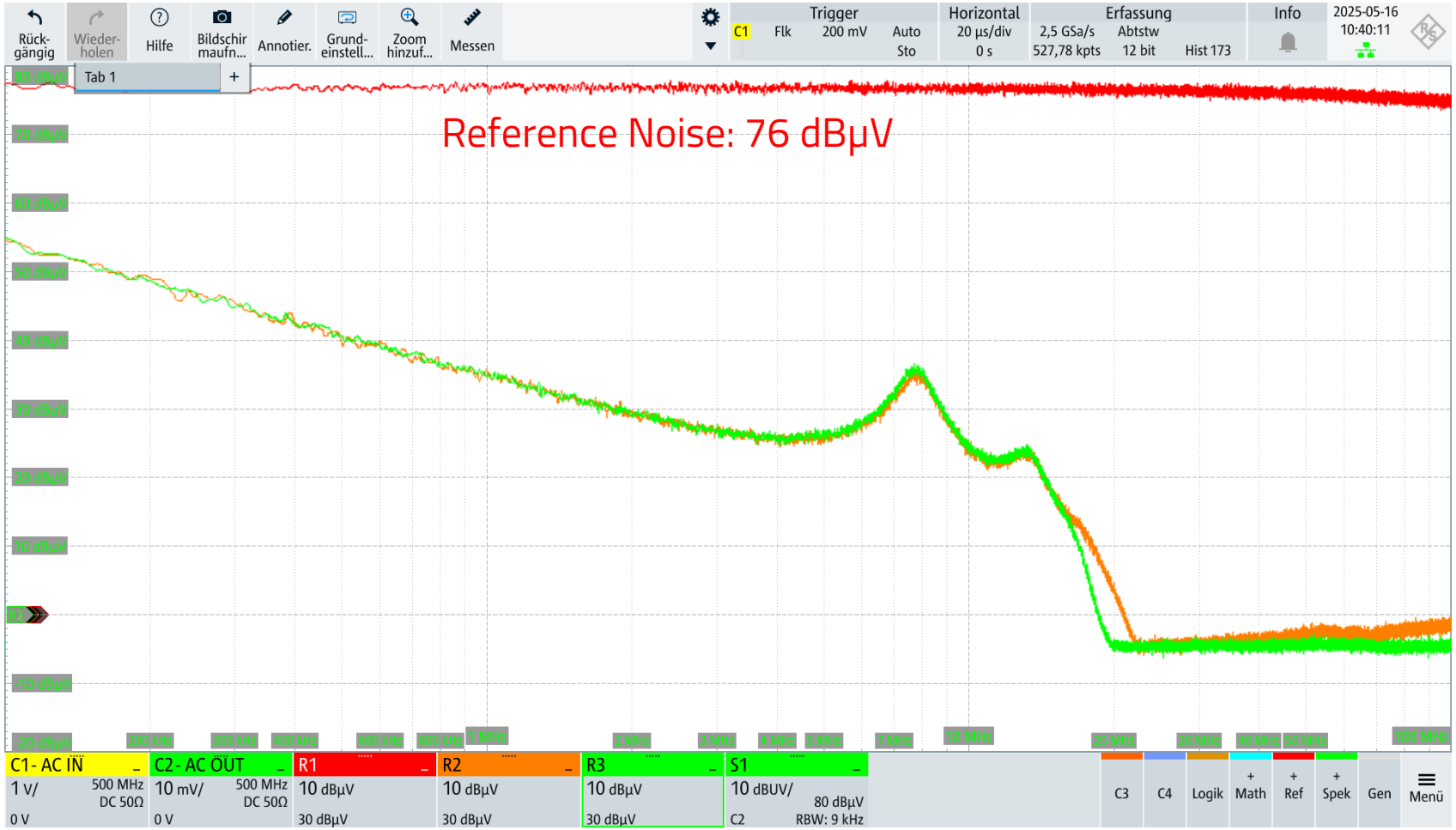




Single Vias vs Grouped Vias

Example: 10x 100nF MLCCs, Oscilloscope Measurement





Filter Capacitors

General Considerations

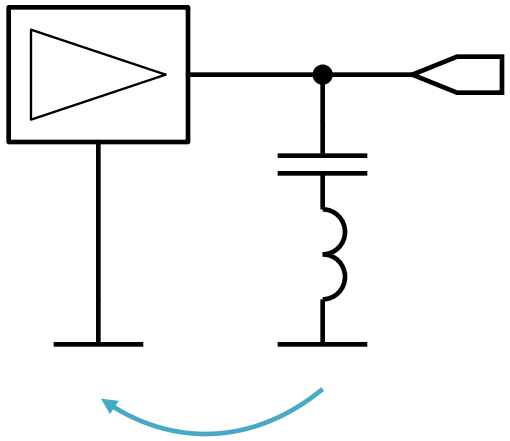
- For all capacitive Filters a low impedance connection to reference potential is key
  - For DM: (A/P) Ground
  - For CM: Earth / Chassis

- Additional Impedances decrease efficiency of RF short
  - THT contact pins
  - Inductance of PCB traces

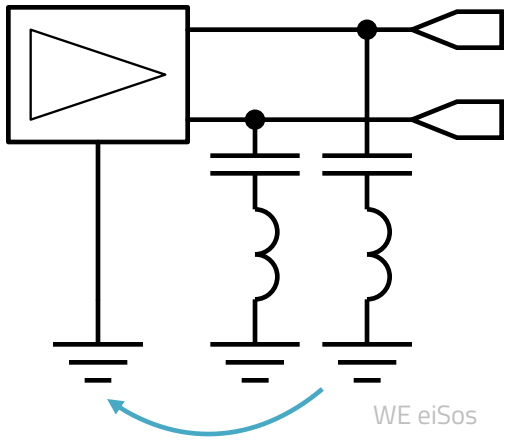
  - 1nH per 1mm
  - 0.5nH per Via

  - Placement connection of steel spacers

Differential Mode Short



Common Mode Short



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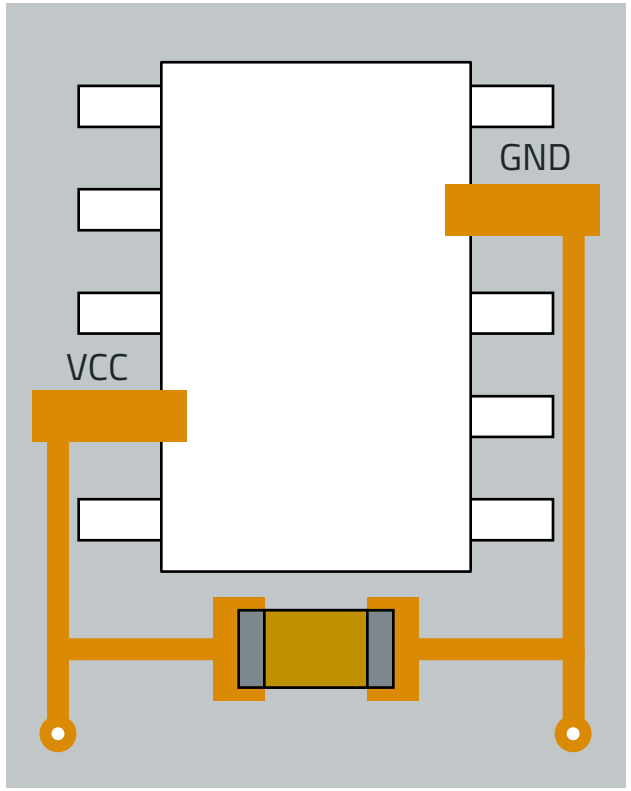
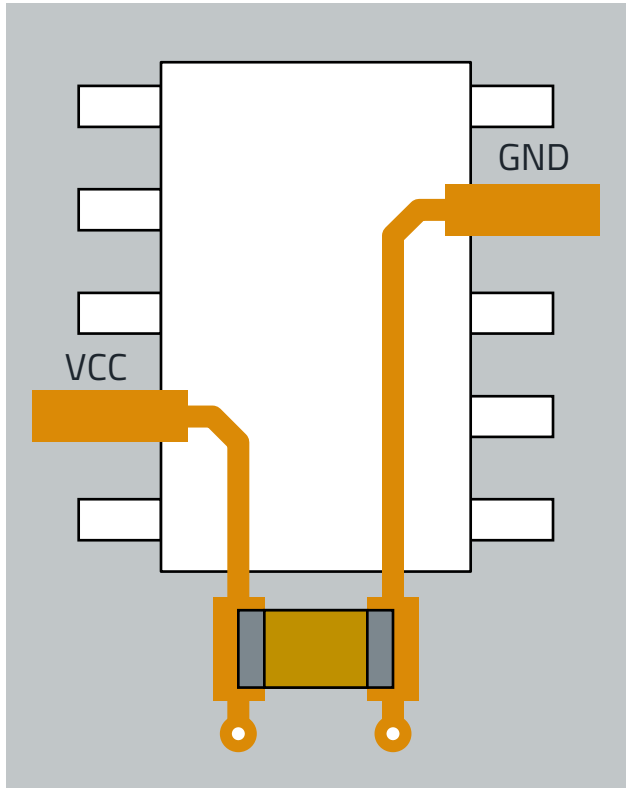
Local Supply Loop

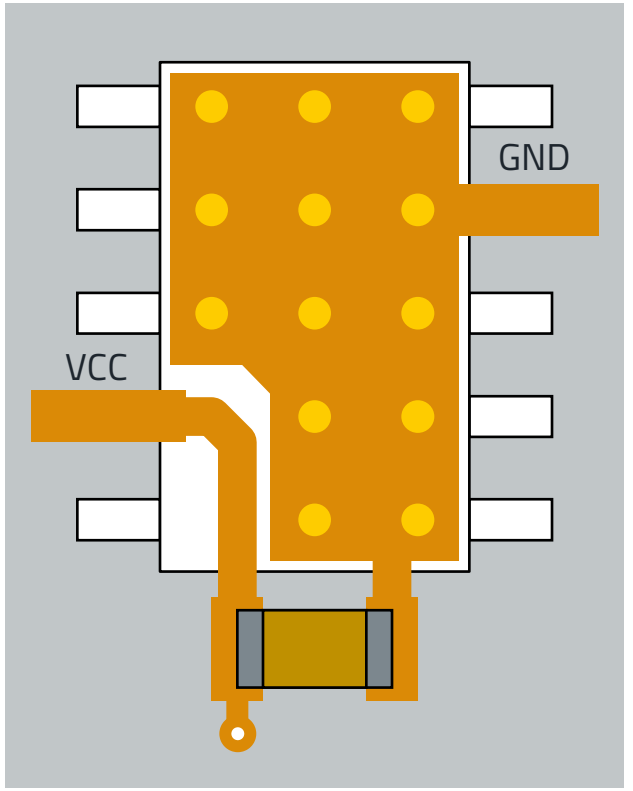
Routing to Ground and Supply Pins



Bad
Connecting the Cap using stubs



Good
Directing current along Capacitor pads



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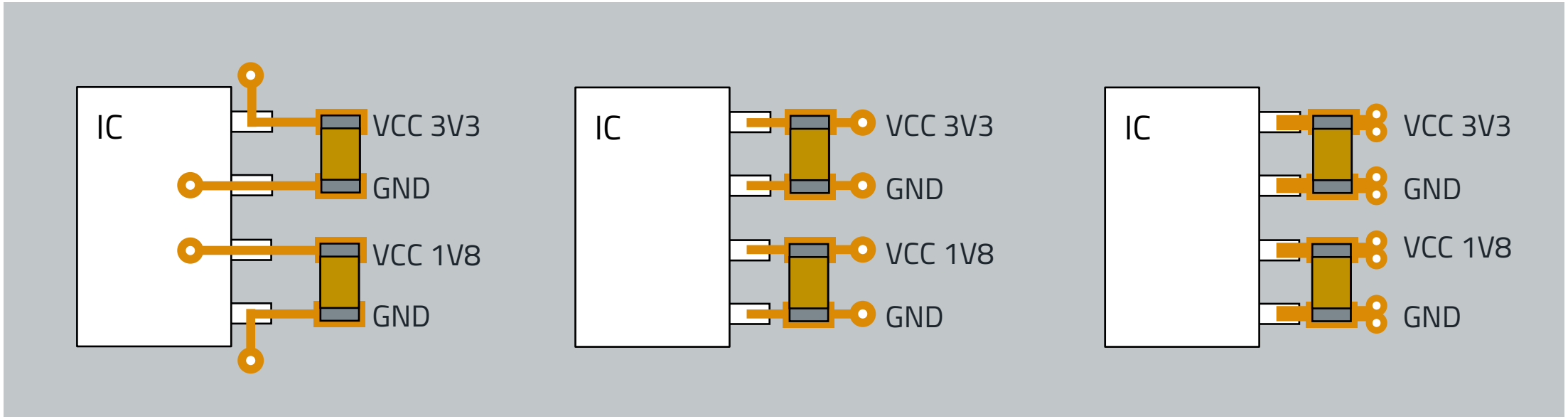
Better
GND Plane to account for loops inside the IC

Local Supply Loop

Routing to Blocking Capacitors & Vias



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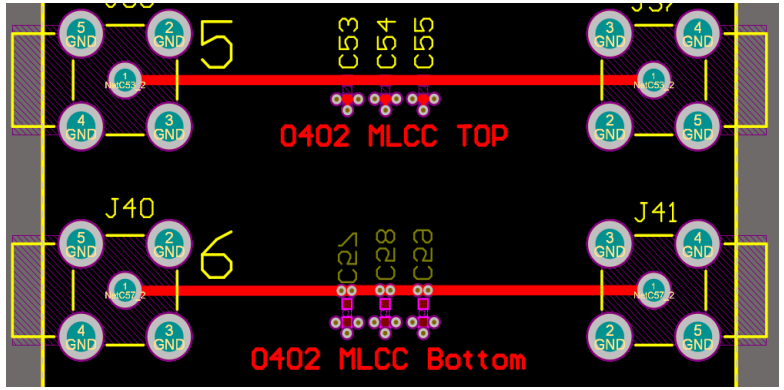
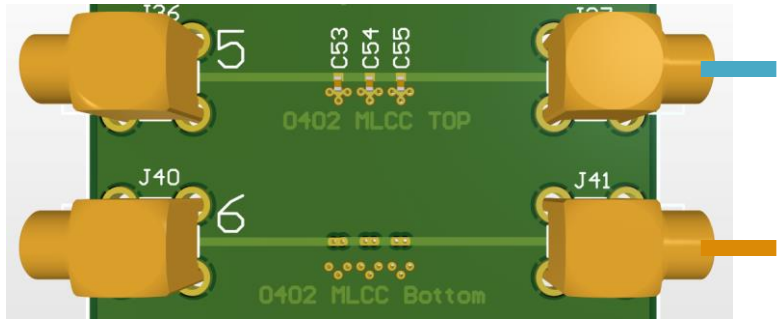
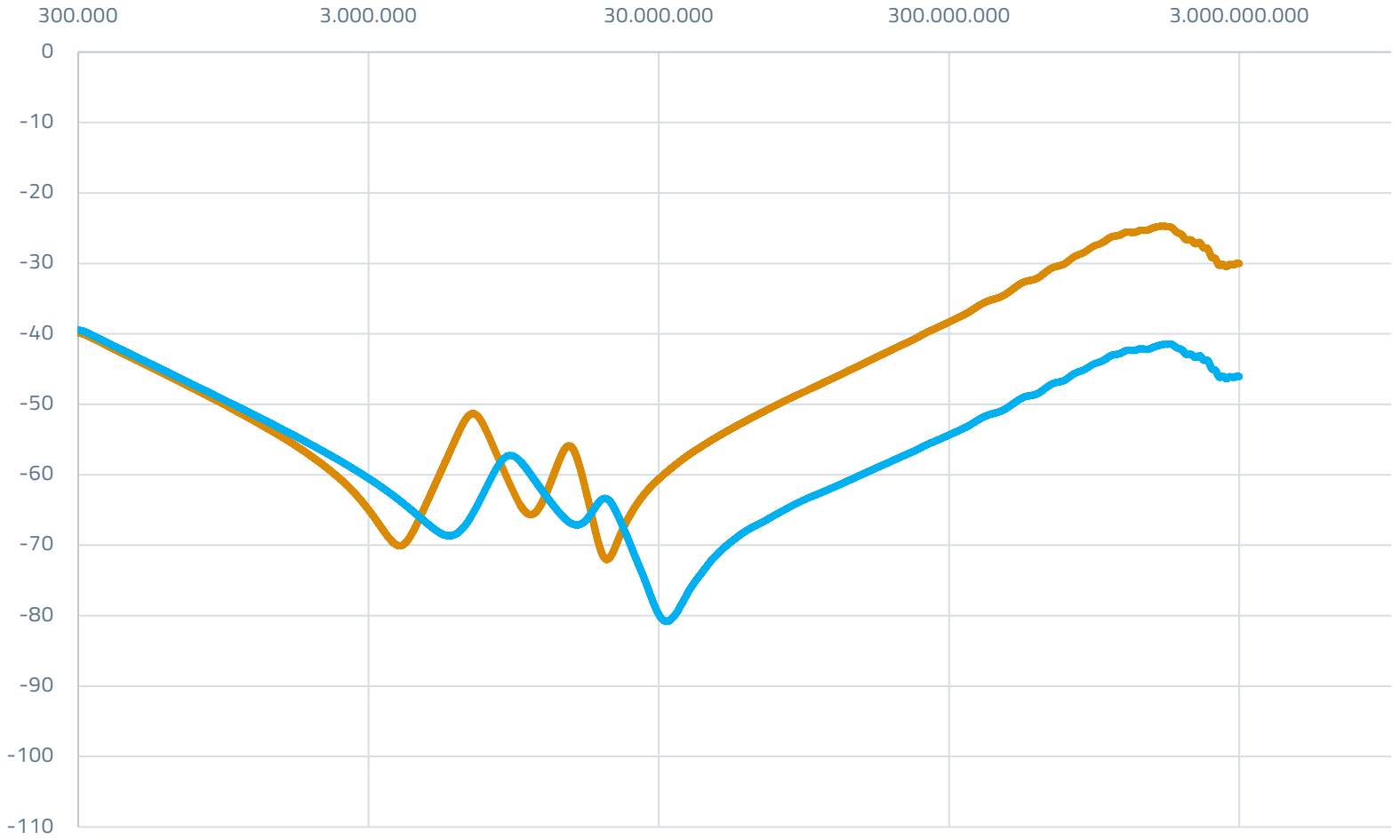
Bad **Good** **Better**

Routing to Blocking Capacitors & Vias

Comparison of standard vs BGA style connection of 3xMLCCs in parallel (2.2µF + 330nF + 68nF)

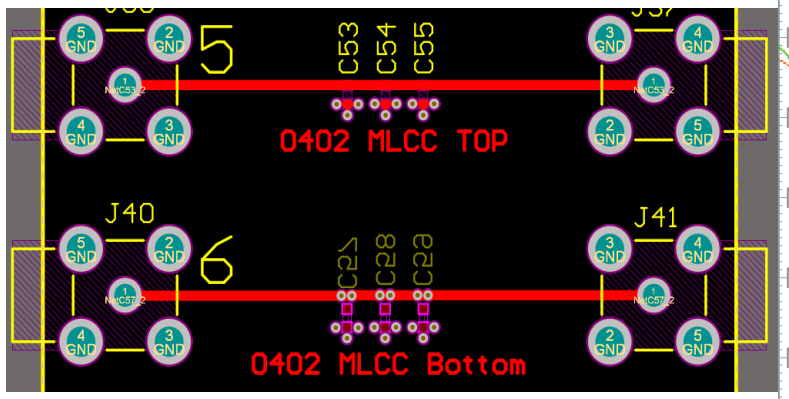


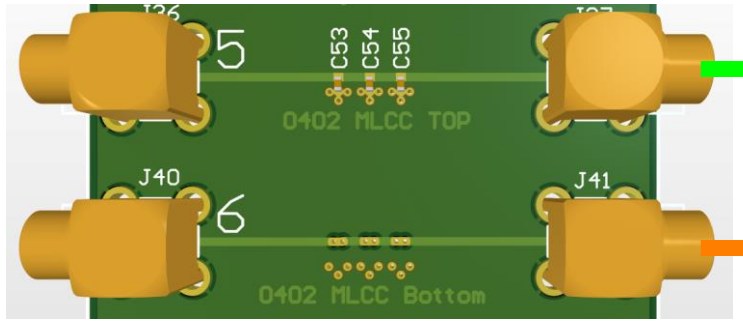


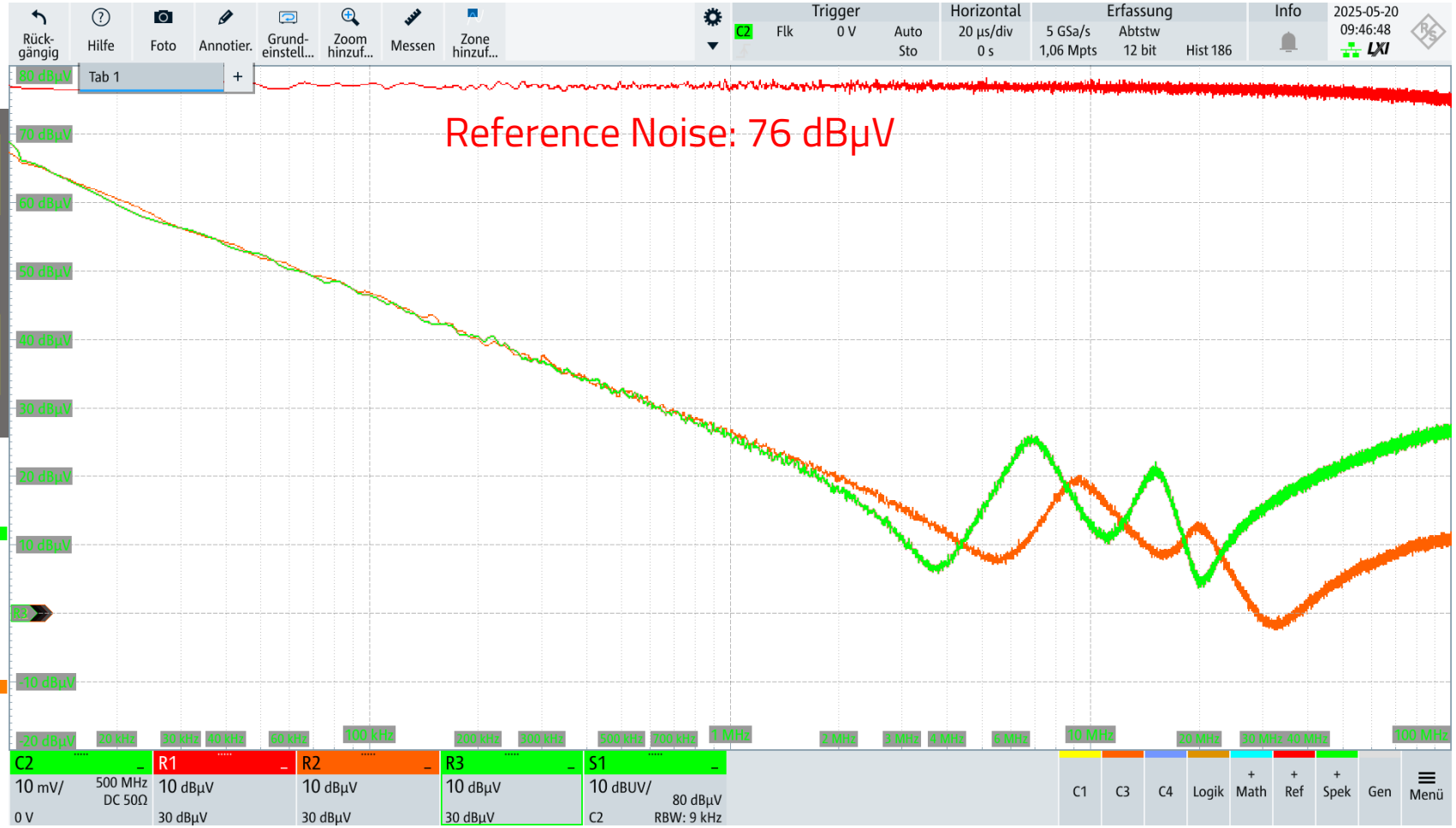


Routing to Blocking Capacitors & Vias

Comparison of standard vs BGA style connection, Oscilloscope Measurement

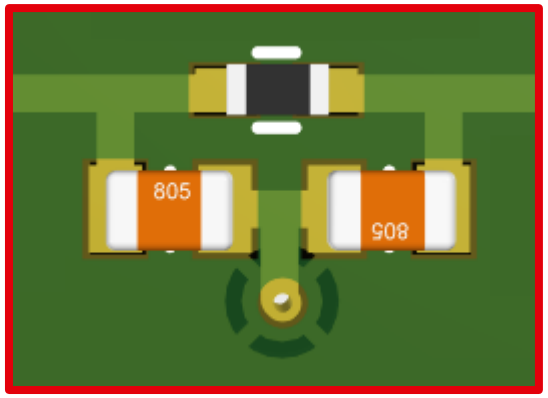




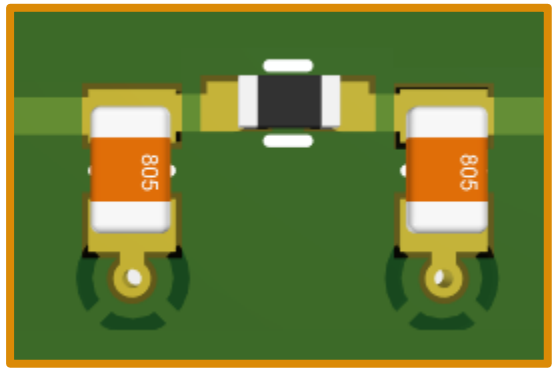


Filter Arrangement

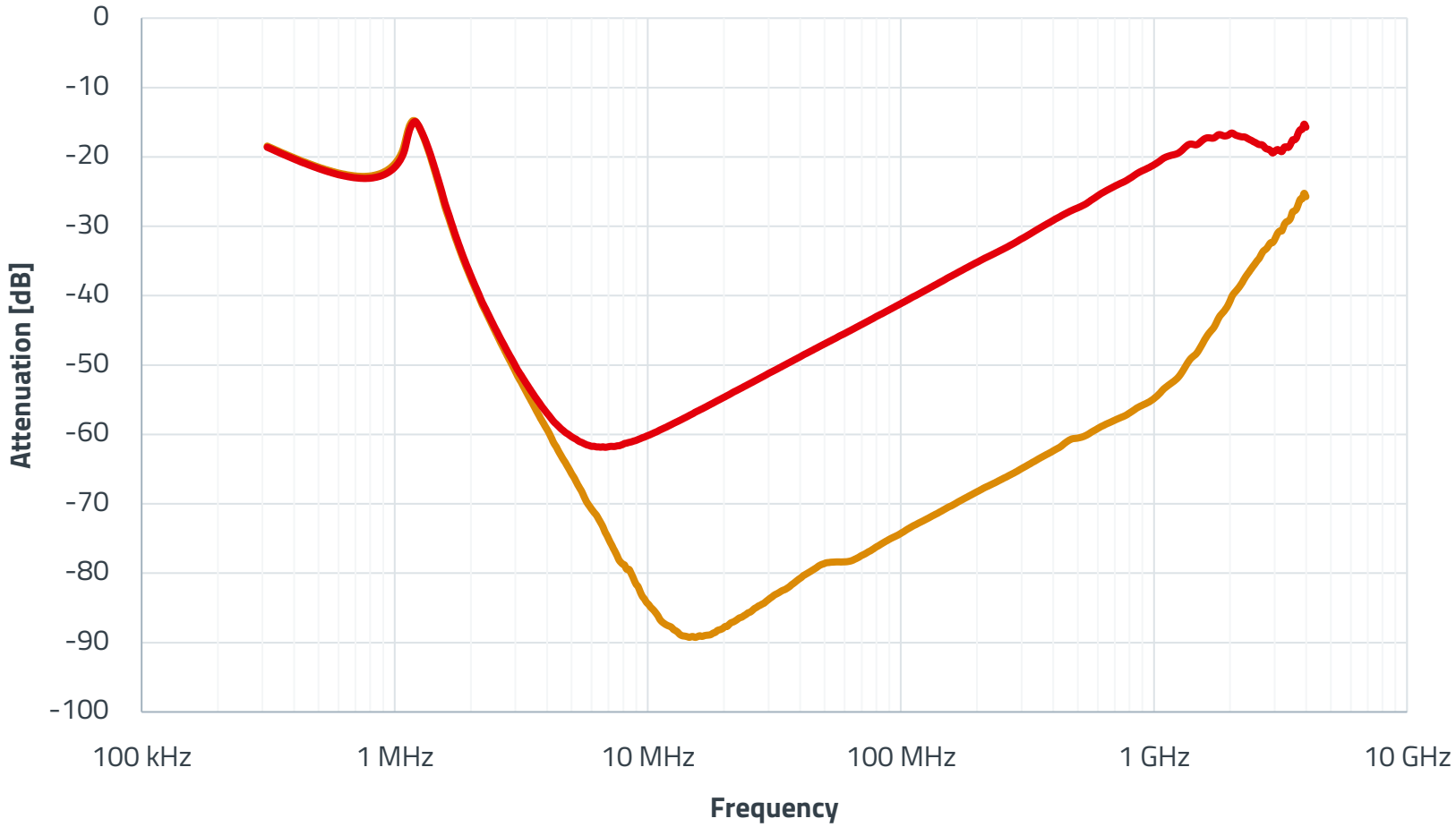
Layout: Influence on Insertion Loss



0805, Bad Layout

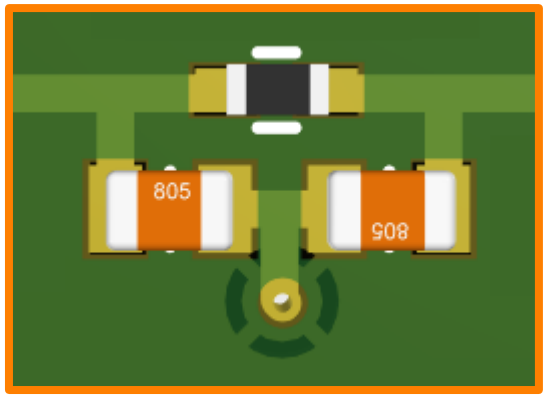


0805, Good Layout

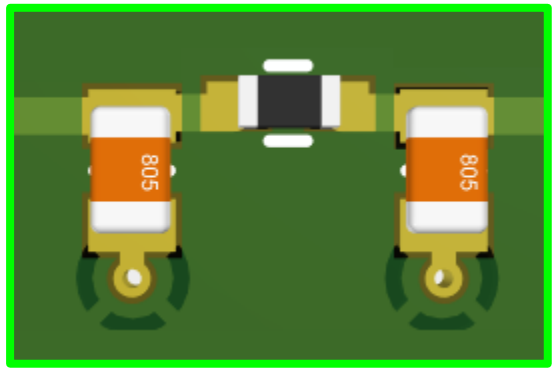


Filter Arrangement

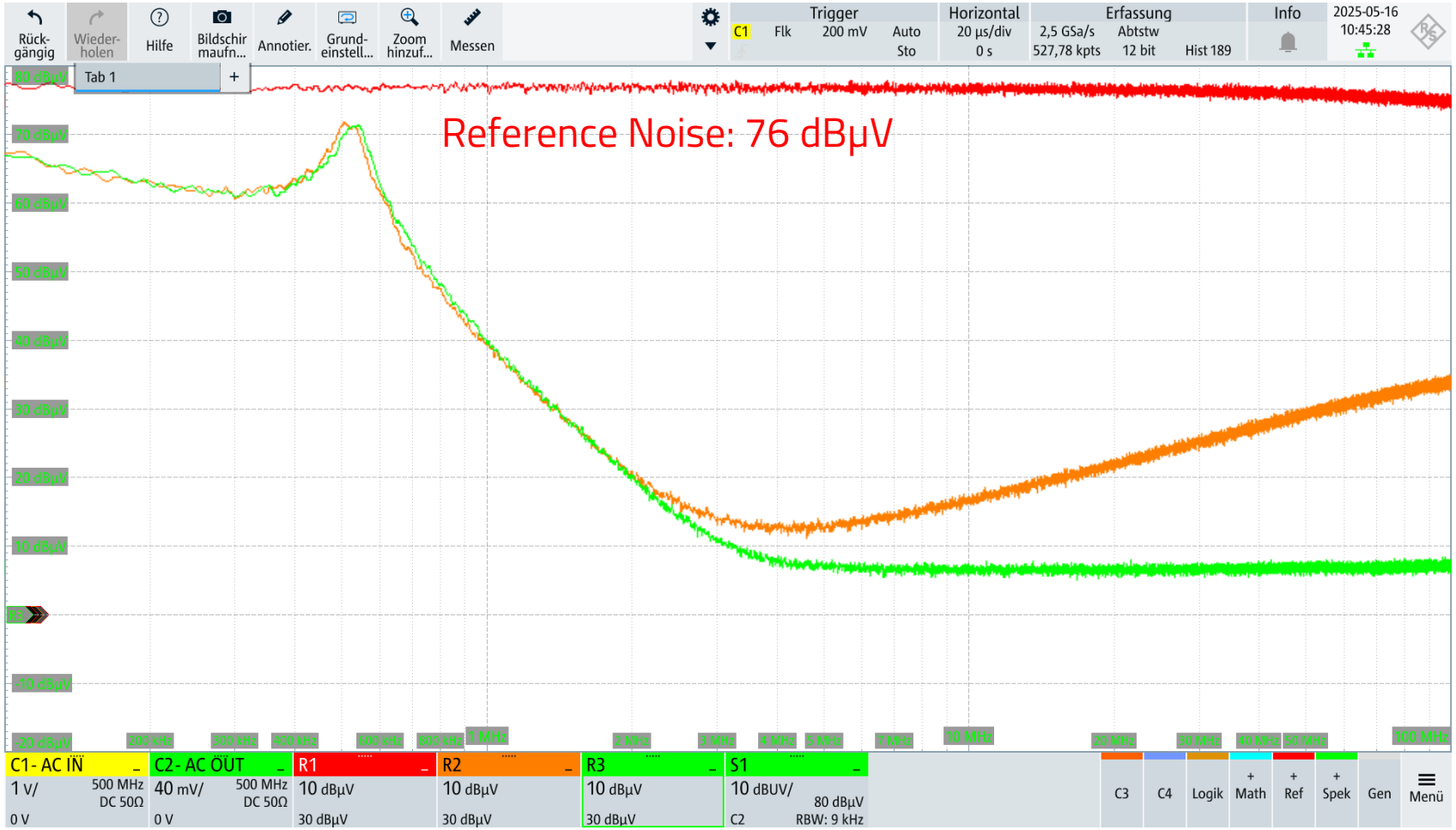
Layout: Influence on Insertion Loss, Oscilloscope Measurement



0805, Bad Layout

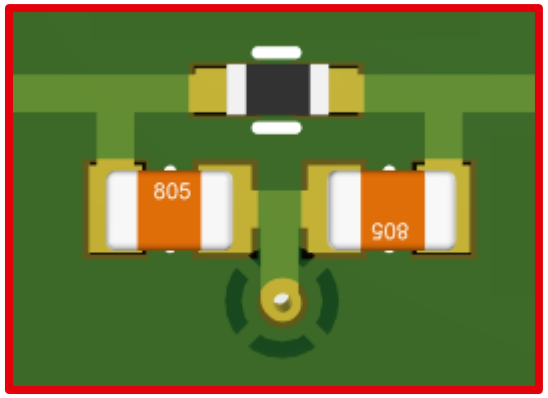


0805, Good Layout

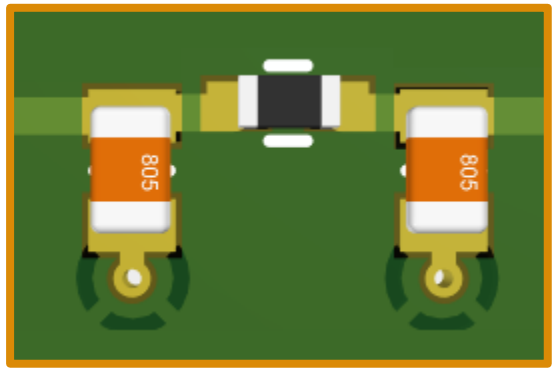


Filter Arrangement

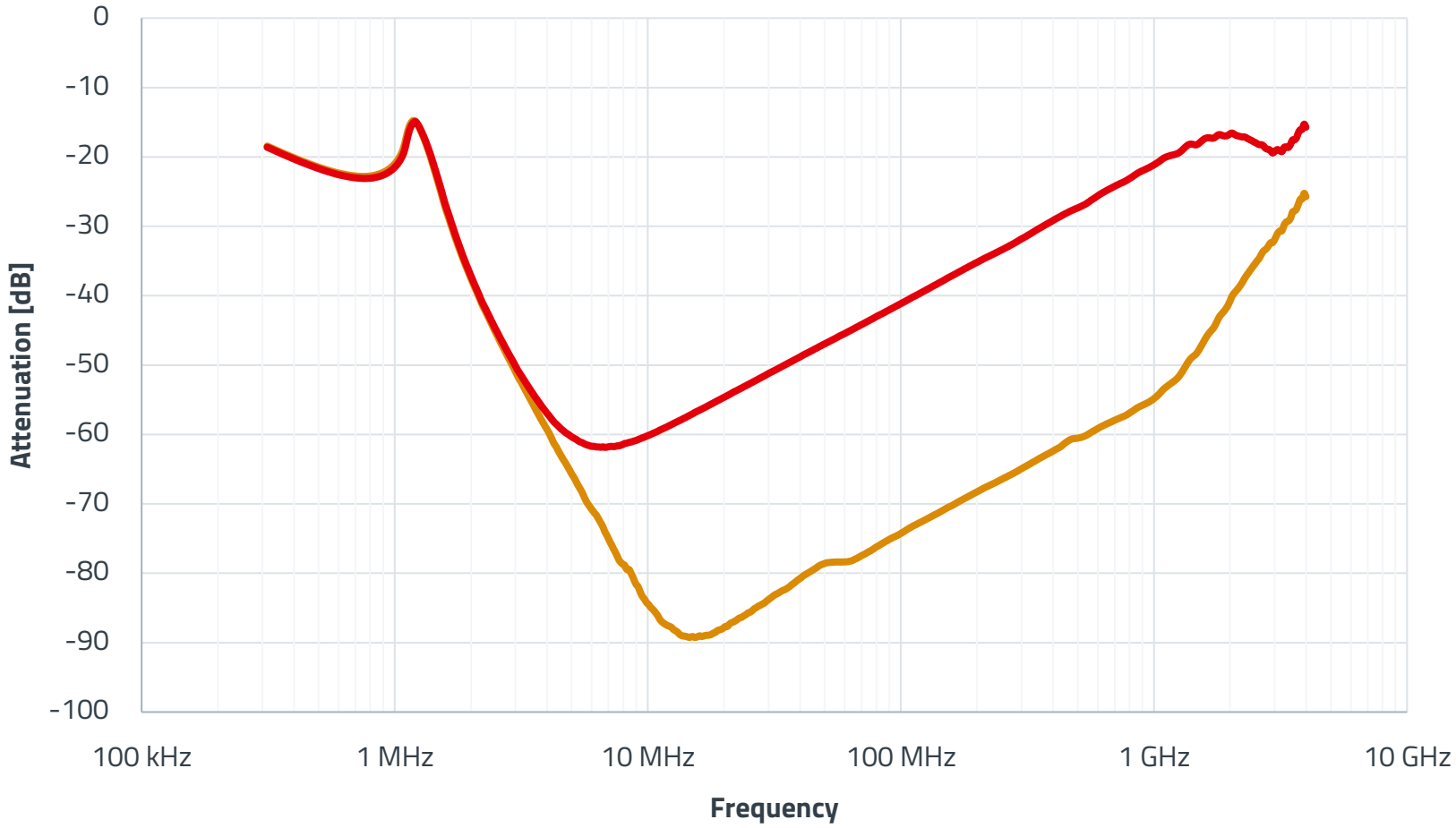
Layout: Influence on Insertion Loss



0805, Bad Layout

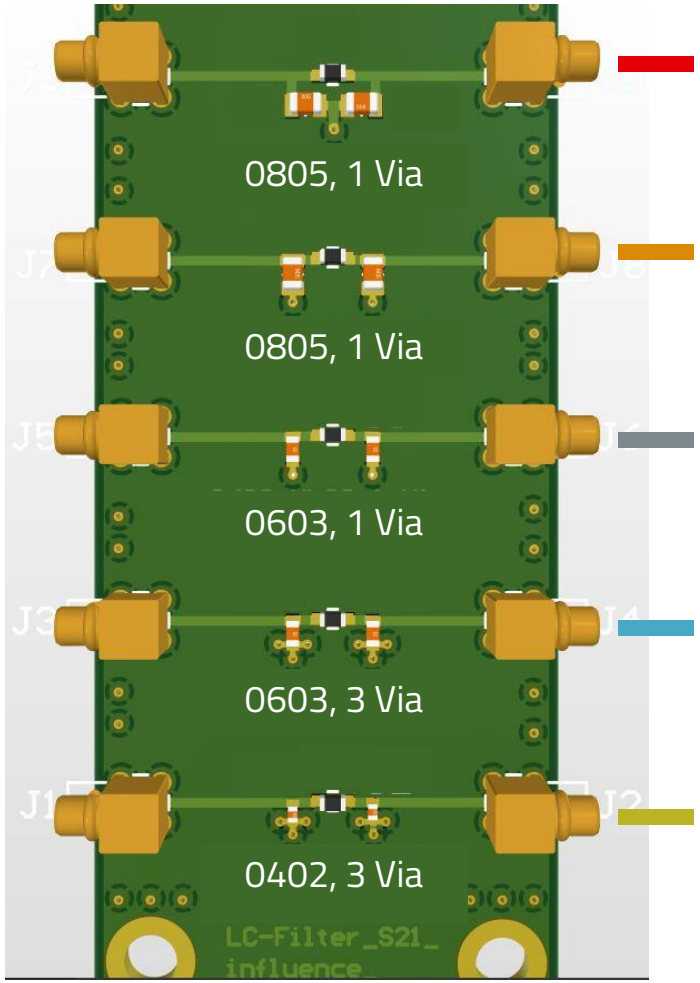


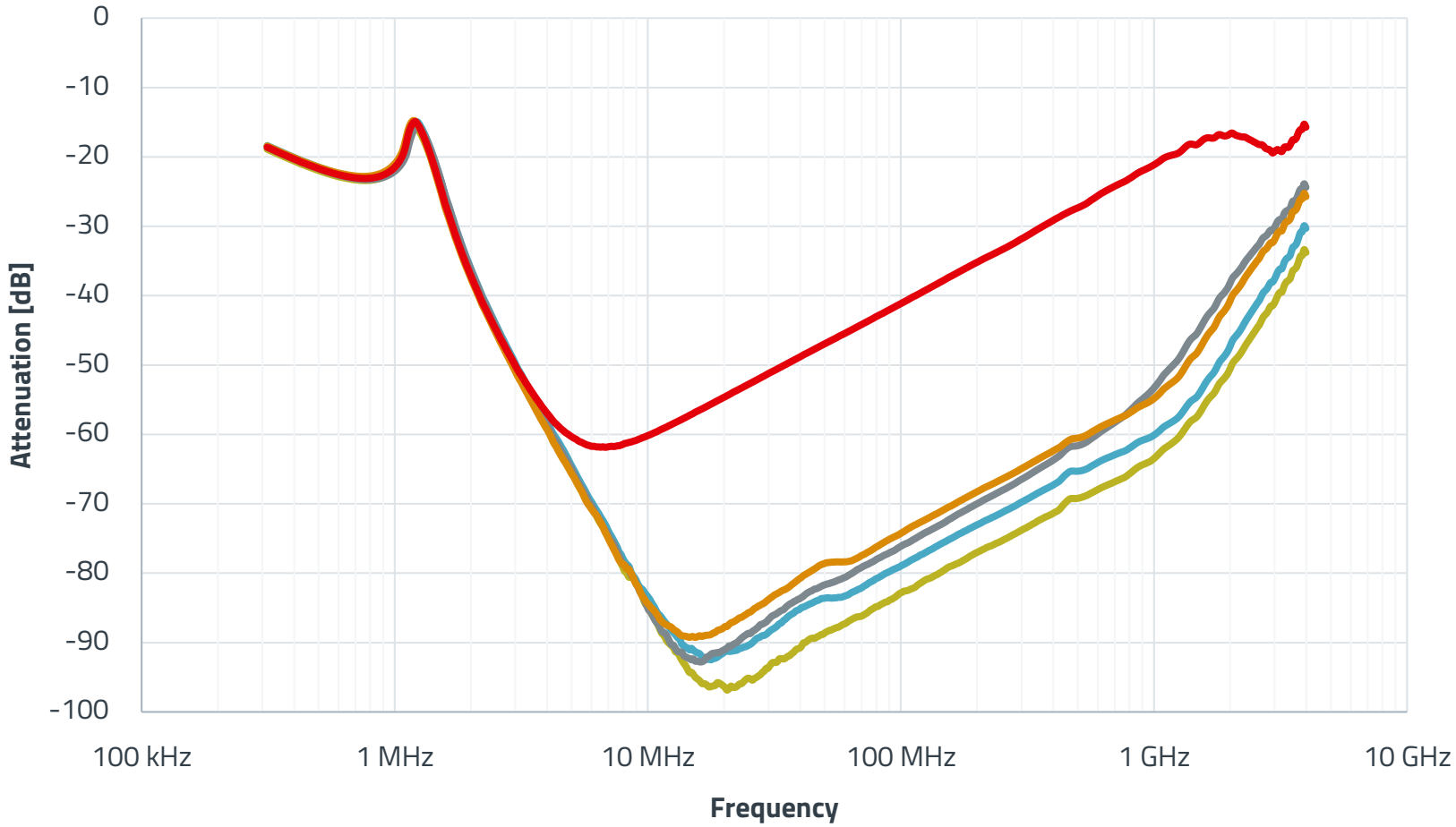
0805, Good Layout



Filter Arrangement

Size and Via Count: Influence on Insertion Loss

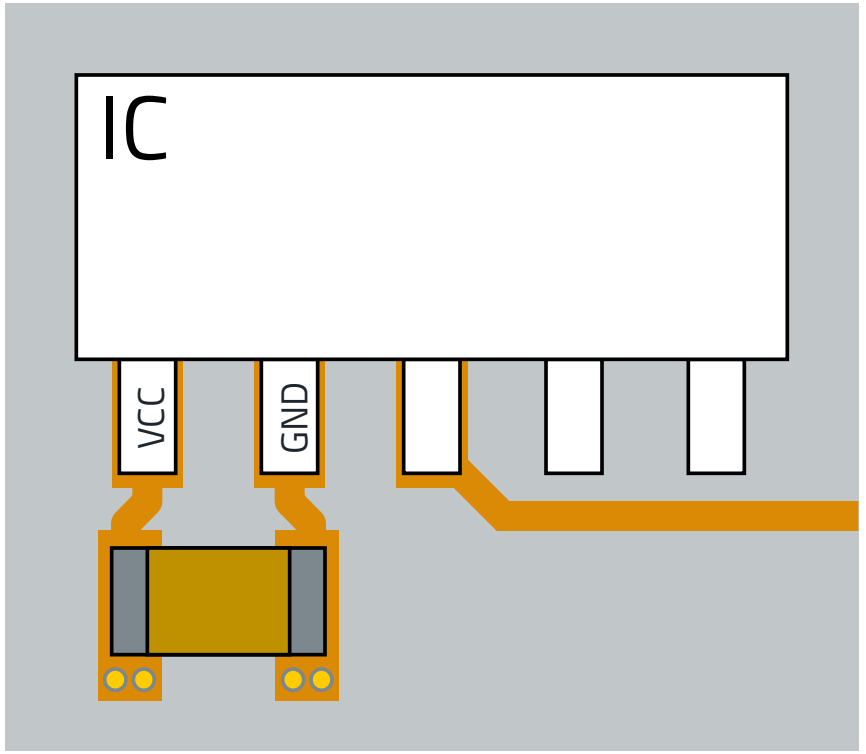




Blocking Capacitors

Routing to Ground and Supply Pins

- RF Currents are fed from the Capacitor
  - Vcc/GND Plane only see low frequency currents
  - Keeps magentic loop for RF as small as possible
  - Distance of Cap to PIN ≤ 0,3mm
- Low impedance connection to the capacitor
  - Keep lines symmetrical (if possible)
- Parallel Vias reduce impedance to GND/Vcc planes



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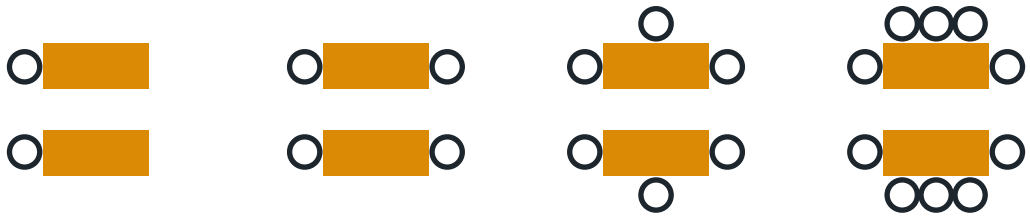
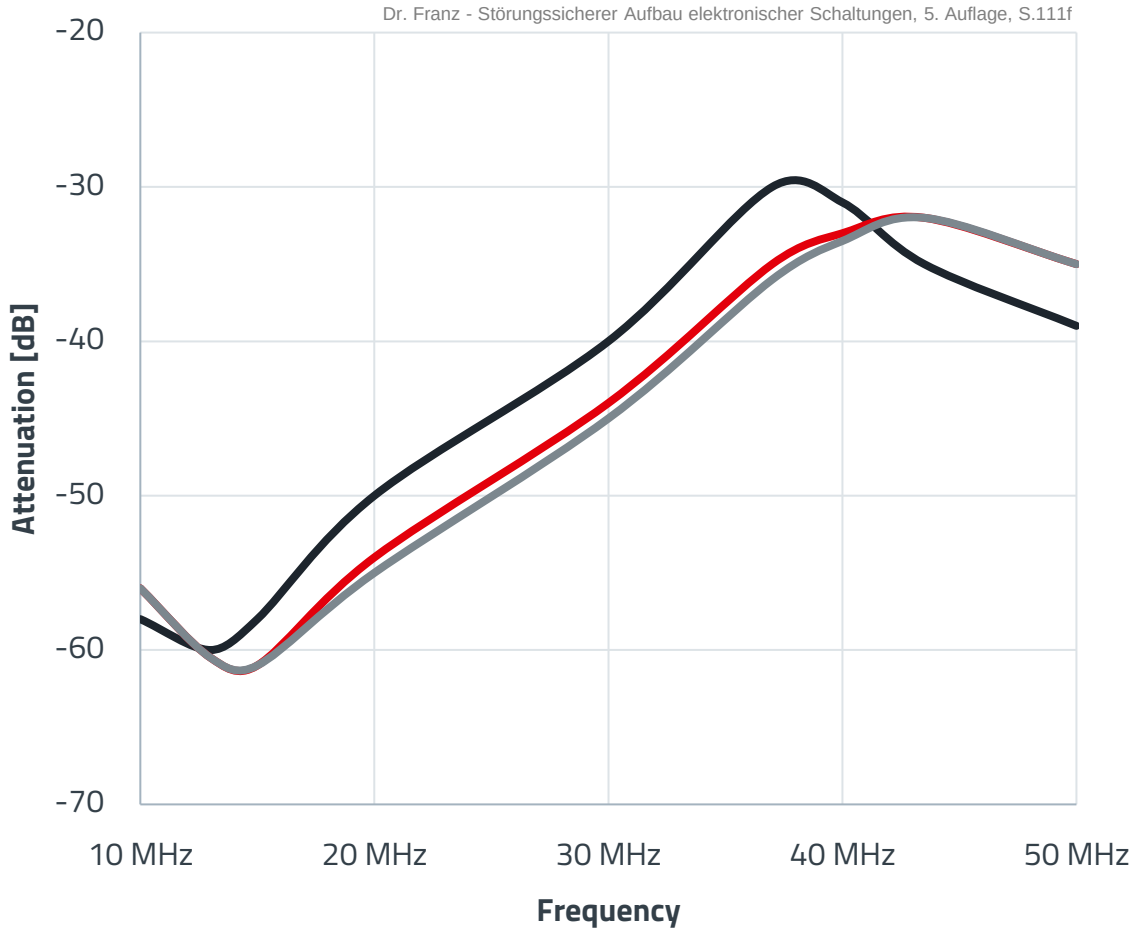
Simulation Einfügedämpfung über Frequenz

Via Anzahl

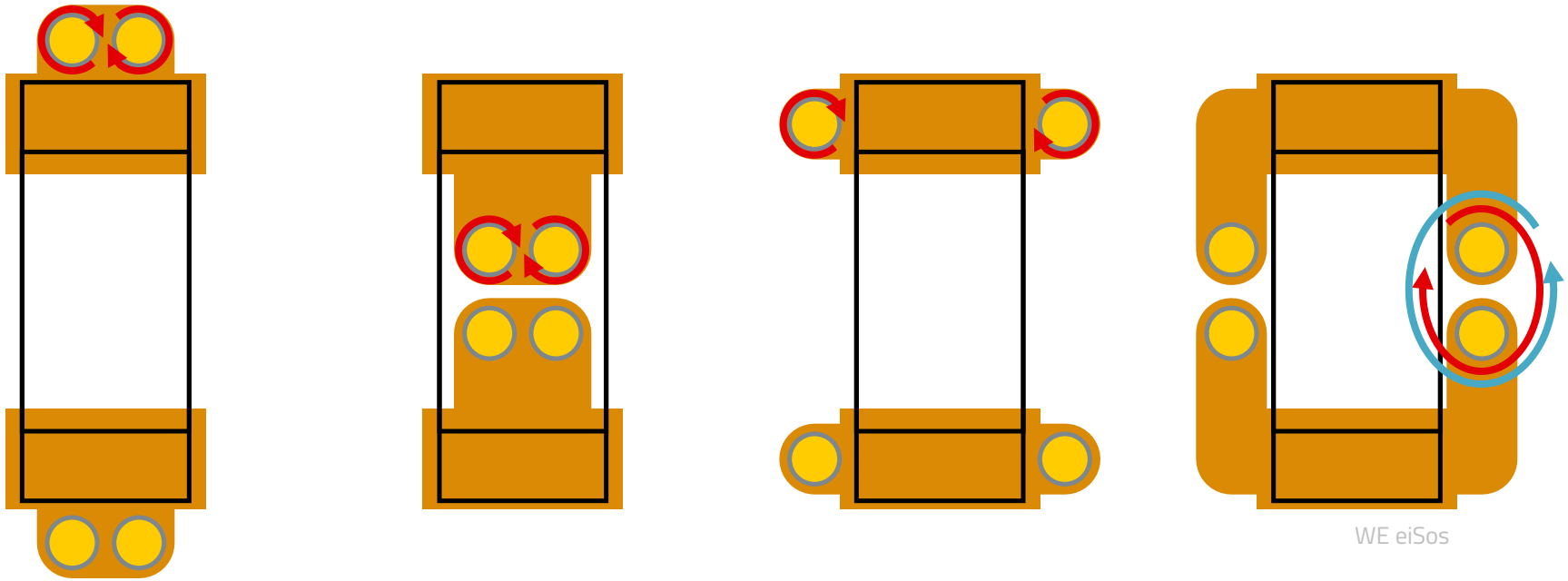
Anzahl	L / nH	ΔL / %
1	1,538	-
2	1,240	-19,4
3	1,176	-23,5
5	1,171	-23,9





Parallel Vias

Discussion: Arrangement of Vias



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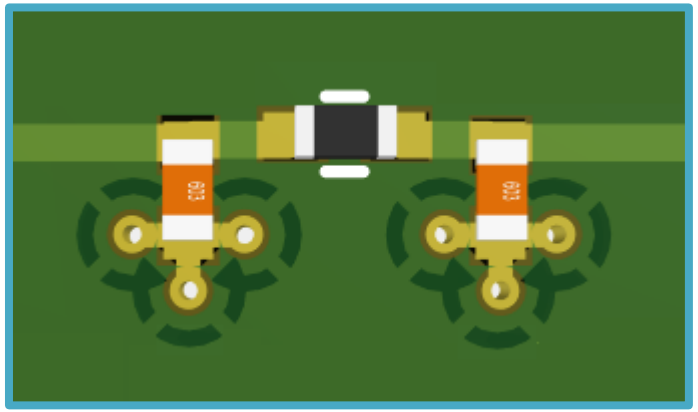
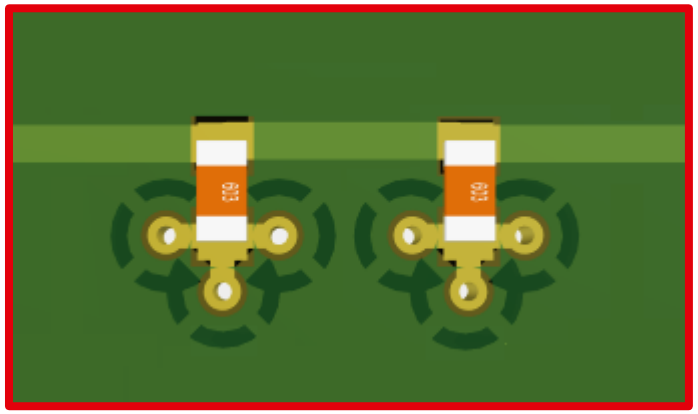
What is the best way to arrange Vias (theoretically) ?

Filter Arrangement

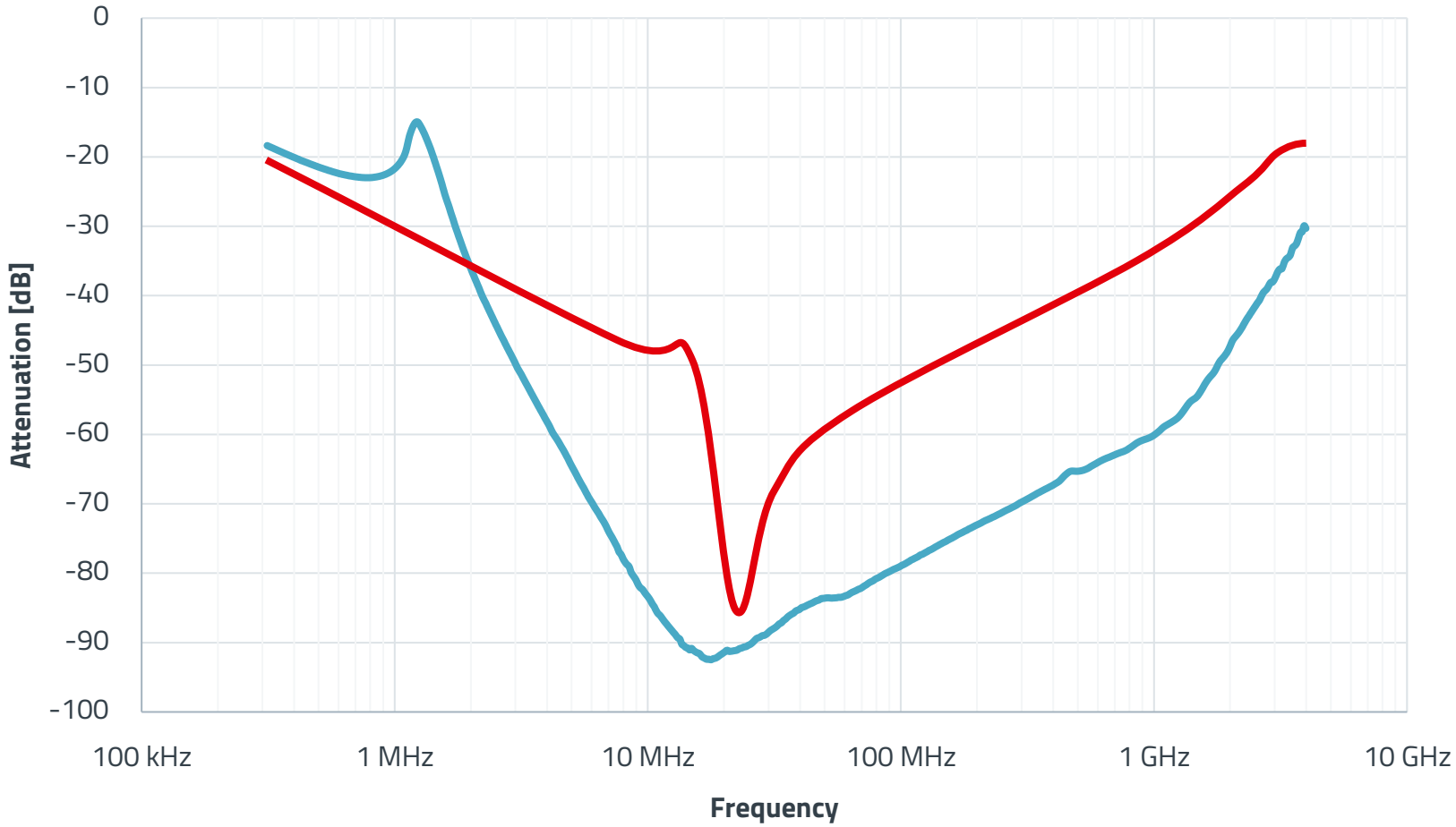
Caps vs. T-Filter: Influence on Insertion Loss



0603, with Ferrite



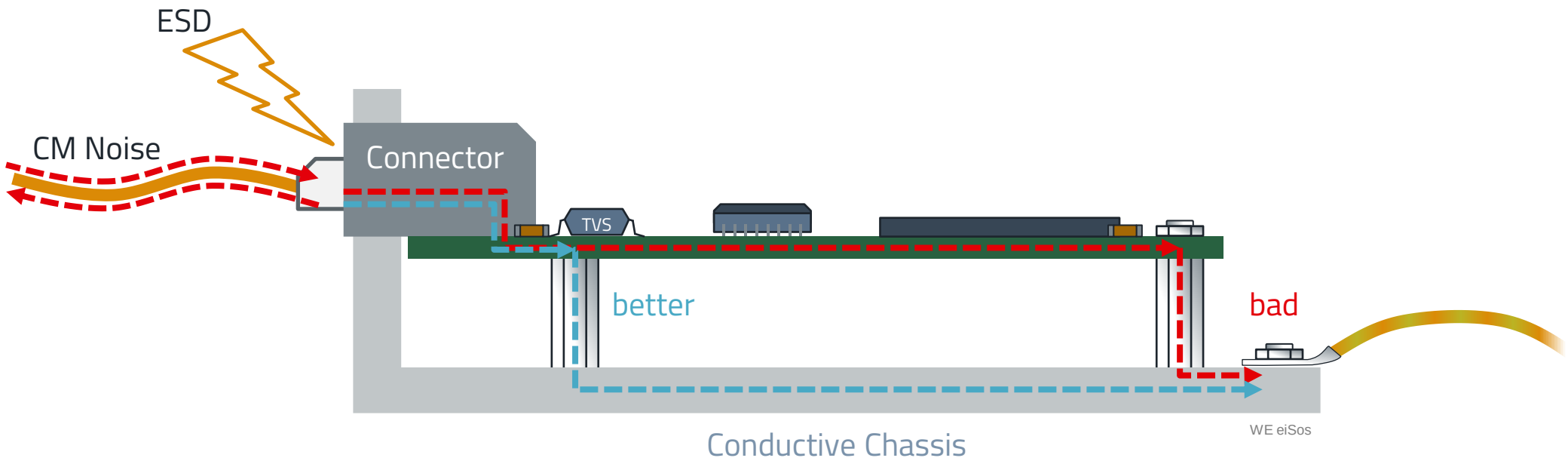
0603, without Ferrite



GROUNDING

Filter Placement

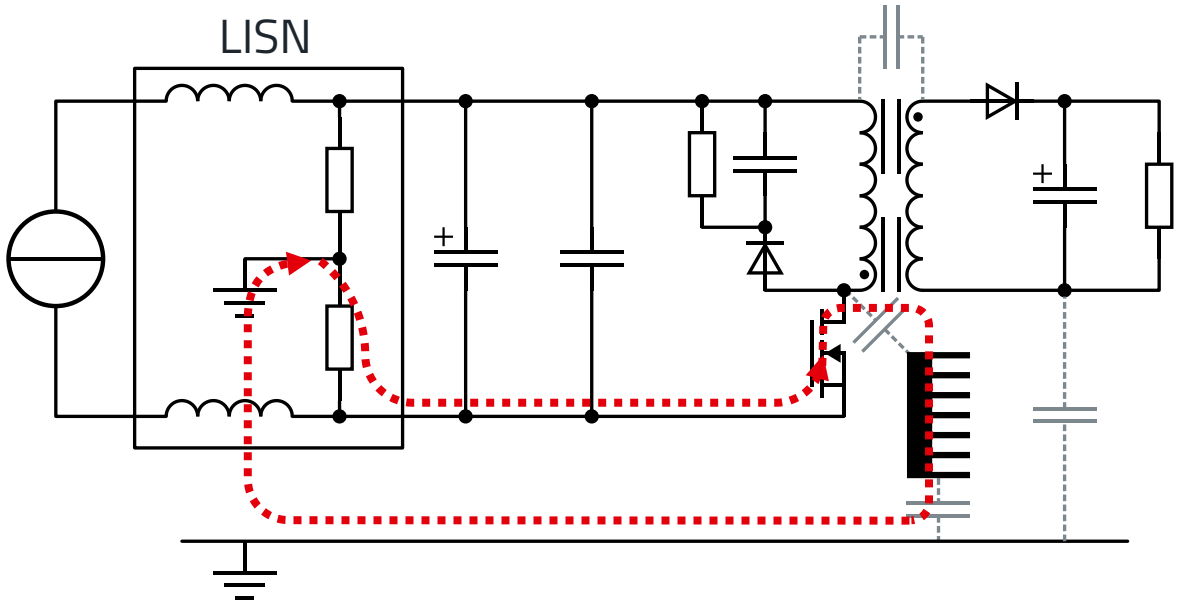
Diverting Noise to Earth



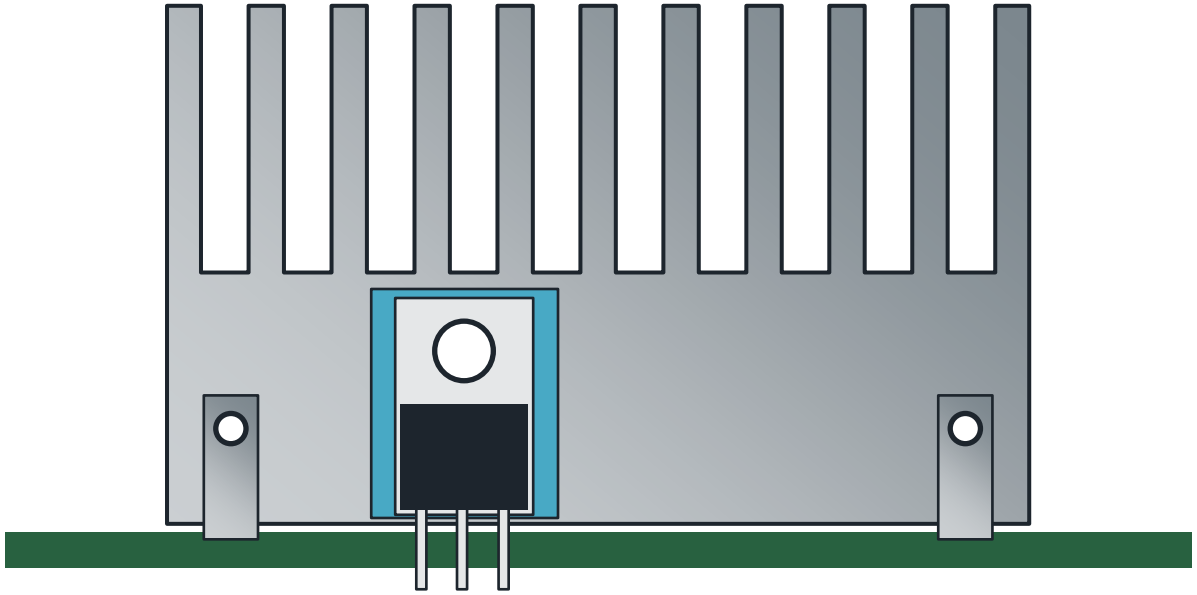
- Grounding studs have to placed so that disturbances don’t affect the electronic parts
- Reference ground for ESD (and common mode noise) is earth potential

Capacitive Coupling over Heatsink

High du/dt common mode currents through parasitic capacitances



Conducted Emissions on a Flyback Converter



Heatsink bonded to reference potential

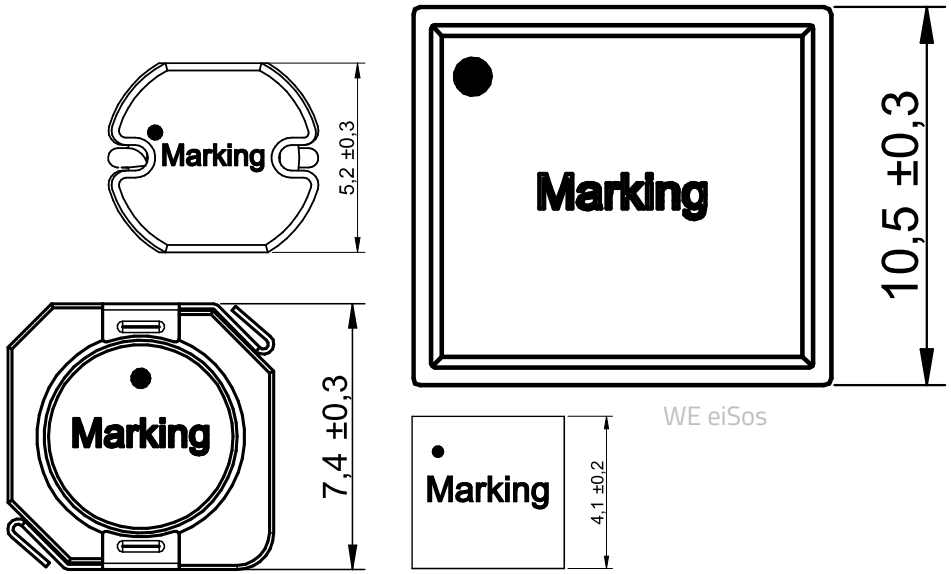
POWER INDUCTORS

Layout Considerations

Orientation of a Power Inductor

Keeping the Hot Node as small as possible

- Power Inductors with more than one layer of windings usually have marking indicating the start of winding
- Start of winding should be facing the Hot Node, so outer winding can act as a self shielding
- Even for Inductors with only one layer, orientation can make a difference (Height of terminal)
- Not every Inductor has a distinct start of winding due to the production process (e.g. Rod Cores)



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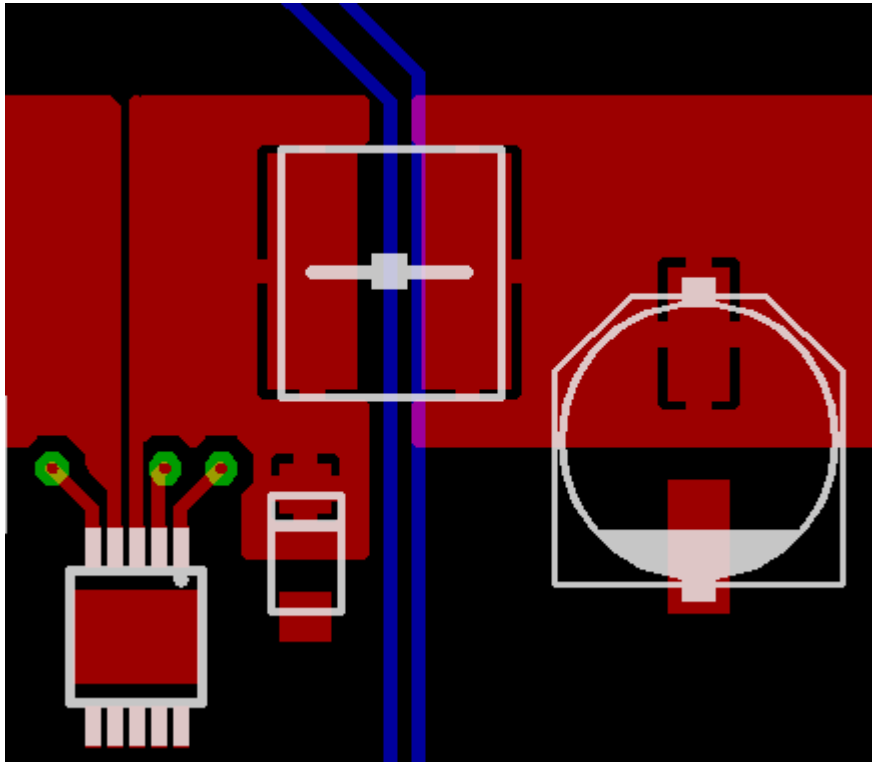
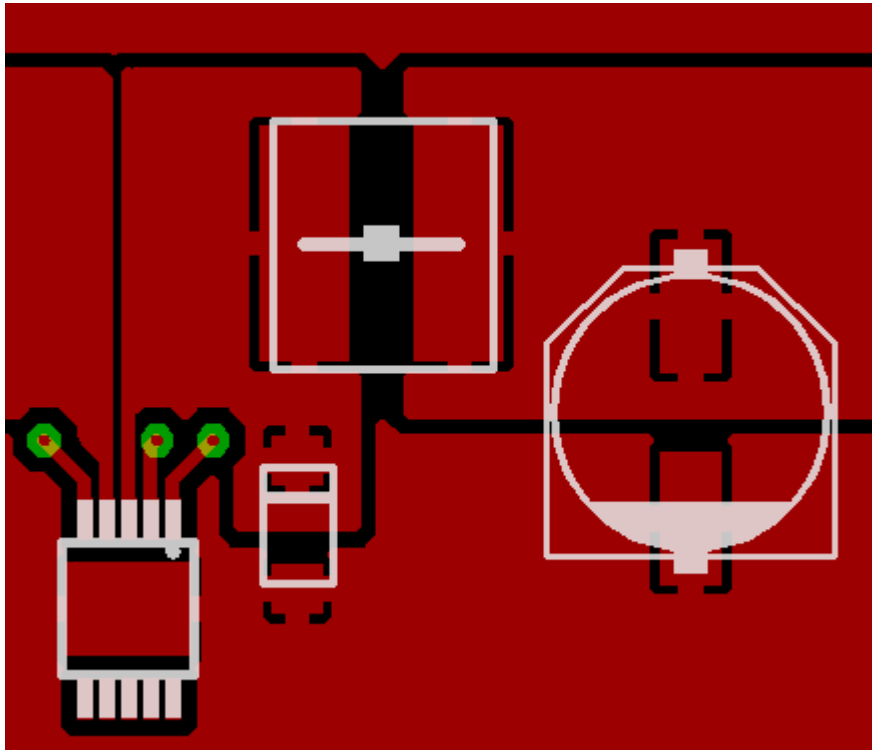
Traces below Power Inductors

Bottom side of Power Inductors is not shielded



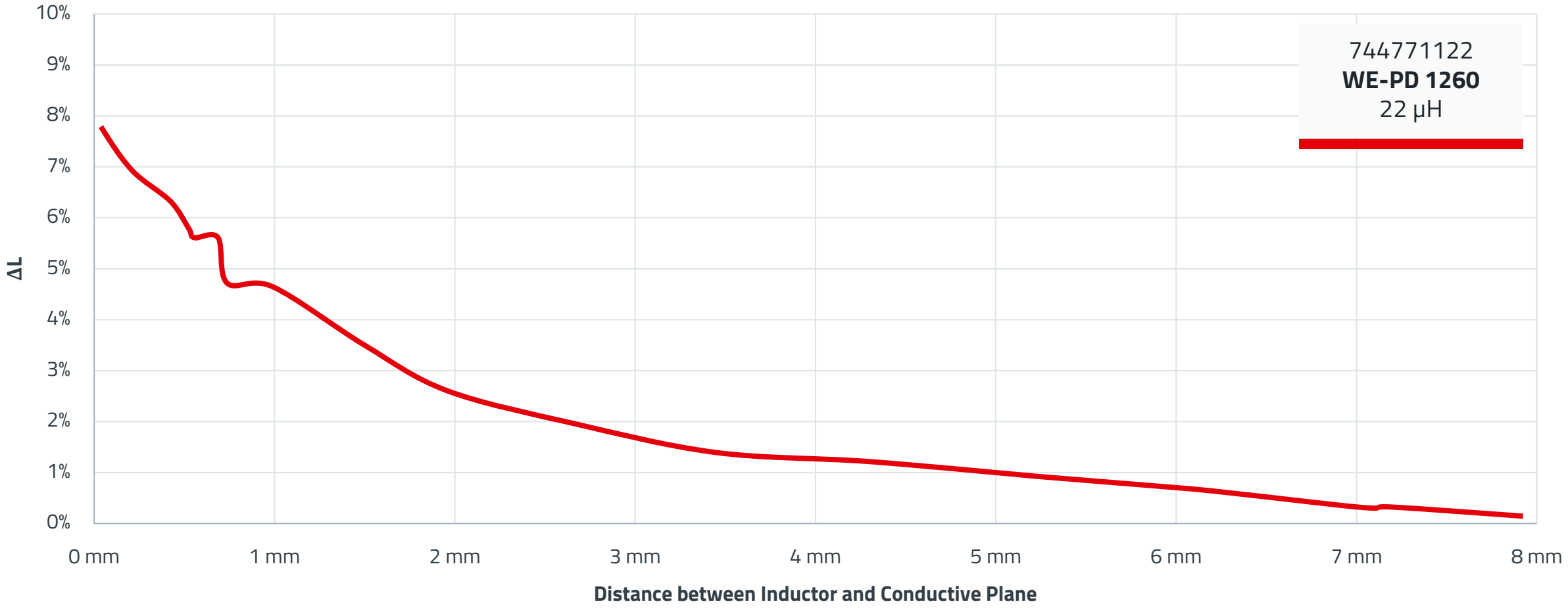
bad



good

Conductive Plane below Power Inductor

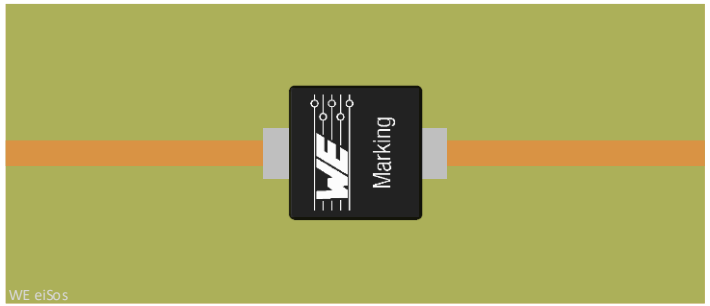
Influence on Inductance



Conductive Plane below Power Inductor

Layout Options

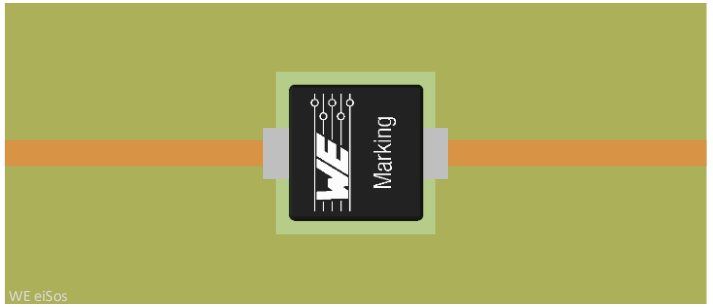
Continuous GND Plane



+ Shielding the electric Near Field

- Eddy Currents affect Inductance

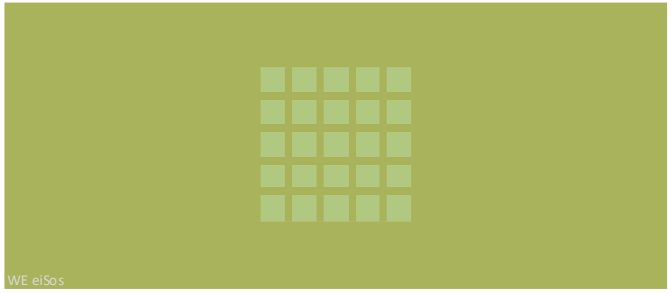
Opening in GND Plane



+ Reduced Eddy Currents

- Radiated Noise through PCB

Tradeoff - GND Grid



+ Reduced Eddy Currents

+ Reduced radiated Noise

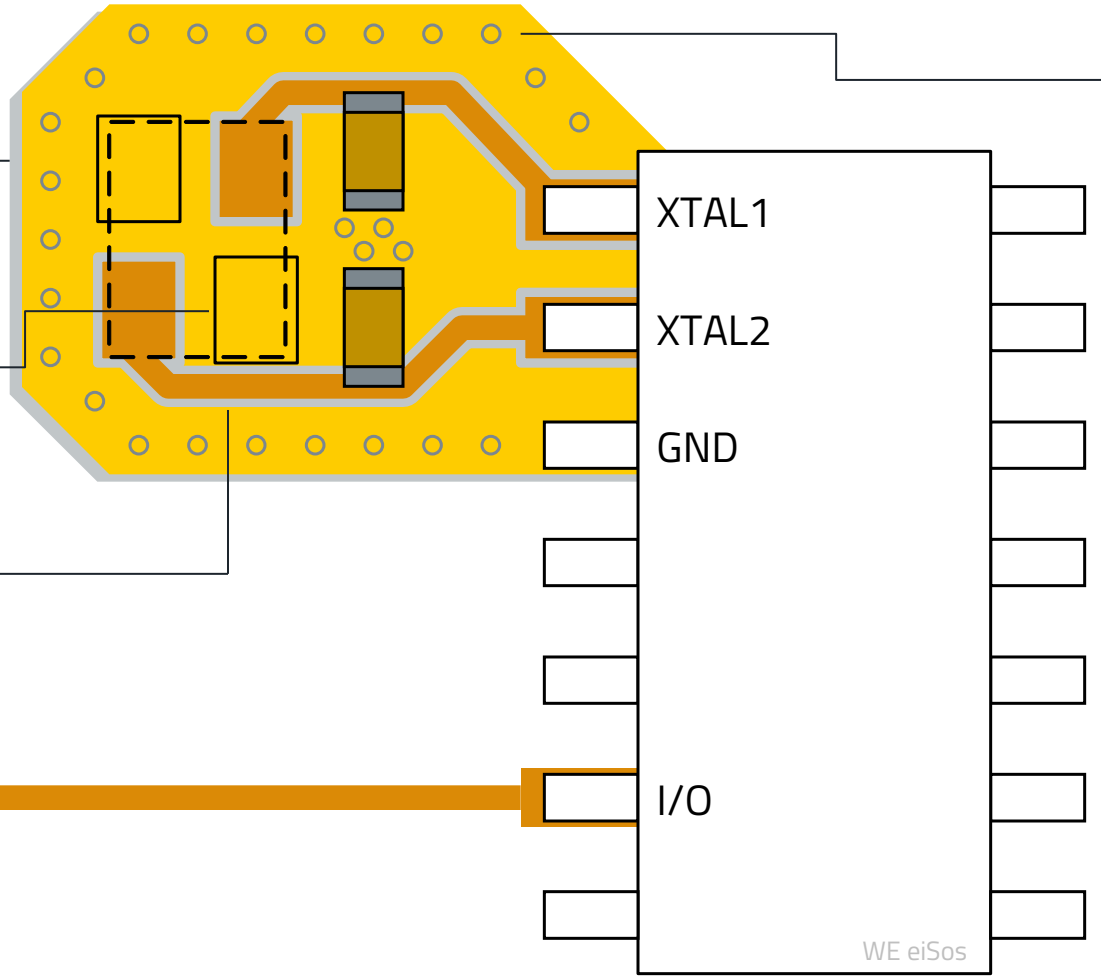
- Increased Layout Efforts

CRYSTALS & OSCILLATORS

Layout Considerations

Quartz Crystals

Layout Considerations



GND Plane under XTAL

Connect **Housing to GND**

No Vias on Crystal trace

Critical Signals as far away as possible

Via Fence around Crystal Circuitry

Load Capacitors: Low Leakage, stable over temperature (NP0)

Crystal as close as possible to IC

No stubs, No loops

Crystal Oscillators

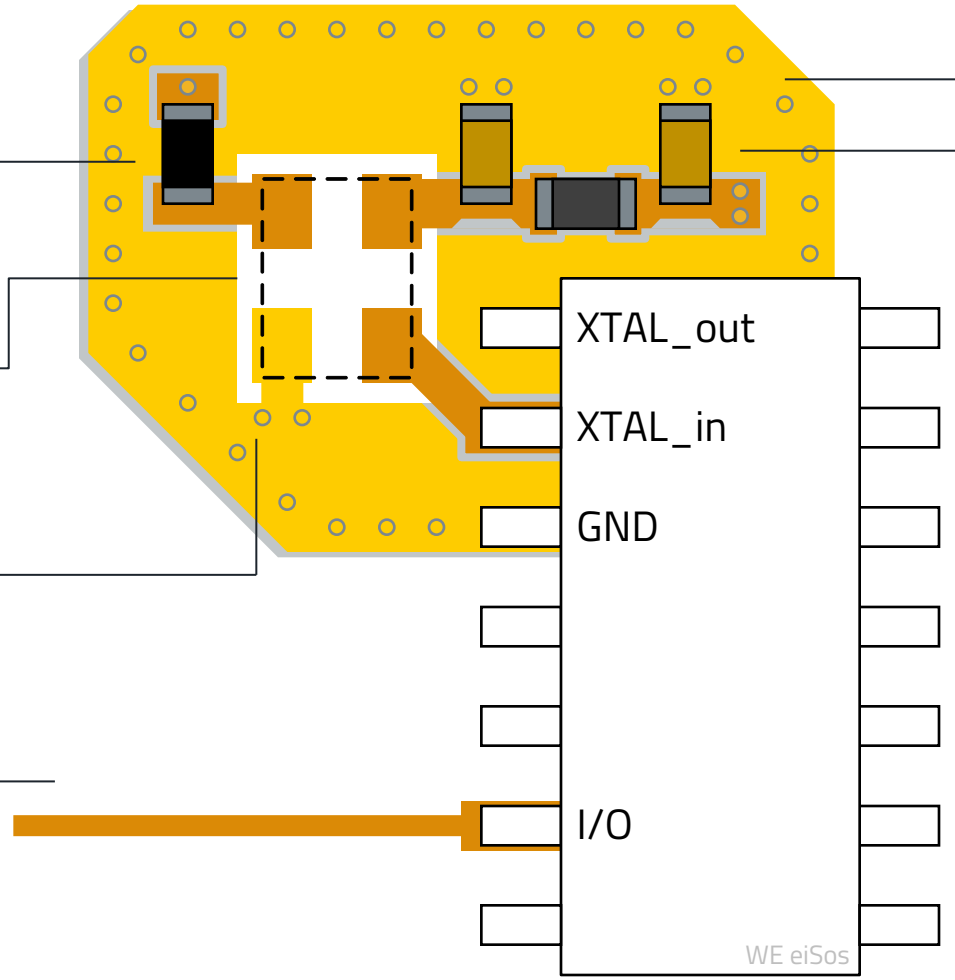
Layout Considerations

100kΩ Pull-Up
if EN is not required

Cut Out GND Plane
under Oscillator

Via to shorten GND Path

Critical Signals as far away as possible



Via Fence around Crystal Circuitry

π-Filter for **RF Decoupling** of Supply Voltage

Keep **RF Lines** as short as possible

No Layer Jumps on RF Lines

π-Filter for RF Decoupling

For Crystal Oscillators @ 50MHz