EFFICIENT EMI FILTERING OF COMMON AND DIFFERENTIAL MODE NOISE

Lorandt Fölkel M.Eng.
FAE & BDM at Würth Elektronik eiSos

LET'S START WITH QUESTIONS

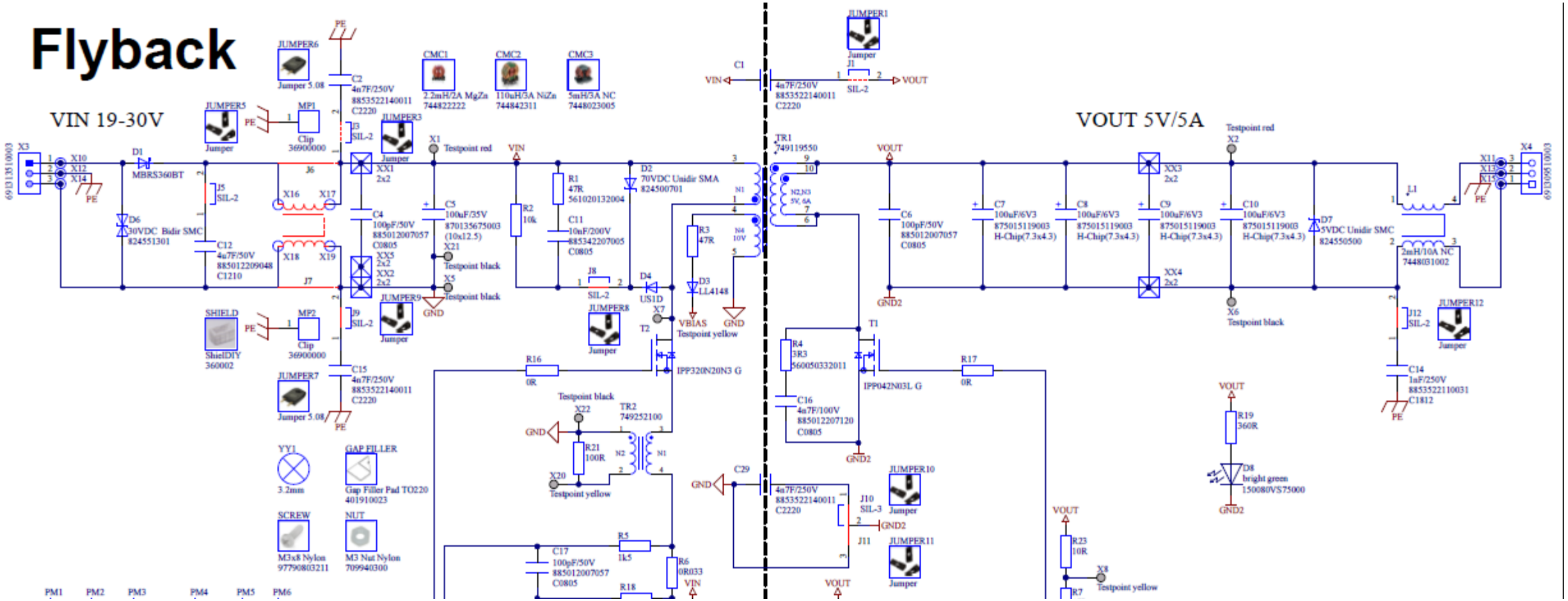
- Do you think that …

  … a DC/DC converter can "*generate Conducted Emission*"?

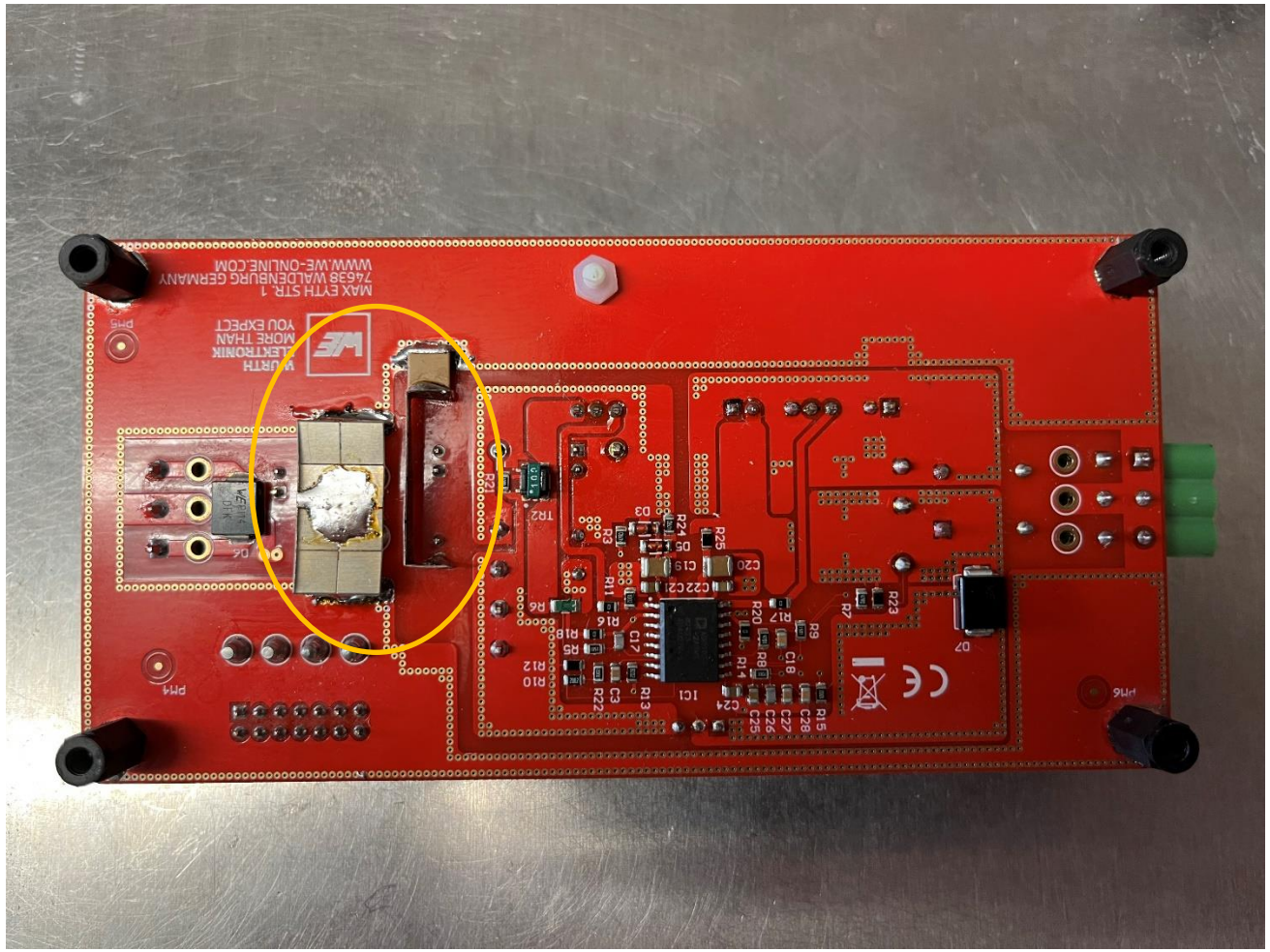
  … the EMC of a DC/DC converter is *"affected only from the PCB layout"*???

  … with an *"oscilloscope you could solve all EMI situations"*???

FLYBACK EMI - SCHEMATIC- V2022.1

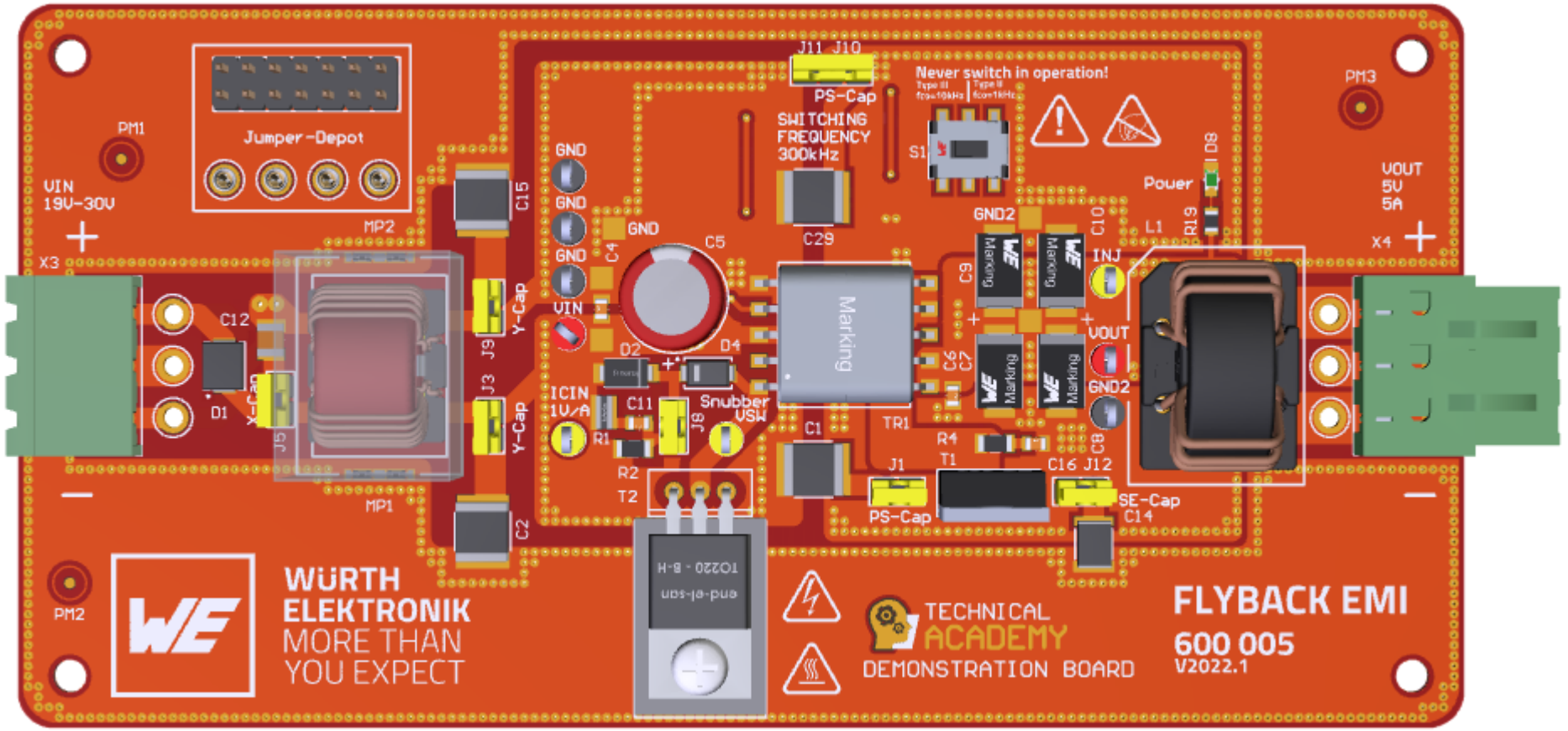


FLYBACK EMI - DEMONSTRATION BOARD - V2022.1 - MODIFICATION



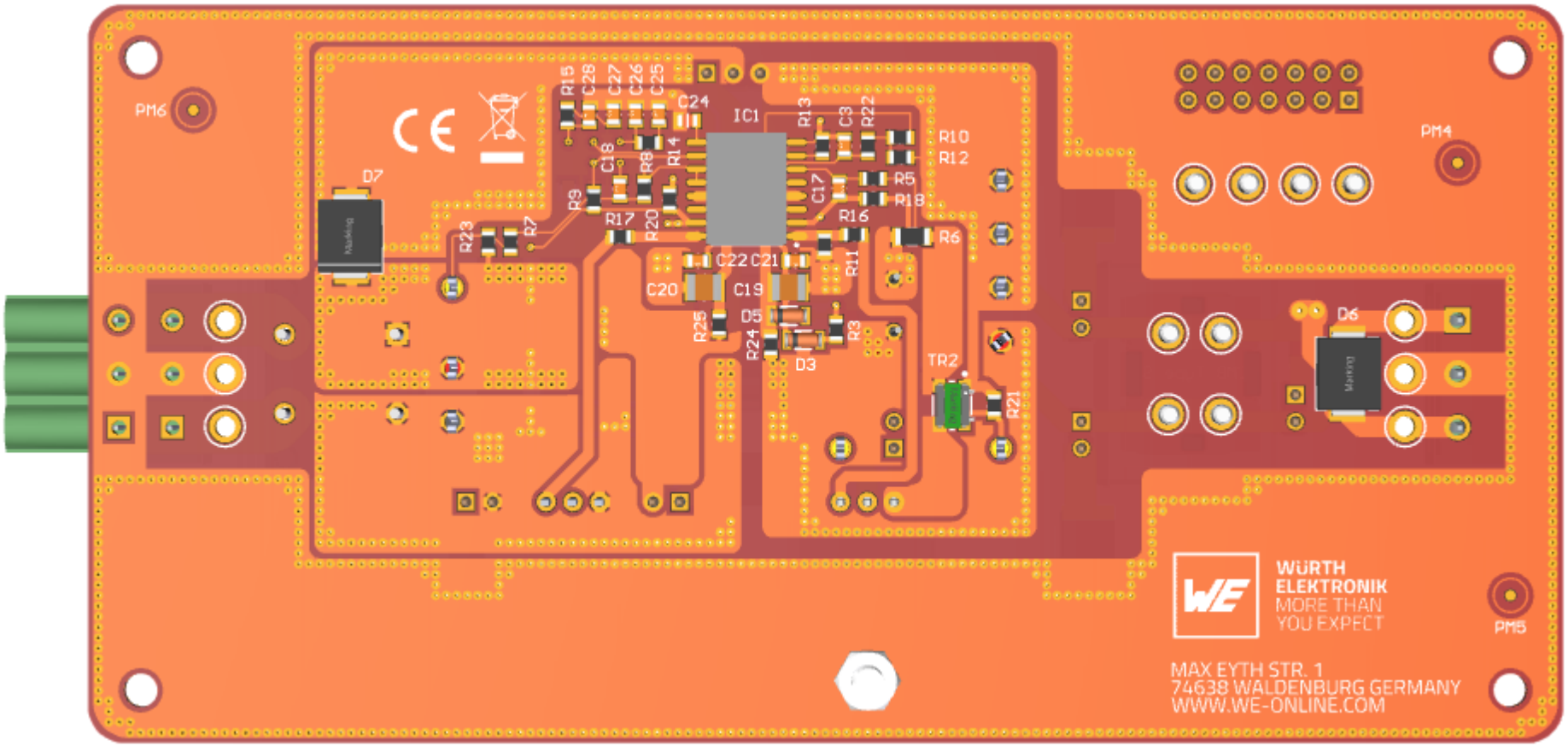
FLYBACK EMI - DEMONSTRATION BOARD - V2022.1

Top

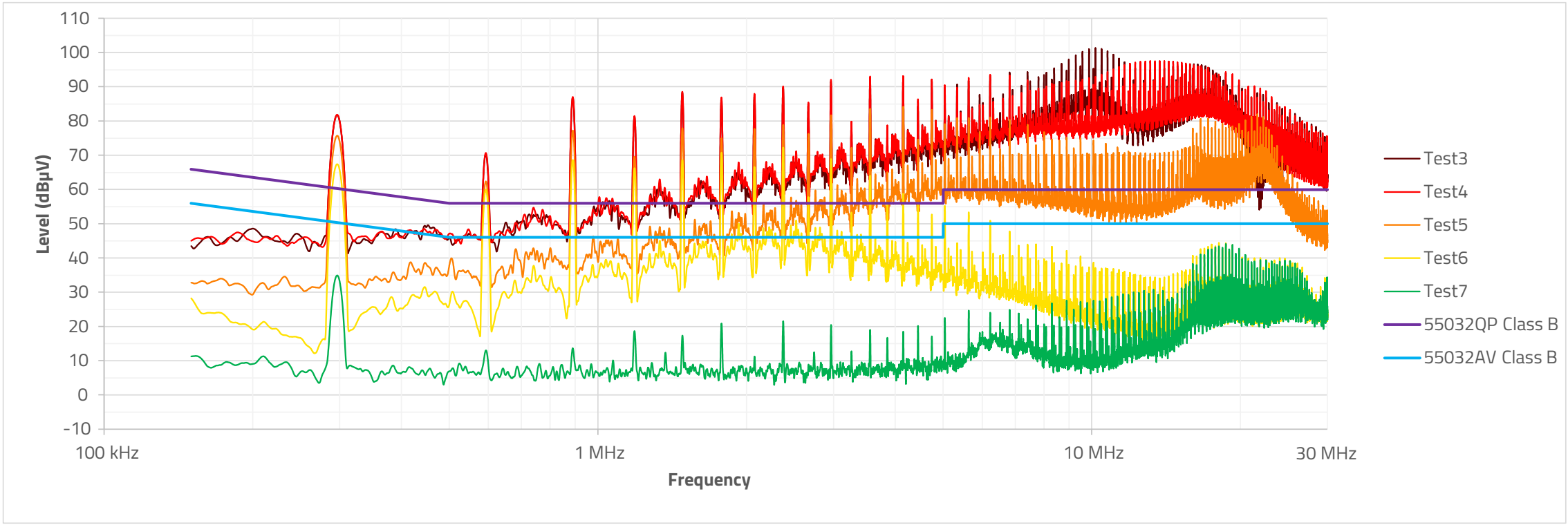


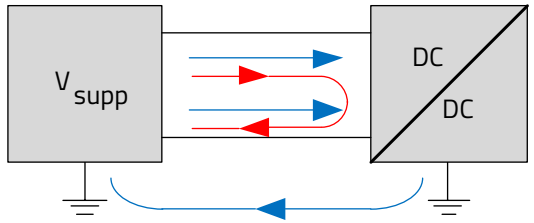
FLYBACK EMI - DEMONSTRATION BOARD - V2022.1

Bottom



TEST#3-7: V2022.1 WITH MODIFICATION - TOTAL CONDUCTED EMISSIONS - LINE

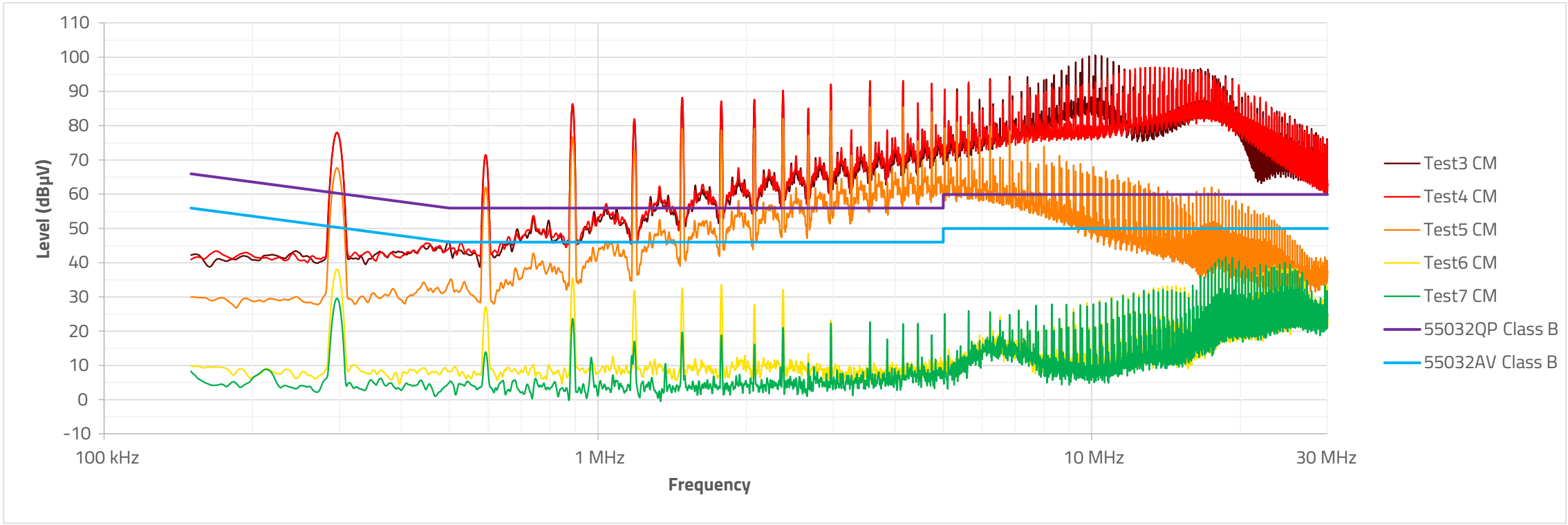


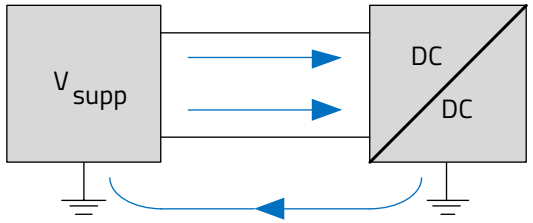


Combined

Namec	Description
Test#3	Reference (no improvement)
Test#4	Test#3 + RCD-snubber
Test#5	Test#4 + primary to secondary y-capacitors
Test#6	Test#5 + CMC and y-capacitors (CM filter)
Test#7	Test#6 + x-capacitor (DM filter)

TEST#3-7: V2022.1 WITH MODIFICATION - CONDUCTED EMISSIONS - COMMON MODE

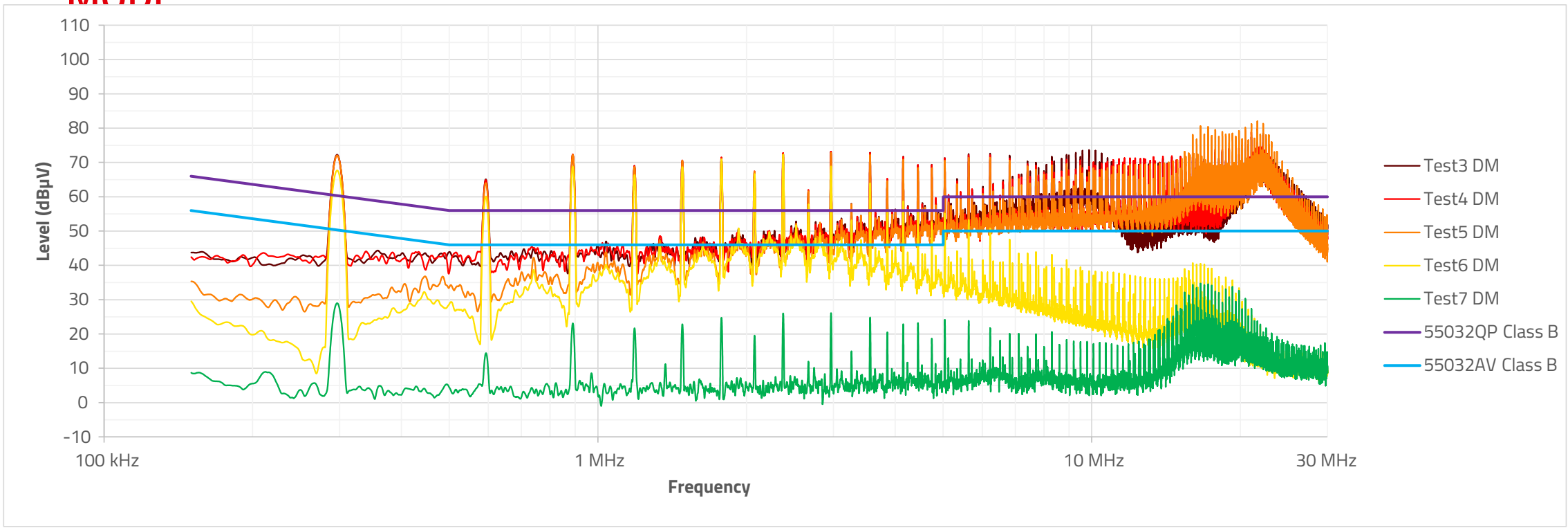


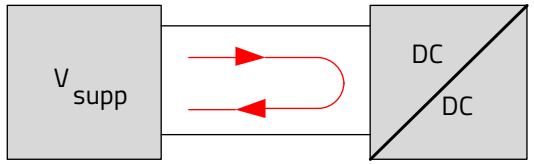


Common Mode

Name	Description
Test#3	Reference (no improvement)
Test#4	Test#3 + RCD-snubber
Test#5	Test#4 + primary to secondary y-capacitors
Test#6	Test#5 + CMC and y-capacitors (CM filter)
Test#7	Test#6 + x-capacitor (DM filter)

TEST#3-7: V2022.1 WITH MODIFICATION - CONDUCTED EMISSIONS - DIFFERENTIAL MODE



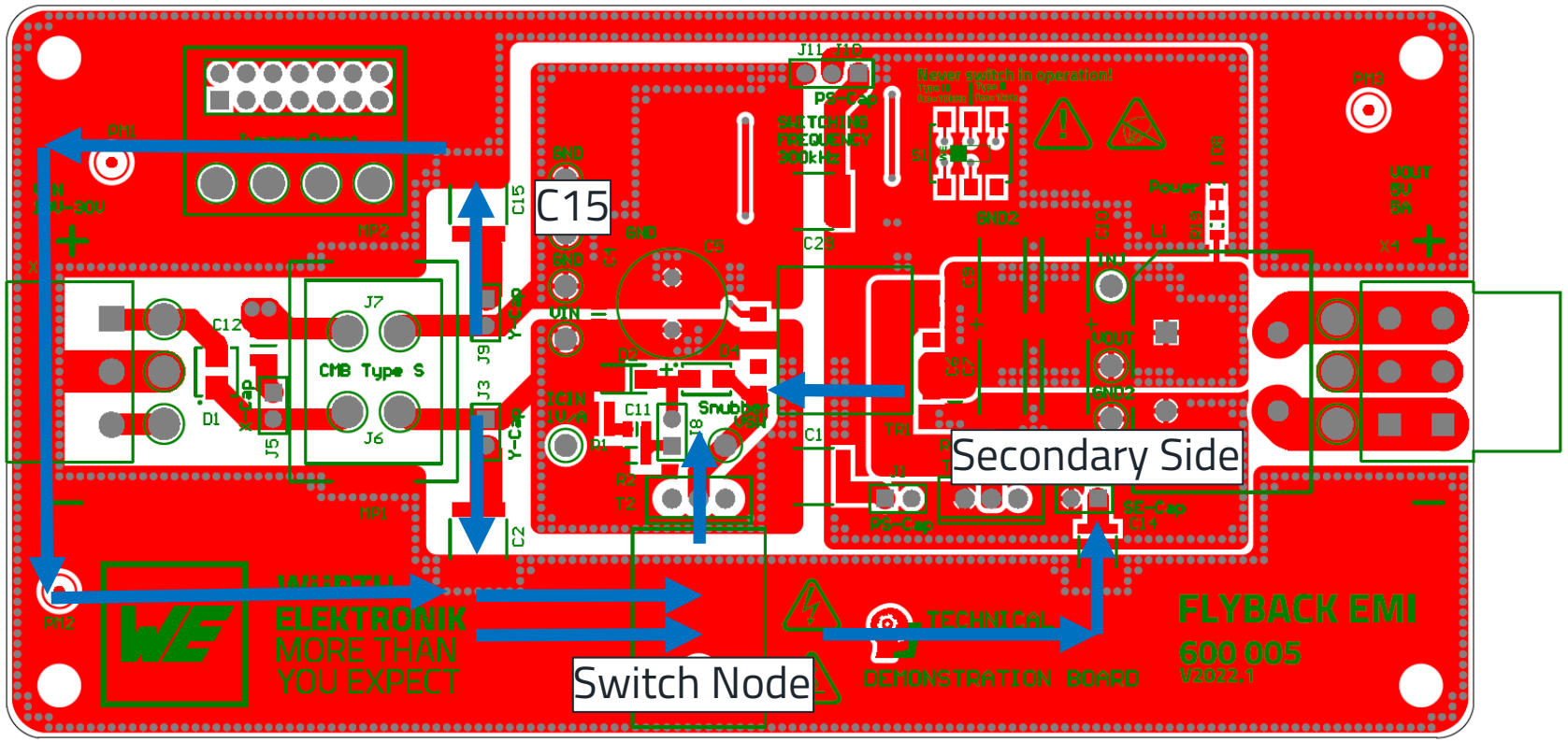


Differential Mode

Name	Description
Test#3	Reference (no improvement)
Test#4	Test#3 + RCD-snubber
Test#5	Test#4 + primary to secondary y-capacitors
Test#6	Test#5 + CMC and y-capacitors (CM filter)
Test#7	Test#6 + x-capacitor (DM filter)

FLYBACK EMI - DEMONSTRATION BOARD - V2022.1 - MODIFICATION

Background

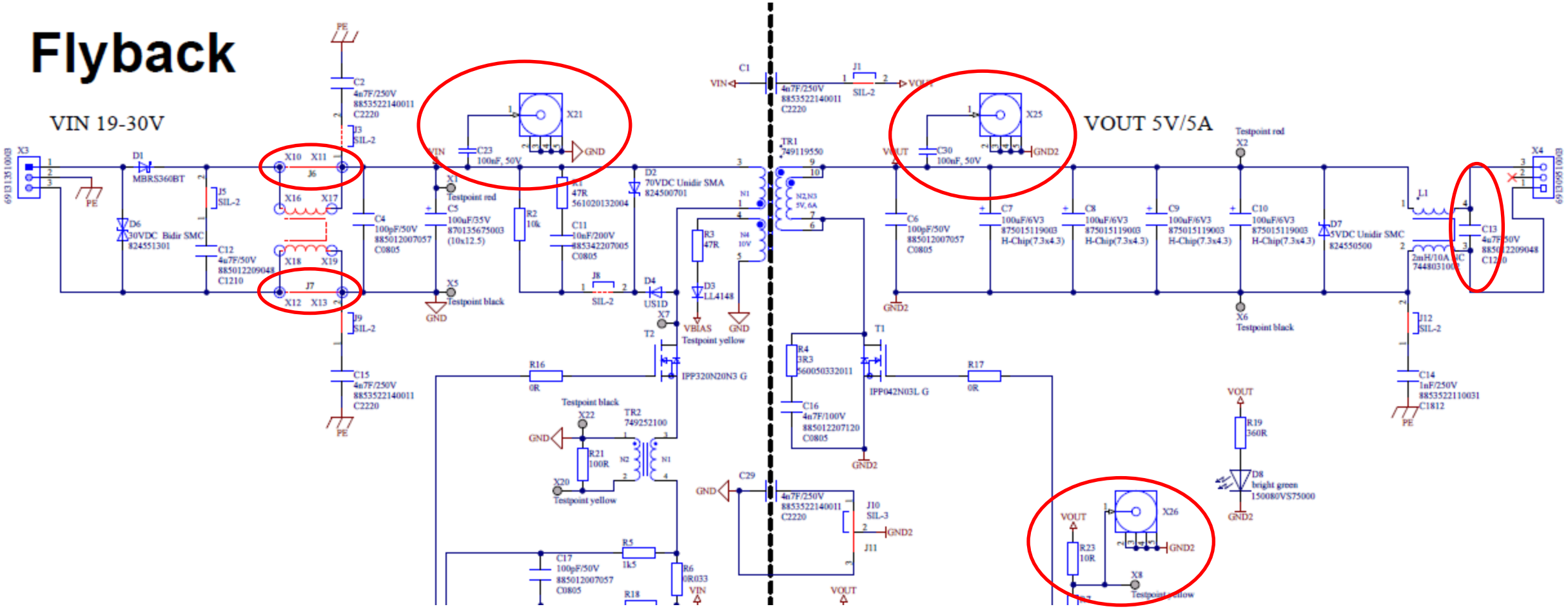


There is no short noise return path from y-capacitor C15 to CM-Noise Source (Switch node, secondary side)

CM-noise bypasses the filter and couples into the filter (parasitic loop antenna)

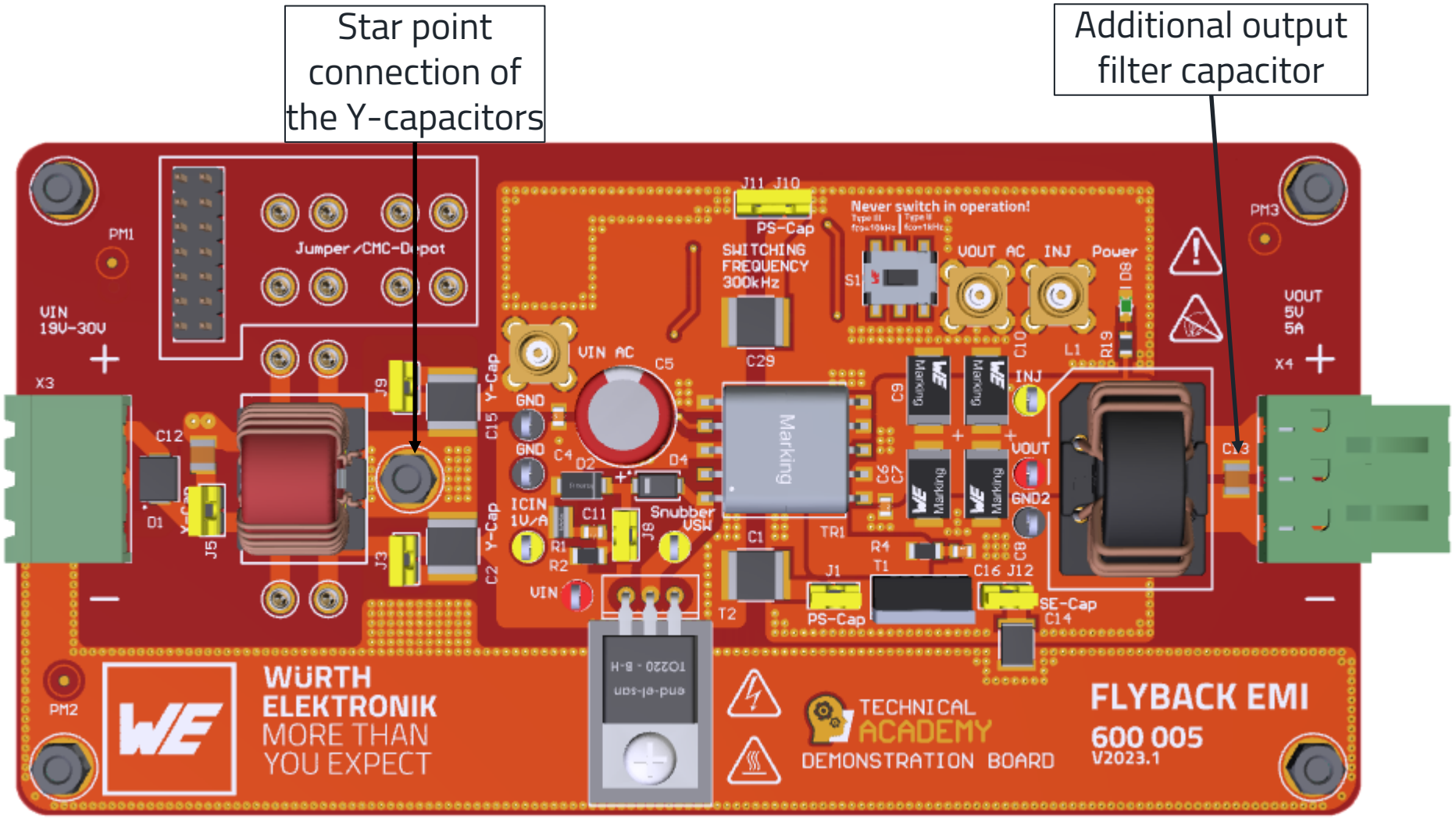
CM noise imbalance occurs (CM/DM conversion)

FLYBACK EMI - SCHEMATIC- V2023.1



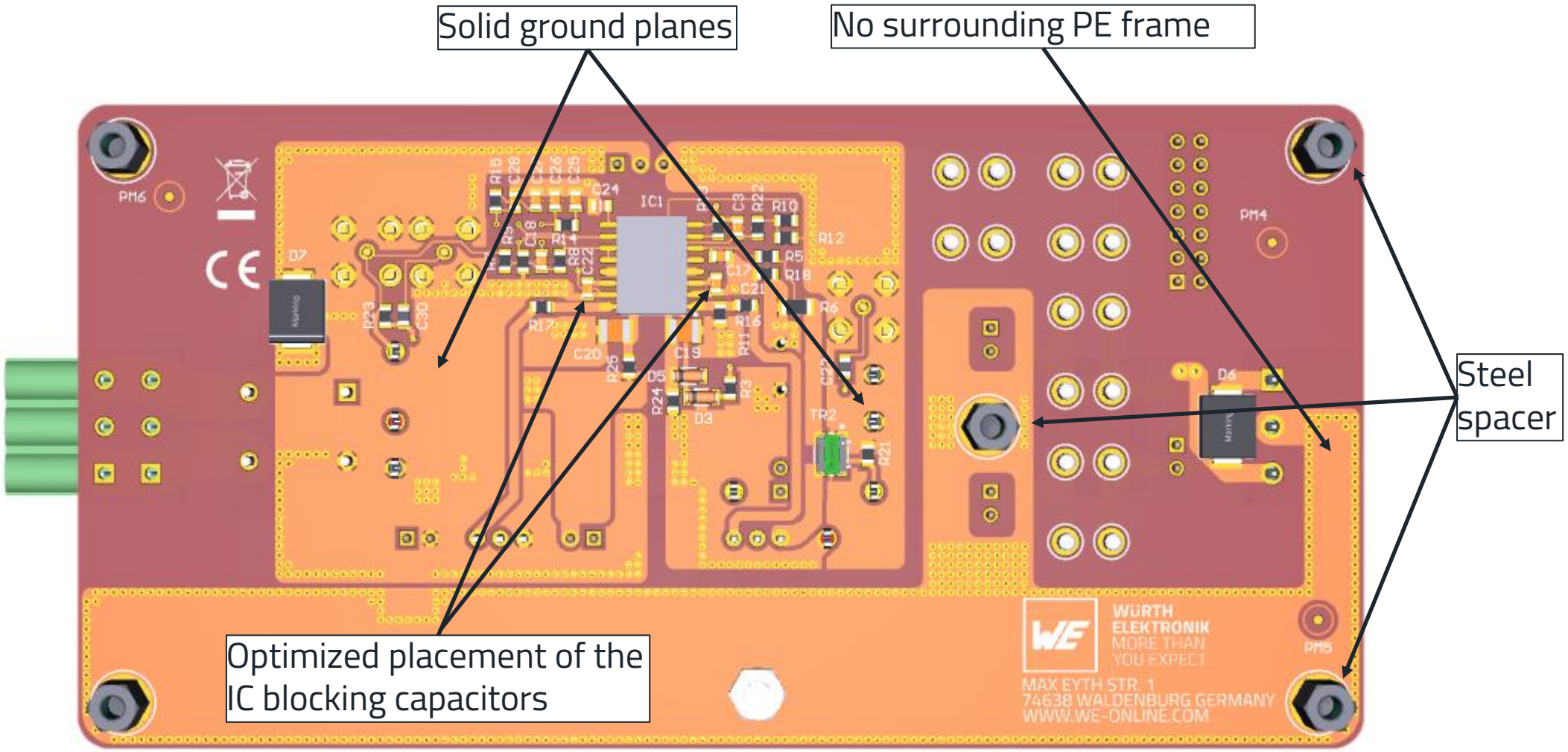
FLYBACK EMI - DEMONSTRATION BOARD - V2023.1

Top

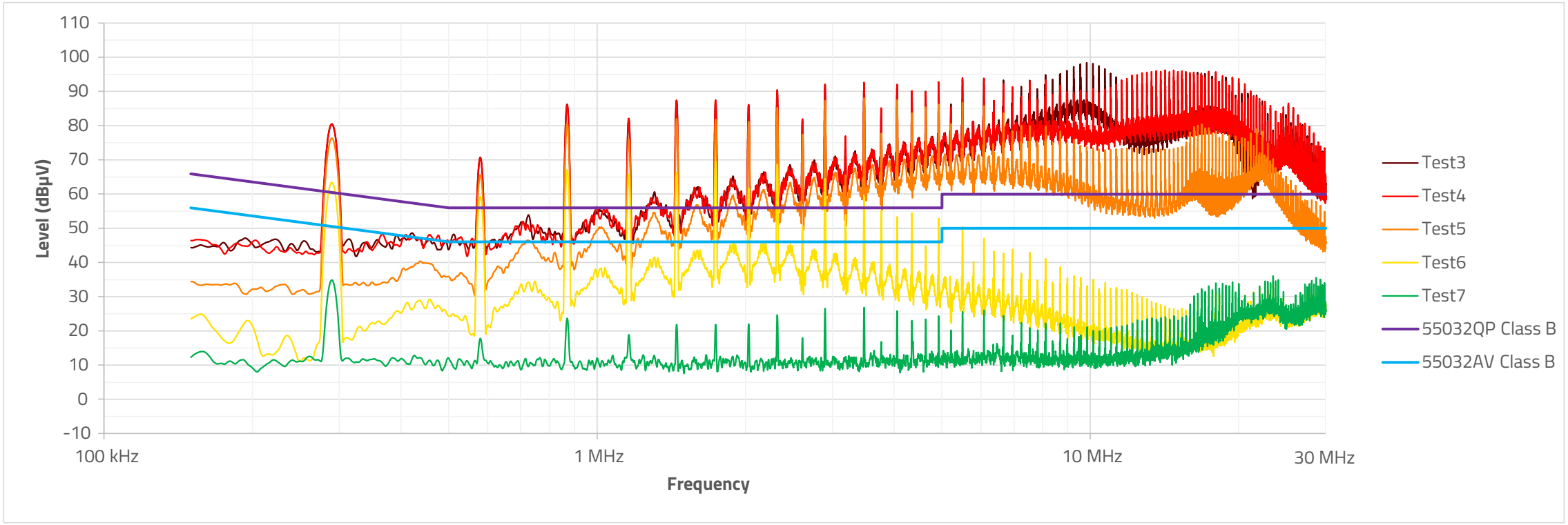


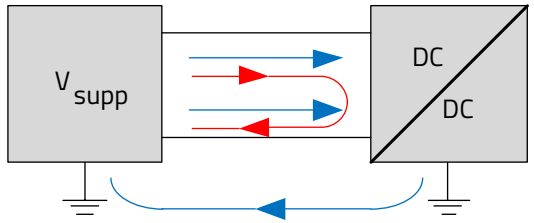
FLYBACK EMI - DEMONSTRATION BOARD - V2023.1

Bottom



TEST#3-7: V2023.1 - TOTAL CONDUCTED EMISSIONS - LINE

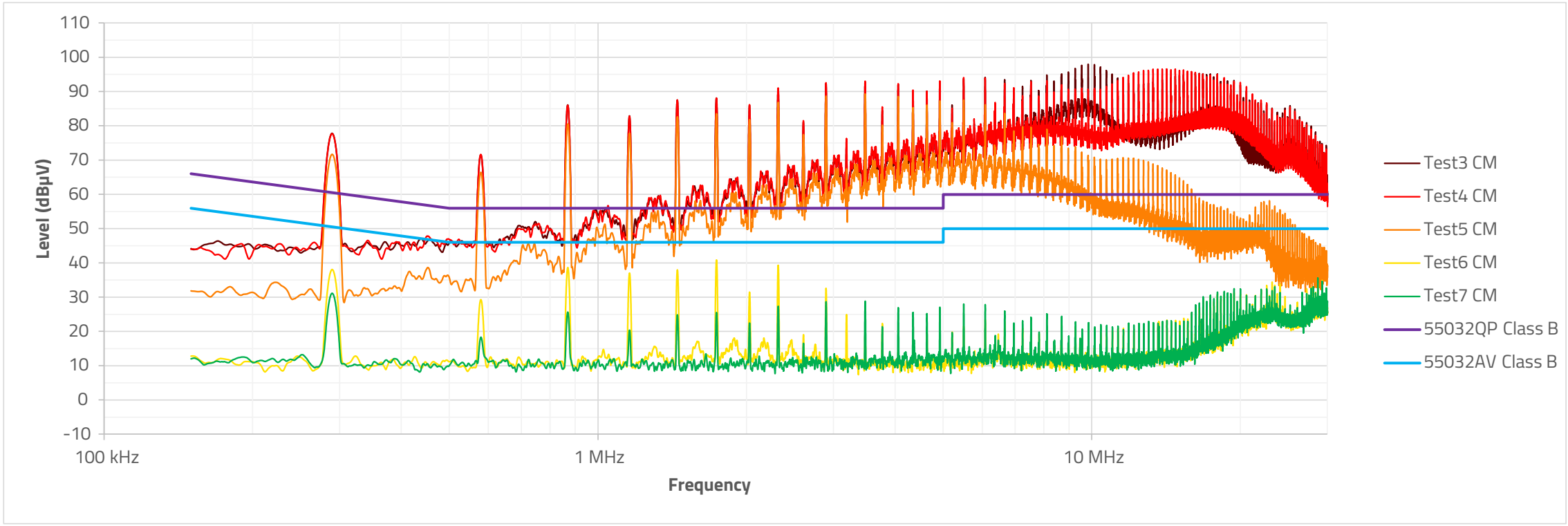


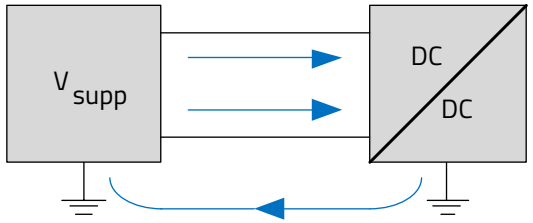


Combined

Namec	Description
Test#3	Reference (no improvement)
Test#4	Test#3 + RCD-snubber
Test#5	Test#4 + primary to secondary y-capacitors
Test#6	Test#5 + CMC and y-capacitors (CM filter)
Test#7	Test#6 + x-capacitor (DM filter)

TEST#3-7: V2023.1 - CONDUCTED EMISSIONS - COMMON MODE

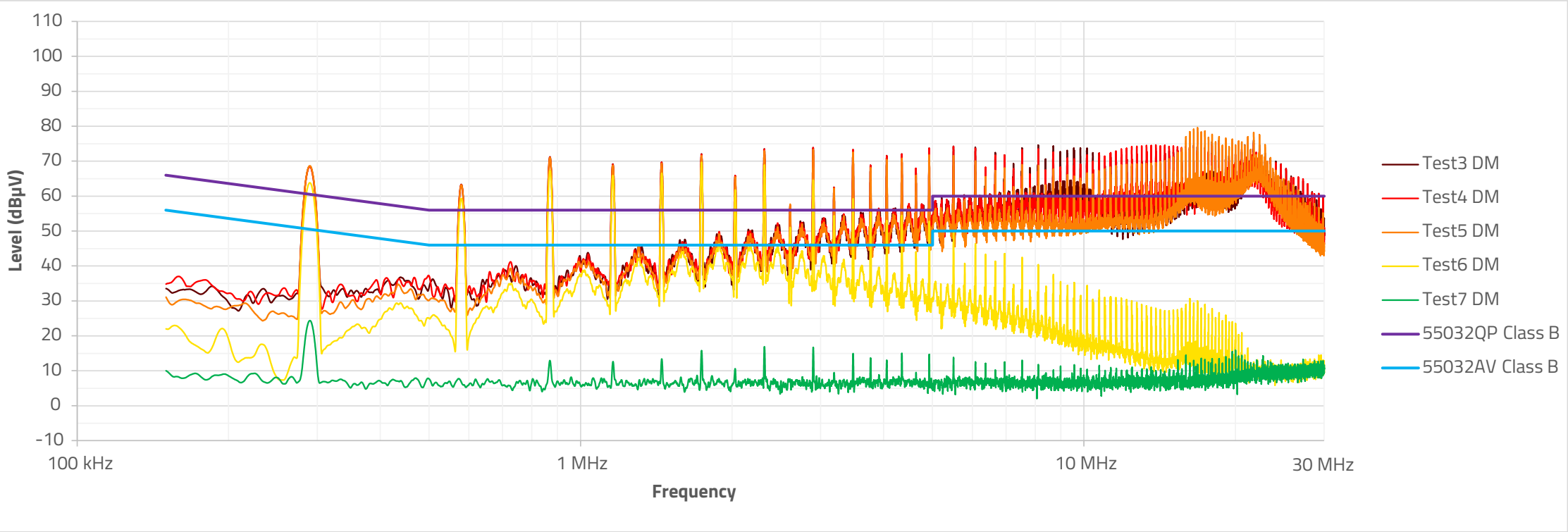


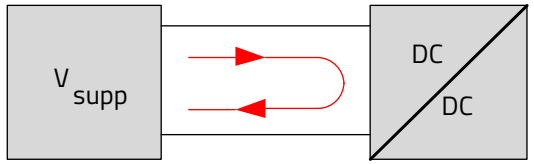


Common Mode

Name	Description
Test#3	Reference (no improvement)
Test#4	Test#3 + RCD-snubber
Test#5	Test#4 + primary to secondary y-capacitors
Test#6	Test#5 + CMC and y-capacitors (CM filter)
Test#7	Test#6 + x-capacitor (DM filter)

TEST#3-7: V2023.1 - CONDUCTED EMISSIONS - DIFFERENTIAL MODE





Differential Mode

Name	Description
Test#3	Reference (no improvement)
Test#4	Test#3 + RCD-snubber
Test#5	Test#4 + primary to secondary y-capacitors
Test#6	Test#5 + CMC and y-capacitors (CM filter)
Test#7	Test#6 + x-capacitor (DM filter)

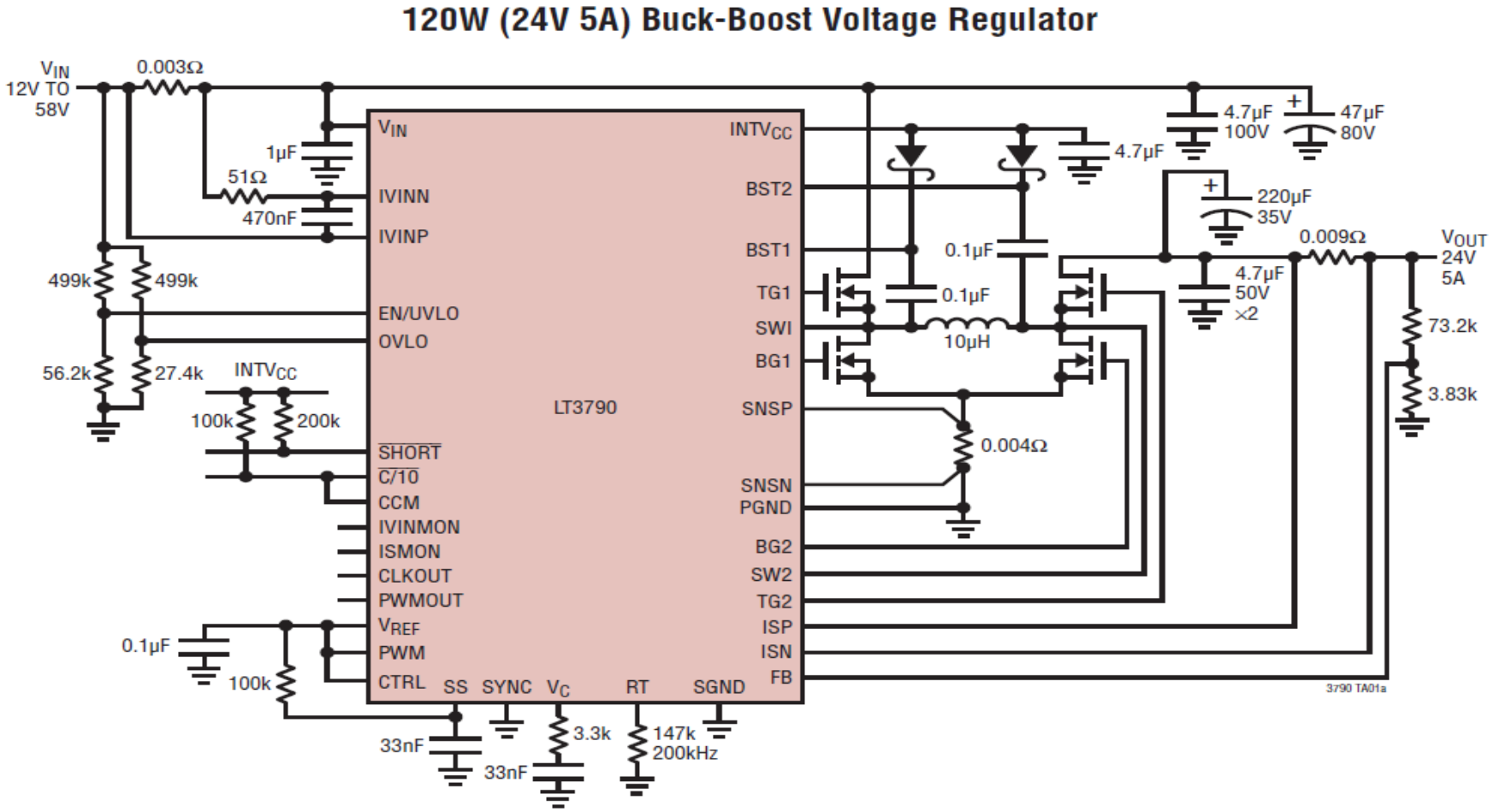
DC/DC CONVERTER DESIGN CHALLENGE

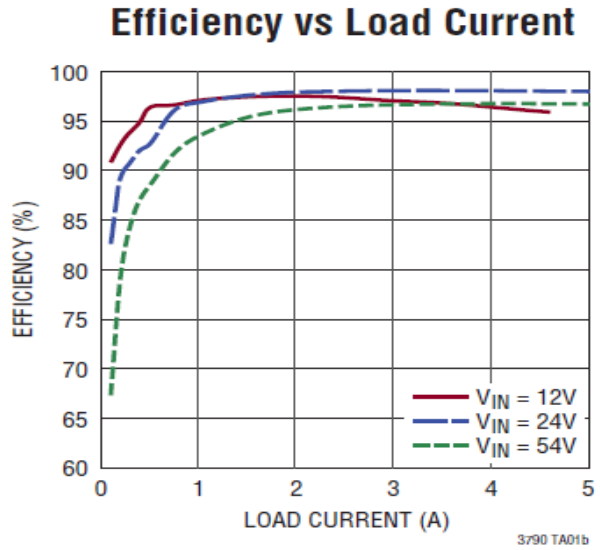
Requested:

- 100W buck-boost DC/DC
- 95% efficiency minimum
- EMC complaint for conducted and radiated
- Must fit in the already defined box
- Decision for the costs
  - lowest possible
  - Compromise for price and performance
  - No budget limit

SELECTED DC/DC IC FOR NEXT EXAMPLES

- 60V Buck-Boost Controller mit 4 external MOSFETs possible switching freq. 200-700kHz

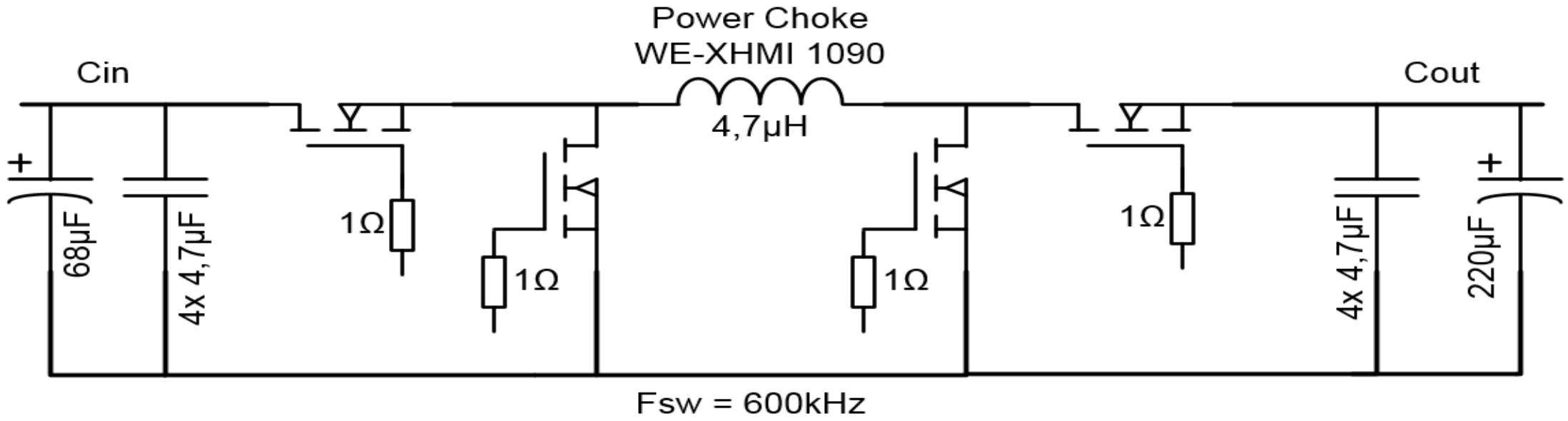




SOLUTION FOR LOWEST COST DESIGN (A)

- Single side PCB
- 4 Layer PCB
- Highest possible switching freq → 600kHz → smalest inductor can be used

➢ Lowest cost in comparation with the next ones

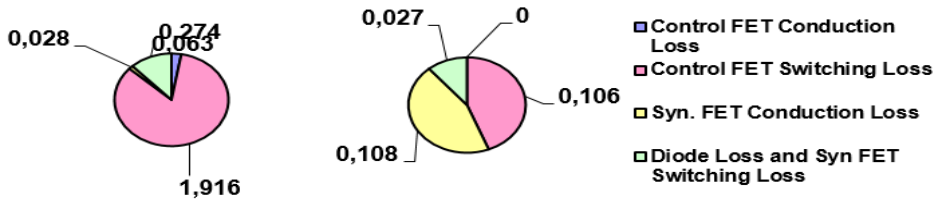


SELECTED MOSFETS FOR DESIGN (A)

- Logic Level N-Kanal FET im DPAK TO-252-3 package
- Rth not optimal
- Package ESL relativ high
- Package not compact

Estimated Power dissipation of each FET at full load, [P_{SYN}]=	0,05	0,11	W
Estimated Junction temperature, [Tj]=	50,04	50,10	°C

MOSFETs Power Loss Break Down (W)

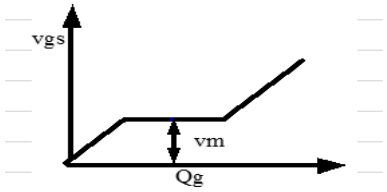


Buck Leg (A,B) Boost Leg(C,D)

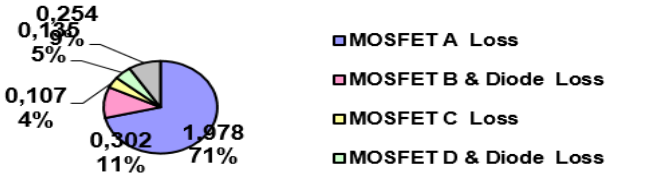
Estimated Efficiency

Overall estimated efficiency @ full load, [η]=	95,52	%

estimated.



Definition of FET Vm on Vgs Vs. Qg curve



Overall Power Loss Breakdown(W, %)

Infineon

IPD031N06L3 G

OptiMOS(TM)3 Power-Transistor

Features

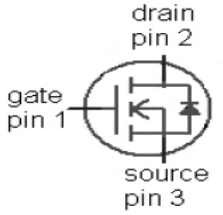
- Ideal for high frequency switching and sync. rec.
- Optimized technology for DC/DC converters
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- N-channel, logic level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC[1] for target applications

Product Summary

V_{DS}	60	V
$R_{DS(on),max}$	3.1	mΩ
I_D	100	A

RoHS

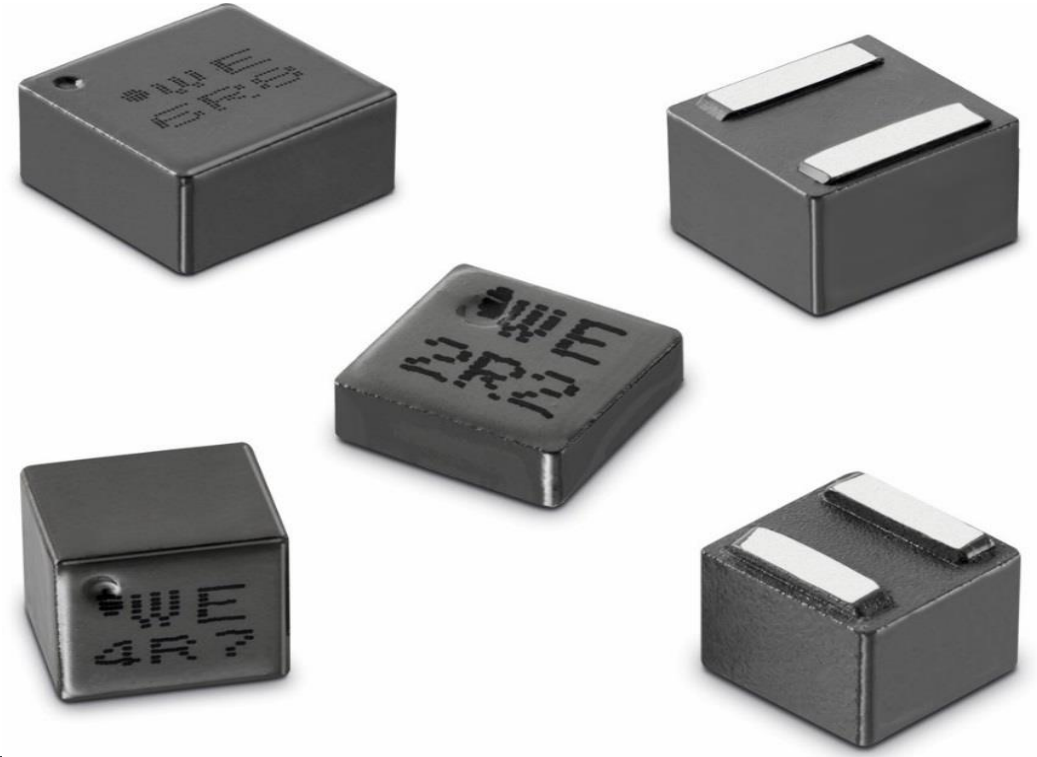
Type	IPD031N06L3 G
	
Package	PG-TO-252-3



REDEXPERT: INDUCTOR SELECTION FOR DESIGN(A)

- Fsw 600kHz → 30% max. Ripple current → Inductor 4,7µH

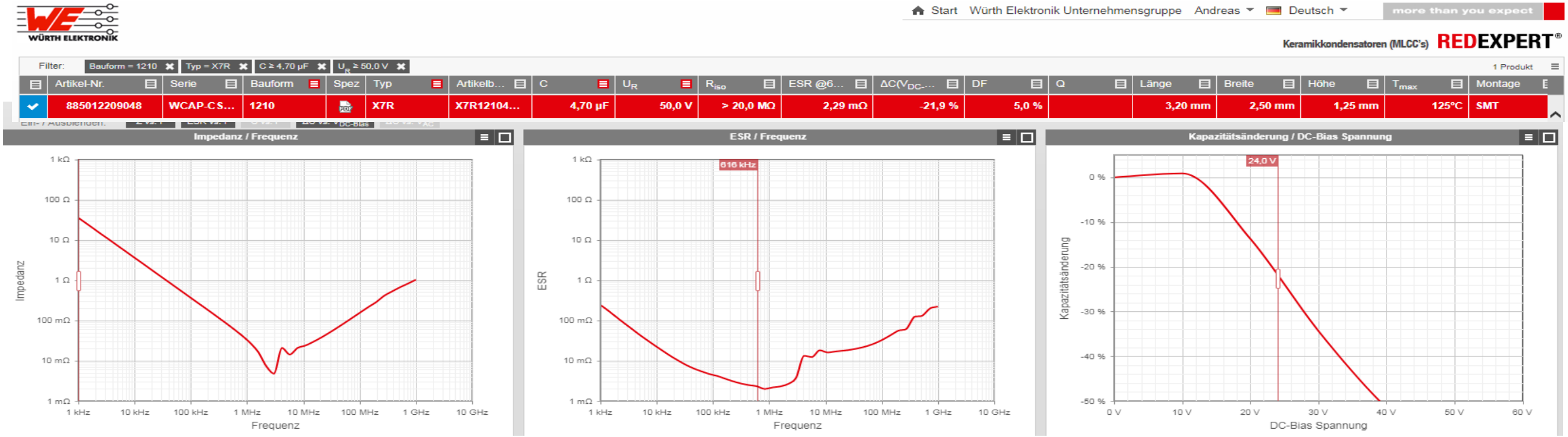
- Selected by REDEXPERT
- Type of inductor : WE-XHMI
  - Flat wire and shielded
  - Size 1090 (10x10x9mm)
  - Nominal current : 13,5A
  - Saturation current : 27A
  - Rdc : 5,4mΩ



REDEXPERT: INPUT CAP SELECTION FOR DESIGN(A)

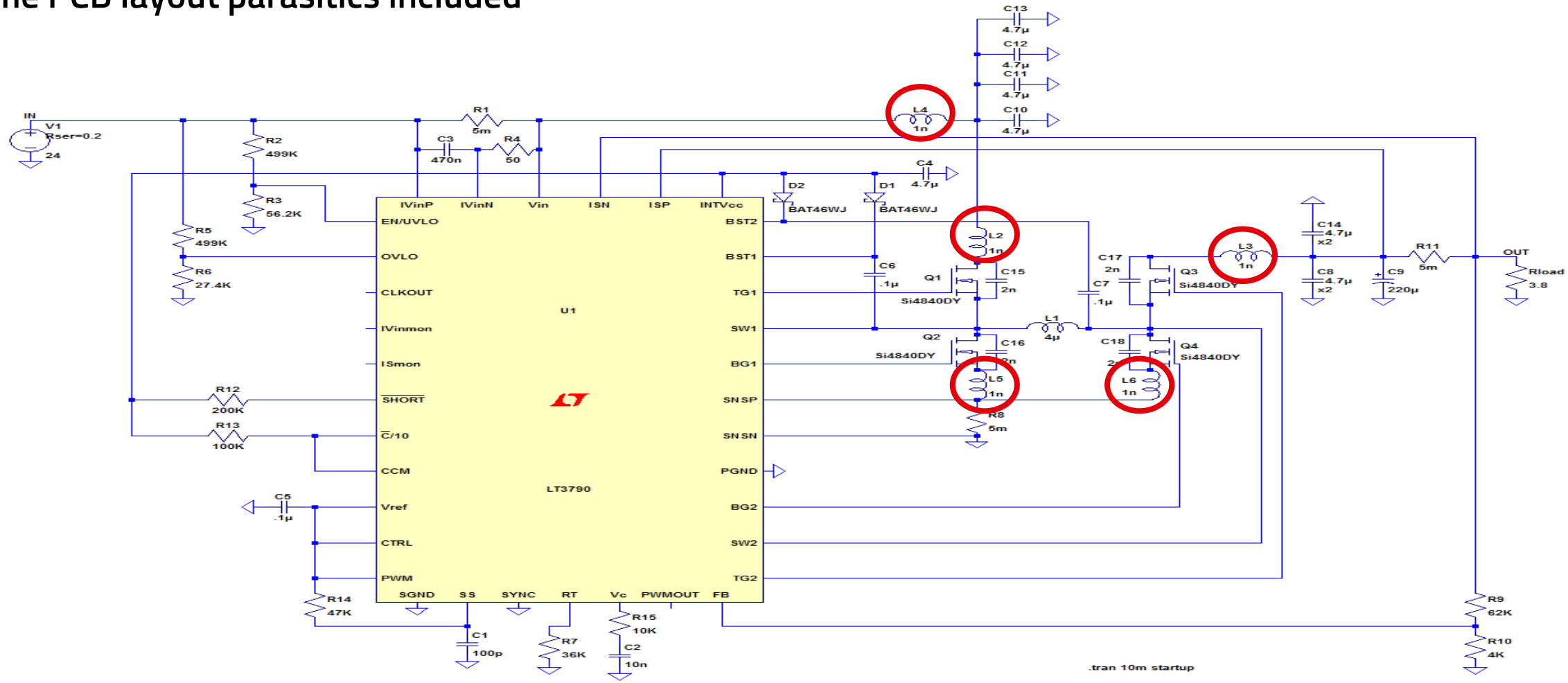
- Calculation for Cin MLCC X7R for maximum allowed ripple current

$$C_{in} \geq \frac{D \times (1 - D) \times I_{outmax}}{\Delta V_{in\,pp} \times f_{sw}} \qquad C_{in} \geq \frac{0{,}78 \times (1 - 0{,}78) \times 5A}{100mVpp \times 600kHz} = 14\mu F$$



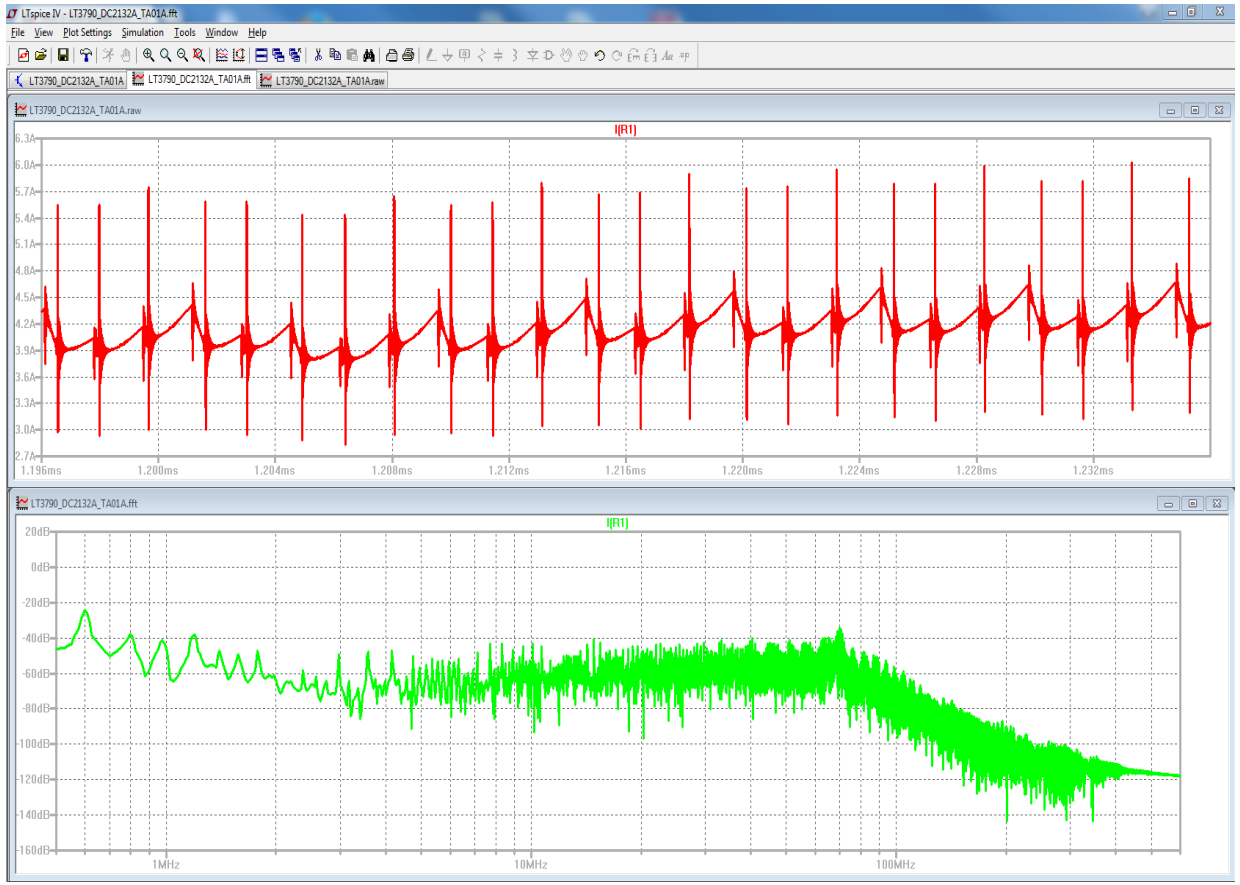
LTSPICE SIMULATION

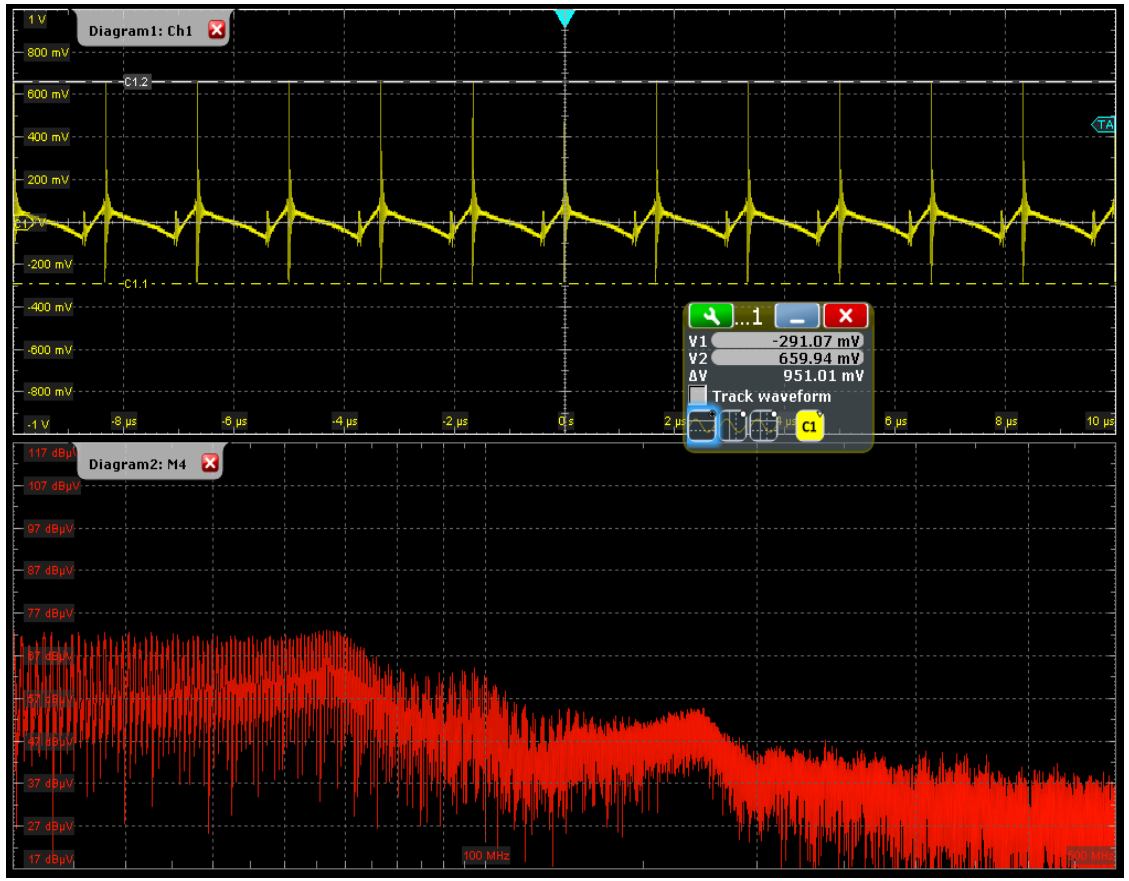
- Simulation for BuckBoost; all coponents including the parasitics
- Some PCB layout parasitics included



FILTER LTSPICE SIMULATION

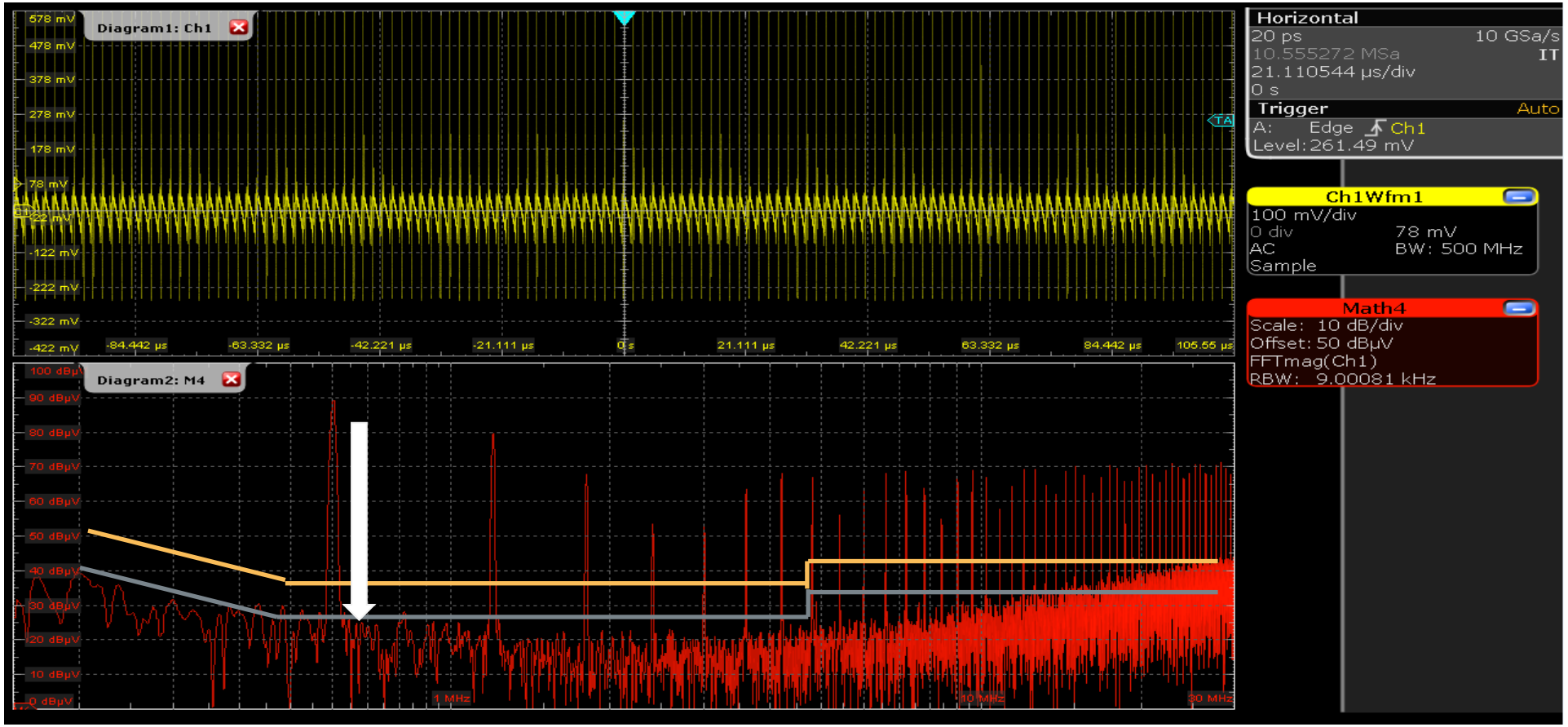
- Simulation vs. measurement





CONCLUSION FOR FILTER DESIGN

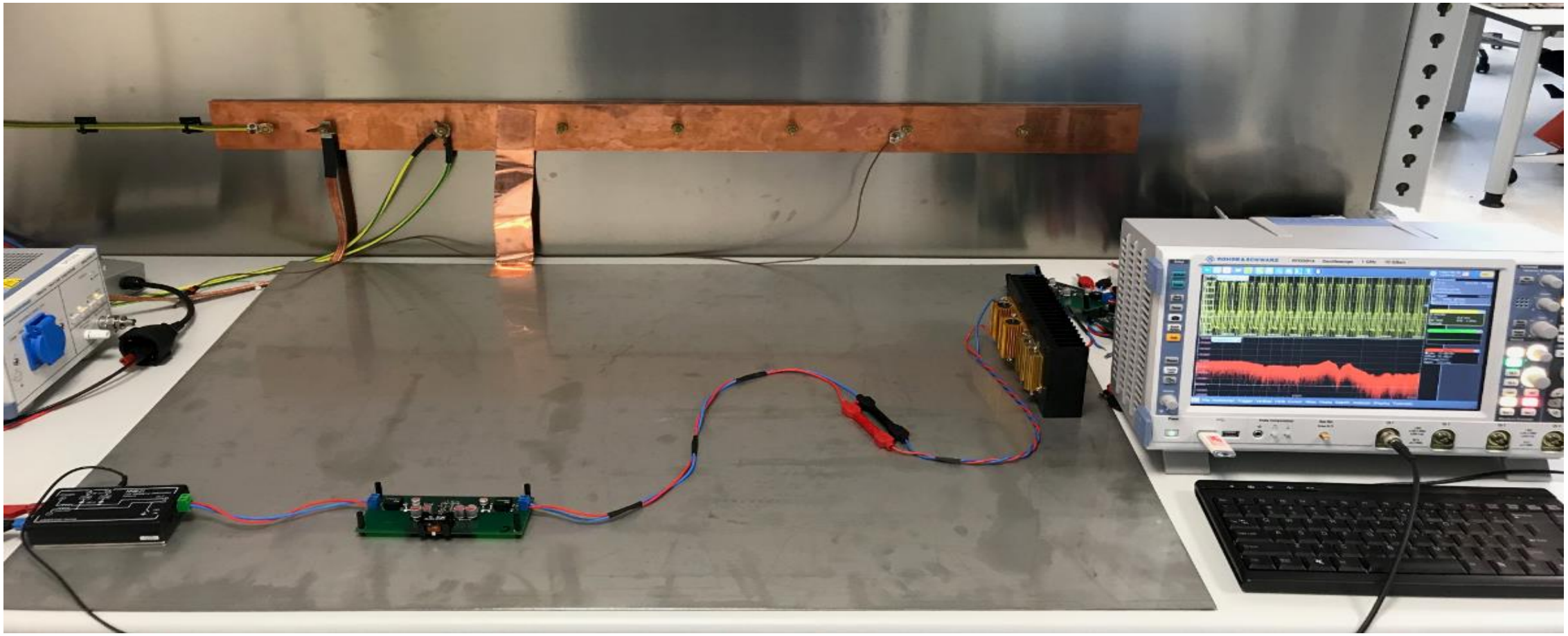
- Measurement for damping / Precompliant (ex. FFT & LISN mit 50Ω)



- Filter need to be at 600kHz ca. : 90dBµV – 40dBµV = 50dB

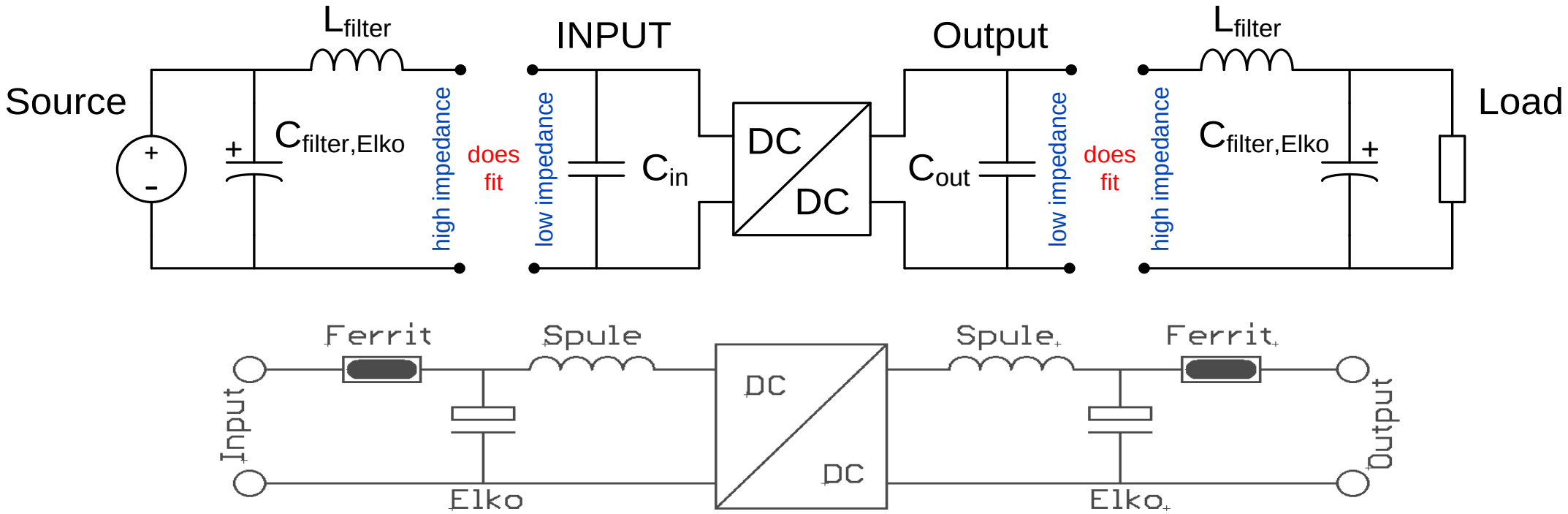
MEASUREMENT SET-UP NNB21 LISN + RTO (50Ω)

- Precompliant Measurement from 150kHz to 400MHz (in case you have a Spectrum analyzer you should use it instead of Scope)



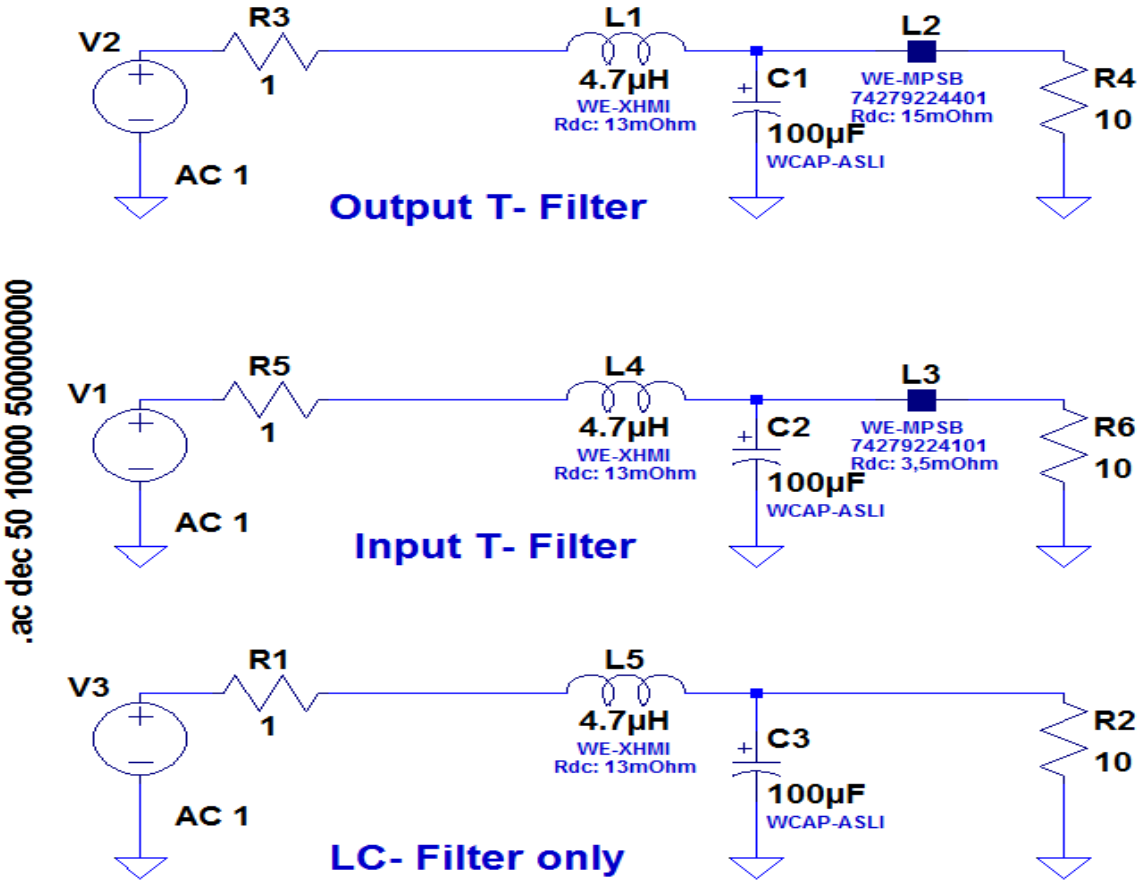
T-FILTER FOR DESIGN (A)

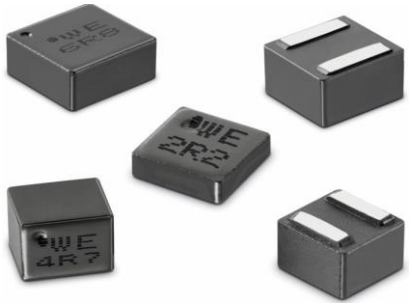
- Due to the long input wires a filter is a must
- Filter for conducted emmisions: 150kHz – 30MHz
- T – Filter can achive in theorie up to 60dB/Dec damping

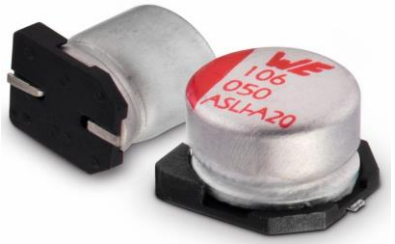


LTSPICE SIMULATION FOR T-FILTER DESIGN (A)

- All components with parasitics included
- MPSB Ferrite are suitable above ca. 5MHz

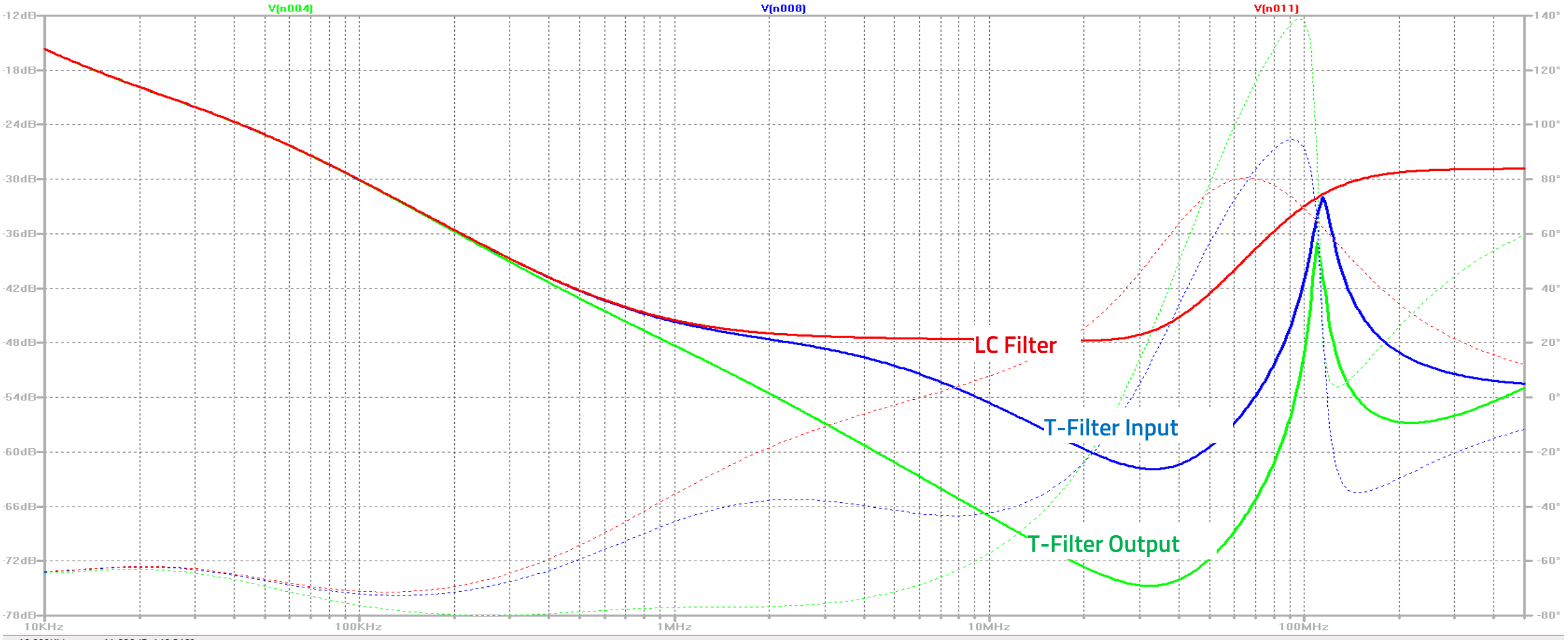






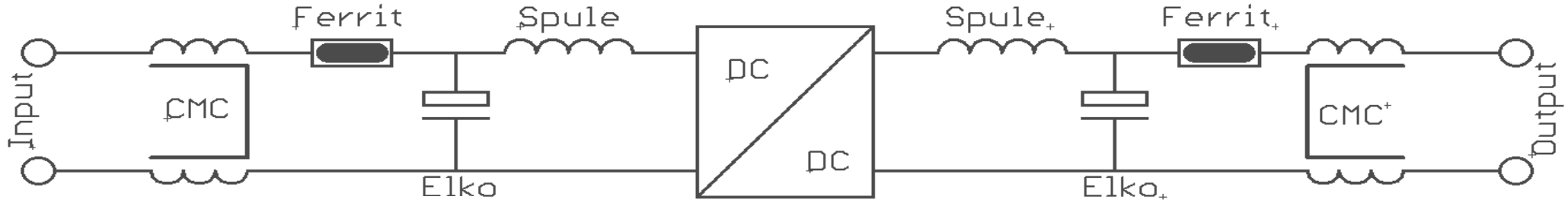
LTSPICE SIMULATION FOR T-FILTER DESIGN (A)

- Damping for T-Filter above 40dB Differntial Mode from 150KHz up to 80MHz

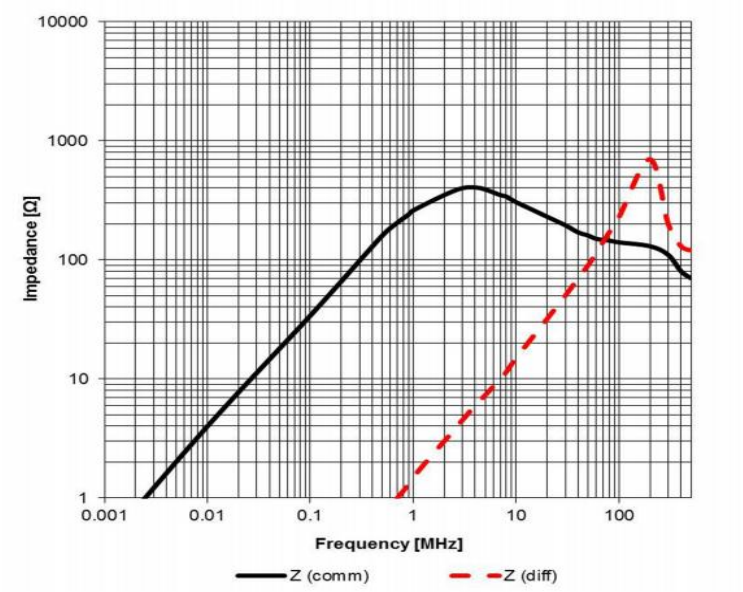


CMC FILTER FOR ALL DESIGNS

- Selected Common Mode Choke with huge bandwith for 30MHz to 500MHz
- Important to know: CMC´s are helping for imunity like BURST & HF

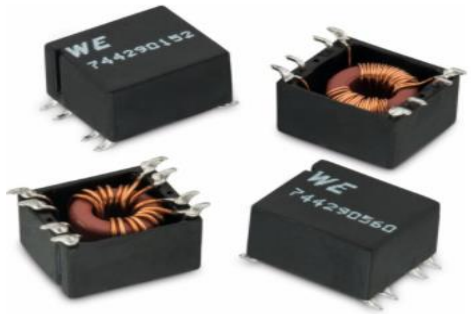


F1 Typical Impedance Characteristics:



Input:

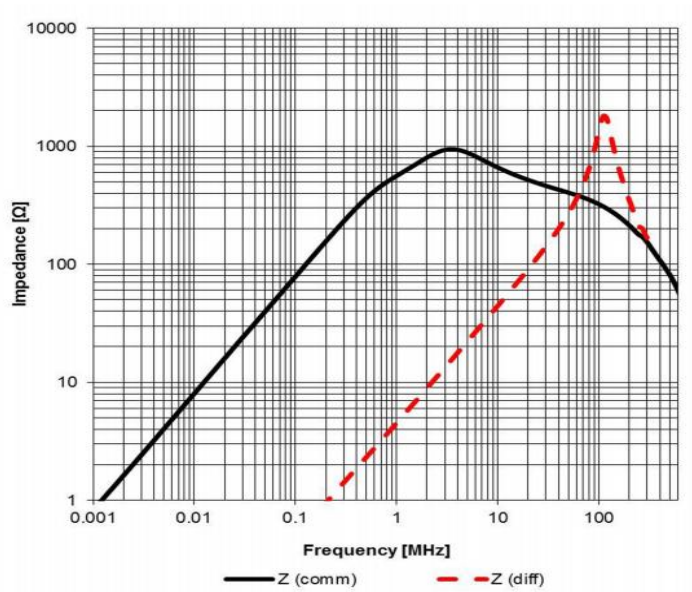
WE-UCF
2x56uH
Ir = 7A
Rdc:4,7m



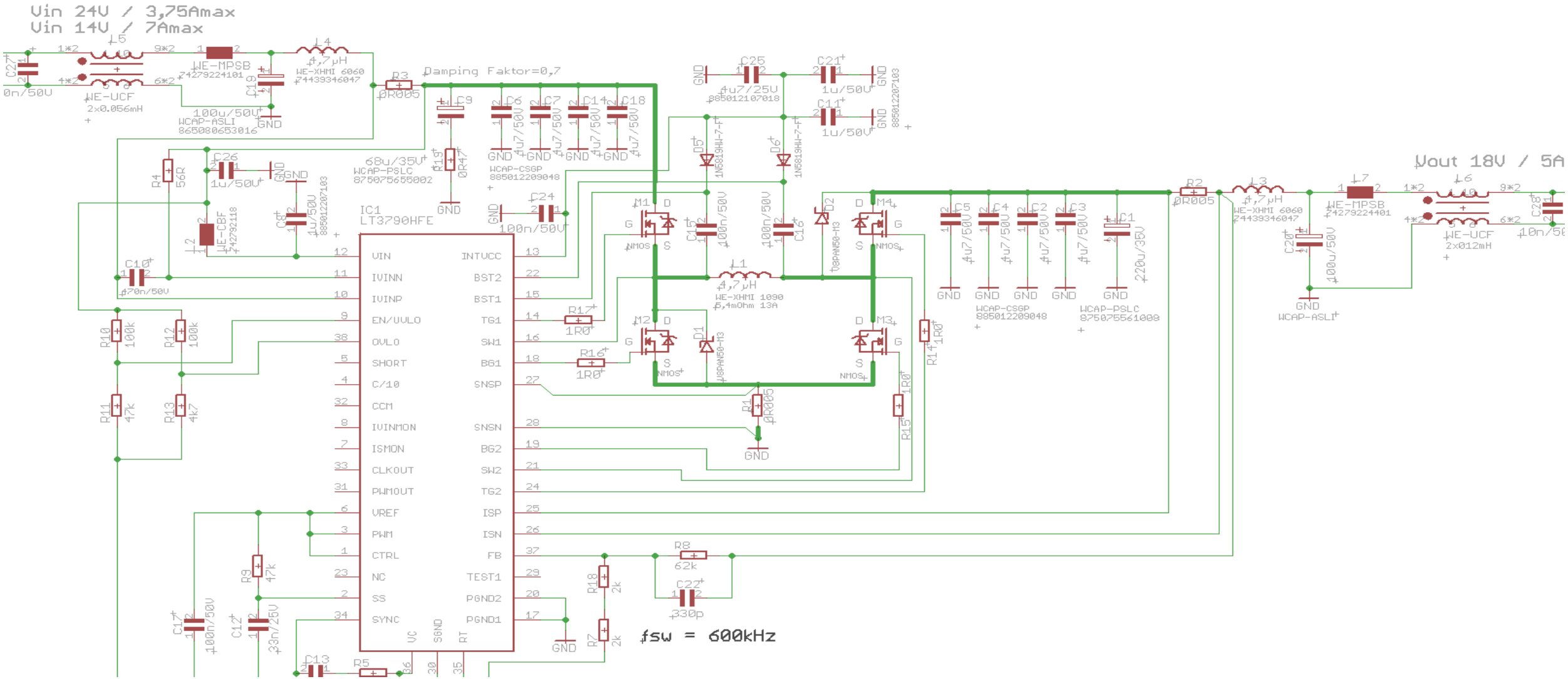
Output:

WE-UCF
2x120uH
Ir = 5,5A
Rdc:10m

F1 Typical Impedance Characteristics:



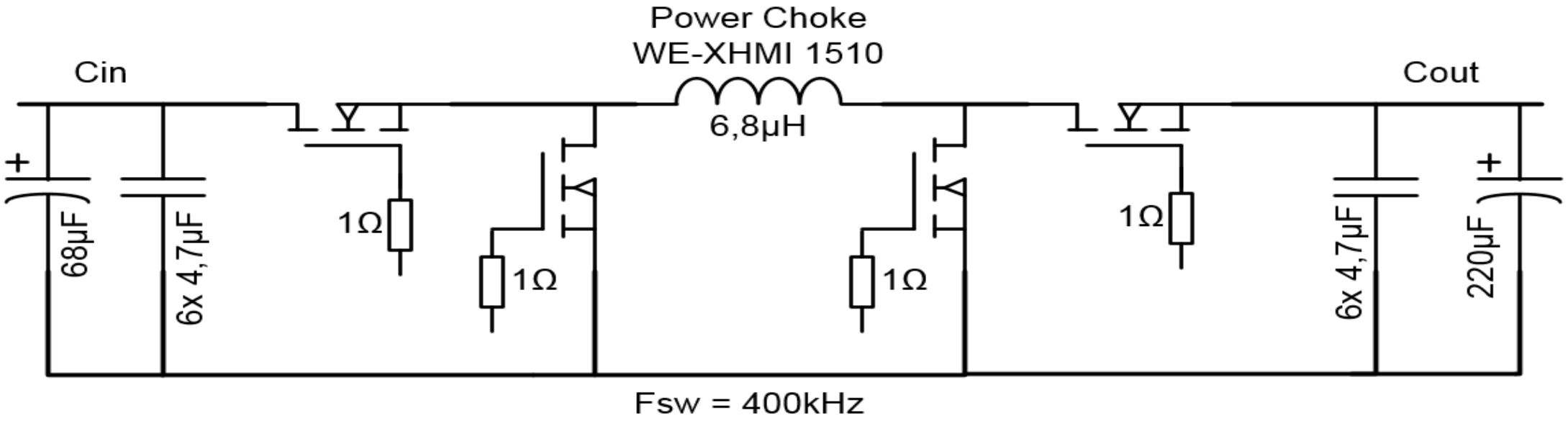
SCHEMATIC DESIGN (A)



DESIGN (B)

DESIGN (B)

- Up and down layer using components
- 6 Layer PCB
- Moderate switching freq → 400kHz → compromise between switching losses and inductor losses
- Optimized Filter at I/O → less RDC losses
- ➢ Medium cost

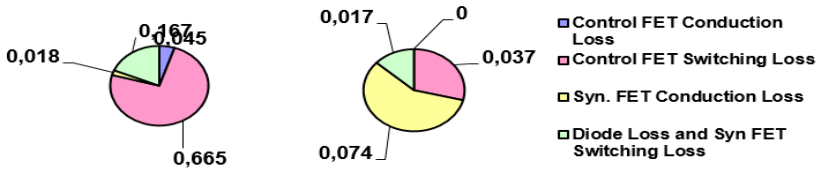


MOSFETS FOR DESIGN (B)

- Logic Level N-Kanal FET in SON 5x6 package
- Rth much better
- Package ESL small
- Rdson small
- Gate Charge small

Estimated Power dissipation of each FET at full load, [P_{SYN}]=	0,02	0,07 W
Estimated Junction temperature, [Tj]=	50,02	50,06 °C

MOSFETs Power Loss Break Down (W)

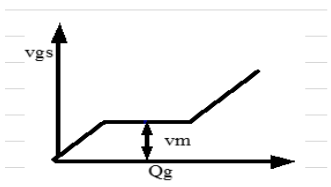


Buck Leg (A,B) Boost Leg(C,D)

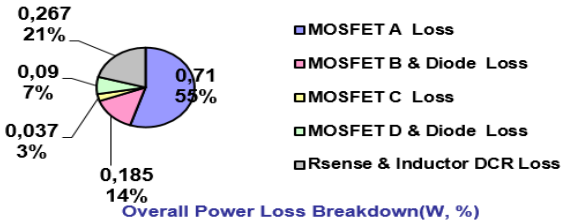
Estimated Efficiency

Overall estimated efficiency @ full load, [η]=	97,72	%

estimated.



Definition of FET Vm on Vgs Vs. Qg curve



Overall Power Loss Breakdown(W, %)

TEXAS INSTRUMENTS

CSD18532Q5B

SLPS322B – NOVEMBER 2012 – REVISED JULY 2014

CSD18532Q5B 60-V N-Channel NexFET™ Power MOSFETs

1 Features

- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Logic Level
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

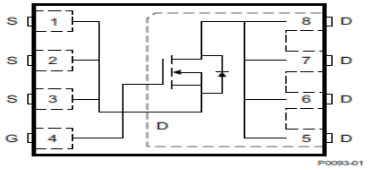
2 Applications

- DC-DC Conversion
- Secondary Side Synchronous Rectifier
- Isolated Converter Primary Side Switch
- Motor Control

3 Description

This 2.5 mΩ, 60 V SON 5 mm × 6 mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

Top View



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	60		V
Q_g	Gate Charge Total (10 V)	44		nC
Q_{gd}	Gate Charge Gate-to-Drain	6.9		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 4.5 V	3.3	mΩ
		V_{GS} = 10 V	2.5	mΩ
$V_{GS(th)}$	Threshold Voltage	1.8		V

Ordering Information(1)

Device	Qty	Media	Package	Ship
CSD18532Q5B	2500	13-Inch Reel	SON 5 × 6 mm Plastic Package	Tape and Reel
CSD18532Q5BT	250	13-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package limited)	100	A
	Continuous Drain Current (Silicon limited), T_C = 25°C	172	
	Continuous Drain Current(1)	23	
I_{DM}	Pulsed Drain Current(2)	400	A
P_D	Power Dissipation(1)	3.2	W
	Power Dissipation, T_C = 25°C	156	
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 80 A, L = 0.1 mH, R_G = 25 Ω	320	mJ

(1) Typical $R_{\theta JA}$ = 40 °C/W on a 1-inch², 2-oz. Cu pad on a 0.06-inch thick FR4 PCB.

(2) Max $R_{\theta JC}$ = 0.8 °C/W, Pulse duration ≤100 µs, duty cycle ≤1%

INDUCTOR SELECTION FOR DESIGN (B)

- Fsw 400kHz → 30% max. ripple current → Inductor ca. 6,8µH
- Selection with REDEXPERT
- Type of inductor: WE-XHMI

➢ Flat wire and shielded

➢ Size 1510 (15x15x10mm)

➢ Nominal current : 15A

➢ Saturation curent : 46A

➢ Rdc : 4,1mΩ

INPUT CAPACITOR CALCULATION FOR DESIGN (B)

- **Cin used MLCC X7R for max allowed ripple voltage**

$$C_{in} \geq \frac{D \times (1 - D) \times I_{outmax}}{\Delta V_{in\,pp} \times f_{sw}} \qquad C_{in} \geq \frac{0{,}78 \times (1 - 0{,}78) \times 5{,}5A}{100mVpp \times 400kHz} = 21\mu F$$

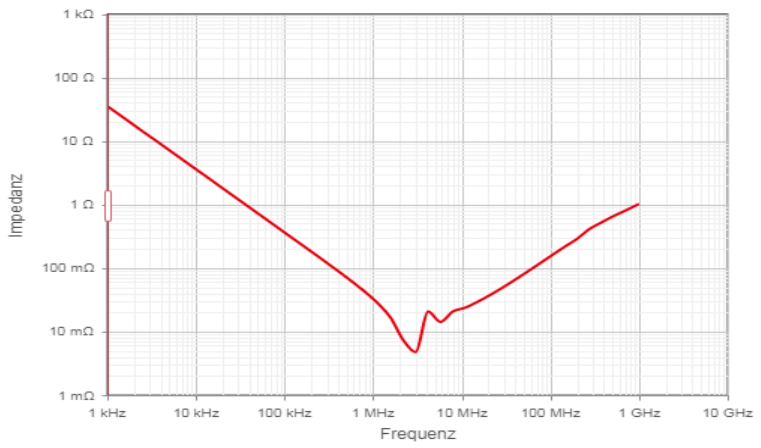
➢ Selected : 6 x 4,7µF / 50V / X7R = 28,2µF – 20% DC-Bias = <u>23µF</u>

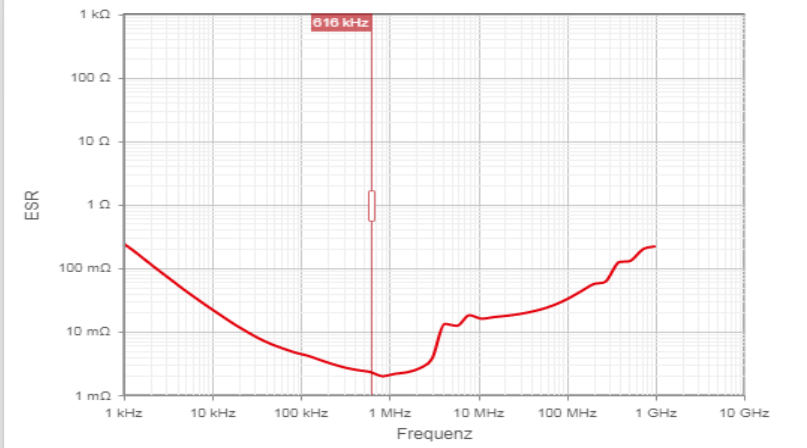
WÜRTH ELEKTRONIK

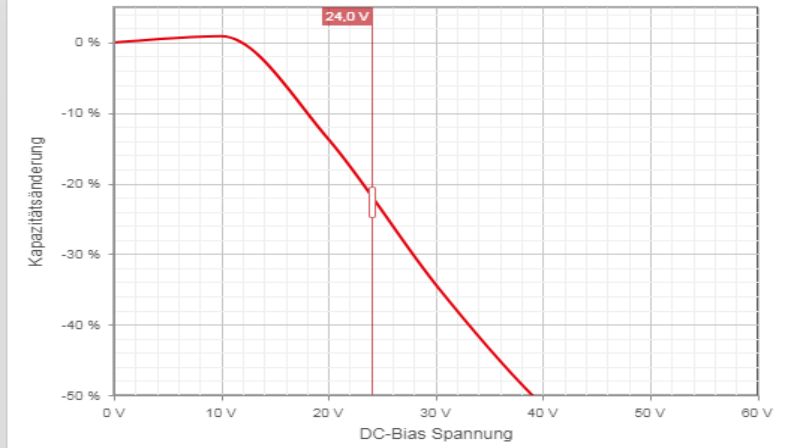
Keramikkondensatoren (MLCC's) **REDEXPERT**®

Filter: Bauform = 1210 | Typ = X7R | C ≥ 4,70 µF | U_R ≥ 50,0 V — 1 Produkt

Artikel-Nr.	Serie	Bauform	Spez	Typ	Artikelb…	C	U_R	R_{iso}	ESR @6…	ΔC(V_{DC}-…	DF	Q	Länge	Breite	Höhe	T_{max}	Montage
885012209048	WCAP-CS…	1210		X7R	X7R12104…	4,70 µF	50,0 V	> 20,0 MΩ	2,29 mΩ	-21,9 %	5,0 %		3,20 mm	2,50 mm	1,25 mm	125°C	SMT

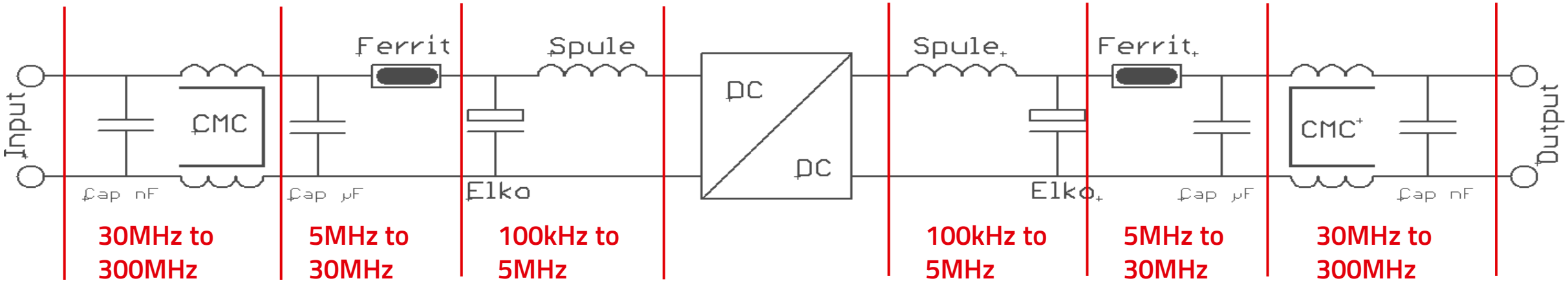






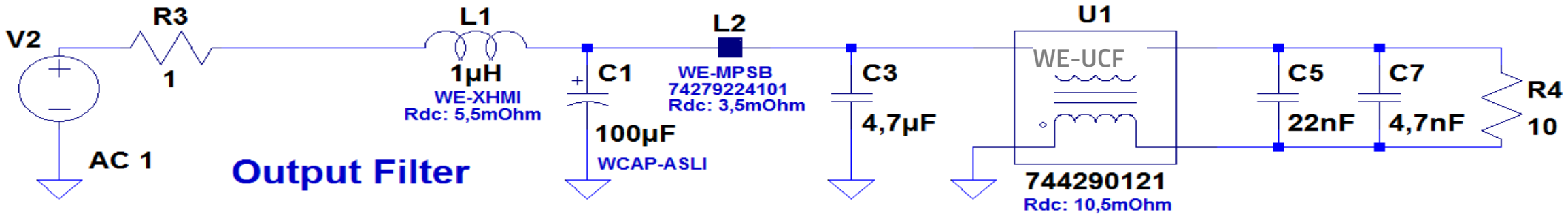
FILTER OPTIMIZATION FOR DIFF MODE FOR DESIGN (B)

- Filter for Conducted und Radiated Emission Test Spectrum
- 3 filter stage's
- At the CMC will only the leackage inductor for diff mode considered

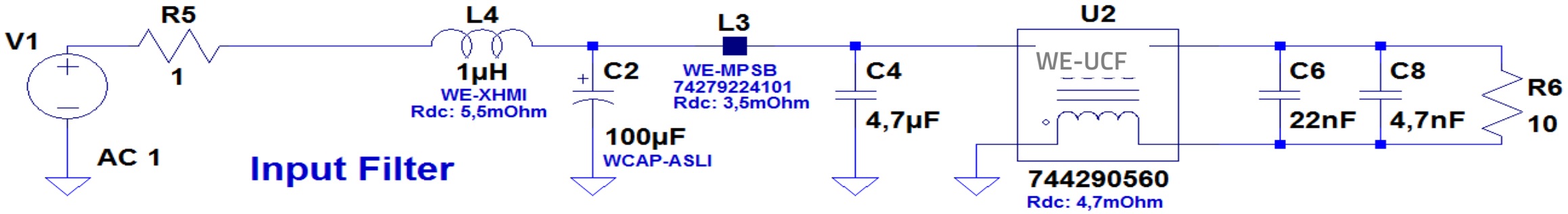


DIFFERENTIAL MODE FILTER FOR DESIGN (B)

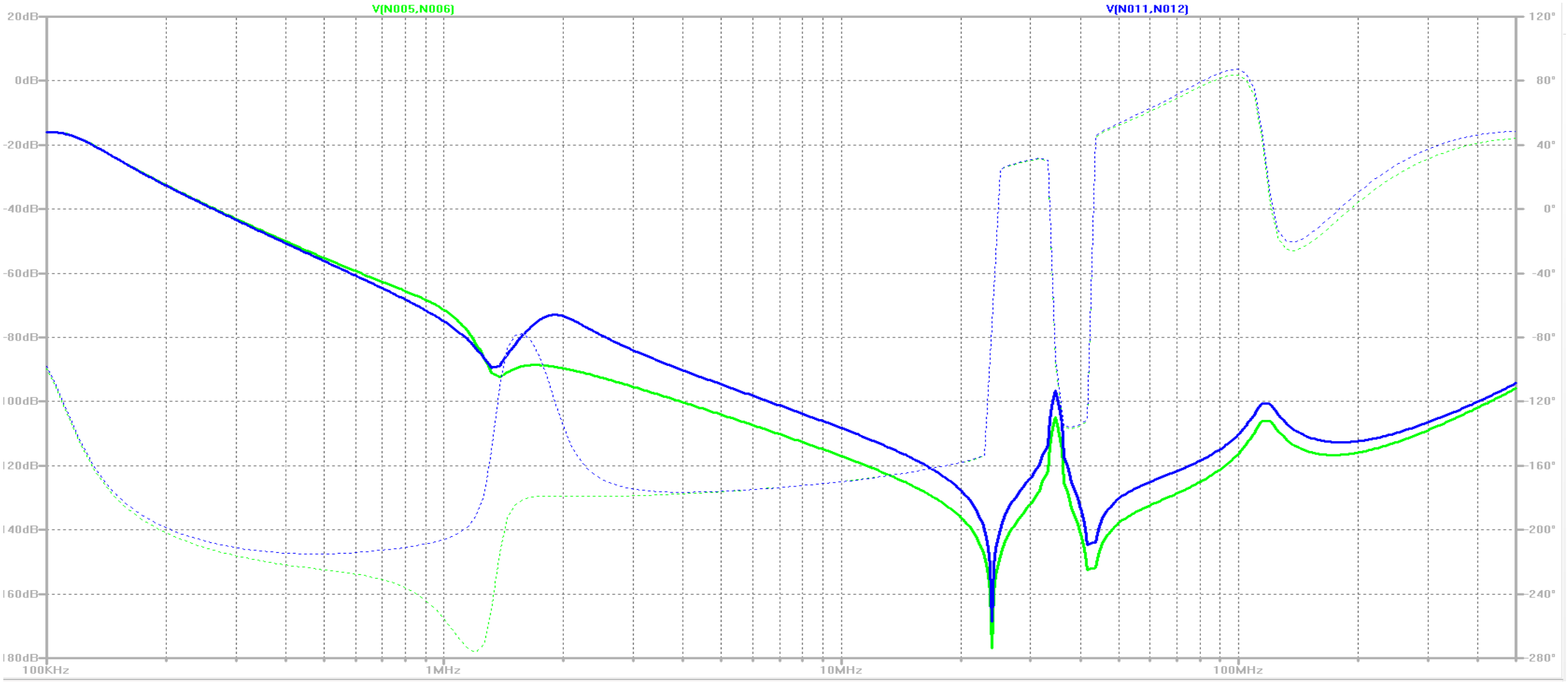
- All components with they parasitics considered for the simulation
- Losses at the Output Filter : $I^2*Rdc = 5{,}5A^2 * 30m\Omega = 907mW$
- Losses at the Input Filter: $I^2*Rdc = 7A^2 * 18{,}4m\Omega = 902mW$



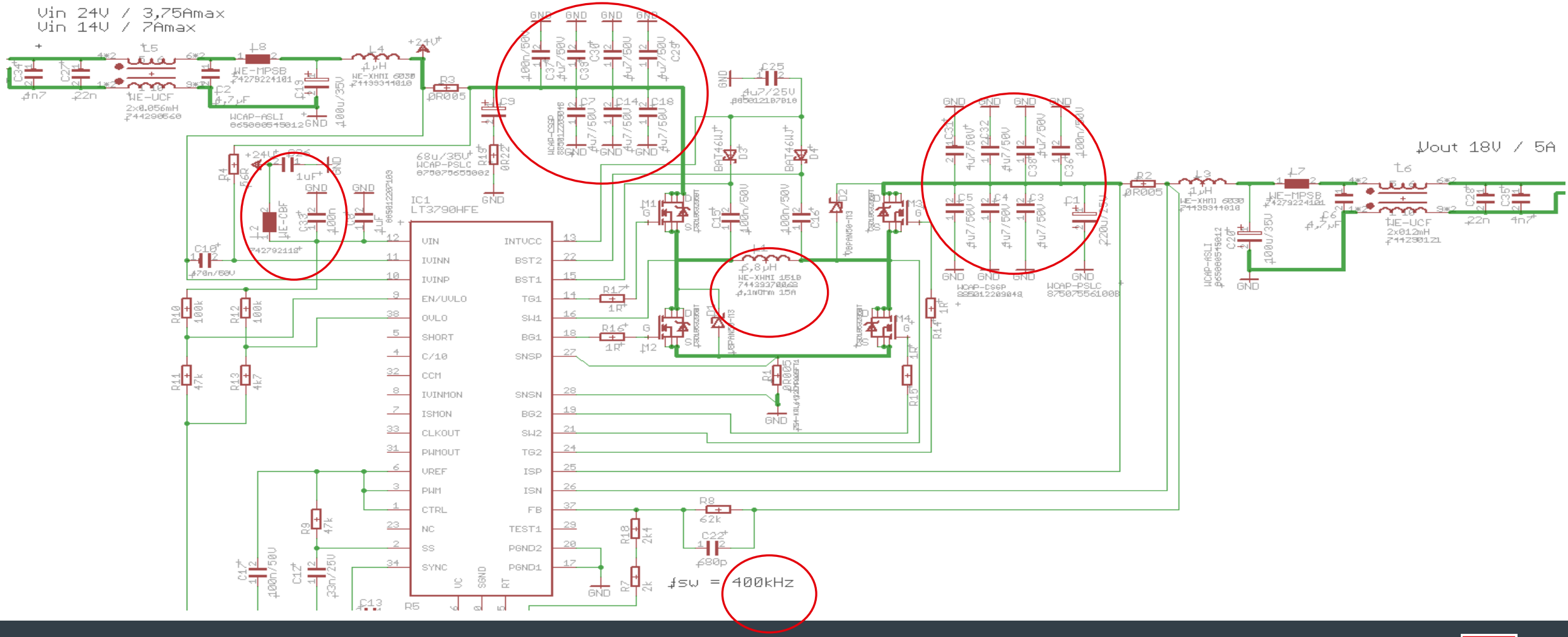
.ac dec 50 10000 500000000



FILTER FOR DESIGN (B)



SCHEMATIC FOR DESIGN (B)

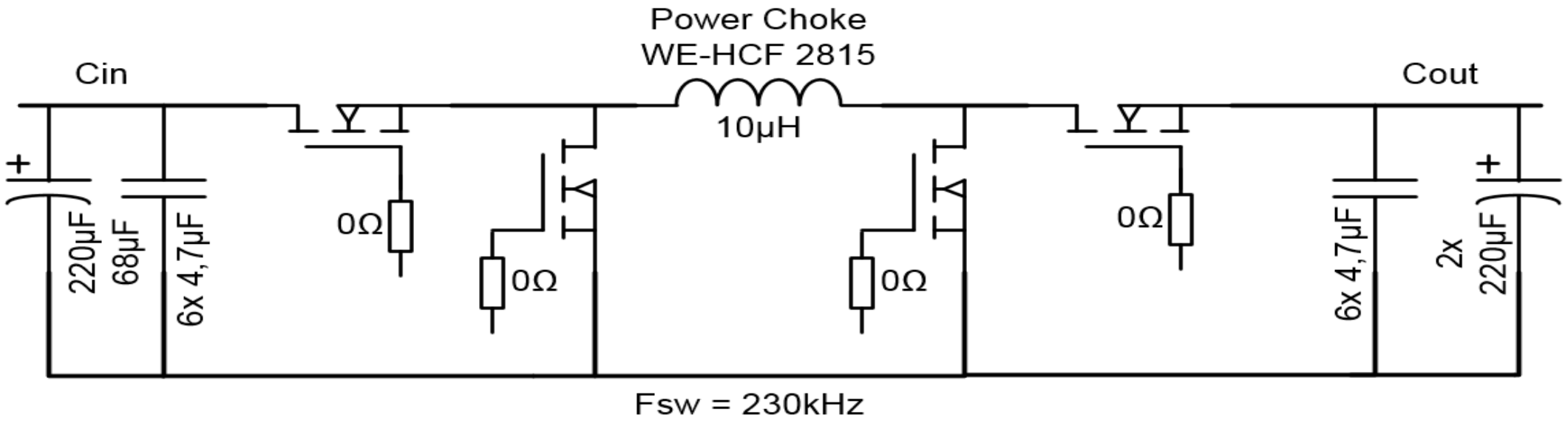


DESIGN (C)

DESIGN (C)

- Top and bottom side using components
- 6 Layer PCB
- Lowest switching freg → 230kHz → to achive lowest losses and highest efficiency → big inductor value / big cap values / no Gate resistors
- Different filters like design B used

➢ Most expensive / biggest size on PCB

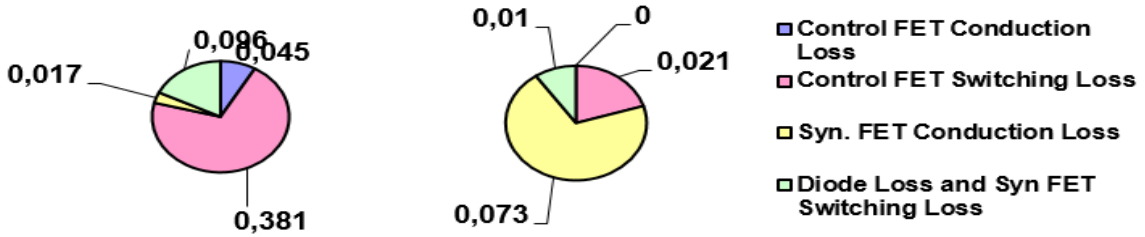


MOSFETS FOR DESIGN (C)

- **Logic Level N-Kanal FET im SON 5x6 same like used in Design (B)**

Estimated Power dissipation of each FET at full load, [P_{SYN}]=	0,02	0,07	W
Estimated Junction temperature, [Tj]=	50,02	50,06	°C

MOSFETs Power Loss Break Down (W)

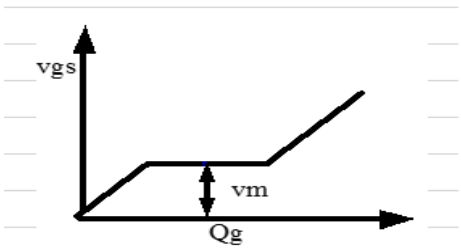


Buck Leg (A,B) Boost Leg(C,D)

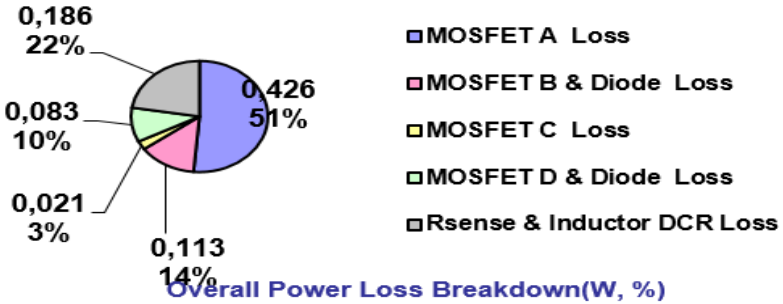
Estimated Efficiency

Overall estimated efficiency @ full load, [η]=	98,51	%

estimated.



Definition of FET Vm on Vgs Vs. Qg curve



Overall Power Loss Breakdown(W, %)

TEXAS INSTRUMENTS

CSD18532Q5B

SLPS322B – NOVEMBER 2012 – REVISED JULY 2014

CSD18532Q5B 60-V N-Channel NexFET™ Power MOSFETs

1 Features

- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Logic Level
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

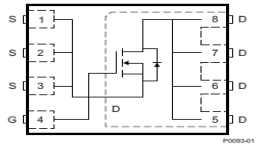
2 Applications

- DC-DC Conversion
- Secondary Side Synchronous Rectifier
- Isolated Converter Primary Side Switch
- Motor Control

3 Description

This 2.5 mΩ, 60 V SON 5 mm × 6 mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

Top View



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	60		V
Q_g	Gate Charge Total (10 V)	44		nC
Q_{gd}	Gate Charge Gate-to-Drain	6.9		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 4.5 V	3.3	mΩ
		V_{GS} = 10 V	2.5	mΩ
$V_{GS(th)}$	Threshold Voltage	1.8		V

Ordering Information(1)

Device	Qty	Media	Package	Ship
CSD18532Q5B	2500	13-Inch Reel	SON 5 × 6 mm Plastic Package	Tape and Reel
CSD18532Q5BT	250	13-Inch Reel		

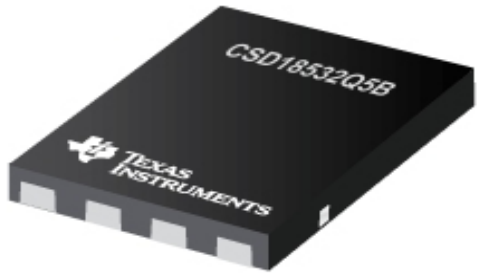
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package limited)	100	A
	Continuous Drain Current (Silicon limited), T_C = 25°C	172	
	Continuous Drain Current(1)	23	
I_{DM}	Pulsed Drain Current(2)	400	A
P_D	Power Dissipation(1)	3.2	W
	Power Dissipation, T_C = 25°C	156	
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 80 A, L = 0.1 mH, R_G = 25 Ω	320	mJ

(1) Typical $R_{\theta JA}$ = 40 °C/W on a 1-inch², 2-oz. Cu pad on a 0.06-inch thick FR4 PCB.

(2) Max $R_{\theta JC}$ = 0.8 °C/W, Pulse duration ≤100 µs, duty cycle ≤1%



INDUCTOR SELECTION FOR DESIGN (C)

- **Fsw at 230kHz → 30% max. ripple current → Inductor value ca. 10µH**

- Selected with REDEXPERT
- Selected Type of inductor: WE-HCF
  - Flat wire and shielded
  - Size 2815 (28x27x15mm)
  - Nominal current : 36A
  - Saturation current : 21,5A
  - Rdc : 1,33mΩ

INPUT CAPACITOR SELECTION FOR DESIGN(C)

- Calculation for Cin using MLCC X7R for max allowed ripple current

$$C_{in} \geq \frac{D \times (1 - D) \times I_{outmax}}{\Delta V_{in\,pp} \times f_{sw}} \qquad C_{in} \geq \frac{0{,}78 \times (1 - 0{,}78) \times 5A}{20mVpp \times 230kHz} = 186\mu F$$

➢ Selected : 7 x 4,7µF / 50V / X7R = 33µF – 20% DC-Bias = 26,3µF

➢ Additional: Parallel to the MLCCs 1x 220µF/35V Al-Polymer WCAP-PSLC

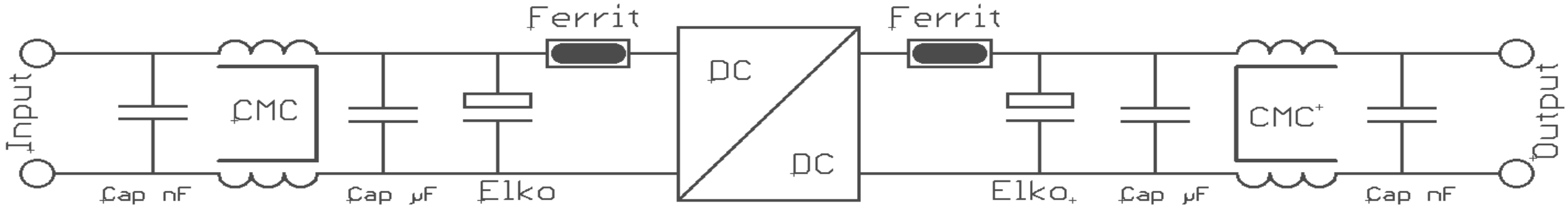
FILTER FOR DESIGN (C)

- Filter for Conducted und Radiated Emission Test Spectrum

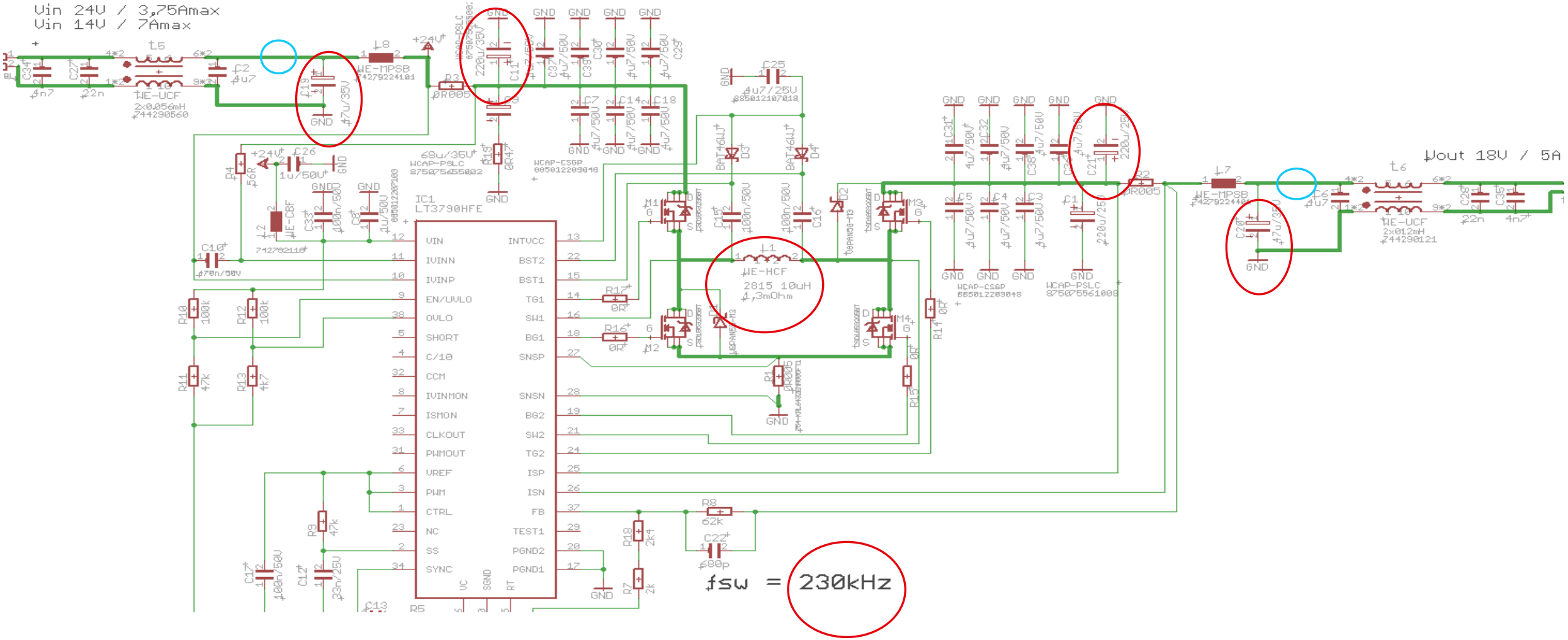
- Target: increase the efficiency compared with design (B)

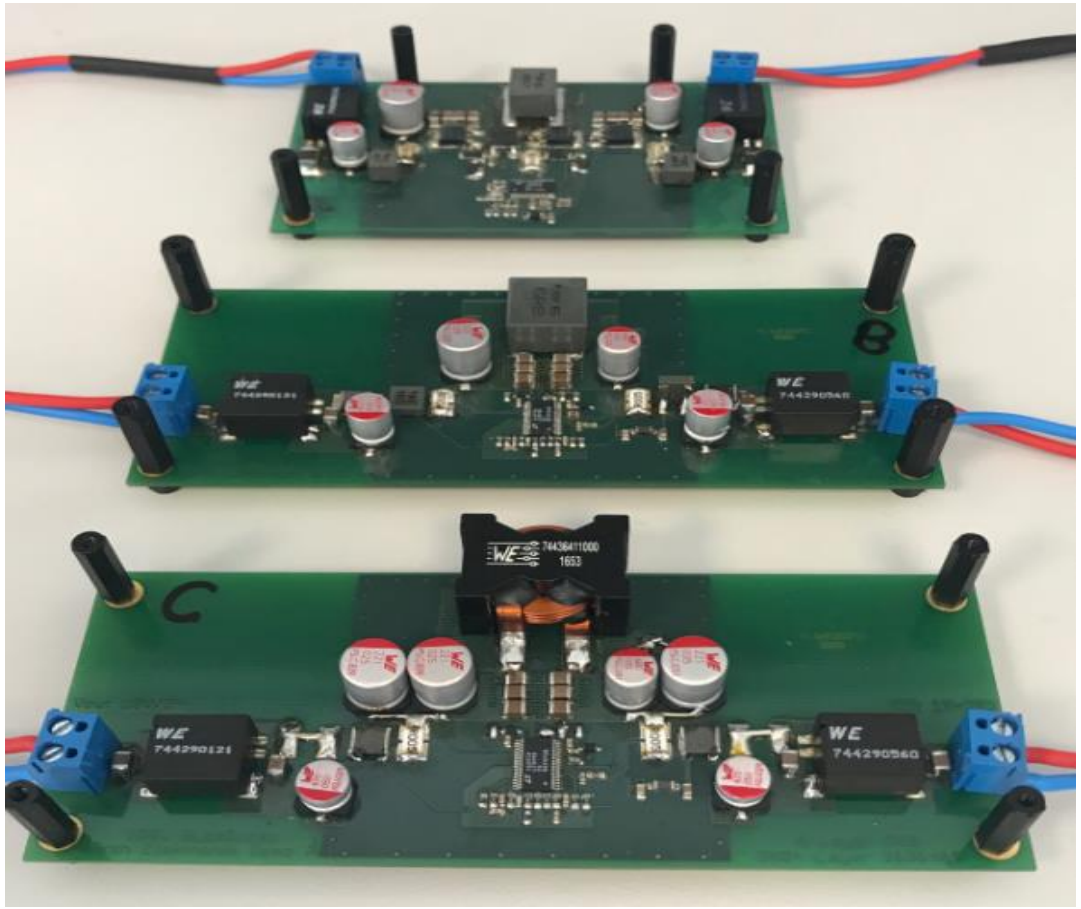
➢ Skip the 1µH Inductor from design (B) → big influence up to 5MHz

➢ Filter Caps from 100µF reduced to 47uF, in rest same components used



SCHEMATIC FOR DESIGN (C)

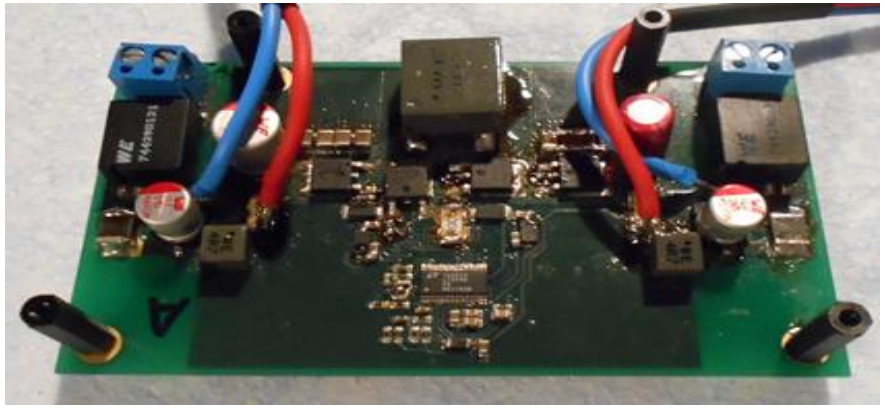


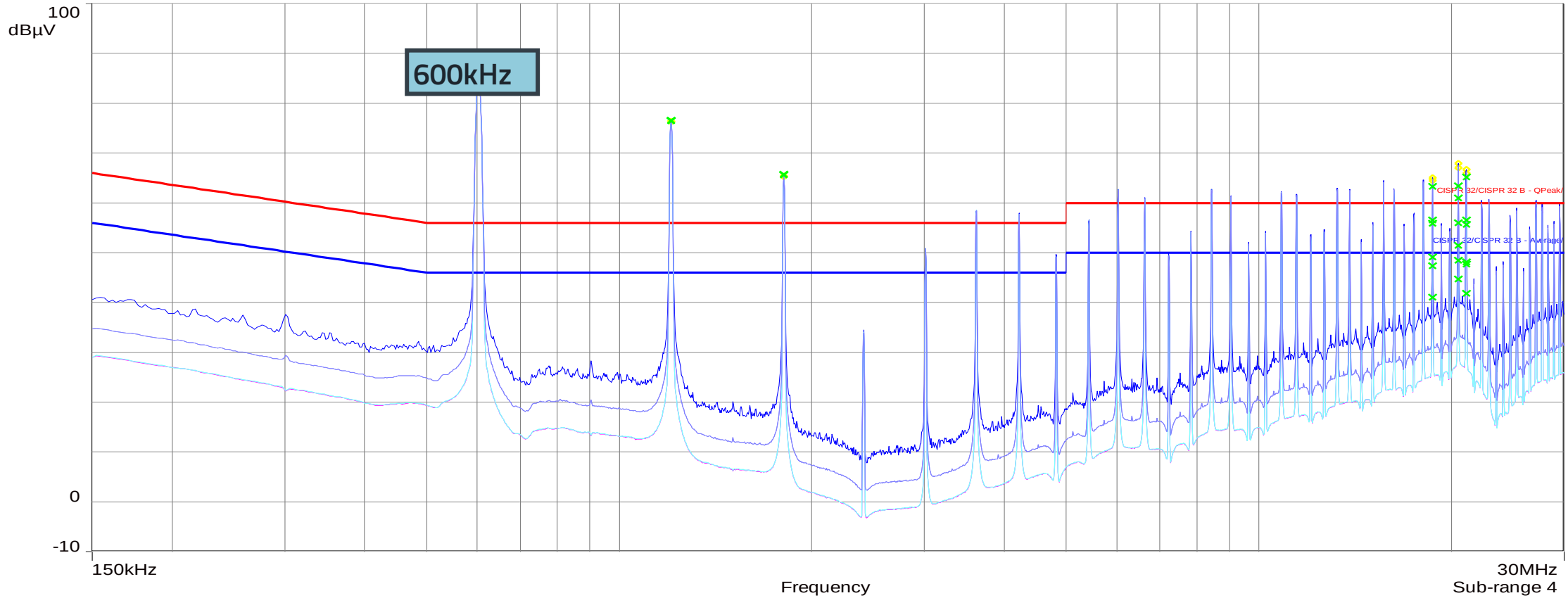


EMC MEASUREMENTS CONDUCTED & RADIATED

MEASURED WITH ENV216 LISN & ESRP

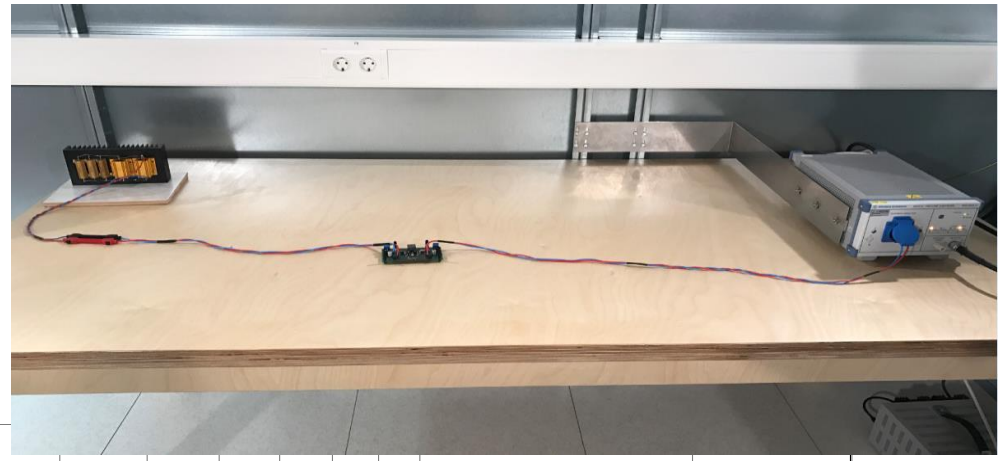
- Conducted Emission 150kHz – 30MHz
- Design (A) without Filter / Buck Mode 100W

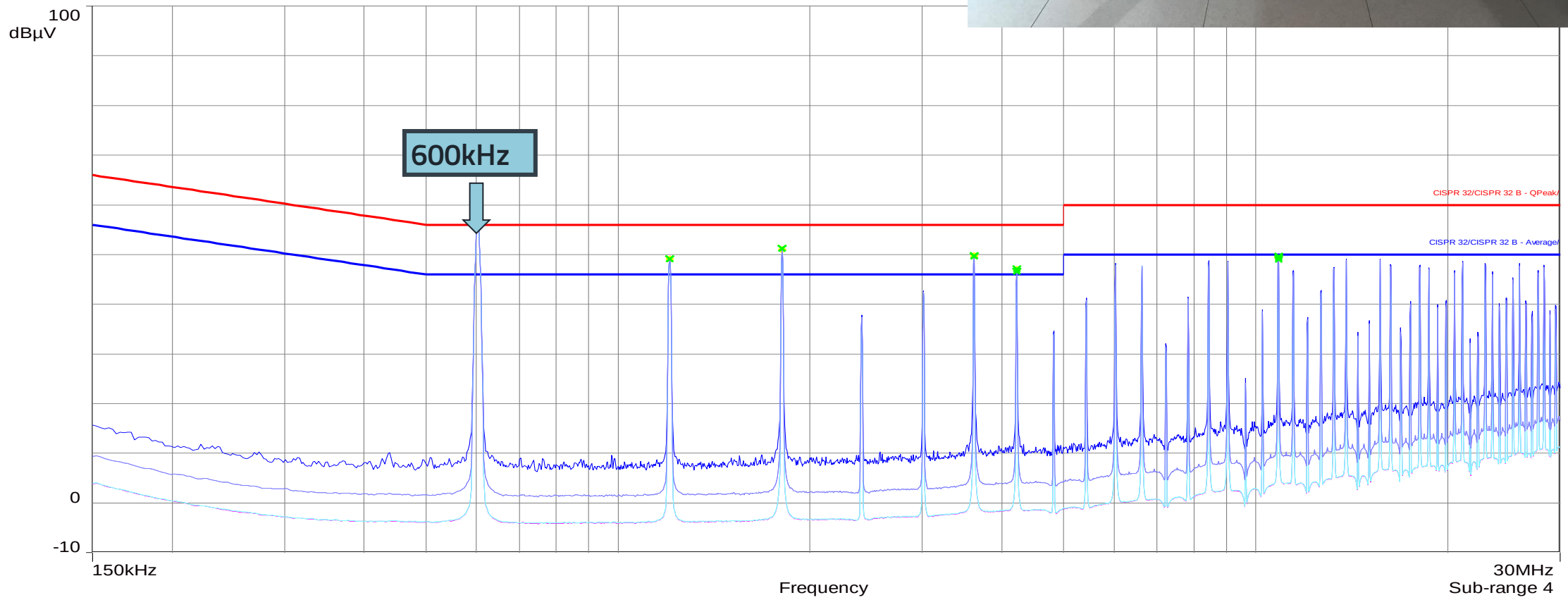




MEASURED WITH ENV216 LISN & ESRP

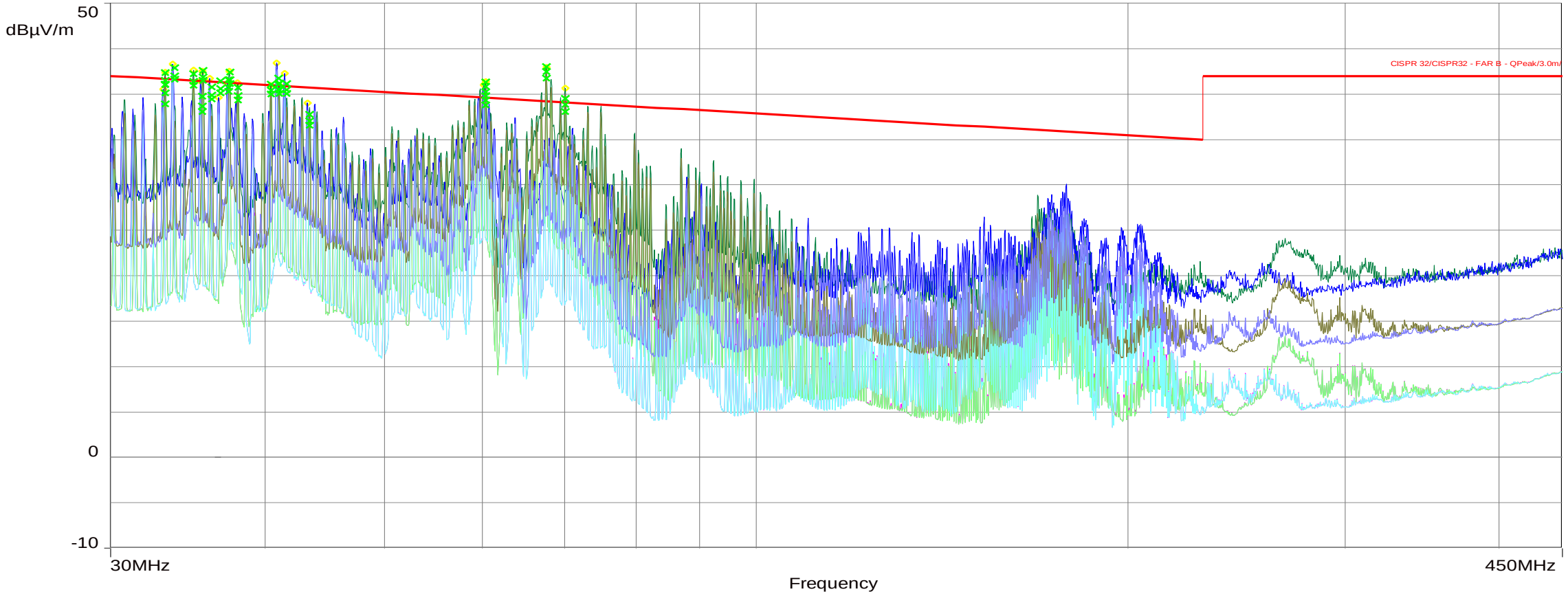
- Conducted Emission 150kHz – 30MHz
- Design (A) with Filter / Buck Mode 100W





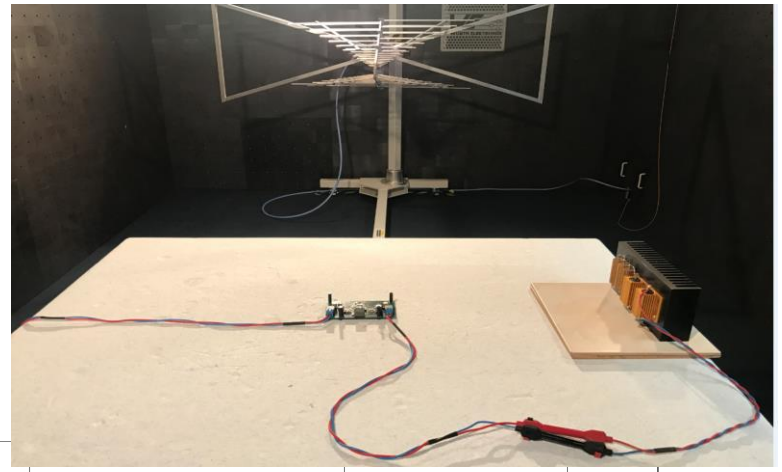
MEASUREMENT IN EMC CHAMBER

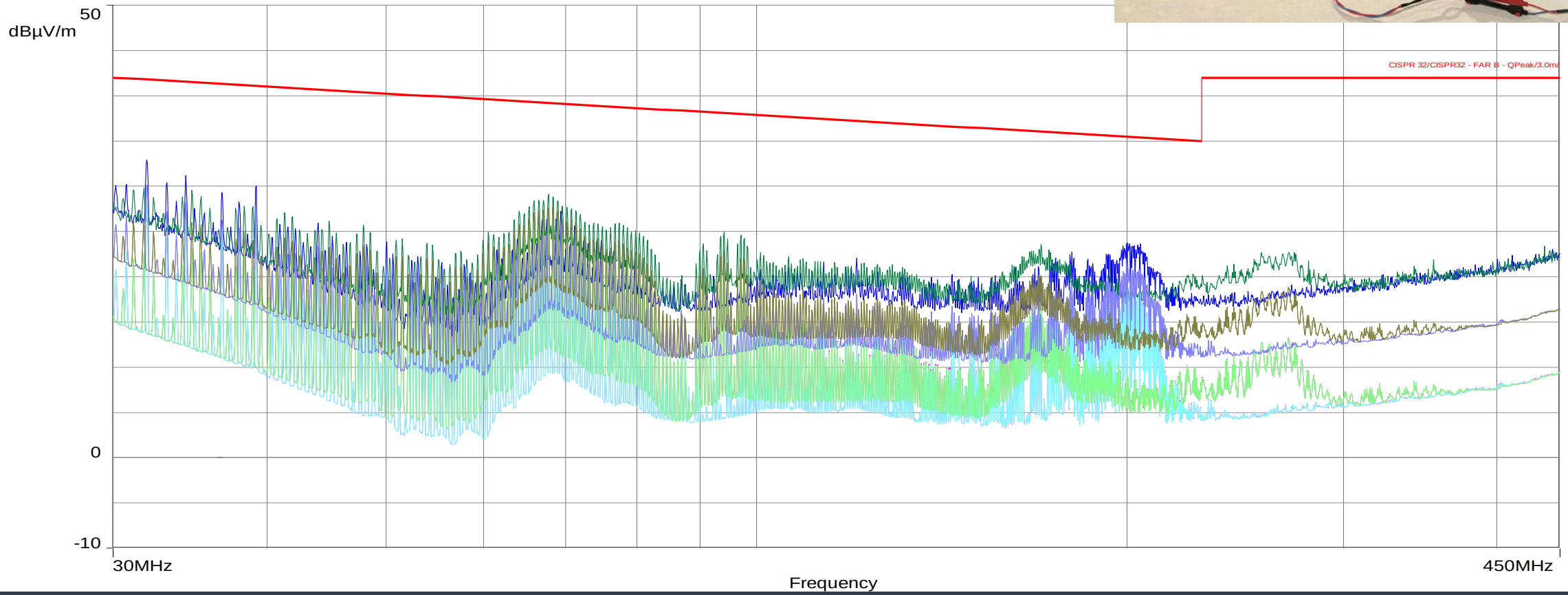
- Radiated Emission 30MHz – 450MHz
- Design (A) without Filter / Buck Mode 100W



MEASUREMENT IN EMC CHAMBER

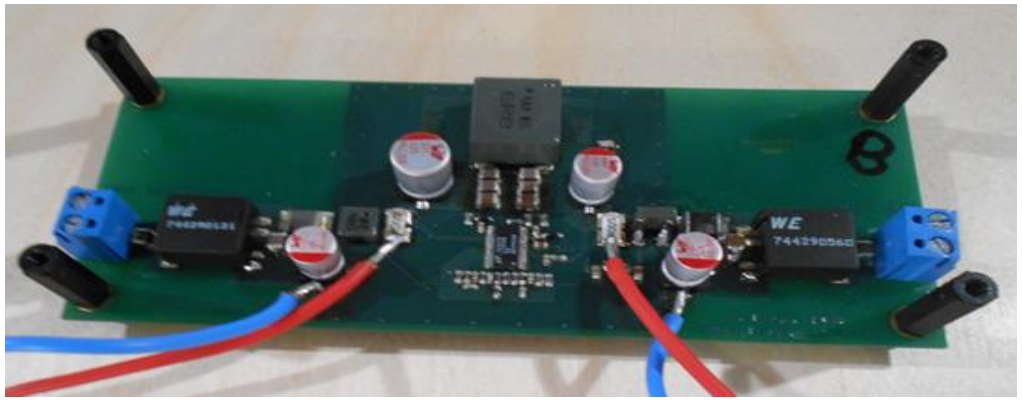
- Radiated Emission 30MHz – 450MHz
- Design (A) with Filter / Buck Mode 100W

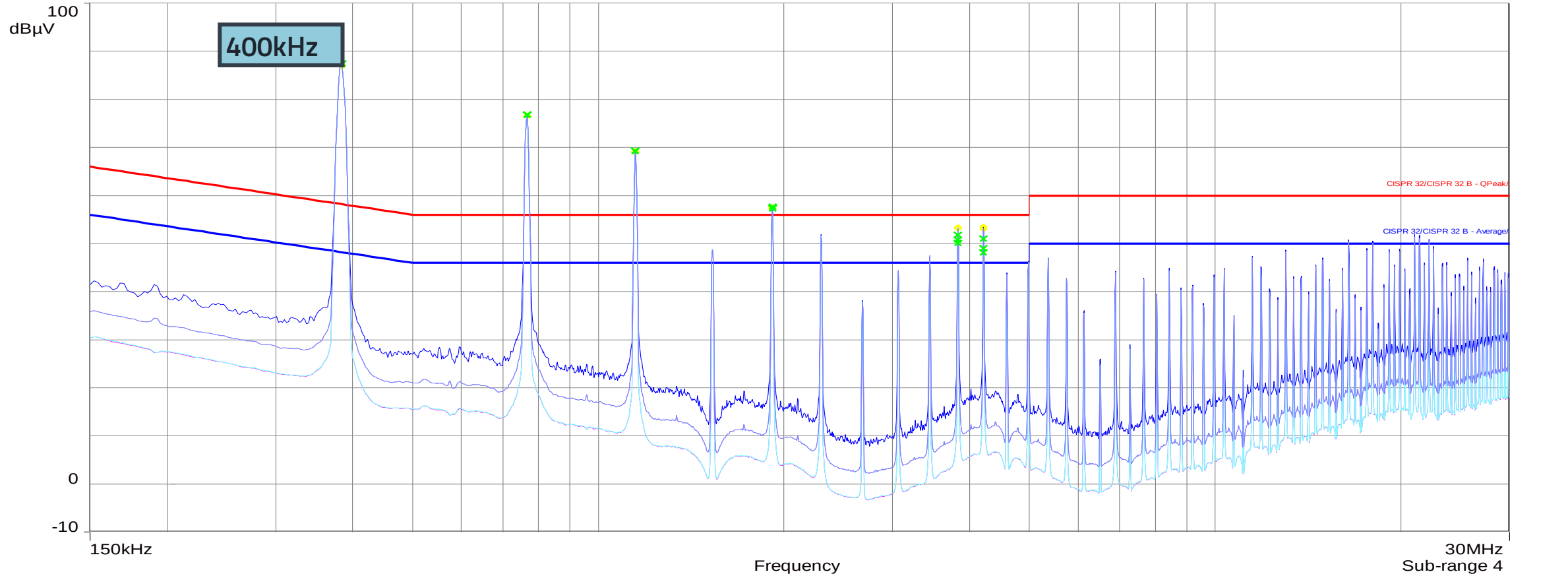




MEASURED WITH ENV216 LISN & ESRP

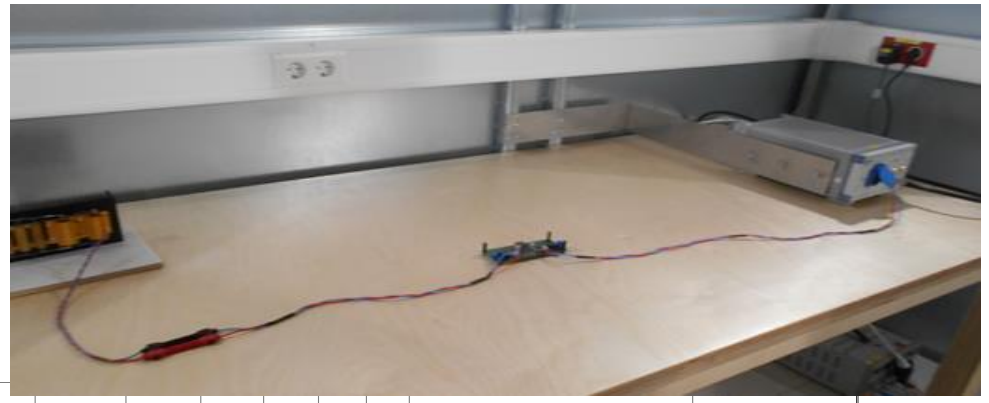
- Conducted Emission 150kHz – 30MHz
- Design (B) without Filter / Buck Mode 100W

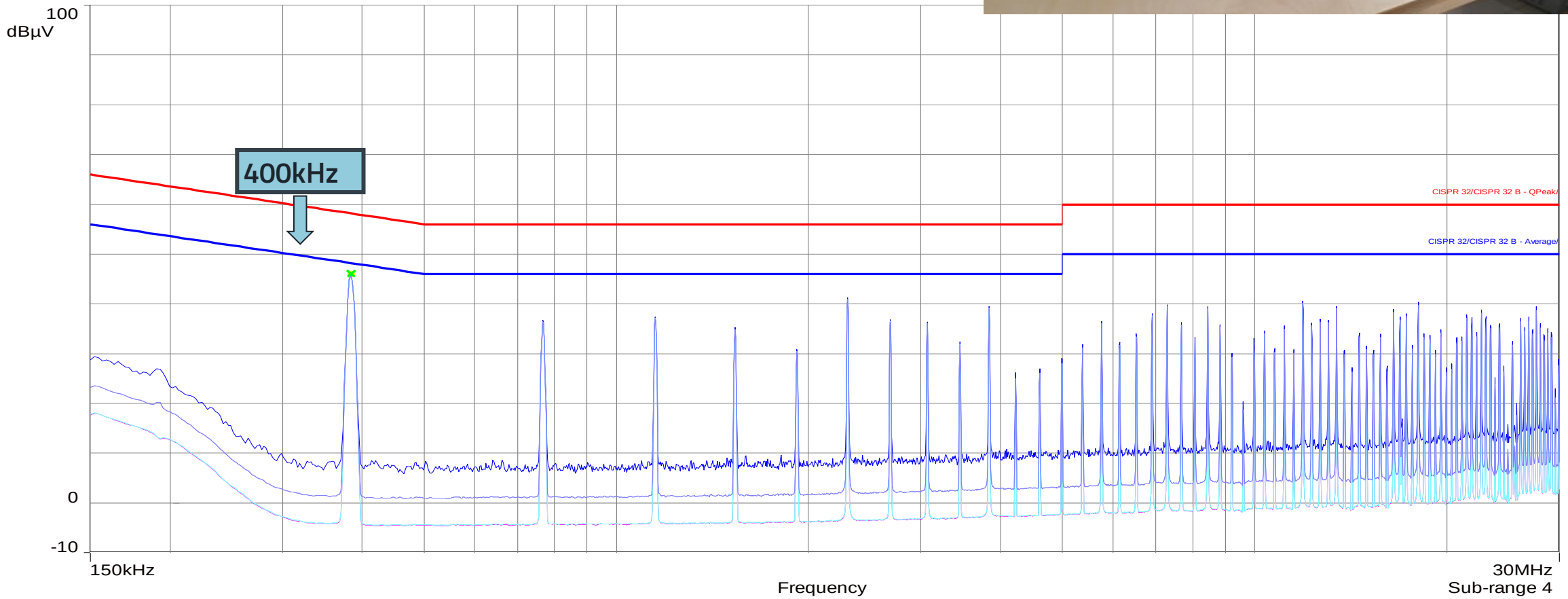




MEASURED WITH ENV216 LISN & ESRP

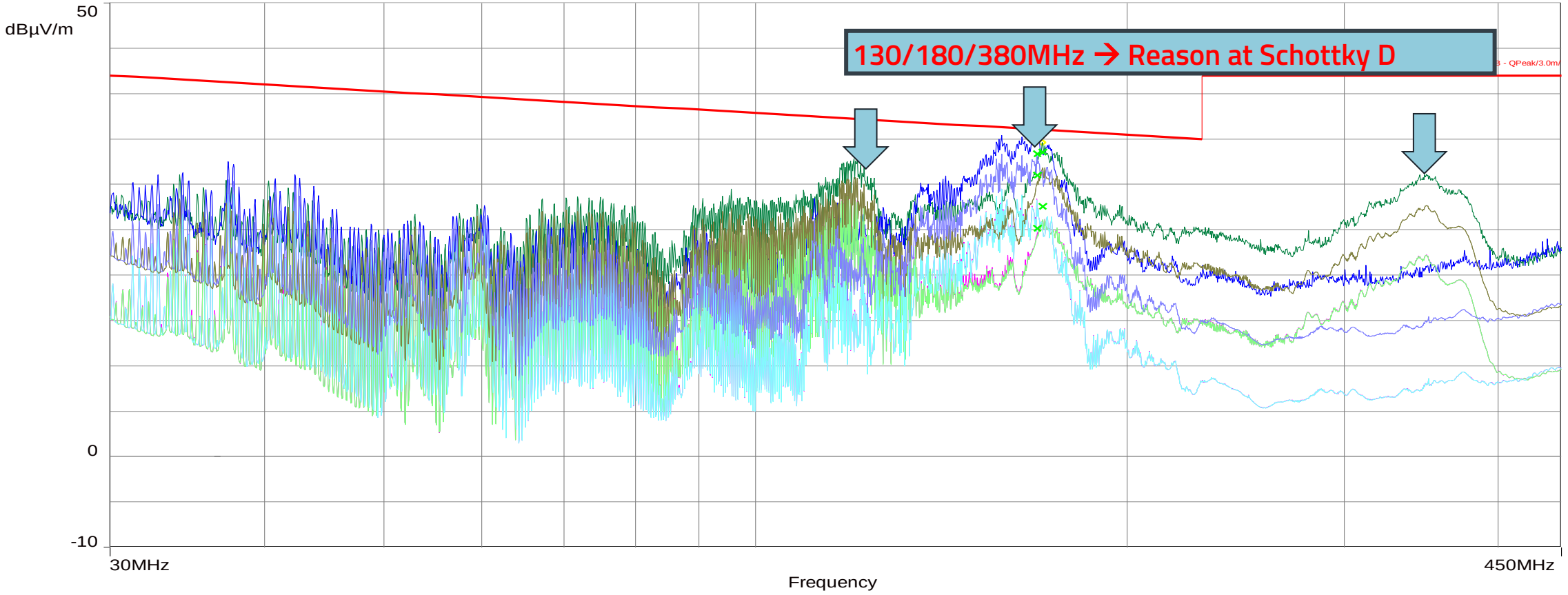
- Conducted Emission 150kHz – 30MHz
- Design (B) with Filter / Buck Mode 100W





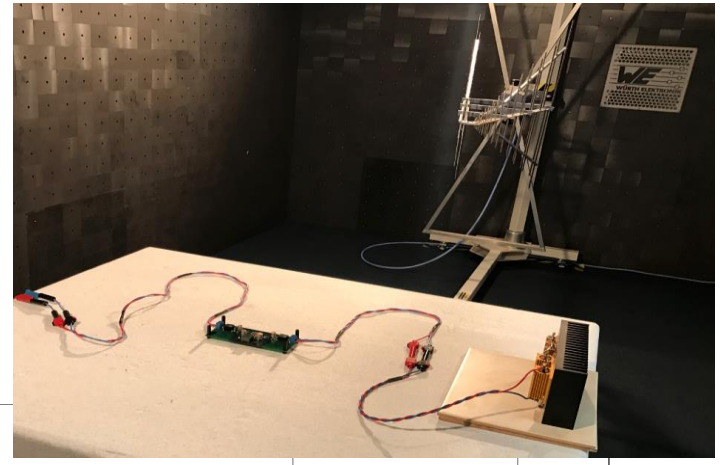
MEASUREMENT IN EMC CHAMBER

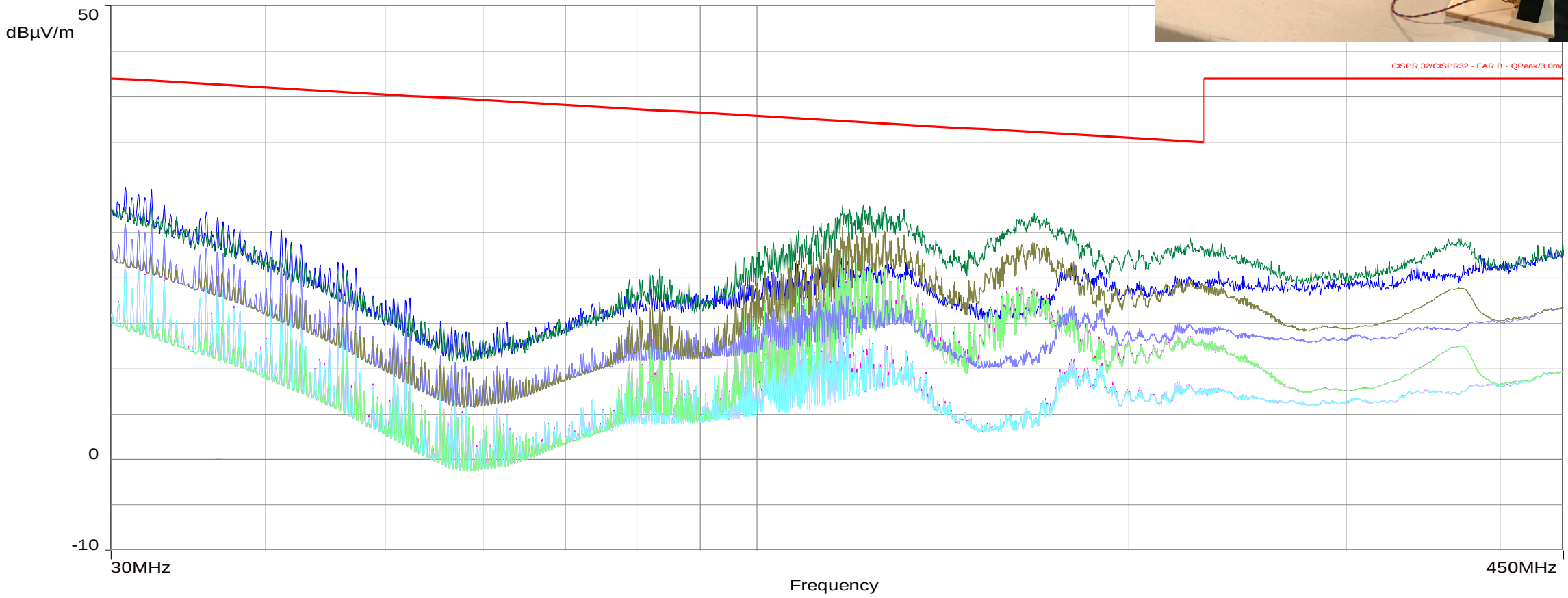
- Radiated Emission 30MHz – 450MHz
- Design (B) without Filter / Buck Mode 100W



MEASUREMENT IN EMC CHAMBER

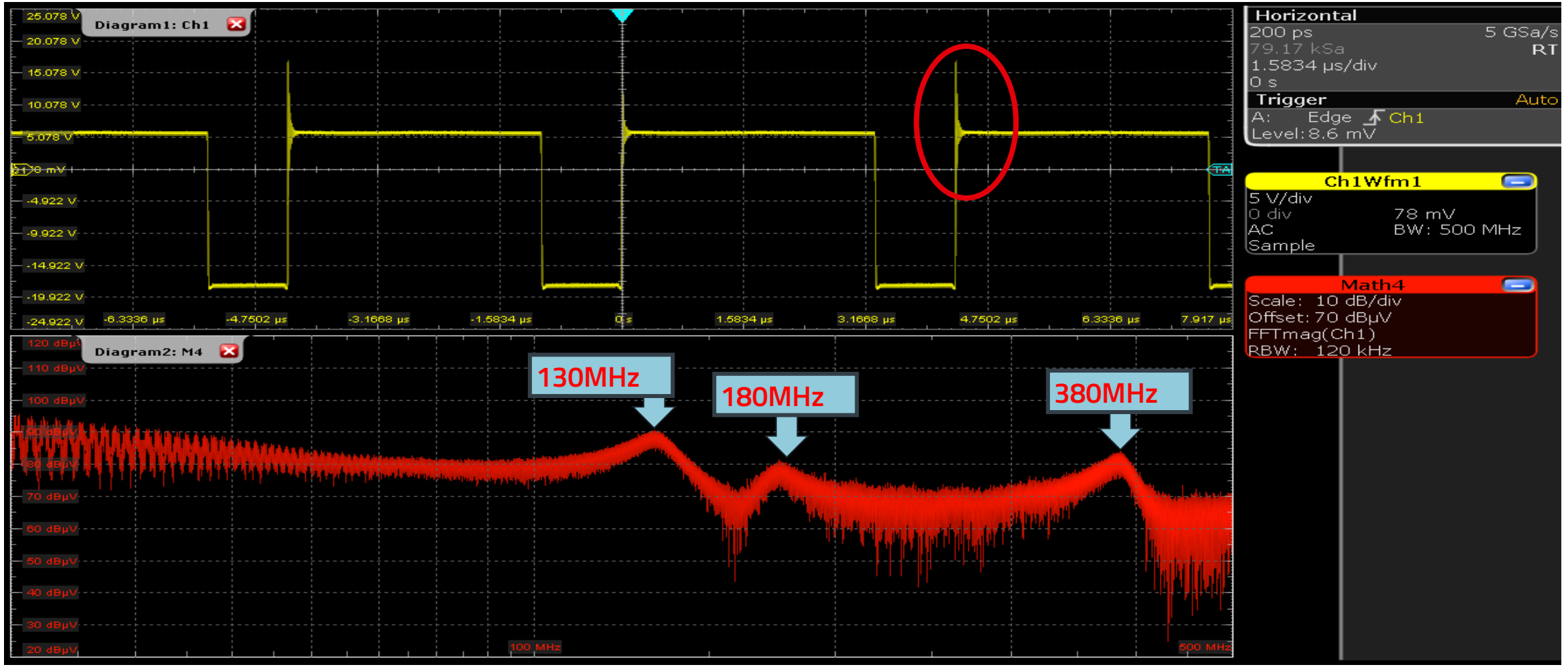
- Radiated Emission 30MHz – 450MHz
- Design (B) with Filter / Buck Mode 100W



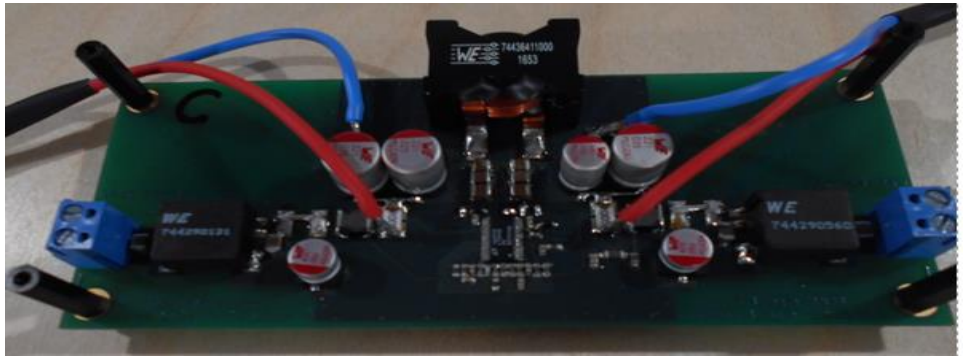


MEASUREMENT AT THE SCHOTTKY

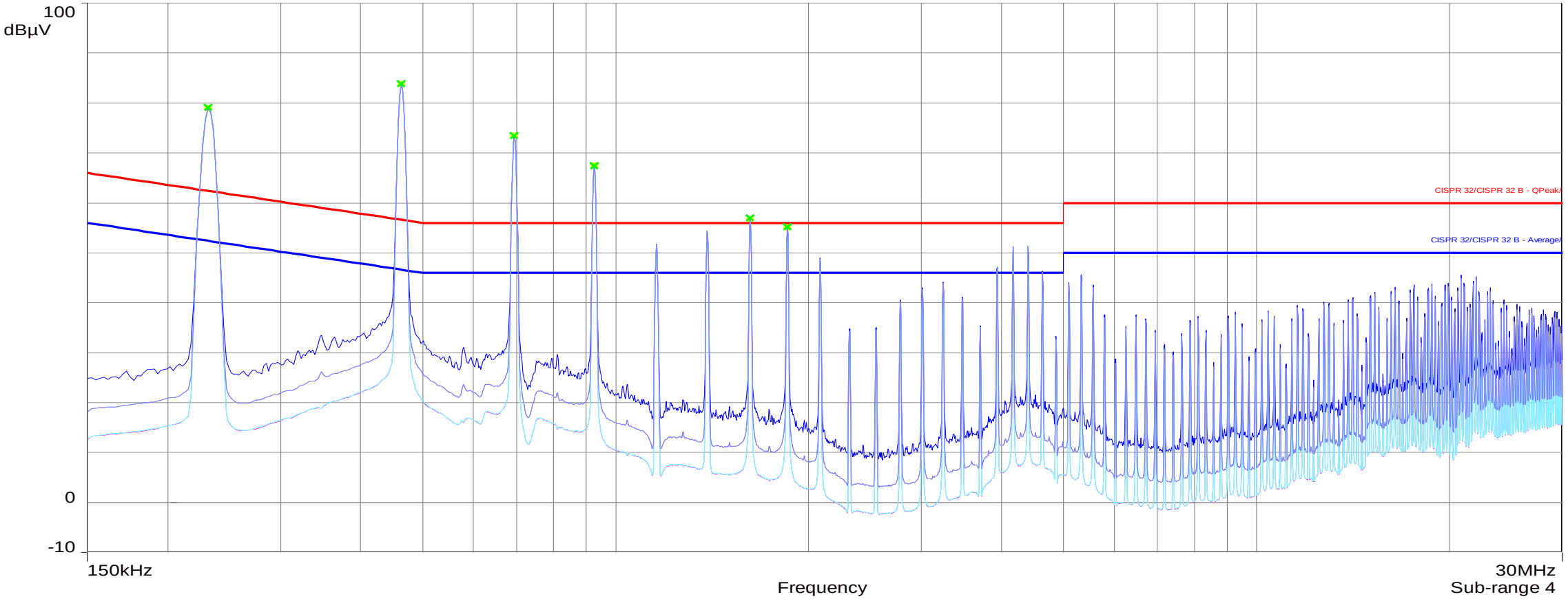
- Measured with R&S RTO at the Schottky D (Buck Leg)



MEASURED WITH ENV216 LISN & ESRP

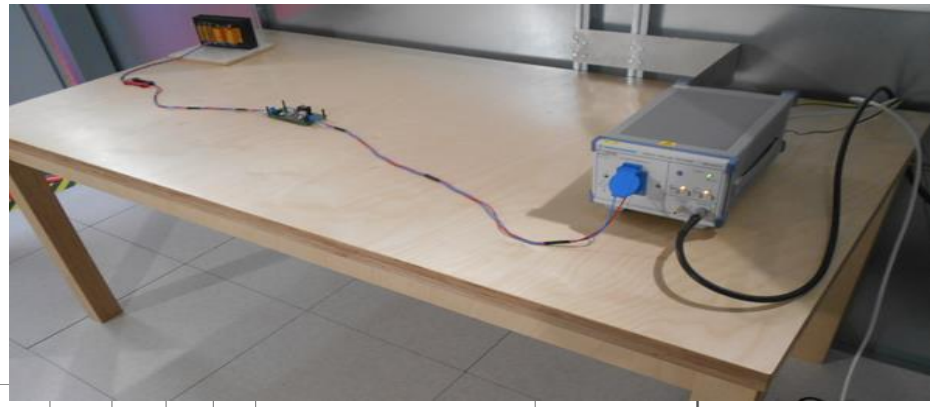


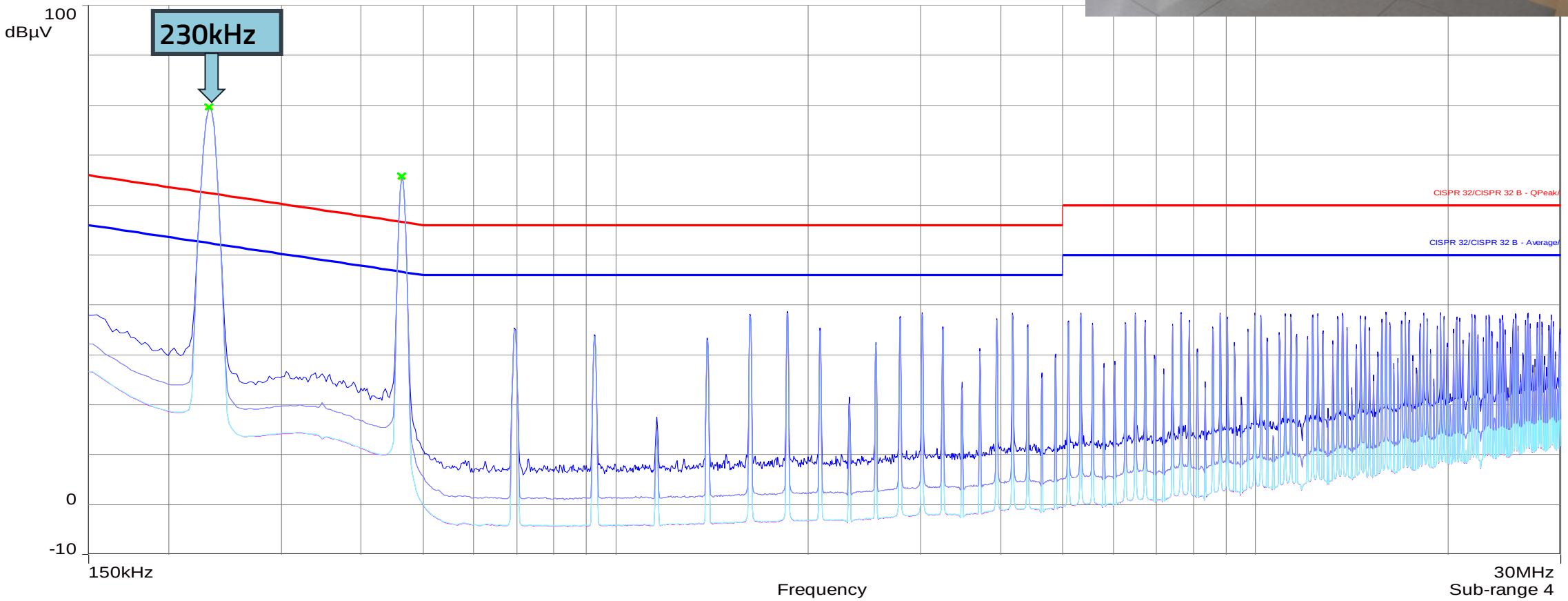
- Conducted Emission 150kHz – 30MHz
- Design (C) without Filter / Buck Mode 100W



MEASURED WITH ENV216 LISN & ESRP

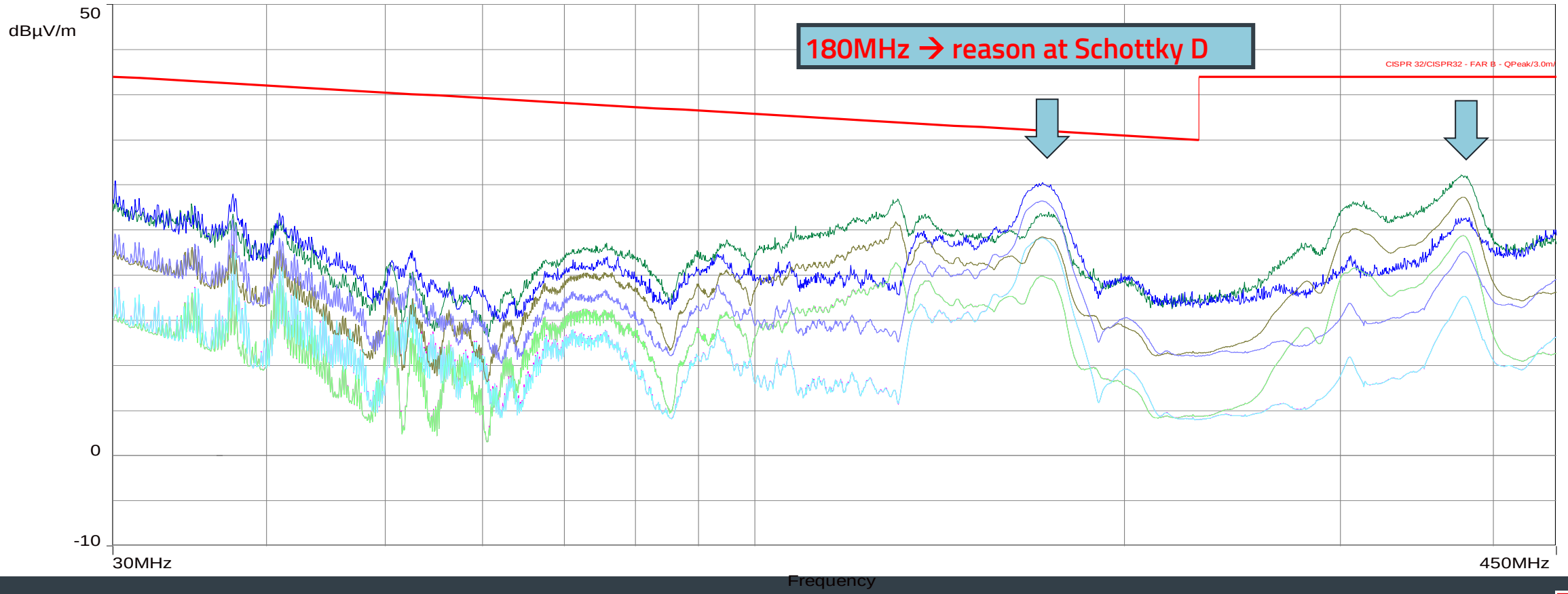
- Conducted Emission 150kHz – 30MHz
- Design (C) with Filter / Buck Mode 100W





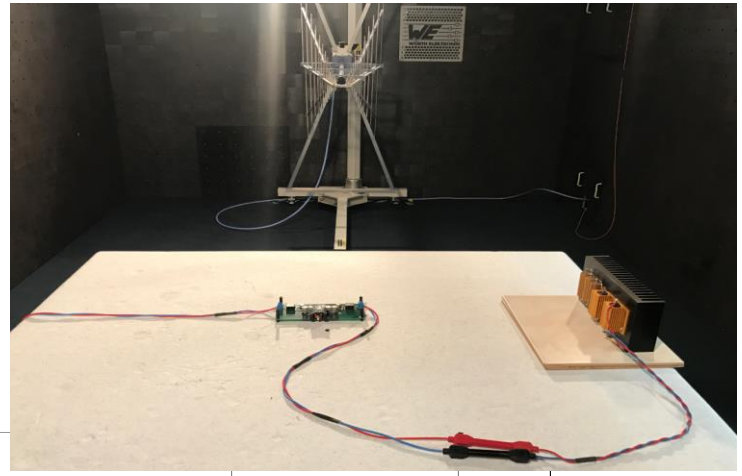
MEASUREMENT IN EMC CHAMBER

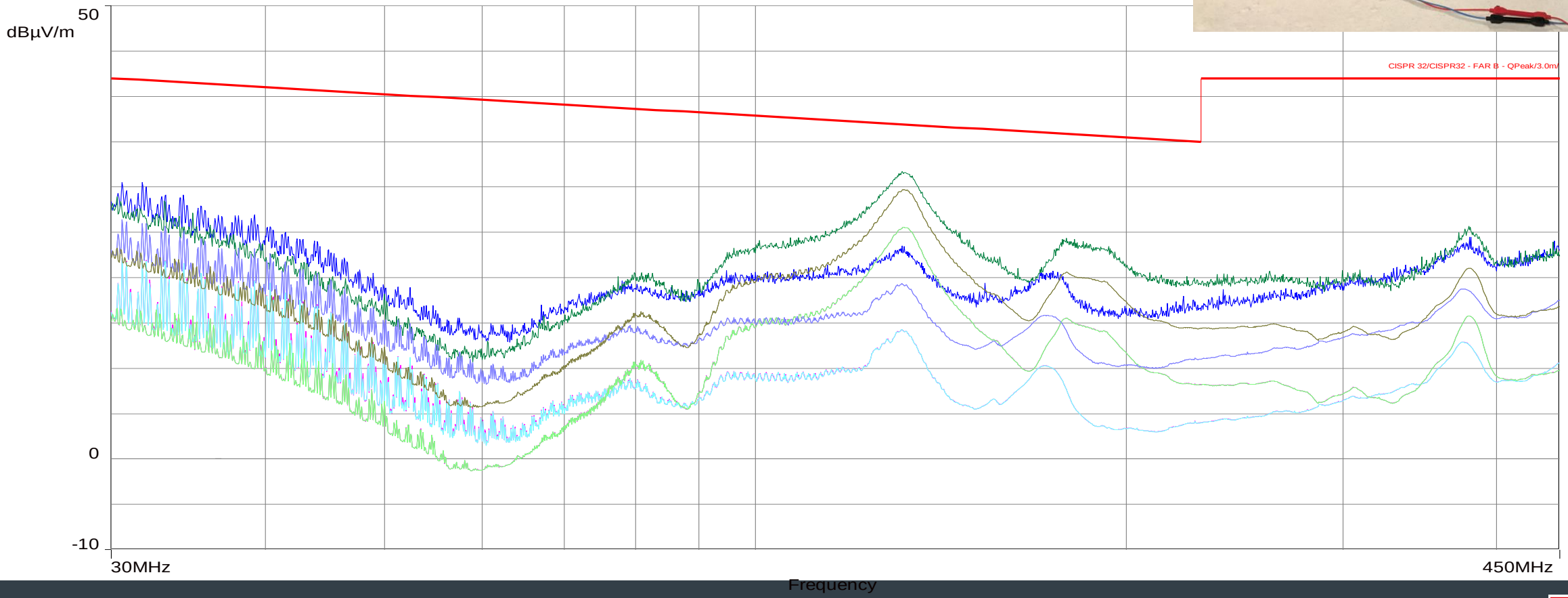
- Radiated Emission 30MHz – 450MHz
- Design (C) without Filter / Buck Mode 100W



MEASUREMENT IN EMC CHAMBER

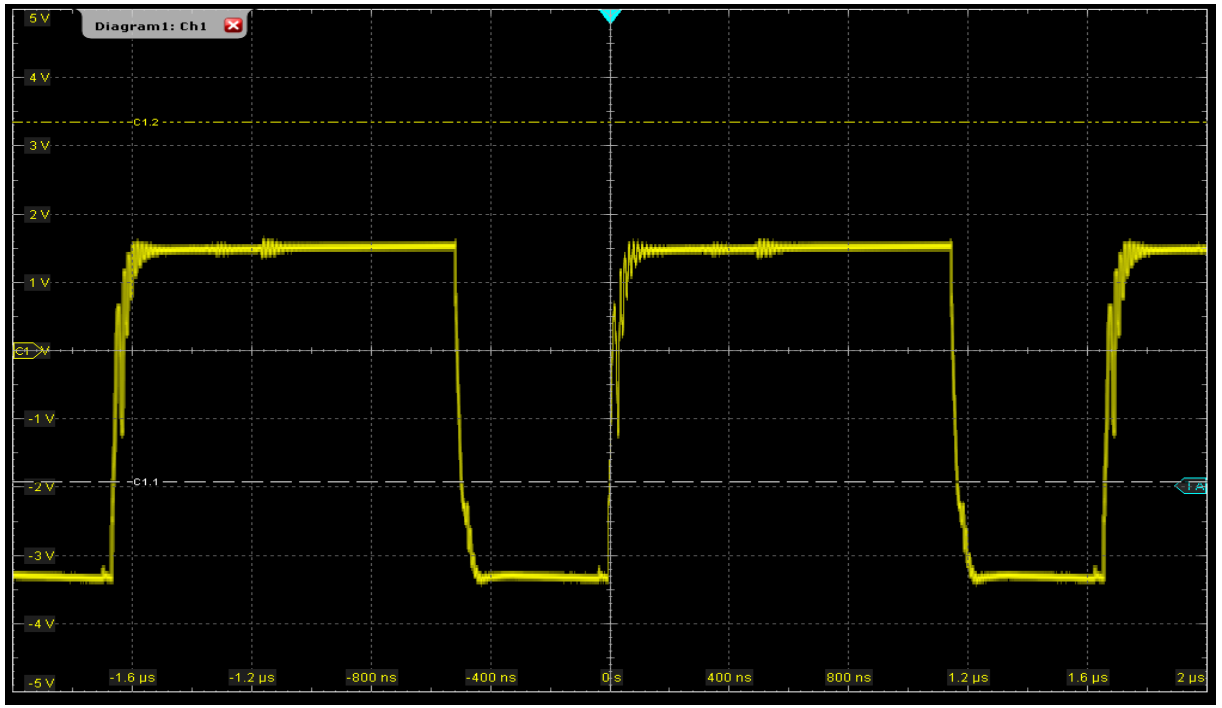
- Radiated Emission 30MHz – 450MHz
- Design (C) with Filter / Buck Mode 100W

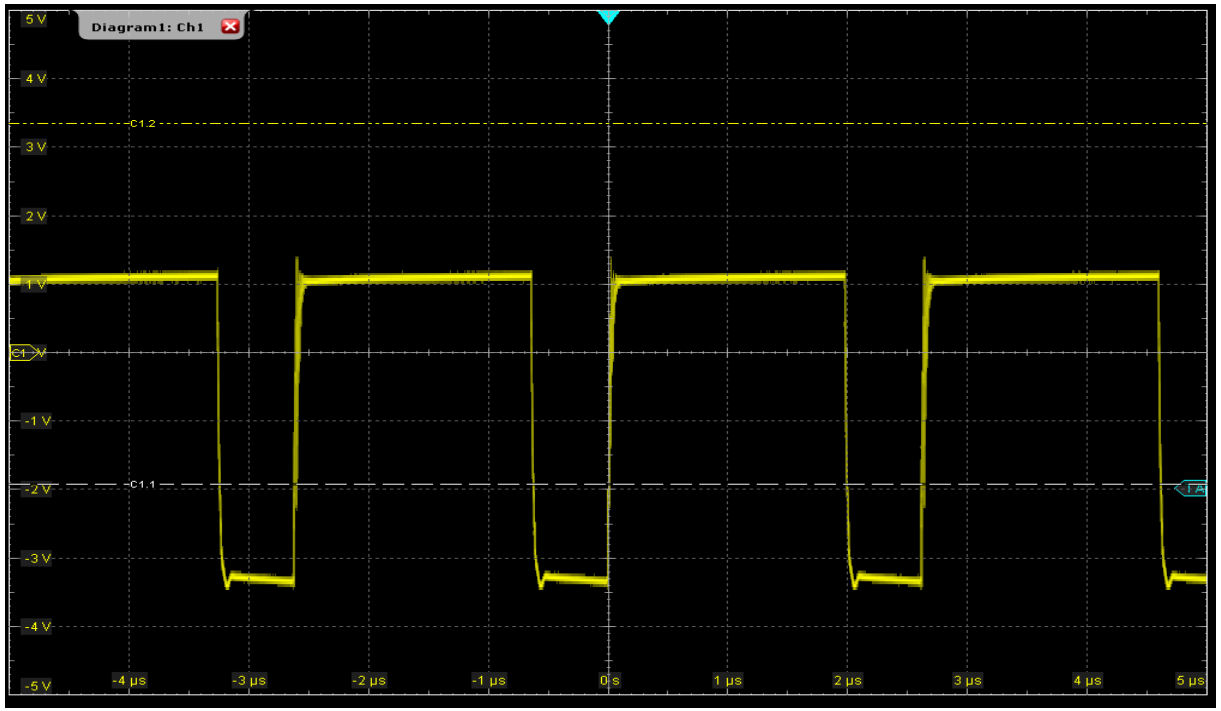




MEASURING DIRECT AT THE COMPONENTS

GATE SOURCE VOLTAGE FROM HIGH SIDE FET

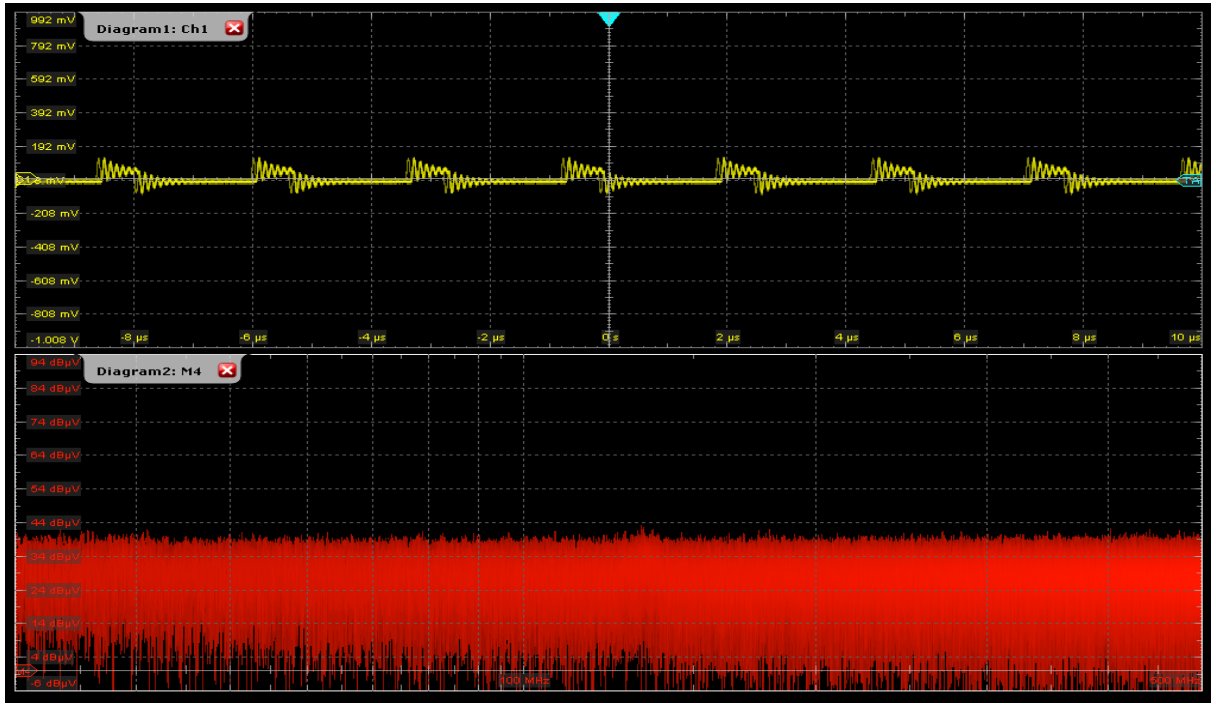


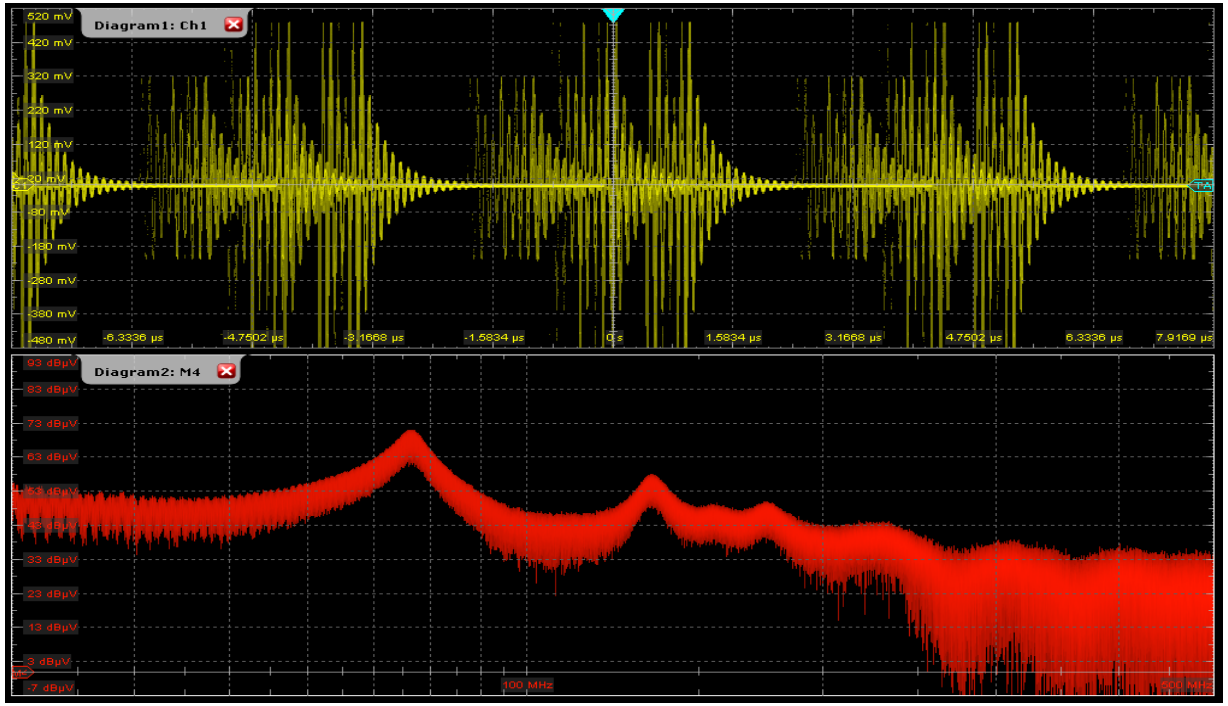


- **Vgs Design (A)**
- **Vgs Design (B)**

Reason: The improved layout and the smaller package of the MOSFET

MEASURED WITH H-FIELD PROBE DESIGN (B) 30MHZ-500MHZ

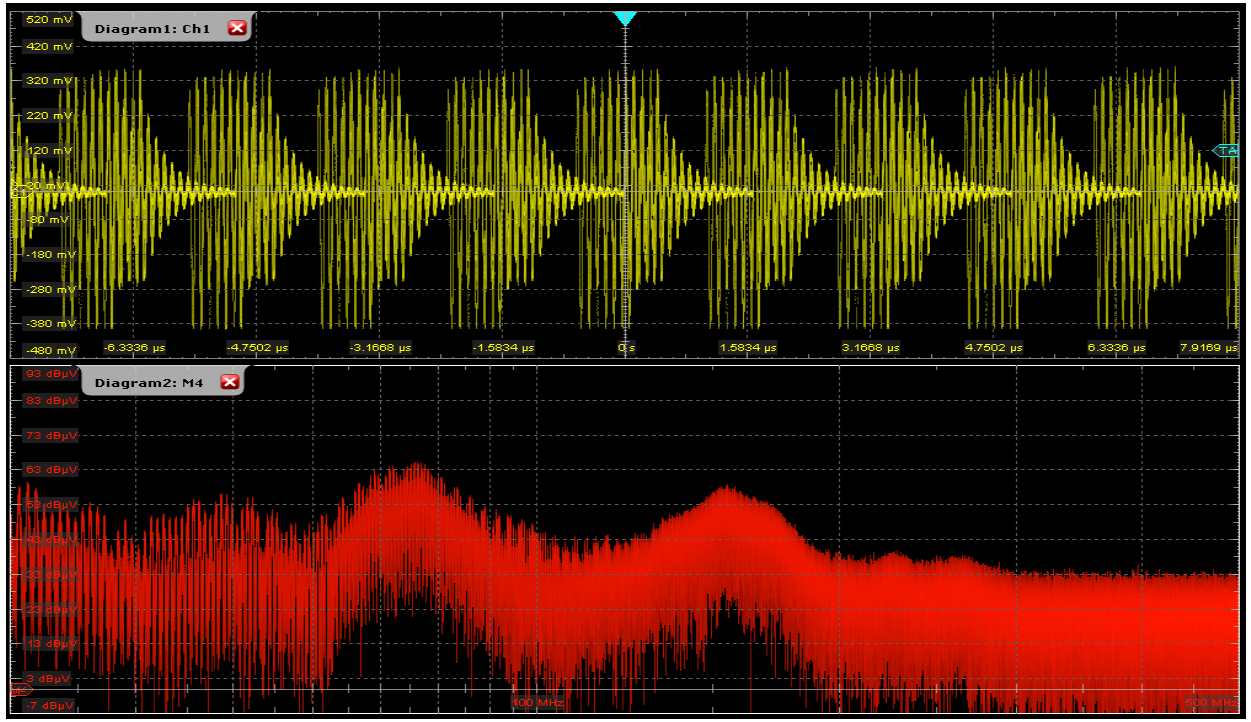


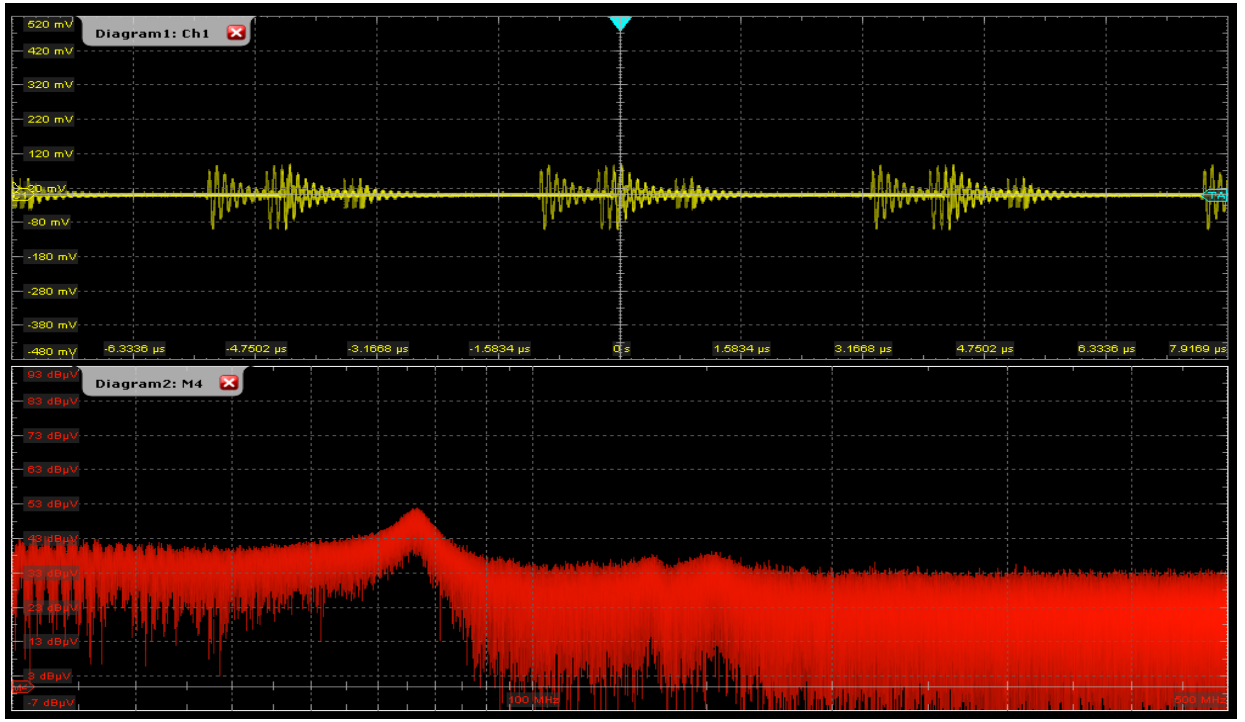


- Measured at the storage inductor
- Measured at the High Side MOSFET

➢ The reason for radiation is not the inductor for sure!

MEASURED WITH H-FIEL PROBE AT THE BOOSTRAP DIODE 30MHZ-500MHZ



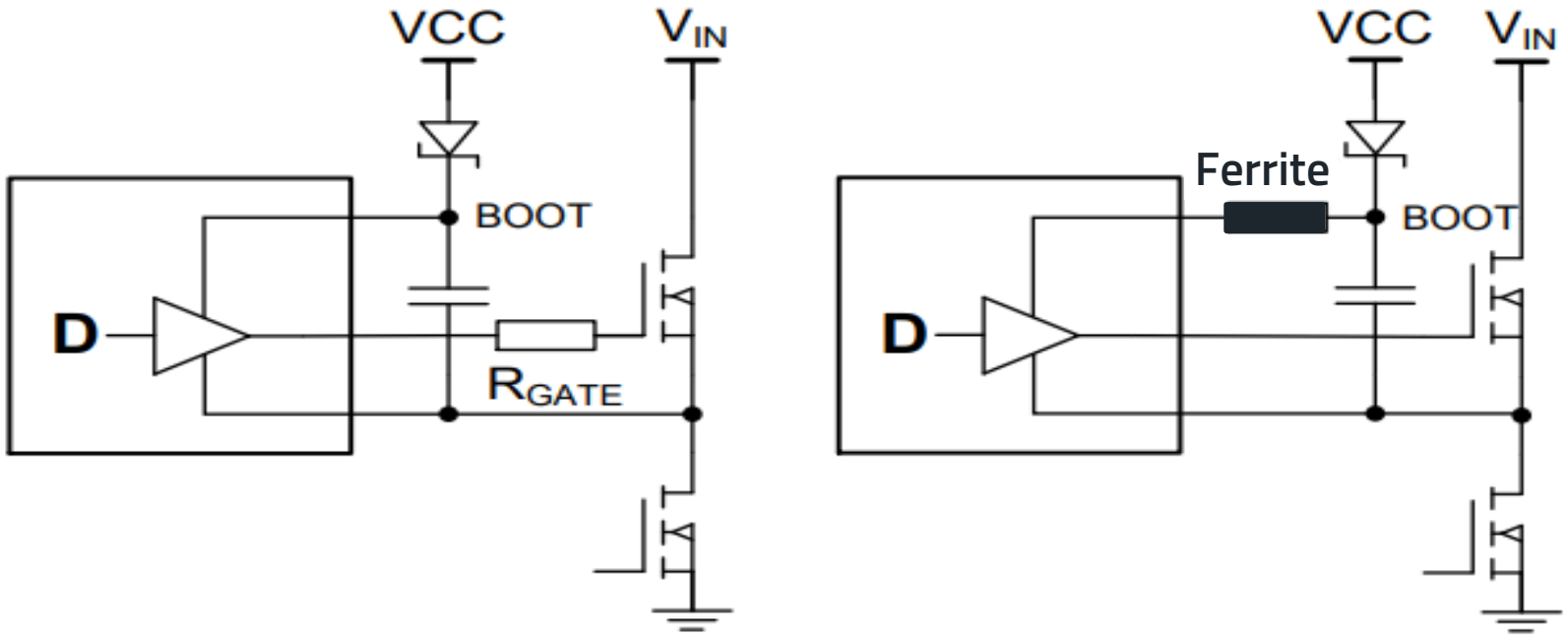


- Boostrap Design (A)
- Bootstrap Design (B)

➢ The improved layout and using an other diode improve of lot

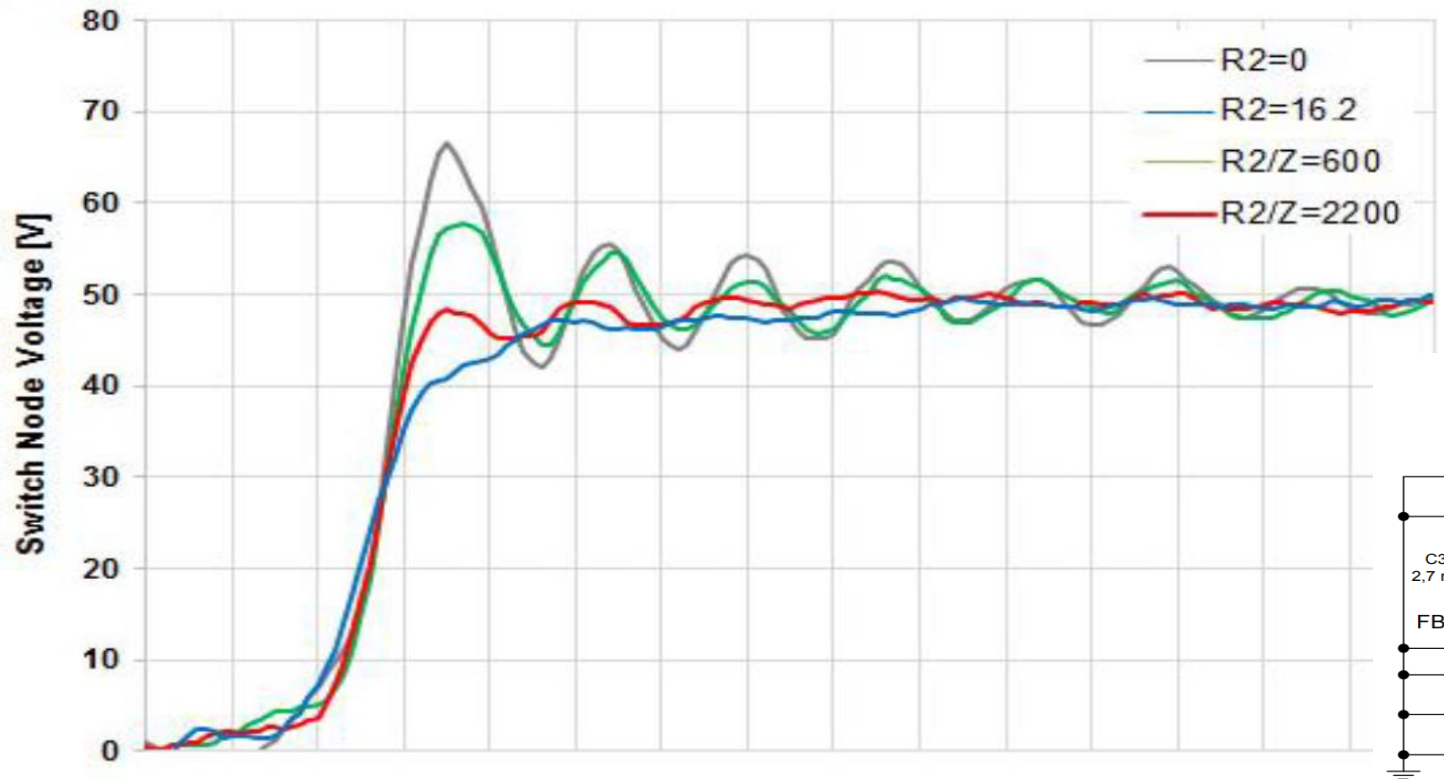
ALTERNATIVE: FERRIT IN BOOSTRAP ADDED (WÜRTH ELEKTRONIK APPNOTE ANP025)

- Advantage: only the rise time afected → More efficient as using a resistor at Gate

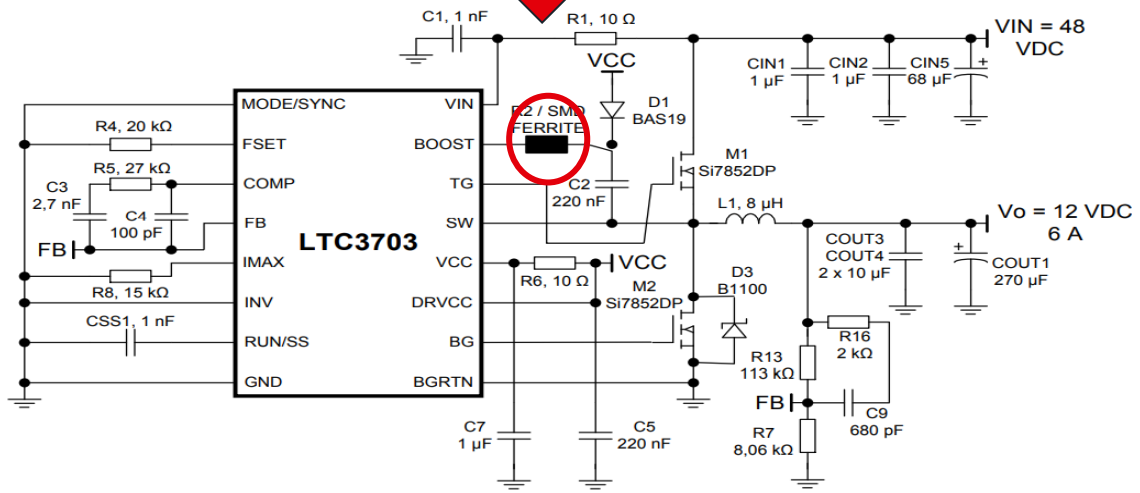


ALTERNATIVE: FERRIT IN BOOSTRAP ADDED (WÜRTH ELEKTRONIK APPNOTE ANP025)

- Measurement made by an LTC3703 Demo Board using different Boostrap resistors / Chip Bead Ferrite (CBF)

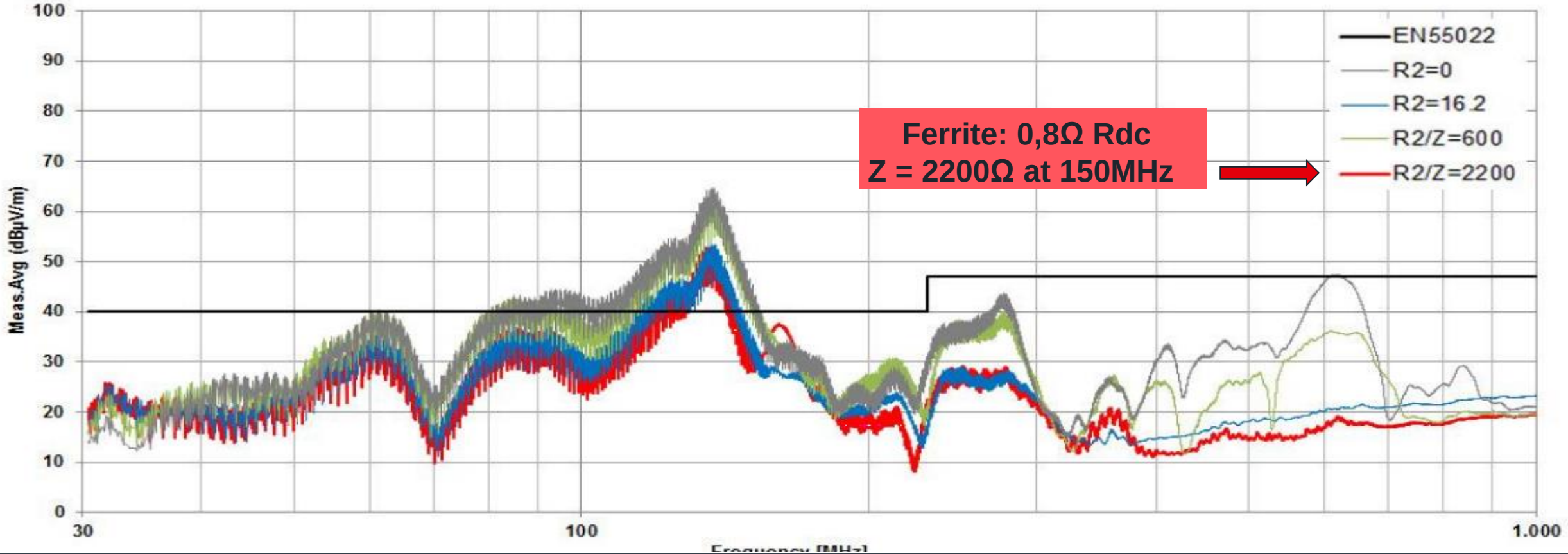


Ferrite: 0,8Ω RDC
Z= 2200Ω at 150MHz



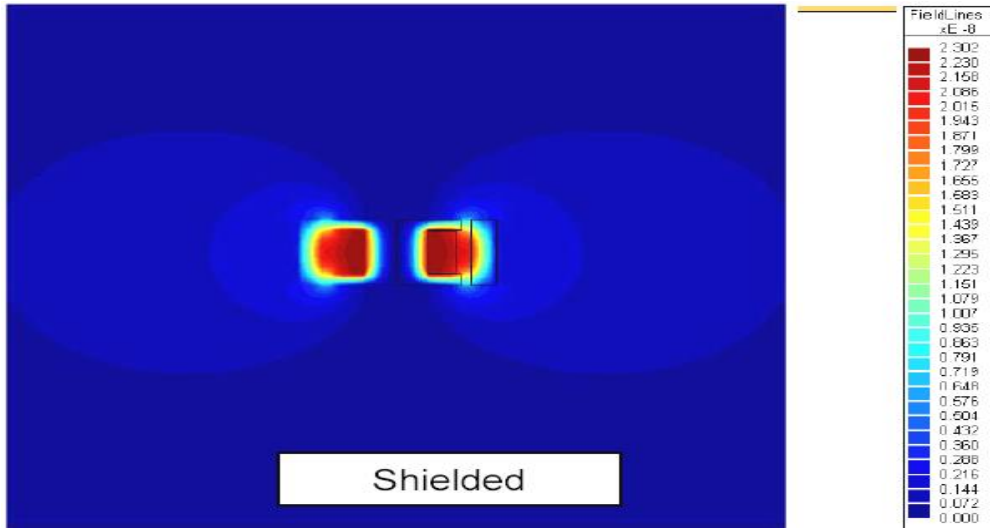
ALTERNATIVE: FERRIT IN BOOSTRAP ADDED (WÜRTH ELEKTRONIK APPNOTE ANP025)

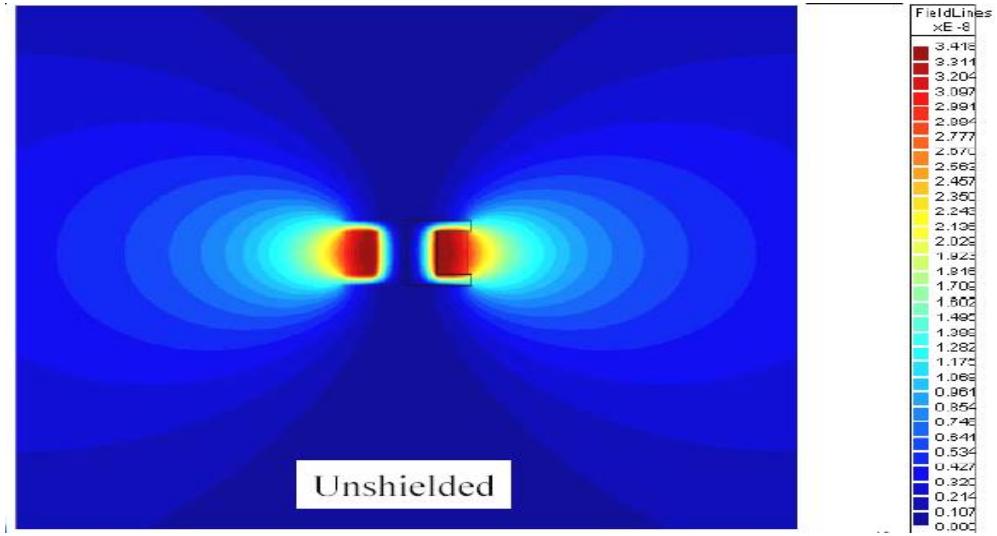
- EMC measurement made by an LTC3703 Demo Board using differnt Boostrap resistors & Chip Bead Ferrite (CBF)

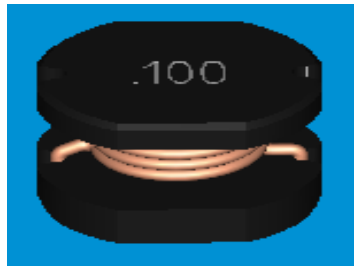


SHIELD VS. UNSHIELD

MAGNETIC FIELD LEAKAGE





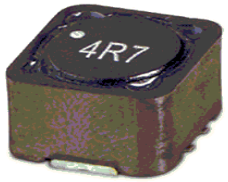


RADIATION BY INDUCTOR

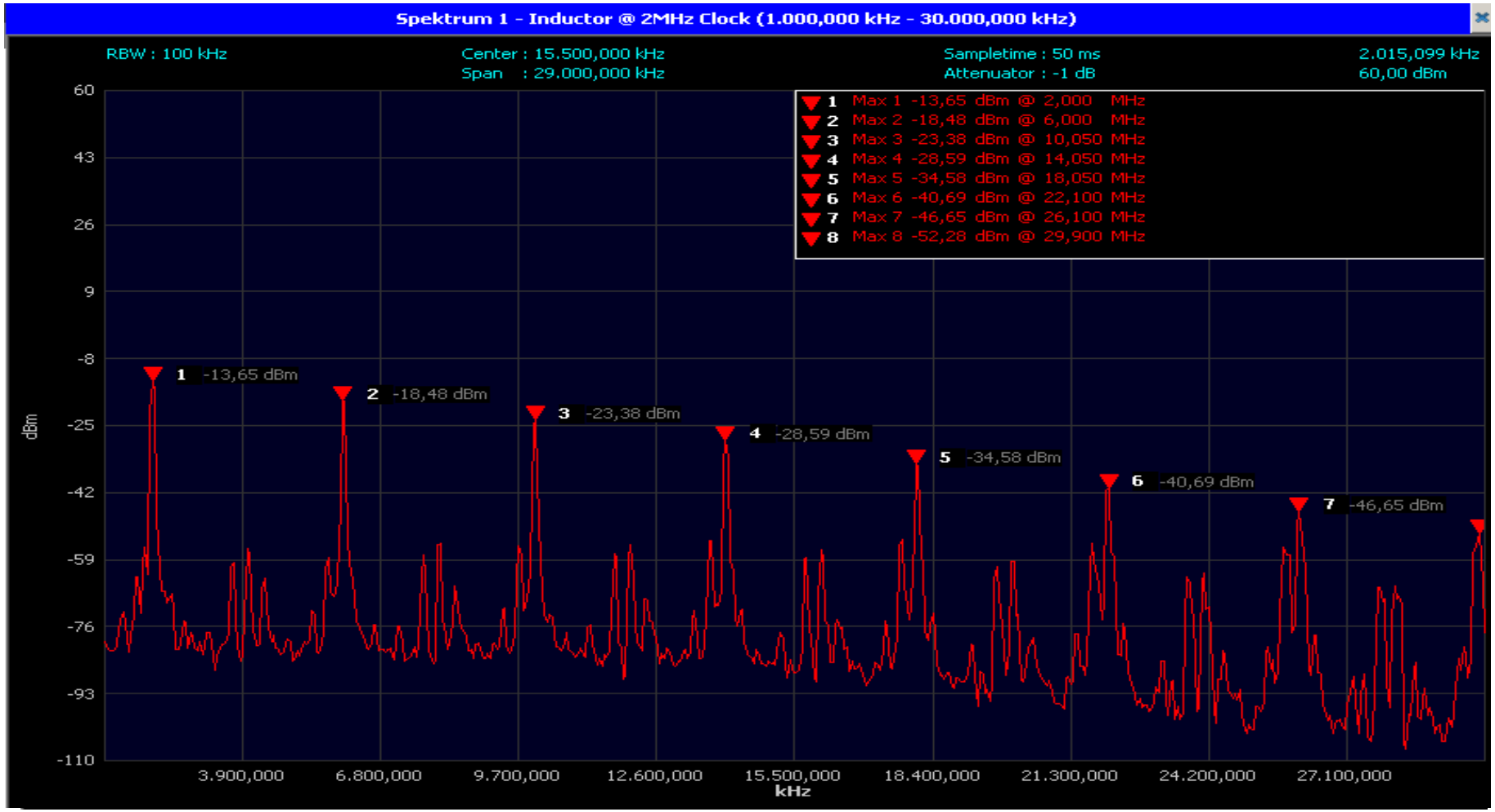
WE - PD2 unshielded
10µH, 2MHz Clock, 1A

WE – PD shielded

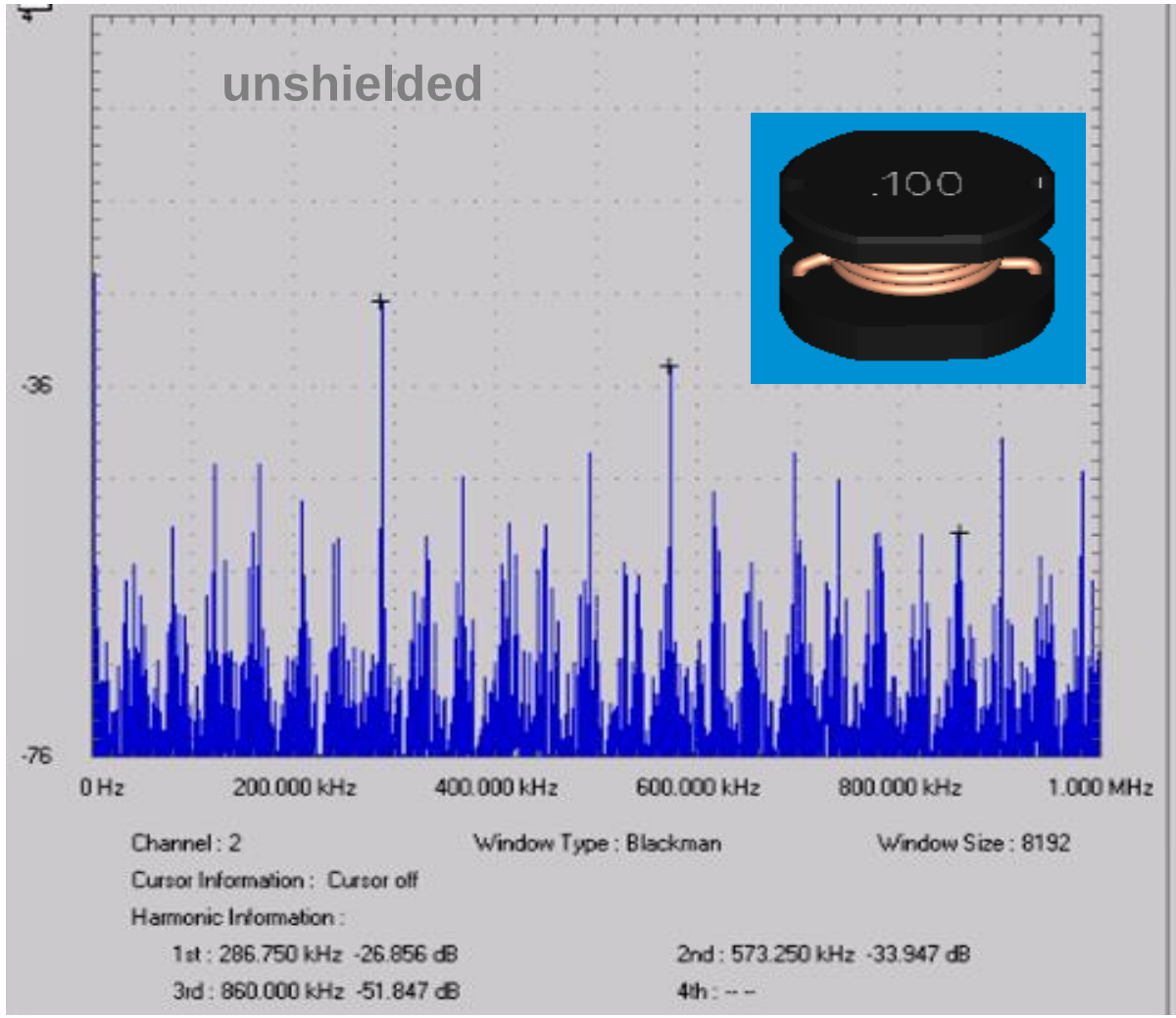
10µH, 2MHz Clock, 1A

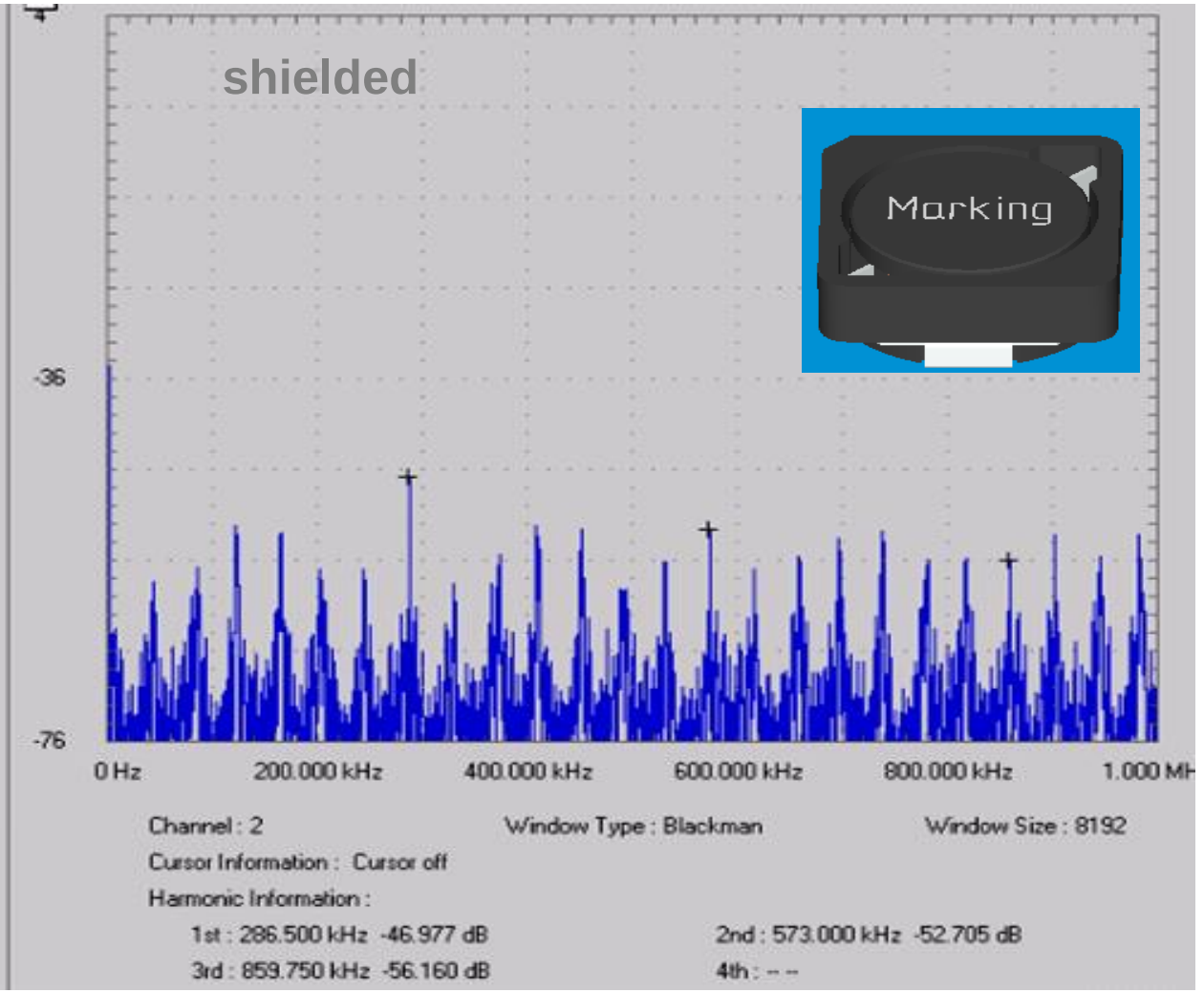


19dBm difference



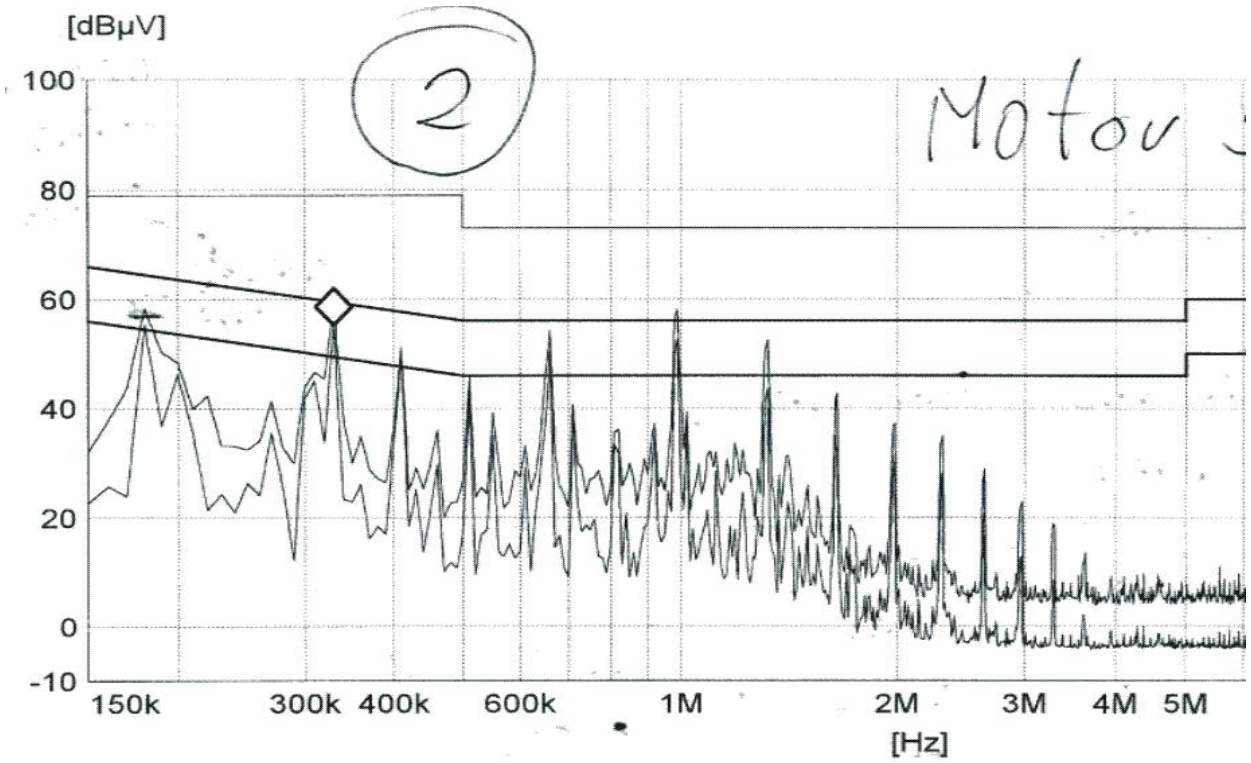
Magnetic leakage shielded vs. unshielded

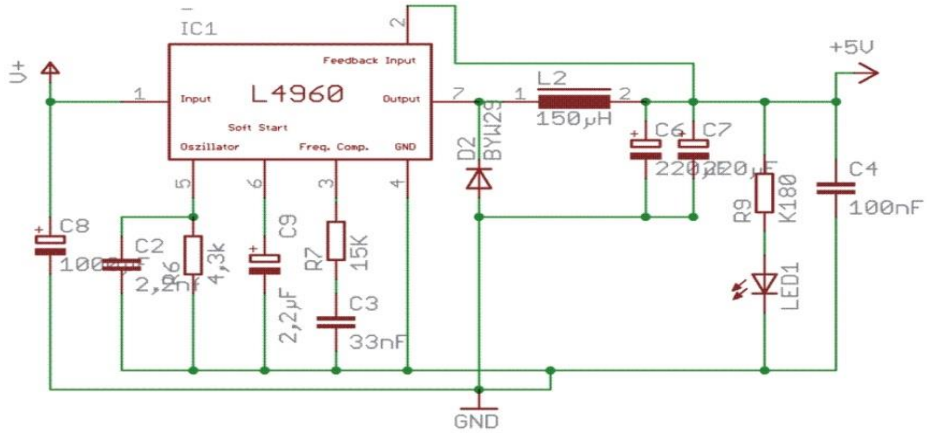




MAGNETIC FIELDS – CONDUCTED EMISSION MEASUREMENT

Power supply V 1.0

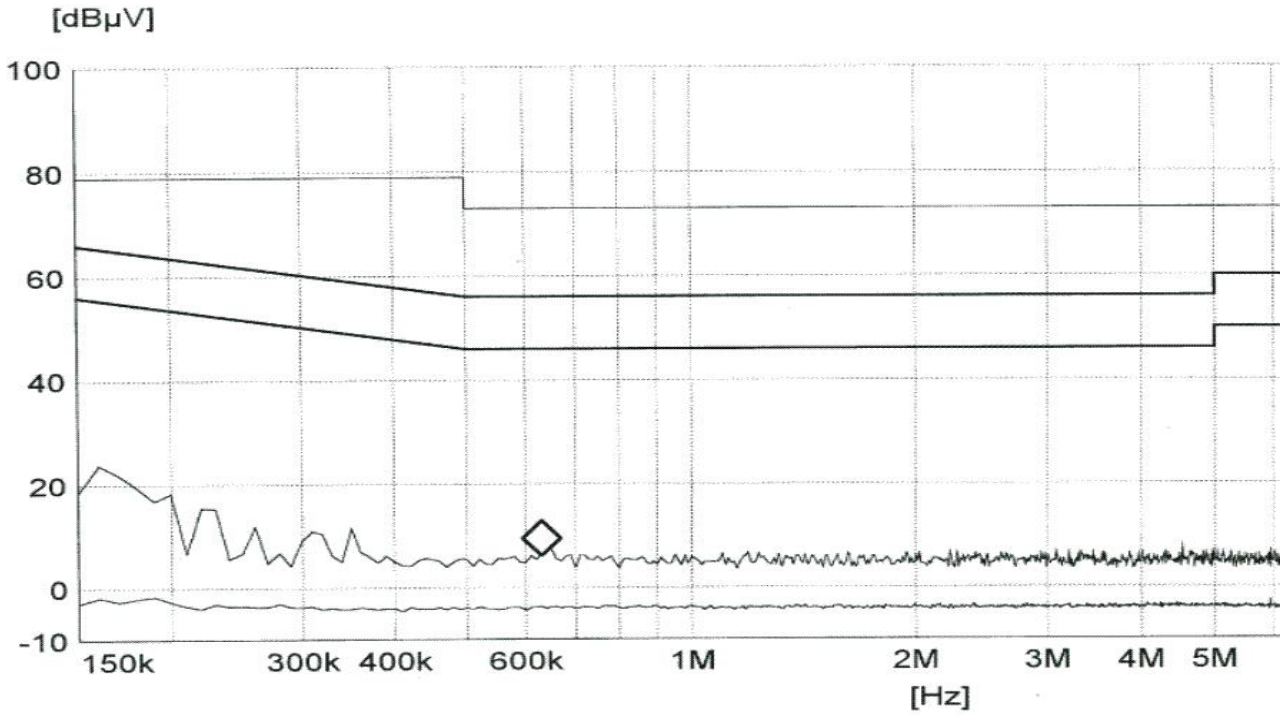


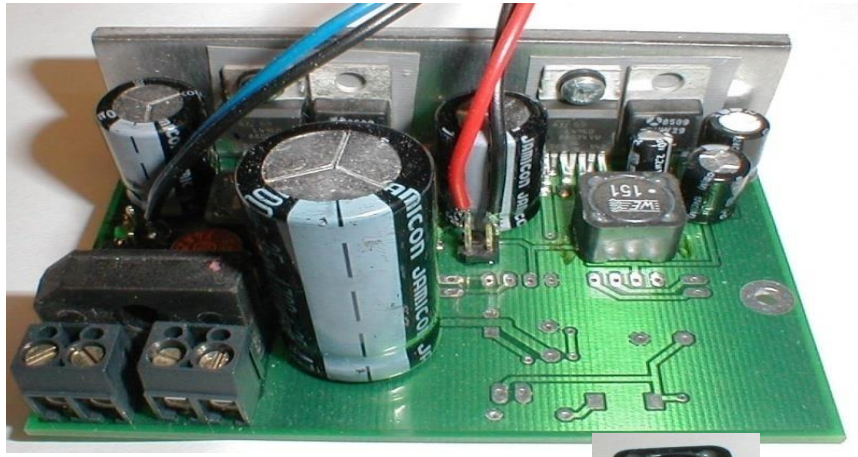


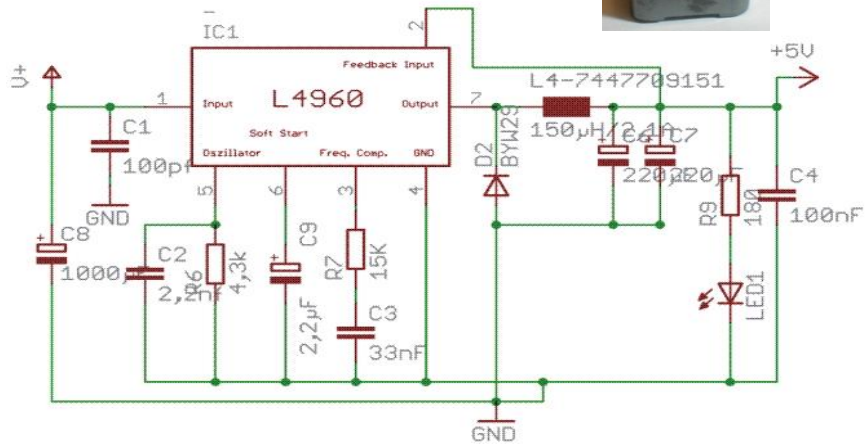
Buck Converter ST L4960/2.5A/fs 85-115KHz

MAGNETIC FIELDS – CONDUCTED EMISSION MEASUREMENT

Power supply V 1.1







TECHNICAL SUPPORT NEEDED?

use: #askLorandt

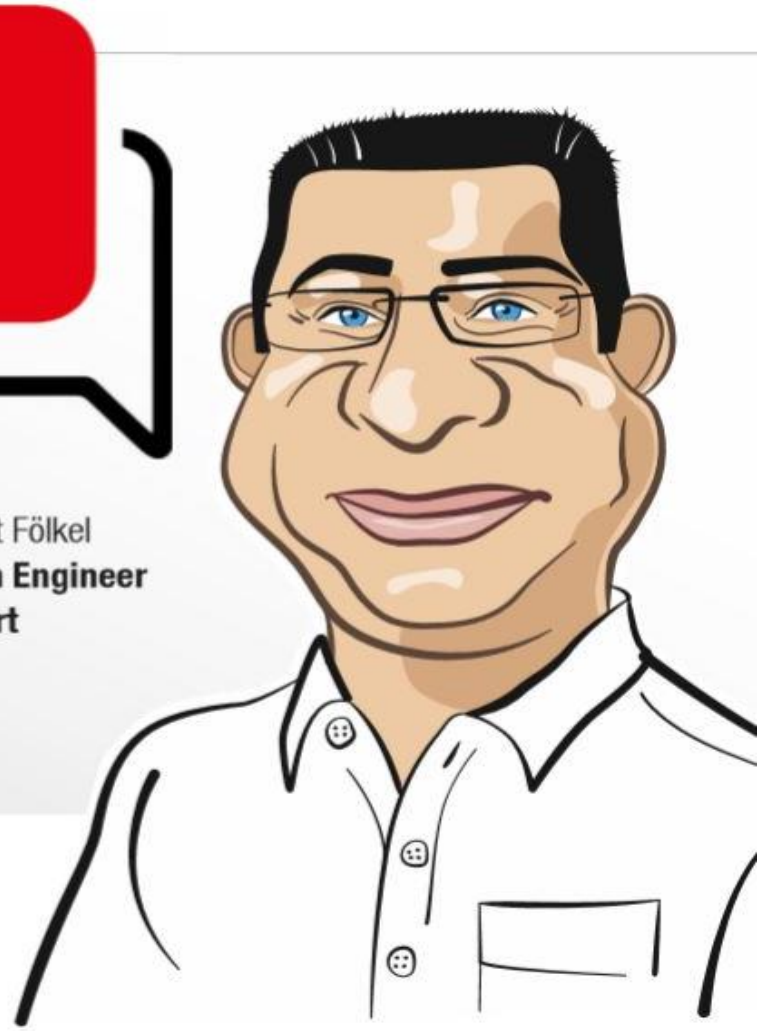
Follow me on …

Twitter.com/askLorandt

we-online.com/youtube

linkedin.com/in/lorandtfoelkel

We-online.com/askLorandt



or contact me directly:
askLorandt@we-online.com