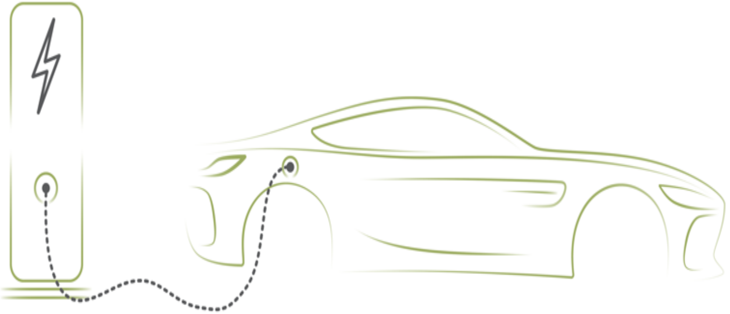
Designing efficient EV charging systems with C2000™ real-time MCUs



Agenda

- EV chargers overview
- DC/DC : Dual active bridge
- C2000 – PWM
- AC/DC: Vienna rectifier, ANPC - PFC
- C2000 Overview

EV charging

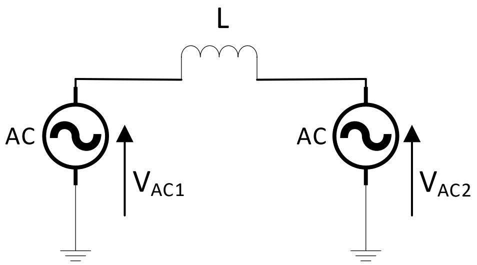
DC fast charger

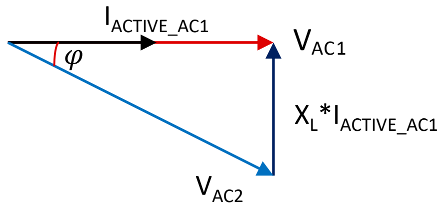
50-150kW+ charging station

- + Offers filling gas like experience for EVs
- + Modular architecture - made up of multiple racks of 25-50kW AC:DC & DC:DC power modules
- + Can support V2G

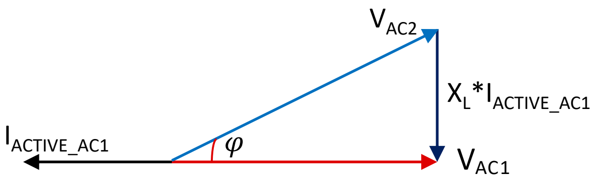
- - Cost
- - Needs infrastructure power line upgrade

V2G: Bidirectional power flow concept

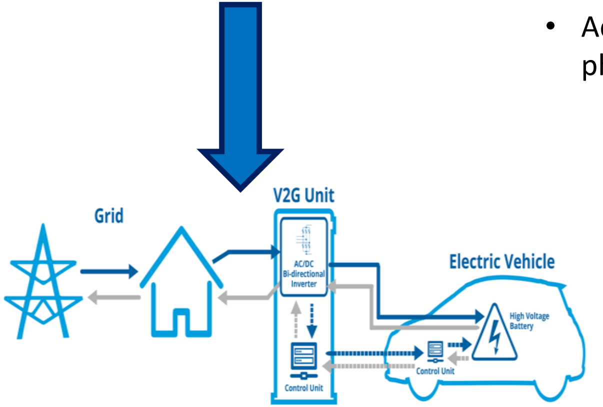


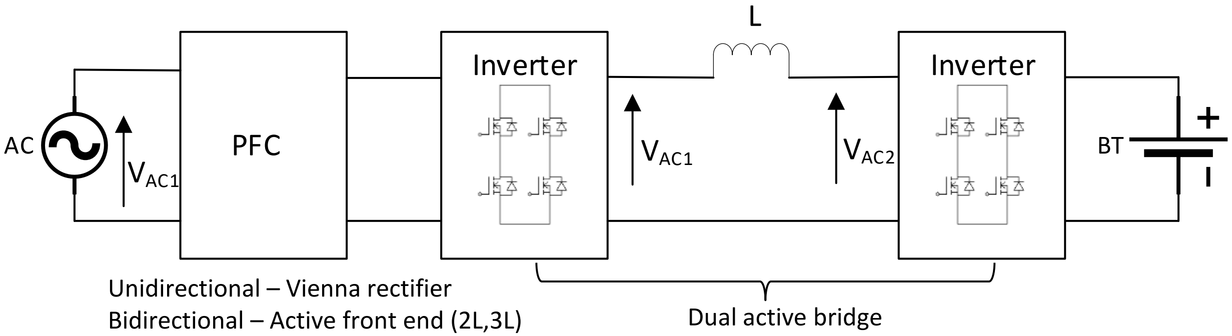


- Power flows from V_{AC1} to V_{AC2} at UPF
- Adding reactive current changes the phase angle



- Power flows from V_{AC2} to V_{AC1} at UPF
- Adding reactive current changes the phase angle





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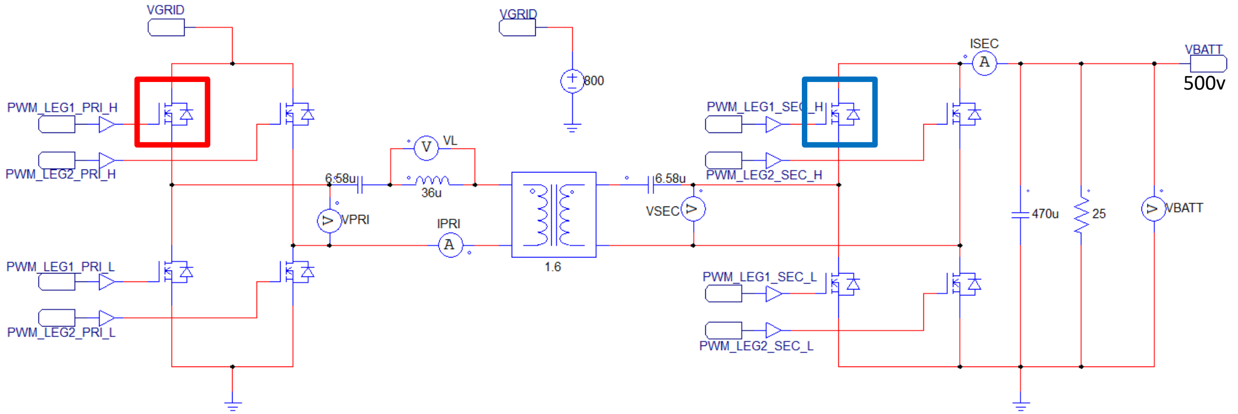
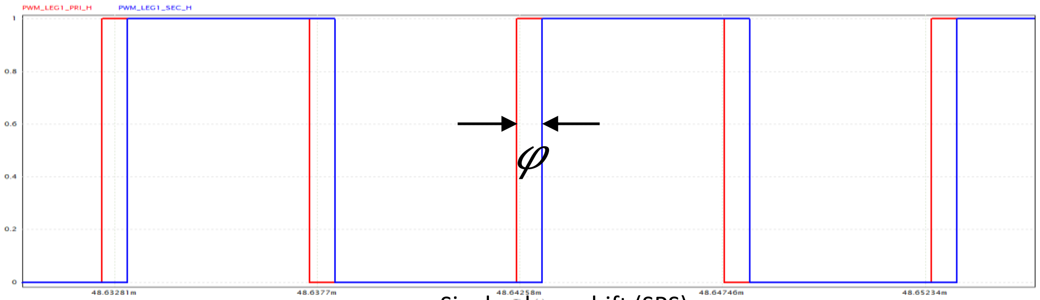
Single phase shift - Dual active bridge (DAB)



Primary bridge (reference)

Secondary bridge



Single phase shift (SPS)

$$P = \frac{V_{GRID} V_{BATT} n\varphi(\pi - |\varphi|)}{2\pi^2 F_{SW} L}$$

n = transformer turns ratio

φ = phase shift between the bridges

π, φ are in radians

$$P = \frac{V_{GRID} V_{BATT} nd(1-d)}{2FSWL}$$

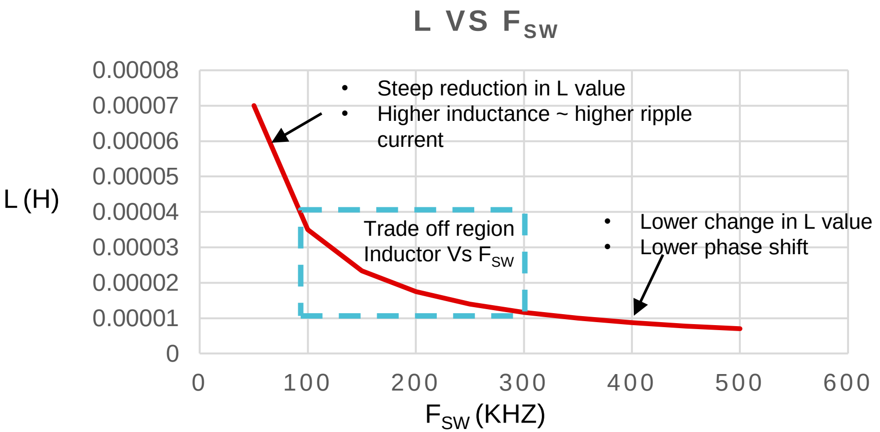
Where d = φ / π

DAB : Simplified design considerations

$$P = \frac{V_{GRID} V_{BATT}\, nd(1-d)}{2 F_{SW} L}$$

$Where\ d = \varphi / \pi$

unknowns



Inductor

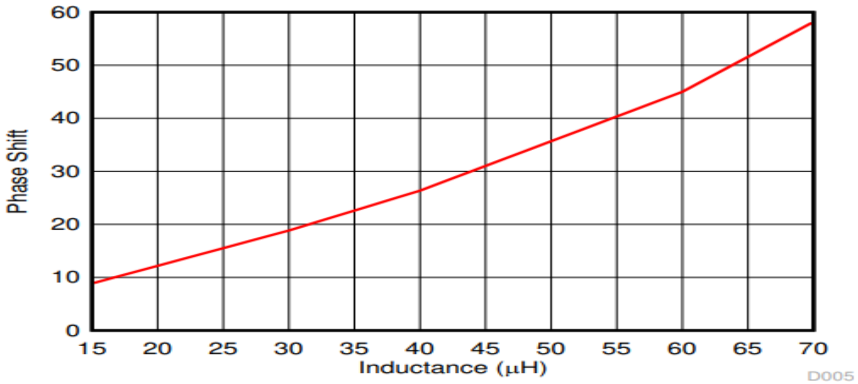
$$L = \frac{V_{GRID} V_{BATT}\, nd(1-d)}{2FSWP} \sim 35\mu H$$

DC Blocking Capacitor

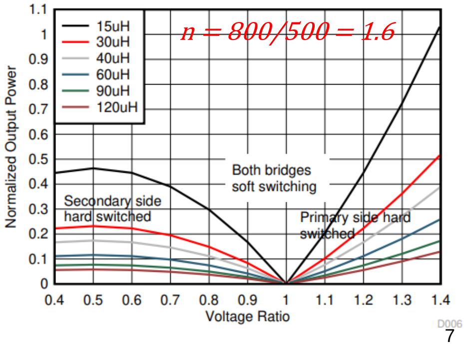
$$C_{DC\_Block} \sim \frac{100}{4\pi^2 F_{SW}^{\;2} L} \sim 7.2\mu F$$

Assumption

φ will be restricted to ~25deg to minimize ripple current



ZVS Vs voltage gain



Reference design : Bi-directional, dual active bridge reference design for level 3 electric vehicle charging stations TIDA-010054

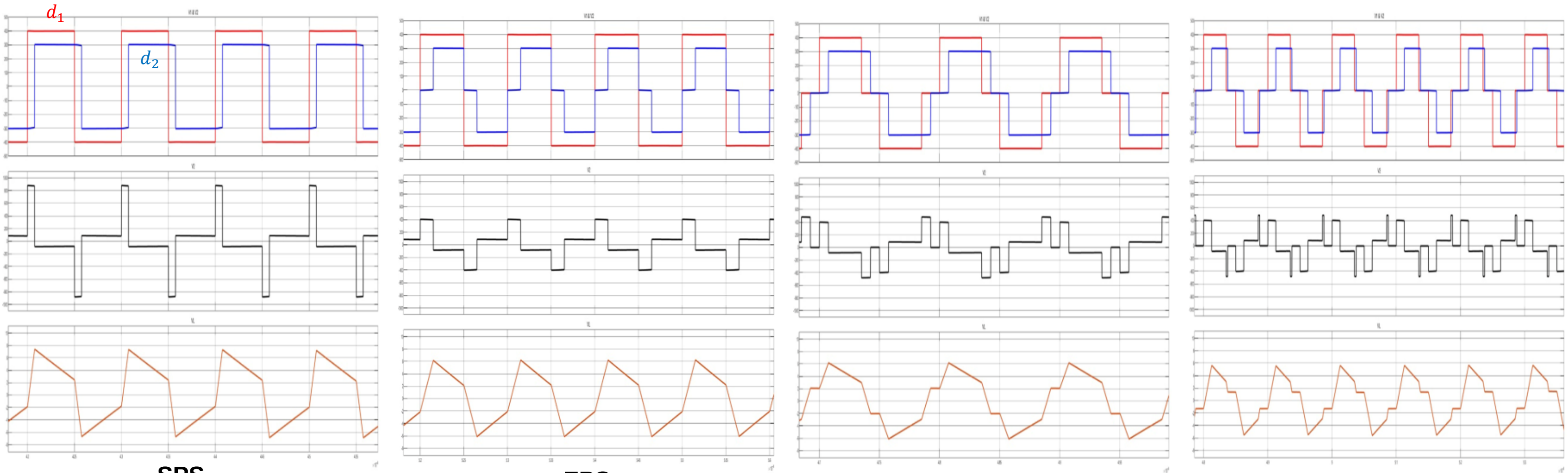
Multi-phase shift DAB

- *DAB when operated away from unity voltage ratio and rated power, the SPS control technique leads to low efficiency, high RMS and peak currents.*
- *Dual phase shift and triple phase shift controls make DAB more efficient*

Primary and secondary inverter voltages

Inductor voltage

Inductor Current



SPS

$d_1 = 1; d_2 = 1; 0 < \varphi \leq 1$
φ is variable
d_1 and d_2 are fixed

EPS

$d_1 = 1; d_2 < 1; 0 < \varphi \leq 1$
φ and d_2 are variable
d_1 is fixed

DPS

$d_1 = d_2 < 1; 0 < \varphi \leq 1$
φ is variable
d_1 and d_2 vary equally

TPS

$d_1 < 1; d_2 < 1; 0 < \varphi \leq 1$
φ is variable
d_1 and d_2 vary independently

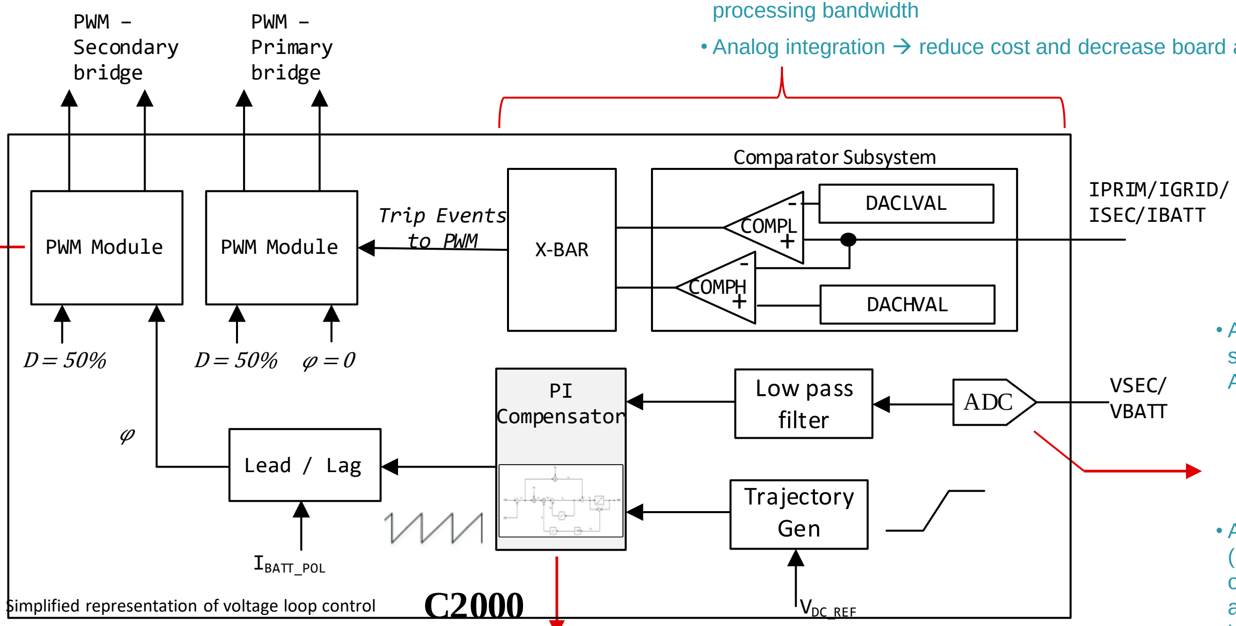
HR-phase shift and synchronization

- *φ -> 0 to ~25deg controlling 10KW Output power*
- *0 to ~25deg at 100KHz corresponds to ~690nsec*
- *PWM module operating at 100MHz can have a resolution of 10ns*
- *Minimum adjustable output power = 10KW * 10/690 ~ 145W*
- *Its not uncommon to have single DAB power module rated for 50KW*
- *C2000 real-time MCU*
    - *With high resolution phase shift of 150ps enables finer control*
    - *Up to 16 high resolution PWM channels*
    - *Synchronization of multiple ePWM modules controlling intra and inter bridge phase shifts*

Controlling DAB with C2000

- Built-in analog comparators against a 12bit DAC with 50ns pin-to-pin response time → enable real-time system protection against over-current & over-voltage events
- Trip any or all PWMs asynchronously to the system clock and independently from processing bandwidth
- Analog integration → reduce cost and decrease board area

- Synchronized PWM modules
- High resolution phase shift
- Flexible high resolution dead time adjustment (Coss Vs antiparallel diode loss)
- One-Shot and Global Load of Registers



- Accurate current and voltage sensing with fast and precise ADCs
  - Separate 3.45MSPS ADCs, each supporting INL of ±2 LSBs & 11bits of ENOB
- ADC Post Processing Block (PPB) helps remove DC-offsets from sensed voltage and current signals in hardware → significant cycle savings

- Optimized C28x core, CLA and TMU enable fast execution of the control loop for advanced multiphase DAB
- FPU unit built in → no more coding concern of scaling, overflow/underflow
- C2000 MCU with TMU can execute trigonometric & division operations, such as a “sine” instruction in 4 pipelined cycles. This compares with up to 41 cycles on an MCU without TMU → ~10x performance improvement
- PLLs or software algorithms that use transforms benefit greatly from the TMU

CLA – Control law accelerator
TMU – Trigonometric math unit

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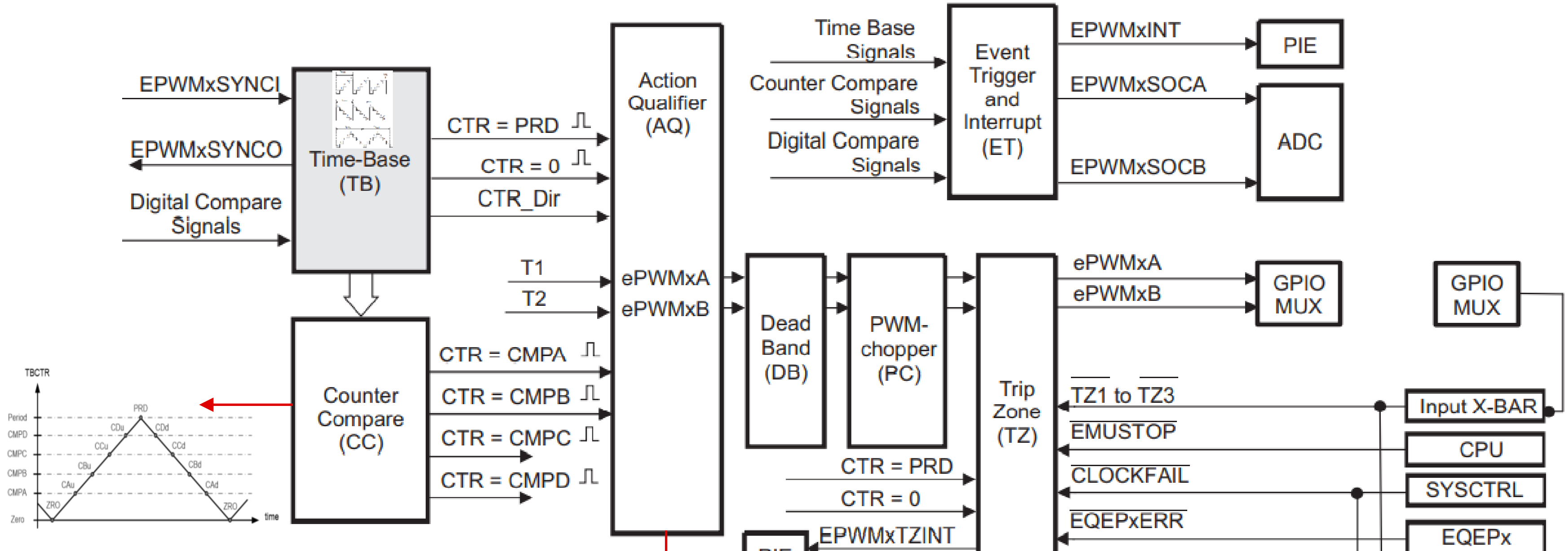
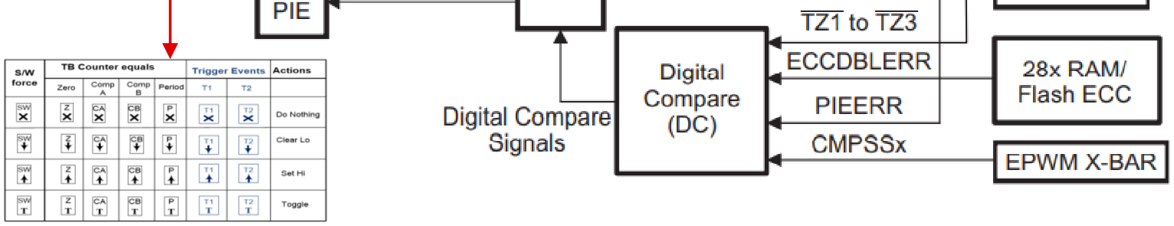
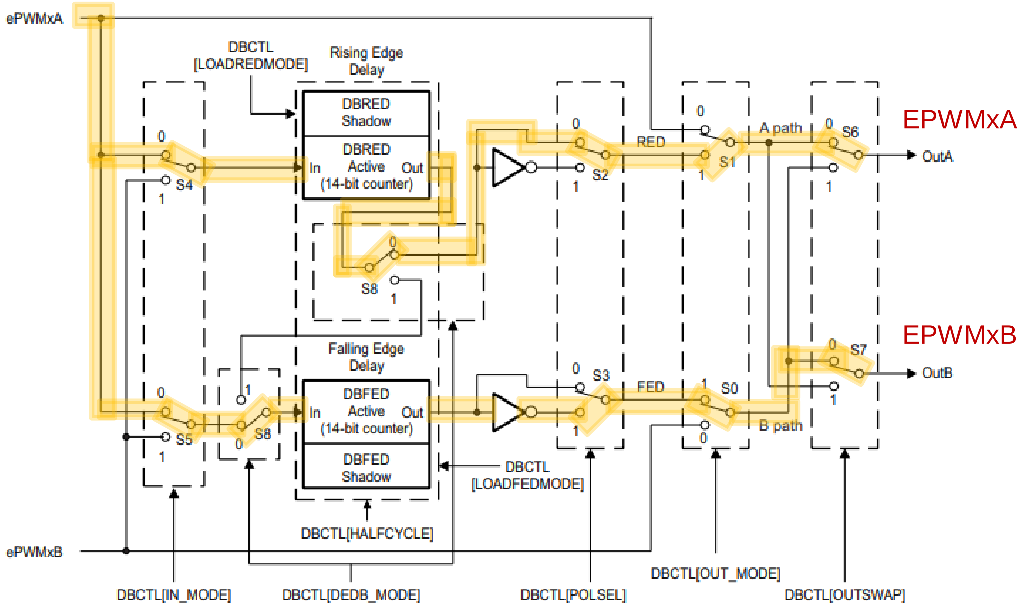
C2000 Type-4 PWM module

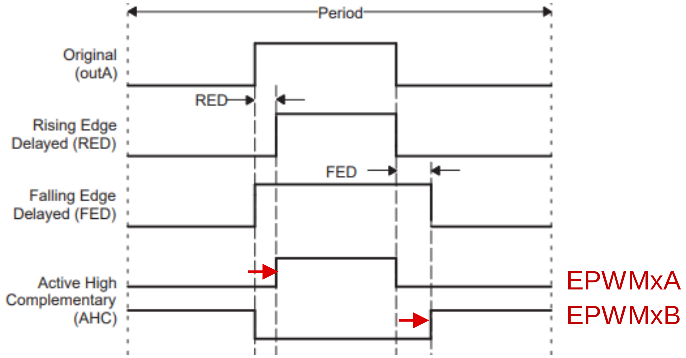




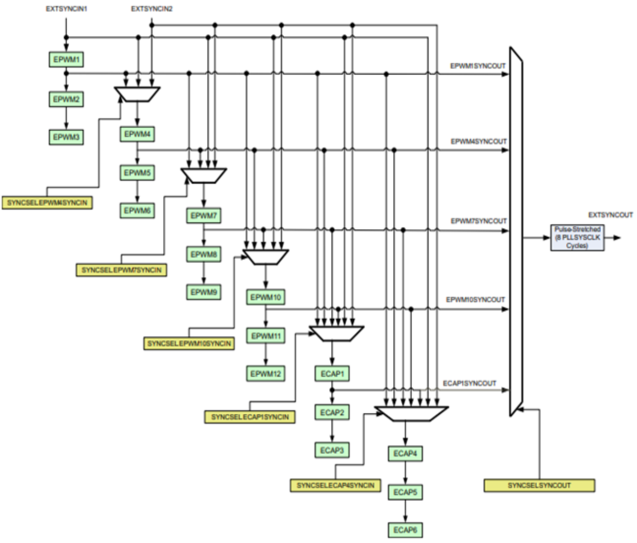
- Events can be specified on any time-base counter threshold crossing.
- Compares C & D can be used to generate SOC events and interrupts.
- Compares A & B can also be used to switch PWM waveform edges.

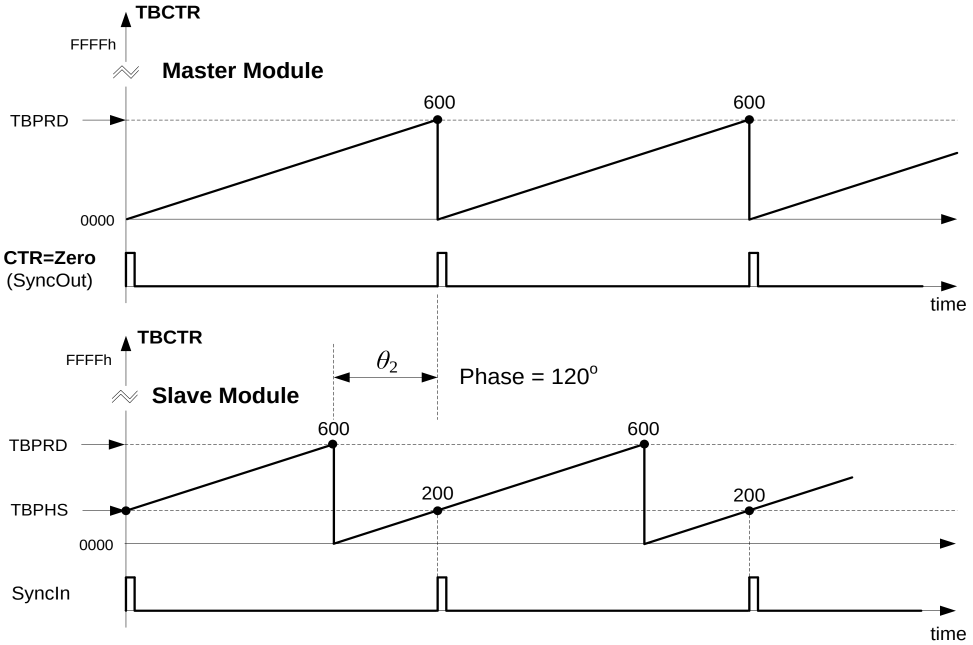
C2000 dead-band submodule





ePWM phase shift and synchronization





- Phase is controlled between PWM modules by synchronizing time-base counters.
- In this example, PWM1 generates a SyncOut pulse on a CNT = Zero event. PWM2 receives the pulse at its SyncIn terminal and loads a phase offset of 200 into its TBCTR.

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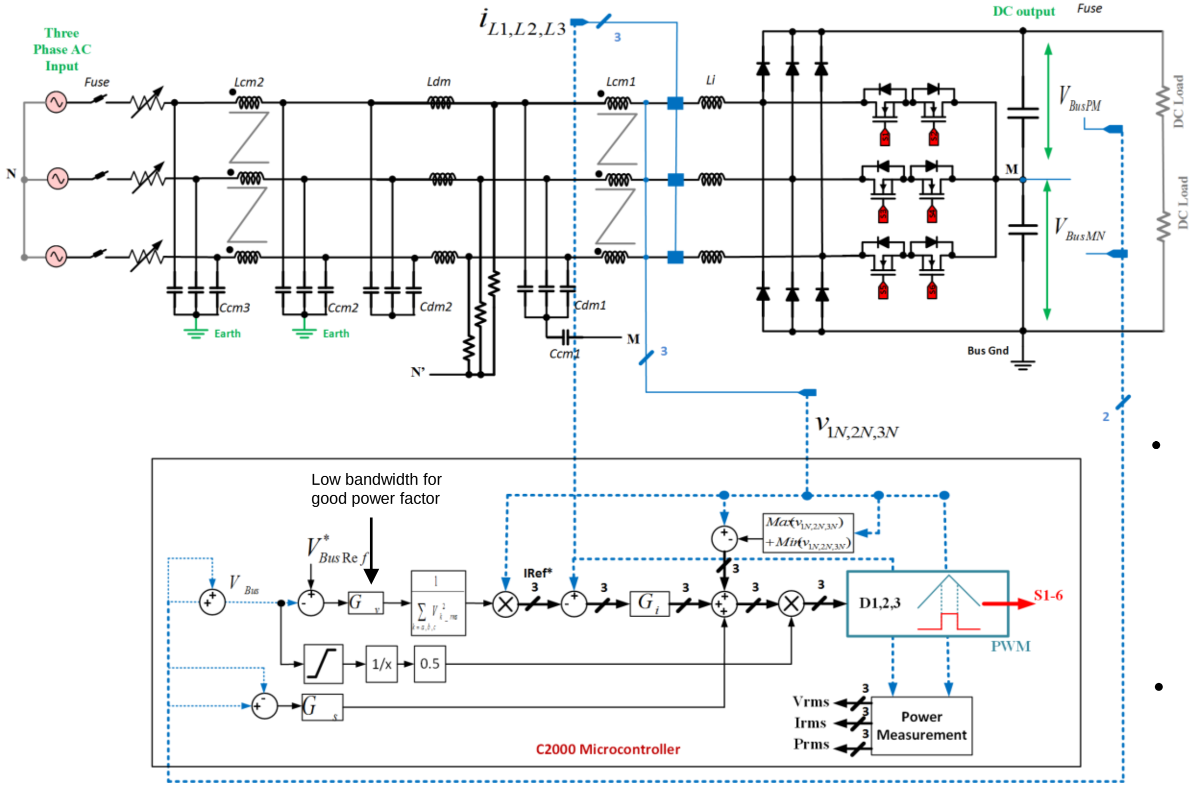
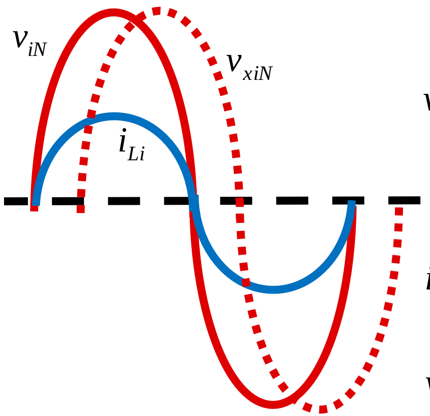
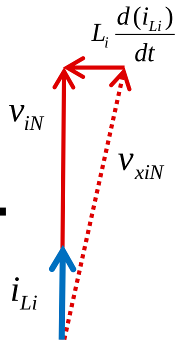
Vienna rectifier



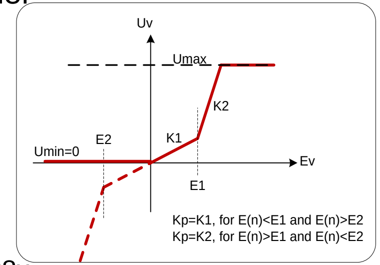




$$v_{xiN} = D * {V_{bus}}/{2}$$

- Improved dynamic response using non-linear voltage controller

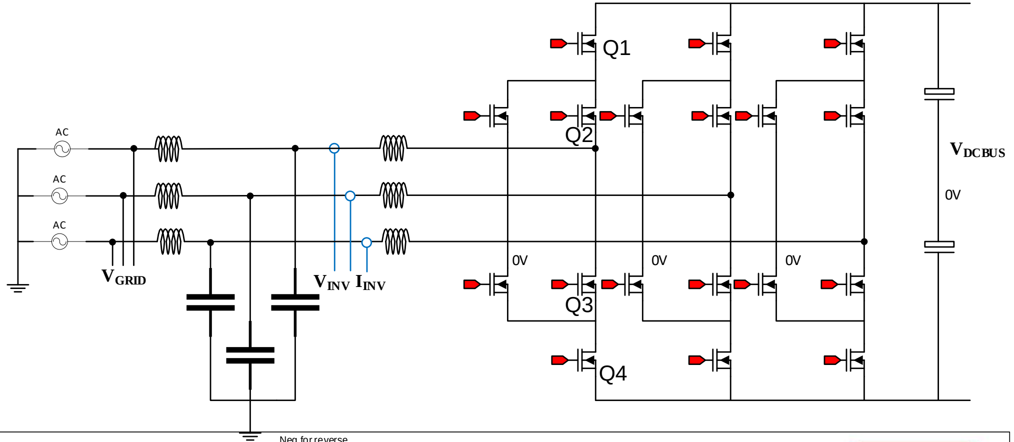
$$G_v(z) = \frac{U_v}{E_v} = K_p + \frac{K_I}{1 - z^{-1}}$$

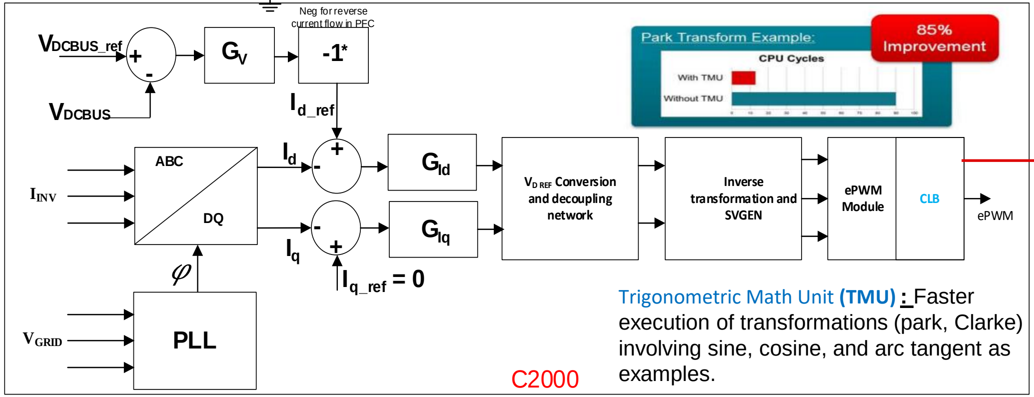


- Use of CLA reduces computation time
  - 2p2z -> 1.23X vs C28x
  - 3p3z -> 1.31X vs C28X

Reference design : Vienna Rectifier-Based, Three-Phase Power Factor Correction (PFC) TIDM-1000

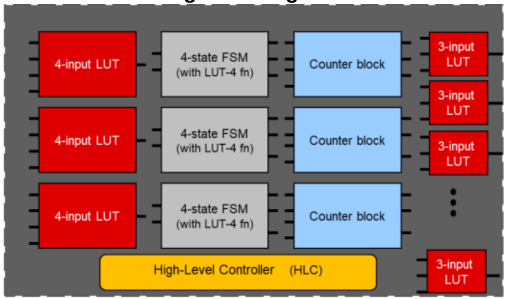
ANPC – Inverter / PFC





- Outer switches (Q1/Q4) need to turn OFF before turning OFF the inner switches (Q2/Q3)
- **Positive cycle**
  - ✓ Q2 should never be turned off if Q1 is still ON
  - ✓ Q1 should be turned OFF first and then Q2 after a defined delay
- **Negative cycle**
  - ✓ Q3 should never be turned off if Q4 is still ON
  - ✓ Q4 should be turned OFF first and then Q3 after a defined delay
- Shutdown sequence need to be followed under trip conditions
- Software algorithm causes too much delay to provide in-time protection
- Use of external hardware circuits, like FPGA or CPLD increases system cost and development cost
- Built-in Configurable logic block within C2000 lowers system cost by enabling shutdown sequence

Configurable logic block



Reference design : 11-kW, bidirectional, three-phase ANPC based on GaN reference design TIDA-010210

Agenda

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- DC/DC: Dual active bridge
- C2000 – PWM and ADC
- AC/DC: Vienna rectifier, T Type PFC
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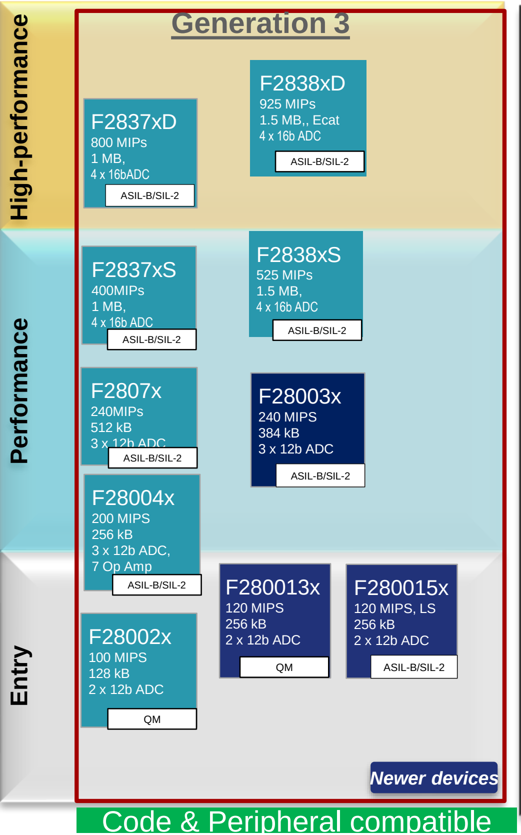
C2000™ product portfolio



C2000 portfolio offering

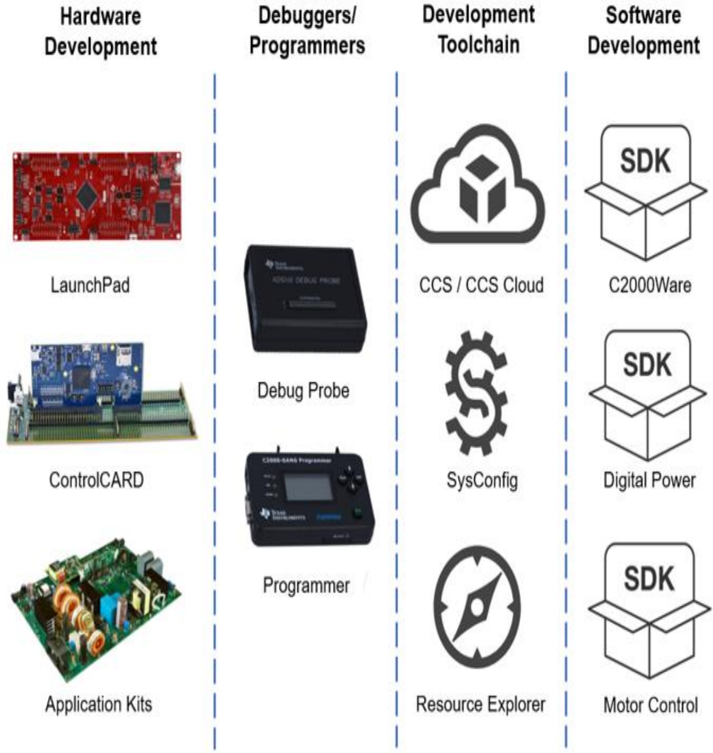
Broadest Portfolio of Real Time MCUs

- Software Compatible Portfolio
- 60 MIPS to 925 MIPS
- 32kB to 1.5MB Flash
- 6-32 PWM ch (16 High-Res)
- Up to 40 ADC ch
- I2C, UART, SPI, CAN, CAN-FD, Ethernet, EtherCAT, USB
- Packages from 32 QFN (5x5mm), QFP, to 337 BGA
- Safety Support, Industrial and Automotive

Real-time Control Systems Made Easy

- Over 25 Years of Expertise in Real-Time Control Systems
- Extensive Library of Public Reference Designs
- Software and Hardware Tools to Jump-Start your Design and Shorten the Time Between Evaluation and Production

C2000 ecosystem snapshot



C2000™ F28003x

http://www.ti.com/product/TMS320F280039C

Differentiation

Building on F28002x for High-Performance Power Control Applications

Improved performance

- 120 MHz with CLA option
- 240 MIPS DSP Processing Power
- More Flash and RAM
- Better ADC Performance - Effective throughput

Advanced actuation and design flexibility

- Premium Type 4 ePWM modules with more instances and channels

Premium analog

- 8 Sigma Delta Decimation Filters (with separate Data and Comparator filters)
- 2 * Buffered DAC 12-bit , +1 * 12 bit ADC @ 3.45MSPS

Rich digital options

- CAN-FD, +2 * CLB tiles, +1 * SCI

Safety

- ASIL-B/ SIL-2 safety enablers

Security

- AES, JTAG Lock & Secure boot

Perfect portfolio

- Pin-pin to F28002x 64-pin (non-Q) and 80-pin(non-Q) and almost compatible to 48-pin and 64-pin (Q)
- 100-pin option

F28003x/ F28003x-Q1

Temperatures	125C	Q100

Sensing
- ADC1: 12-bit, 4 MSPS,
- ADC2: 12-bit, 4 MSPS
- ADC3: 12-bit, 4 MSPS
- 4x CMPSS : 12-bit DAC, 8 COMP, 8 digital filters
- 8x Sigma Delta Channels (2x Filters per ch)
- Temperature Sensor
- 2x eQEP
- 3x eCAP , 1x HRCAP

Configurable Logic Block
- 4 Tiles

System Modules
- 3x 32-bit CPU Timers
- NMI Watchdog Timer
- 192 Interrupt PIE

Processing
- C28x™ DSP core, 120 MHz
- FPU, FastDIV, VCRC
- TMU +NLPID
- CLA core, 120 MHz, FPU
- 6ch DMA
- BGCRC & HWBIST

Memory
- 384 kB FLASH (3 bank) +ECC
- 69 kB SRAM +ECC
- ROM with parity
- Dual Security Zones, Secure boot and JTAG lock
- AES
- Host Interface Controller (HIC)

Actuation
- 8x ePWM Modules, 16x Outputs (8x High-Res)
- Fault Trip Zones
- 2 * 12-bit Buffered DAC

Connectivity
- 2x SCI, 2x LIN/SCI
- 2x I2C, 1x PMBus
- 2x SPI, 1x FSI-TX , 1x FSI-RX
- 1x CAN-FD, 1 CAN 2.0B

Power & Clocking
- 2x 10 MHz OSC
- 1.2V VREG
- POR/BOR Protection

Debug
- cJTAG / Real-time JTAG
- ERAD

For device spins

Tools

Experimenter's Kit

Part Number: TMDSCNCD280039C
https://www.ti.com/tool/TMDSCNCD280039C

LaunchPad

Part Number: LAUNCHXL-F280039C, 2Q22

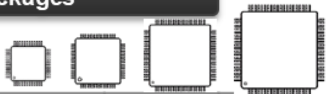
Software

C2000Ware™ Software Package

Application SDKs

Functional Safety Compliant Product	
Target Systematic Capability	ASIL-D/SIL-3
Target Diagnostic Coverage (DC)	ASIL-B/SIL-2

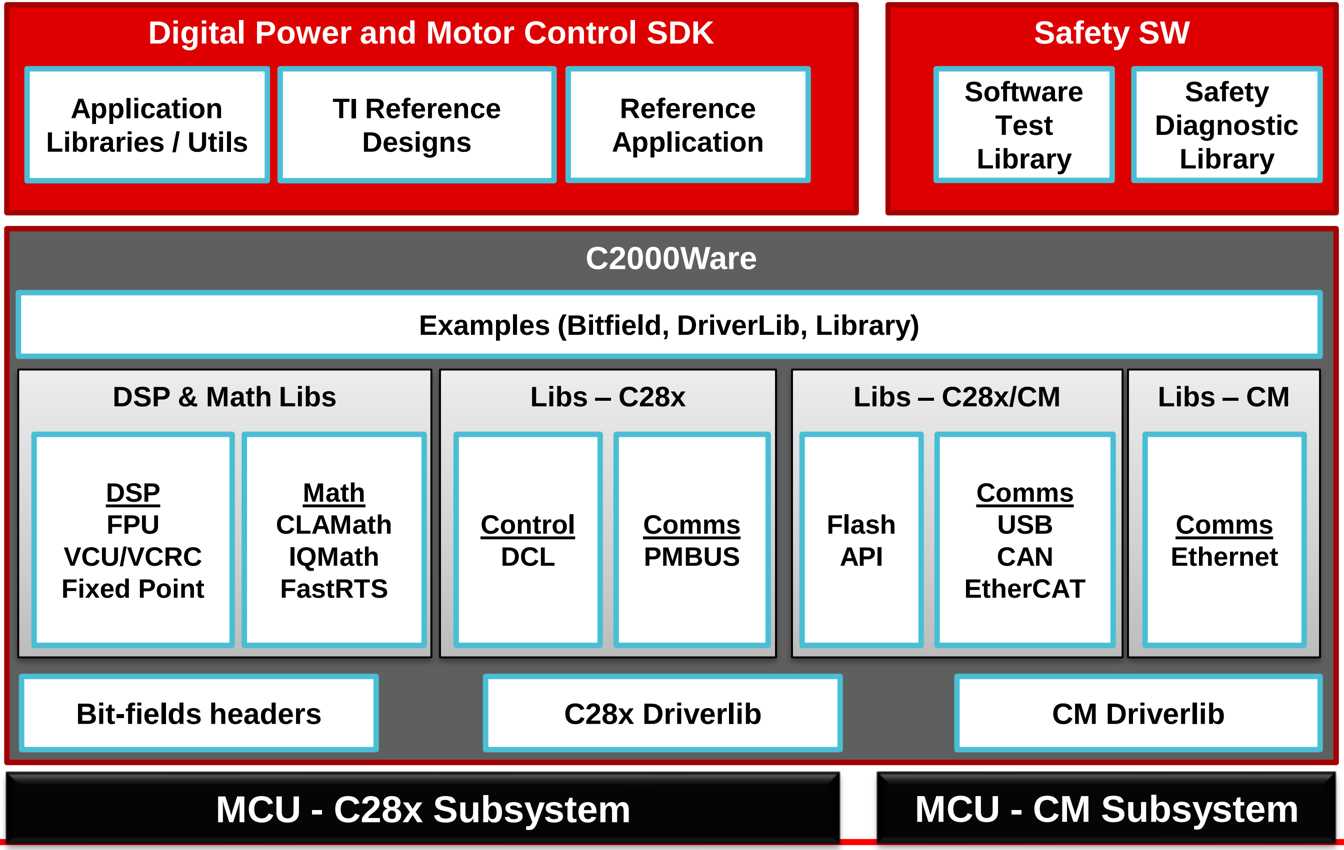
Packages



Package	Footprint Dimensions	Temp
48-pin LQFP	9 x 9 mm	S, Q
64-pin LQFP	12 x 12 mm	S, Q
80-pin LQFP	14 x 14 mm	S
100-pin LQFP	16 x 16 mm	S, Q

Texas Instruments

Software interfacing levels



Application-specific SDKs

- Reference SW to get started for Digital Power and Motor Control
- Libraries and utilities to get started

Safety software (SW)

- Reference SW to implement Safety manual mechanisms
- Production ready STL for C28x and CLA diagnostic coverage

C2000Ware examples

- Examples for peripheral access using driver-lib or bit-field
- Examples for compute and communication libraries

C2000Ware libraries

- Compute and Communication libraries for standard functions

C2000Ware driver lib / bit-field

- Functional APIs for using a peripheral or accessing hardware registers

C2000 Academy: overview

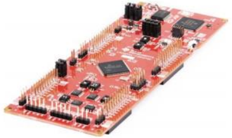
Current device workshops

Specialized training for
a specific device

TMS320F2837xD Microcontroller Workshop

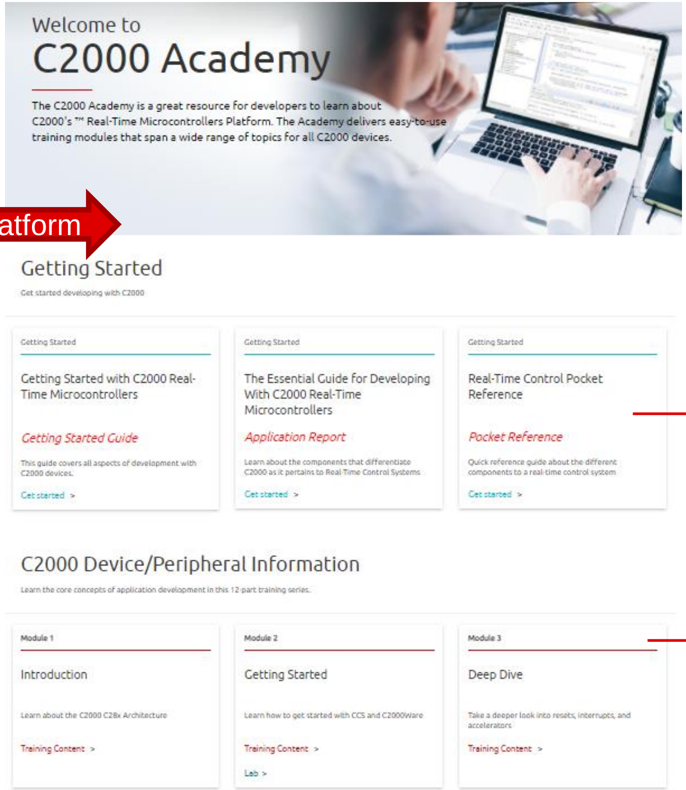
Texas Instruments C2000 Technical Training

TMS320F28004x Microcontroller Workshop



Texas Instruments C2000 Technical Training

New Platform



How is this different?
C2000 Academy contains training content and labs for all Gen 3 devices with a more interactive and foundational approach

Getting started
A section which links to key C2000 collateral

C2000 device/peripheral Info. Bundles training content and labs into "modules" that cover specific areas (ex. Analog, Control, SYSCONFIG)

Dev.ti.com-> Resource Explorer -> Software -> C2000 Academy

EMC FILTERING ON EV CHARGING STATION

Angelo Strati
Italian Technical Team
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☏ 334-6054571

WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

The Würth Elektronik Group

Würth Elektronik eiSos
Electronic & Electromechanical Components

Würth Elektronik CBT
Printed Circuit Boards

Würth Elektronik ICS
Intelligent Power- and
Control Systems

Free Technical Support

- Possibility to agree on the presence of a FAE during the EMC tests in the laboratory

- Realization of free in-House seminars at your headquarters or in video-conference on different topics (EMC, ESD, DC / DC filtering, selection of inductors ...)

- Support in the selection of components for your application

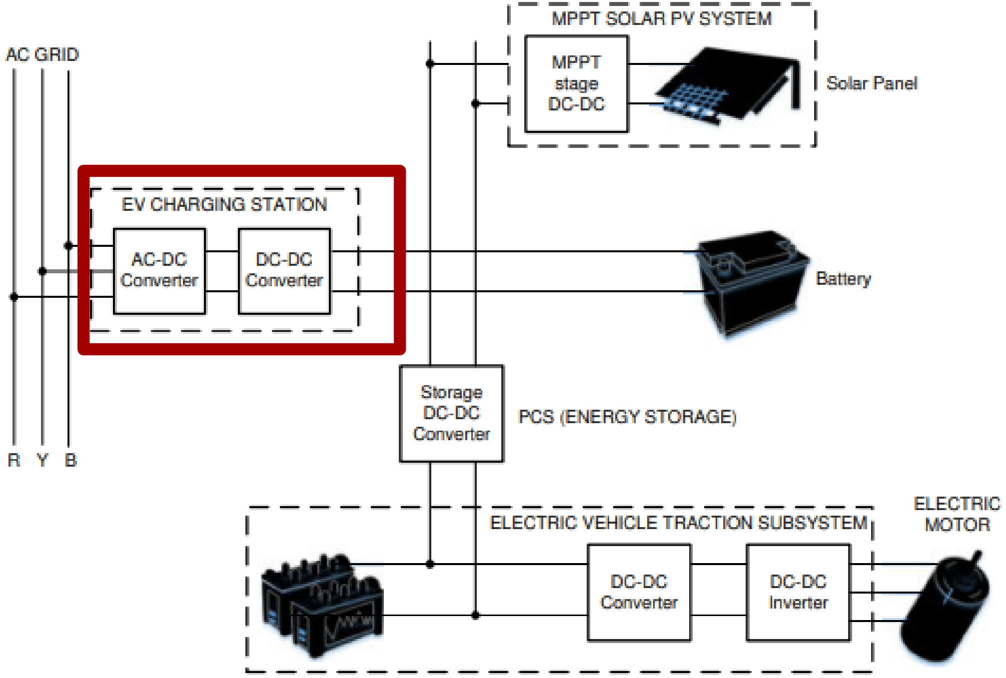
- Sending of free samples for the prototyping phase and / or the EMC test phase

- Possibility to request on-site presence for project support

Agenda

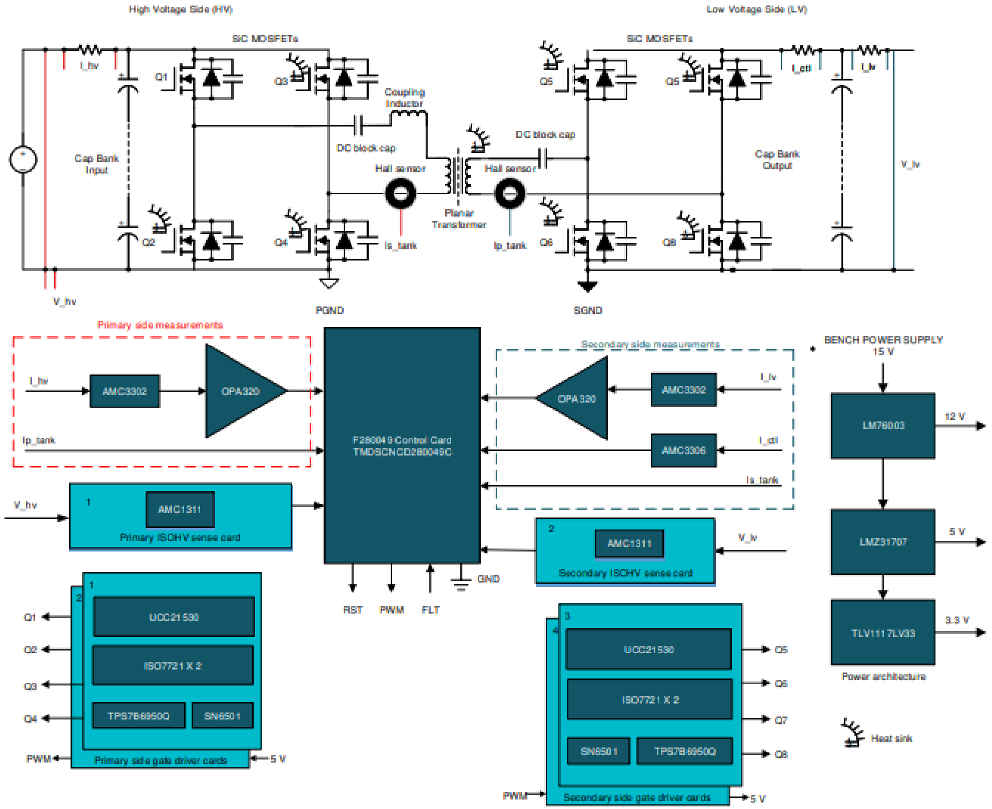
- EV Charging Station with C2000
- Sources Of Interference
- Filtering Components

EV Charging Station Scheme



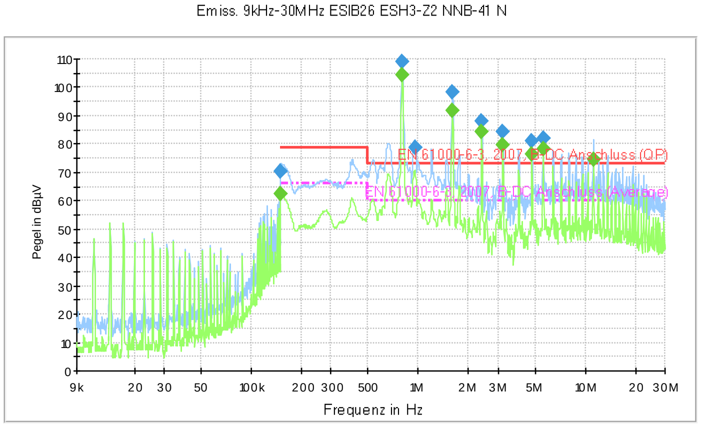
Sources Of Interference

- PWM Drive
- Control Logic and Oscillator
- Interfaces
- Switching Regulator
- Layout
- Wiring



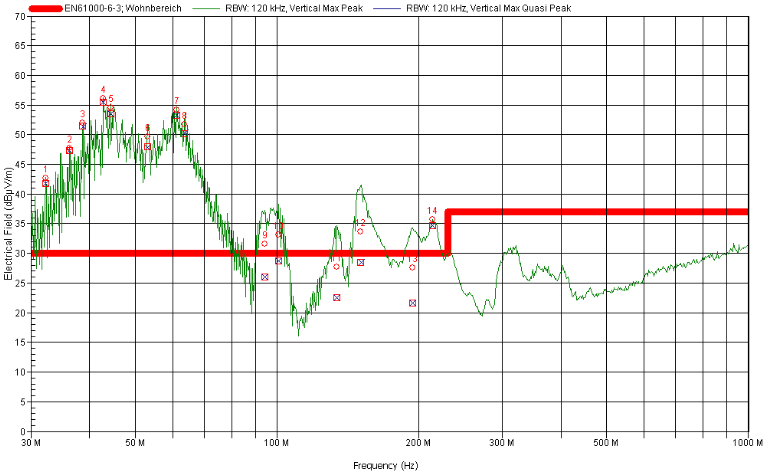
Wired Interference – Conducted Emission

- Cause of the interference voltage of 150kHz ... 30MHz:
  - Ripple current on the supply side
  - Rise/fall time controlled by gate drive
  - Interference current via parasitic coupling capacitances to ground (common mode)
- The unbalanced voltage sampled per phase contains symmetrical and asymmetrical components. .
- Limit value for the asymmetrical interference voltage, e.g. according to EN 61000-6-3



Noise Emission – Radiated Emission

- Cause for the interference field strength of 30MHz ... 1 (6) GHz:
  - Noise current on conductor tracks or loops
  - Noise current on conductive housings
  - Interference current on lines connected to interfaces
- Limit value for the radio interference field strength e.g. according to EN 61000-6-3

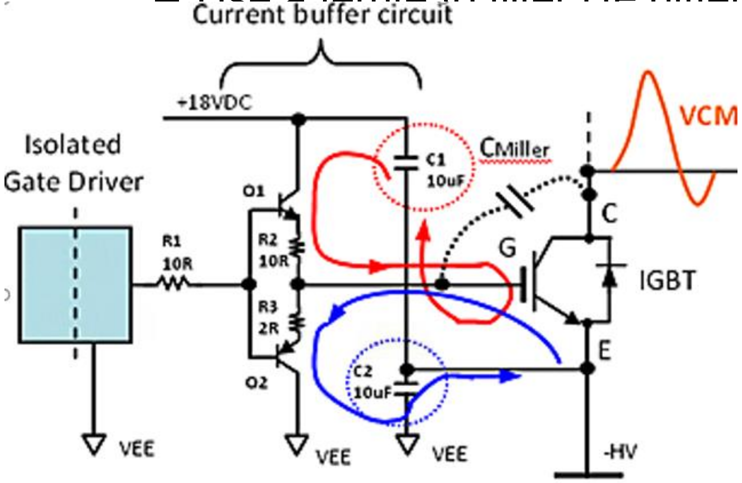


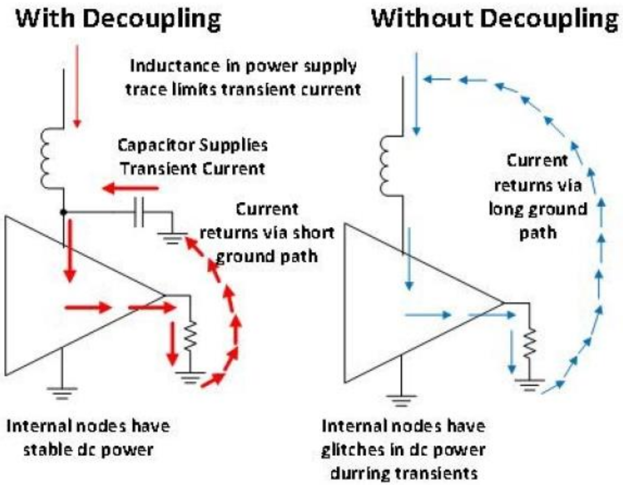
Overwiev Sources Of Interference

Type of Fault	Dominant Source	Frequency Range	Radiated or Conducted
Low Frequency Range	Fundamental and harmonics of the controller switching frequency	10kHz to 30MHz	Conducted
Broadband Interference	dI / dt and dU / dt of the FET (silicon) switching edges and parasitic resonant circuits	30MHz to 200MHz	Conducted and Radiated
High Frequency interference	Reverse Recovery of Schottky Diodes	Over 200MHz	Radiated

Differential Mode Interference: Filtering

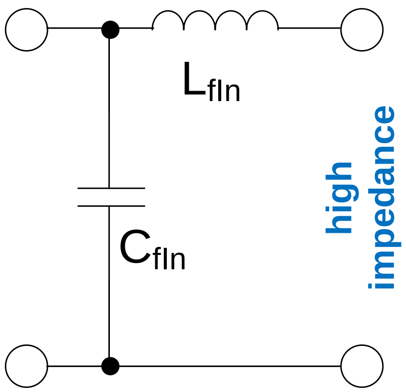
- Minimizing the differential mode interferers by:
  - Placing a RF decoupling "C" close to the switching node
  - Keep high ΔI / Δt loops (loop antennas) compact → Minimization of H-fields
  - Use a ferrite to filter HF differential noise generated by Oscillator

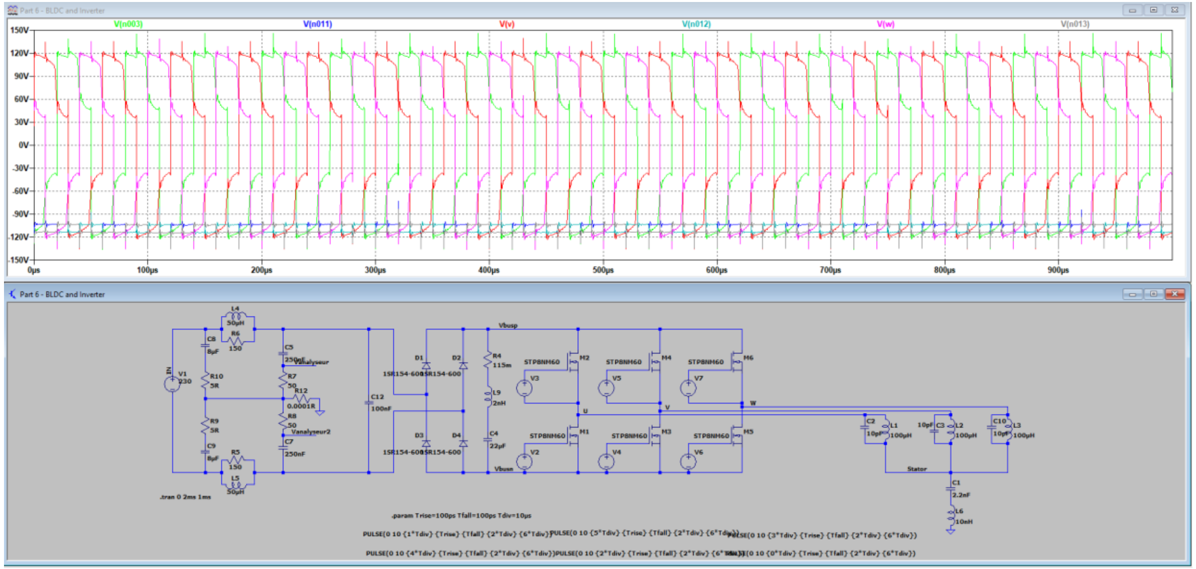




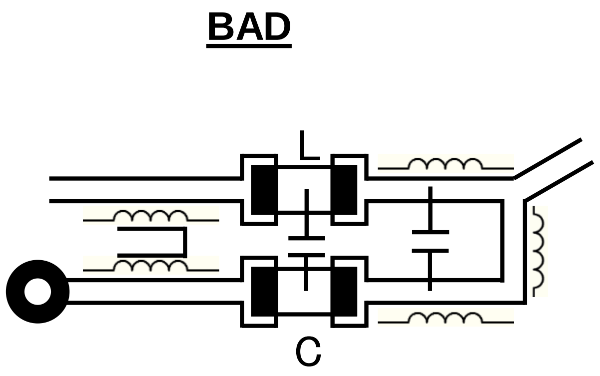
Differential Mode Interference: Filtering

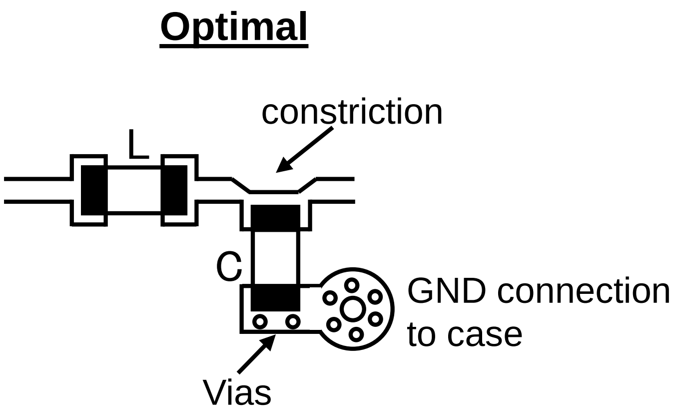
- DM Filtering:
  - Input LC Filter to attenuate PWM signals (High repetitive pulse)
  - Rise/Time controlled by Gate Drive
  - Place the correct way: input impedance of the transducer is very low, normally mainly dominated by the one or two capacitors





Layout Suggestions On Drive Board: GND Reference For Filter

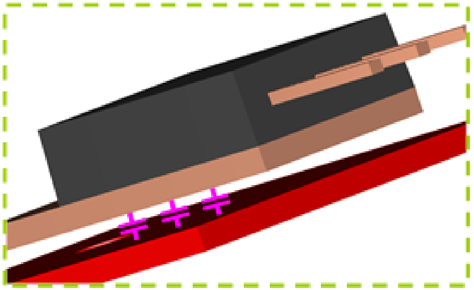


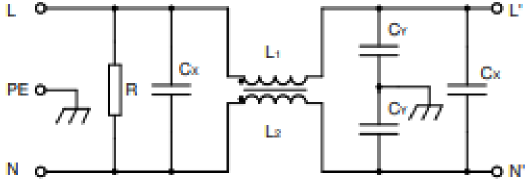


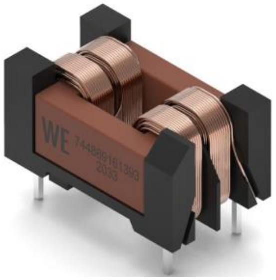
- Constriction reduces reflections (VSWR) in gigahertz range
- Right angle arrangement reduces capacitive coupling
- Vias and direct conductive board mounting enable low-impedance ground connection

Common Mode Interference: Common Mode Choke

- Large common mode current paths due to the heat sink formation of HF capacitance
- These leads to problems with the Conducted & Radiated Measurement!
- Use Common Mode Choke and X or Y caps





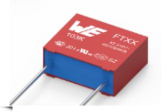


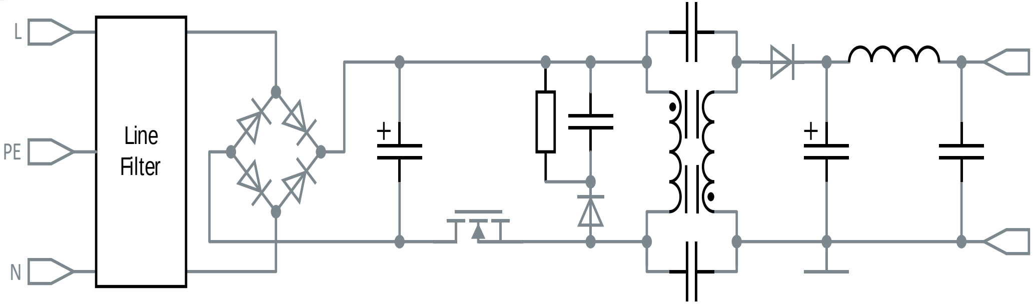
FET : fsw to 20MHz

Aux ACDC converter, what can we provide?

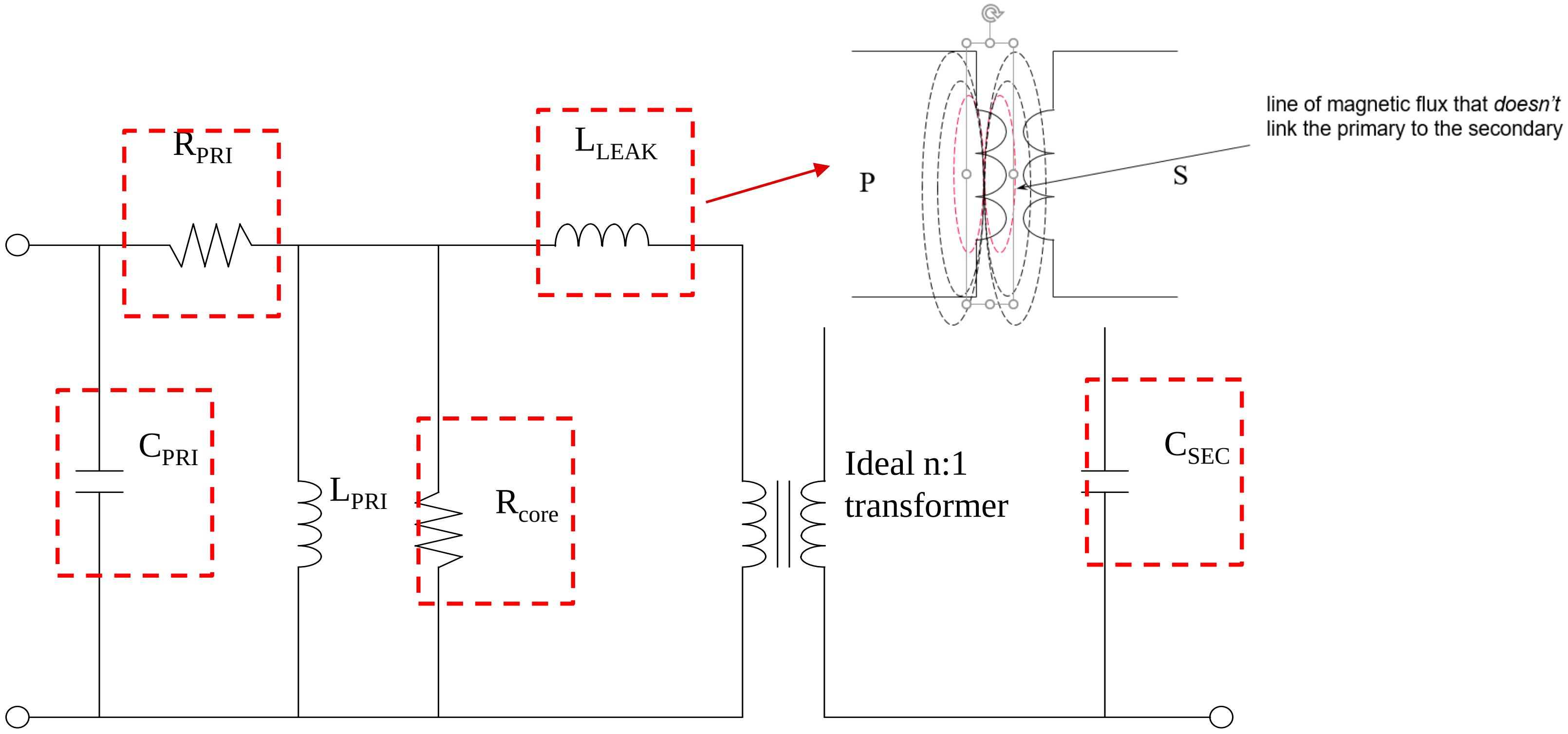
Converts the AC input to power up all the DC logic inside

- WE-TFC/WE-FC/WE-FCLP
- WCAP-FTXX
- WCAP-CSSA
- WE-VD
- Transformer
- WE-ATG8/ATG5
- WE-PSLC
- WE-PD2/PD-HV/TI-HV

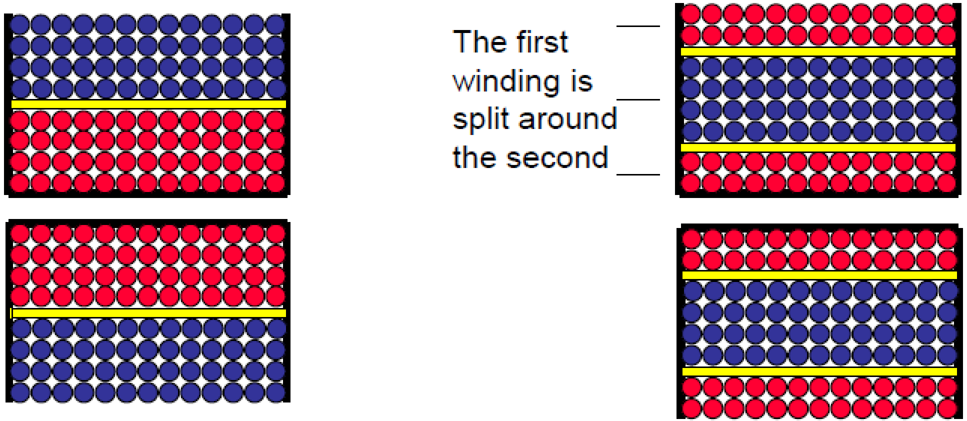




Parasitics – Transformer Standard Model

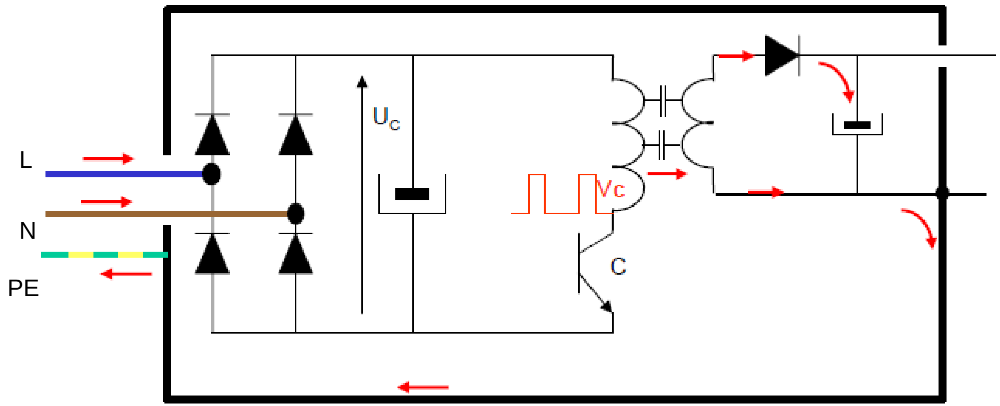


Leakage Inductance – Good Construction



To improve the coupling between the windings we can sandwich the first winding around the second. This reduces the average distance between the windings and results in 1/4th the original value of leakage inductance – at the expense of more winding labor.

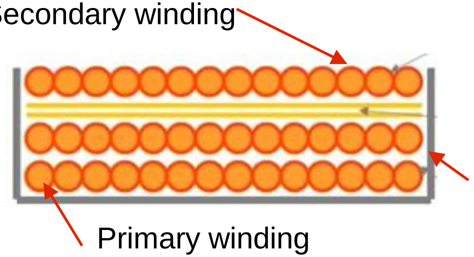
Transformer for EMC : C_{ww}



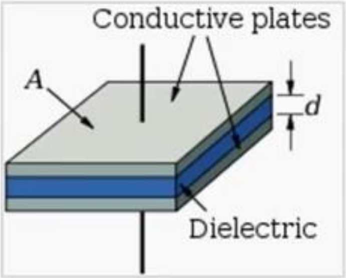
- **Noise couples through the transformer via C_{ww}**
  - Noise seeks path to primary circuit
  - Without path, noise may become conducted emissions

Reducing InterWinding Capacitance

- **How can we reduce the inter-winding capacitance**



$$C = \varepsilon_r \varepsilon_0 \frac{A}{d}$$



- Multi-section or Narrow bobbin
- Lots of tapes and increase the insulation thickness on wire

➔ This will result in increasing the leakage inductance (we have to use Snubber to control it)

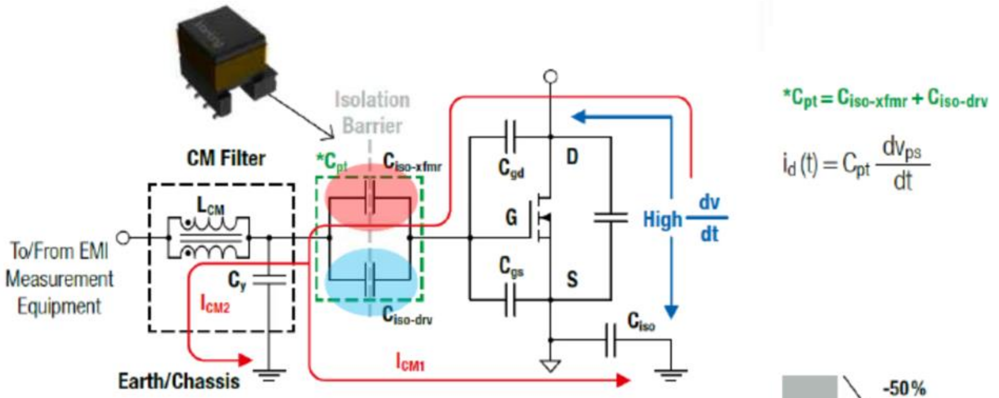
- Possibly reducing the electric constants using for example low dielectric varnishes or potting compounds on wires (Does not affect the leakage inductance)

Gate Drive Trasformer for SIC-MOSFET

Isolation Barrier Parasitic Capacitance: Common-mode Transient Immunity (CMTI) and EMI Performance

Common-mode Transient Immunity (CMTI) (measured in kV/us or V/ns), is an indication of the maximum dV/dt which can be tolerated across the isolation barrier before malfunction of the gate driver system occurs, due to excessive distortion of the gate drive control signals.

- SiC-MOSFETs switch extremely fast, helping to increase efficiency and reduce system size and cost.
- Fast switching speed causes high dV/dt to appear across the isolation barrier parasitic capacitance (Gate driver IC and auxiliary supply transformer).
- Common-mode displacement currents are generated.
- A lower parasitic capacitance reduces these displacement currents, helping to achieve a higher CMTI rating and better EMI performance.
- **It is critical to minimize the transformer interwinding capacitance in fast-switching SiC-MOSFET gate drive applications.**



Minimize displacement current / common mode current for

- Improved control robustness
- Better EMC performance

Compared to regular transformers

- 50 % less interwinding capacitance
- Higher Common Mode Transient Immunity (CMTI) over 100 kV/µs