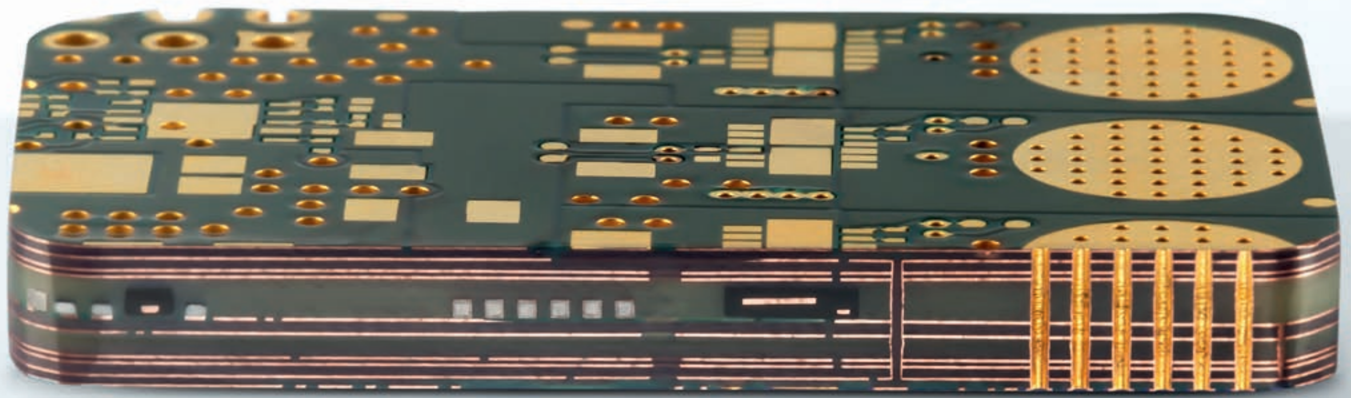


DEVICE.embedding
DESIGN GUIDE

EN

WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

EMBEDDING COMPONENTS IN THE PRINTED CIRCUIT BOARD

The future of electronics is tending towards higher reliability, more functionality and increasing miniaturisation. The efficient use of ever smaller housing volumes and tiny surfaces is gaining in importance. The embedding of components serves as a solution for reduces spaces.

In an embedding process, active or passive components are positioned in the stack up so that they are completely integrated into its construction. Würth Elektronik distinguishes between three manufacturing processes: SOLDER.**embedding,** MICROVIA.**embedding** and FLIP-CHIP.**embedding**.

The fields of application range from the automotive industry to industrial electronics to medical technology and to sensor technology.

Below is an overview on the subject of "Embedding Technology" and practical tips for design:

- Indicators for the choice of technology
- Technology comparison
- Availability of components
- Design Rules

THE ADVANTAGES OF EMBEDDING TECHNOLOGY AT A GLANCE:

MINIATURISATION

- Package replacement
- Space savings of assembly area on the outer layers

FUNCTION

- Integrated shielding
- Short signal paths
- Protection against plagiarism

RELIABILITY

- Protection against environmental influences
- Fully encapsulated and supported components
- Thermal management

INDICATORS FOR THE USE OF THE TECHNOLOGIES

SOLDER.**embedding**

- Active components that are not available as a bare die
- Active and passive components
- Range of the solid SMD components can be used (with restrictions)

MICROVIA.**embedding**

- Combination of active and passive components
- Highly reliable assembly and packaging technology
- Copper or nickel-palladium pad metallisation on the components

FLIP-CHIP.**embedding**

- Active components, which were previously wire-bonded
- No passive components possible
- Active components with pitch < 250 µm

Unless otherwise agreed, IPC-7092 applies to all products with embedded components.
The associated PCB production corresponds to IPC-A-600 Class II and the assembly to IPC-A-610 Class II.

Depending on the design and final build-up of the PCB with embedded components, the design rules/design guides currently valid at Würth Elektronik „Basic Design Guide", „Flex-Rigid Design Guide", „Heat Management Design Guide" and the „HDI Design Guide" apply. If you have different requirements, please contact us directly!

PROJECT PLANNING

IMPLEMENTATION PLANNING

The following data and information are required for implementation planning of projects with embedded components:

- Data sets (Extended Gerber, ODB++)
  - Copper layers
  - Paste data for inner and outer layers
  - Soldermask data for inner and outer layers
  - PCB outline
  - Maximum dimensions of the components (including outlines of the contacts protruding the body e.g. Gull-Wing- and J-Leads) as a projection from above onto the layer to be assembled.
- Stack-up
  - On the part of the customer with the desired layer connections, copper thicknesses and, if necessary, predefined layer distances (due to impedances or insulation distances).
  - Proposal from WE, if applicable
- Bill of materials (BOM) with all max. dimensions of the components (nominal plus max. tolerances) in X, Y and Z
  - Components (sourced by WE or provided by customer)
- Pick&Place data as .txt file (only of the components that will be embedded)
- Drawings, assembly plans (inner layers) and test instructions
- Information on layer distances regarding impedances or insulation distances

PROJECT FLOW

1. Customer
- New product
- Re-Design of an existing board

2. Development
- Presentation of the project or product idea
- Supported by tips and tricks from WE through design guides, possible layer structures and layout tips

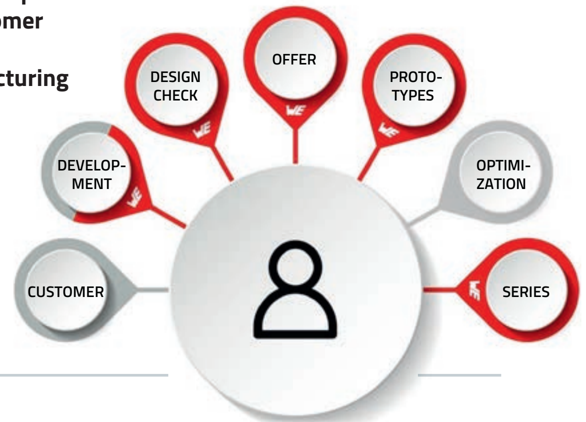
3. Checking of data and optimization proposals
- Stack-Up
- Design Rule Check
- BOM and component availability check

4. Quotation
- Prototypes
- Series

5. Prototype manufacturing

6. Possible optimizations by customer

7. Series manufacturing



AVAILABILITY AND REQUIREMENTS FOR THE COMPONENTS

SOLDER.embedding

All SMD components can be used in principle with the following restrictions:
- All passive components according to EIA standard 0201 to 1206
- All molded SMD packages like QFN, SOT etc.
- Substrate based packages like LGA, BGA etc.
- Maximum component size 10 x 10 mm² (further sizes may be available on request)
- Maximum component thickness dependent upon the layer structure
- No liquids or electrolytes permitted in the component
- No air inclusion permitted in the component, such as with quartz crystals with metallic cover, for example

MICROVIA.embedding

Active components:
- Bare dies with Cu-pad metallisation
- Bare dies with NiPd metallisation
- Maximum component size 10 x 10 mm² (further sizes may be available on request)

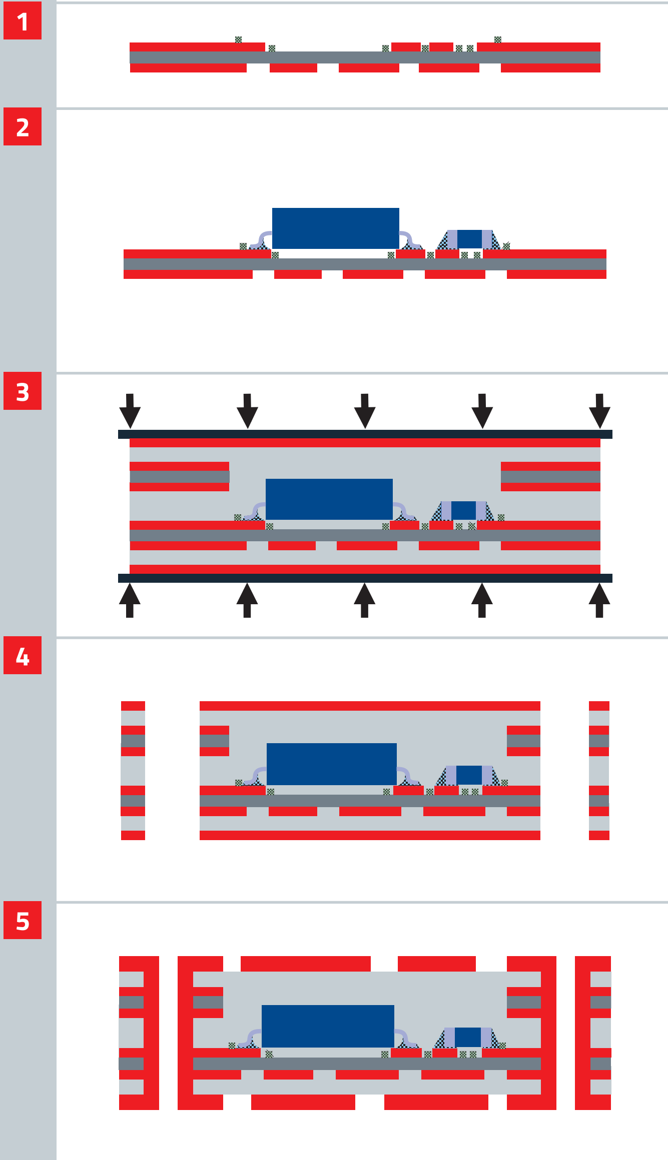
Passive components:
- Passive components (capacitors and resistors) with copper termination are purchased from Würth Elektronik directly.
- Designs: EIA 0402 and, in some cases, EIA 0201
- Resistance values: E96 series
- Capacitor values: Please contact us, as only a few values are available from the manufacturers

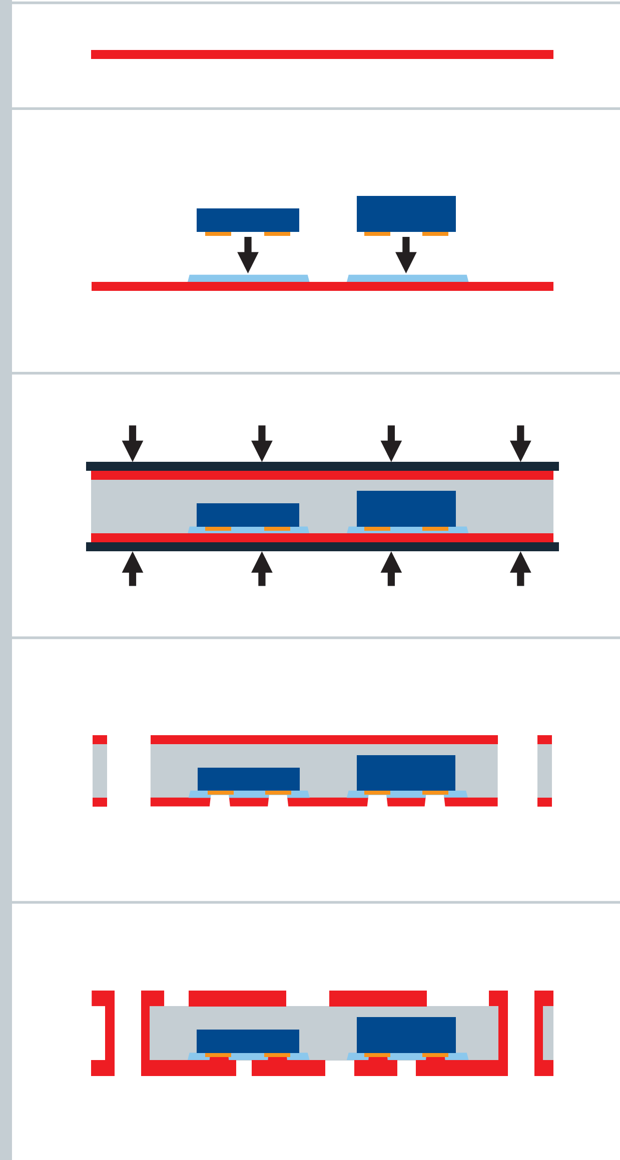
FLIP-CHIP.embedding

Active components:
- Bare dies with wire-bonded Au stud bumps
- Bare dies with Au stud bumps applied at wafer level
- Maximum component size 10 x 10 mm² (further sizes may be available on request)
- Components must be bumped (nickel-gold or gold stud bumps) or can be bumped at WE (gold stud bumps)

No passive components possible

PROCESS FLOWS





SOLDER.embedding

1. Structured inner layer core with footprint for SMD components
2. SMD assembly (lead free reflow)
3. Multilayer lamination

4+5 Depending on customer request, additional circuit board processes

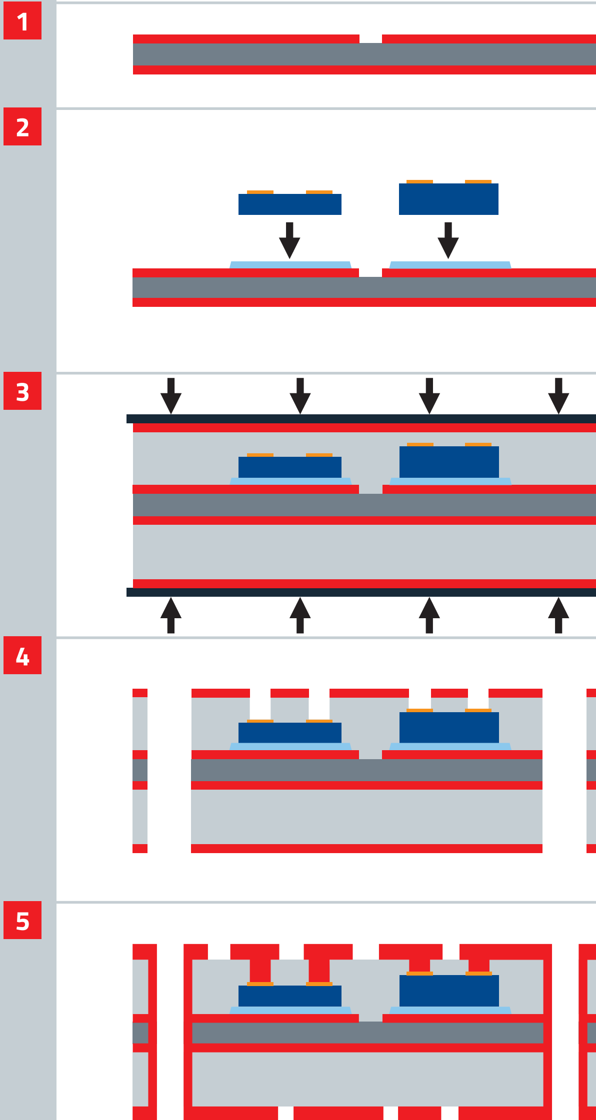
MICROVIA.embedding Version 1

1. Cu foil as starting substrate
2. Assembly (face-down) on Cu foil with non-conductive adhesive (NCA)
3. Multilayer lamination
4. Laser drilling in Cu and adhesive
5. Electrical connection between chip and PCB via Cu metallisation and structuring

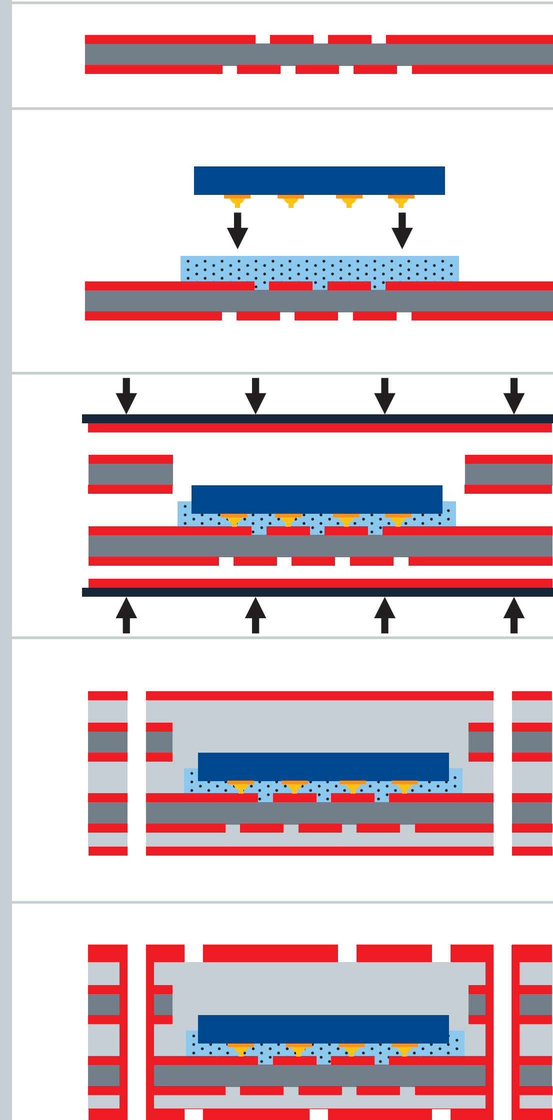
THE PROCESS FLOWS SHOWN HERE ONLY SERVE AS A DESCRIPTION OF THE PROCESS.
THE ACTUAL STACK-UP AND THE NUMBER OF LAYERS WILL BE ADAPTED TO THE CUSTOMER´S REQUIREMENT.

PROCESS FLOWS

MICROVIA.**embedding** Version 2



FLIP-CHIP.**embedding**



MICROVIA.embedding Version 2

1. Structured inner layer core
2. Assembly (face-up) on core with conductive (ICA – isotropic conductive adhesive) or non-conductive adhesive (NCA)
3. Multilayer lamination
4. Laser drilling in Cu and resin
5. Electrical connection between chip and PCB via Cu metallisation and structuring

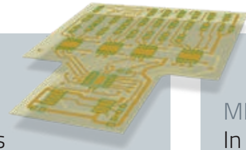
FLIP-CHIP.embedding

1. Structured inner layer core with footprint for Flip-Chip
2. Flip-Chip assembly using ACA adhesive (anisotropic conductive adhesive)
3. Multilayer lamination

4+5 Depending on customer request, additional circuit board processes

THE PROCESS FLOWS SHOWN HERE ONLY SERVE AS A DESCRIPTION OF THE PROCESS.
THE ACTUAL STACK-UP AND THE NUMBER OF LAYERS WILL BE ADAPTED TO THE CUSTOMER´S REQUIREMENT.

LAYOUT TIPS



SOLDER.**embedding**
Virtually all EDA tools are unable to implement any solder resist frames on inner layers.

- Solder resist frames for internal layers can be defined on a mechanical layer.

MICROVIA.**embedding**
In most cases, it has previously not been possible to define a microvia between the component and copper layer.

- Can be achieved by adding a (virtual) copper layer.

Placement and grouping of components
Due to the technology, not the entire inner layer area can be populated with components. The maximum area to be populated is 35-40% depending on the technology and components used and should be clarified in advance. If possible, the components should be arranged in groups and a specific distance should be left between the groups for PCB material.

Possible combinations and implementation of the technology

Possible base materials

- FR-4.1 TG150 und TG170
- Other materials and special materials on request

Can be combined with the following technologies

- Multilayer and HDI with 1–24 layers
- RIGID.**flex**
- SEMI.**flex**

PCB properties

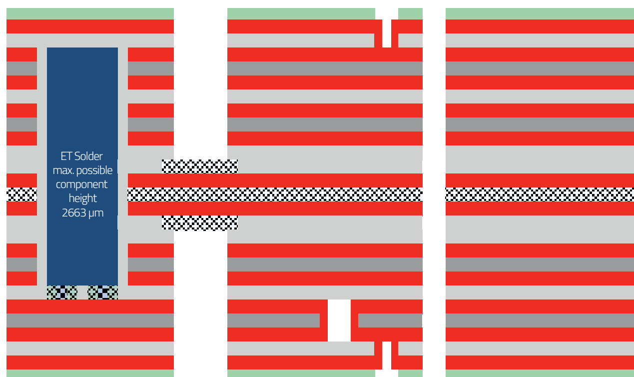
- min. inner layer thickness 0,1 mm
- Maximum final thickness 3,2 mm

Selection of tests (must be clarified in advance)

- In-Circuit Test
- Flying Probe
- Module-specific solutions such as high-voltage testing
- X-Ray inspection

Separation & Delivery

- Milling / V-Scoring
- Sawing of panels (e.g. for subsequent wafer-like dicing)
- Special delivery solutions such as SMD Tape & Reel



Example of stack-up ET12S10T + 5Ri–2F–5Ri

Design-to-Cost

Prices are individual due to the variability of layouts and processes and are composed of these points:

Basic PCB

- Base material
- Number of layers and thicknesses
- Mechanical processing
- Solder surface

Assembly

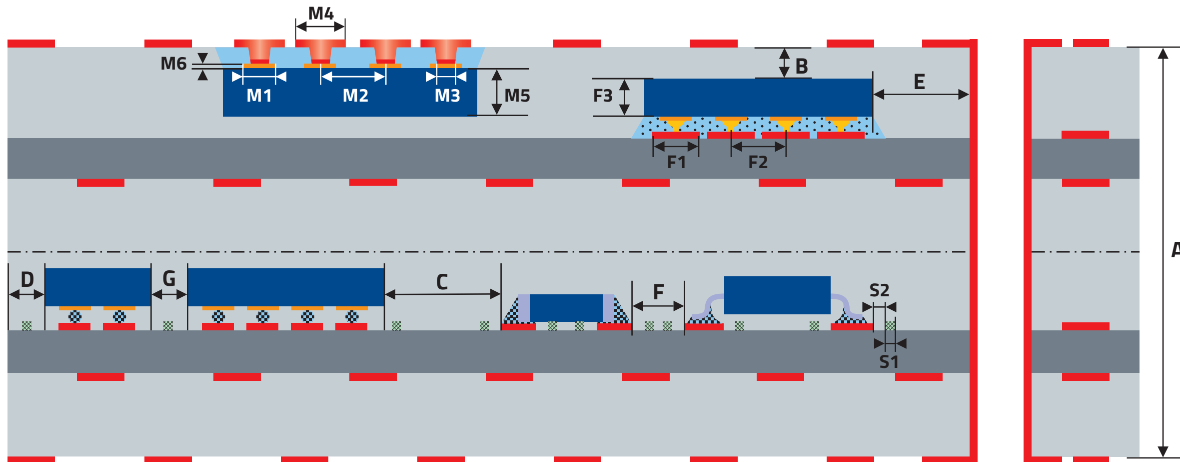
- Number of layers to be assembled
- Type of components to be assembled
- Number of components to be assembled
- Cost of SMD stencil

Scope of inspection

- Which product test are necessary
- Scope of electrical testing

Special delivery solutions

EMBEDDING TECHNOLOGY
DESIGN RULES



SOLDER.embedding
S1 Solder resist frames: 100 µm (advanced: 75 µm)
S2 Solder resist clearance: 75 µm (advanced: 50 µm)

MICROVIA.embedding
M1 Pad size of component: ≥ 150 µm
M2 Pitch on component/PCB: ≥ 250 µm
M3 Microvia onto component: ≥ 50 µm
M4 Pad size PCB: ≥ 175 µm
M5 Thickness of component: ≥ 150 µm
M6 Thickness of pad metal: ≥ 8 µm

FLIP-CHIP.embedding
F1 Pad size PCB: ≥ 75 µm
F2 Pitch on component/PCB: ≥ 150 µm
F3 Thickness of component: ≥ 150 µm

A PCB thickness – according to our general PCB specification.
- Standard: 2,4 mm
- Upon request: 3,2 mm
- In special cases: > 3,2 mm (needs to be evaluated for specific applications)

B Layer stack-up
- At least one layer of prepreg should always be inserted between the component and the copper layer above, or it must be ≥ 100 µm (smaller on request).
- Based on assembly technology and layer stack, the max. thickness of the components is calculated
- The WE layer stack-up proposal specifies the maximum possible component height – or references the maximum component height.

C Distance group to group or component to group:
- Min. 1.000 µm
- 700 µm also possible upon request (700 µm ≙ 300 µm material + 2 × 200 µm clearance)

D Distance component to PCB edge
≥ 500 µm (less possible upon request and after clarification)

E Distance via to component edge
≥ 500 µm (less possible upon request and after clarification)

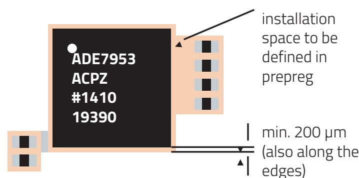
F Distance component to component
- Condition: pad of the footprint extends beyond the component.
- ≥ 300 µm between the pads
- Smaller distances upon request and after clarification

G Distance between component and component
- Condition: component extends beyond pads
- ≥ 200 µm between component outlines
- Smaller distances upon request and after clarification

Components in general
- All components must fit into the actual layer stack-up
- No component may protrude in the z-axis
- Max. component size: 10 × 10 mm^2
- Components must not contain cavities (e.g. Quartz Crystal devices) or liquids (e.g. liquid electrolytes).

Placement of components
- Occupation of an inner layer with components
  - max. 40 % of the available are
  - Individual clarification necessary with > 40 % occupancy
- Components should be grouped
- Max. size of the group: each point in the group must be reachable from the group edge within 5 mm to ensure the resin flow into the cavity of each group

Component positioning – resin flow



The following applies to the cut-outs milled in prepreg:
All points within the cut-out must be accessible at a distance of ≤ 5.0 mm from the boundary of the cut-out.

Nomenclature

The nomenclature includes technology, placement level and part orientation and is composed for DEVICE.embedding as follows:

ETXBYO

ET	Reference to embedding technology
X	Total number of layers in stack-up
B	Technology: S for SOLDER.embedding, M for MICROVIA.embedding and F for FLIP-CHIP.embedding
Y	Placement layer counted from top (=1) downwards
O	Orientation of components on the placement layer: T for top and B for bottom of the layer

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