DESIGN, LAYOUT & SIMULATION OF 3-PHASE ACDC FILTERS

Andreas Nadler
Field Application Engineer
WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

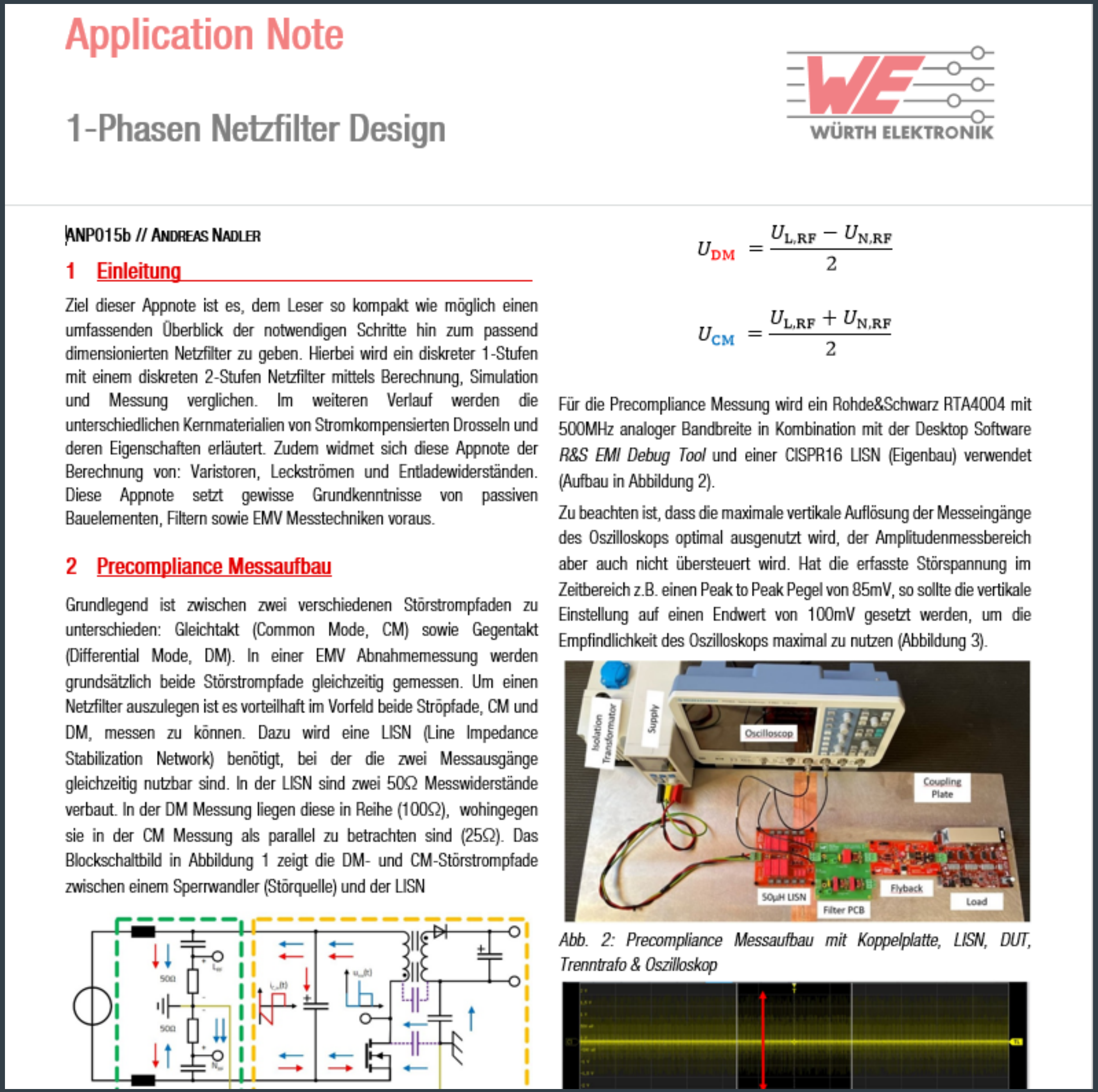
3-Phase Filter Design

- Sources of interference
- Components for filtering
- Filter Design
- Y-Cap placement, leakage current and PE connection style
- Calculation and simulation
- Measurements of interference suppression
- Varistor calculation and placement

FILTER DESIGN 1-PHASE & DCDC

Related Appnote: ANP015

Coming 2025: ANP137 (3-Phase)



Application Note

1-Phasen Netzfilter Design

ANP015b // Andreas Nadler

1 Einleitung

Ziel dieser Appnote ist es, dem Leser so kompakt wie möglich einen umfassenden Überblick der notwendigen Schritte hin zum passend dimensionierten Netzfilter zu geben. Hierbei wird ein diskreter 1-Stufen mit einem diskreten 2-Stufen Netzfilter mittels Berechnung, Simulation und Messung verglichen. Im weiteren Verlauf werden die unterschiedlichen Kernmaterialien von Stromkompensierten Drosseln und deren Eigenschaften erläutert. Zudem widmet sich diese Appnote der Berechnung von: Varistoren, Leckströmen und Entladewiderständen. Diese Appnote setzt gewisse Grundkenntnisse von passiven Bauelementen, Filtern sowie EMV Messtechniken voraus.

2 Precompliance Messaufbau

Grundlegend ist zwischen zwei verschiedenen Störstrompfaden zu unterschieden: Gleichtakt (Common Mode, CM) sowie Gegentakt (Differential Mode, DM). In einer EMV Abnahmemessung werden grundsätzlich beide Störstrompfade gleichzeitig gemessen. Um einen Netzfilter auszulegen ist es vorteilhaft im Vorfeld beide Strõpfade, CM und DM, messen zu können. Dazu wird eine LISN (Line Impedance Stabilization Network) benötigt, bei der die zwei Messausgänge gleichzeitig nutzbar sind. In der LISN sind zwei 50Ω Messwiderstände verbaut. In der DM Messung liegen diese in Reihe (100Ω), wohingegen sie in der CM Messung als parallel zu betrachten sind (25Ω). Das Blockschaltbild in Abbildung 1 zeigt die DM- und CM-Störstrompfade zwischen einem Sperrwandler (Störquelle) und der LISN

$$U_{DM} = \frac{U_{L,RF} - U_{N,RF}}{2}$$

$$U_{CM} = \frac{U_{L,RF} + U_{N,RF}}{2}$$

Für die Precompliance Messung wird ein Rohde&Schwarz RTA4004 mit 500MHz analoger Bandbreite in Kombination mit der Desktop Software *R&S EMI Debug Tool* und einer CISPR16 LISN (Eigenbau) verwendet (Aufbau in Abbildung 2).

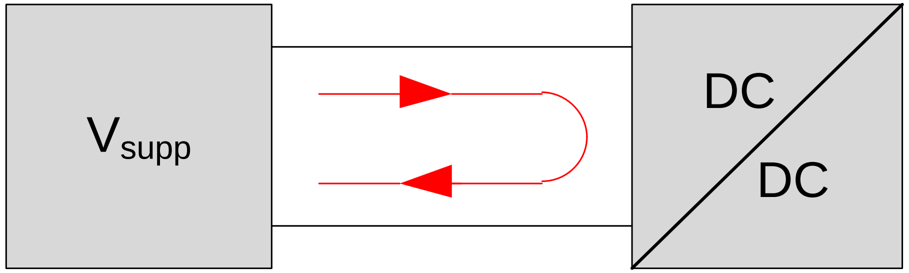
Zu beachten ist, dass die maximale vertikale Auflösung der Messeingänge des Oszilloskops optimal ausgenutzt wird, der Amplitudenmessbereich aber auch nicht übersteuert wird. Hat die erfasste Störspannung im Zeitbereich z.B. einen Peak to Peak Pegel von 85mV, so sollte die vertikale Einstellung auf einen Endwert von 100mV gesetzt werden, um die Empfindlichkeit des Oszilloskops maximal zu nutzen (Abbildung 3).

Abb. 2: Precompliance Messaufbau mit Koppelplatte, LISN, DUT, Trenntrafo & Oszilloskop

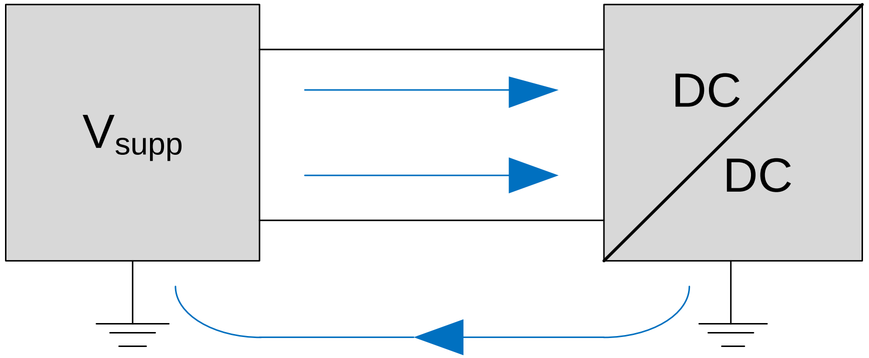
SOURCE OF INTERFERENCE

Differntial Mode & Common Mode

Differential Mode



Common Mode



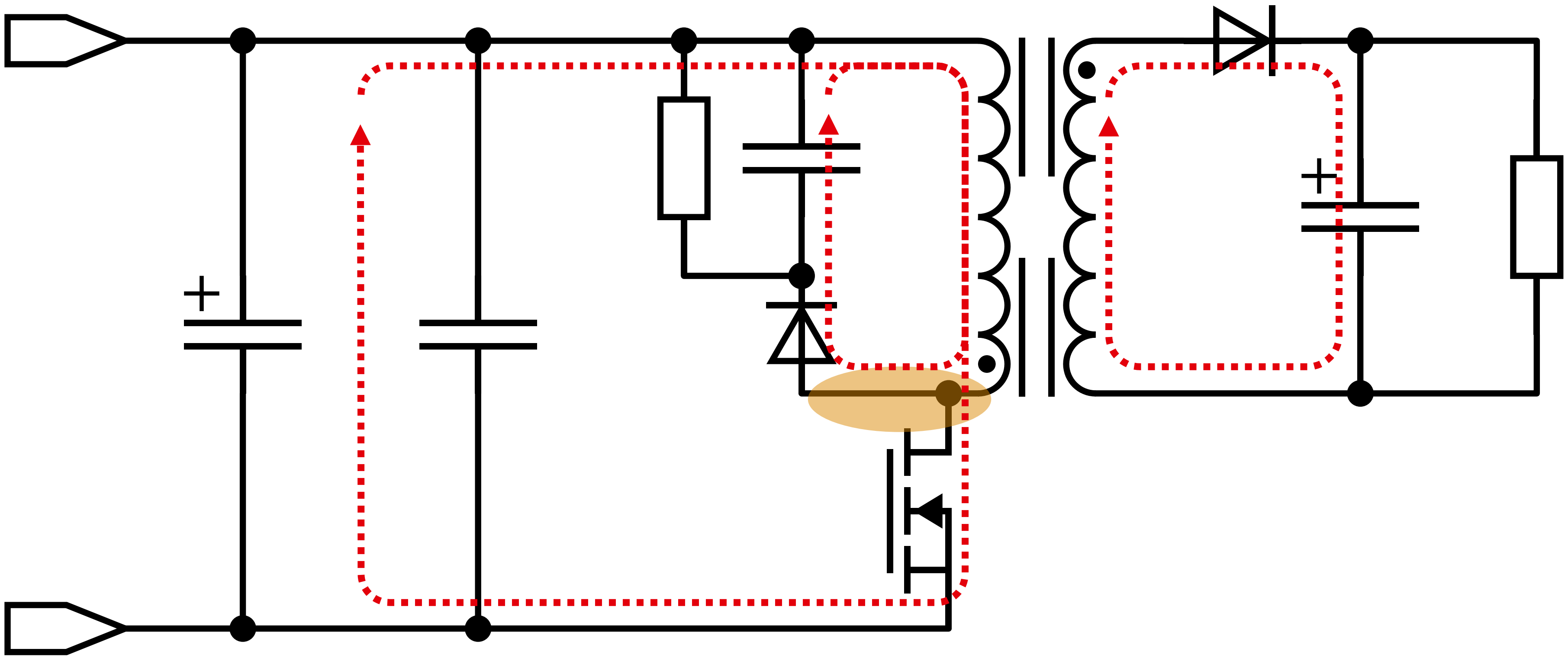
CM & DM comparisson

- **Differential mode currents**
- Current path as in circuit diagram
- Easy to follow paths
- Return current path very close
- Relatively large currents
- Filtering with LC , π , T topologies
- dI / dt is dominant cause
- Conducted EMI problem

- **Common-mode currents**
- Unexpected current path
- Current flows via parasitic paths
- Return current path very large
- Relatively small currents (μA)
- Filtering with CMC and Y-caps
- dU / dt is dominant cause
- Radiated & conducted EMI problem

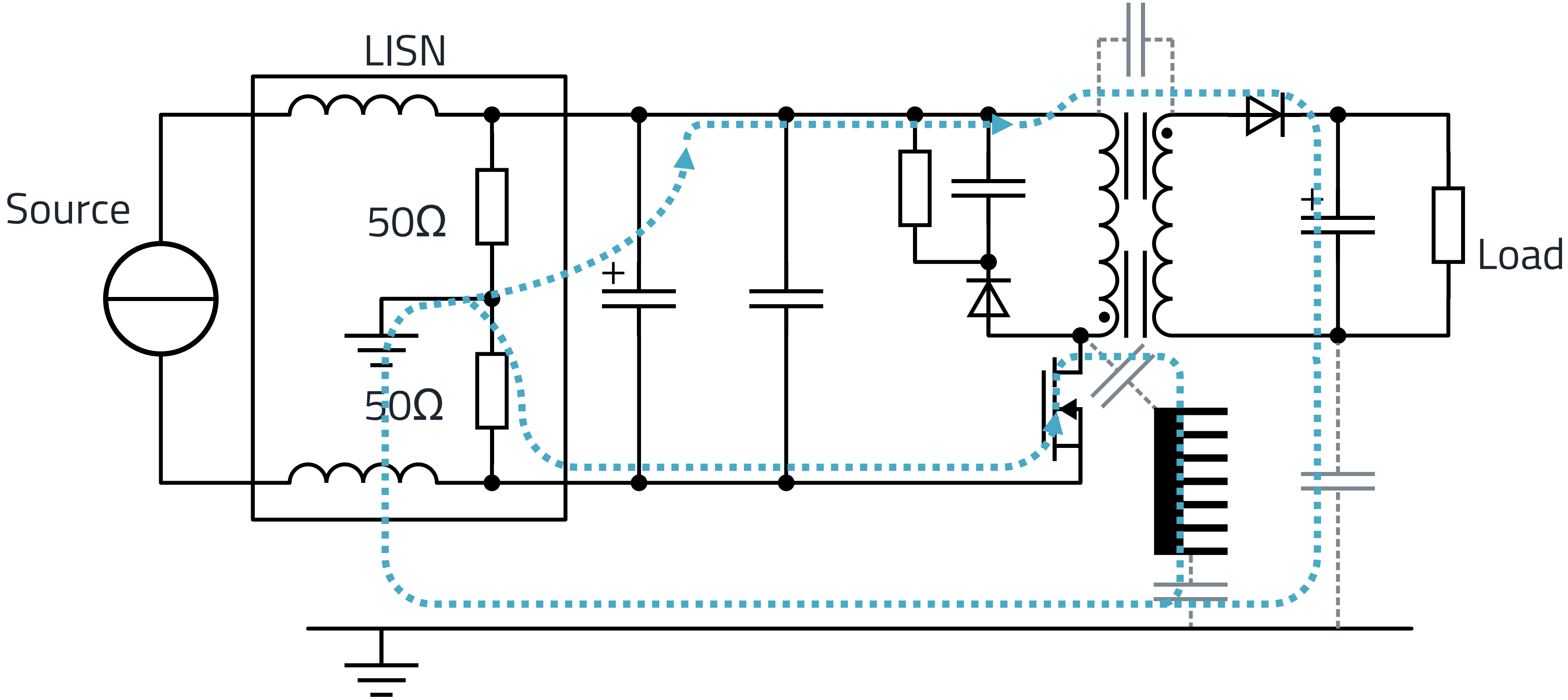
Introduction - Flyback Converter

Hot Node and Critical Loops



Introduction - Capacitive Coupling in a Flyback Converter

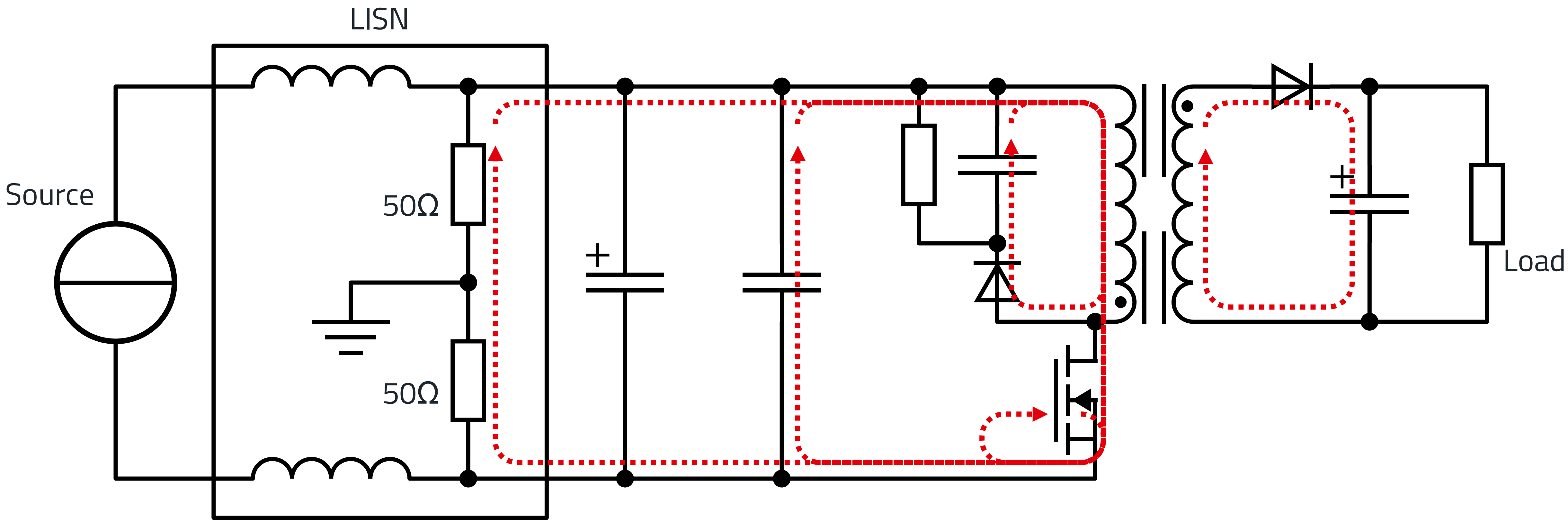
Common mode current paths



High du/dt common mode currents through parasitic capacitances (electric dipole and monopole antennas)

Introduction - Inductive Coupling in a Flyback Converter

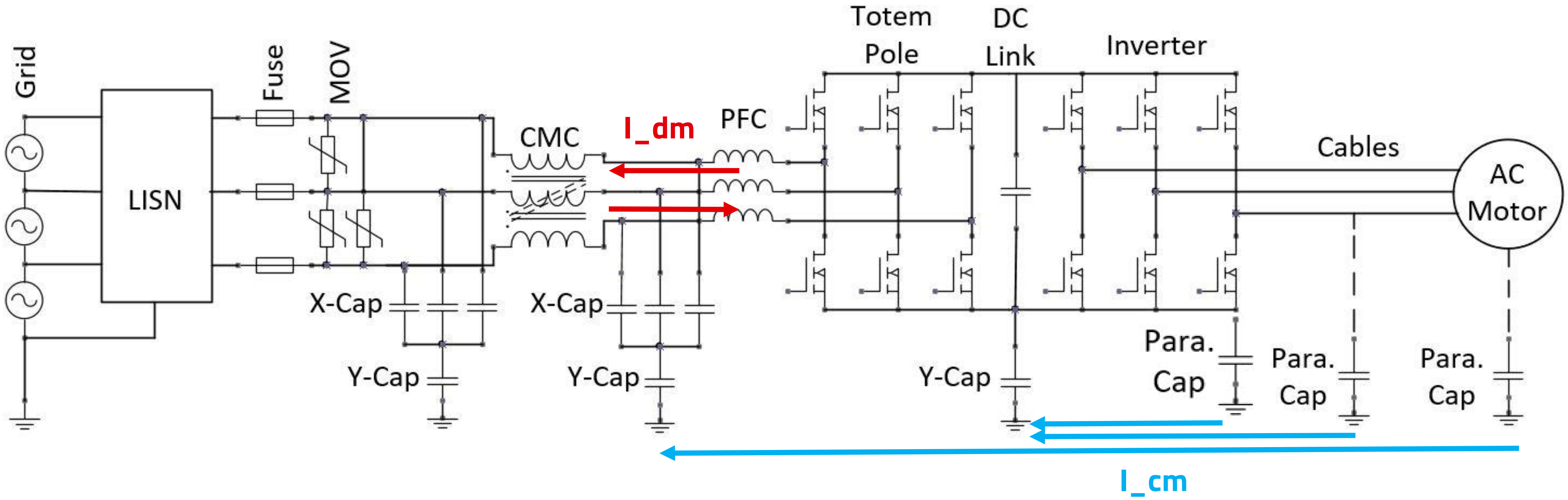
Differential mode current paths



Inductive coupling caused by high di/dt differential mode currents
(magnetic loop antennas)

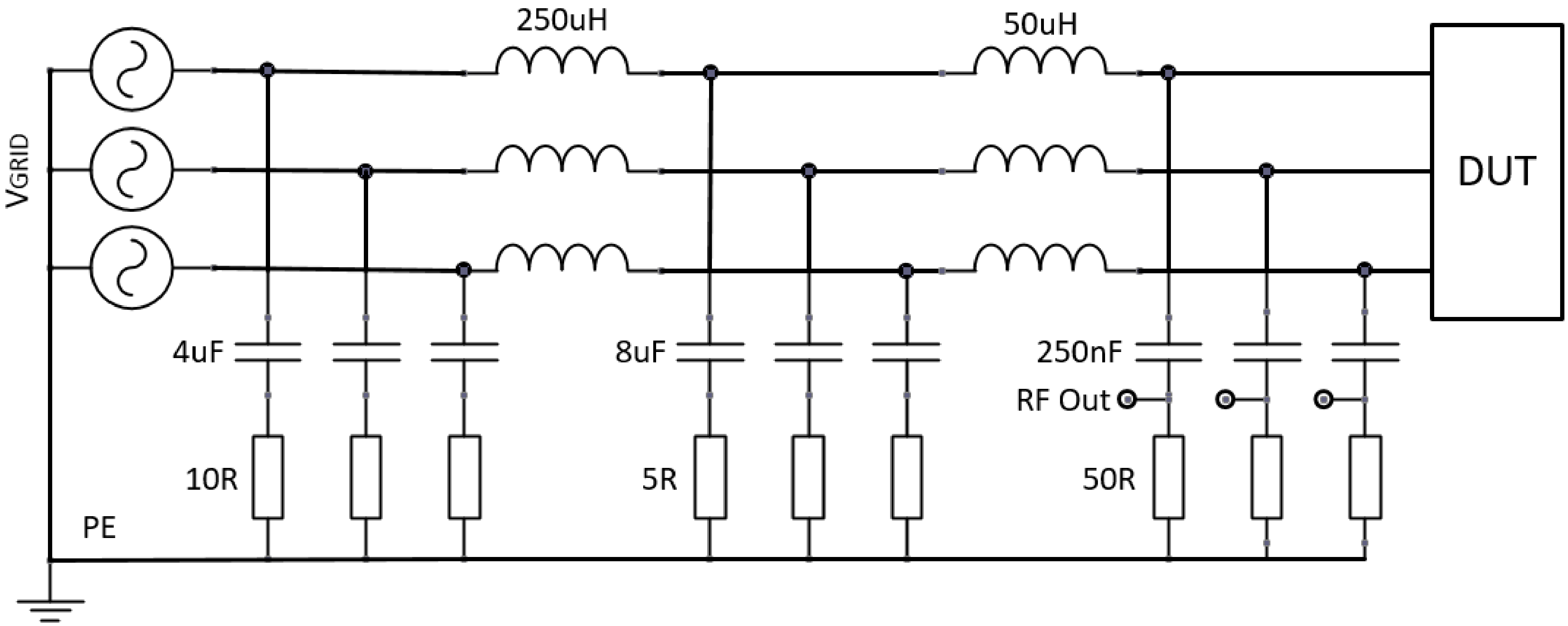
Sources of interference 3 phase system

Typical application: inverter for industrial drives



3-Phase LISN

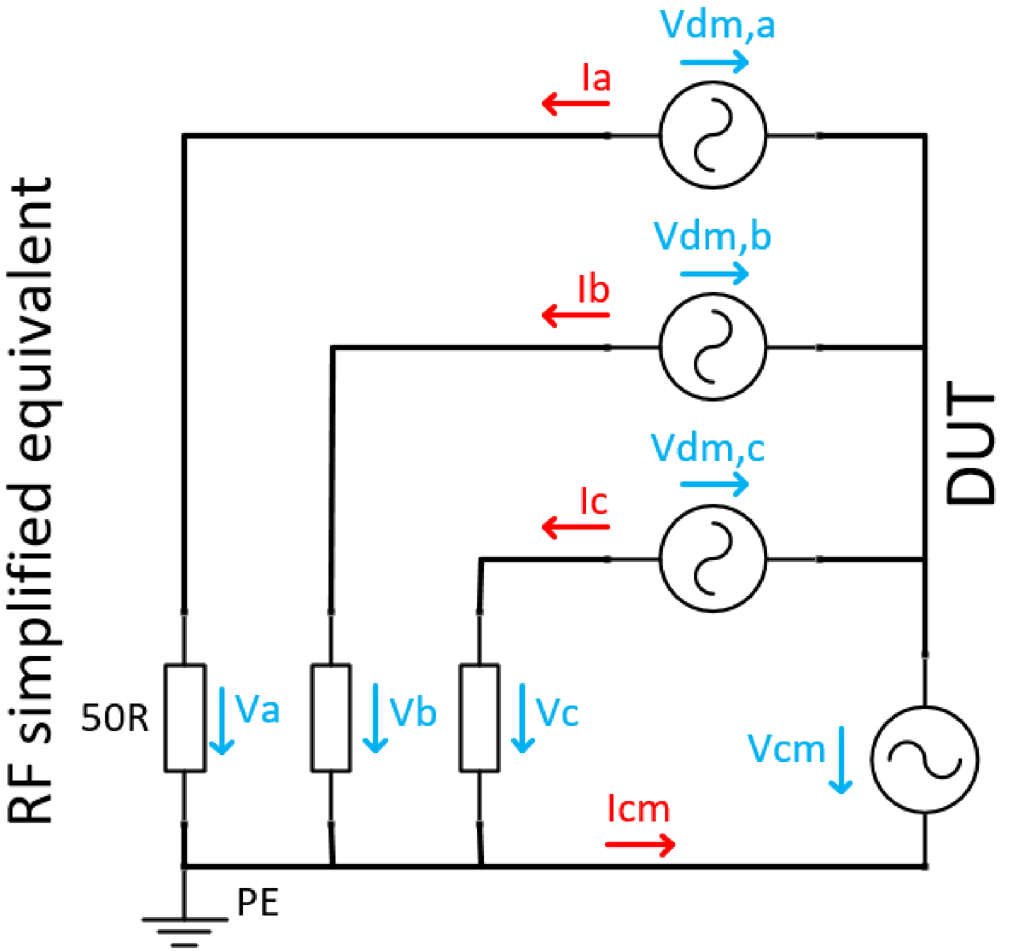
CISPR 16 LISN



LISN / DUT

Simplified RF model

- $R_{CM} = \frac{R_{LISN}}{3} = \frac{50\Omega}{3} = 16.67\Omega$
- $R_{DM} = R_{LISN} \cdot 2 = 50\Omega \cdot 2 = 100\Omega$
- $I_{CM} = I_a + I_b + I_c$
- $I_{DM,a} + I_{DM,b} + I_{DM,c} = 0$
- $V_{CM} = I_{CM} \cdot \frac{R_{LISN}}{3} = \frac{V_a+V_b+V_c}{3}$
- $V_{DM,a} = V_a - V_{CM} = \frac{2 \cdot V_a}{3} \cdot \frac{V_b}{3} \cdot \frac{V_c}{3}$



COMPONENTS

X1 / Y2 Caps

MKP Film(Prototyp Status)

- WCAP-FTY2
- Pitch 10 – 37,5mm
- Vr: 330VAC
- 1nF – 1µF
- X1 + Y2 class

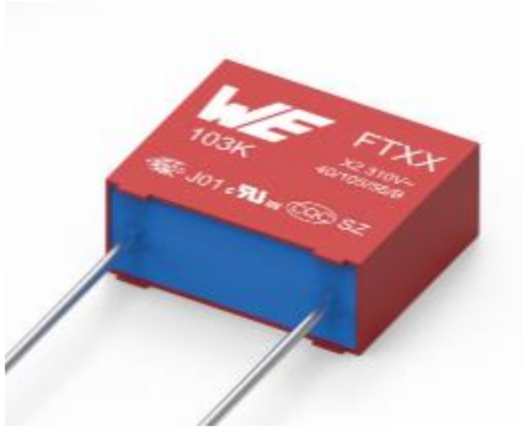
MLCC X7R / NP0

- WCAP-CSSA
- 1808 – 2220
- Vr: 250VAC
- 33pF – 4.7nF
- X1 + Y2 class
- -55°C to +125°C

X2 Caps

MKP

- WCAP-FTXX / FTX2
- Pitch: 7.5 – 37.5mm
- Vr: 310VAC / 275VAC
- 5.6nF – 6.8µF
- -40°C to +105°C



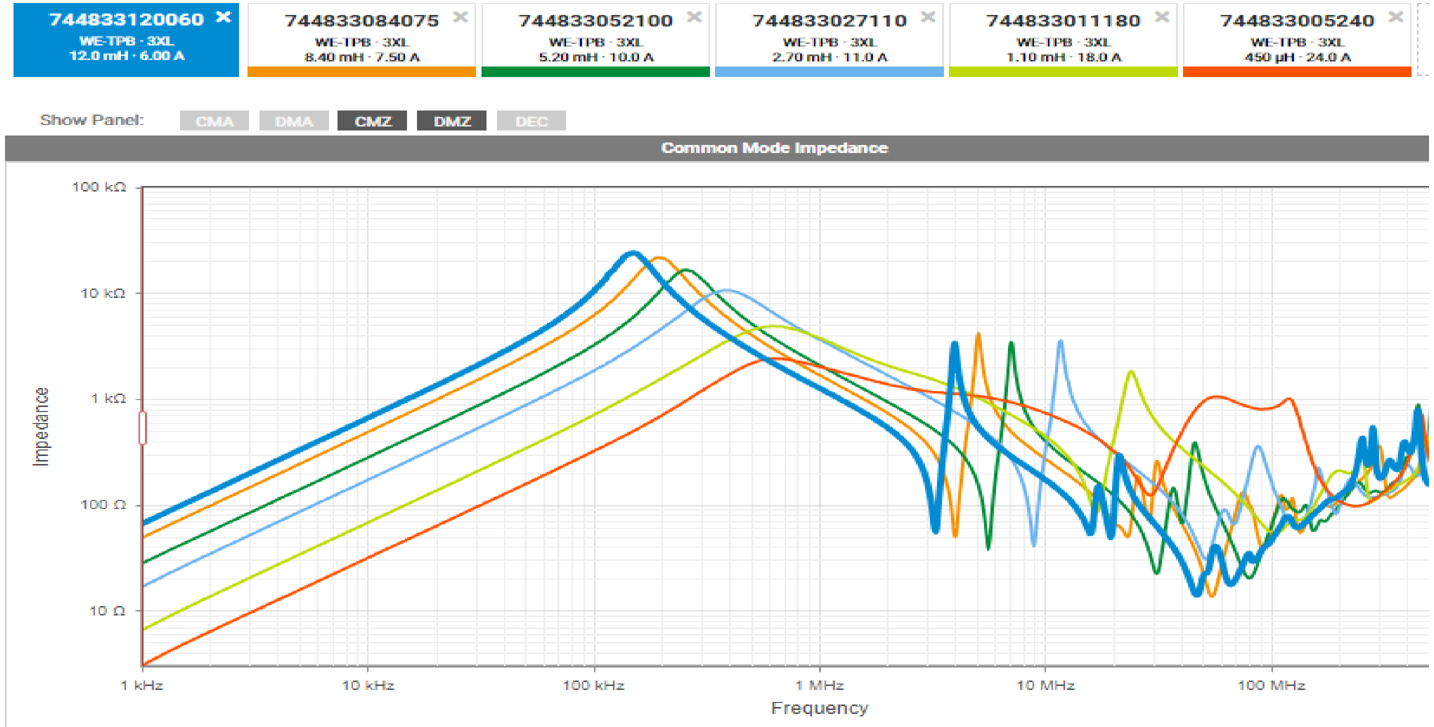
MKP

- WCAP-FTXH
- Pitch: 15 – 37.5mm
- Vr: 310VAC
- 33nF – 10µF
- -40°C to +110°C
- THB rated: 1000h @ 85°C + 85% humidity

CMC´s

3-phase 500V - WE-TPB – Ø47mm

- **MnZn** core material / -40°C to +125°C
- 1kHz to 2MHz effective frequency range
- Up to 24A
- 0,52mH to 12mH

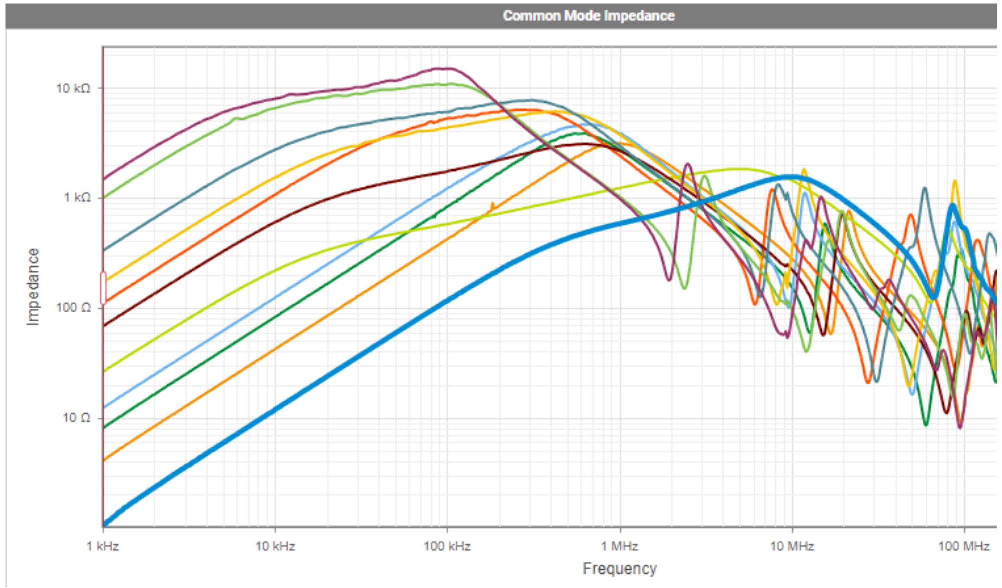


CMC´s

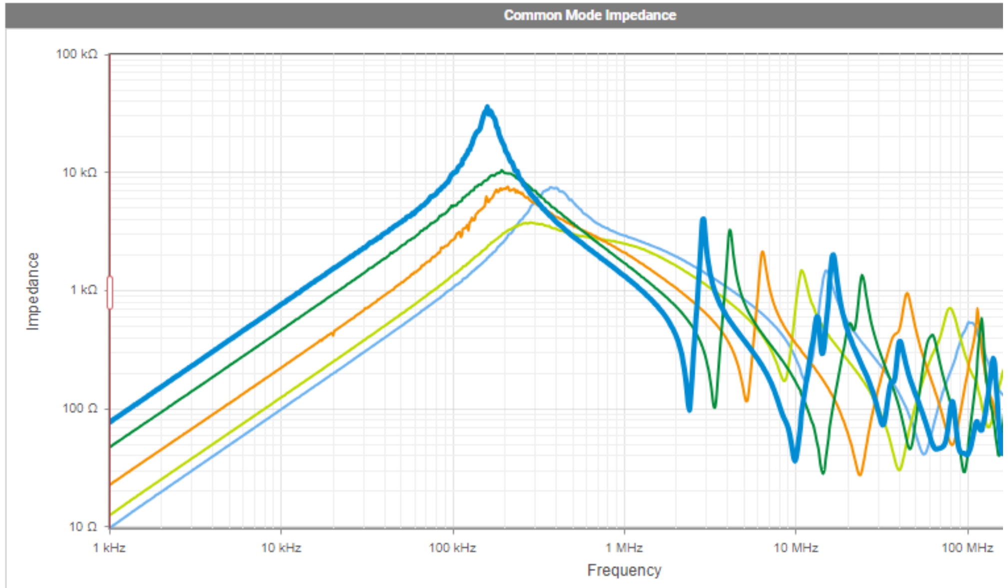
3-phase 760V – WE-TPBHV – Ø70mm

- MnZn & Nanocrystaline core materials / -40°C to +125°C
- 1kHz to 20MHz effective frequency range
- Up to 46A
- 0,2mH to 208mH

Nanocrystaline



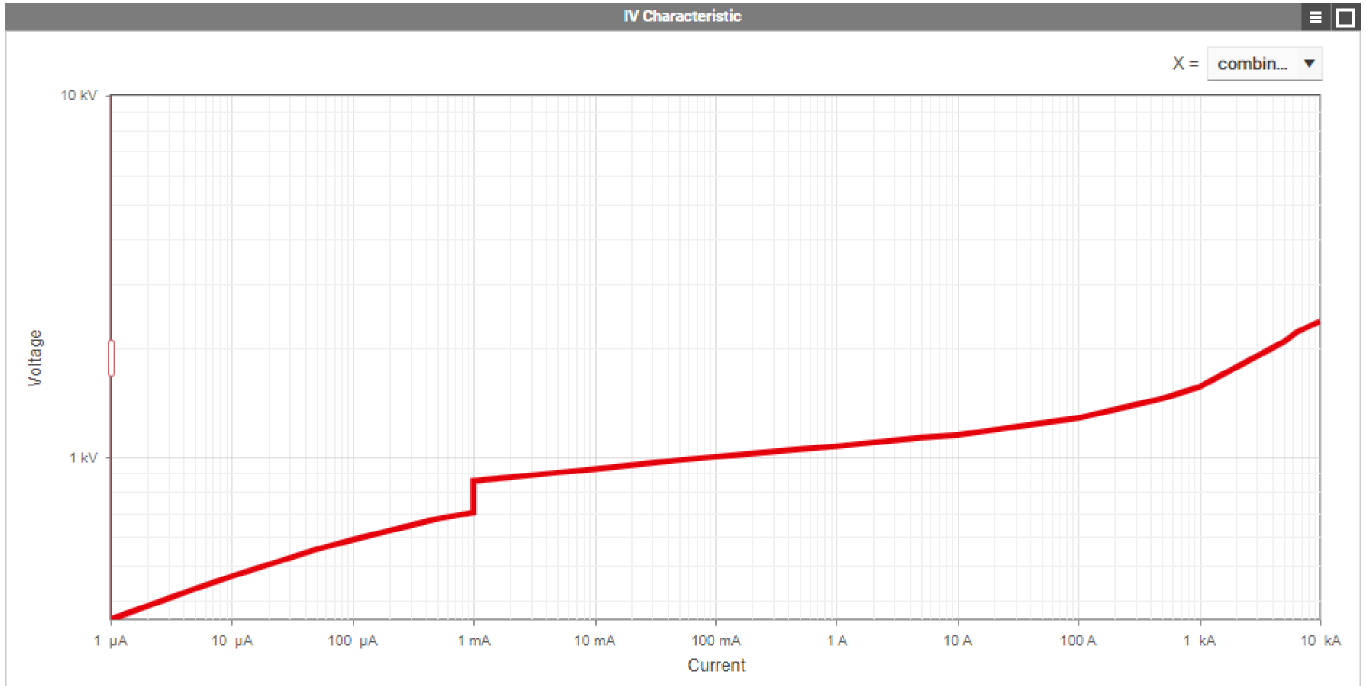
MnZn



Surge Protection Varistors

WE-VD

- 5 – 20mm Ø THT
- Vrms: 14V – 1000V
- Imax: 100A – 10000A
- -40°C to 85°C
- UL, IEC & VDE certified

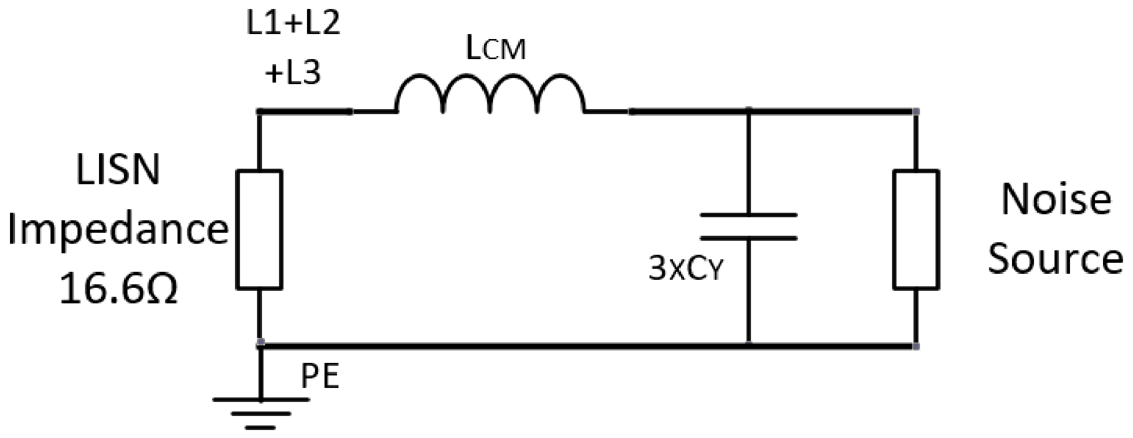


POSSIBLE FILTER STRUCTURES

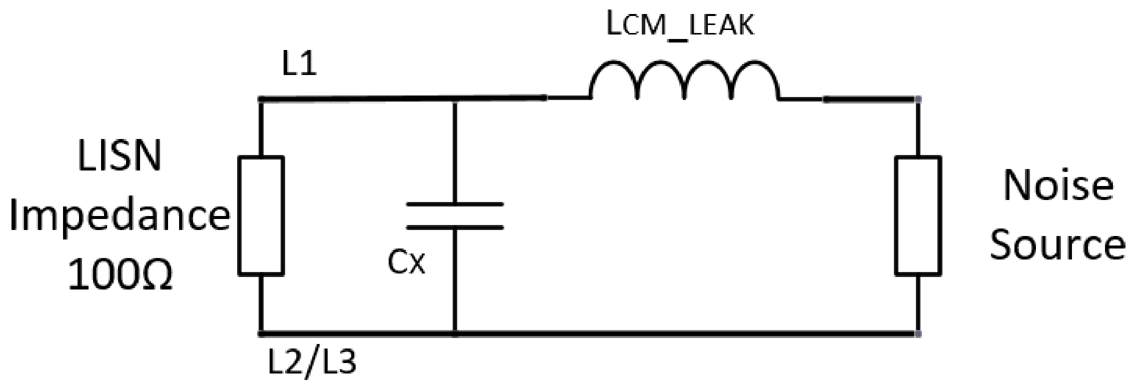
CM & DM Filter Equivalent

Effective LISN Impedance and Component Arrangement

- CM

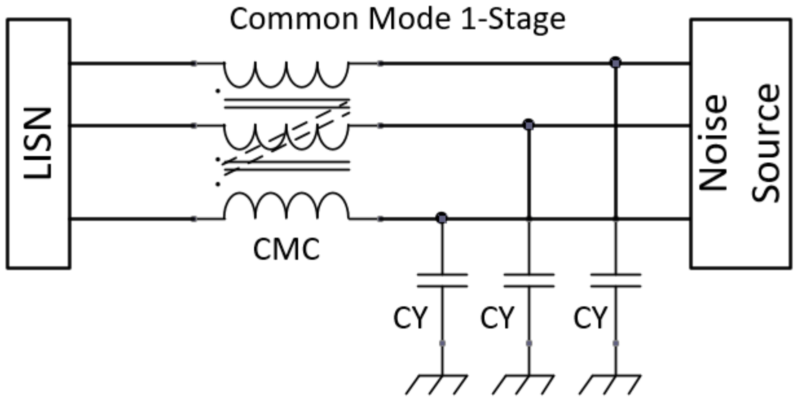


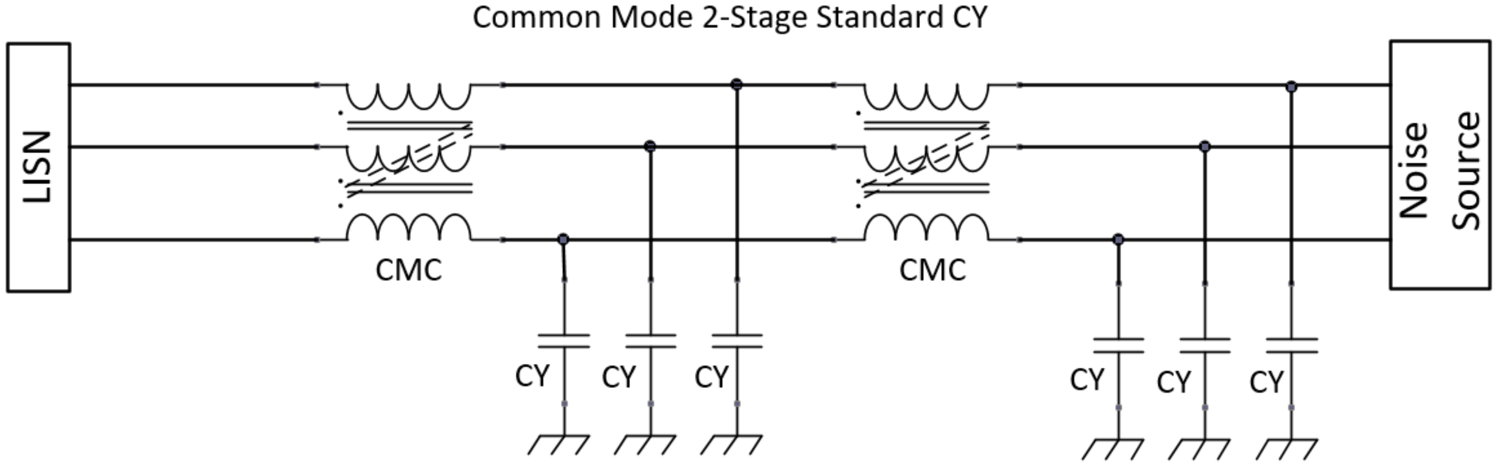
- DM

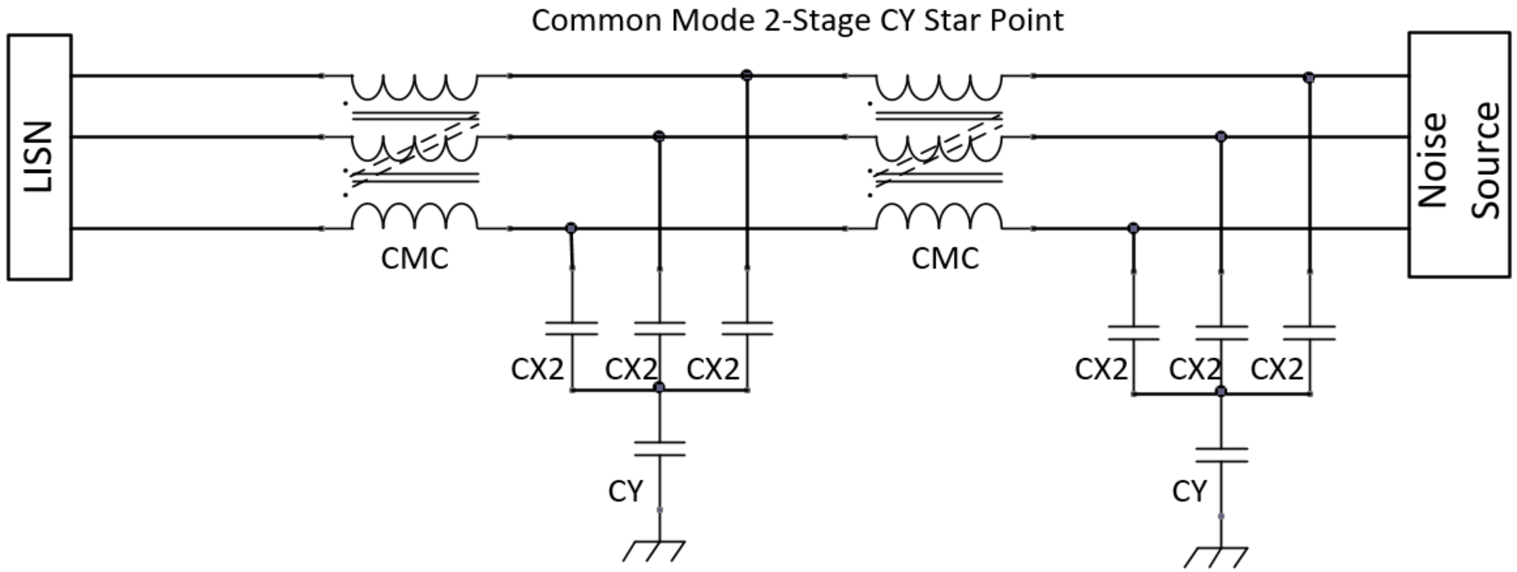


Possible Filter Structures Common Mode

Main CMC Inductance + Y-Caps



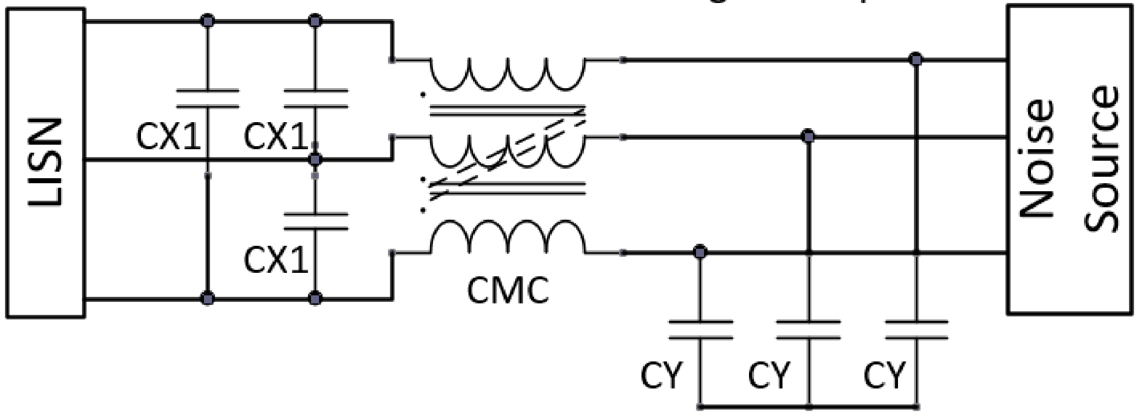




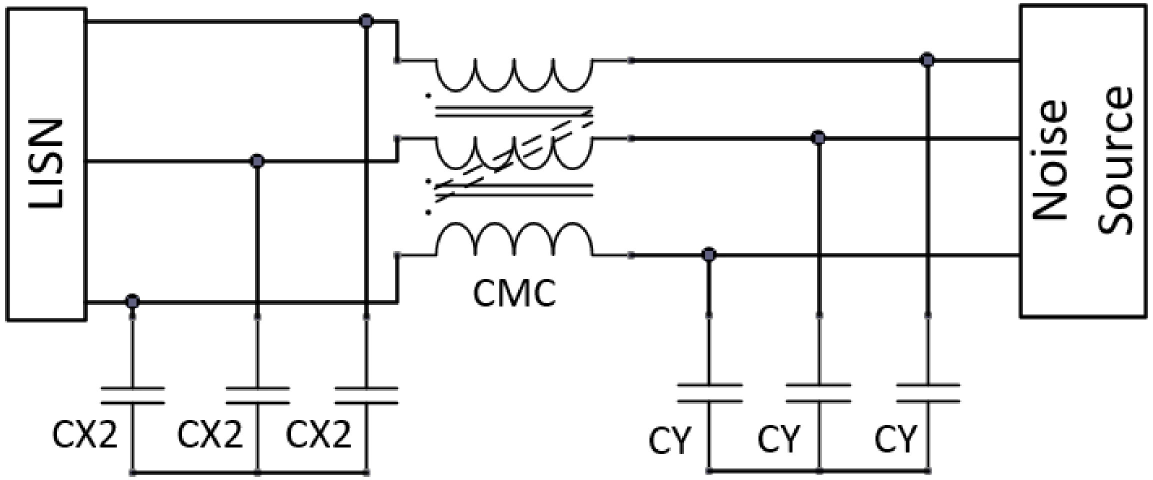
Possible Filter Structures Differential Mode

CMC Stray Inductance + X-Caps

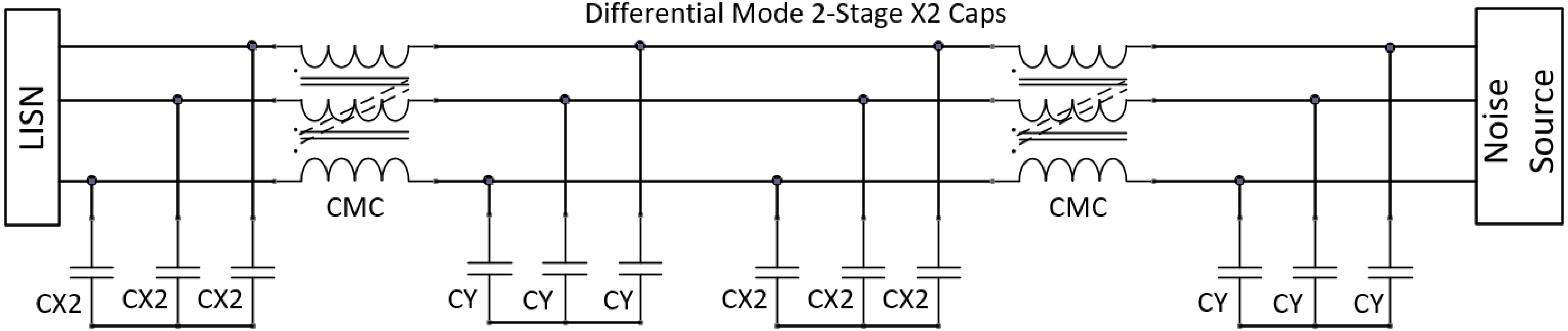
Differential Mode 1-Stage X1 Caps



Differential Mode 1-Stage X2 Caps



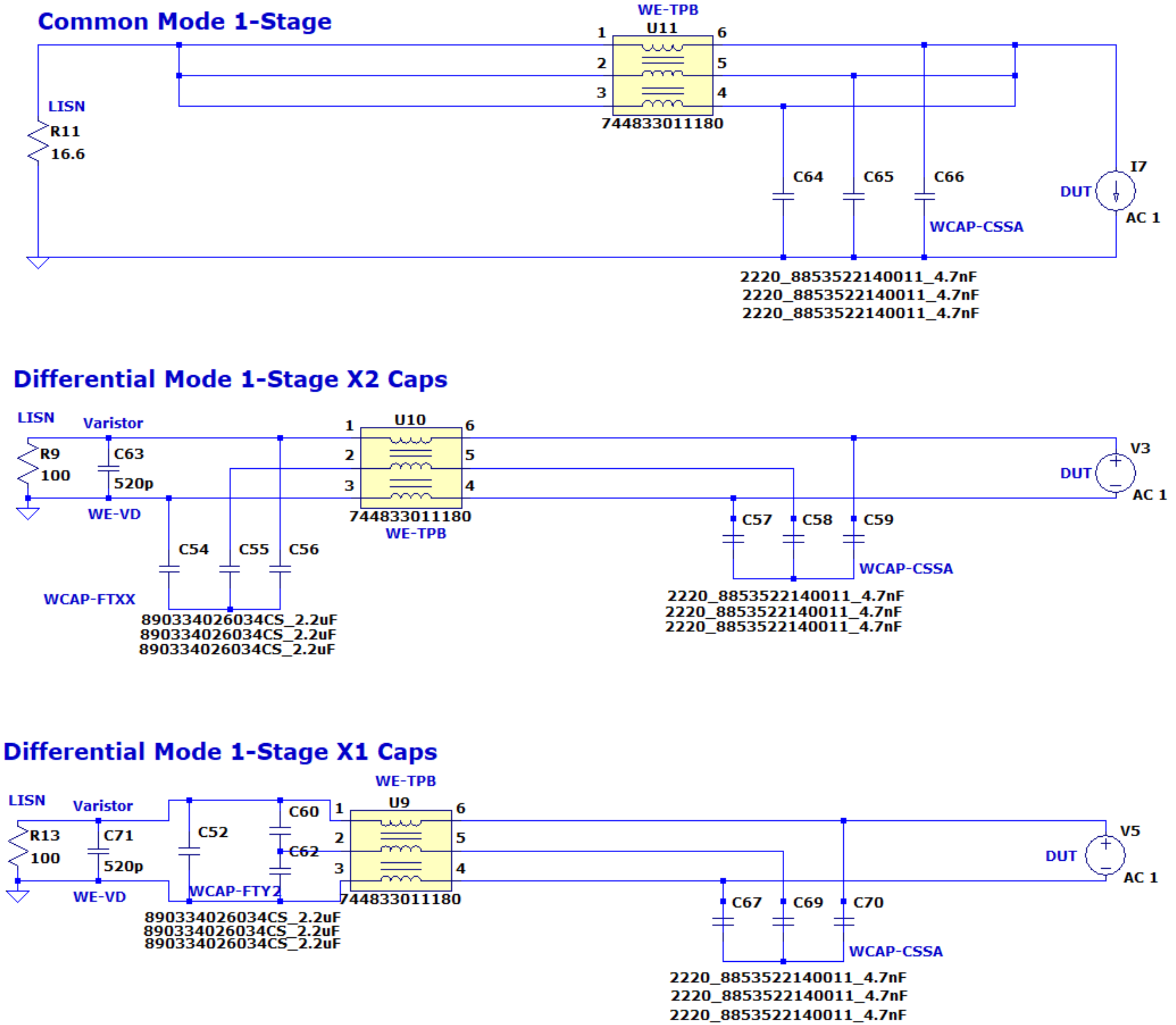
Differential Mode 2-Stage X2 Caps



SIMULATION OF DIFFERENT FILTER STRUCTURES

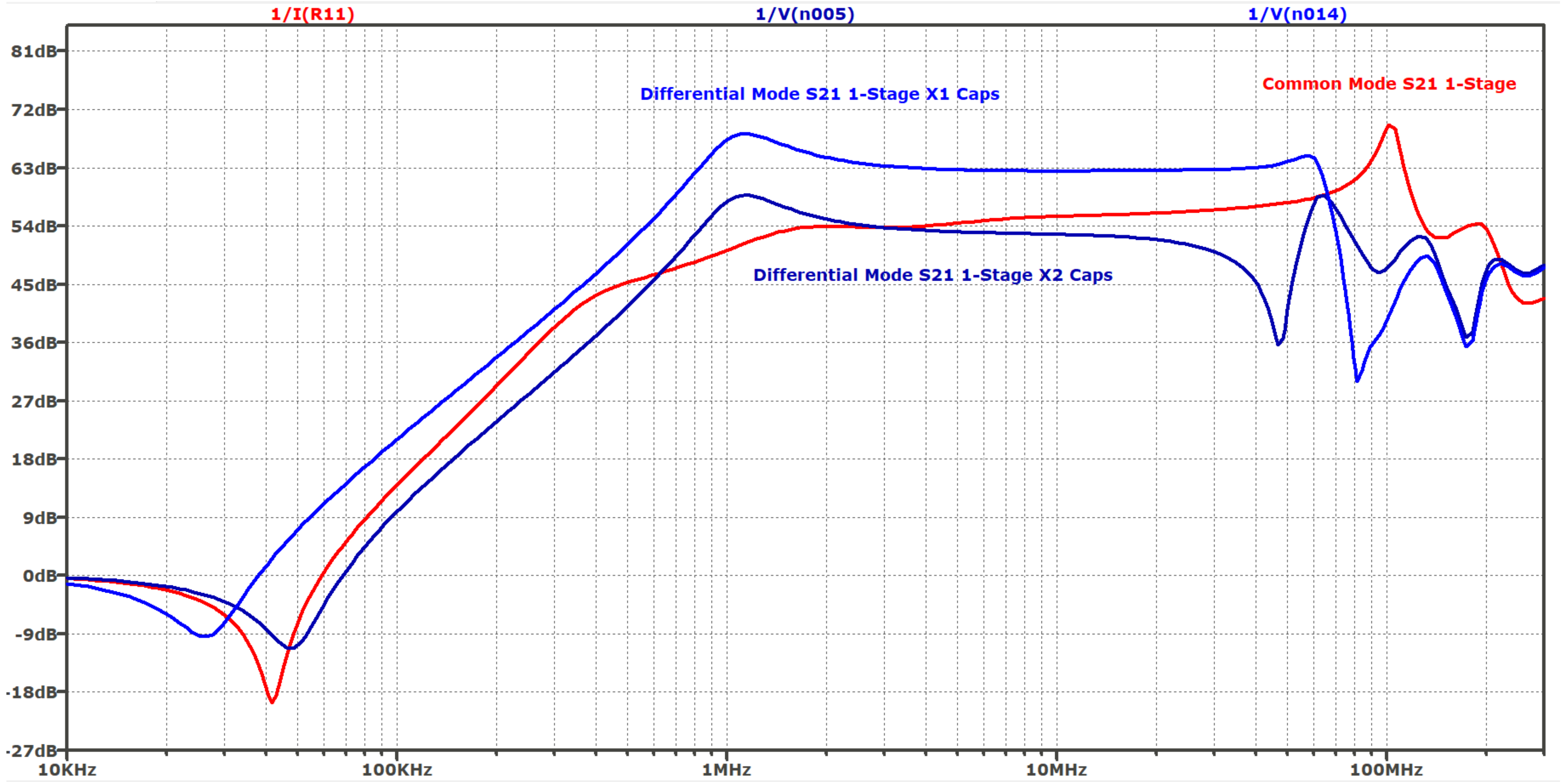
LT Spice Simulation

1-stage filter for 400V / 18A / 11kW



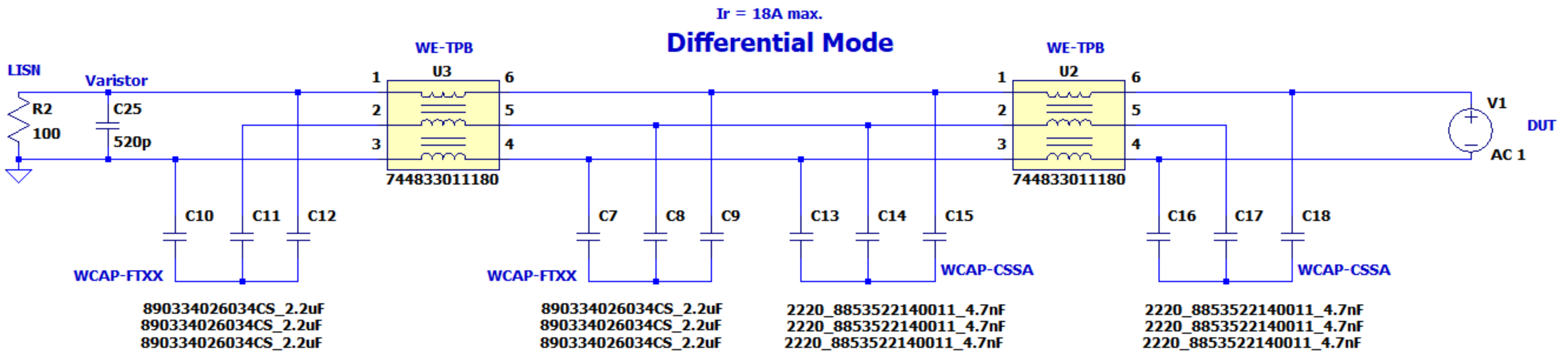
LT Spice Simulation Insertion Loss

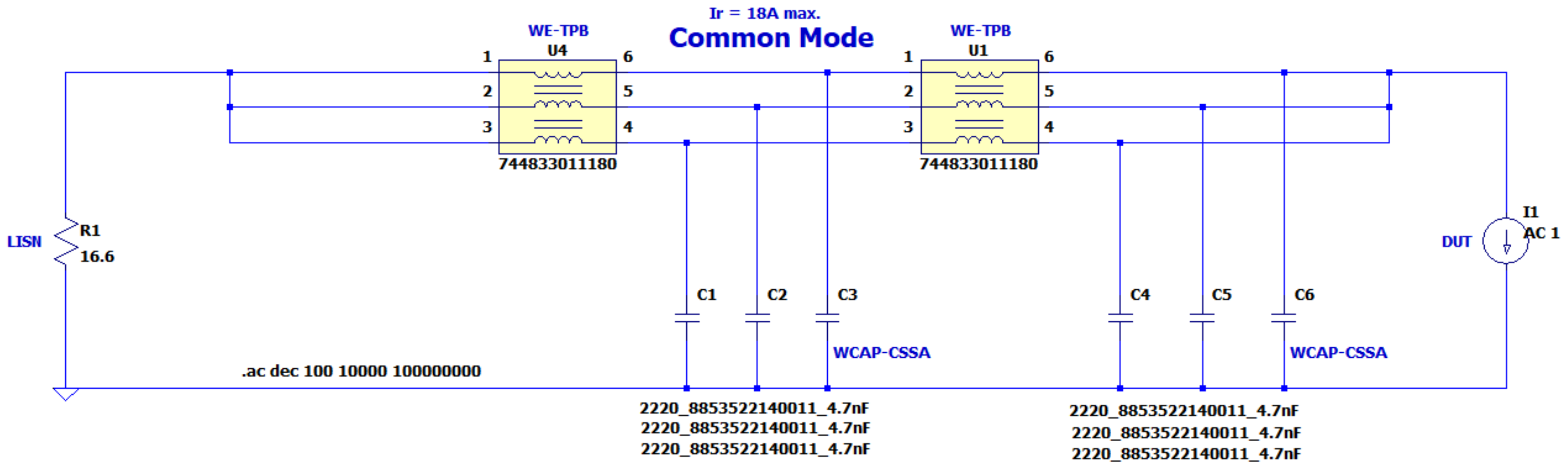
1-stage filter for 400V / 18A / 11kW



LT Spice Simulation

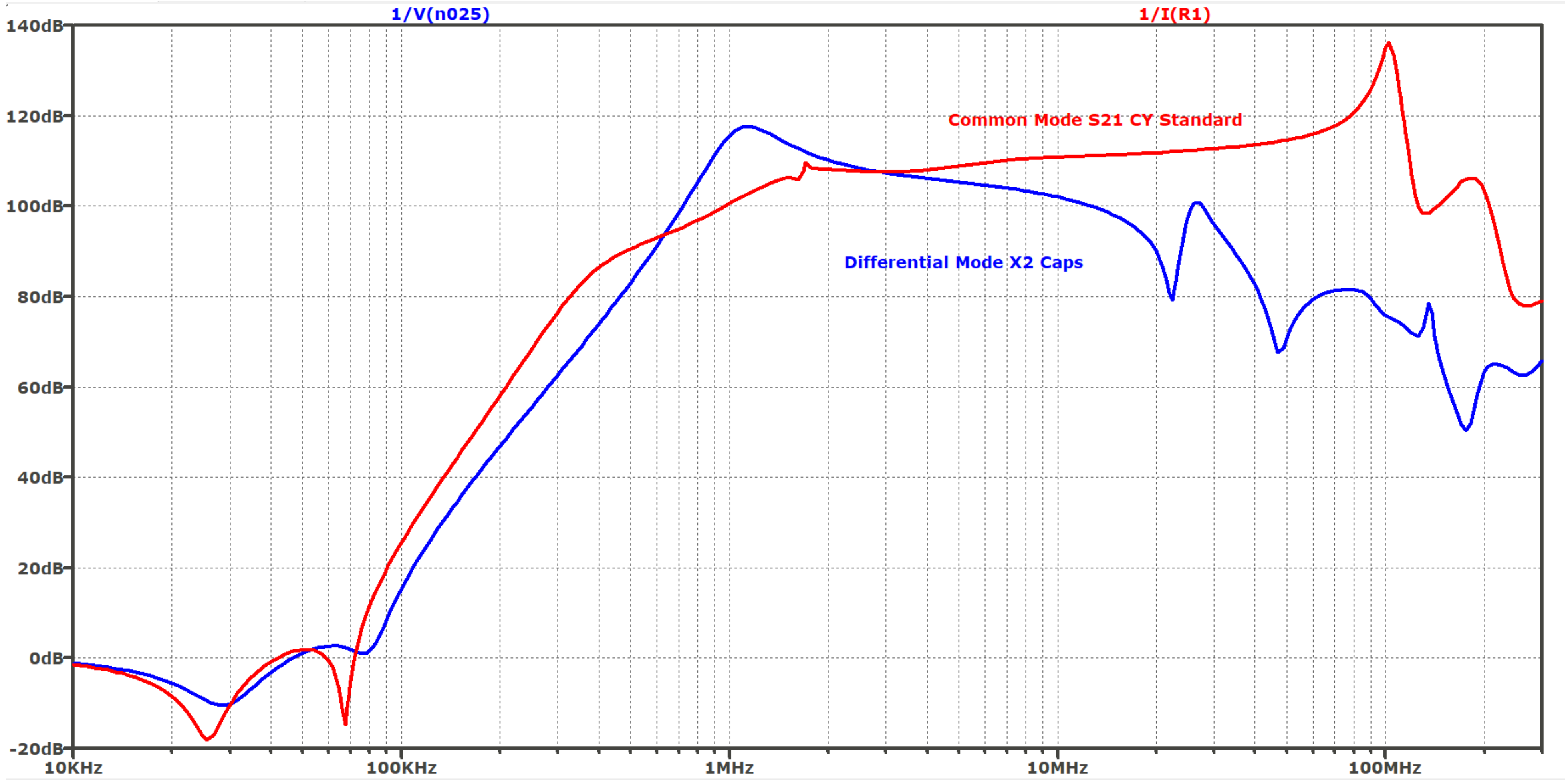
2-stage filter for 400V / 18A / 11kW / Standard CY





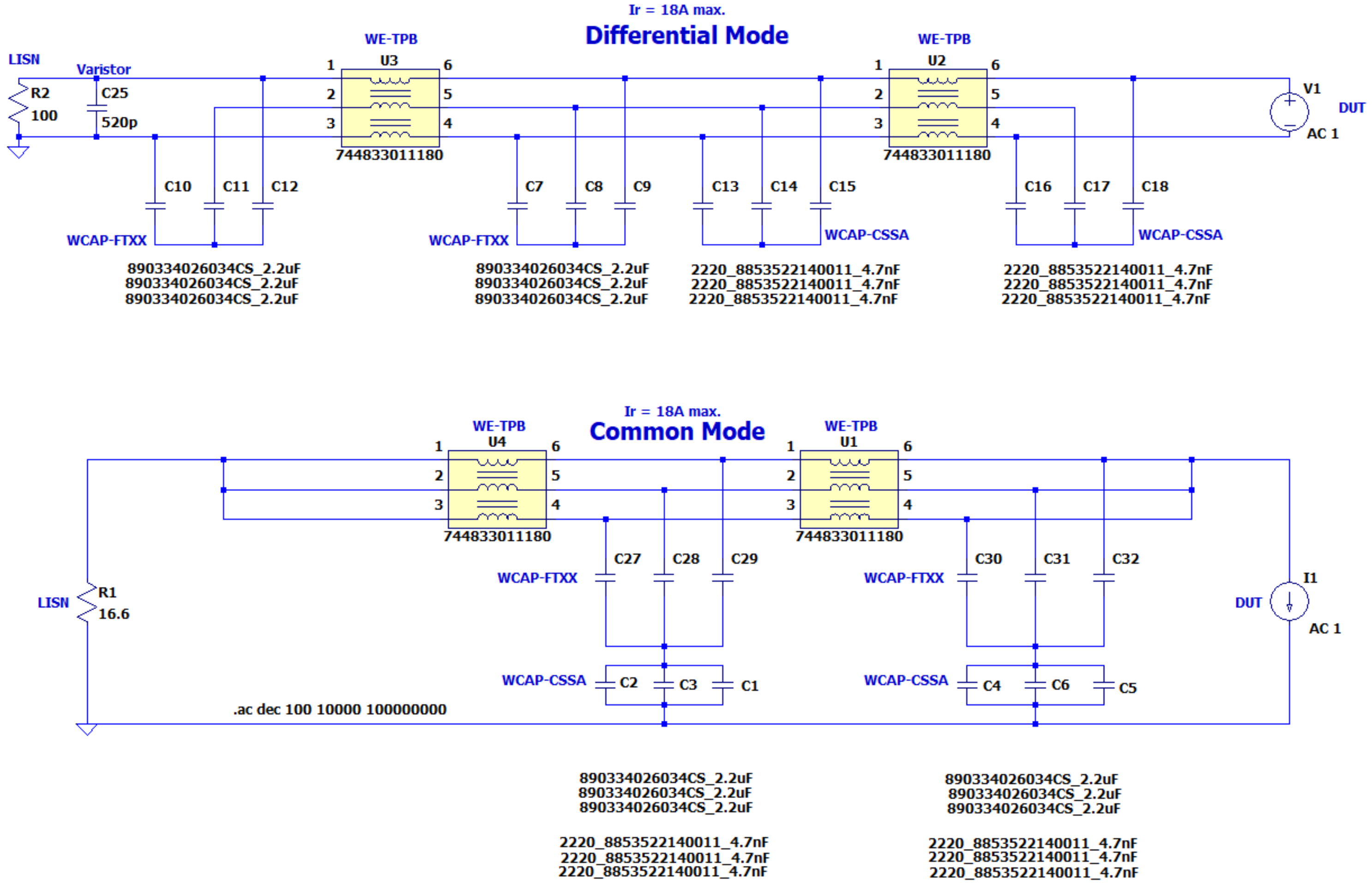
LT Spice Simulation Insertion Loss S21

2-stage filter for 400V / 18A / 11kW / Standard CY



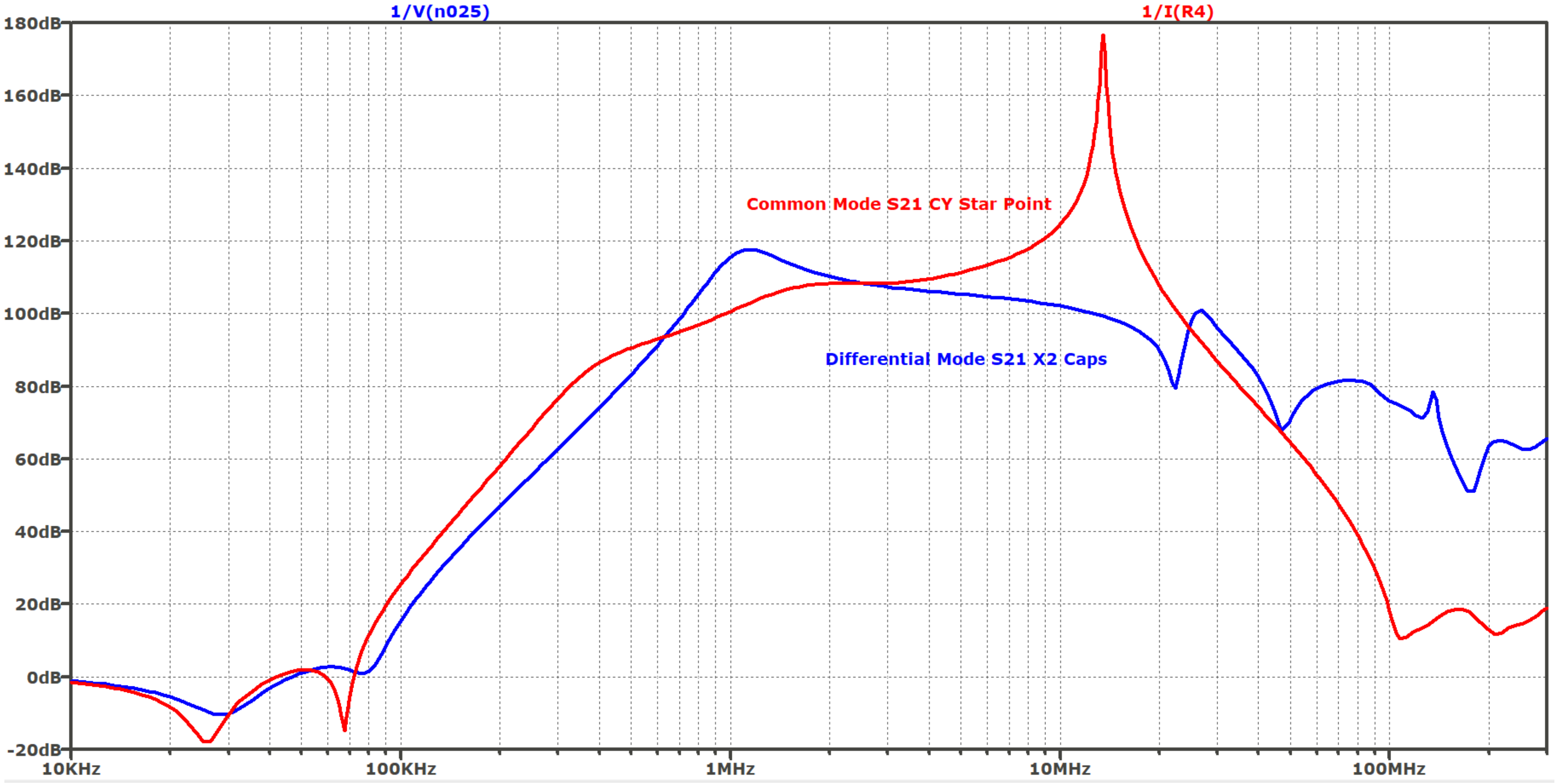
LT Spice Simulation

2-stage filter for 400V / 18A / 11kW → CY - Star Connection



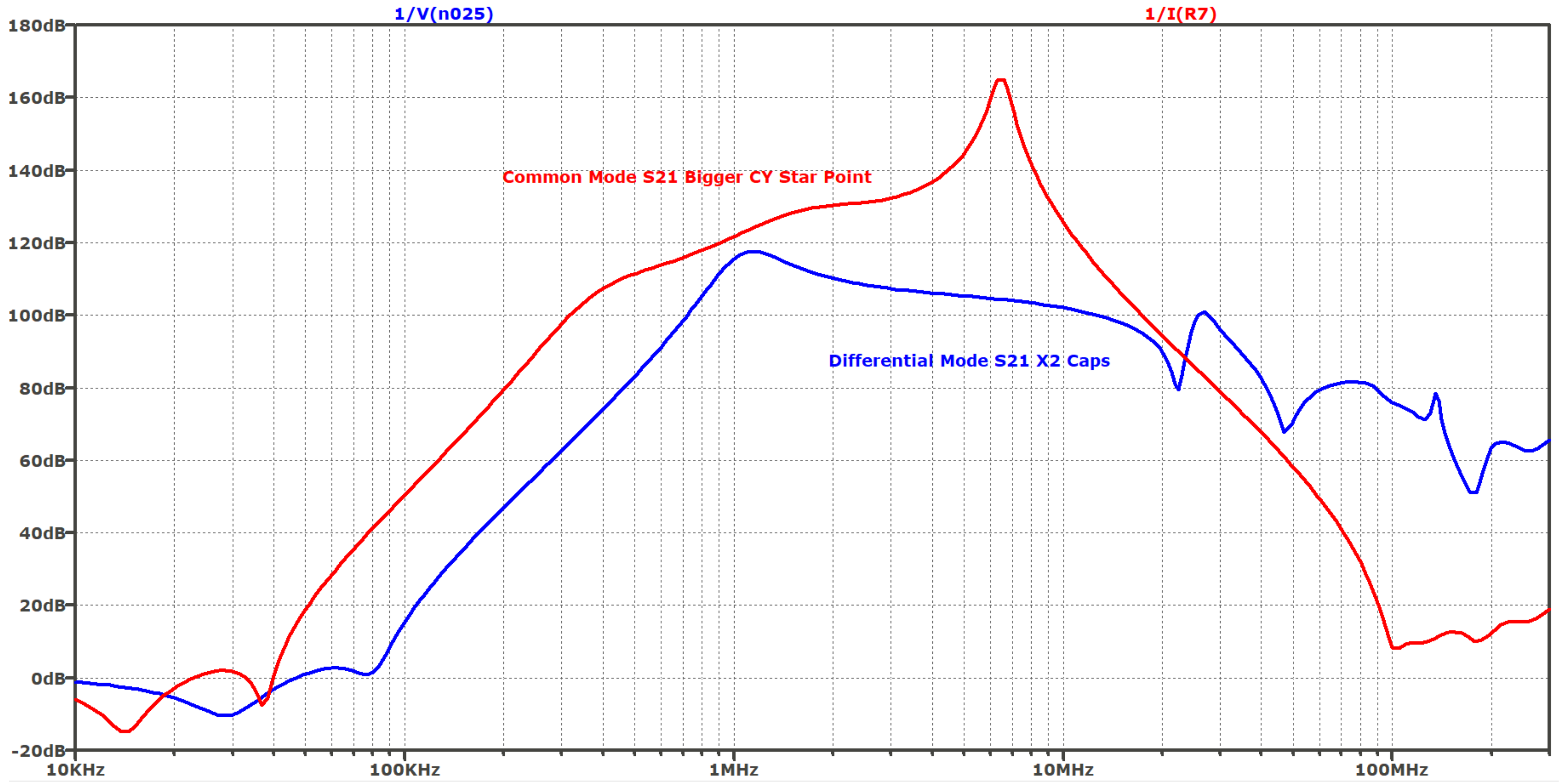
LT Spice Simulation Insertion Loss S21

2-stage filter for 400V / 18A / 11kW → Y-Cap Star Connection 3x4.7nF= 14.1nF



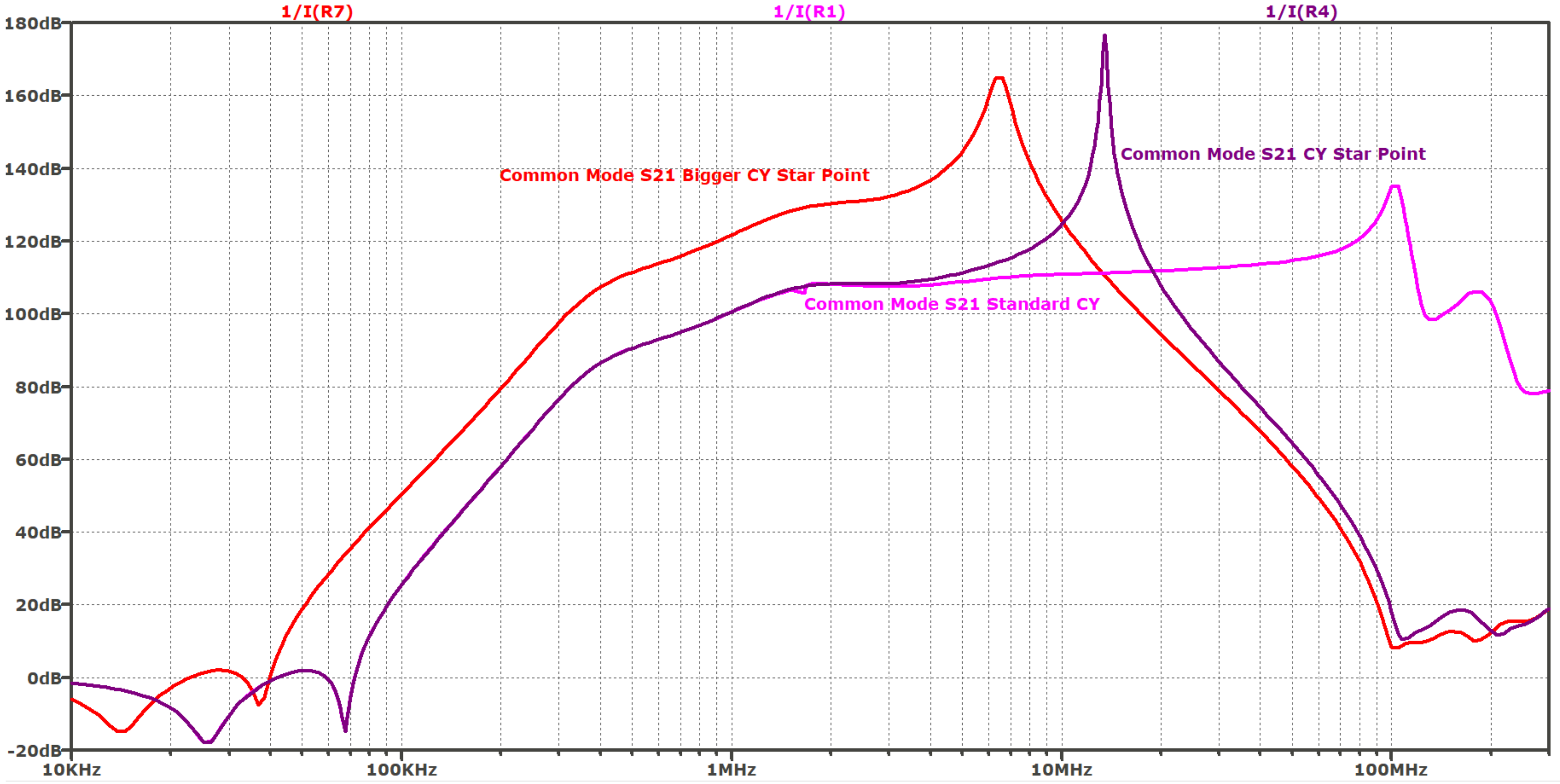
LT Spice Simulation Insertion Loss S21

2-stage filter for 400V / 18A / 11kW → Y-Cap Star Connection **bigger** Y-Cap (47nF)



ST Spice Simulation Insertion Loss S21

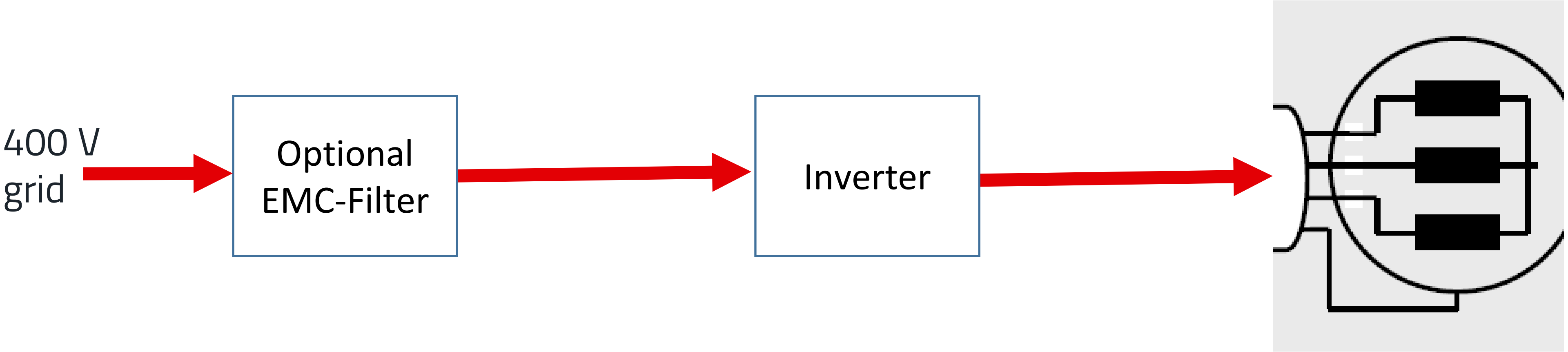
Compare all 3 Common Mode Configurations



MEASUREMENTS IN THE LAB

DUT

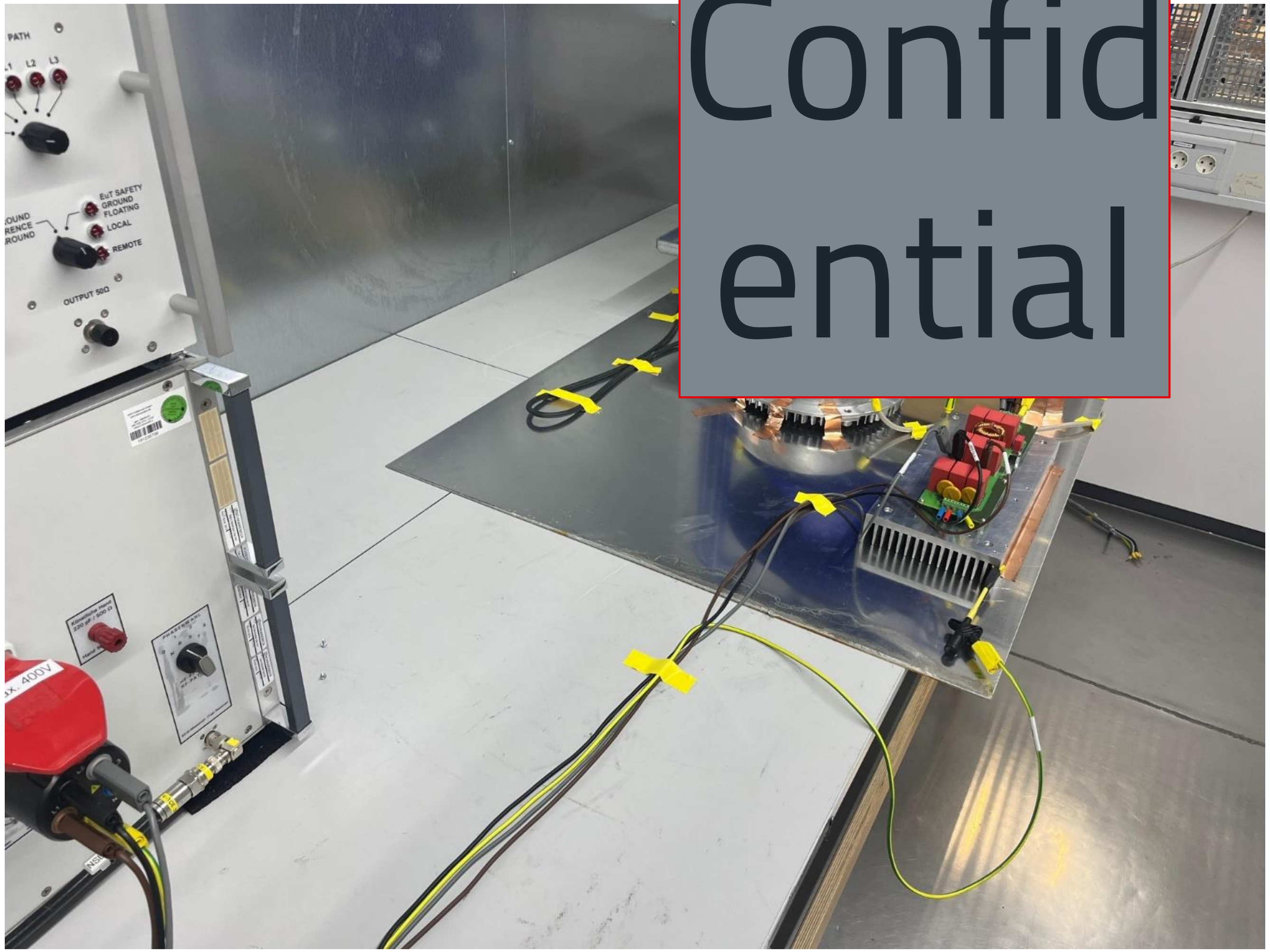
Motor drive system



3 kW; 5 A motor current.

Test Setup

Conducted emission testing



Confidential

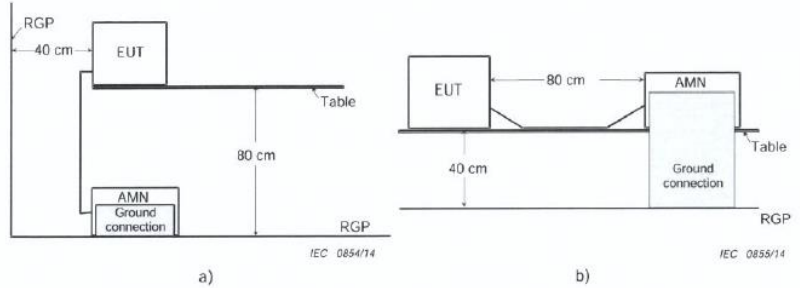
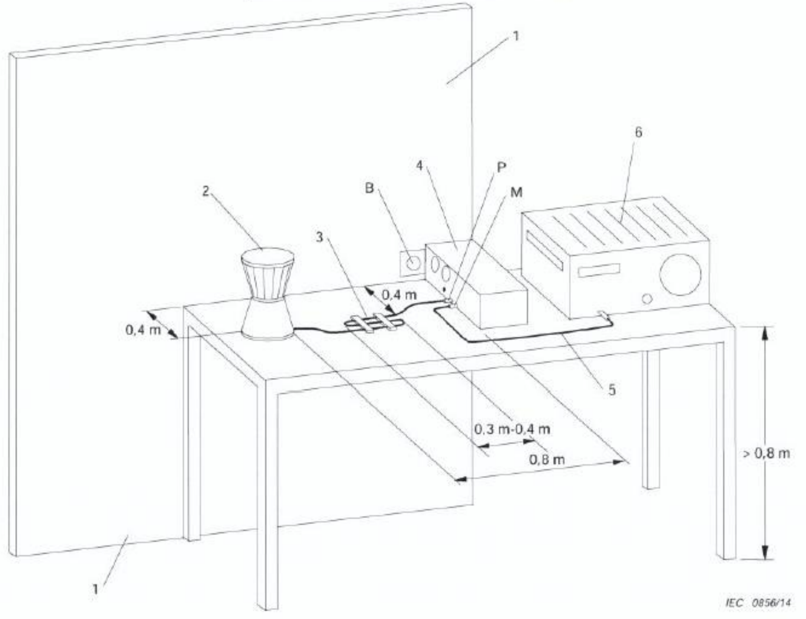
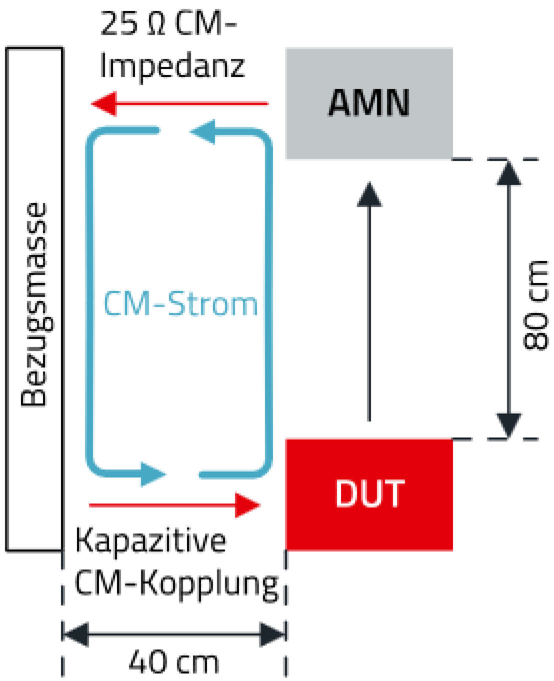


Figure 10 – Arrangement of EUT and AMN at 40 cm distance, with a) vertical RGP and b) horizontal RGP



Test Setup

Conducted emissions testing – basic idea CM-coupling



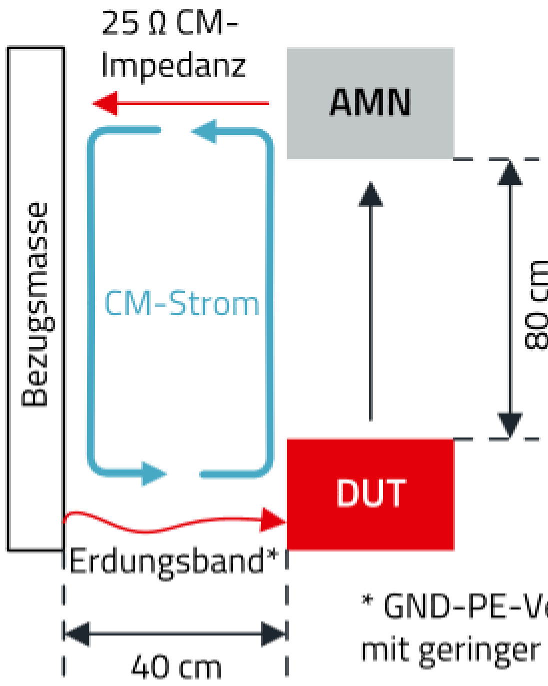
$$C = \frac{\varepsilon_0 \cdot A}{d}$$

$$= \frac{\varepsilon_0 \cdot 1\,m^2}{0{,}4\,m} = 22\,pF$$

$$X_C = \frac{1}{\omega \cdot C} = \frac{1}{2 \cdot \pi \cdot f \cdot C}$$

$$= \frac{1}{2 \cdot \pi \cdot 1\,MHz \cdot 22\,pF} = 7{,}2\,k\Omega$$

C = CM-Kapazität
A = Fläche Plattenkondensator
d = Abstand der Platten;
40 cm durch genormten Aufbau
f = betrachtete Frequenz

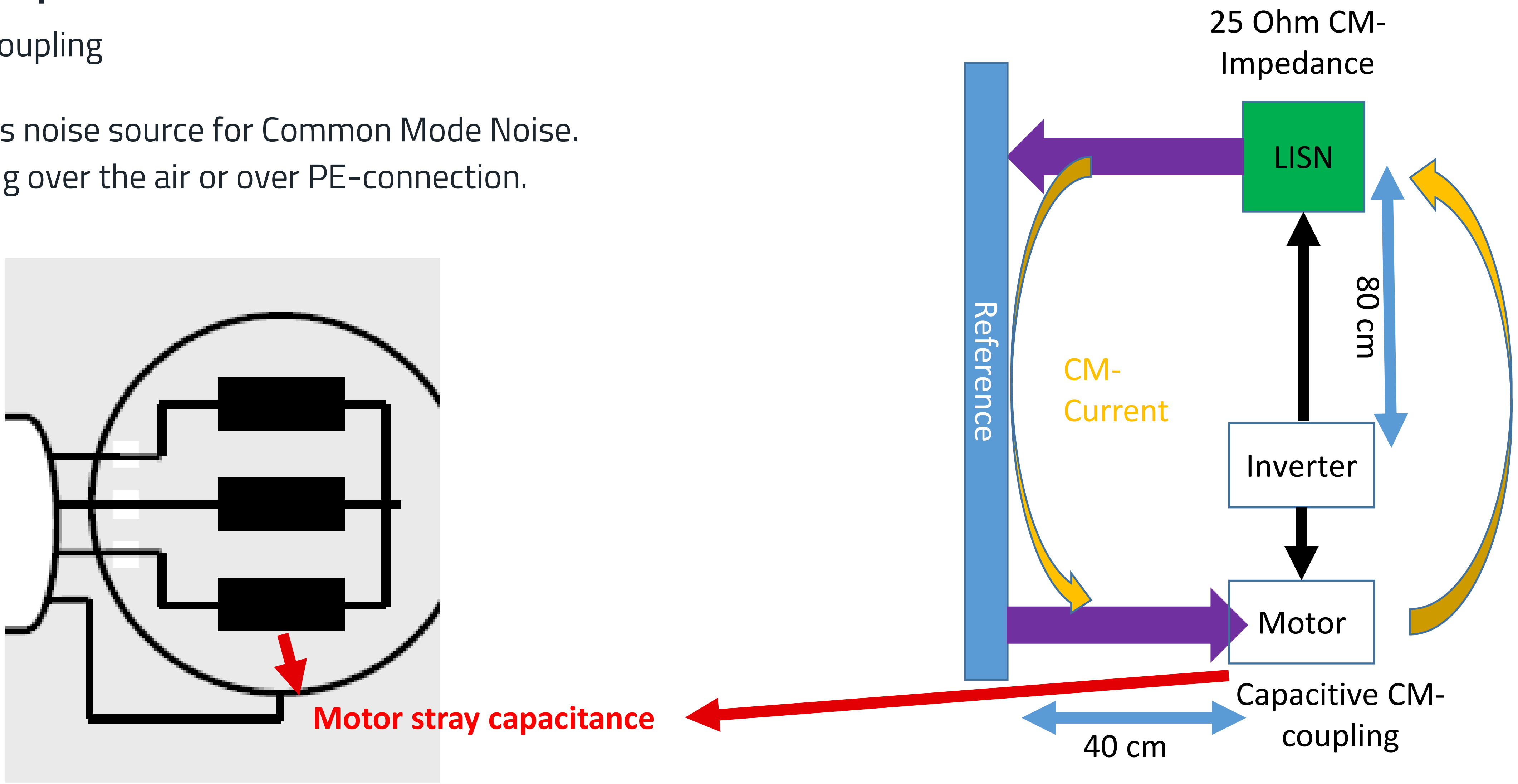


* GND-PE-Verbindung mit geringer Impedanz

Test setup

Detailed coupling

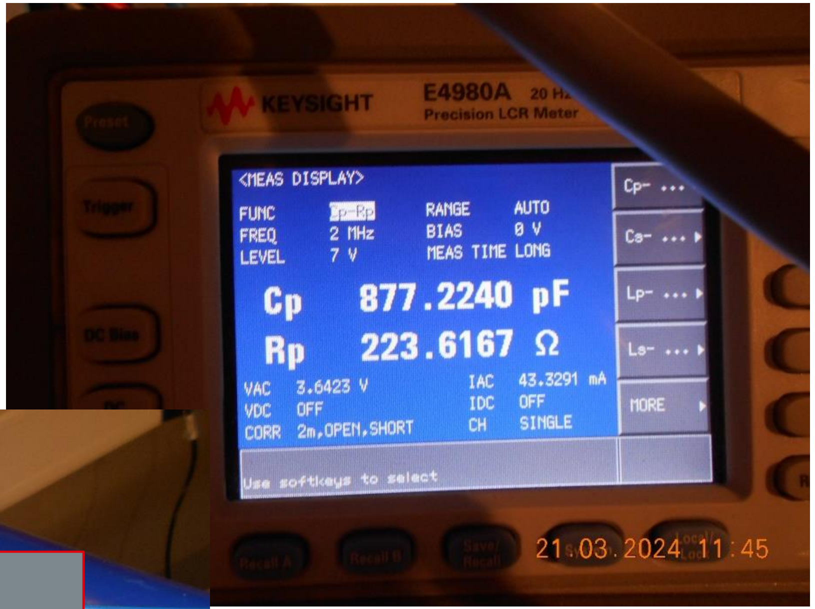
- Motor is noise source for Common Mode Noise.
- Coupling over the air or over PE-connection.



Motor stray capacitance

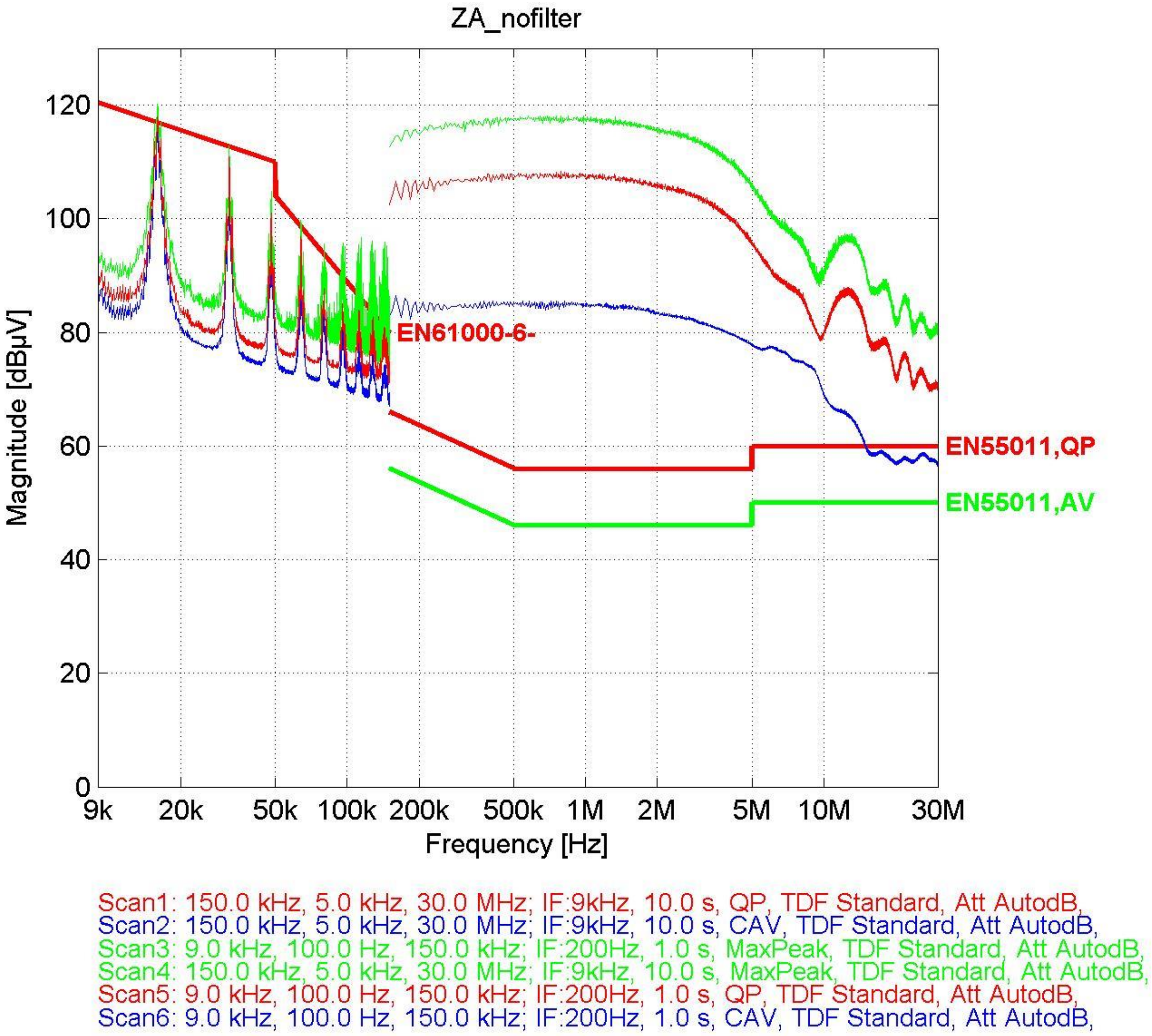
Measurement with LCR-meter

- Motor stray capacitance: 877 pF @ 2 MHz.
- Winding to chassis.



Conducted emissions

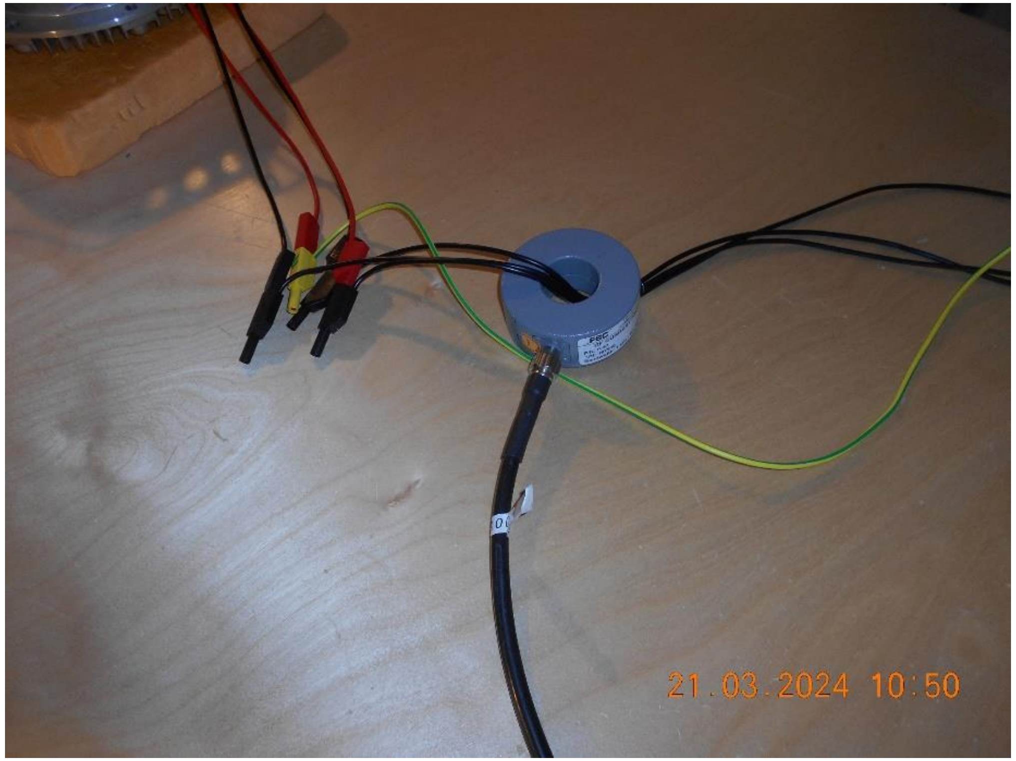
No filter



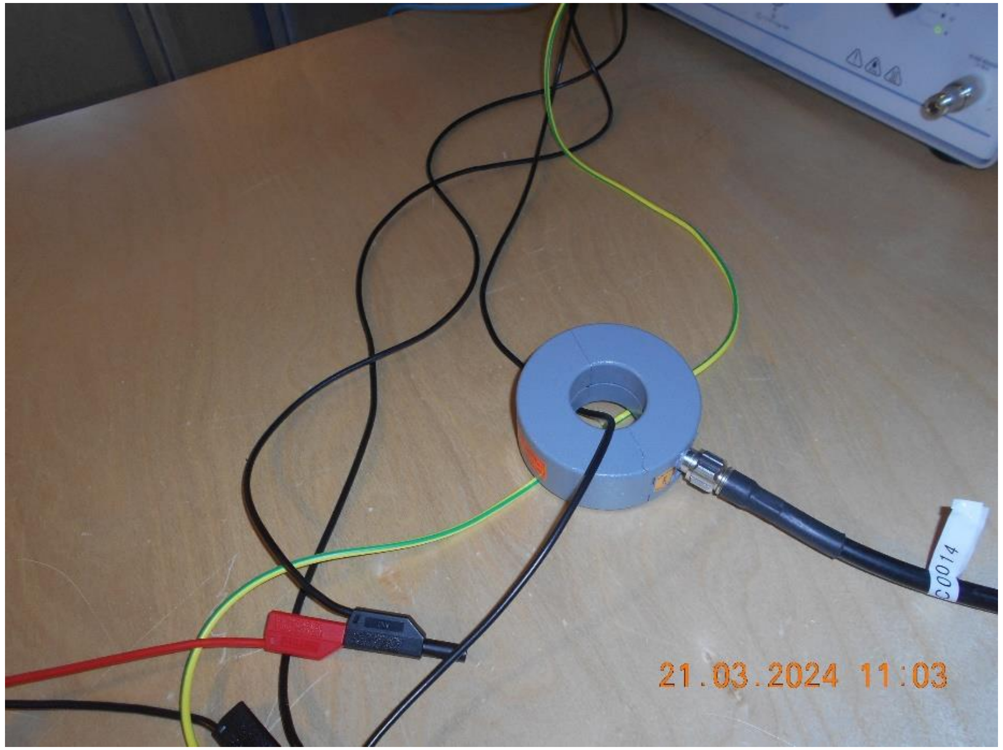
Common Mode vs Differential Mode

Current probe setup

- Common mode on all 3 lines:



- Differential mode + common mode on single line



Common Mode vs Differential Mode

Current probe setup

- Current probe:
  - Linear performance starting at 10 kHz.
  - Note: LISN is linear at 50 Ohms starting at MHz range!
  - LISN linear starting at 1 MHz.

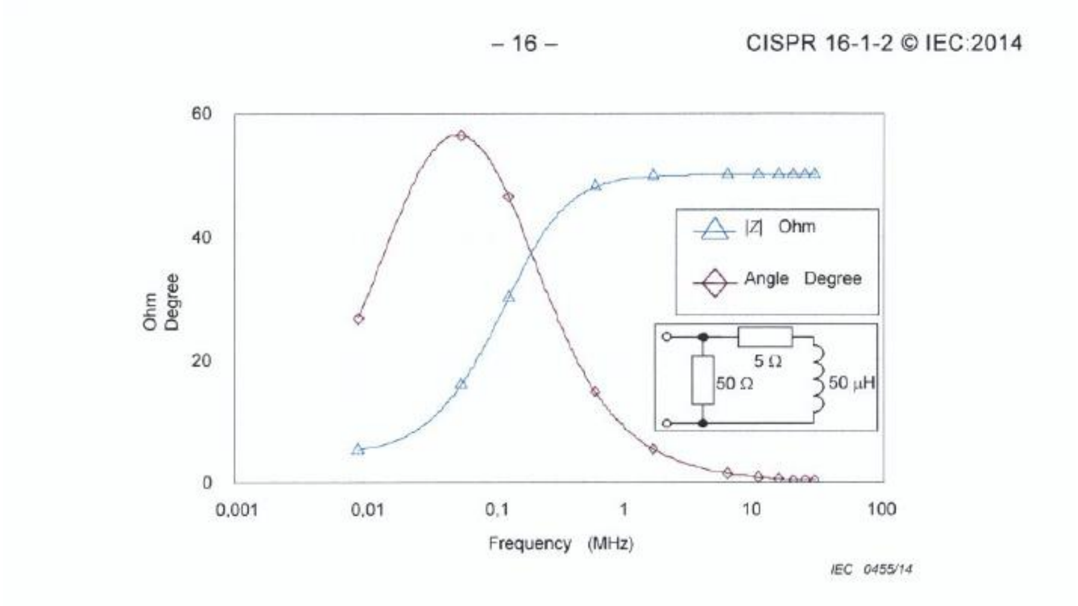
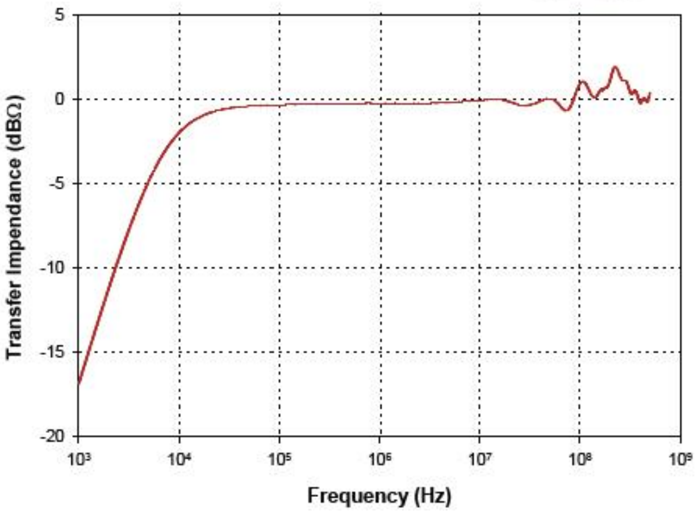


Figure 1 – Impedance (magnitude and phase) of the V-network for Band A (see 4.3, the relevant frequency range is from 9 kHz to 150 kHz)



Specifications

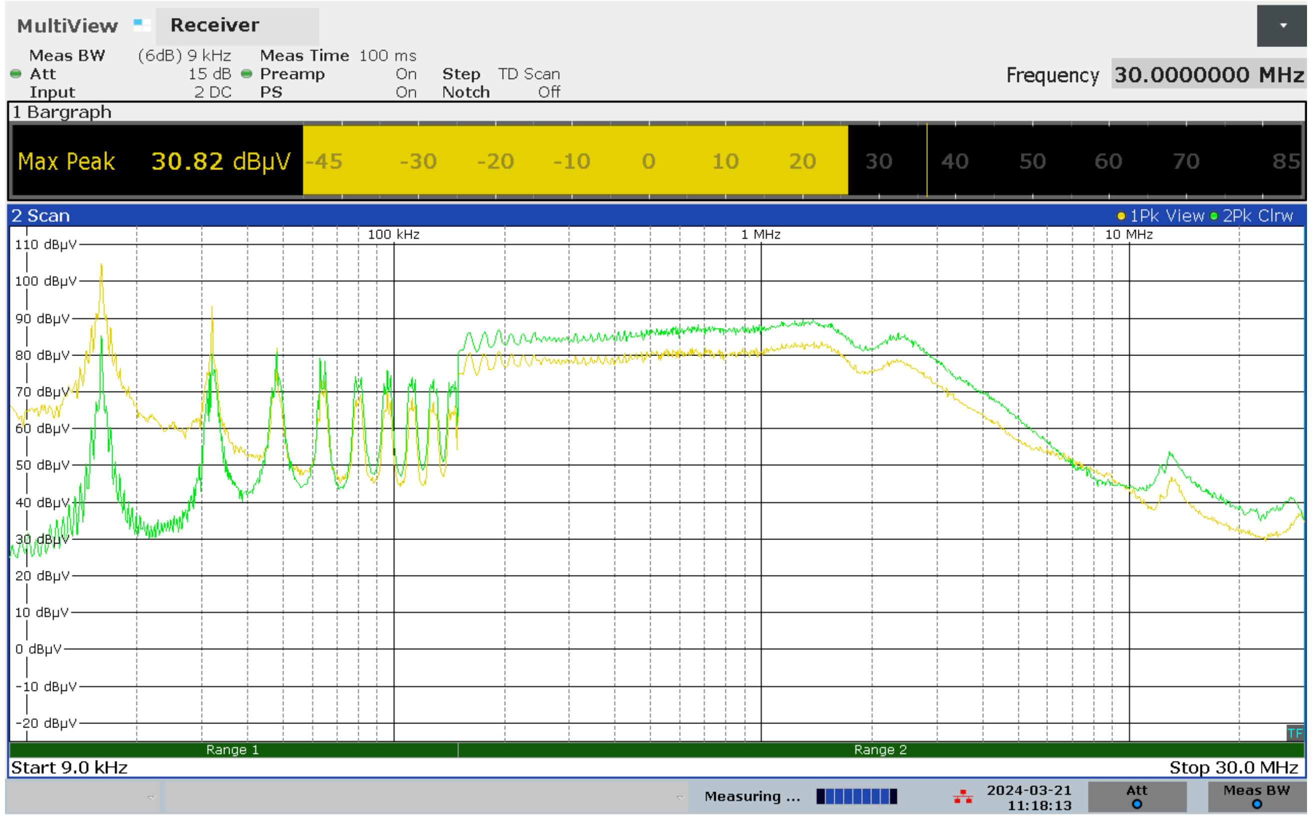
Frequency:	1 kHz – 500 MHz
Internal diameter:	48 mm
External diameter:	98 mm
Height:	38 mm
$Z_t\Omega$[1]:	1
dBΩ[1]:	0
Connector:	Type-N
DC to 400 Hz:	200 amperes
RF(CW):	2 amperes Peak Pulse
Peak Pulse Current[2]:	100 amperes

1: Probe calibrated with 50 Ω + j0Ω Load Impedance.
2: Depends upon the pulse width and pulse rep. rate.

Common Mode vs Differential Mode

DUT with PE / Earth connection

- Green = common mode current on all 3 lines
- Yellow = differential mode current + common mode current on a single line



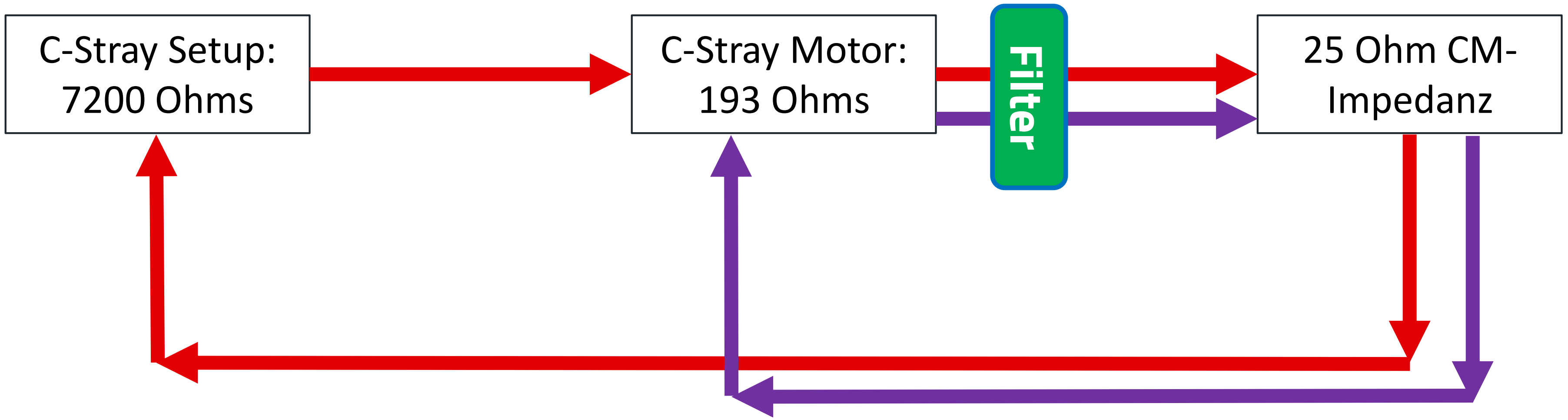
11:18:13 AM 03/21/2024

DM noise dominant below 50 kHz!

Filter Calculation

Common mode loop

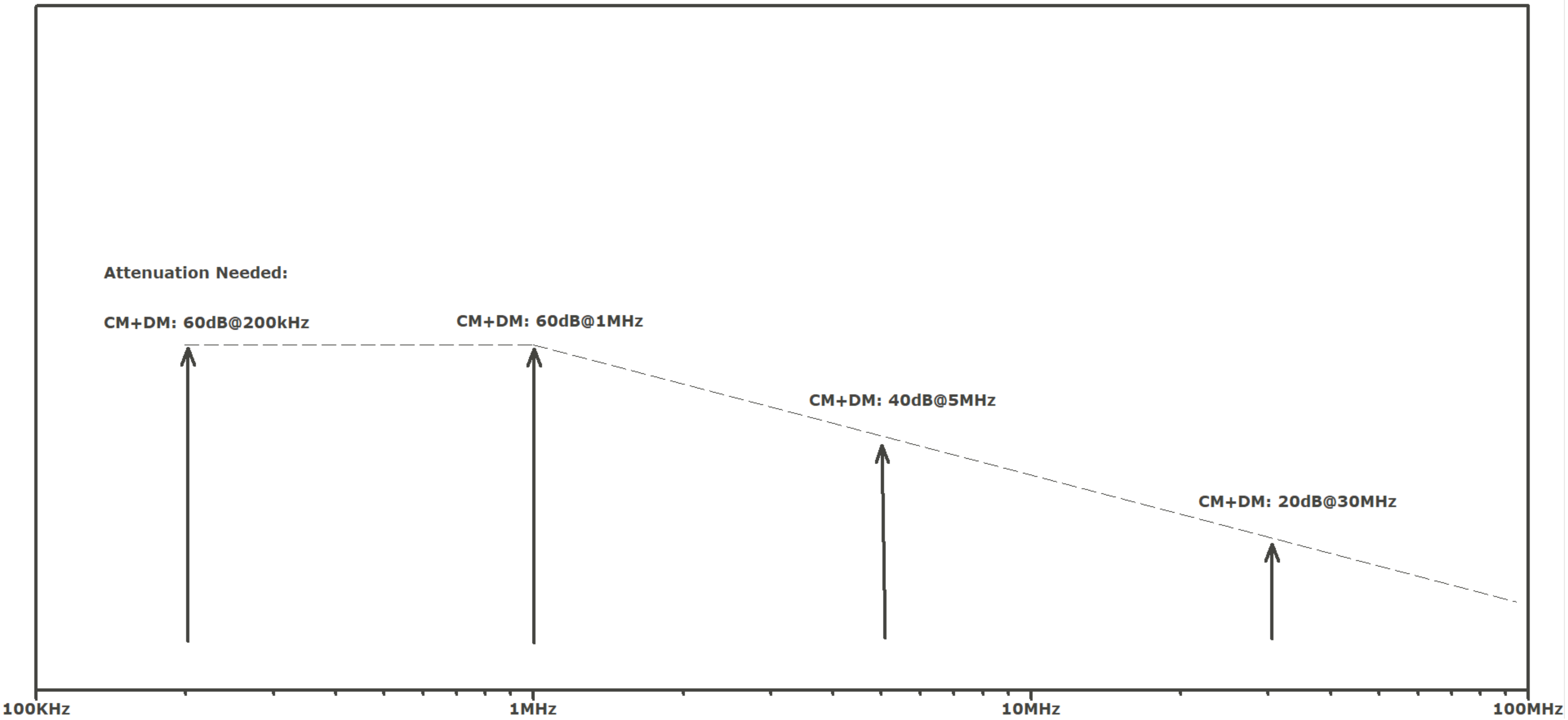
- Attenuation earthed 60 dB required -> 1000 times reduction of the noise current.
- 218 Ohms loop impedance -> 218 000 Ohms Filter impedance if only CMC is used…



- Complexe filter calculation or simulation possible, when impedance system is known.

Requiered Filter Attenuation

DM & CM

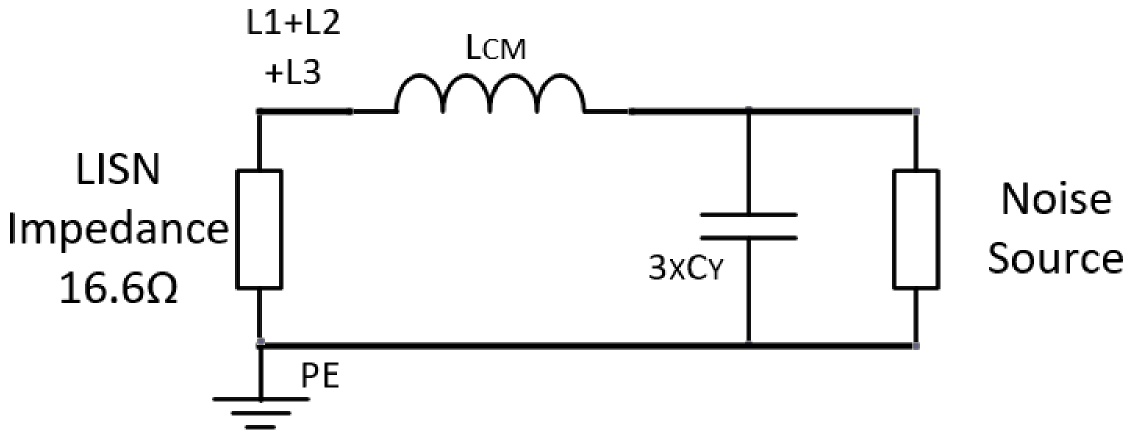


MATH

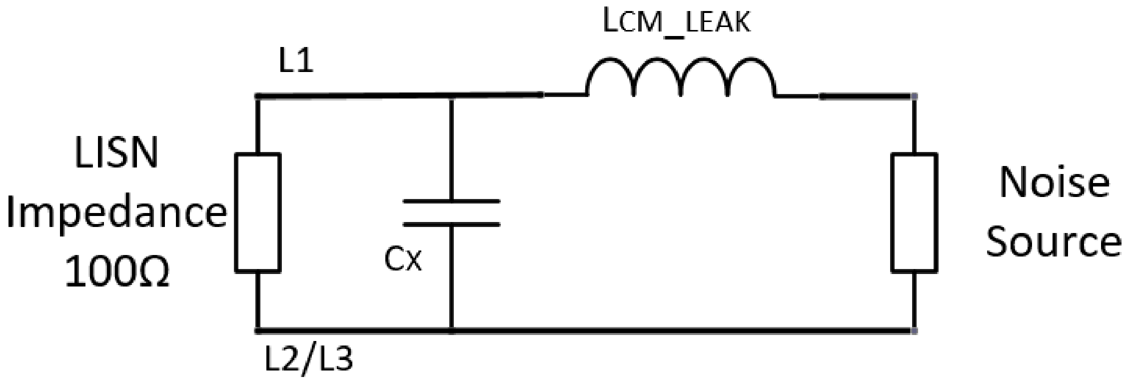
CM & DM Filter Equivalent

Effective LISN impedance and component arrangement

- CM



- DM

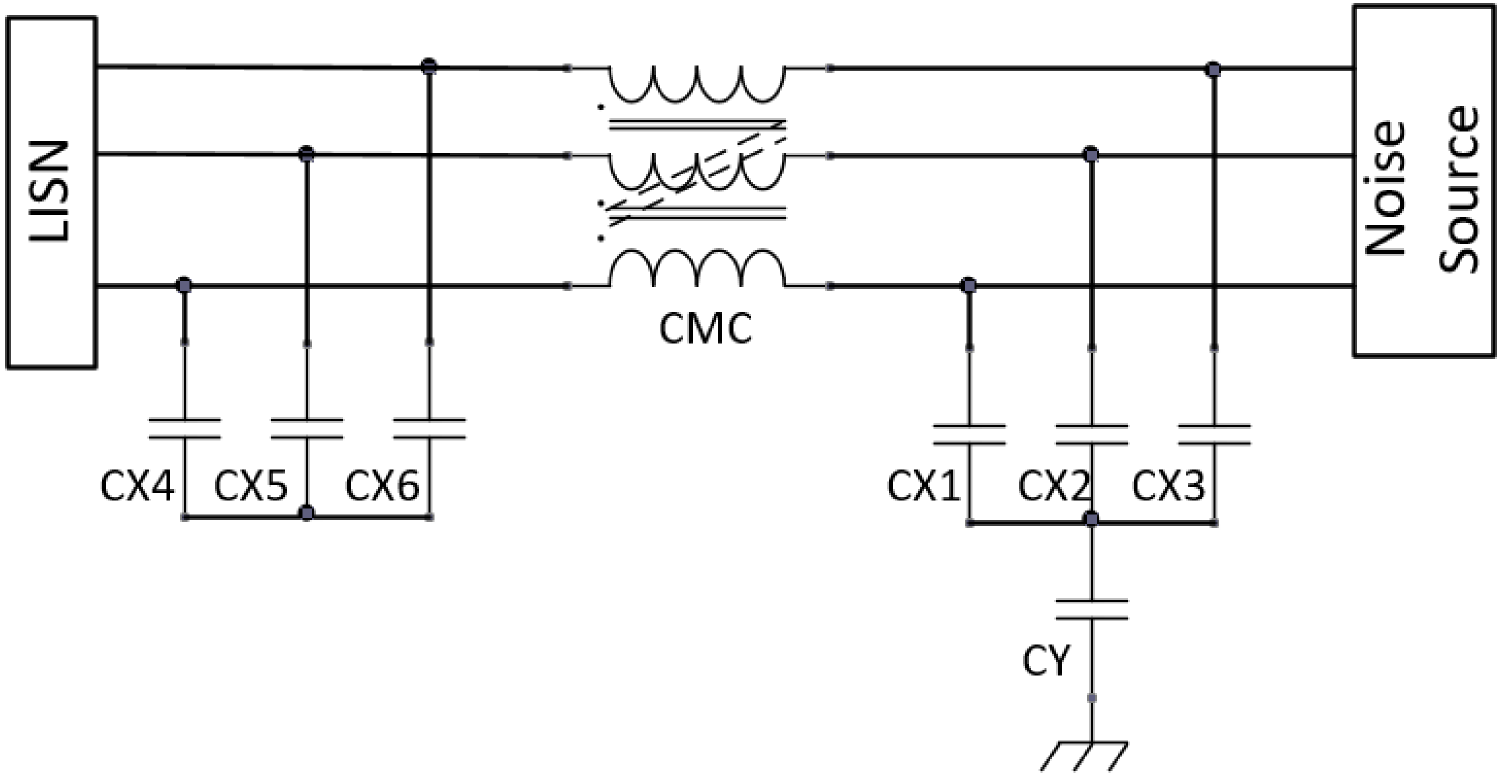


CM & DM Filter Equivalent

Effective Cx and Cy in 3 phase systems

- Cx between each phase:
- $Cx_{effective} = \left(\frac{1}{CX1} + \frac{1}{CX2}\right)^{-1}$

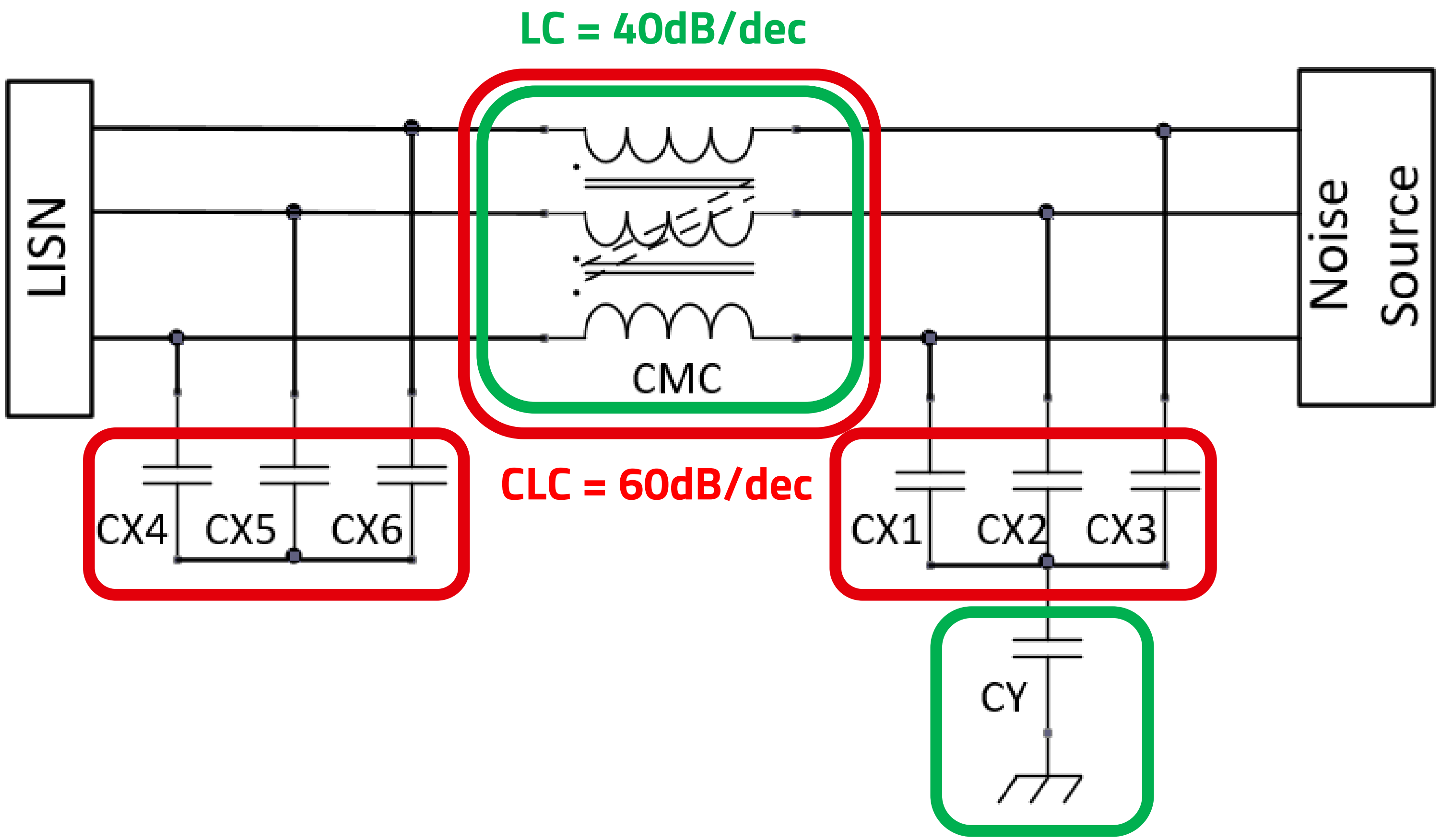
- Cy betwenn all 3 phases and PE:
- $Cy_{effective} = (\frac{1}{CX1+CX2+CX3} + \frac{1}{CY})^{-1}$



Chosen Filter Structure for DUT 150kHz to 30MHz

„CLC“ for **DM** and „LC“ for **CM**

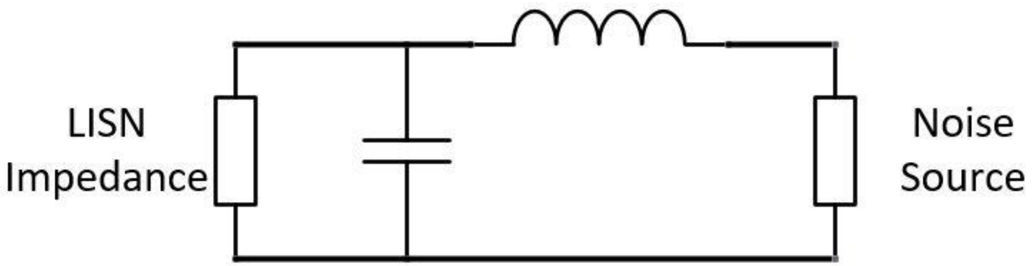
- **DM** filter provides 60dB/dec
  - Leakage of CMC + X-Caps
- **CM** filter provides 40dB/dec
  - CMC main inductance + Y-Cap

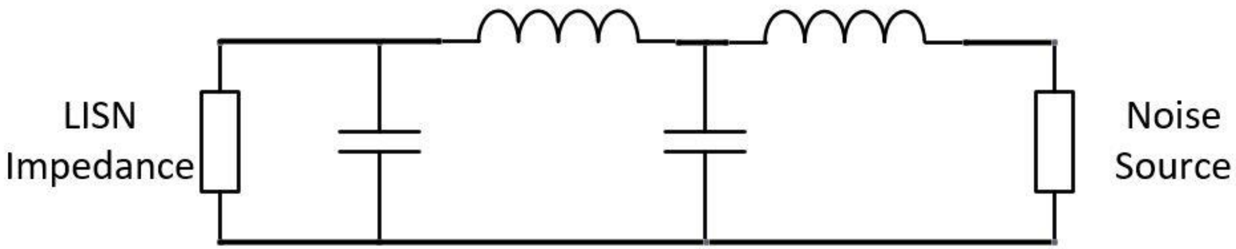


Corner Frequency for desired Attenuation at fsw = A_fsw

Valid for both: CM & DM

1-Stage LC	2-Stage LC
$A_{\mathrm{fsw}} = \log\left(\frac{f_{\mathrm{sw}}}{f_{\mathrm{co}}}\right) \cdot 40dB$	$A_{\mathrm{fsw}} = \log\left(\frac{f_{\mathrm{sw}}}{f_{\mathrm{co}}}\right) \cdot 80dB$
$f_{co} = \frac{f_{sw}}{10^{\frac{A_{fsw(dB)}}{40dB}}}$	$f_{co} = \frac{f_{sw}}{10^{\frac{A_{fsw(dB)}}{80}dB}}$





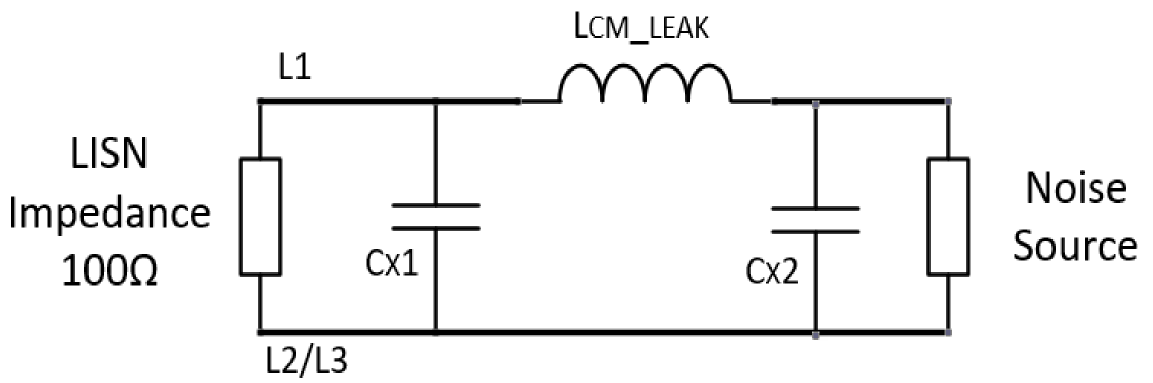
Corner Frequency for desired Attenuation at fsw = A_fsw

DM PI filter

1-Stage CLC = „PI“

$$A_{\mathrm{fsw}} = \log\left(\frac{f_{\mathrm{sw}}}{f_{\mathrm{co}}}\right) \cdot 60dB$$

$$f_{co} = \frac{f_{sw}}{10^{\frac{A_{fsw(dB)}}{60dB}}}$$



Additional Math for „CLC – PI“

$$f_{co} = \frac{1}{2\pi\sqrt{L_{CMleak} \cdot C_{XG}}}$$

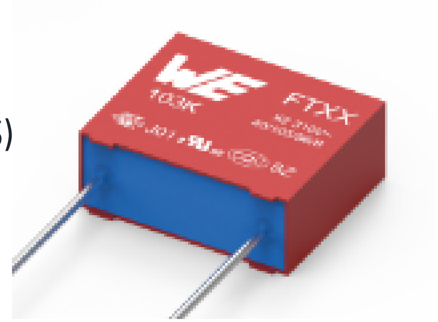
$$C_{XG} = \frac{Cx1 \cdot Cx2}{Cx1 + Cx2}$$

CLC (DM) & LC (CM) - Stage Calculation (worst case without real CM couping)

Desired damping for CM & DM = 60dB @ (200kHz)

1. „CLC PI“ = 60dB/Dec (DM) and „LC“ = 40dB/Dec (CM)
2. DM filter corner frequency: fc_dm = **20kHz** & CM filter corner frequency: fc_cm = **6.3kHz**
3. Define Y-caps → 47nF(star connected) → $Cy_{effective} = (\frac{1}{CX1+CX2+CX3} + \frac{1}{CY})^{-1} = \mathbf{47nF}$
4. Define L_cm for fc_cm = 6.3kHz → $L_{cm} = \frac{1}{(2\pi fc)^2 C_y} = \frac{1}{(2\pi \cdot 6.3kHz)^2 \cdot 47nF} = 13.6mH$ → **12mH** chosen (744833120060)

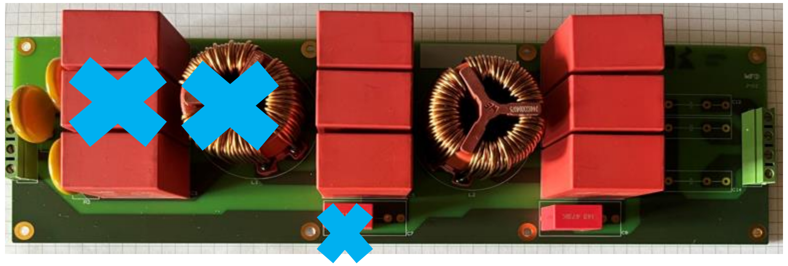
5. $Actual\ f_{cm} = \frac{1}{2\pi\sqrt{L_{cm}Cy}} = \frac{1}{2\pi\sqrt{12mH \cdot 47nF}} = 6.7kHz \ \longrightarrow A_{fsw_{cm}} = log\left(\frac{200kHz}{6.7kHz}\right) \cdot 40dB = \mathbf{59dB}$
6. Calc. L_dm → XL = 54Ω@100kHz → $L_{dm} = \frac{XL}{2\pi f} = \frac{54\Omega}{2\pi \cdot 100kHz} = \mathbf{86\mu H}$ (use REDEXPERT for help)

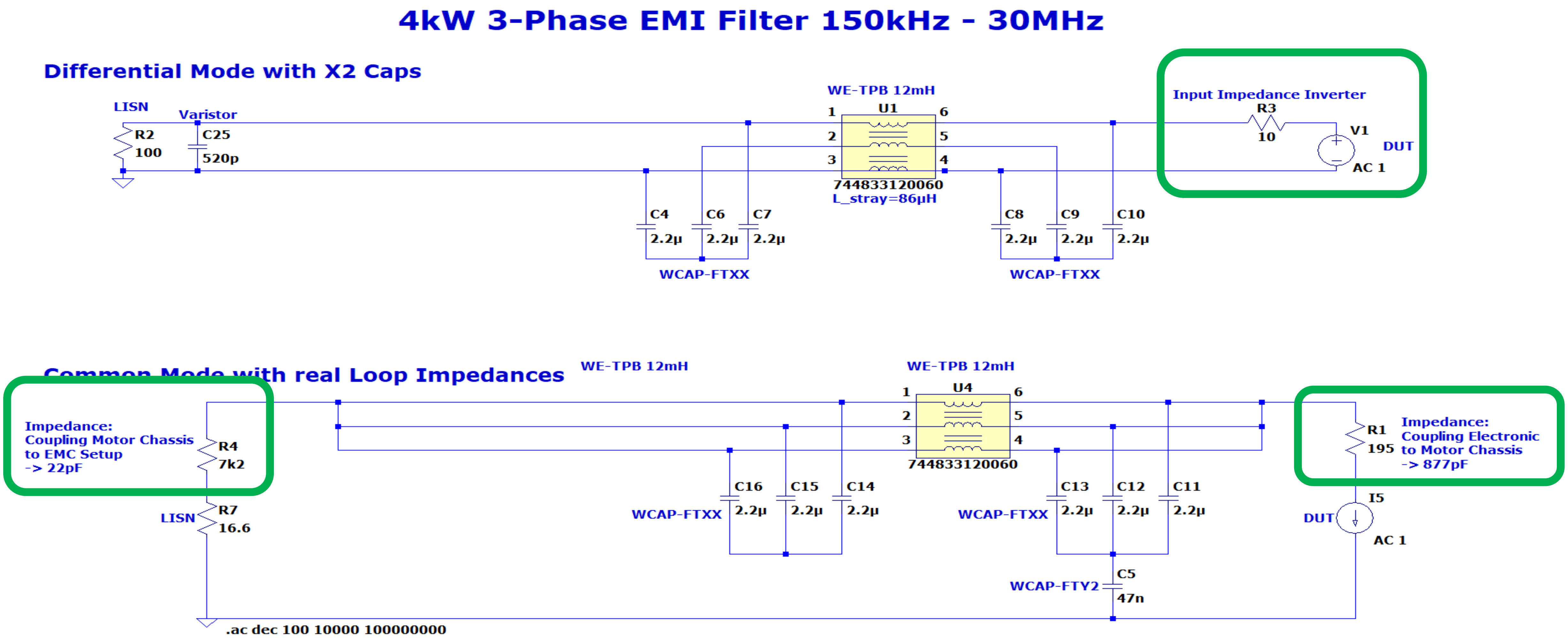


7. Define Cx → $C_x = \frac{1}{(2\pi fc)^2 L_{dm}} = \frac{1}{(2\pi \cdot 20kHz)^2 \cdot 86\mu H} = 737nF$ → 2,2µF chosen → $C_{XG} = \frac{Cx1 \cdot Cx2}{Cx1 + Cx2} = \mathbf{1,18\mu F}$ (6x890334027030CS)
8. $Actual\ f_{dm} = \frac{1}{2\pi\sqrt{L_{dm}Cx}} = \frac{1}{2\pi\sqrt{86\mu H \cdot 1.18\mu F}} = 15.8kHz \ \longrightarrow A_{fsw_{dm}} = log\left(\frac{200kHz}{15.8kHz}\right) \cdot 60dB = \mathbf{66dB}$

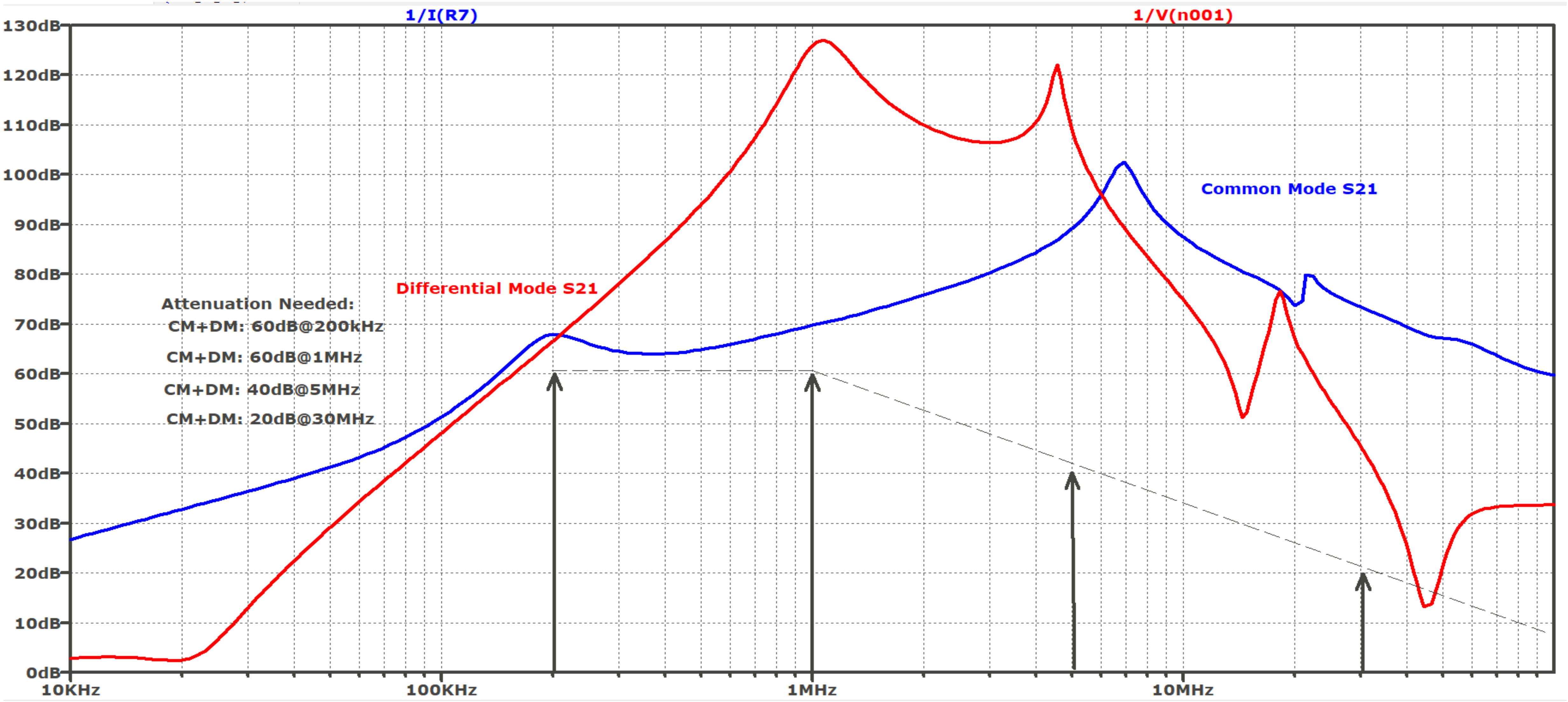
SIMULATION OF THE CALCULATED CLC FILTER

LT Spice Schematic CLC

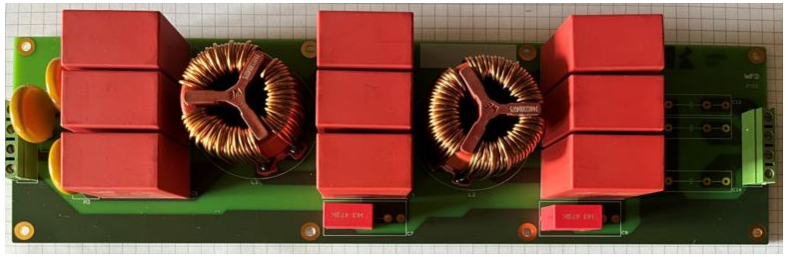




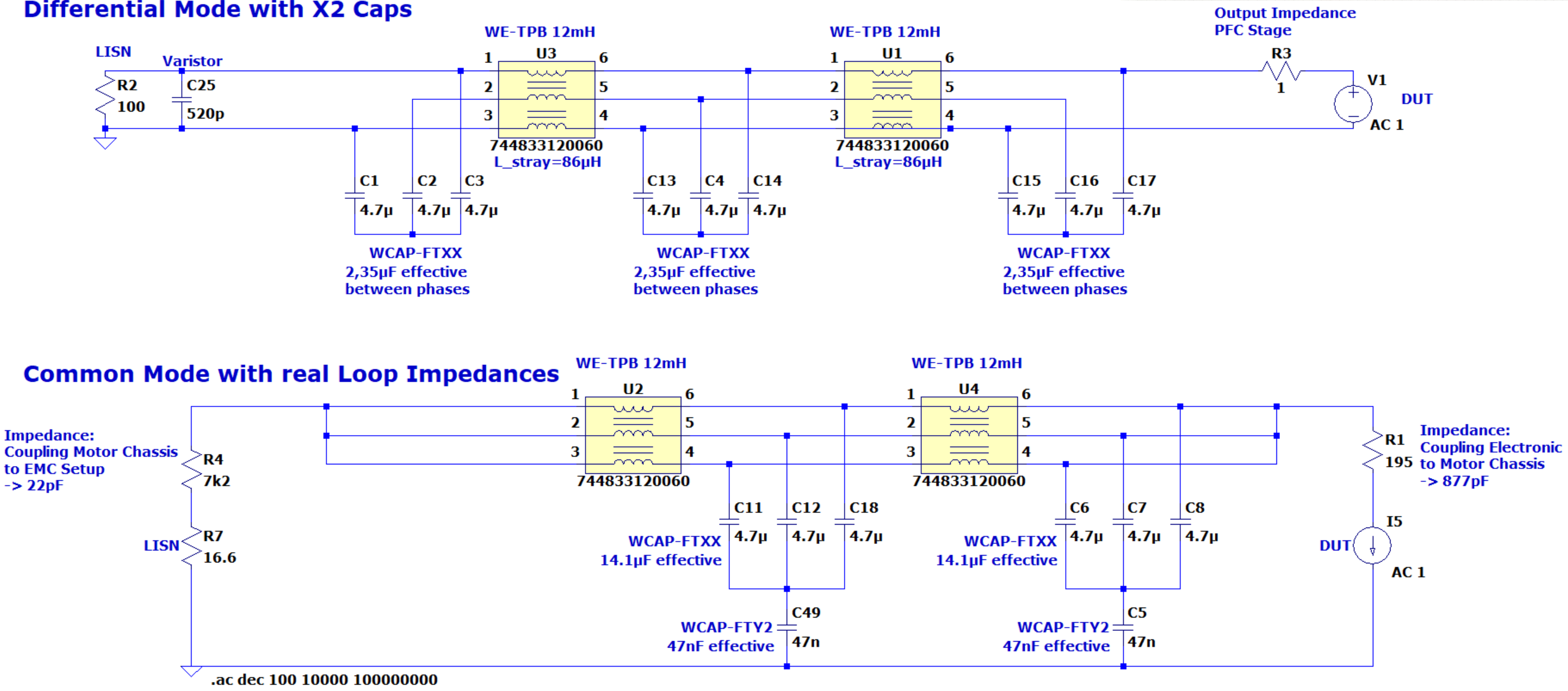
LT Spice Simulation CLC



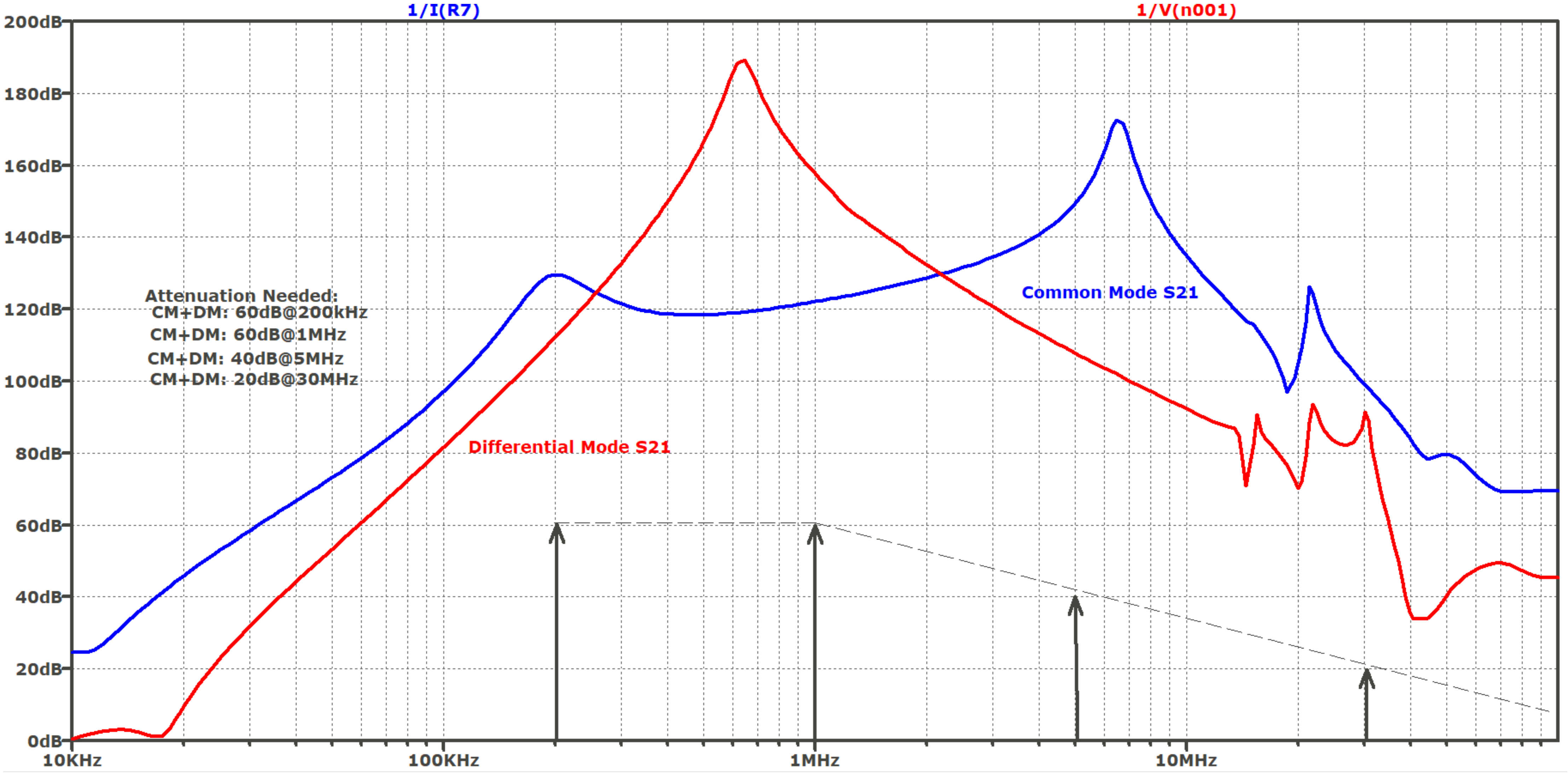
LT Spice Schematic CLCLC



4kW 3-Phase EMI Filter 150kHz - 30MHz



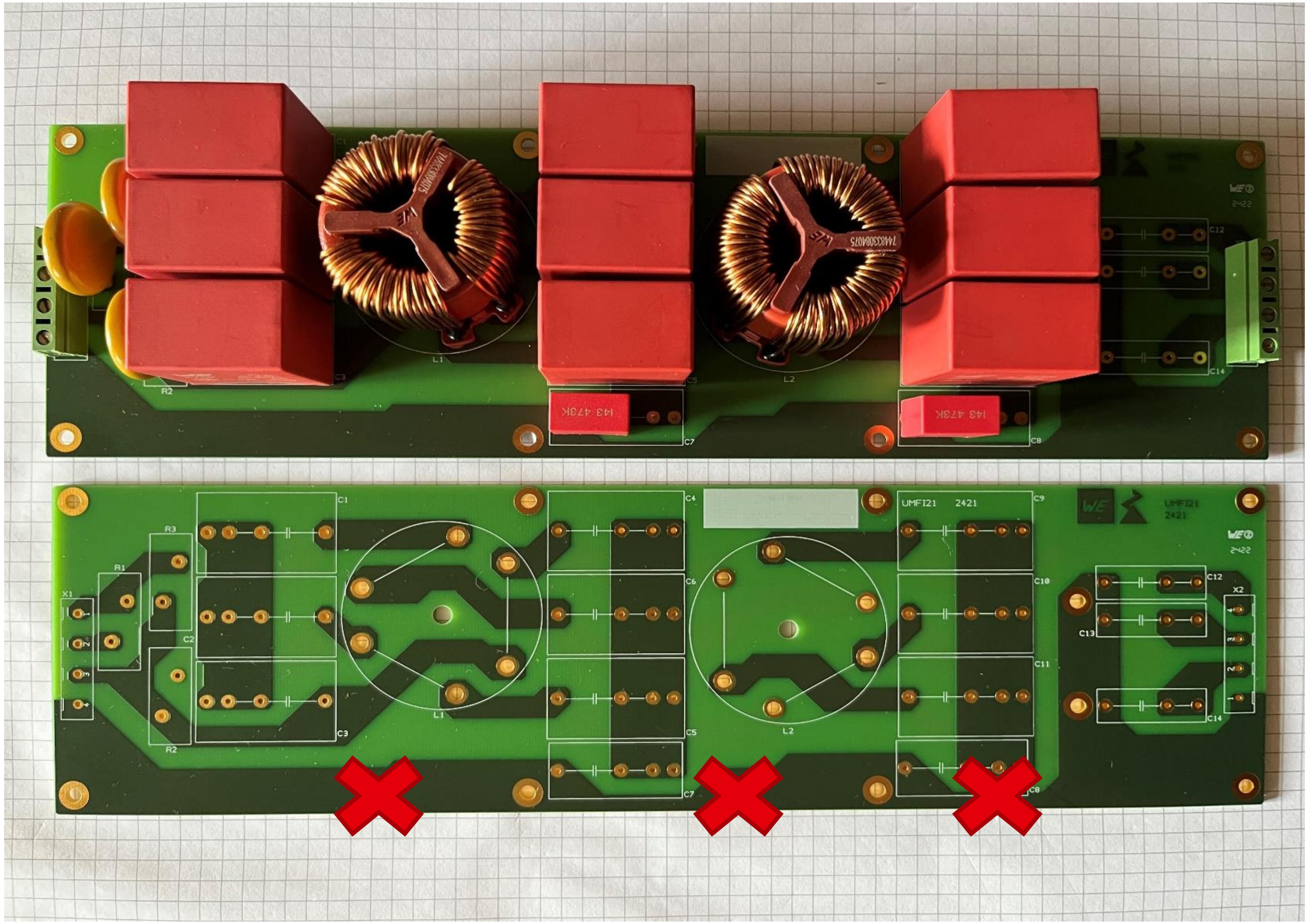
LT Spice Simulation CLCLC



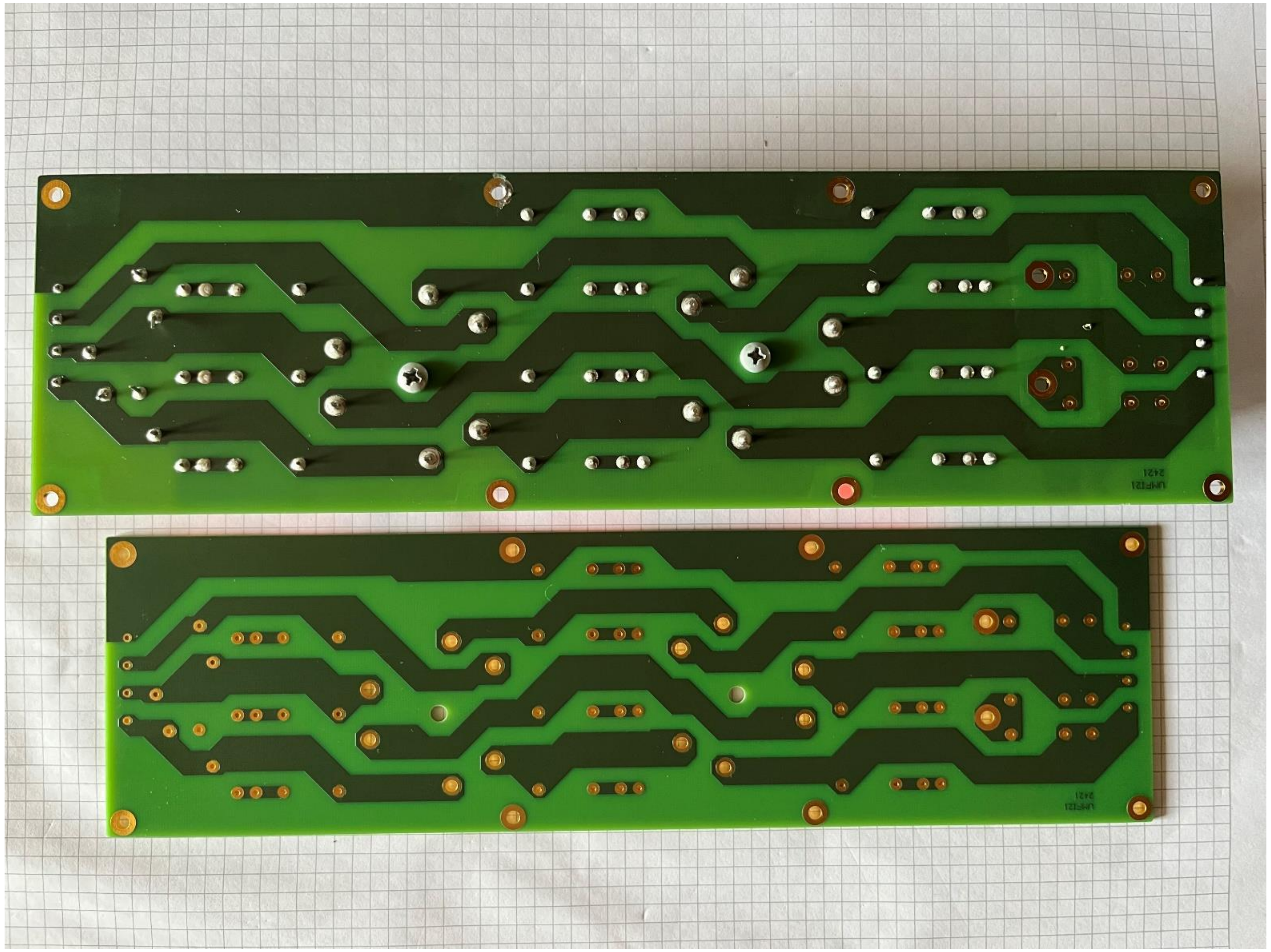
FILTER PCB

Example 2-Stage Design TOP view

What can be improved?



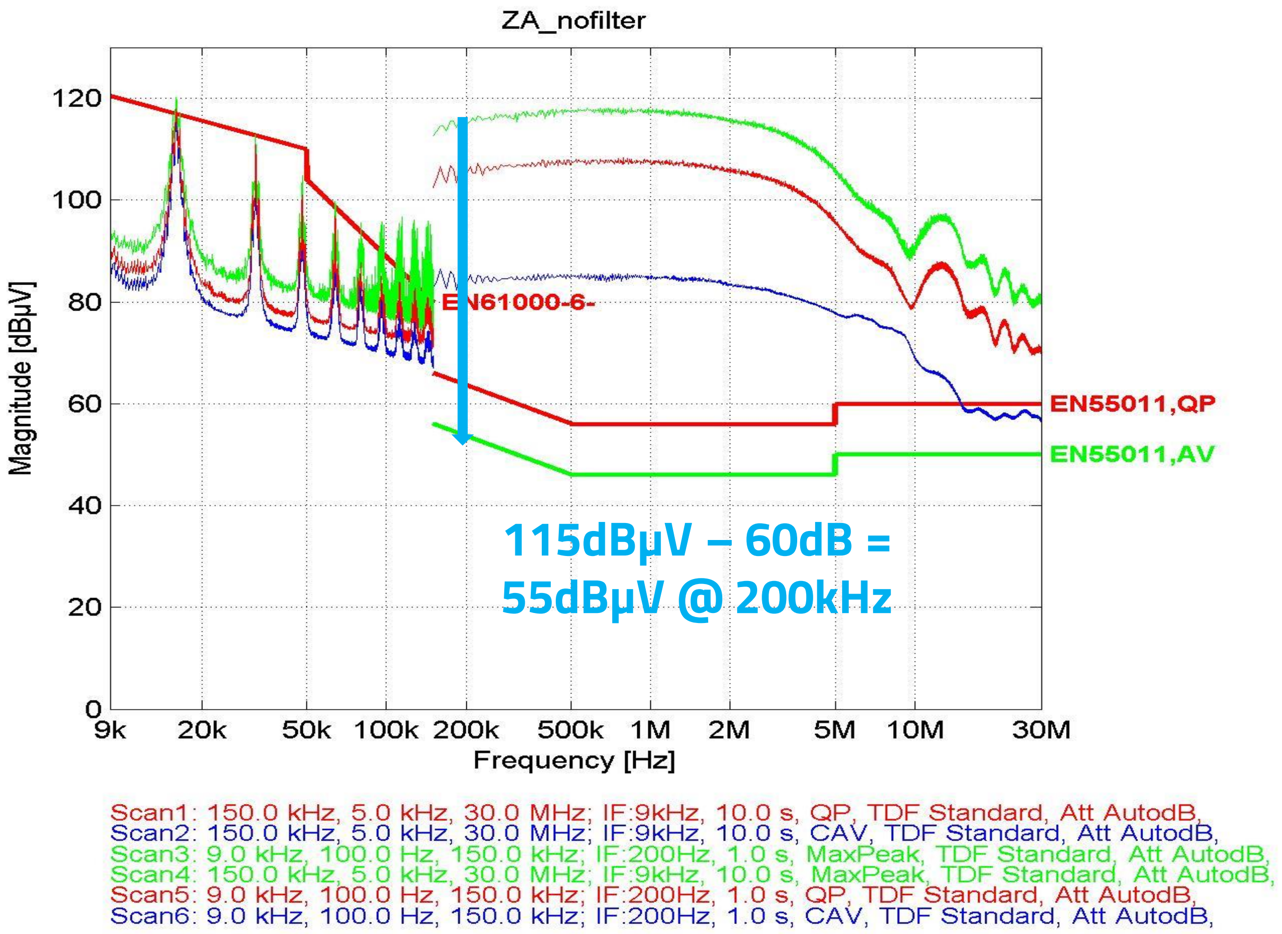
Example 2-Stage Design BOT view



NEW MEASUREMENTS WITH CALCULATED & SIMULATED FILTER

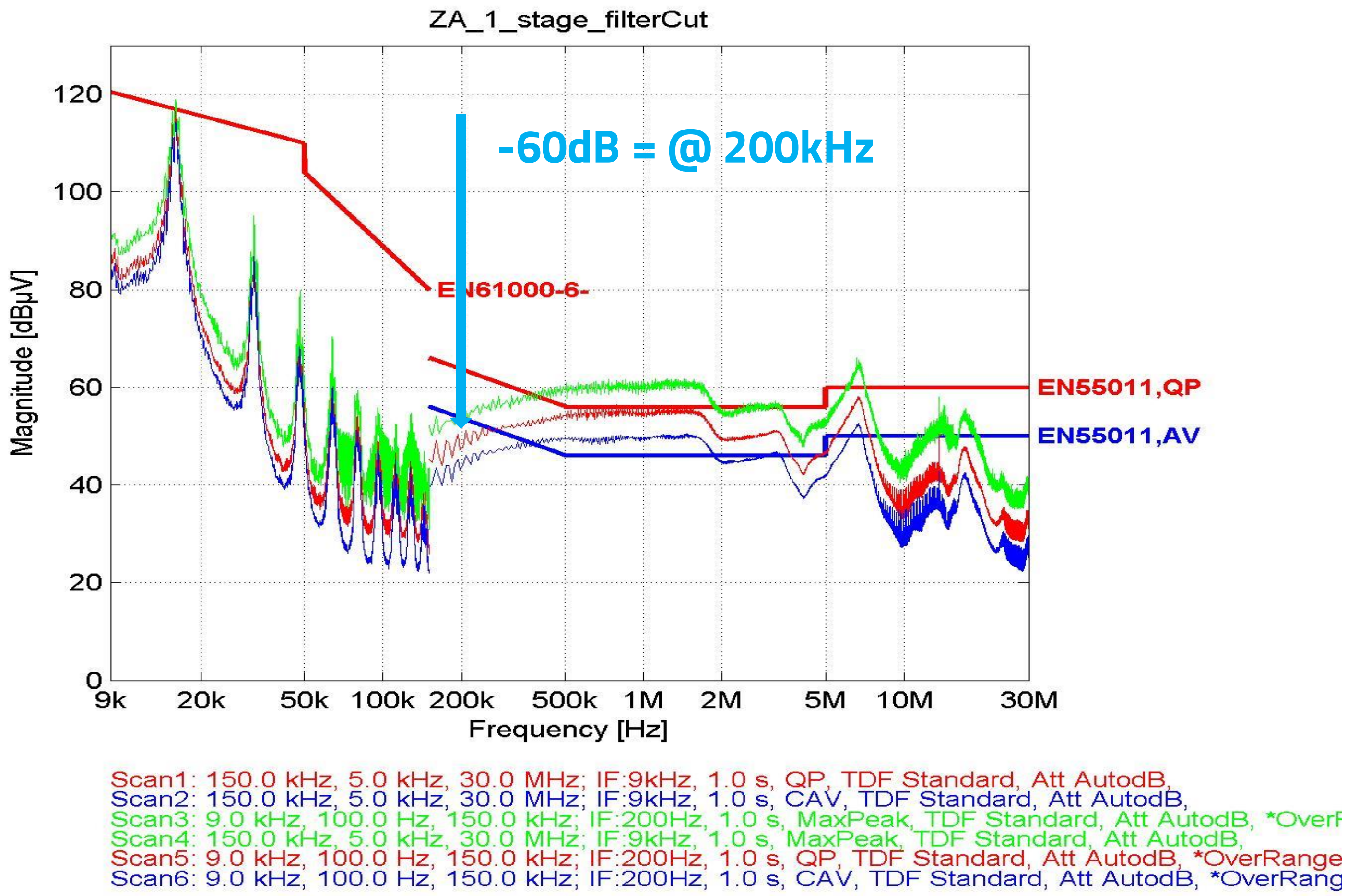
Measurements in the Lab

No Filter



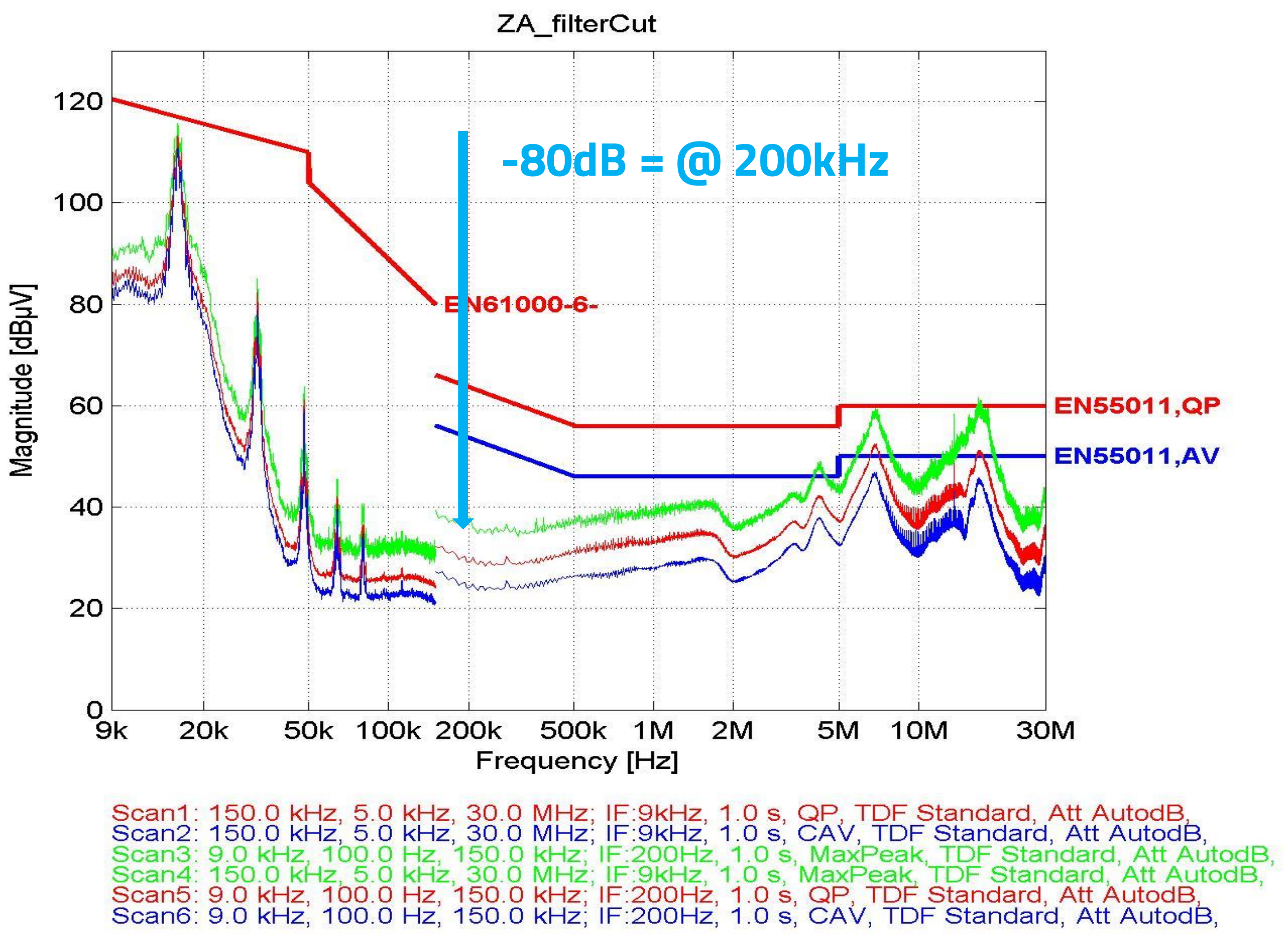
Measurements in the Lab

Calculated **CLC** Filter for 60dB @ 200kHz

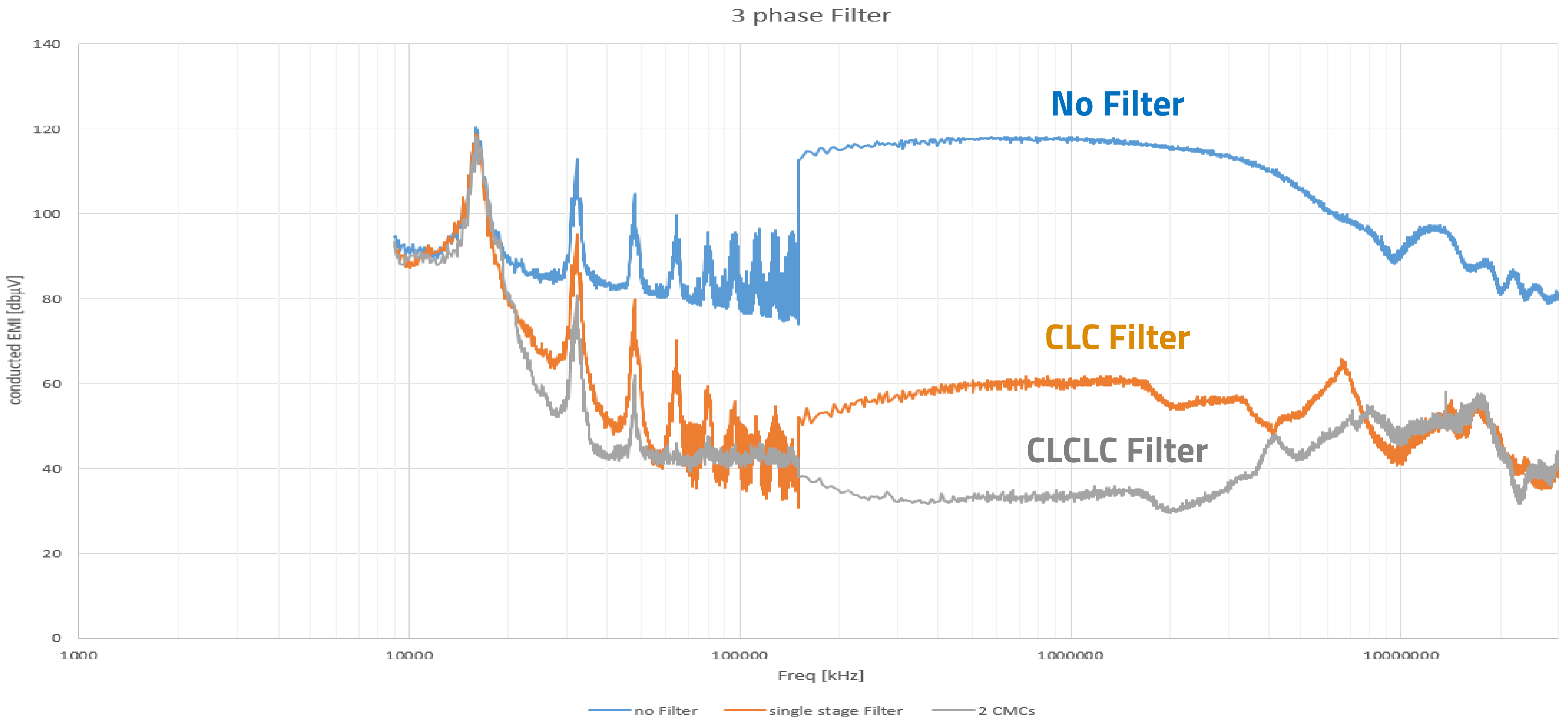


Measurements in the Lab

2- Stage **CLCLC** Filter for 80dB @ 200kHz



Overview



3 phase Filter
140
120
100
80
60
40
20
0
conducted EMI [dbµV]
1000
10000
100000
1000000
10000000
Freq [kHz]
No Filter
CLC Filter
CLCLC Filter
no Filter
single stage Filter
2 CMCs

Deviation between Math, Simulation and Real Test

Why don´t we get so much attenuation as simulated?

- CMC tolerance
- Cap tolerance
- Coupling between components
- Layout coupling (e.g. PE/chassis connection in multi stage filter)
- Grounding impedance is to high
- Wrong system impedance estimation
- Wrong DM – CM separation setup
- CMC saturation (e.g. applications with high dv/dt and long unshielded motor cables)
- Nominal CMC inductance does not match with impedance curve at requiered frequency

Y-CAP LEAKAGE

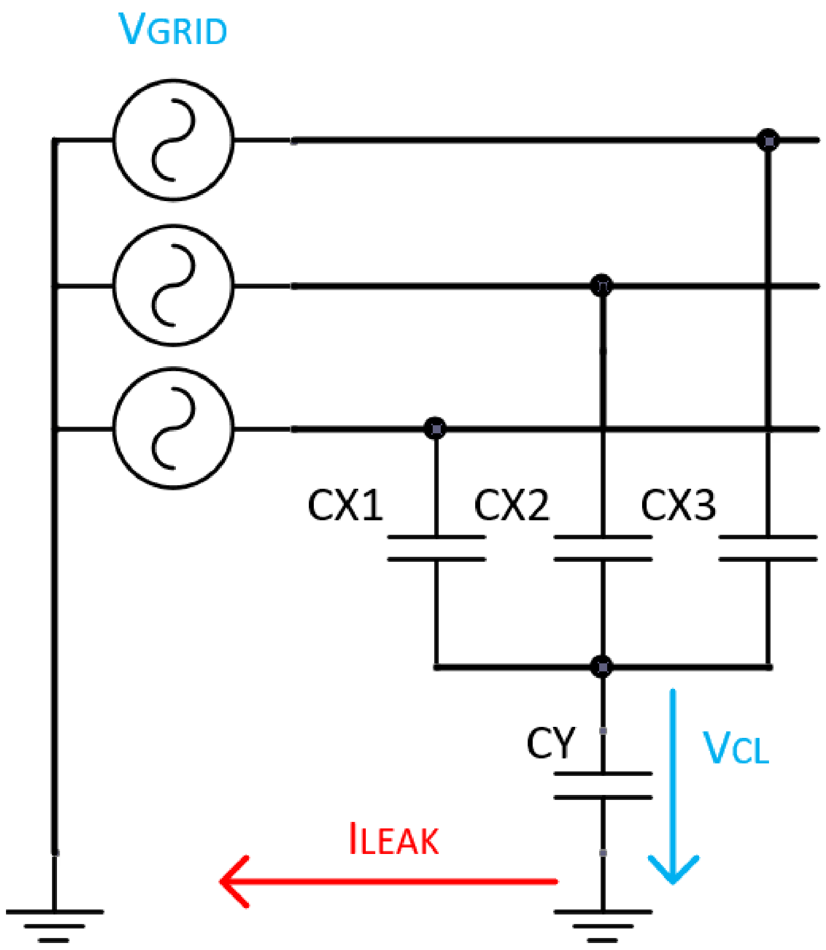
Y-Cap leakage

3-phase system with X-cap star connection

- In a balanced capacitor networtk, the sum of all 3 line currents are zero
- In theory, if all X-caps are equal, there will be no leakage
- In reality, the tolerances of the X-caps will cause some leakage
- The highest leakage occur at the highest unbalance between the phases
- Cause for the unbalance are the tolerances of the grid voltage & caps
- Assume 3% tolerances for grid voltage and 10% for caps

$$I_{leak,max} = V_{CL} \cdot 2\pi f \cdot C_{Y,max}$$

$$|I_{leak,max}| = 2\pi f \cdot C_{Y,max} \cdot \frac{V_{GRID,max} \cdot C_{X,max} - V_{GRID,min} \cdot C_{X,min}}{C_{X,max} + 2 \cdot C_{X,min} + C_{Y,max}}$$



Y-Cap leakage

3-phase system with X-cap star connection

- Example calculation
- Cx = 2.2µF / Cy = 100nF / +10% tolerance
- 400VAC grid 50Hz +-3% tolerance (EN50160)

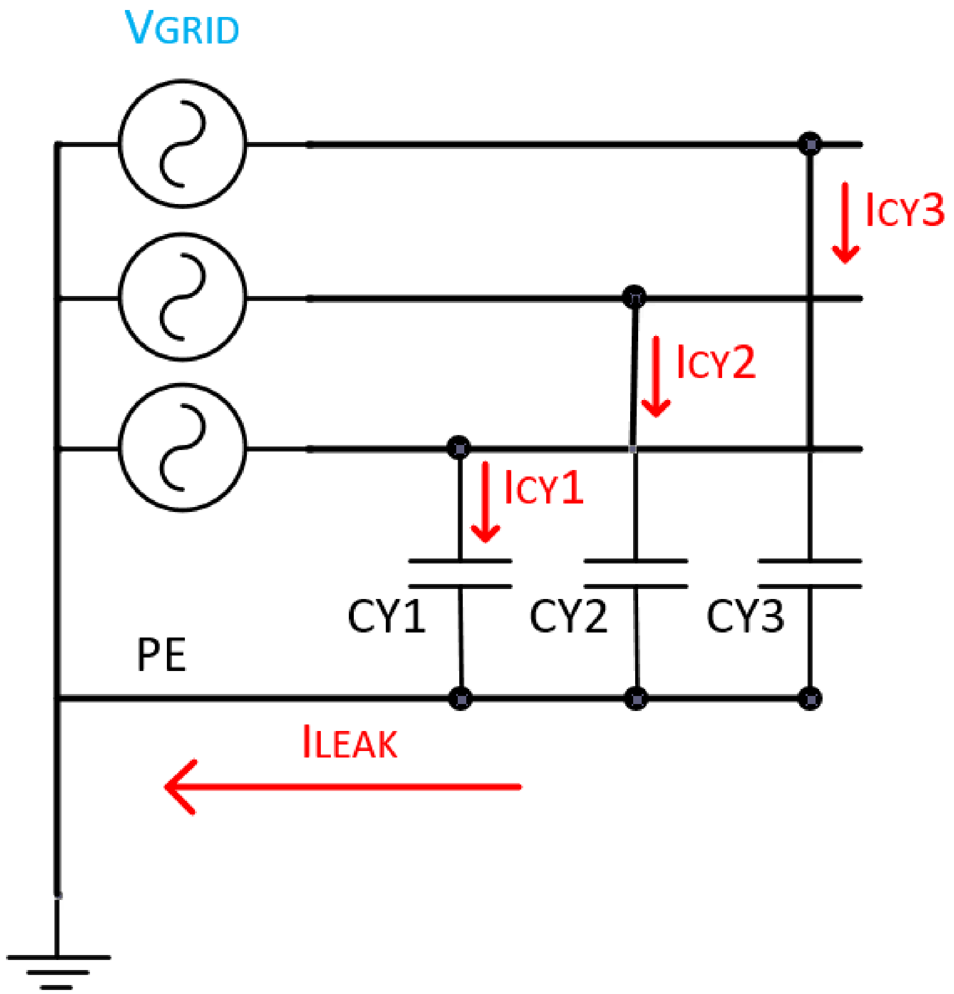
$$\left|I_{leak,max}\right| = 2\pi f \cdot C_{Y,max} \cdot \frac{V_{GRID,max} \cdot C_{X,max} - V_{GRID,min} \cdot C_{X,min}}{C_{X,max} + 2 \cdot C_{X,min} + C_{Y,max}}$$

$$\left|I_{leak,max}\right| = 2\pi 50Hz \cdot 110nF \cdot \frac{412V \cdot 2.42\mu F - 388V \cdot 1.98\mu F}{2.42\mu F + 2 \cdot 1.98\mu F + 110nF} = 1.22mA$$

Y-Cap Leakage

3-phase system

- In a perfect symmetrical / balanced system there is no leakage
- In reality a 3-phase filter is always loaded unbalanced:
- →Y-cap tolerances
- → Imbalance of the supply grid
- → Asymmetrical load



Y-Cap leakage

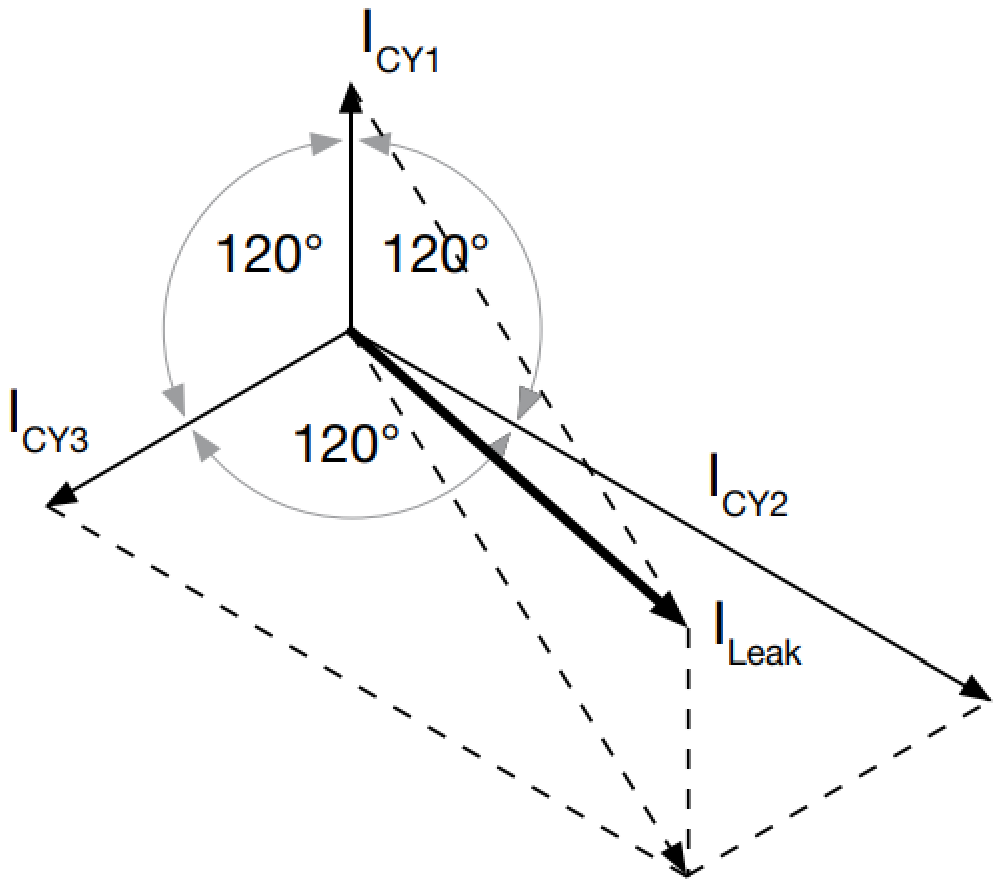
3-phase system

- The leakage currents of the vecotors of the phases need to be added together to determine the resulting discharge current!

- Practical assumption: Cy: 100nF / 50Hz / 400V

$$|I_{leak,max}| = 2\pi f \cdot (C_{Y,max} - C_{Y,min}) \cdot V_{Grid}$$

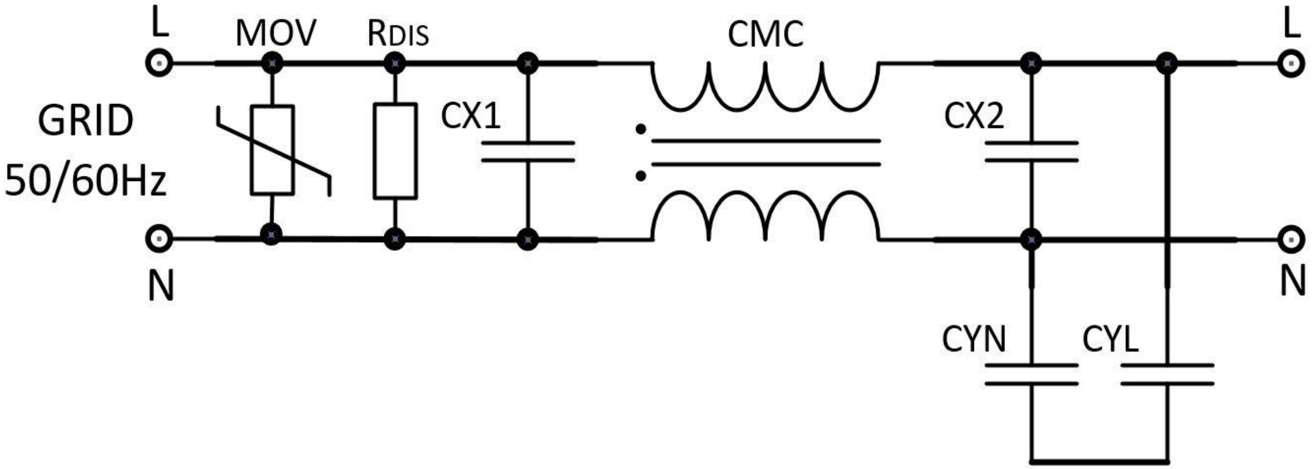
$$|I_{leak,max}| = 2\pi 50Hz \cdot (110nF - 90nF) \cdot 400V = 2.51mA$$



DISCHARGE RESISTOR

Caps Discharge Resistor

Voltage after power plug removed: In 1 second



- Power rating resistor: $Pv = \frac{{V_{Line}}^2}{R_{Discharge}}$
- e.g. $R = 220k\Omega \rightarrow 720mW@400V$
- Total capacitance: $C_{tot} = C_{X1} + C_{X2} + C_{ParaMOV} + (\frac{1}{\frac{1}{C_{Y1}}+\frac{1}{C_{Y2}}})$
- Cap discharge voltage decay: $V = V_{Grid} \cdot e^{-(t/RC)}$
- Example:
- $C_{tot} = 2{,}2\mu F \;\; V_{Grid} = 400V \;\; R = 220k\Omega \;\; t = 1sec$
- $V = V_{Grid} \cdot e^{-\left(\frac{t}{RC}\right)} = 400V \cdot e^{-1s \div (220k\Omega \cdot 2{,}2\mu F)} = 50{,}6V$
- [Capacitor Safety Discharge Conversion Calculator | DigiKey]
- Take care of: creepage, clerance and voltage rating when choosing the discharge resistor!

VARISTOR FOR 4KV SURGE TEST

Varistor

Typical 3-Phase , 4kV Surge Test

- Industrial inverter with 400 V AC voltage supply
- Surge test according to DIN EN 55024
- Coupling type: symmetrical (phase to neutral conductor)
- Test voltage: $\hat{U}$_G= 4kV
- Coupling impedance (= internal resistance of the test generator):
- $Z_{\mathrm{G}} = 2\Omega$

- Selection of the varistor:
- Operating voltage taking into account the tolerance:
- U_rms = 460V
- **20 mm high surge** disk varistor WE-VD 820424611

- Specification:
- Voltage at the electronics should not exceed **1.6kV**

Electrical Properties:

Properties		Test conditions	Value	Unit	Tol.
AC Operating Voltage	V_{RMS}		460	V	max.
DC Operating Voltage	V_{DC}		615	V	max.
Clamping Voltage	V_{Clamp}	100 A @ 8/20 µs	1240	V	max.
(Reverse) Peak Pulse Current	I_{Peak}	8/20 µs	10000	A	max.
Power Dissipation	P_{Diss}		1	W	max.
Energy Absorption	W_{max}	10/1000 µs	440	J	max.
Nominal Discharge Current	I_n		5	kA	max.
Measured Limiting Voltage	V_{ML}		1690	V	max.
(Reverse) Breakdown Voltage	V_{BR}	1 mA	750	V	±10%
(Channel) Input Capacitance	C_{Ch}	1 kHz	520	pF	typ.

Varistor 3-Phase / 4kV Surge

Determination of operating point Alternative iterative calculation (use Redexpert V/I max. curve for reading)

- Step 1: Determination of the maximum clamping voltage for the short-circuit current of the test generator ($\hat{V}_G$=4kV/ Z_G = 2Ω / 2kA / 400V x 1.41) → $I_G = \frac{V_G + V_{Grid}}{Z_G} = \frac{4kV + 564V}{2\Omega} = 2282A$

V/I characteristic curve +10% tolerance: $V_{CALMP_{max}@2282A} \rightarrow 1.69kV$

- Step 2: Calculation of the new current value through the varistor using the known coupling impedance Z_G and V_clamp_max: $\mathrm{I_{C1}} = \frac{\mathrm{V_G + V_{Grid} - V_{CLAMP_{max}}}}{\mathrm{Z_G}} = \frac{\mathrm{4kV + 564V - 1.69kV}}{2\Omega} = 1437A$
- V/I characteristic curve +10% tol. : $V_{CALMP@1437A} \rightarrow \mathbf{1.56kV}$✓
- Step 3: Determine max. I_clamp through varistor using the V/I curve with -10%
- $V_{CALMP_{min}@1437A} \rightarrow 1.29kV$
- Step 4: Calculate the max. current through the varistor: $\mathrm{I_{C\_max}} = \frac{\mathrm{V_G + V_{Grid} - V_{CLAMP_{min}}}}{\mathrm{Z_G}} = \frac{\mathrm{4kV + 564V - 1.29kV}}{2\Omega} = \mathbf{1637A}$

Varistor

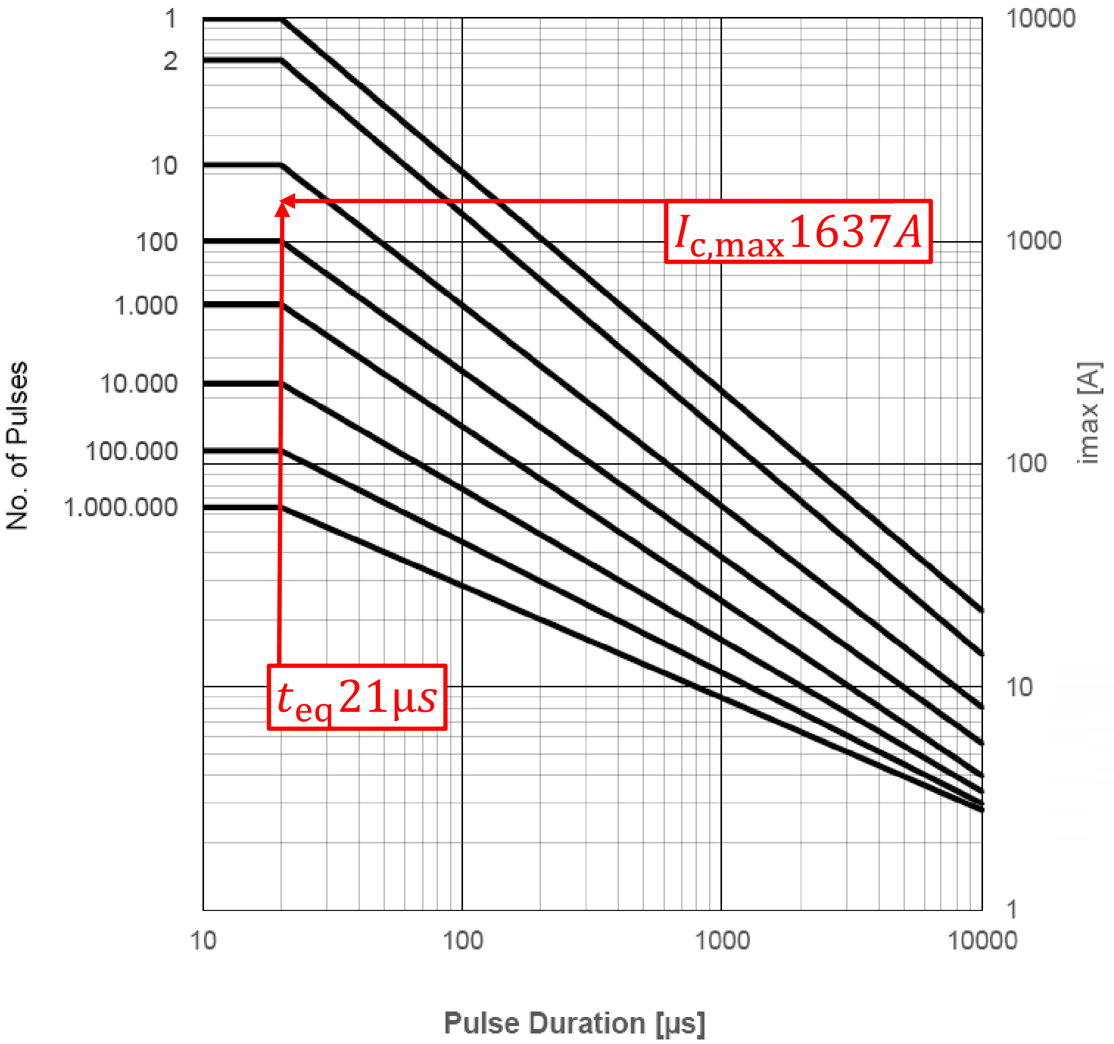
Typical 3-Phase, 4kV Surge Test

- Check how many 8/20µs current pulses the varistor can withstand
- Determining the equivalent width of the square-wave current pulse

$$t_{\mathrm{eq},8/20} = 0{,}5 \cdot T_1 + 1{,}43 \cdot (T_2 - T_1)$$
$$= 0{,}5 \cdot 8\mu s + 1{,}43 \cdot 12\mu s$$
$$= 21{,}16\mu s$$

- The varistor can withstand approx. 50 @ 21µs pulses with 766A
- What is the maximum energy occurring in the varistor during the test? → 40 pulses ✓

Pulse Lifetime Derating:



Varistor

Typical 3-Phase, 4kV Surge Test

- Maximum energy occurring in the varistor:

$$W_V = I_{clamp,max} \cdot U_{clamp,min} \cdot t_{eq,8/20} = 1637\text{A} \cdot 1290\text{V} \cdot 21{,}16\mu\text{s} = 44.7\text{Ws}$$

- Datasheet: $W_{max} = 440\text{Ws}$ (Joule) ✓

- The maximum power loss is specified as P_max=600mW. The minimum necessary recovery time (cooling of the component) is therefore given as:

$$T > \frac{W_V}{P_{max}} = \frac{44.7\text{Ws}}{1\text{W}} = 44{,}7\text{s} \checkmark$$

- The basic standard DIN EN 61000-4-5 requires a maximum recovery time of 60 seconds. The varistor fulfills this criterion.