

DIGITAL WE DAYS

2023



BOARD-TO-BOARD CONNECTORS  
IN HIGH-SPEED SIGNAL CHAINS

WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

## TODAY'S SPEAKERS



### **PRESENTATION**

Baptiste Bouix  
Product Manager



### **MODERATION**

Markus Eberle  
Marketing Department

# INFORMATION ABOUT THE WEBINAR

**You are muted during the webinar.**

However, you can ask us questions using the chat function.

**Duration of the presentation** 30 Min  
**Q&A:** 10 – 15 Min

**Any questions?**  
**No problem! Email us** [digital-we-days@we-online.com](mailto:digital-we-days@we-online.com)

**Please help us to optimize our webinars!**  
We are looking forward to your feedback.

**On our channel** Würth Elektronik Group  
**And on** [Digital WE Days 2023 YouTube Playlist](#)



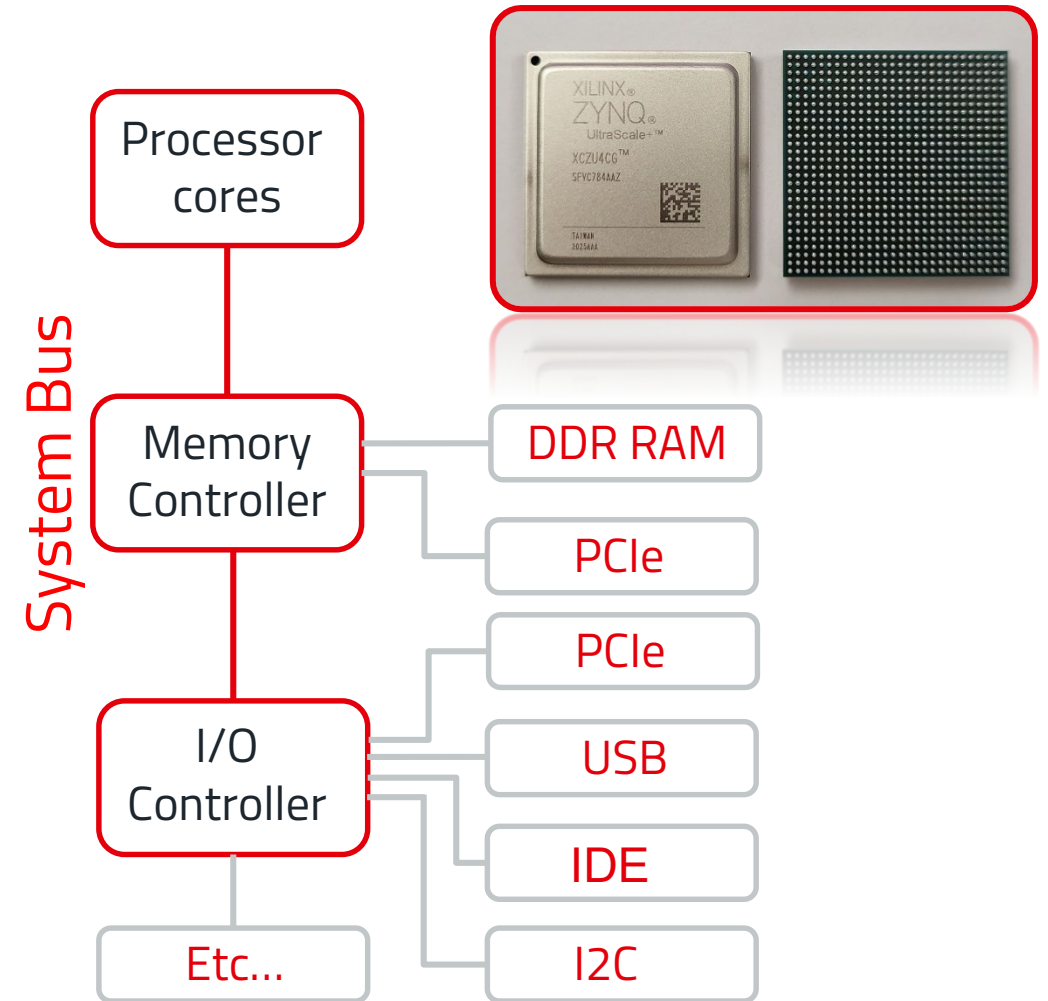
# INTRODUCTION

Required concepts for understanding

# INTRODUCTION

## Electronic System Architecture

- In a electronic system, a computing chip (either a microcontroller, a microprocessor or system-on-chip) will be **processing** what it gets from its system bus.
- The system bus links to the **memory controller**, which handle the system's communication with the memory
- Downstream of the system bus, a **I/O controller** will handle all the inputs and outputs of the system
- **I/O protocols don't necessarily involve an external connector on the device**
- Some protocols can either be on the memory or the I/O controller



# INTRODUCTION

## Parallel and Serial Transmission

- **Serial**

- Symbols are transmitted over 1 channel in sequence



- 1 channel = 1 or 2 wires

- **Parallel**

- Symbols are transmitted over n channels, then put again into a sequence
- The number of channels n is referred as the « bit width »



# INTRODUCTION

## Limits of Transmission

- The receiving chip has to be able to read the symbol
  - Symbol = voltage level or transition
- Sample Rate = the frequency of the reading in the receiving device
  - In Transfers/second (T/s)
- Losses are frequency-dependant

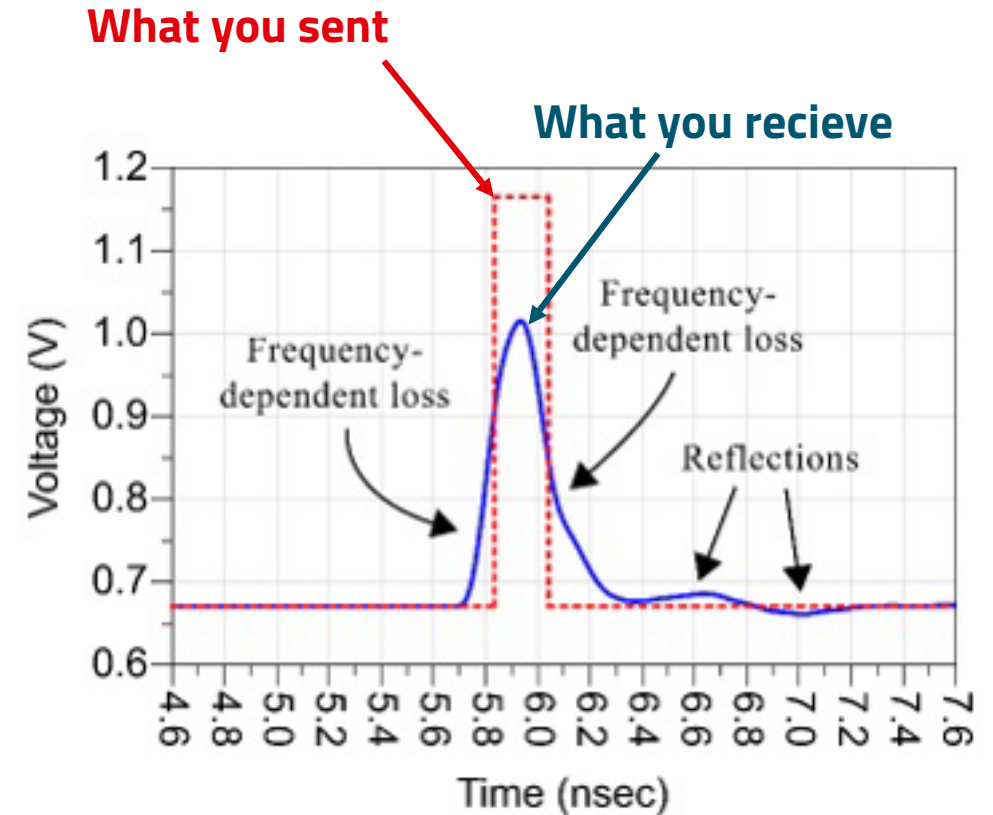


Figure 2. Single pulse response of a DQ line shows both frequency-dependent loss and reflections in a DDR5 channel.

# INTRODUCTION

## Limits of Transmission

- The receiving chip has to **be able to read the symbol**
  - Symbol = voltage level or transition
- Sample Rate = the frequency of the reading in the receiving device
  - In Transfers/second (T/s)
- Losses are frequency-dependant

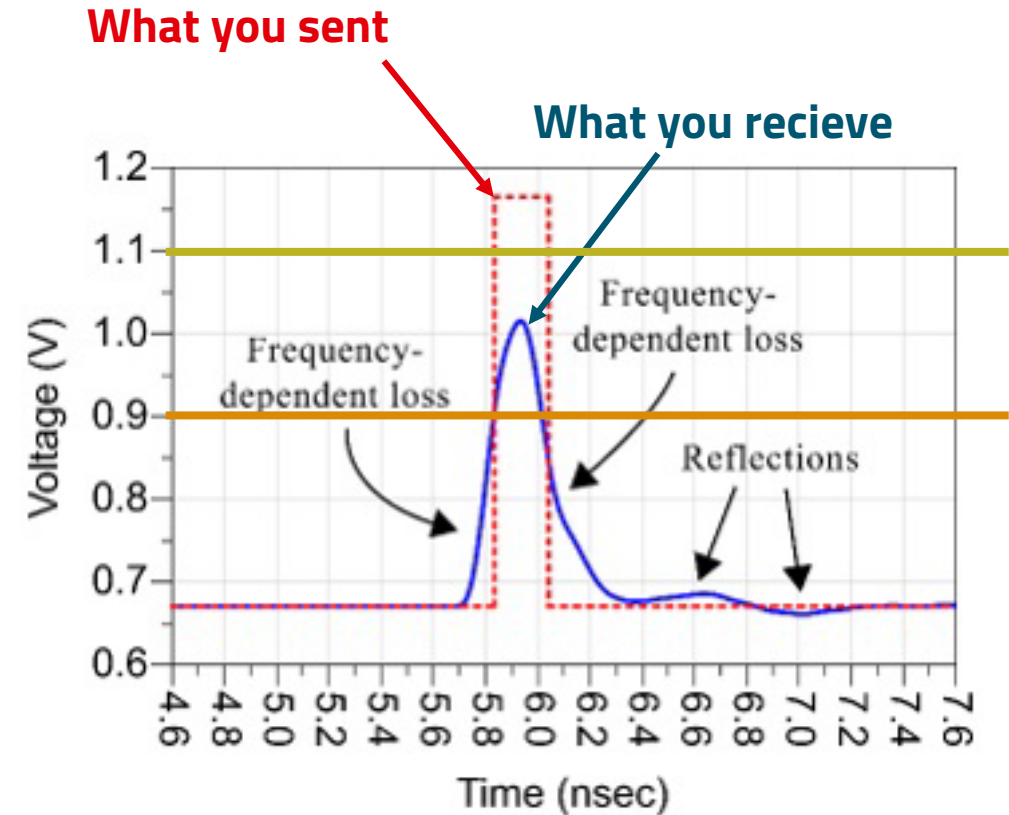


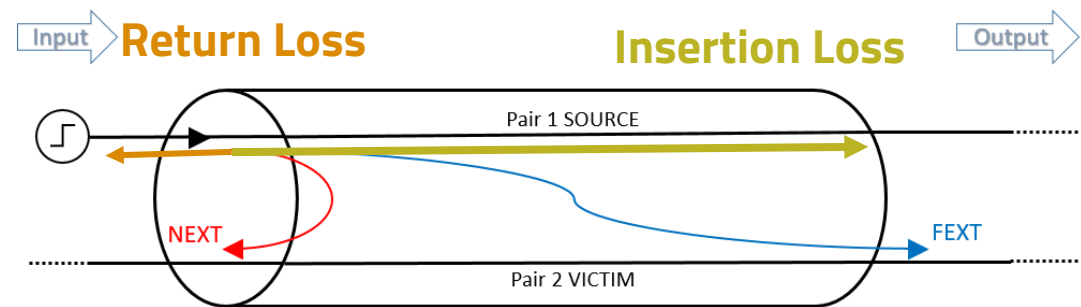
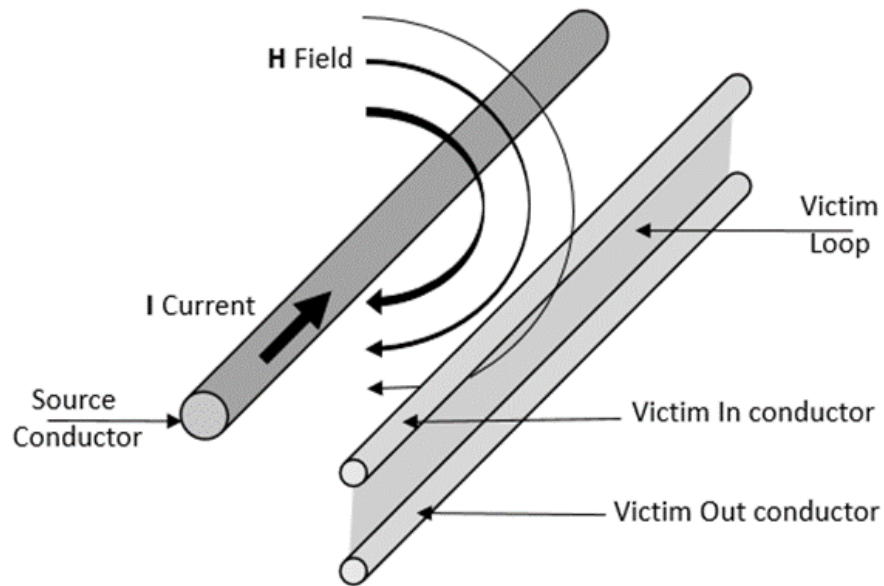
Figure 2. Single pulse response of a DQ line shows both frequency-dependent loss and reflections in a DDR5 channel.



# INTRODUCTION

## Frequency Channel Losses

- Signal loss at high frequency comes from :
  - Impedance
  - Impedance mismatch
  - Signal going to nearby conductors : Crosstalk
- ➔ **Connectors and cables are a source of high-frequency losses**



# INTRODUCTION

## Frequency Channel Losses

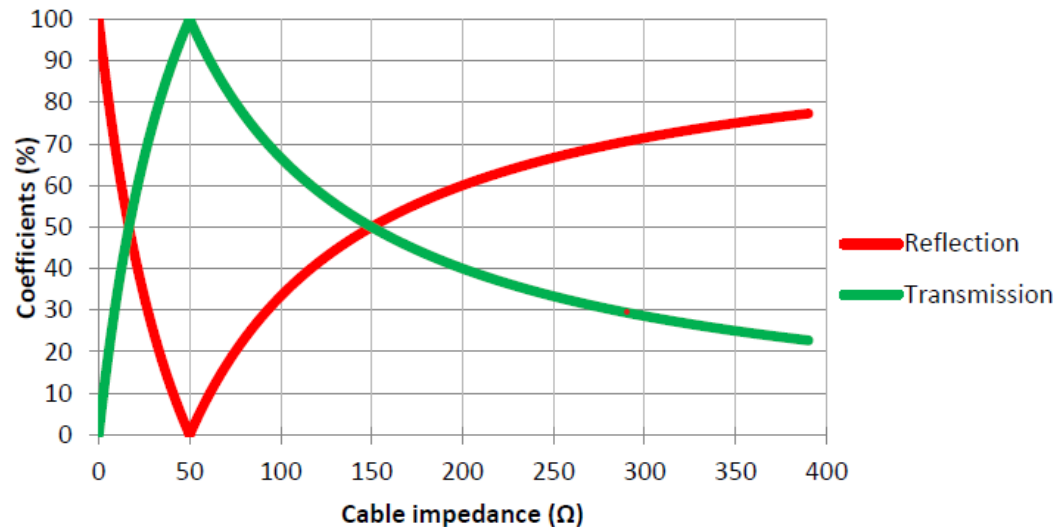
- Signal loss at high frequency comes from :
  - Impedance
  - **Impedance mismatch**
  - Signal going to nearby conductors : Crosstalk
- ➔ **Connectors and cables are a source of high-frequency losses**

Reflection Coefficient

$$\rho = \frac{Z_{CAB} - Z_S}{Z_{CAB} + Z_S}$$

Transmission Coefficient

$$\tau = 1 - \frac{Z_{CAB} - Z_S}{Z_{CAB} + Z_S}$$



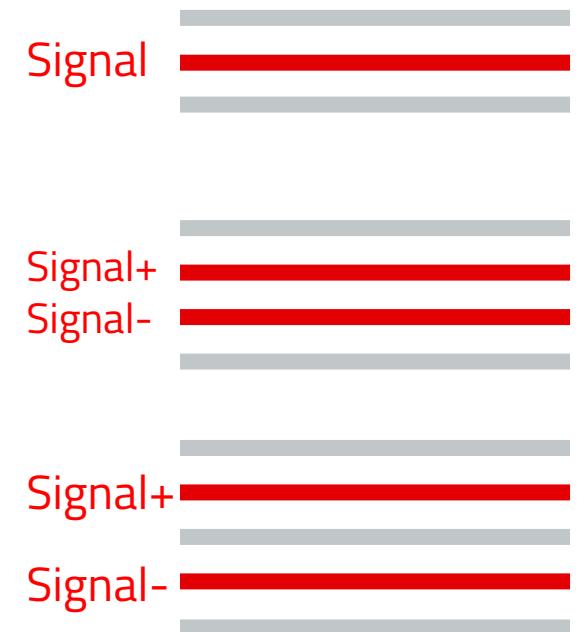
Impedance matching

- Minimizes signal reflections
- Maximizes efficiency

# INTRODUCTION

## Transmission line in connectors

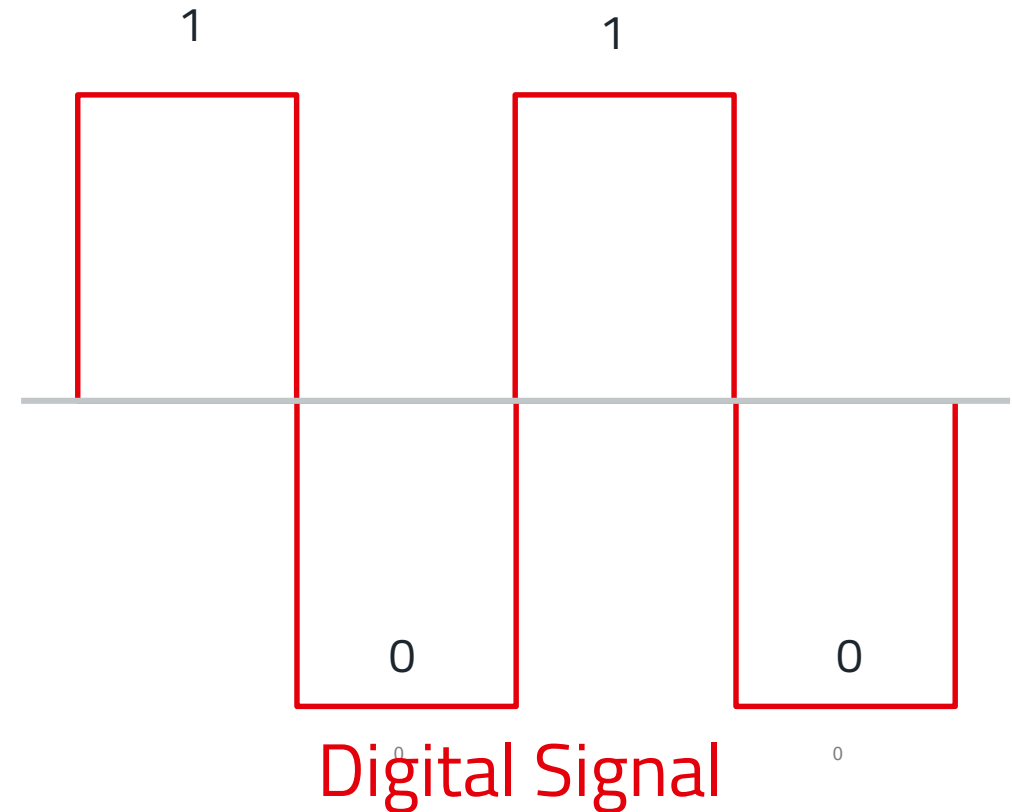
- To limit losses in connectors, impedance must be matched with PCB
  - Pins on connector ends have a different impedance, it is unadvised to use them for signal
    - It is not always possible (see RJ45)
    - Best performance is reached when signal pins have ground pins around them
- GSG
  - Generic transmission line in connectors
- GSSG
  - Used for Differential Signalling
  - Best performances in higher frequencies and noisy environments
- GSGSG
  - GSG for Differential Signalling
  - Better performance at lower frequencies than GSSG



# INTRODUCTION

## Nyquist Frequency

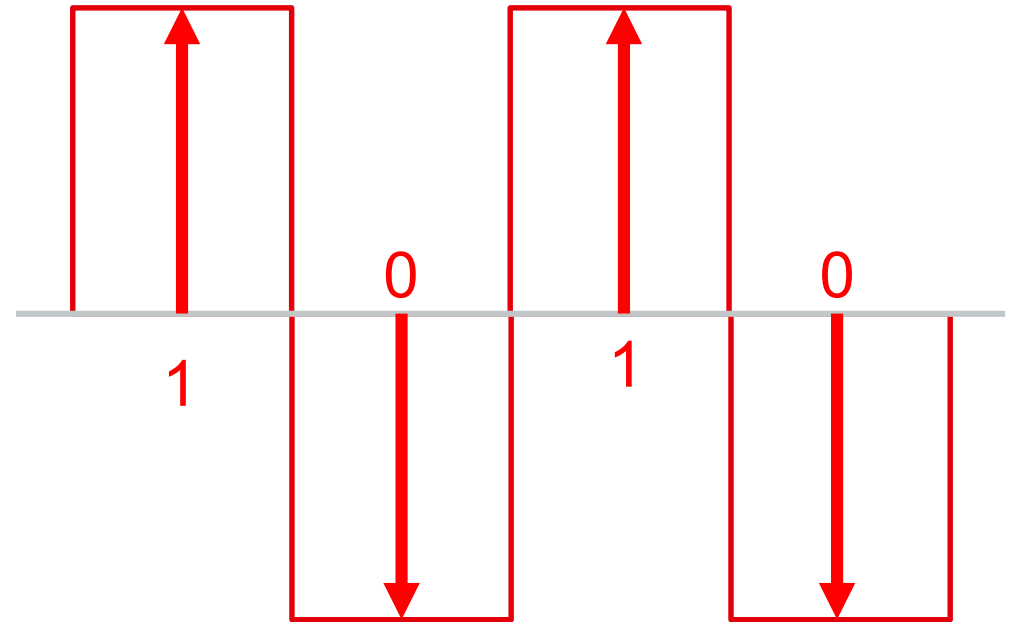
- **Shannon's theorem** states that a periodic signal must be sampled at more than **twice the highest frequency** component of the signal to keep information integrity
- $f_{max,signal} = \frac{Sample\ Rate}{2}$
- Protocols can specify a channel loss at  $f_{max,signal}$ , called the Nyquist Frequency
  - To see if a connector technology, you have to check the allowed Insertion Loss at the  $f_{Nyquist}$



# INTRODUCTION

## Nyquist Frequency

- **Shannon theorem** states that a periodic signal must be sampled at more than **twice the highest frequency** component of the signal to keep information integrity
- $f_{max,signal} = \frac{Sample\ Rate}{2}$
- Protocols can specify a channel loss at  $f_{max,signal}$ , called the Nyquist Frequency
  - To see if a connector technology, you have to check the allowed Insertion Loss at the  $f_{Nyquist}$

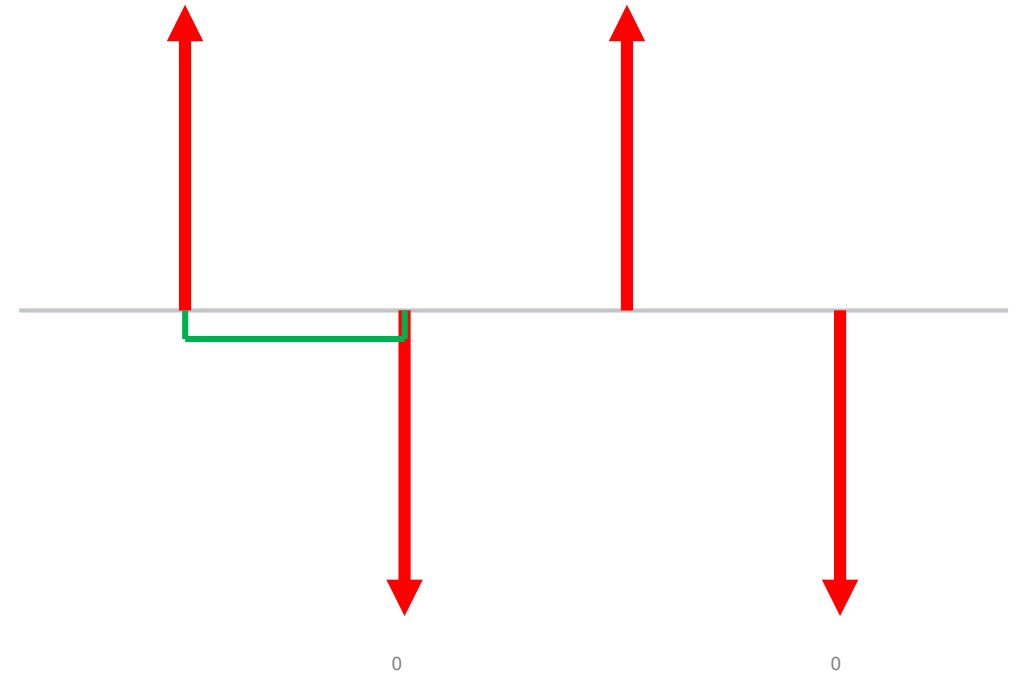


Sampling

# INTRODUCTION

## Nyquist Frequency

- **Shannon theorem** states that a periodic signal must be sampled at more than **twice the highest frequency** component of the signal to keep information integrity
- $f_{max,signal} = \frac{Sample\ Rate}{2}$
- Protocols can specify a channel loss at  $f_{max,signal}$ , called the Nyquist Frequency
  - To see if a connector technology, you have to check the allowed Insertion Loss at the  $f_{Nyquist}$

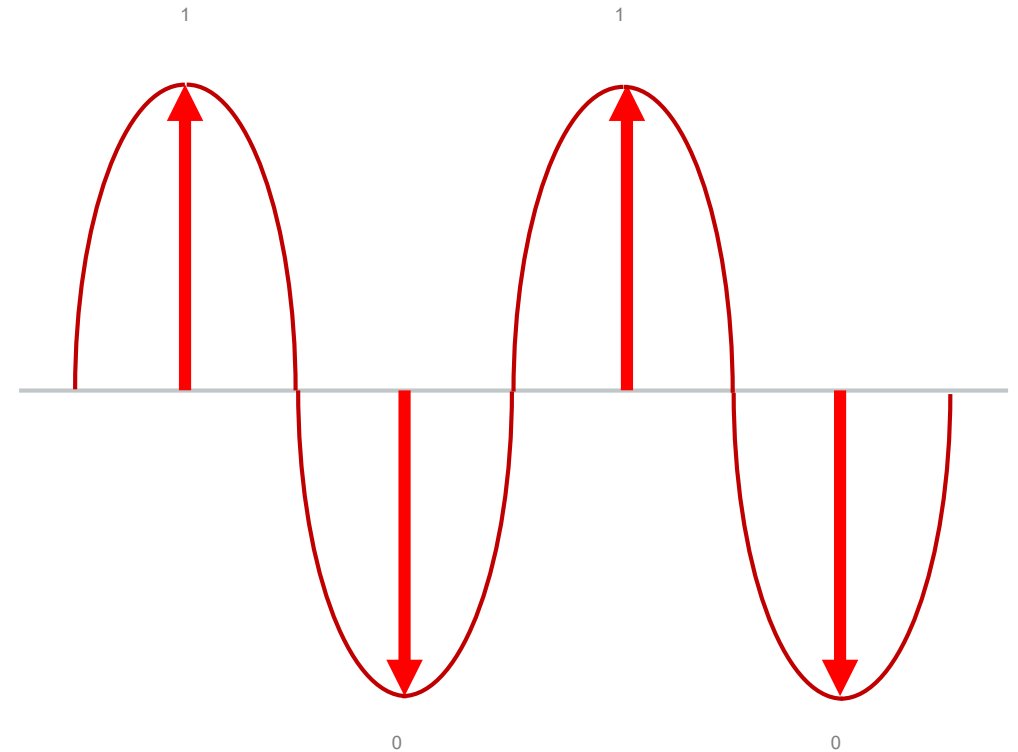


Sample Rate : 1/T

# INTRODUCTION

## Nyquist Frequency

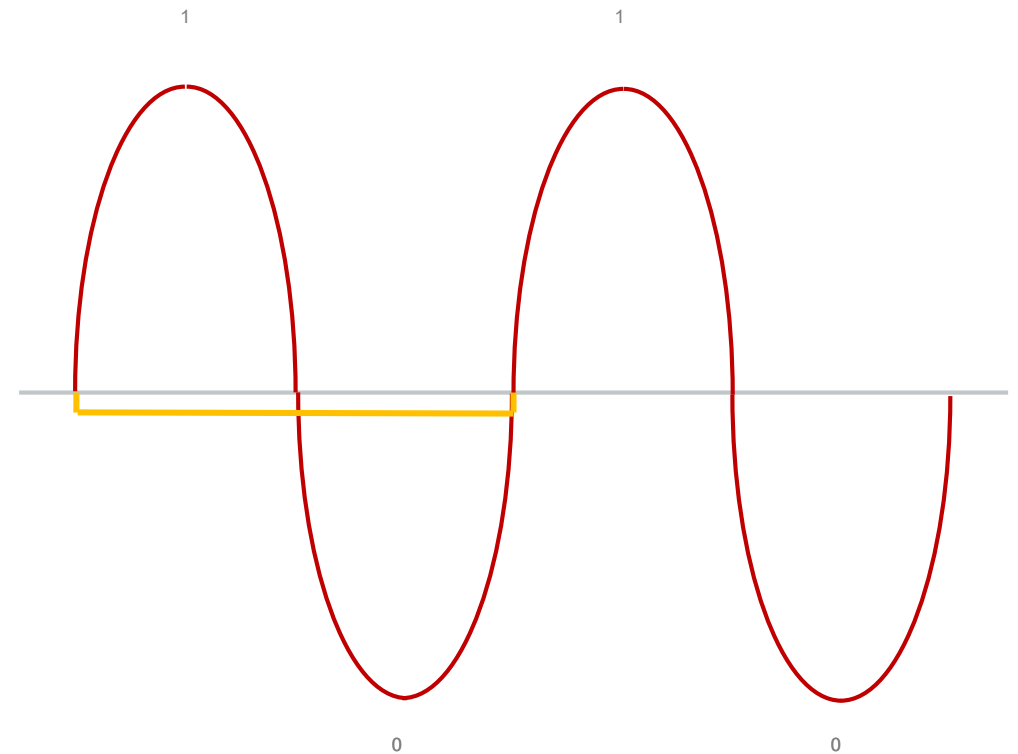
- **Shannon theorem** states that a periodic signal must be sampled at more than **twice the highest frequency** component of the signal to keep information integrity
  - $f_{max,signal} = \frac{Sample\ Rate}{2}$
  - Protocols can specify a channel loss at  $f_{max,signal}$ , called the Nyquist Frequency
- ➔ To see if a connector technology, you have to check the allowed Insertion Loss at the  $f_{Nyquist}$



# INTRODUCTION

## Nyquist Frequency

- **Shannon theorem** states that a periodic signal must be sampled at more than **twice the highest frequency** component of the signal to keep information integrity
  - $f_{max,signal} = \frac{Sample\ Rate}{2}$
  - Protocols can specify a channel loss at  $f_{max,signal}$ , called the Nyquist Frequency
- To see if a connector technology, you have to check the allowed Insertion Loss at the  $f_{Nyquist}$



Nyquist Frequency:  $1/2T$



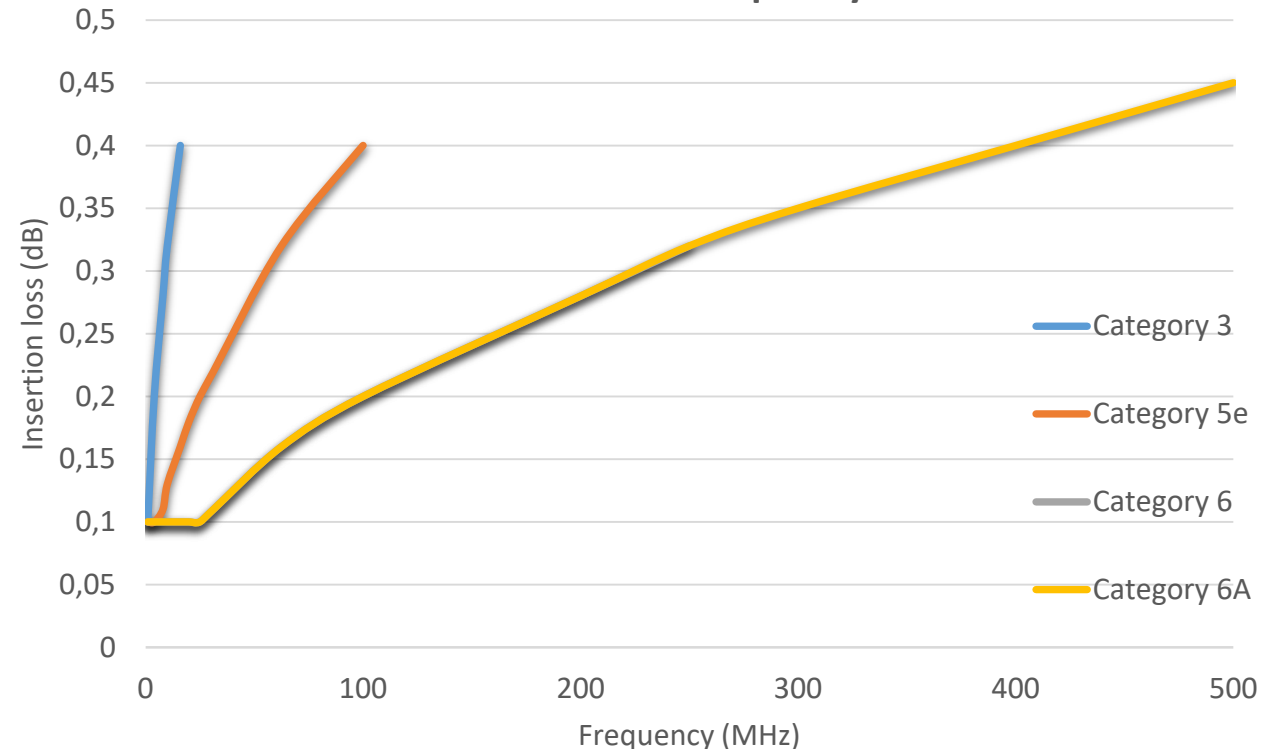
# INTRODUCTION

Example : Category Rating for Ethernet Physical Layer

- Example in the industry : Ethernet cabling
  - Every component (Modular Jacks, Cable...) has an allowed **loss budget in dB**
    - 1,5 dB loss is 29% of the signal lost
    - 3 dB loss is half of the signal lost
  - You can add the losses of the components on the signal chain

➔ **Standards : Physical Layers**

EIA 568 standard insertion losses for Ethernet Jacks as a function of frequency



# CONNECTORS FOR MEMORY SIGNAL CHAINS

Northbridge/Memory Bus

# CONNECTORS FOR MEMORY SIGNAL CHAINS

## DRAM Connectors

- Dynamic Random-Access Memory (as opposed to Static RAM embedded in chips)
- Used by systems to store data and programs while in use
- Widespread technology : DDR SDRAM
  - Double Data Rate Synchronous Dynamic Random-Access Memory
  - **Standardized chips** and modules treated like commodities
  - Standard maintained by the **JEDEC**
  - Levels of standard from **DDR (1) to DDR5**
  - Available in higher bandwidth for video memory (GDDR)
- Parallel Transmission (**GSG** configuration)
- Nyquist Frequency from 100MHz (DDR) to 3,6GHz (DDR5)

# CONNECTORS FOR MEMORY SIGNAL CHAINS

## DRAM Connectors

- Dynamic Random-Access Memory (as opposed to Static RAM embedded in chips)
- Used by systems to store data and programs while in use
- Widespread technology : DDR SDRAM
  - Double Data Rate Synchronous Dynamic Random-Access Memory
  - Standardized chips** and modules **treated like commodities** →
  - Standard maintained by the **JEDEC**
  - Levels of standard from **DDR (1) to DDR5**
  - Available in higher bandwidth for video memory (GDDR)
- Parallel Transmission (**GSG** configuration)
- Nyquist Frequency from 100MHz (DDR) to 3,6GHz (DDR5)

Spot	Memory Card	SSD	Contract	Mobile DRAM	eMMC		
<b>DRAM Spot Price</b> <a href="#">MORE</a> Last Update: Sep.28 2023 18:10 (GMT+8) <Price Notice>							
Early notice was announced at 17:50. (20 minutes in advance)							
Item	Daily High	Daily Low	Session High	Session Low	Session Average	Session Change	History
DDR4 16Gb (1Gx16)3200	3.45	2.68	3.45	2.68	2.996	0.98 %	
DDR4 16Gb (2Gx8)3200	3.35	2.65	3.35	2.65	2.934	0.21 %	
DDR4 8Gb (1Gx8) 3200	1.65	1.37	1.65	1.37	1.450	0.00 %	
DDR4 8Gb (512Mx16) 3200	1.75	1.42	1.75	1.42	1.502	0.00 %	
DDR4 8Gb (1Gx8) eTT	1.27	1.03	1.27	1.03	1.152	0.17 %	
DDR3 4Gb 512Mx8 1600/1866	SK Hynix, Micron, Samsung, Nanya					0.00 %	
<b>Module Spot Price</b> <a href="#">MORE</a> Last Update: Sep.18 2023 14:40 (GMT+8) <Price Notice>							
Item	Weekly High	Weekly Low	Session High	Session Low	Session Average	Average Change	History
DDR4 SODIMM 8GB 2666	15.70	11.60	15.70	11.60	13.856	0.93 %	
DDR4 UDIMM 8GB 2666	15.20	11.60	15.20	11.60	13.684	2.55 %	
DDR4 RDIMM 16GB 3200	38.50	37.00	38.50	37.00	37.500	3.59 %	
<b>Flash Spot Price</b> <a href="#">MORE</a> Last Update: Sep.28 2023 18:10 (GMT+8) <Price Notice>							
Early notice was announced at 17:50. (20 minutes in advance)							
Item	Daily High	Daily Low	Session High	Session Low	Session Average	Session Change	History
SLC 2Gb 256MBx8	1.25	0.56	1.25	0.56	0.771	-0.52 %	
SLC 1Gb 128MBx8	1.65	0.52	1.65	0.52	0.812	0.37 %	
MLC 64Gb 8GBx8	4.25	3.40	4.25	3.40	3.867	0.00 %	
MLC 32Gb 4GBx8	3.00	1.90	3.00	1.90	2.063	0.00 %	
<b>GDDR Spot Price</b> <a href="#">MORE</a> Last Update: Sep.18 2023 14:40 (GMT+8) <Price Notice>							
Item	Weekly High	Weekly Low	Session High	Session Low	Session Average	Average Change	History
GDDR5 8Gb	4.20	3.40	4.20	3.40	3.649	4.62 %	
GDDR6 8Gb	3.50	2.10	3.50	2.10	2.957	0.72 %	
<b>LPDDR Spot Price</b> <a href="#">MORE</a> Last Update: Sep.18 2023 14:40 (GMT+8) <Price Notice>							
LPDDR 3 32Gb	LPDDR 3 16Gb		LPDDR 3 8Gb				
LPDDR 4 32Gb	LPDDR 4 16Gb		LPDDR 4 8Gb				

# CONNECTORS FOR MEMORY SIGNAL CHAINS

## PCI Express

- Used for **chip-to-chip** communication at high speed
- Widespread Technology
  - **Power** and **Data delivery** Standard
  - Standard maintained by the **PCI-SIG**
  - Levels of standard available from **PCIe 1 to PCIe 7**
  - Available with **1 to 16 transmission/reception line**
- Serial Transmission in **GSSG** differential configuration
- Nyquist Frequency from 1,2GHz (PCIe 1) to 32GHz (PCIe 7)

PCIe® Speeds/Feeds - Pick Your Bandwidth

- Flexible to meet needs from handheld/client to server/HPC
- ~Max Total Bandwidth = Max RX bandwidth + Max TX bandwidth
- 35 Permutations yielding 11 unique bandwidth profiles
- Encoding overhead and header efficiency not included

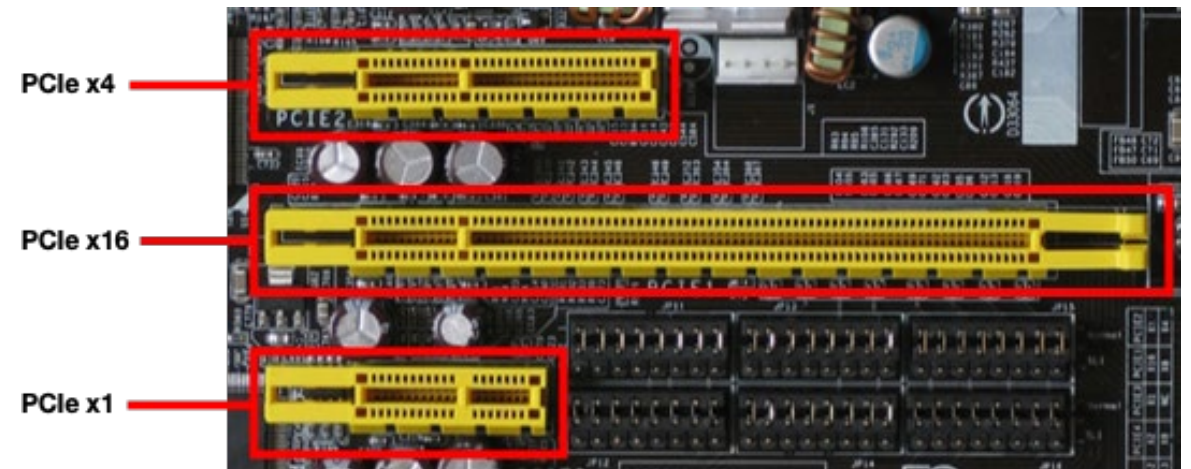
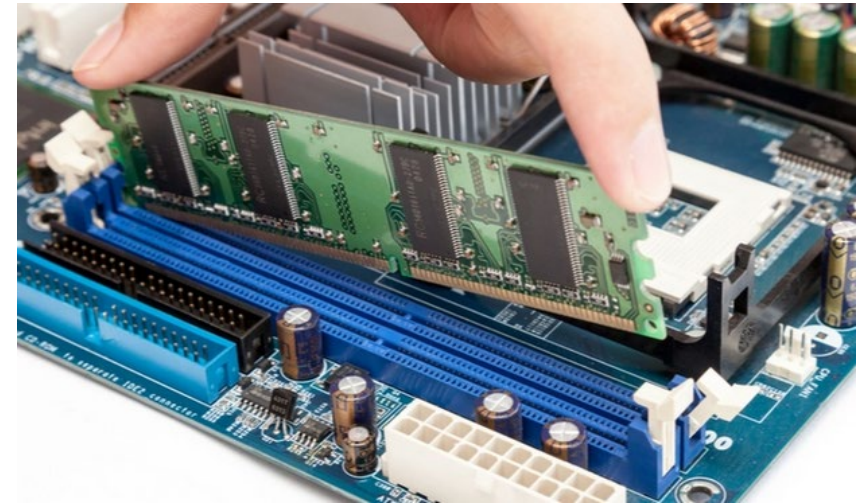
Specifications	Lanes				
	x1	x2	x4	x8	x16
2.5 GT/s (PCIe 1.x +)	500 MB/S	1 GB/S	2 GB/S	4 GB/S	8 GB/S
5.0 GT/s (PCIe 2.x +)	1 GB/S	2 GB/S	4 GB/S	8 GB/S	16 GB/S
8.0 GT/s (PCIe 3.x +)	2 GB/S	4 GB/S	8 GB/S	16 GB/S	32 GB/S
16.0 GT/s (PCIe 4.x +)	4 GB/S	8 GB/S	16 GB/S	32 GB/S	64 GB/S
32.0 GT/s (PCIe 5.x +)	8 GB/S	16 GB/S	32 GB/S	64 GB/S	128 GB/S
64.0 GT/s (PCIe 6.x +)	16 GB/S	32 GB/S	64 GB/S	128 GB/S	256 GB/S
128.0 GT/s (PCIe 7.x +)	32 GB/S	64 GB/S	128 GB/S	256 GB/S	512 GB/S

+ = data rate supported by this and subsequent spec revisions.

# CONNECTORS FOR MEMORY SIGNAL CHAINS

## DDR SDRAM and PCI Express Standard Connectors

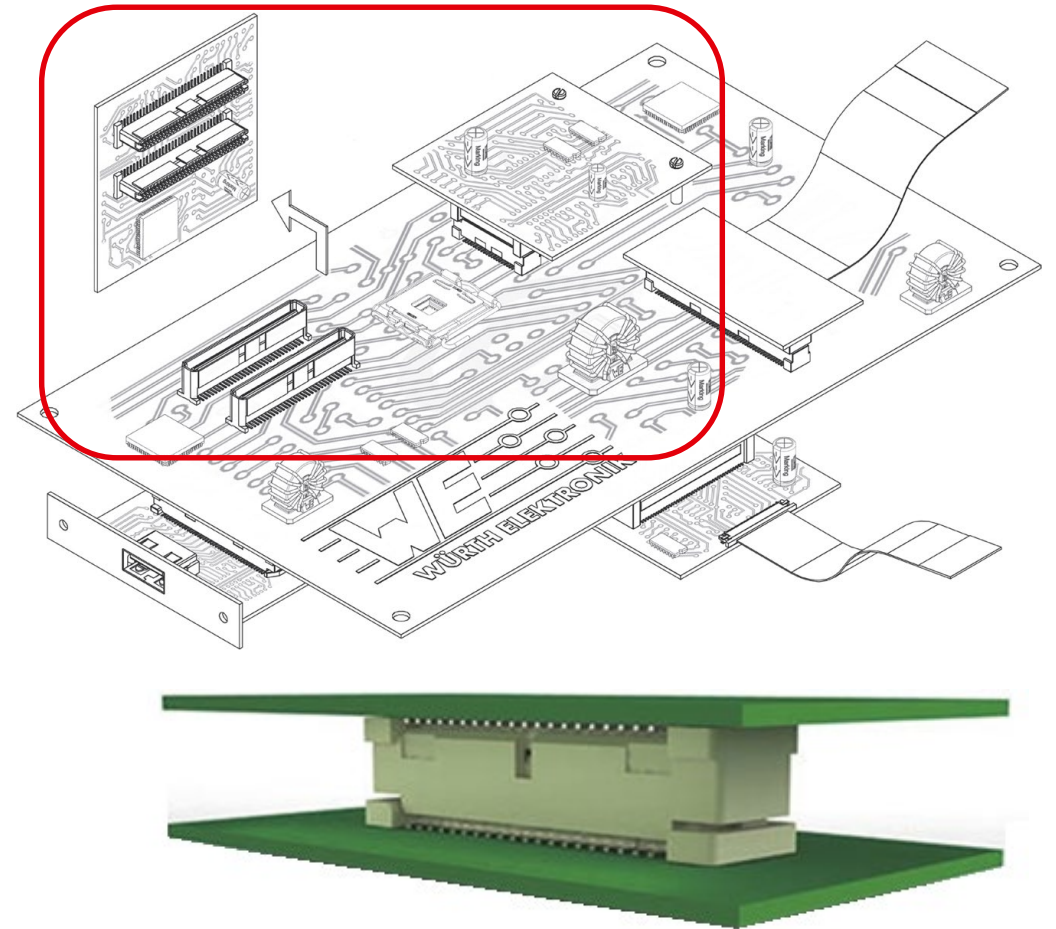
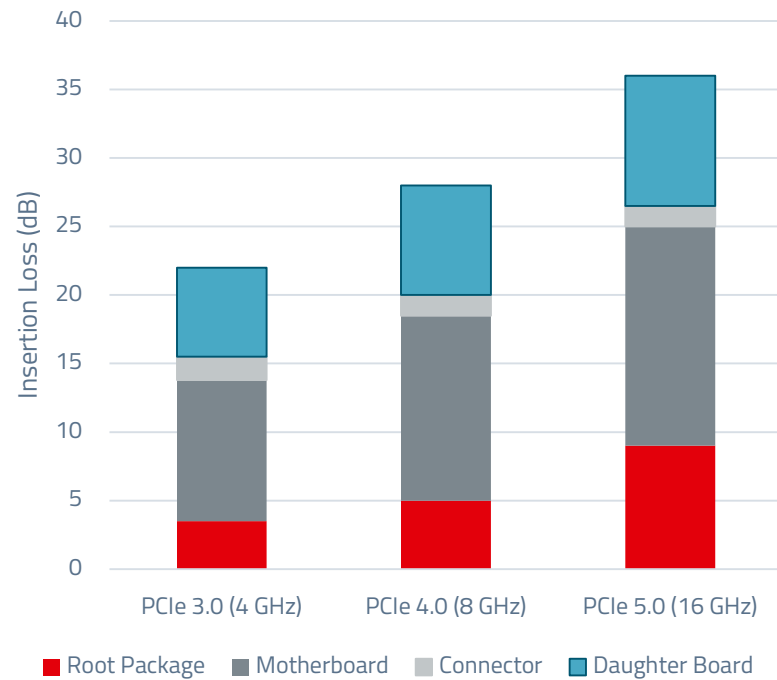
- **Board Edge** Connector
  - A counterpart PCB makes the connection
  - Very low losses at high frequency
  - Very bulky, only adapted for desktop PC and servers
- DIMM Connector
  - 150-200 contacts
  - DIMM : Dual Inline Memory Module
  - Different variants for each DDR level (notches)
- PCI Express connector
  - 36 contacts for PCIe x1
  - 64 contacts for PCIe x4
  - 98 contacts for PCIe x8
  - 164 contacts for PCIe x16
  - Physically compatible with all levels of PCIe



# CONNECTORS FOR MEMORY SIGNAL CHAINS

## DDR SDRAM and PCIe

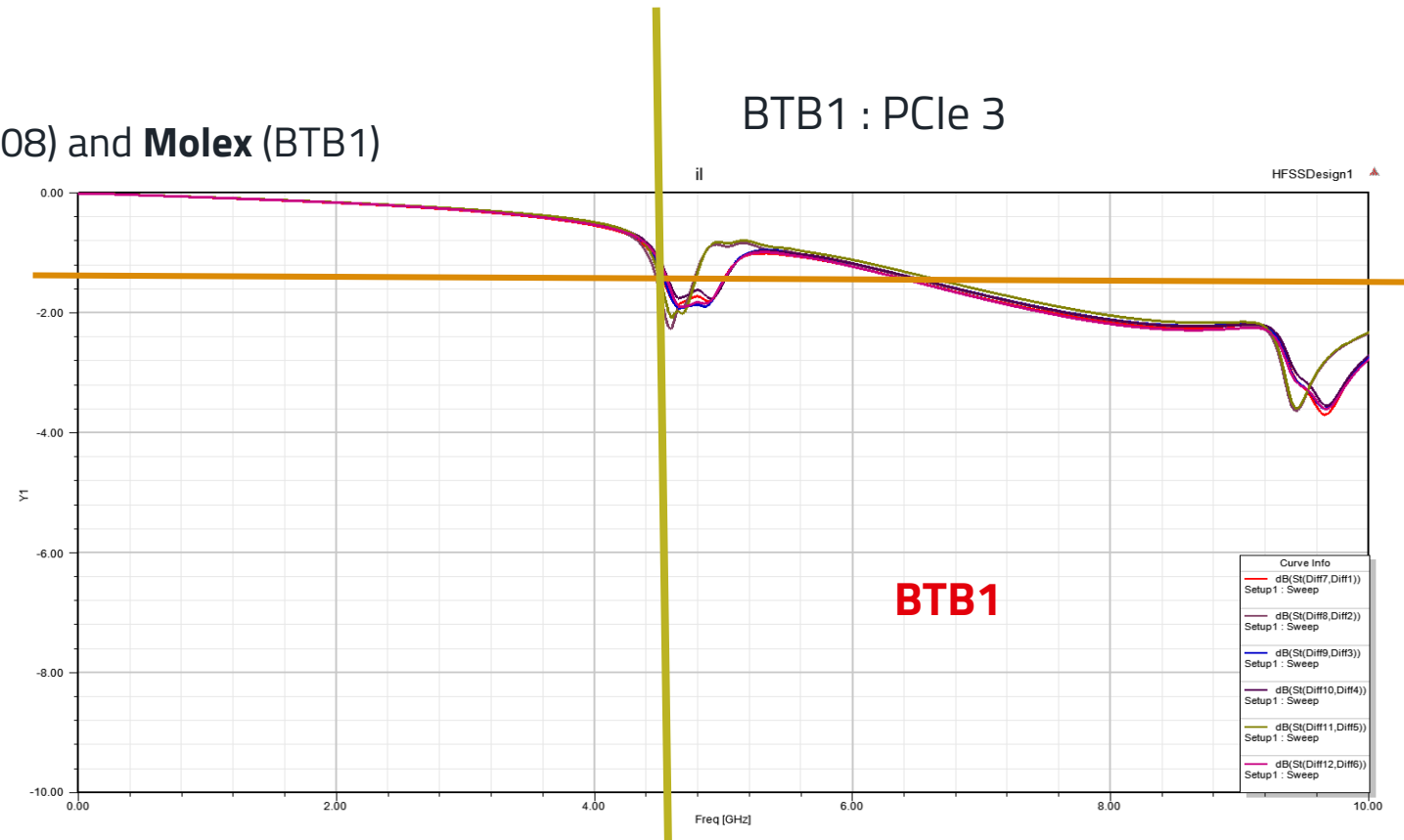
- Alternative : Using Mezzanine Board-to-Board Connector is possible, however the standards are very demanding
  - 1,5 dB allowed losses GSSG at Nyquist in PCIe standard



# CONNECTORS FOR MEMORY SIGNAL CHAINS

## Mezzanine Board-to-Board connectors

- WE **BTB08** and **BTB1** series are well-suited for such applications
  - 100 Ohm Differential Impedance (as PCIe)
  - More compact than Board Edge Connectors
  - **Limited** insertion loss in **GSSG configuration**
  - Cross reference with **TE and Amphenol (BTB08)** and **Molex (BTB1)**
- However
  - Non-standard (limits interchangeability)
  - Lower power allowed than Board Edge Connectors





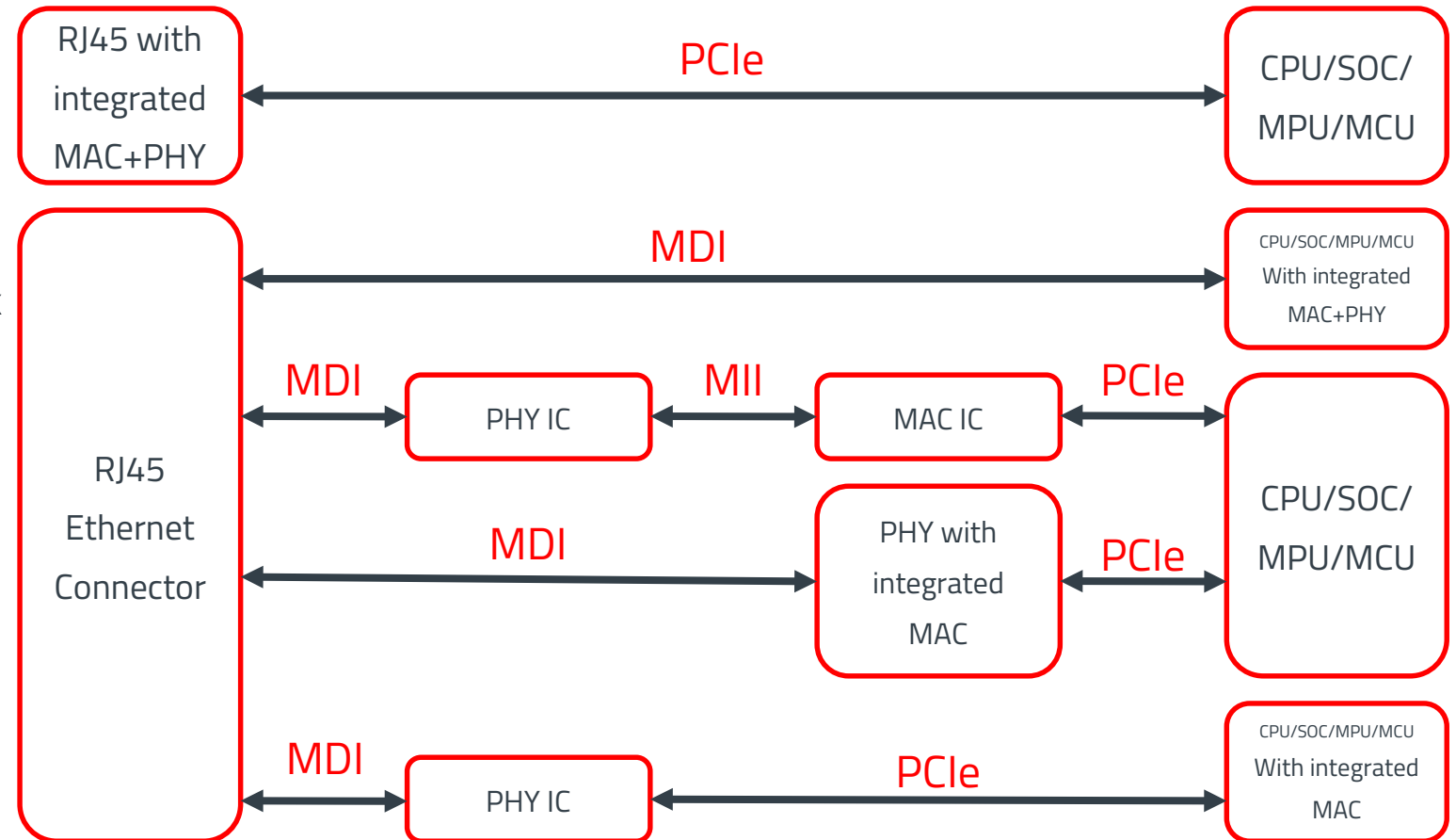
# CONNECTORS FOR I/O SIGNAL CHAINS

Southbridge/I/O

# CONNECTORS FOR I/O SIGNAL CHAINS

## Ethernet Interfaces

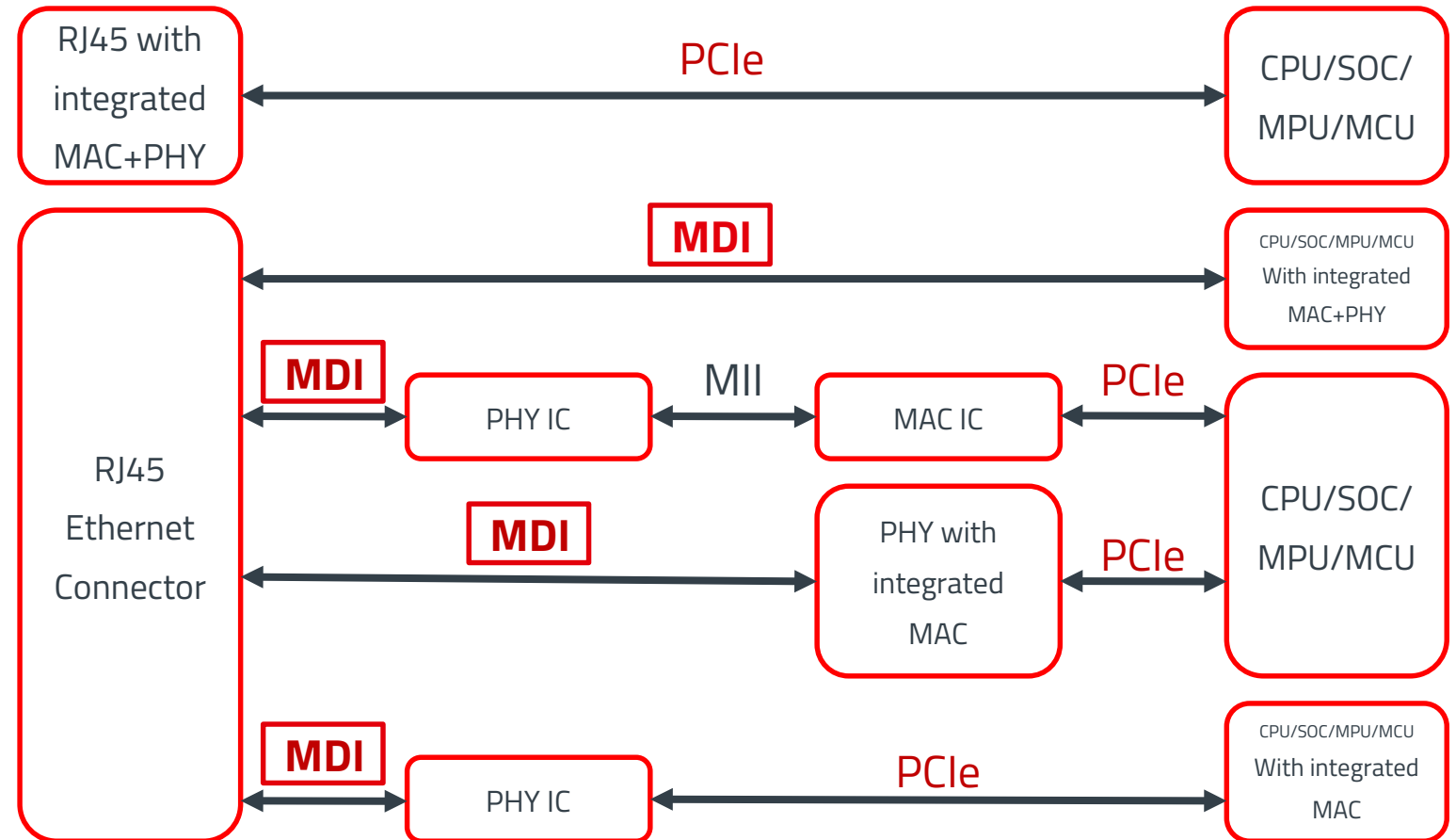
- Ethernet has a very complex signal chain
  - An internal interface has to be used to bring signal to the MAC (here, PCIe)
  - **MII** : internal universal interface to link the MAC to the PHY (the PHY can be optical or electrical)
  - **MDI** : external signal that goes in the Modular Jack and cable



# CONNECTORS FOR I/O SIGNAL CHAINS

## Ethernet Interfaces

- Ethernet has a very complex signal chain
  - An internal interface has to be used to bring signal to the MAC (here, PCIe)
  - MII : internal universal interface to link the MAC to the PHY (the PHY can be optical or electrical)
  - **MDI : external signal that goes in the Modular Jack and cable**



# CONNECTORS FOR I/O SIGNAL CHAINS

## Ethernet Interfaces

- Ethernet has a very complex signal chain
  - **MDI : external signal that goes in the Modular Jack and cable**

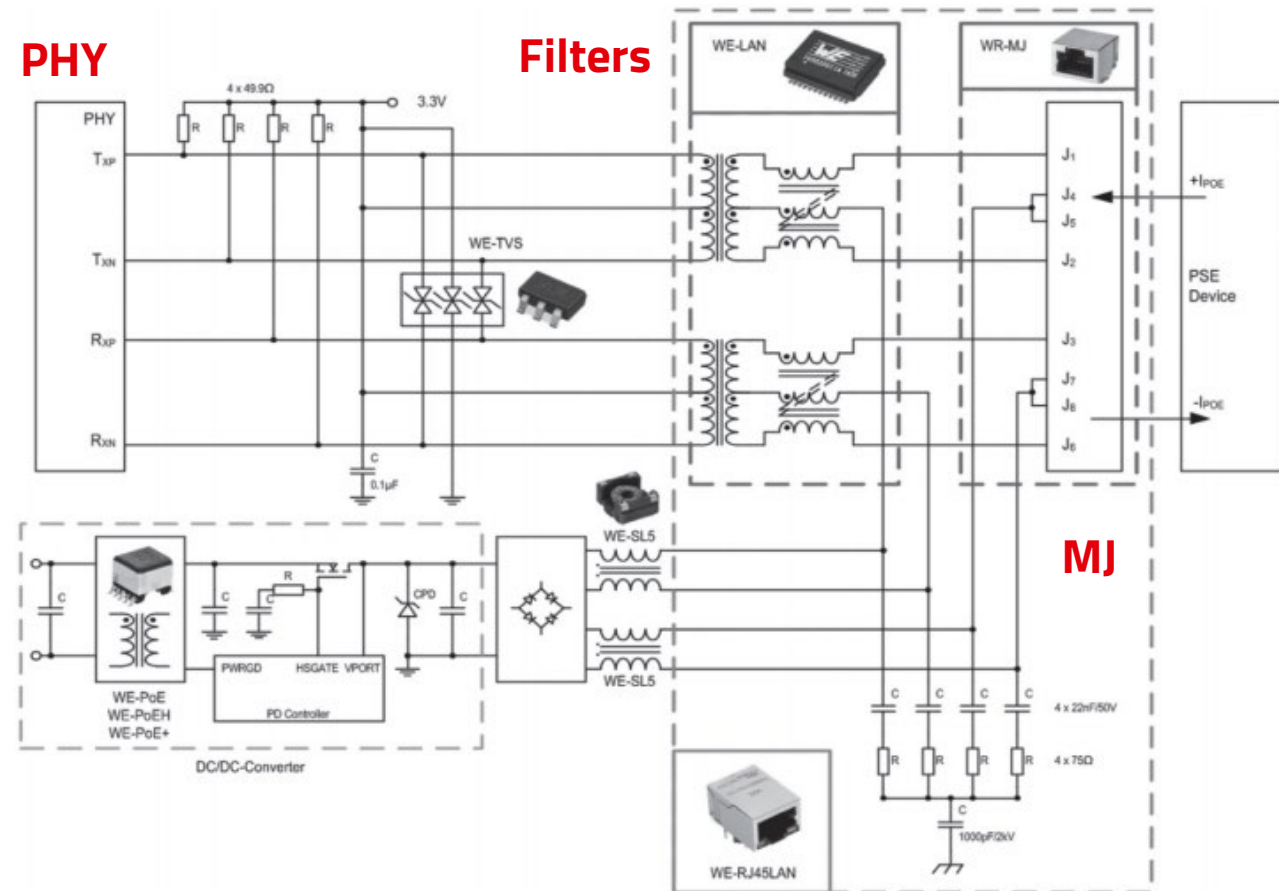
- Active PHYciever
- PCB trace
- Passive Filters
- Modular Jack

**Device 1**

- Cable with modular plugs

- Modular Jack
- Passive Filters
- PCB trace
- Active PHYciever

**Device 2**



# CONNECTORS FOR I/O SIGNAL CHAINS

## Ethernet Interfaces

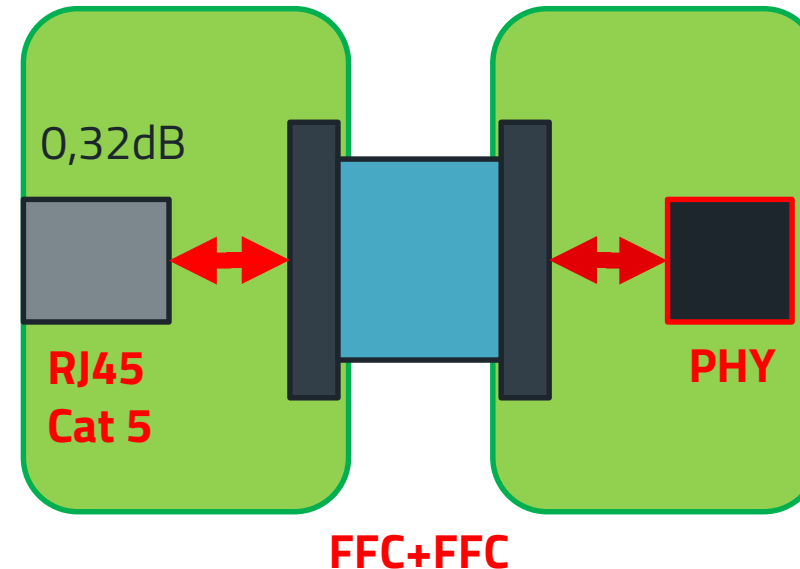
- Customer example
  - PHY and RJ45 not on the same PCB
  - 100BASE-T (Cat 5)
  - How to link both ?

# CONNECTORS FOR I/O SIGNAL CHAINS

## Ethernet Interfaces

- Customer example
  - PHY and RJ45 not on the same PCB
  - 100BASE-T (Cat 5)
  - How to link both ?
- Use a FFC with FPC connectors !

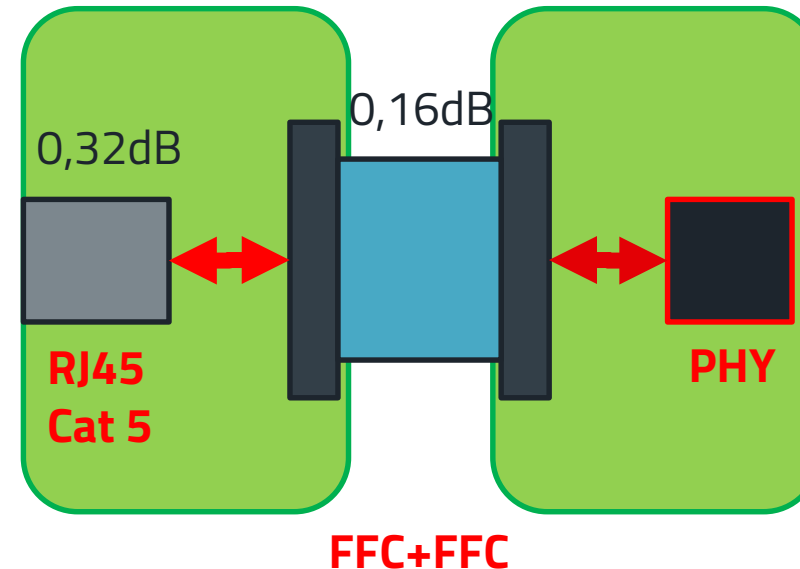
- But how ?



# CONNECTORS FOR I/O SIGNAL CHAINS

## Ethernet Interfaces

- Customer example
  - PHY and RJ45 not on the same PCB
  - 100BASE-T (Cat 5)
  - How to link both ?
- ➔ Use a FFC with FPC connectors !
- But how ?
  - Use GSSG configuration
  - At least 13 pins
  - Not over 5-10cm
  - 100Ω differential impedance
- But isn't there a problem with Ethernet standard?

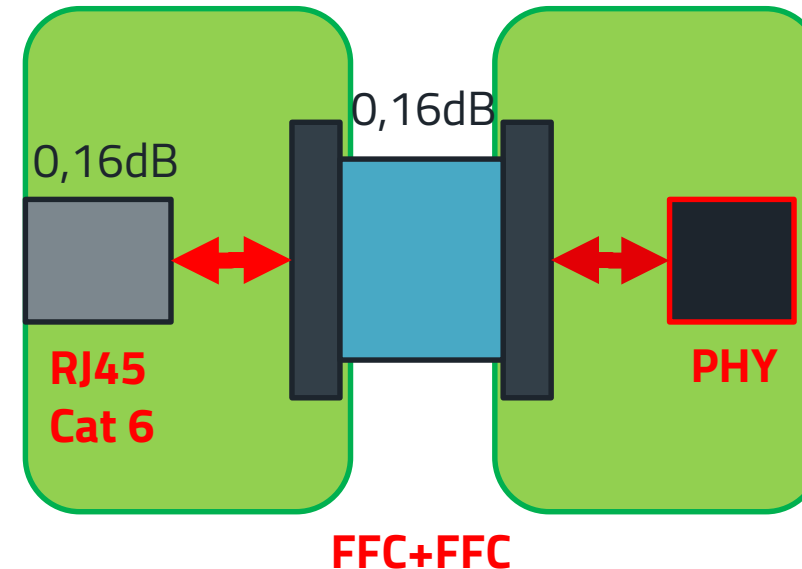
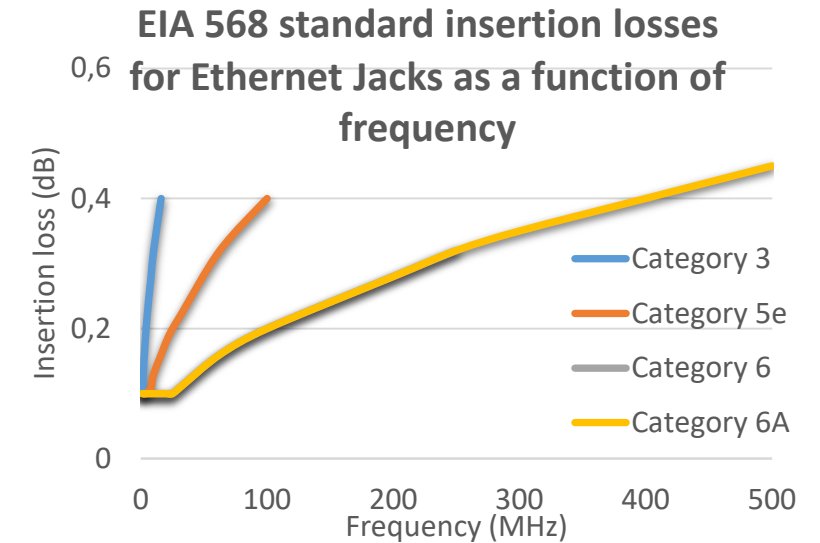


Pin	Signal
1	Ground
2	Line from RJ45 pin 1
3	Line from RJ45 pin 2
4	Ground
5	Line from RJ45 pin 3
6	Line from RJ45 pin 6
7	Ground
8	Line from RJ45 pin 4
9	Line from RJ45 pin 5
10	Ground
11	Line from RJ45 pin 7
12	Line from RJ45 pin 8
13	Ground

# CONNECTORS FOR I/O SIGNAL CHAINS

## Ethernet Interfaces

- Customer example
  - PHY and RJ45 not on the same PCB
  - 100BASE-T (Cat 5)
  - How to link both ?
- ➔ Use a FFC with FPC connectors !
  
- But how ?
  - Use GSSG configuration
  - At least 13 pins
  - Not over 5-10cm
  - 100Ω differential impedance
  
- But isn't there a problem with Ethernet standard?
  - ➔ Use a RJ45 one category higher ! (Cat 6)



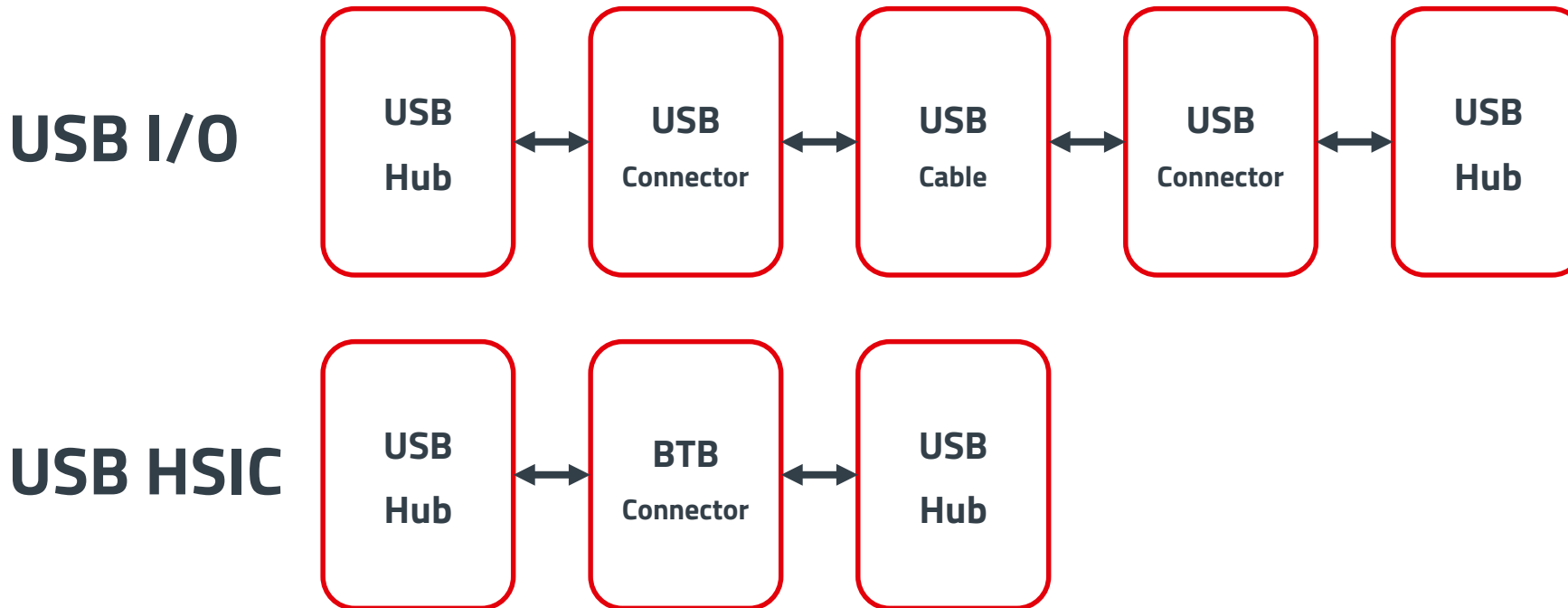
Pin	Signal
1	Ground
2	Line from RJ45 pin 1
3	Line from RJ45 pin 2
4	Ground
5	Line from RJ45 pin 3
6	Line from RJ45 pin 6
7	Ground
8	Line from RJ45 pin 4
9	Line from RJ45 pin 5
10	Ground
11	Line from RJ45 pin 7
12	Line from RJ45 pin 8
13	Ground



# CONNECTORS FOR I/O SIGNAL CHAINS

## USB HSIC

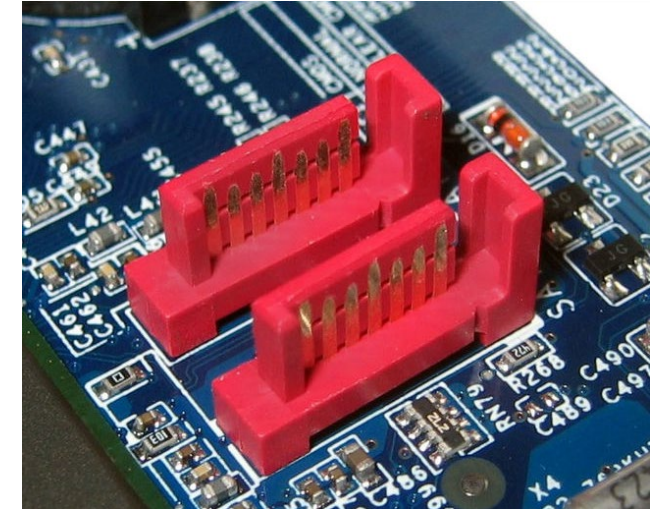
- **USB** can be used as a serial **Board-to-Board** communication protocol
  - Up to **2 high-speed** lanes for transmission and reception in **GSSG**
  - Nyquist Frequency from 2.5 to 10 GHz for SuperSpeed
  - Total allowed losses : 24,5dB



# CONNECTORS FOR I/O SIGNAL CHAINS

## Serial I/O Buses

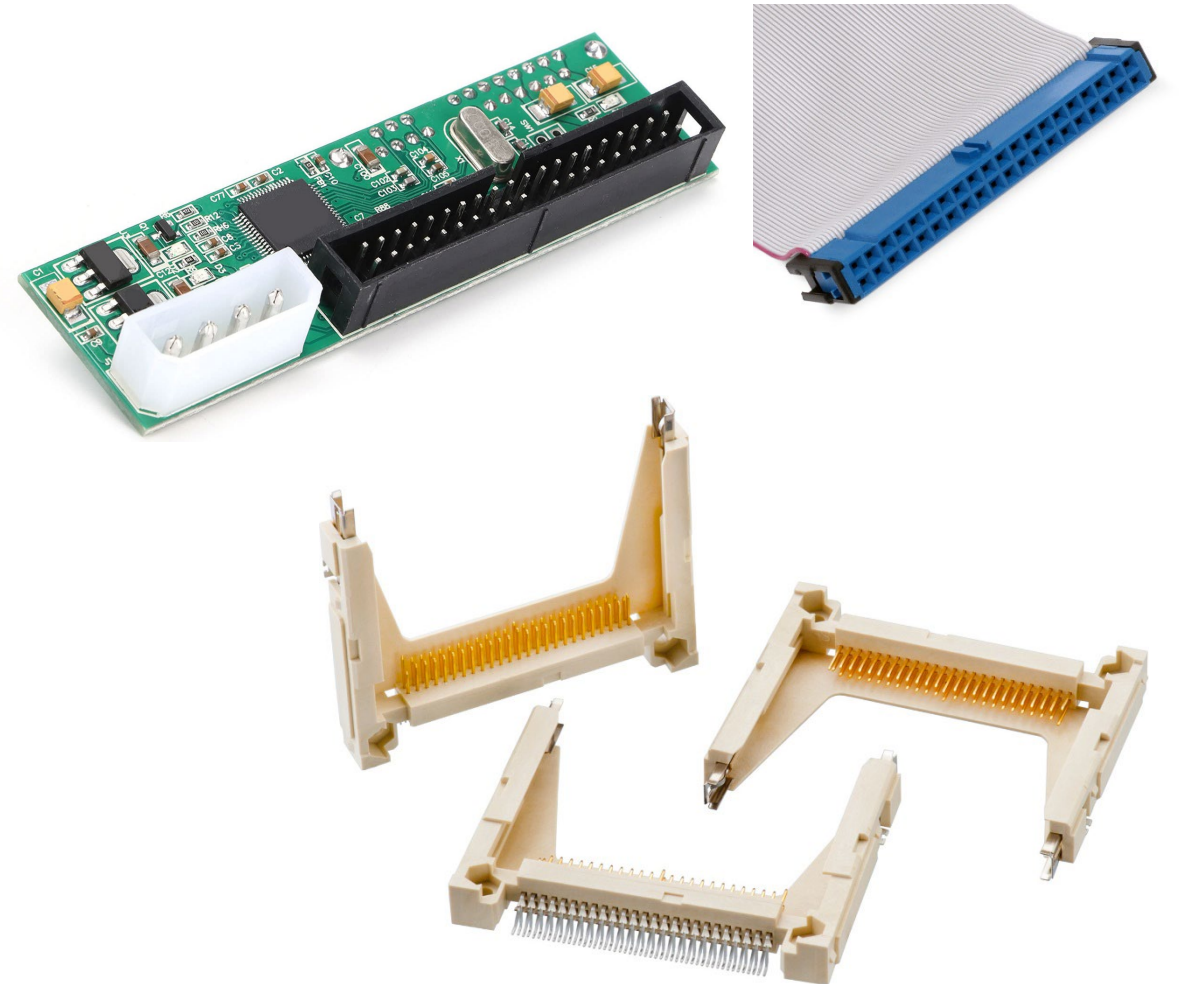
- **Serial bus SATA**
  - Generally for **internal** uses only
  - **One** transmission line, one reception line
  - Flat cable with **GSSG strips**
  - Nyquist Frequency from 1,5 to 6GHz
- High speed serial I/O buses can use **BTB connectors**
- **I2C**
  - 5 to 2500 kHz Nyquist Frequency
  - Most used :
    - 10kB/s (standard mode)
    - 400kB/s (fast mode)
  - Used in a lot of other protocols for inter-chip communication
    - HDMI VGA, DVI, DIMMs, PCI, PCI Express
- Low-speed serial I/O buses can use pin and socket headers



# CONNECTORS FOR I/O SIGNAL CHAINS

## Parallel I/O Buses

- **IDE/PATA**
  - 16 bits wide
  - Sample rate 80MT/s max
  - Bandwidth 1Gb/s max
  - 40-wire Ribbon Flat cable with 40-pins Box Headers
- **CompactFlash/PCMCIA**
  - 16 bits wide
  - Sample rate up to 12,5Mt/s (PCMCIA), up to 80MT/s (CF)
  - Bandwidth up to 200Mb/s (PCMCIA), up to 1,3Gb/s (CF)
  - 50-pin or 68-pin Card Connector



# CONCLUSION

# CONCLUSION

- **Signal chain** analysis is going from the **core** of the system and analyzing the **different protocols** in place
- For us, signal chain analysis is :
  - How to find out **which connectors** customer may need to propose **new solutions** to customers.
  - A framework to **adapt our qualification tests** to give the most accurate information to the customers.
  - A good way to integrate work **with our colleagues**.
- It's always interesting to know and understand the environment in order to propose suitable solutions.



# Questions

& Answers



We are here for you now!  
Ask us directly via our chat or via E-Mail.

[digital-we-days@we-online.com](mailto:digital-we-days@we-online.com)  
[Baptiste.Bouix@we-online.com](mailto:Baptiste.Bouix@we-online.com)