BASIC DESIGN RULES

LAYOUT ACCORDING TO THE WE PARAMETERS AND THE PCB FITS

Andreas Schilpp

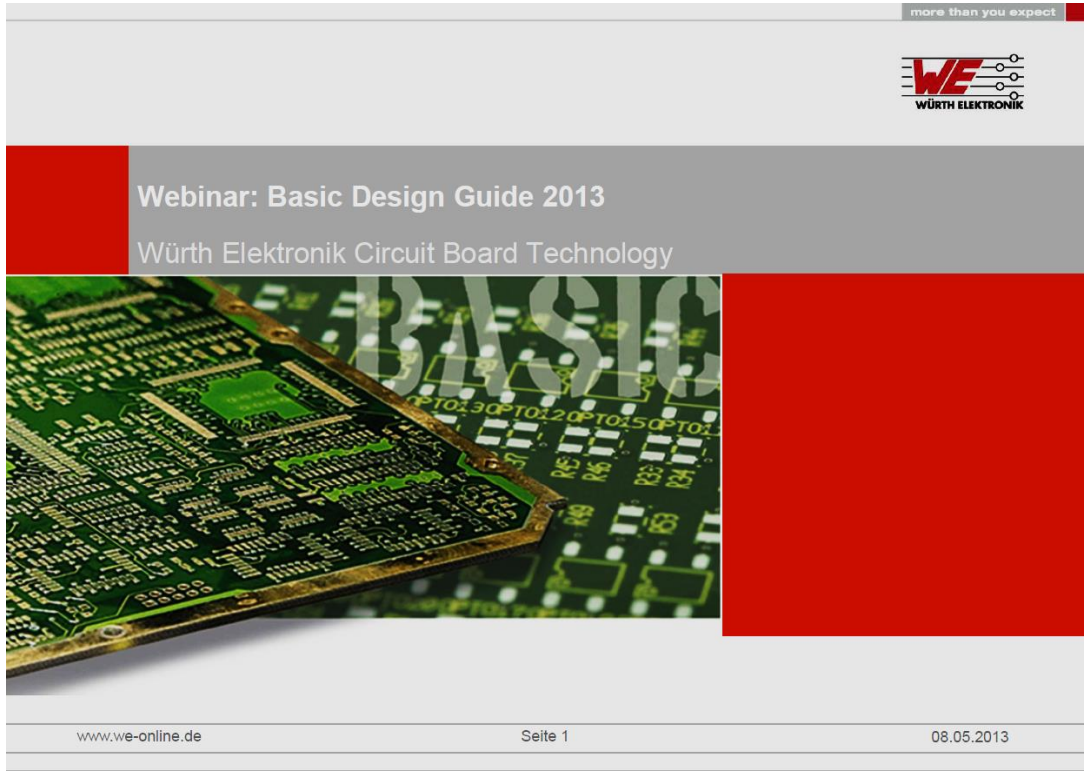
WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

WELCOME TO THE ANNIVERSARY WEBINAR

10 Years of Würth Elektronik PCB Webinars

- The first webinar of your Top 3, originally offered in May 2013, is more current than ever: Recently, the Würth Elektronik BASIC Design Rules have been updated and restructured.

- First webinar: 7 May 2013
- EN: 47 Attendees



AGENDA

BASIC Design Rules: Layout according to the WE parameters and the PCB fits

1. BASIC and standard – what is the difference?
2. Introduction of the new BASIC Design Rules
   - Scope of application
   - Contents
   - What is different?
3. Background information on the changes
   - Processes for copper structuring
   - Specification of copper thickness according to IPC
   - Aspect ratio for holes
4. Application of the BASIC Design Rules – an example

Andreas Schilpp
Technical Marketing

BASIC AND STANDARD – WHAT IS THE DIFFERENCE?

Definitions

STANDARD

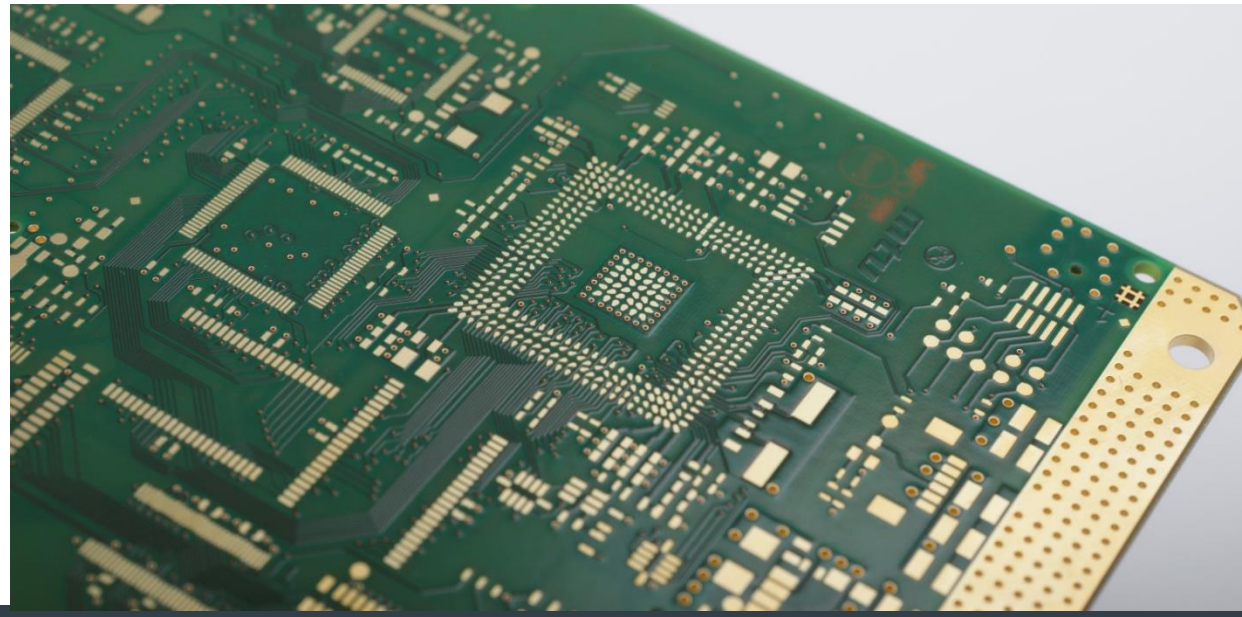
- a category or classification
  - available from all plants
  - at a favorable standard price
  - other categories are
    - Advanced
    - (Leading Edge / State-of-the-Art)
- Standard / Advanced are available in all technologies

Further example for standards

- Standard Stackup
  - Material in stock, processes standardized
  - Standard processes ensure high quality and favorable prices with short delivery times

BASIC

- a technology. By BASIC technology we mean
  - single-sided,
  - double-sided and
  - multilayer printed circuit boards.



TIP
USE STANDARDS

Use of standards:

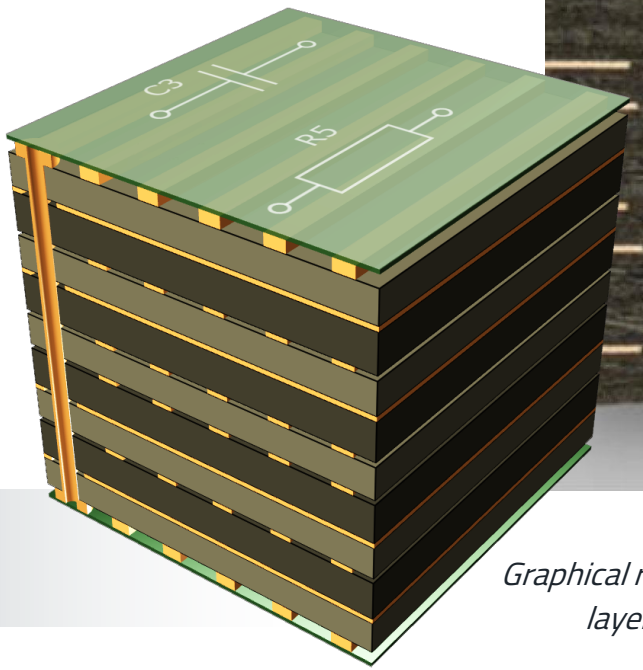
- Standard material
- Material database of the PCB manufacturer (if available)
- Standard layer stackups also digital for import
- Standard design rules
- Standard delivery specification
- Standard packaging
- ...

BASIC TECHNOLOGY – VARIANT MULTILAYER

The third generation in the history of PCBs is characterised by a multilayer structure, created by pressing copper foil, FR4 based copper-clad inner layer cores and pre-pregs.

The obvious additional effort and higher costs are offset by the many advantages:

- More layers to route complex components, such as BGA packages
- Possibility to design power supply systems to improve power integrity and EMC.
- Possibility to design transmission lines with defined impedance to improve signal integrity



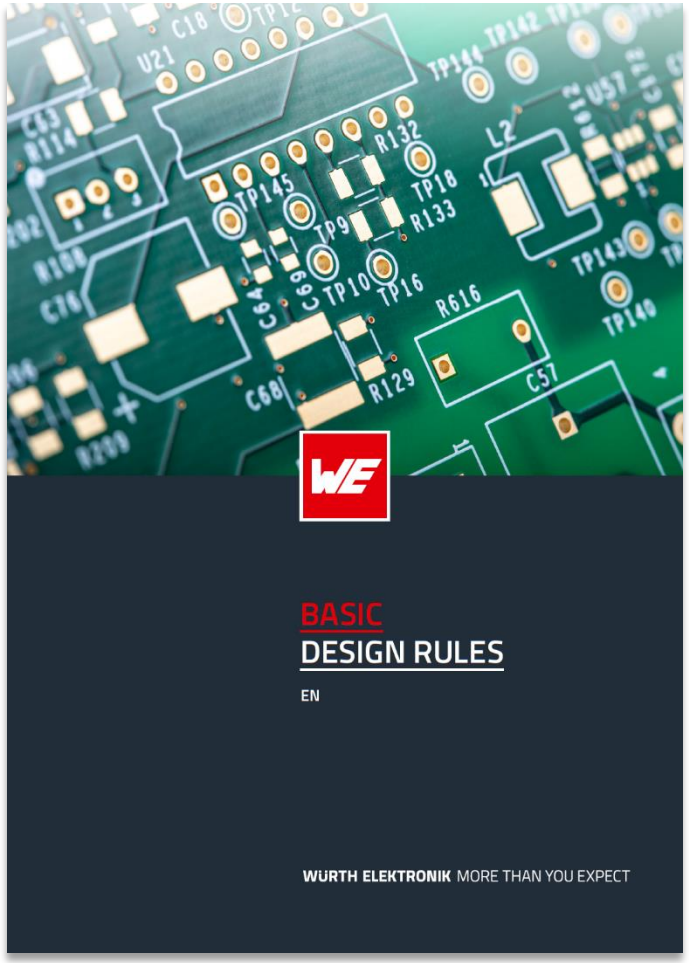
Graphical representation of a multilayer layer stack with 10 copper layers

Microsection

Multilayer PCBs make use of small through hole vias, also known as PTH (plated through holes), to connect layers

NEW BASIC DESIGN RULES

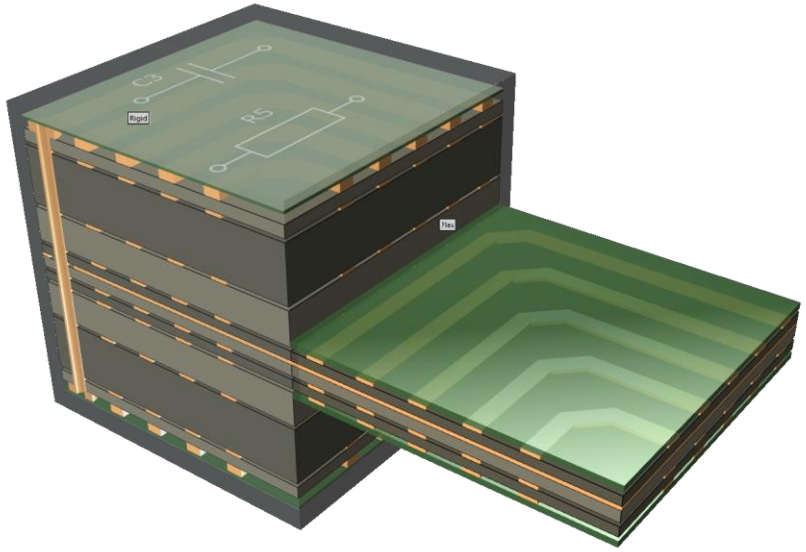
Contents

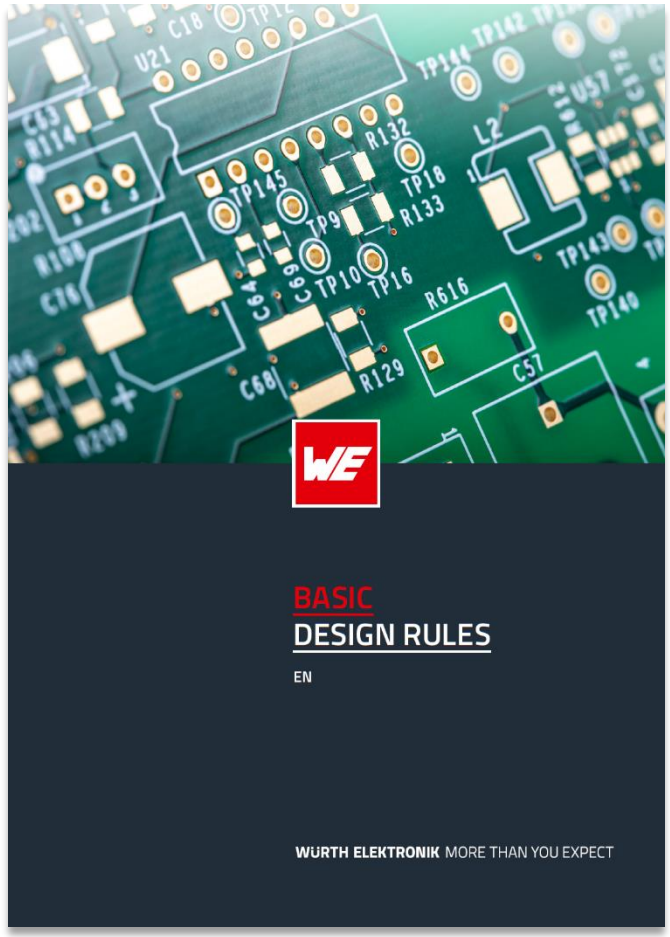


NEW BASIC DESIGN RULES

Scope of application

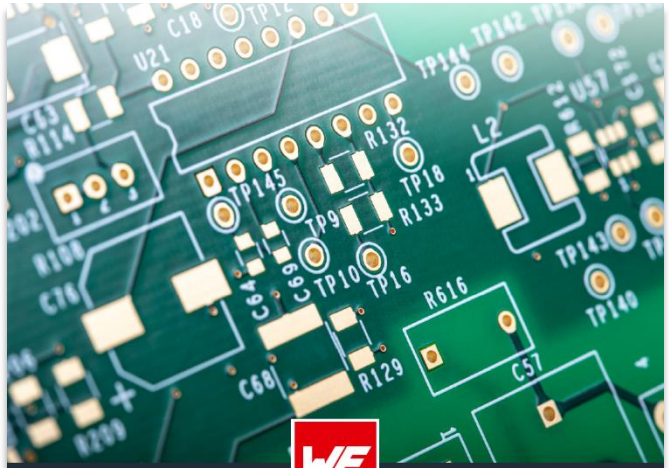
- The BASIC design parameters (copper structures or spacing, holes, solder mask, markings and solder surfaces) are basically valid for all PCB technologies, beyond BASIC for example also for
  - HDI Microvia,
  - Embedding technology or
  - Flex solutions.



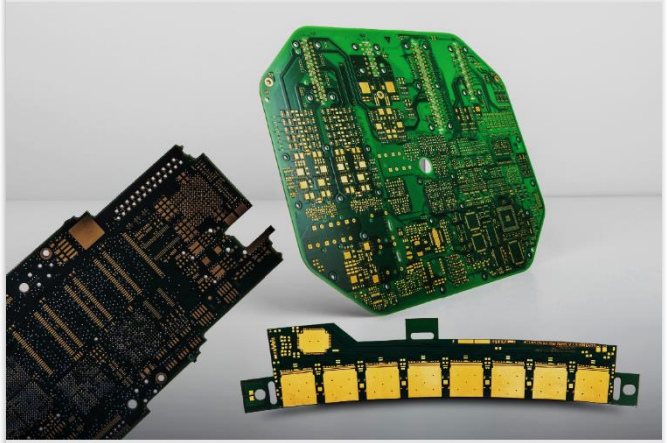


NEW BASIC DESIGN RULES

Flyer



CONTENTS



1 SCOPE OF APPLICATION

These design rules apply in principle to BASIC technology, i.e. for single-sided, double-sided and multilayer PCBs. The design parameters (copper structures or spacing, holes, solder mask, markings and solder surfaces) also apply to all PCB technologies, for example HDI Microvia, Embedding Technology or Flex solutions.

2 BASIC NOTES

a. Please refer to general standards like IPC or IEC.
As standard we manufacture according to IPC-A-600 class 2.
b. Please refer to our **technical delivery specification** (www.we-online.com/tds)
c. Holes in soldering surfaces:
Do not use open holes in soldering surfaces! Keep a distance of at least 400µm distance on both sides from solder pads to holes that are to be plugged (plugged via, IPC type III). For vias according to IPC type VII (filled and capped) please consult us for allowed design rules (conductor spacing)!
d. Plugging und Filling
In our **Design Guide "Plugging/Filling/Tenting"** (https://www.we-online.com/designguidepluggingfillingtenting) we have, in addition to basic definitions of terms, also explained the individual via variants with their respective goals clearly summarized for you. This will help you to find the right solution for each of your applications - within IPC-4761 and beyond.
e. We will be happy to create an optimum delivery panel for you (best price!)

3 BASIC BASE MATERIAL

All base materials used are IPC compliant. Rigid base materials are specified in IPC-4101 and its specification sheets. For standard FR-4.0 with Tg135, for example, specification sheet 21 applies, higher grade FR-4.1 for example in specification sheets 128 (92, 94, 127) for elevated operating temperatures with Tg150 and low CTE (Coefficient of Thermal Expansion). Our portfolio is rounded off with CEM-1 materials (specification sheets 10, 12, 14, 15, 81) and CEM-3 materials (specification sheets 16, 35).

4 BASIC STANDARD STACKUPS

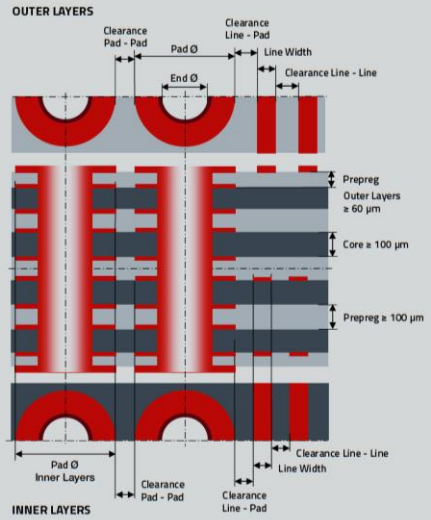
For the BASIC technology, we offer **standard stackups** on our website that are usual in the market and cost-optimized. Here you will also find all standards as digital stackup files for import into your EDA software. You can use these standards as a basis for your solutions and modify them according to your requirements.

NEW BASIC DESIGN RULES

Flyer

5 COPPER STRUCTURES, SPACINGS

a. The conductor spacing, more generally the "copper spacing", is crucial for the production of the copper structures. This affects all features such as trace-trace/trace-shape/shape-trace/shape-shape/trace-all pin pads/ trace-all Via pads/trace-all non signal geometries/ etc.
b. For the design of the conductor width, criteria such as current carrying capacity, permissible tolerances and other specifications apply.
c. In principle, the conductor width can also be larger or smaller than the conductor spacing.
Example: conductor width/conductor spacing (line/space) 80µm/120µm is easier to manufacture than 100µm/100µm.
d. Minimum conductor widths:
i. The minimum allowed conductor width is 60µm, for impedance defined structures smaller than 75µm please consult us.
ii. UL marking for conductor widths <4mil is partly only possible according to UL-94. For conductor widths ≥4mil, marking according to UL-94 and UL-796 is possible. We ask for your consultation.



Outer layers – conductor spacing

Starting foil thickness	Minimum copper thickness[1]		Minimum conductor spacing Standard	Minimum conductor spacing Advanced	Minimum possible line width
	IPC-class 1, 2	IPC-class 3			
8,5 µm [1/4 oz.][2]	26,2 µm	31,2 µm	100 µm	75 µm	60 µm
12 µm [3/8 oz.][2]	29,3 µm	34,3 µm	100 µm	80 µm	60 µm
17,1 µm [1/2 oz.]	33,4 µm	38,4 µm	120 µm	100 µm	60 µm
34,3 µm [1 oz.]	47,9 µm	52,9 µm	180 µm	160 µm	120 µm
68,6 µm [2 oz.]	78,7 µm	83,7 µm	275 µm	225 µm	125 µm
102,9 µm [3 oz.]	108,6 µm	113,6 µm	390 µm	320 µm	150 µm

1) IPC-6012E-EN Table 3-15: External Conductor Thickness after Plating
2) Extra cost: No standard copper foil

Inner layers - conductor spacing

Starting foil thickness	Minimum copper thickness[3]		Minimum conductor spacing Standard	Minimum conductor spacing Advanced	Minimum possible line width
	IPC-class 1, 2, 3				
17,1 µm [1/2 oz.]	11,4 µm		100 µm	75 µm	60 µm
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102,9 µm [3 oz.]	86,6 µm		250 µm	225 µm	175 µm

3) IPC-6012E-EN Table 3-14: Internal Layer Foil Thickness after Processing

6 DRILLS, DRILL PADS, ANNULAR RINGS, CLEARANCES

Plated Through Holes

Pad size	Remark	Aspect Ratio[1]	Drill tool diameter	Finished hole diameter	Tolerance (Standard)	Copper clearance plane on inner layer without Pad
0,60 mm	Standard	8:1	0,35 mm	0,25 mm	+0,1/-0,05 mm	≥ 0,80 mm
0,55 mm			0,30 mm	0,20 mm		≥ 0,75 mm
0,50 mm (Cu max. 35 µm)	Max. ca. 12 layers Max. ca. 1,80 mm PCB thickness		0,25 mm	0,15 mm		≥ 0,70 mm
0,45 mm (Cu max. 35 µm)	For less complex Layer stackups		0,25 mm (0,20 mm)	0,15 mm		≥ 0,70 mm

1) Aspect Ratio" for drill holes: Ratio of drill hole length or depth to drill hole tool diameter.
For further information, see technical delivery specification chapter 3.7.1.

a. Drill diameter
The PCB design specifies the via design by defining the via hole size and the via pad size. The hole size in the manufacturing data represents the final diameter that is specified for the finished PCB. For the drill tool (drill tool diameter), a larger diameter is always selected for the drilling tool (drill tool diameter), because the hole diameter becomes smaller after drilling due to the deposition of copper and solder surface in the hole barrel. Therefore, the pad size must also not be selected too small.

b. Spacing between holes

Minimum distances between holes (based on final diameter)	
Hole-to-hole clearance same potential	300µm
Hole-to-hole clearance different potential	500µm
Distance NPTH-NPTH (Non Plated Through Hole)	350µm

c. Copper layer thicknesses in PTHs, blind and buried vias
see IPC-6012E-EN, Tables 3-4ff: Minimum Requirements for Surface and hole copper Plating.

NEW BASIC DESIGN RULES

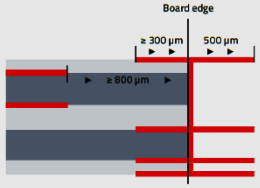
Flyer

7 EDGE PLATING

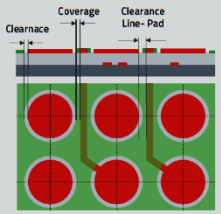
We offer edge metallization (sideplating) for the edges of your printed circuit boards. For a correct production we ask you to observe the design parameters:

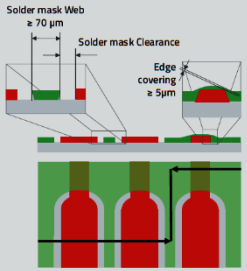
In your layout data, the PCB edge to be metallized must be designed with 500µm protruding copper and at least 300µm connection to the edge.

Layers that are not to be connected should have a clearance of min. 800µm on the outer contour.



8 SOLDER MASK





Solder Mask		
	Standard	Advanced
Clearance	≥ 50 µm	35 µm
Coverage	50 µm	40 µm
Solder mask web	≥ 70 µm	–
Via-opening	final diameter +0.25 mm	

Manufacture without solder mask clearances involves additional effort and is not recommended due to quality reasons.

Our standard for soldermask is green photosensitive soldermask that meets the requirements of IPC-SM-840 Class T and H. Other colors such as white, black, blue, red or yellow can also be applied on request. Depending on the production location, the execution is as a colored solder mask instead of the green solder mask or as an additional print over the standard green solder mask. Please ask for these options, we will provide you with a quote.

9 PEELABLE MASKING

A peelable protective solder resist for protecting drill holes or assembly pads in wave soldering processes is applied by screen printing.
Coating thickness = 300 µm +/-200 µm (special tolerances possible after clarification). 1 mm circumferential distance to solder structures not to be covered (special tolerances possible after clarification).

10 MARKINGS

Markings (Legend Print)	Standard	Advanced
Clearance Silkscreen to copper (Viapads, SMDpads, conductor)	300 µm	
Clearance Silkscreen to NPTH Bore rim	300 µm	
Minimum line width an length of Print	150 µm	100 µm (white)
Clearance between markings	200 µm	

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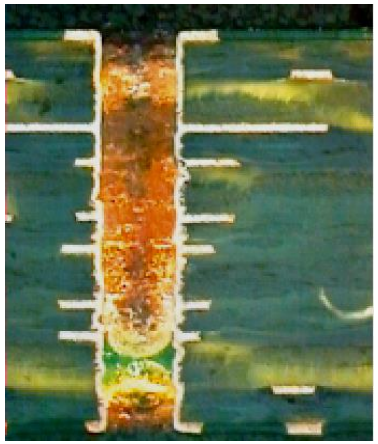
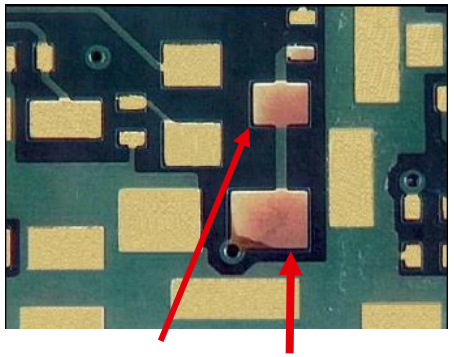
8 SOLDER MASK

- Laquer residues in via holes



- Follow-up error ENIG Surface



BASIC DESIGN RULES: LAYOUT ACCORDING TO THE WE PARAMETERS

Poll: Multiple choice with only one correct answer

What has the greatest influence on the minimum copper spacing (subtractive etching technique on inner layers)?

- Number of layers
- Thickness of the copper foil
- Thickness of the electroplated metallization
- Total thickness of copper foil and electroplated metallization
- Prepreg thickness

NEW BASIC DESIGN RULES

Flyer: What is new?

5 COPPER STRUCTURES, SPACINGS

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   Example: conductor width/conductor spacing (line/space) 80 µm / 120 µm is easier to manufacture than 100 µm / 100 µm.
d. Minimum conductor widths:
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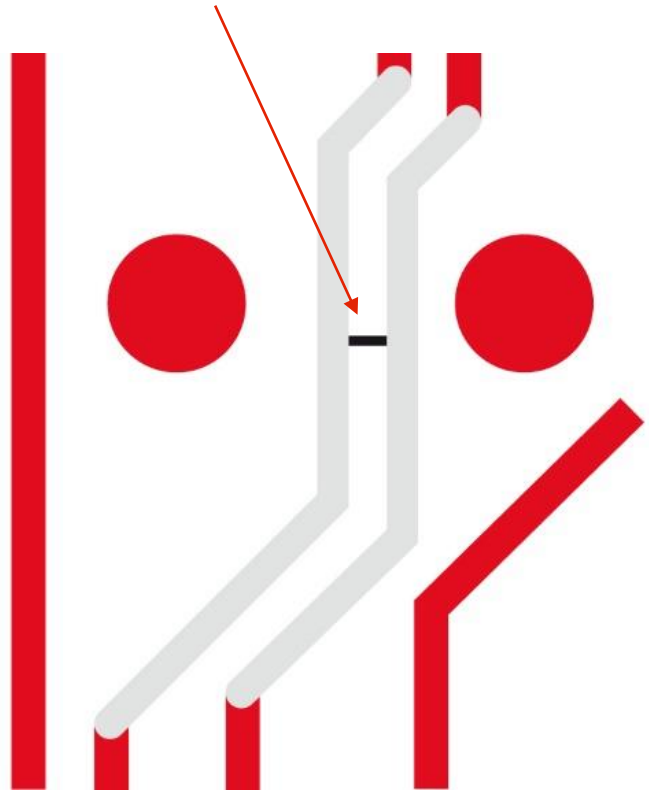
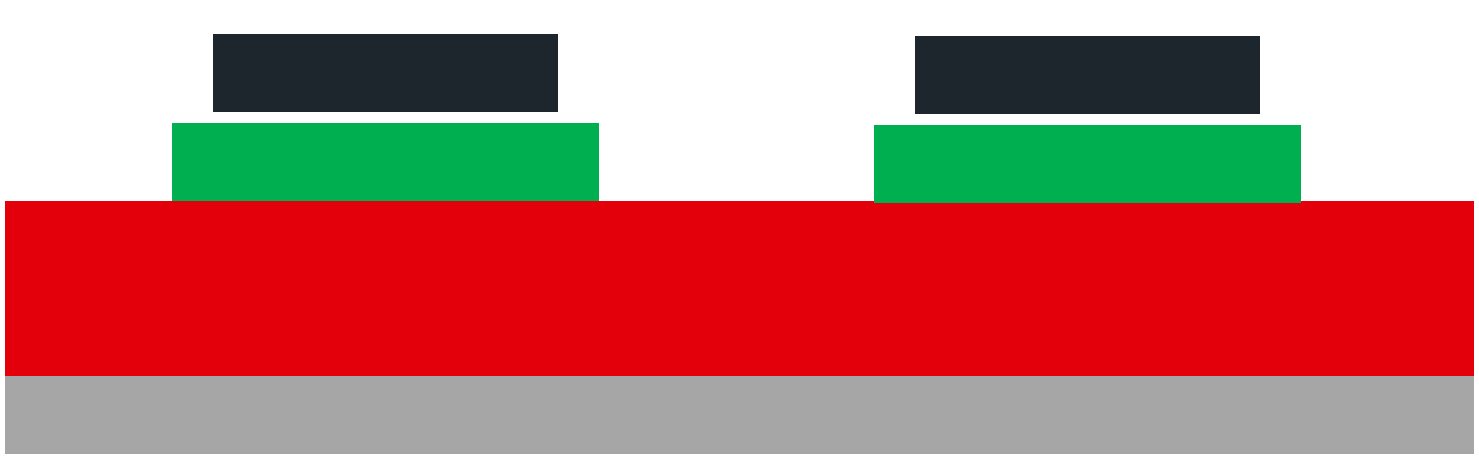
   ii. UL marking for conductor widths <4 mil is partly only possible according to UL-94. For conductor widths ≥ 4mil, marking according to UL-94 and UL-796 is possible. We ask for your consultation.

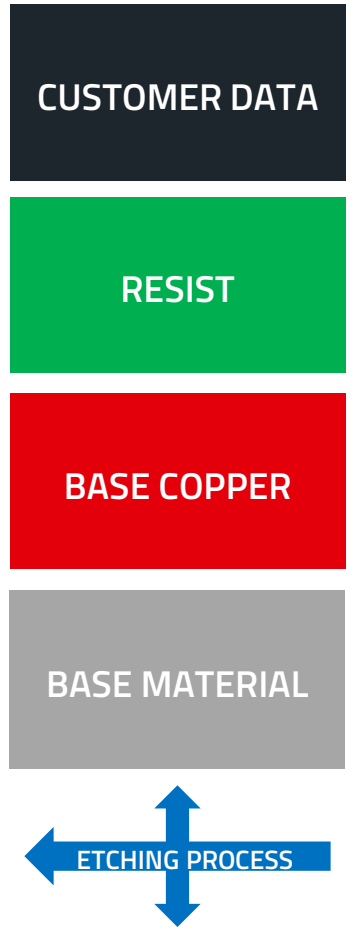
- Feature to Feature Spacing



BASICS: COPPER STRUCTURING

Inner layers: Imaging positive + etching subtractive





NEW BASIC DESIGN RULES

Flyer: What is new?

5 COPPER STRUCTURES, SPACINGS

- Table for inner layers

Inner layers - conductor spacing					
Starting foil thickness	**Minimum copper thickness[3]**		**Minimum conductor spacing Standard**	**Minimum conductor spacing Advanced**	**Minimum possible line width**
	IPC-class 1, 2, 3				
17,1 µm [1/2 oz.]	11,4 µm		100 µm	75 µm	60 µm
34,3 µm [1 oz.]	24,9 µm		120 µm	100 µm	60 µm
68,6 µm [2 oz.]	55,7 µm		180 µm	150 µm	125 µm
102,9 µm [3 oz.]	86,6 µm		250 µm	225 µm	175 µm
3) IPC-6012E-EN Table 3-14: Internal Layer Foil Thickness after Processing					

BASICS: COPPER STRUCTURING

Outer layers: Imaging negative + copper deposition selective + etching base copper

CUSTOMER DATA

TIN RESIST

PHOTORESIST

COPPER PLATING

BASE COPPER

BASE MATERIAL

ETCHING PROCESS

NEW BASIC DESIGN RULES

Flyer: What is new?

5 COPPER STRUCTURES, SPACINGS

- Table for outer layers

Outer layers – conductor spacing					
Starting foil thickness	**Minimum copper thickness[1]**		**Minimum conductor spacing Standard**	**Minimum conductor spacing Advanced**	**Minimum possible line width**
	IPC-class 1, 2	IPC-class 3			
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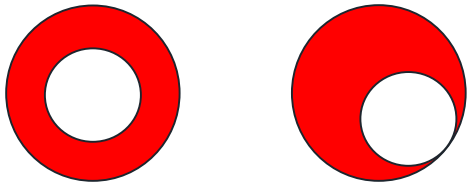
102,9 µm [3 oz.]	108,6 µm	113,6 µm	390 µm	320 µm	150 µm
1) IPC-6012E-EN Table 3-15: External Conductior Thickness after Plating					
2) Extra cost: No standard copper foil					

BASICS: PTHS AND VIAS

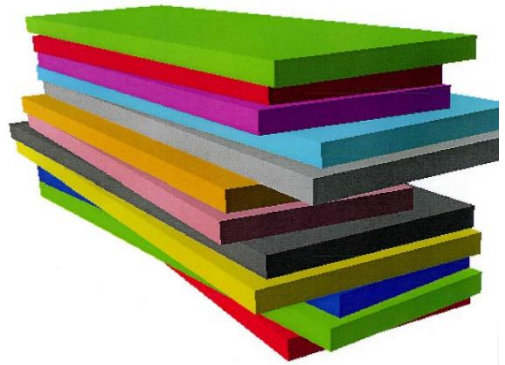
Why are annular rings needed around via holes?

- Relationship between via pad size, registration and drill diameter
  - Annular ring specifications of IPC classes (see IPC-2221)
  - Influence of the drill tool: deflection
  - Influence of the machine
  - Layout-dependent shrinkage/expansion values: Offset of layers relative to each other
- Ideal versus real



- Important for the drill diameter: Aspect ratio - next slide

6 DRILLS, DRILL PADS, ANNULAR RINGS, CLEARANCES



BASICS: PTHS AND VIAS

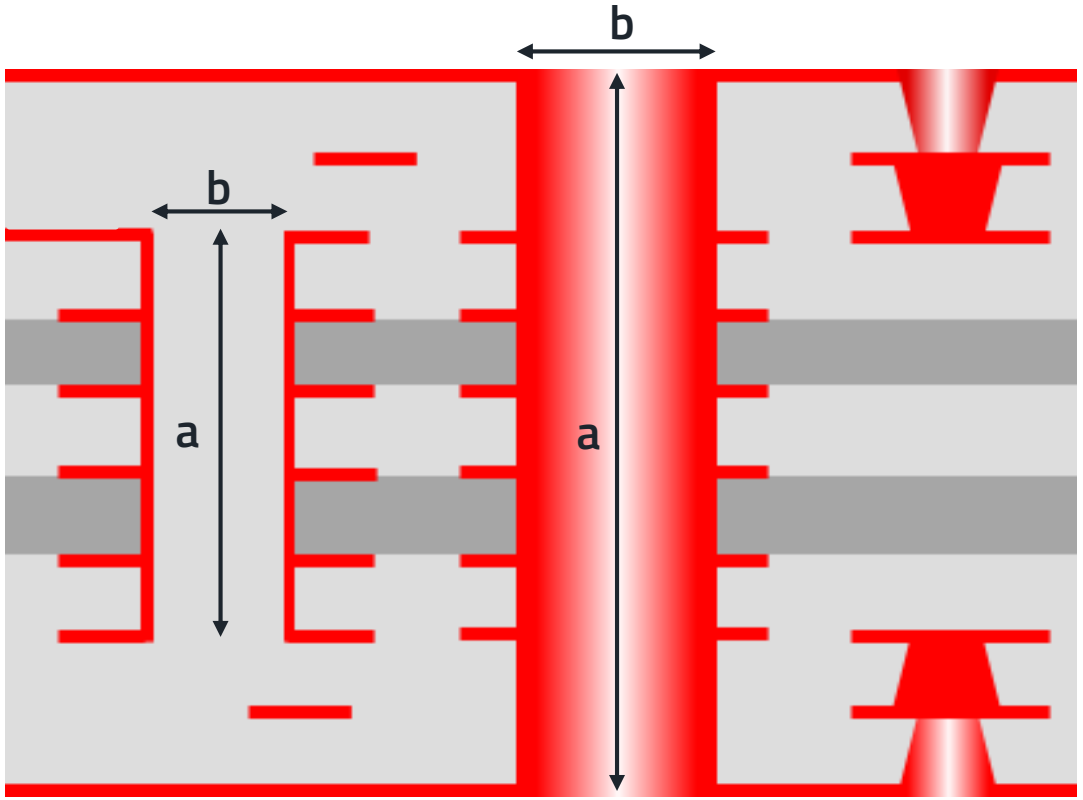
Aspect Ratio

- Ratio drill-diameter b – drill depth a
- PTH & BV: max. 1:8

- Important for a complete and even copper build-up in the barrel.

Example PTH:
b = ?
a = 1.6mm
b = a / 8 = 0.20mm
→ Smallest drill-Ø = 0.20mm
→ Smallest pad-Ø = 0.45mm

6 DRILLS, DRILL PADS, ANNULAR RINGS, CLEARANCES



BASICS: PTHS AND VIAS

6 DRILLS, DRILL PADS, ANNULAR RINGS, CLEARANCES

Table

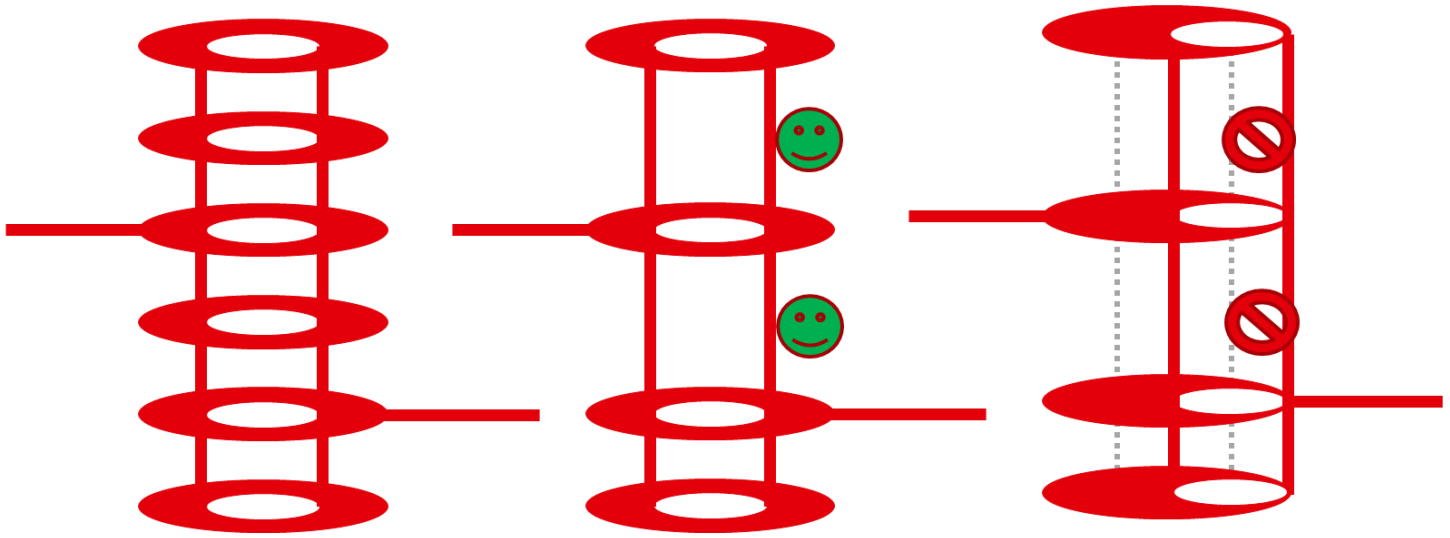
Plated Through Holes						
Pad size	**Remark**	**Aspect Ratio[1]**	**Drill tool diameter**	**Finished hole diameter**	**Tolerance (Standard)**	**Copper clearance plane on inner layer without Pad**
0,60 mm	**Standard**	8:1	0,35 mm	**0,25 mm**	+0,1/-0,05 mm	≥ 0,80 mm
0,55 mm			0,30 mm	**0,20 mm**		≥ 0,75 mm
0,50 mm (Cu max. 35 µm)	Max. ca. 12 layers Max. ca. 1,80 mm PCB thickness		0,25 mm	**0,15 mm**		≥ 0,70 mm
0,45 mm (Cu max. 35 µm)	For less complex Layer stackups		0,25 mm (0,20 mm)	**0,15 mm**		≥ 0,70 mm

1) Aspect Ratio" for drill holes: Ratio of drill hole length or depth to drill hole tool diameter.
For further information, see technical delivery specification chapter 3.7.1.

BASICS: PTHS AND VIAS

Why do you need copper releases in ground inner layers without a pad?

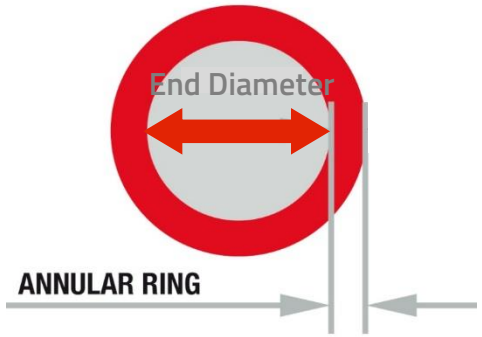
- Non-used / non-functional pads:



- Pad removal does not add space on inner layers because tolerances, offset and deflection are real and permissible.
- A design rule check must be performed before pad removal!
- The total clearance is pad size plus minimum copper clearance!

6 DRILLS, DRILL PADS, ANNULAR RINGS, CLEARANCES

- Annular ring

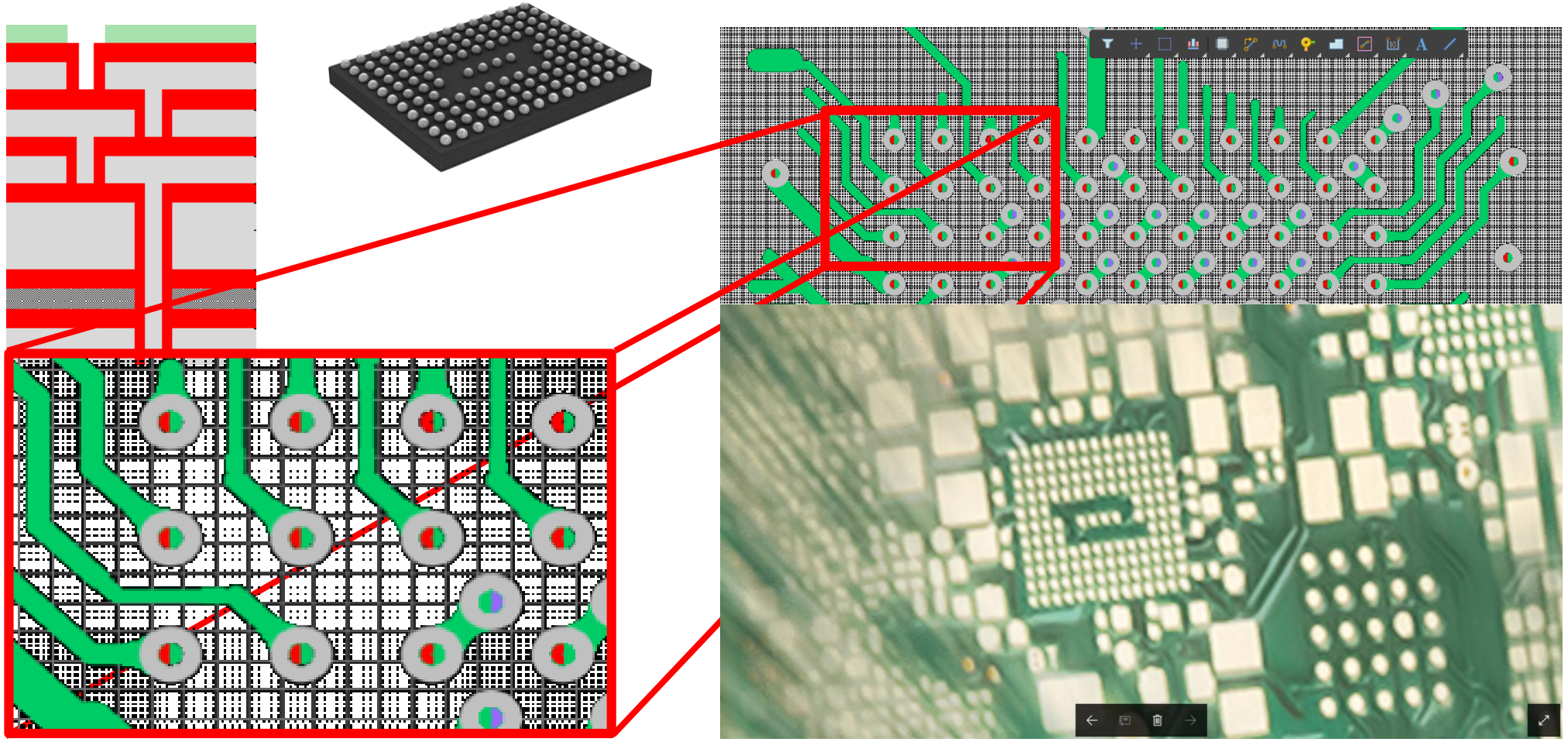


- **ATTENTION** with RIGID.flex: Do NOT remove non-used / non-functional via pads on flex layers for reliability reasons!

BASIC DESIGN RULES: LAYOUT ACCORDING TO THE WE PARAMETERS

Usage of table for UFBGA 7X7X0.6 169L P 0.5mm

TOP
Layer 2
Layer 3
Layer 4



BASIC DESIGN RULES: LAYOUT ACCORDING TO THE WE PARAMETERS

Poll: Multiple choice with only one correct answer

Please rate the BASIC Design Rules: How many points on a scale of 1 to 10 do you give the document?

- 1 to 2 points (unusable)
- 3 to 4 points (incomplete and incorrect)
- 5 to 6 points (ok, but incomplete)
- 7 to 8 points (good, helpful, understandable)
- 9 to 10 points (almost perfect, I use it often)

NOTES

→ Participants with a rating of less than 5 points I will contact in writing after the webinar (this is not a threat, but a partnership offer!)

→ Feel free to write me errors, additions and optimizations in the question field

SUMMARY

New BASIC Design Rules

- BASIC is a technology
- Standard is a category or classification
- Conductor spacing is important for PCB manufacture
- Conductor width and conductor spacing should be considered independently of each other. Different values should be considered at least locally.
- Annular rings around via holes are still necessary
- Non-used pad removal does not save space

- Würth Elektronik Webinars – more than you expect!


MANY THANKS
FOR YOUR
ATTENTION!