HELLO TÜRKIYE 2026

WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

ONE STOP SHOP; A MEASUREMENT APPROACH TO PRACTICAL DESIGN FOR EMC

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WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

Agenda

- DC/DC Filter Architecture
- Boost Debugging Example
- SEPIC Snubber Design and Measurement

DC/DC FILTER ARCHITECTURE

NOISE PROPAGATION

CM & DM Noise Currents

- Differential mode current (DM)
  - Current path as in the schematic
  - Easier to understand the noise paths
  - High currents, di/dt and dv/dt
  - Conducted EMI problems

- Common mode current (CM)
  - Current path unexpectedly
  - Return current path very big
  - Relative low currents (some µA)
  - Radiated EMI problems

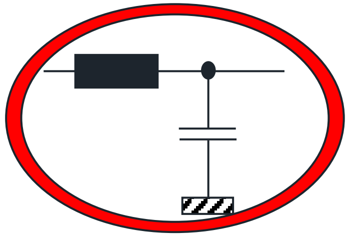
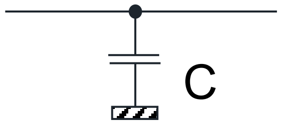
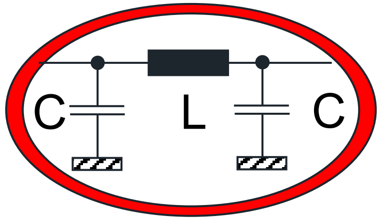
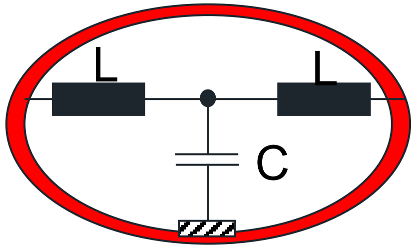
ARCHITECTURE

DESIGN CONSIDERATIONS

- Multiple stages
- Considers Conducted and Radiated Emissions/Immunity
- Accounts for Common mode and Differential mode transmission
- Includes OVP (ESD/EFT/Surge)
- Considers Layout and Tracking
- Considers practical component and functional shortfalls

ARCHITECTURE

DIFFERENTIAL FILTER TOPOLOGIES

Source Impedance		Load Impedance
low		high
high		high
high or unknown		high or unknown
low		low
low or unknown		low or unknown

→ **small C = higher SRF**

Choose ferrite bead

= build no resonance with C

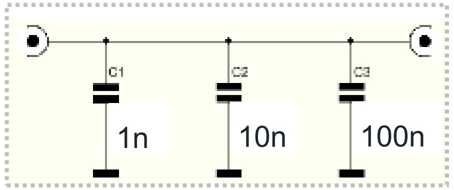
= broadband filter

Pay attention to:

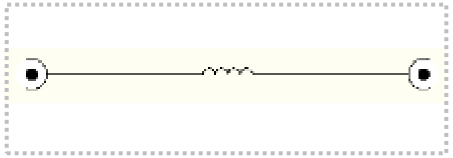
SRF of used components

Filter topologies – Demo board

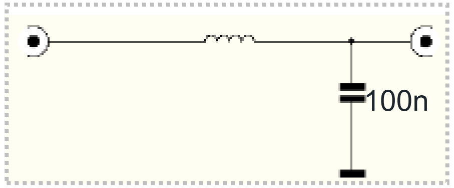
- Parallel-C-filter



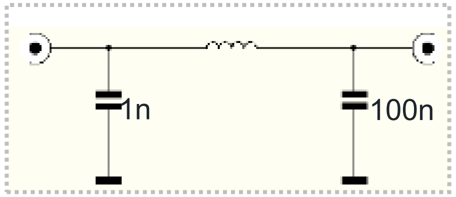
- L-filter



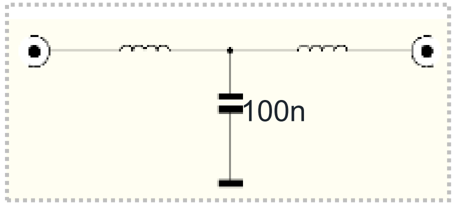
- LC-filter

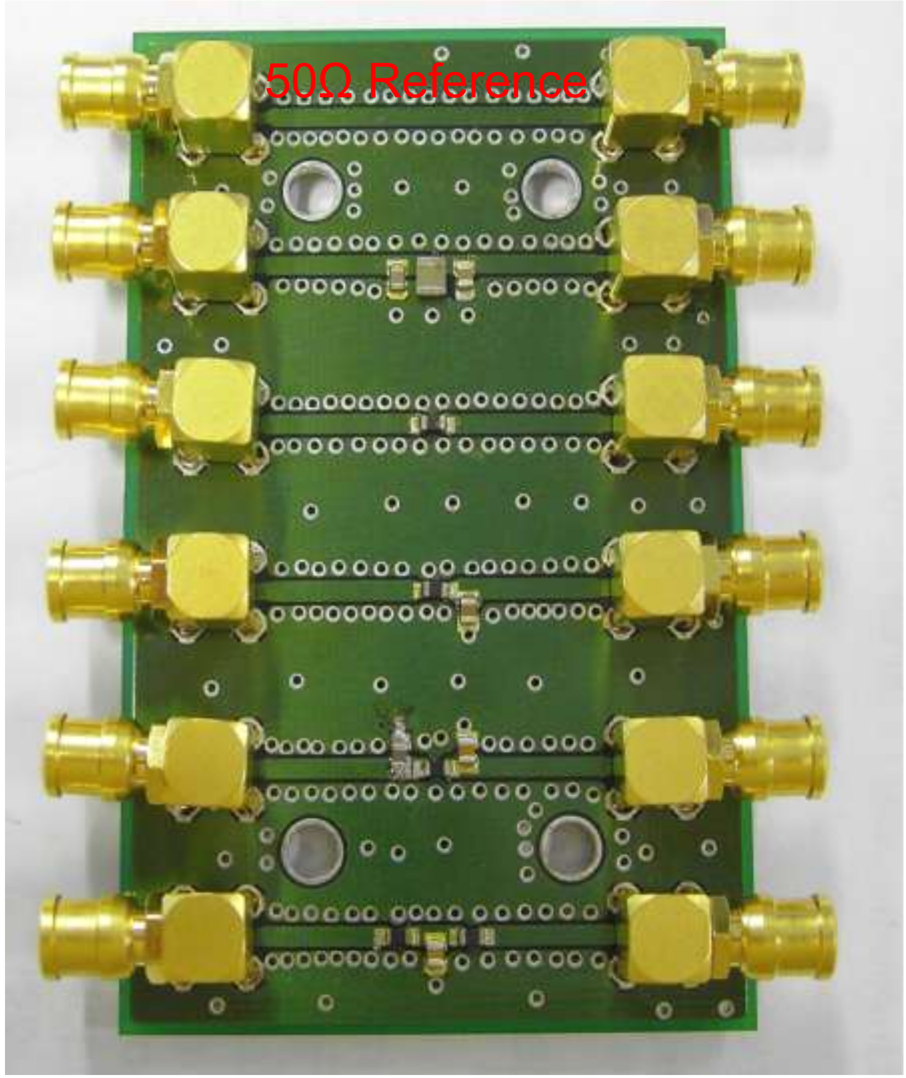


- Π-filter

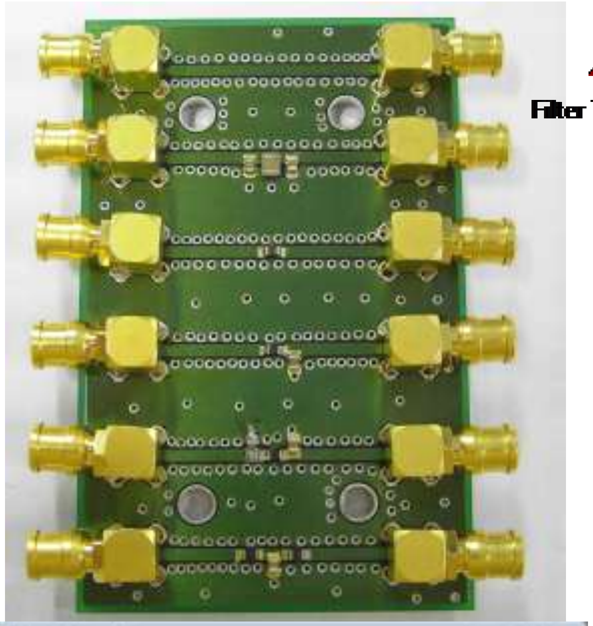


- T-filter

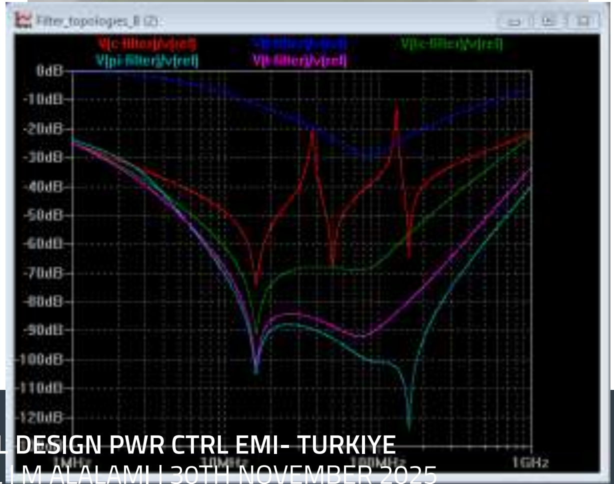


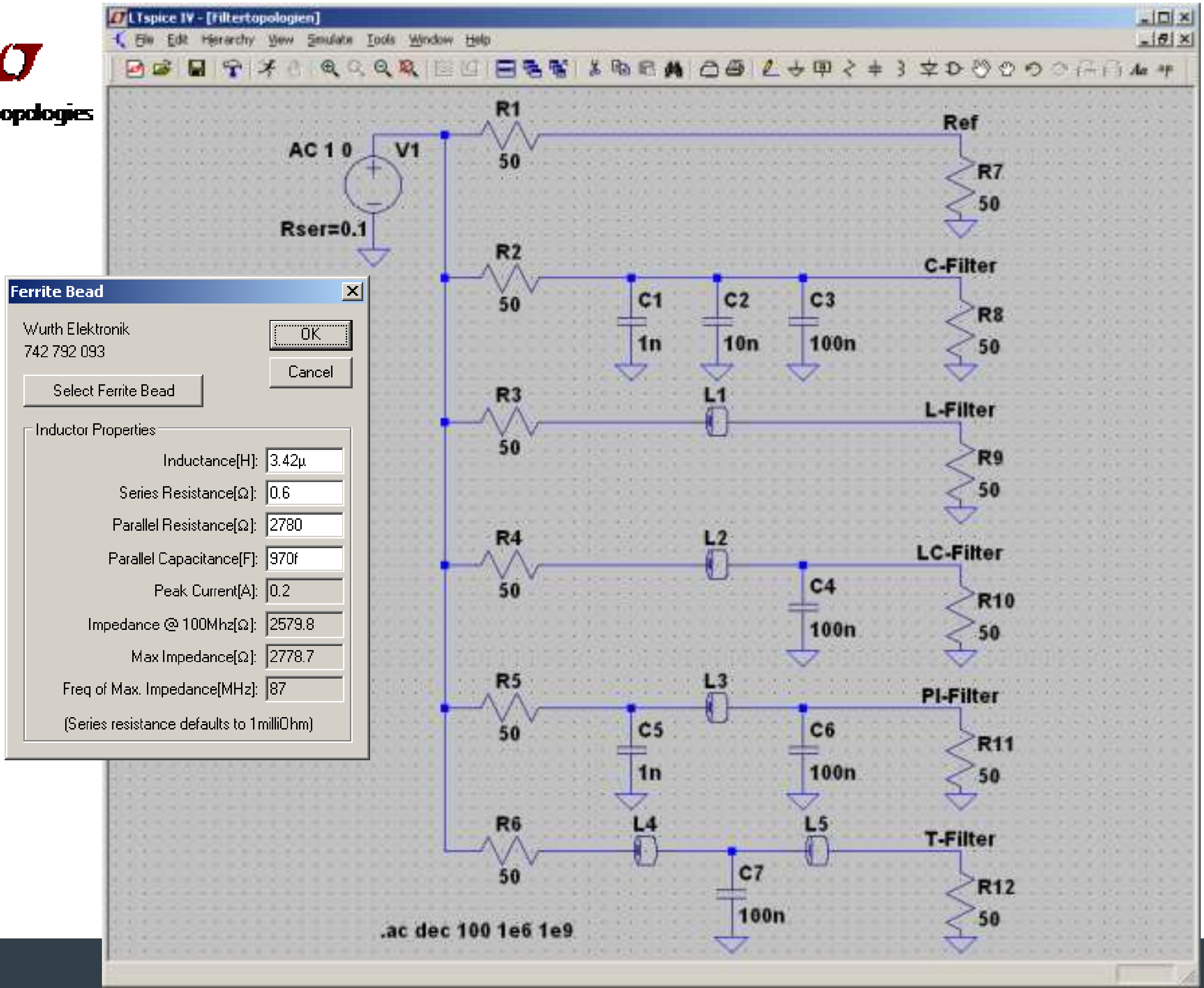


Filter Topologies – LT Spice Simulation



Filter Topologies

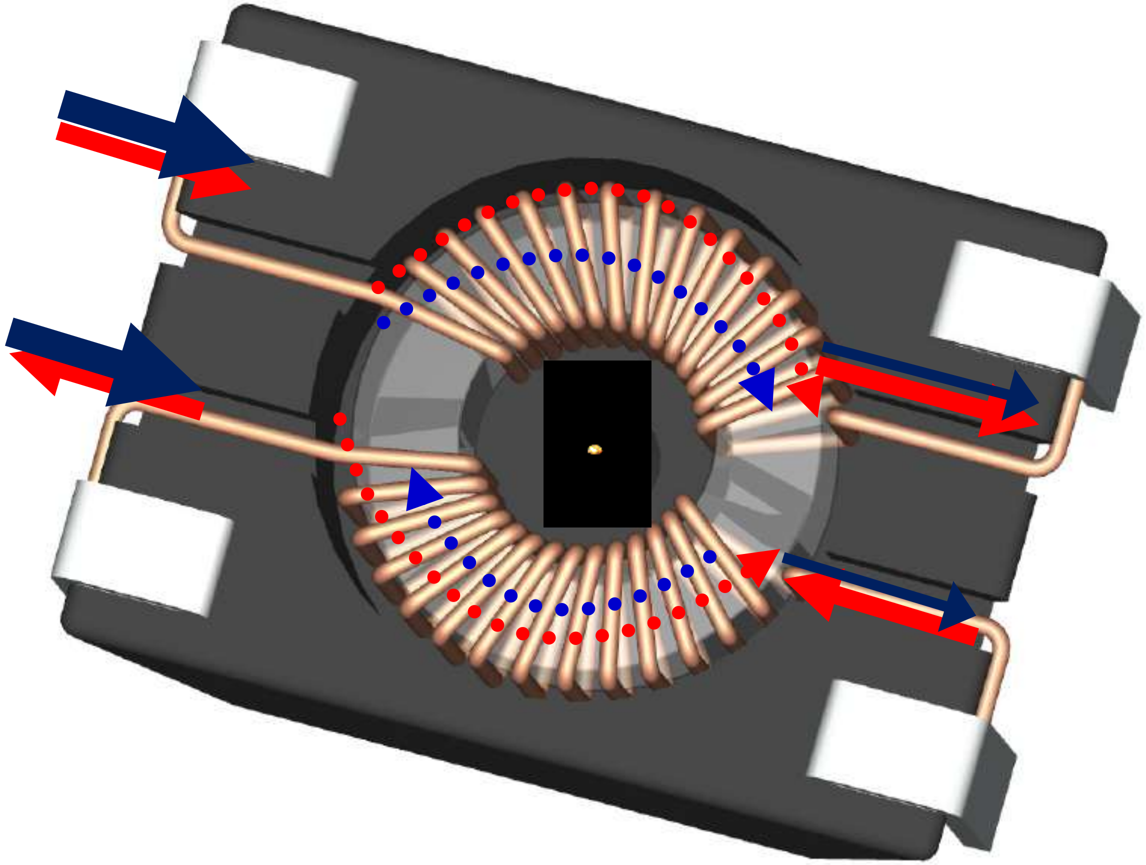




ARCHITECTURE

COMMON MODE CHOKE – PRINCIPLE OF OPERATION

- It is a Bi-directional filter
  - From device to outside environment
  - From outside environment to inside device



- Intended Signal - Differential mode
- Interference Signal (noise) – Common Mode

- Conclusion:
  - “almost” no affect the signal - Differential mode
  - high attenuation to the interference signal (noise) – Common Mode

SELECTION

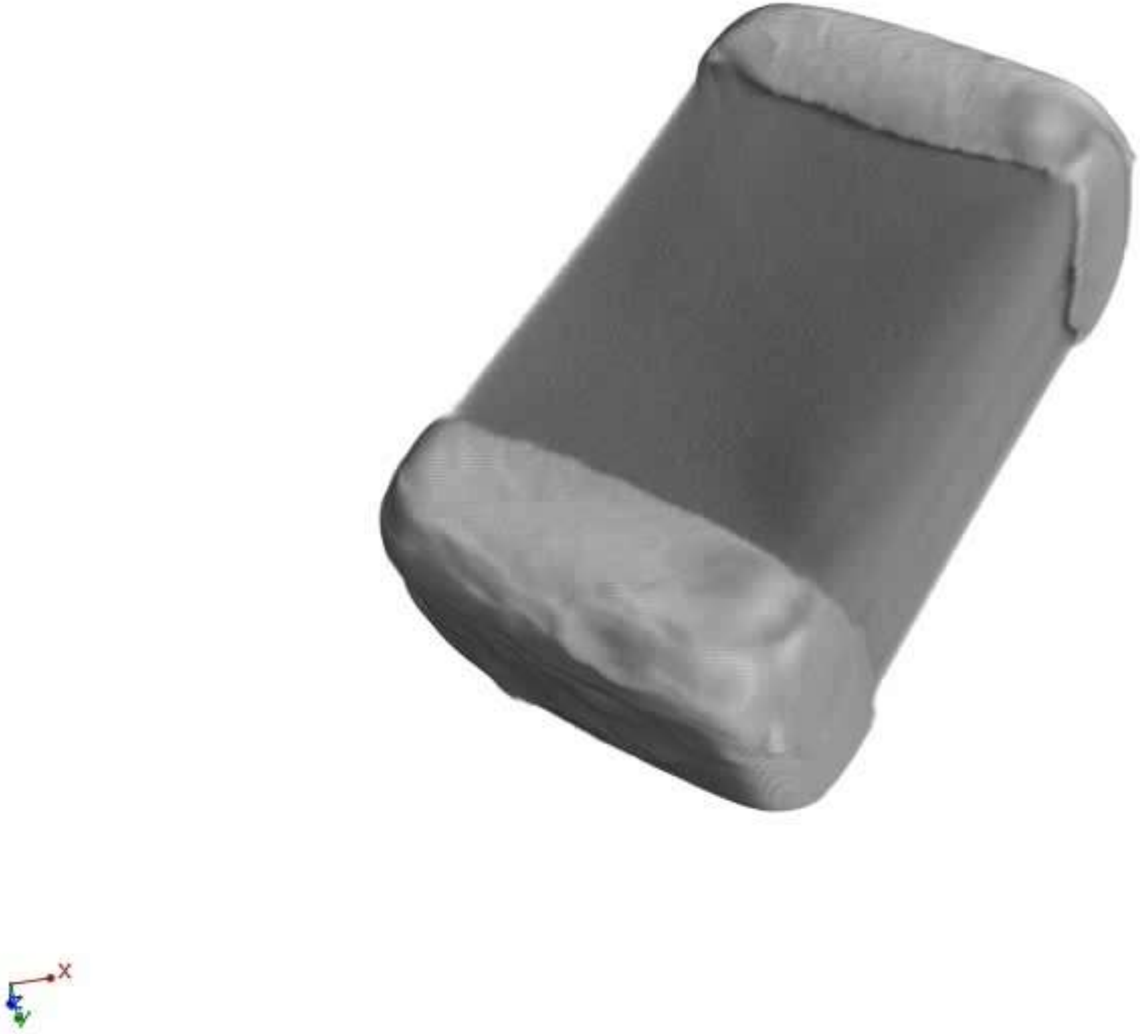
SELECTION

COMPONENT SELECTION CONSIDERATIONS

- DC Bias Effect
- Impedance vs Frequency
- Pulsed / Inrush Current

SELECTION

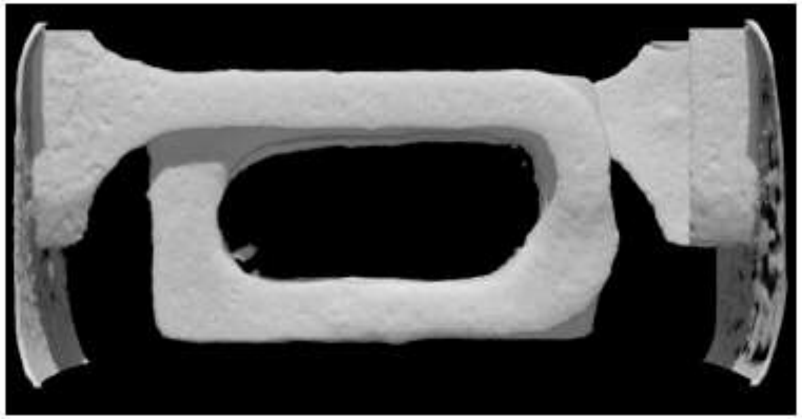
MULTILAYER FERRITE BEAD : INTERNAL STRUCTURE



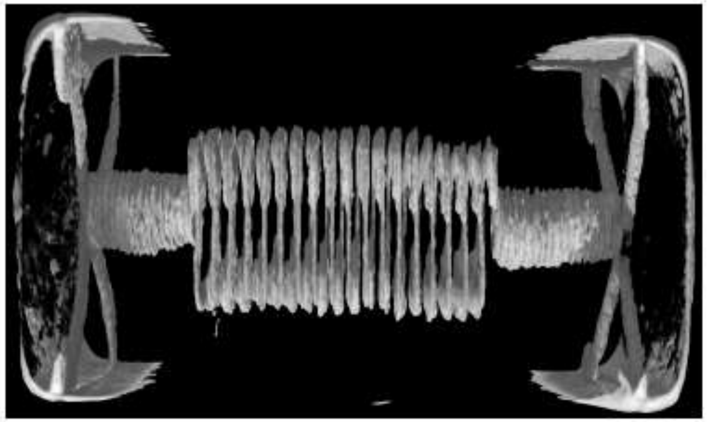
SELECTION

MULTILAYER FERRITE BEAD CONSTRUCTION

General Structure

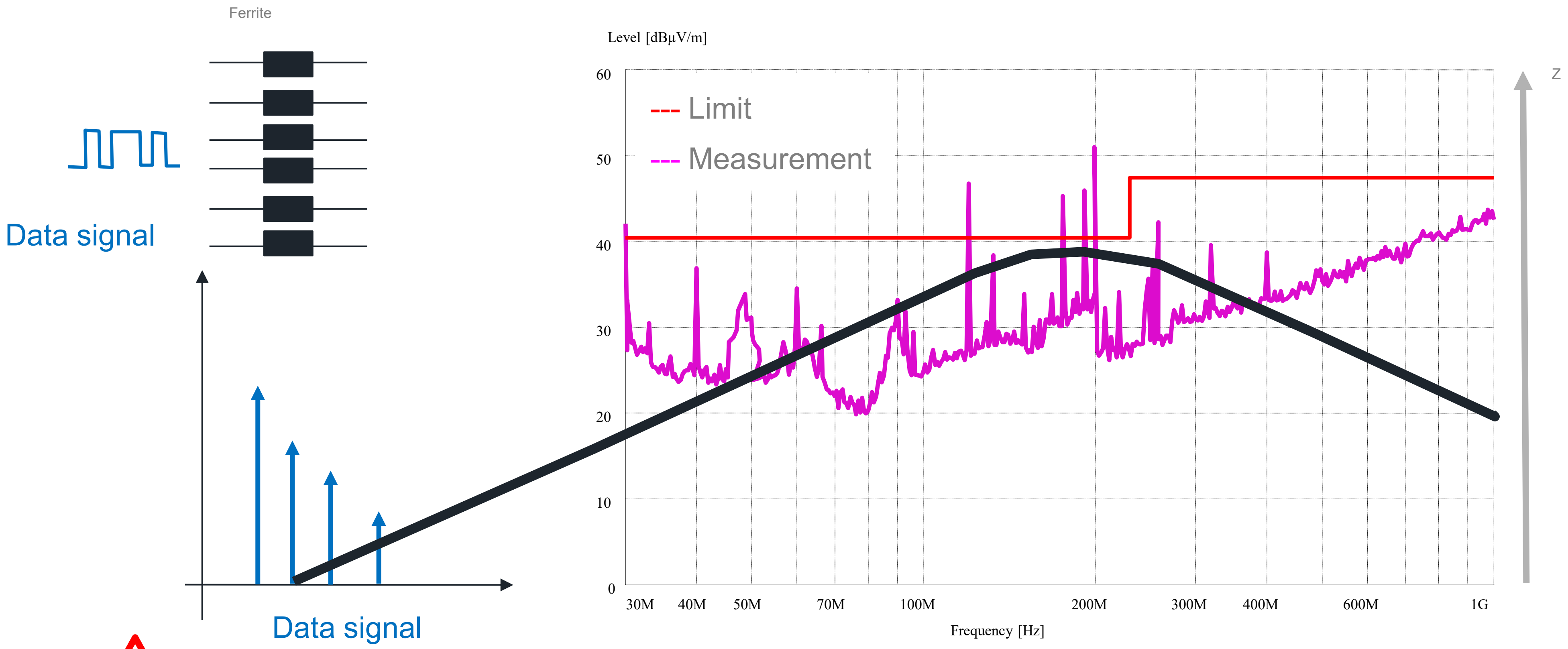


High Frequency Structure



SELECTION

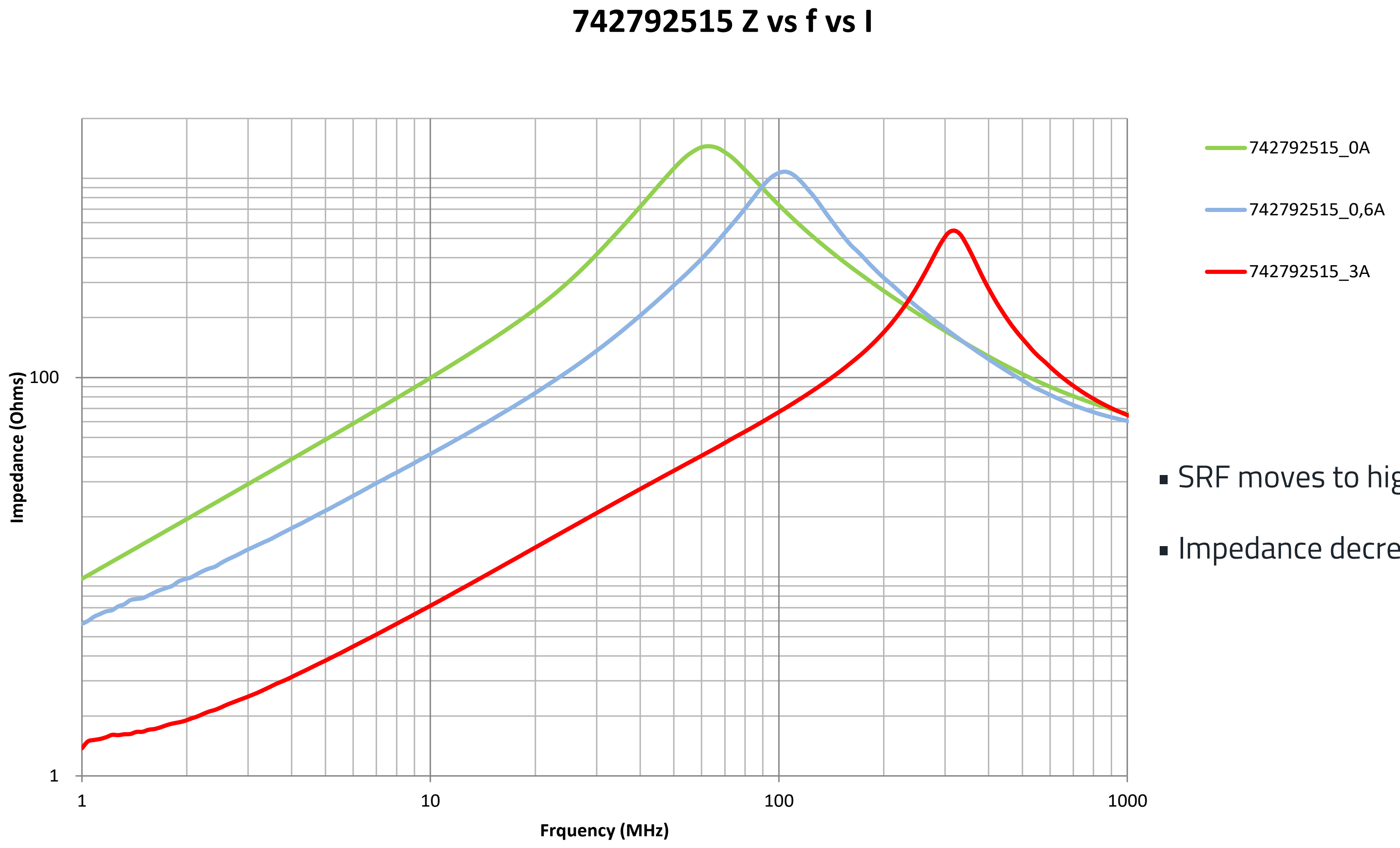
Data line : Compromise



The impedance of the ferrite must be high enough to attenuate the noise but not too high to not damage the useful signal

SELECTION

CHIP FERRITES DC BIAS

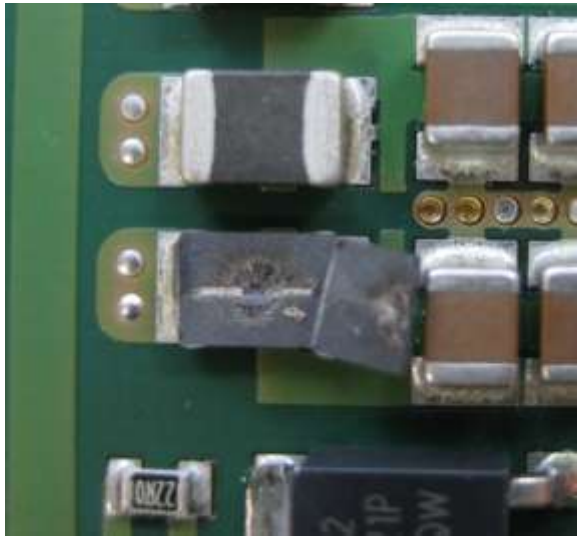


- SRF moves to higher frequency
- Impedance decrease

SELECTION

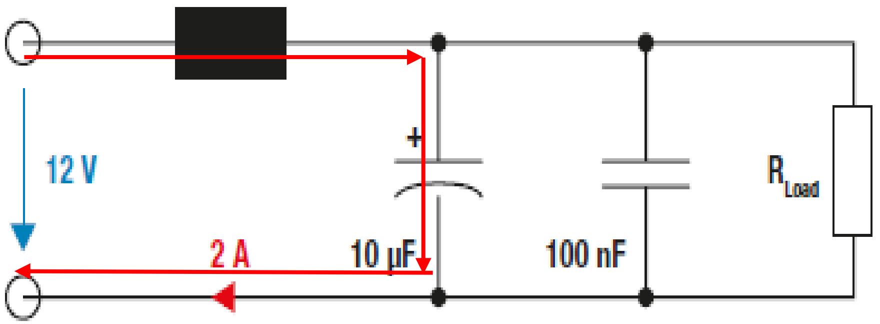
Effect of Current and Temperature

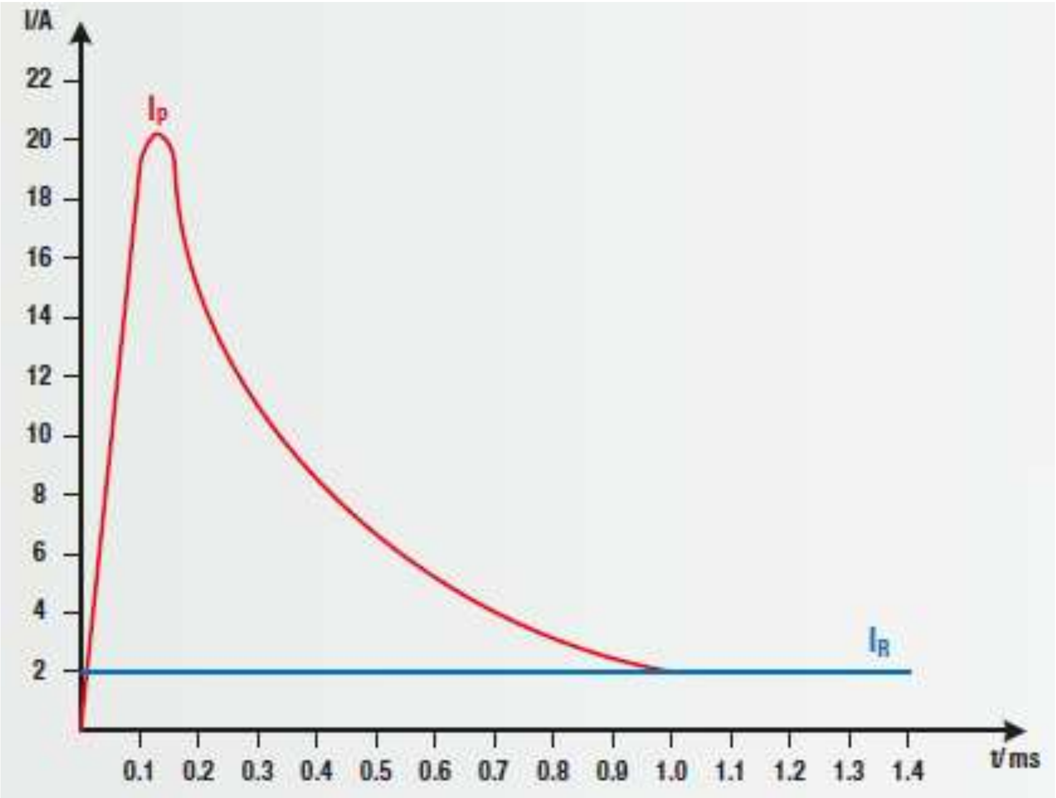
Pulse peak after switch on



SELECTION

IN-RUSH CURRENT

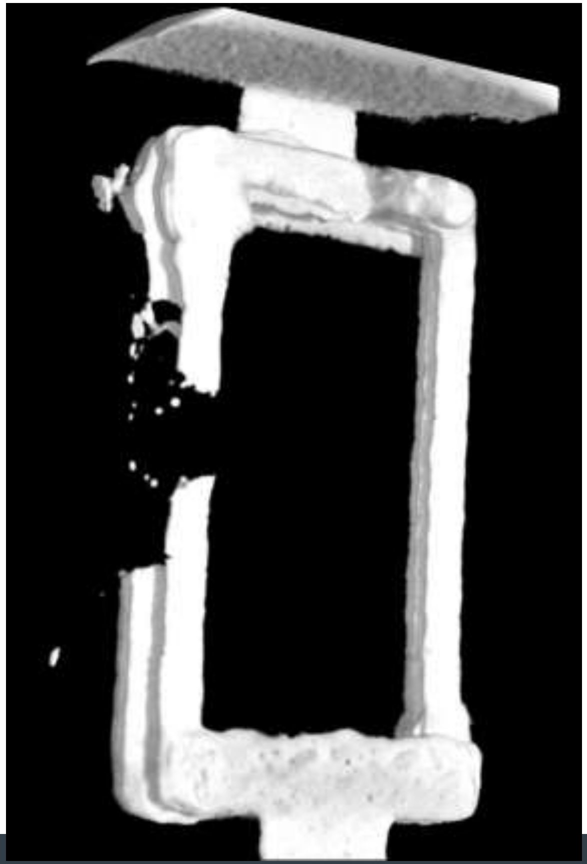


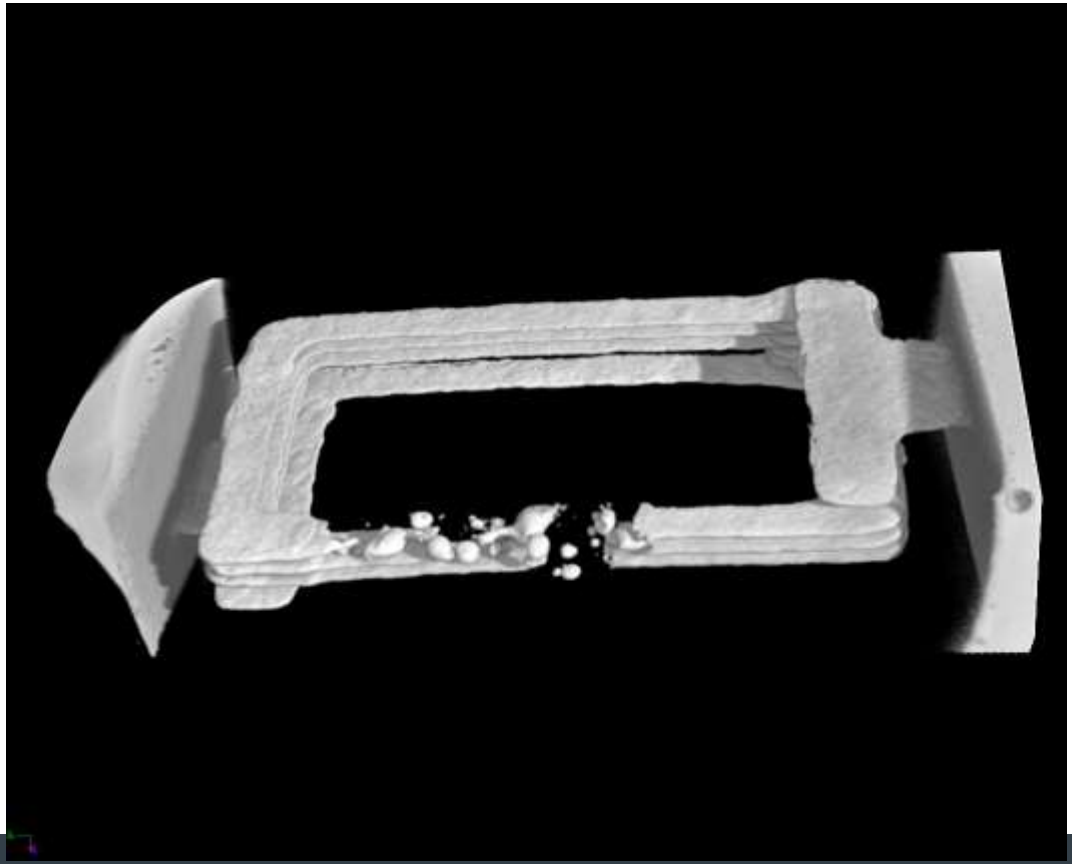


SELECTION

IN-RUSH CURRENT

- Multilayer Ferrite (0805)
- Destruction at a pulse of 1ms with max. 40A pulse current





SELECTION

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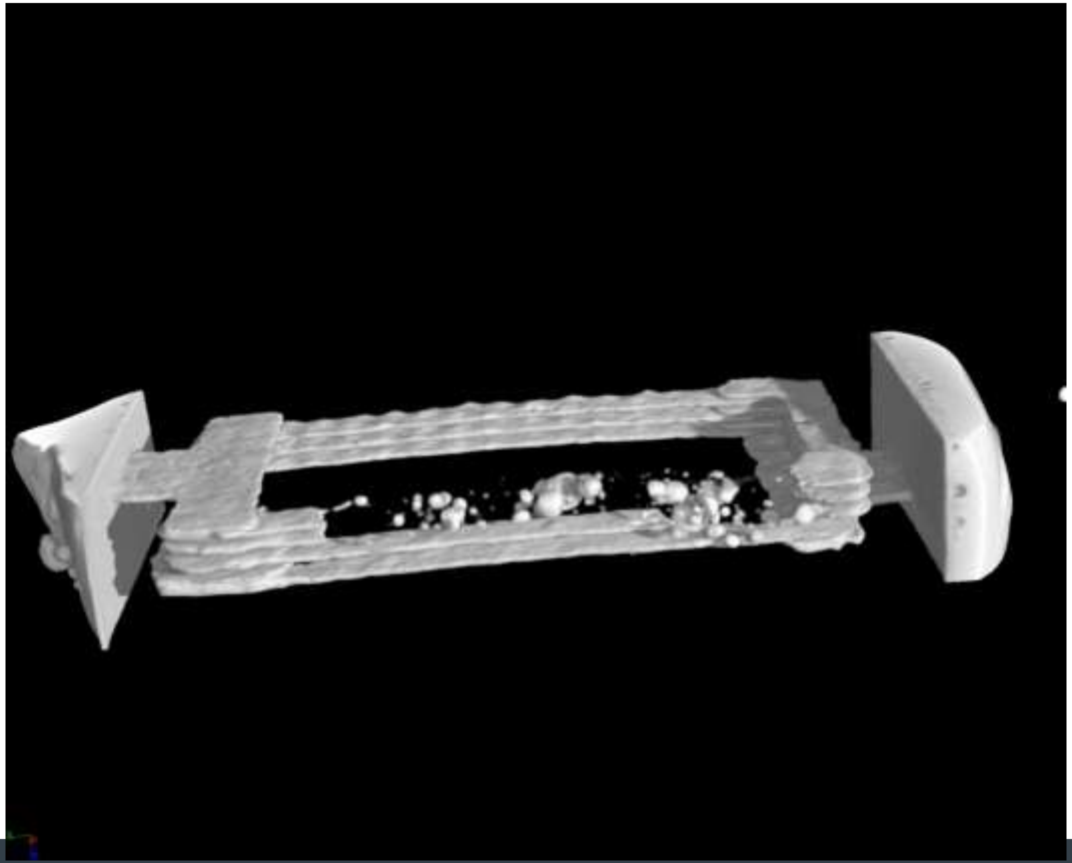
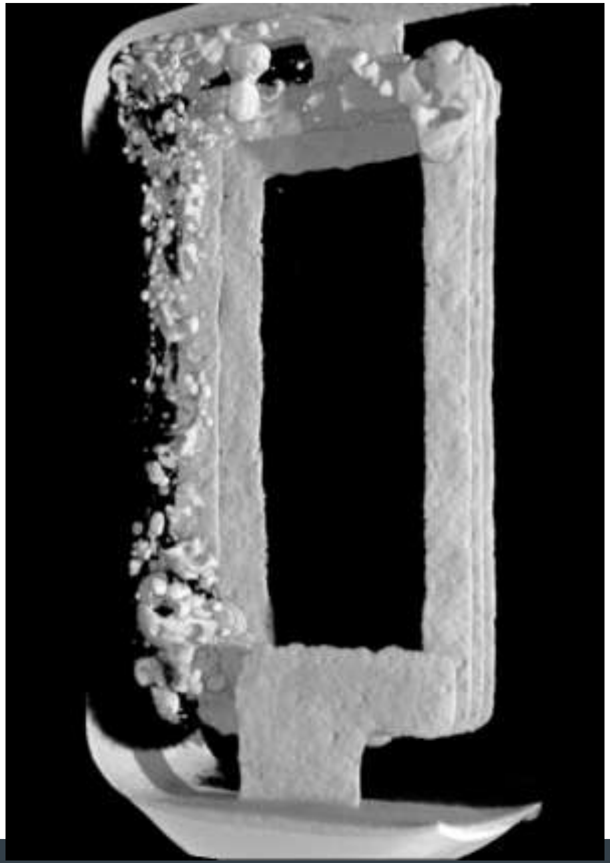
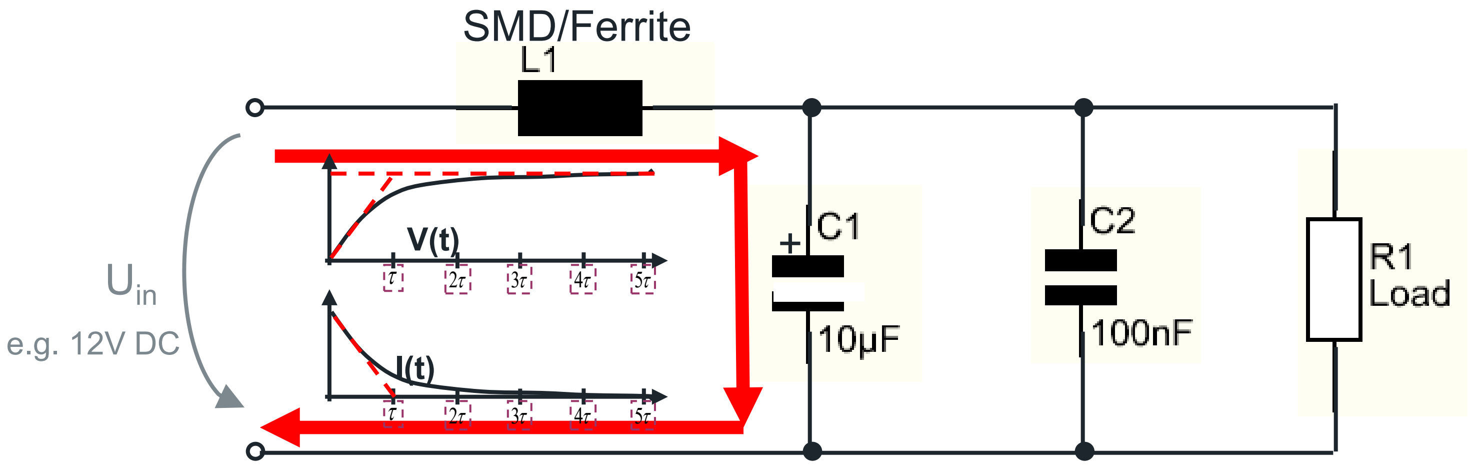




SELECTION

HOW TO PROTECT THE FERRITE

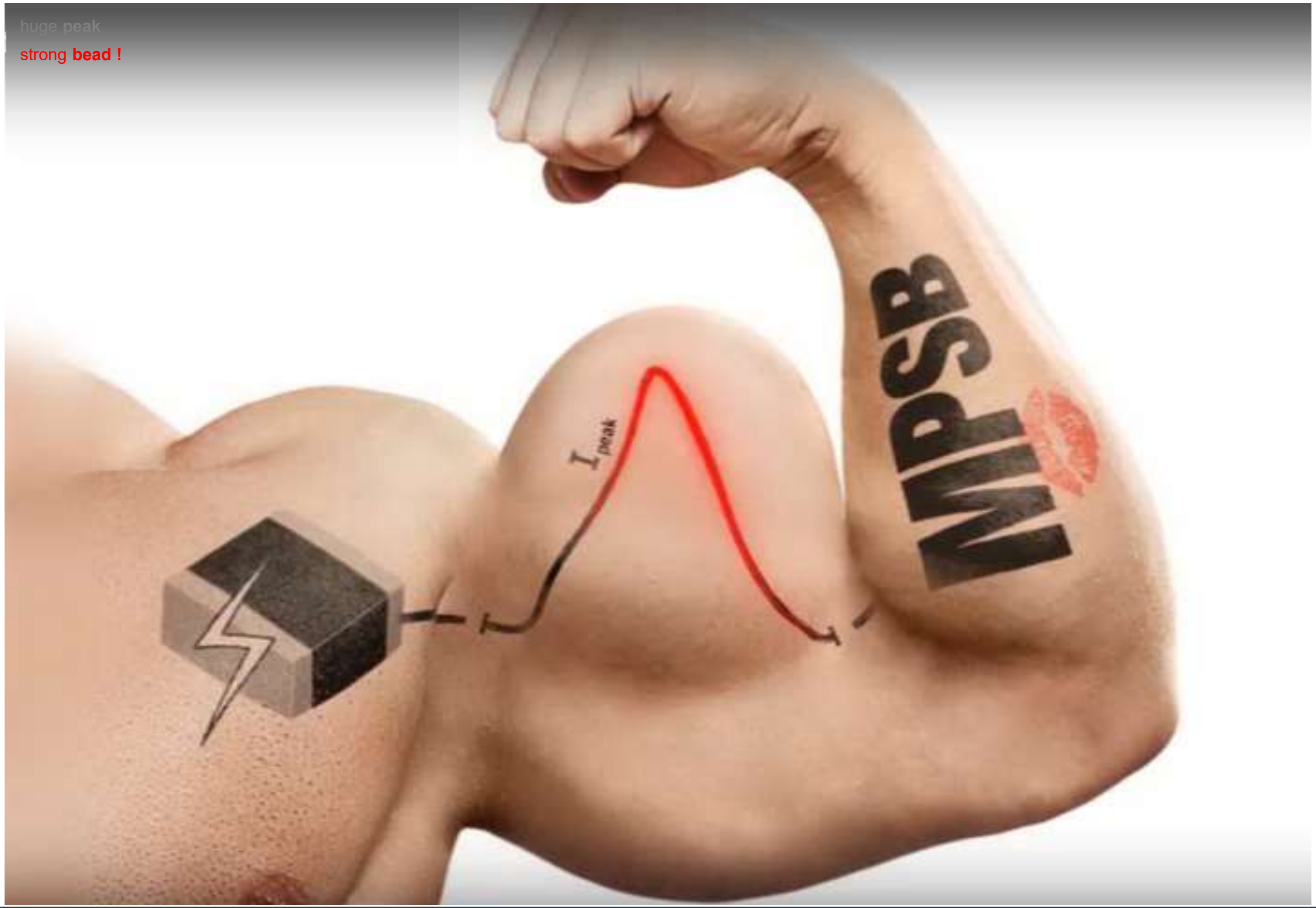
Avoiding inrush current damage to SMD ferrite beads



- Protect ferrite from In Rush current during :
  - Power up
  - Hot plugging
  - Line Transient
    - Surge
    - Load dump
    - Safety for SMD ferrite against In-Rush current (load dump) current

SELECTION

MPSB SOLUTION



www.we-online.com/we-mpsb

SELECTION

WE-MPSB MULTILAYER POWER SUPPRESSION BEAD

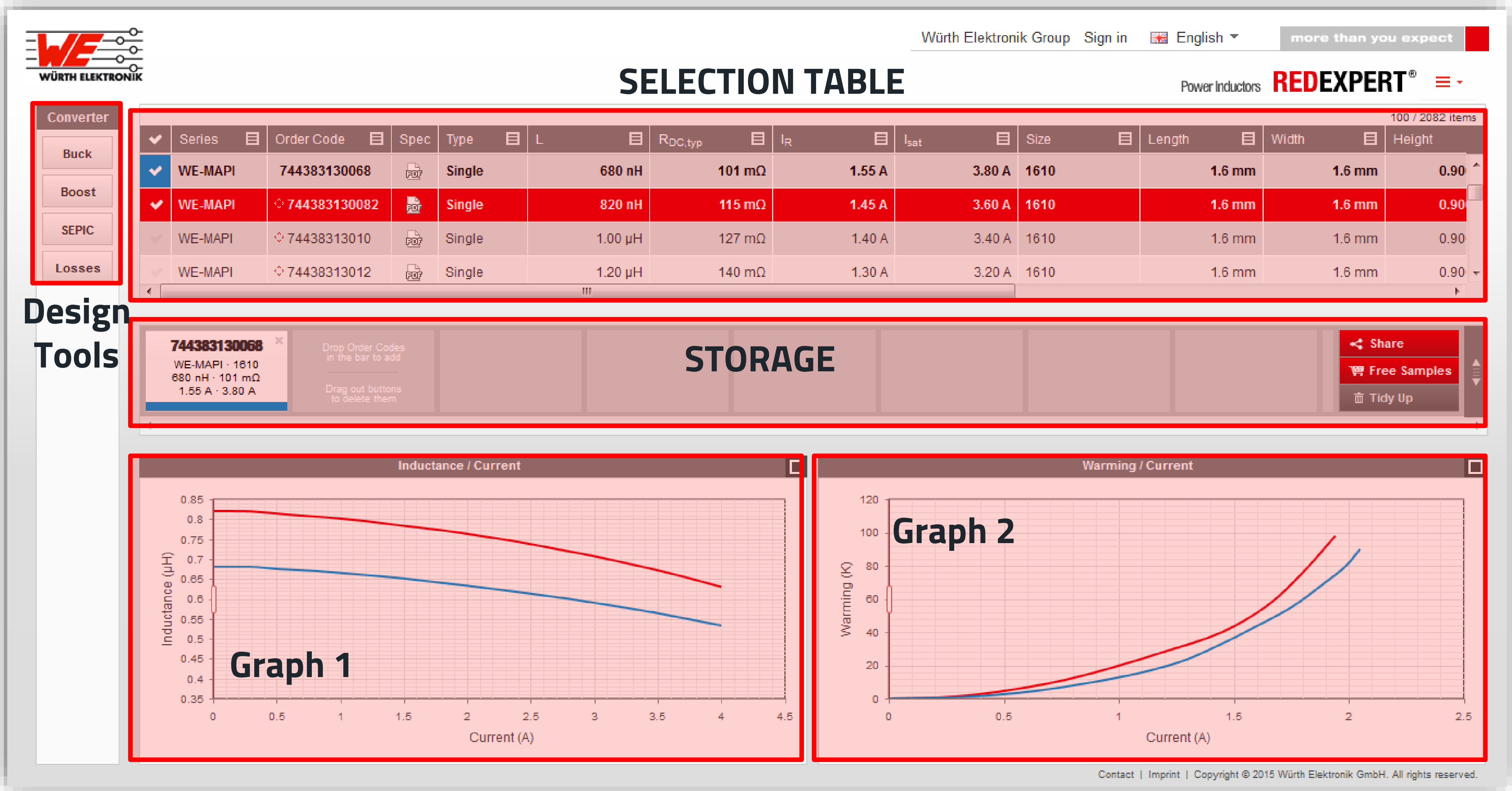
- Current Load Measurments :

SELECTION

SELECTION TOOL - REDEXPERT

SELECTION

REDEXPERT - USER INTERFACE



REDEXPERT

https://www.we-online.com/redexpert/#/module/1

www.we-online.com/redexpert

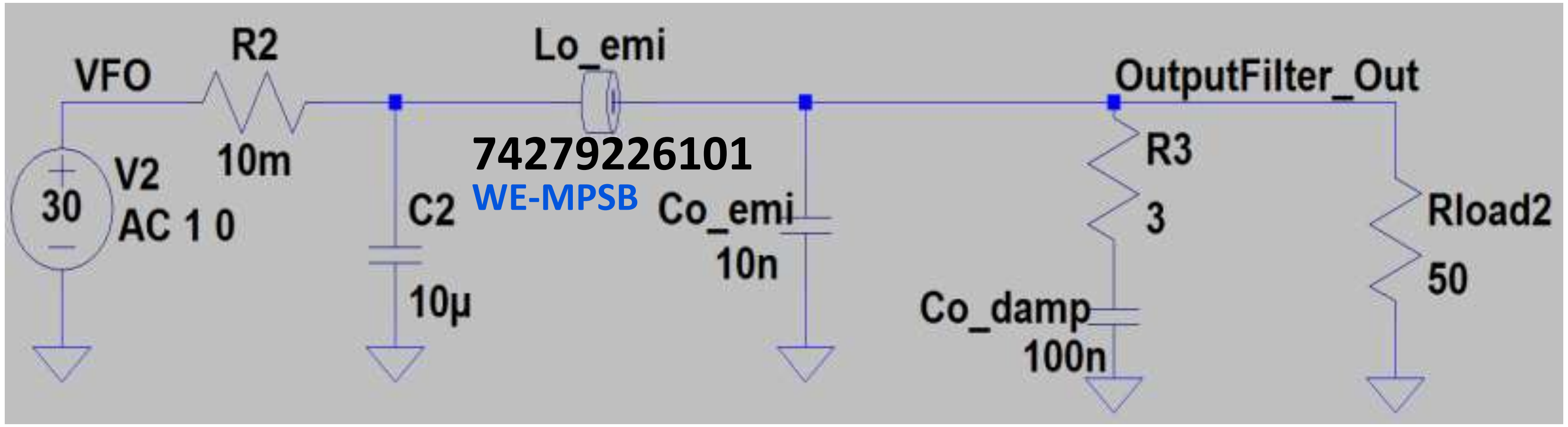
SIMULATION

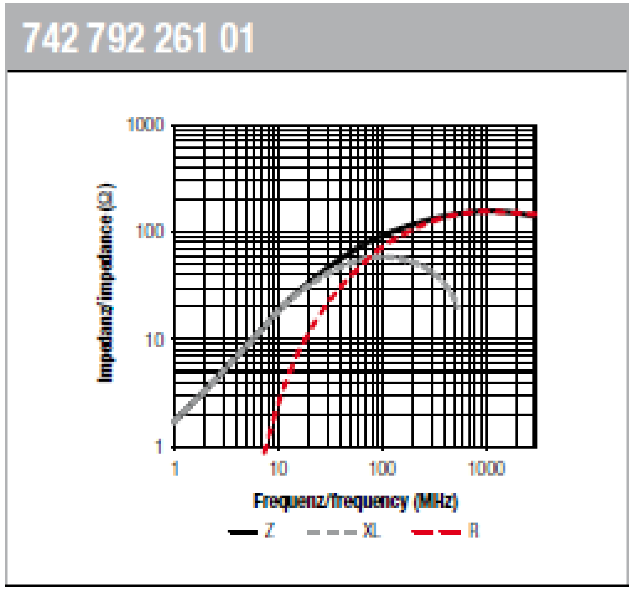
SIMULATIONS

- Conducted Emissions (CE) and Radiated Emissions (RE)
- Damping
- Time domain

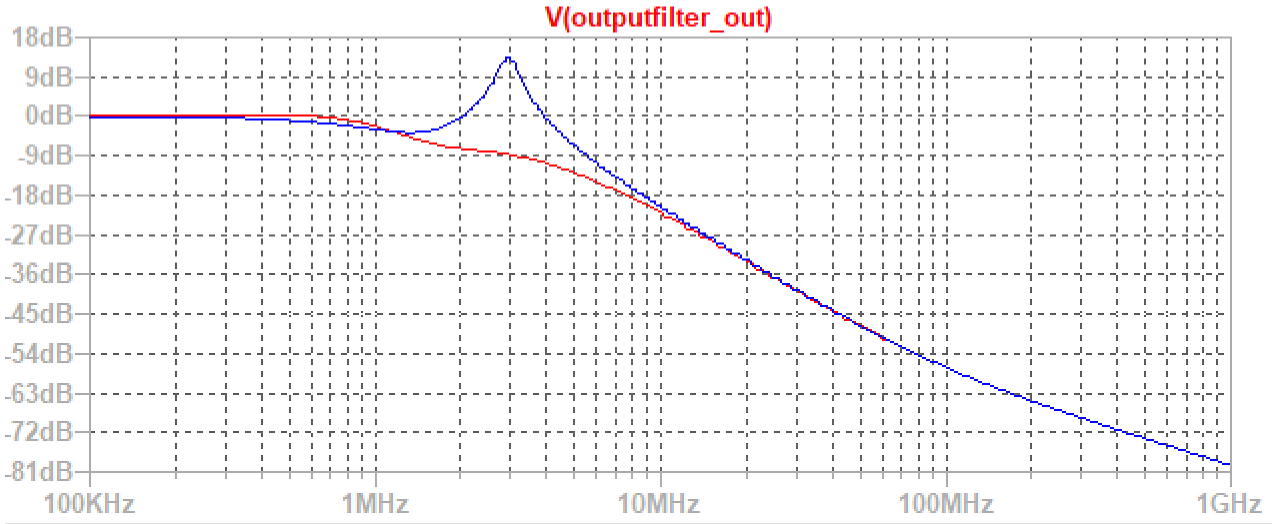
SIMULATIONS

RE DIFFERENTIAL MODE FILTER DESIGN



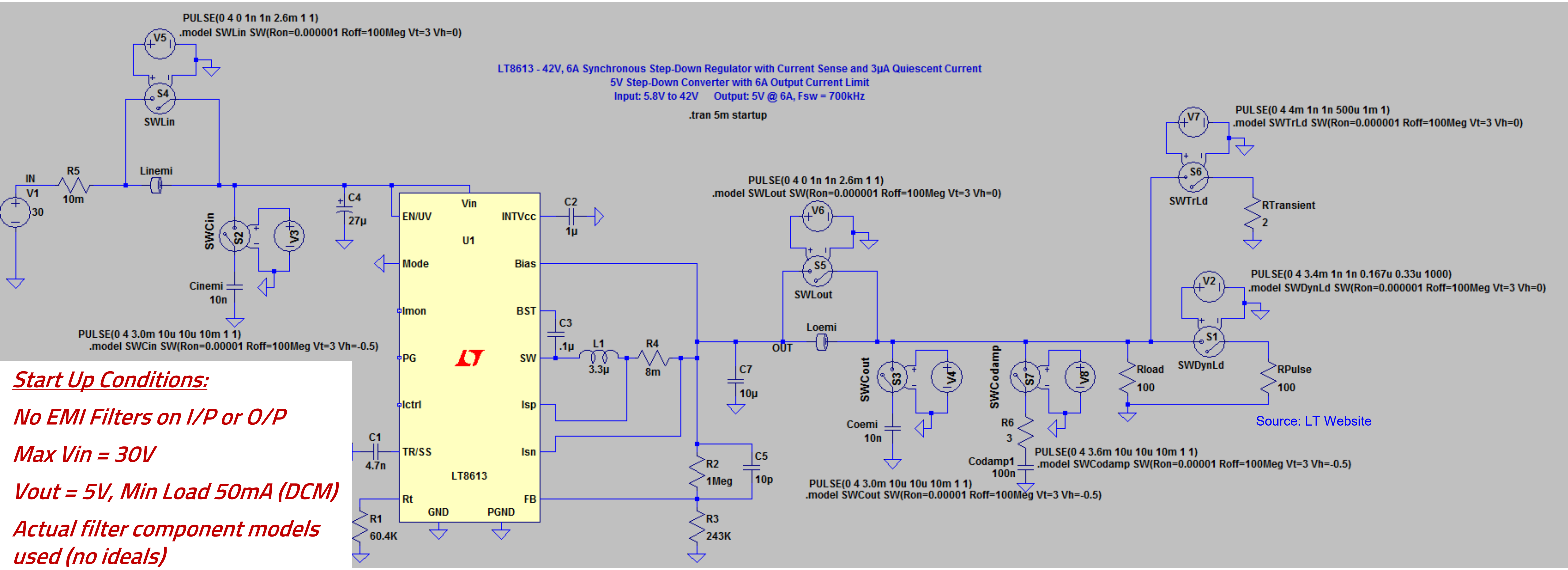


- Load Impact
- EMI Higher Frequency Considerations
- Pulse Rating (WE-MPSB)
- Layout and Tracking
- Capacitor Damping



SIMULATIONS

RE DIFFERENTIAL MODE FILTER DESIGN – BUCK EXAMPLE



Start Up Conditions:

No EMI Filters on I/P or O/P

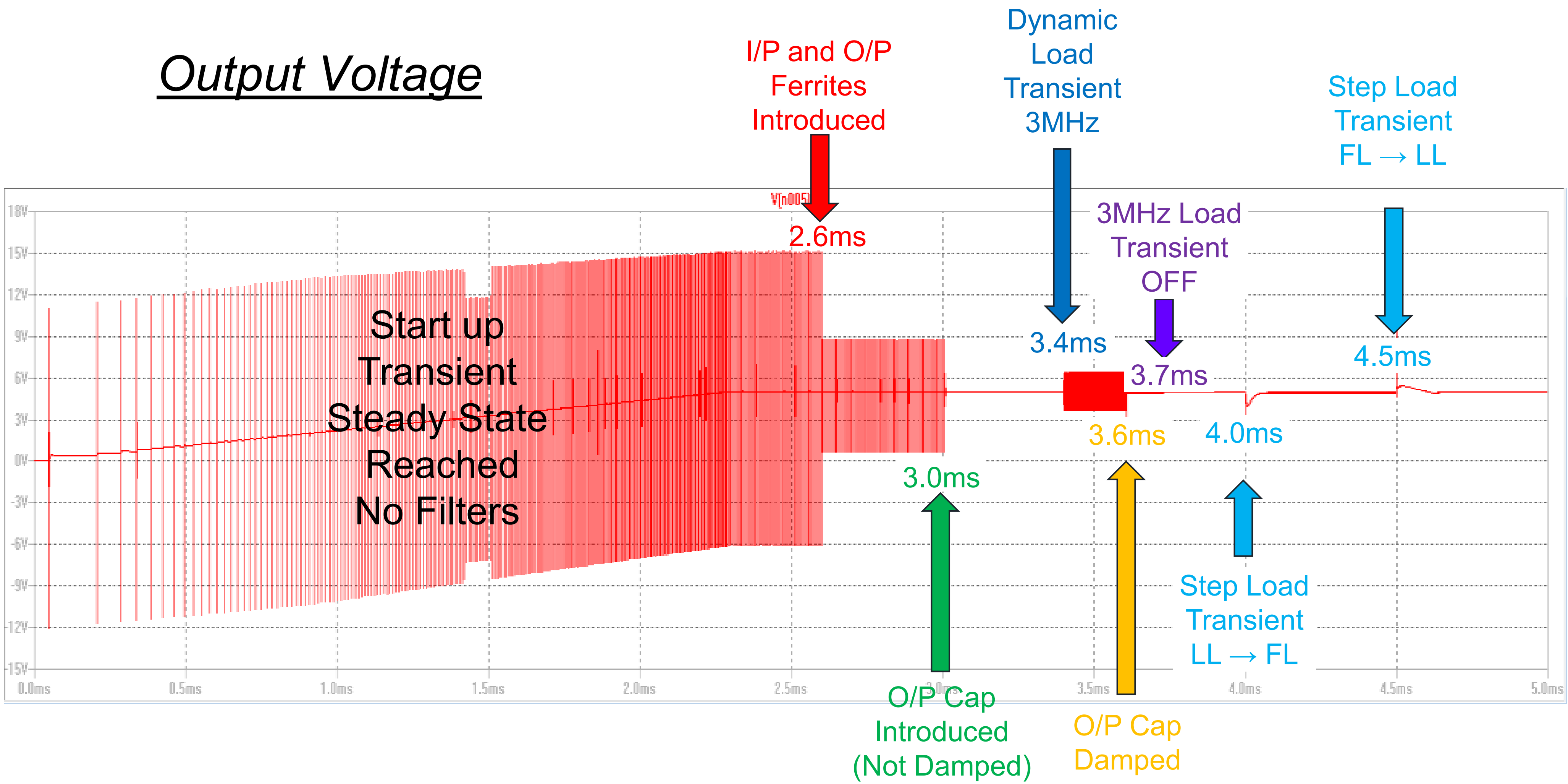
Max Vin = 30V

Vout = 5V, Min Load 50mA (DCM)

Actual filter component models used (no ideals)

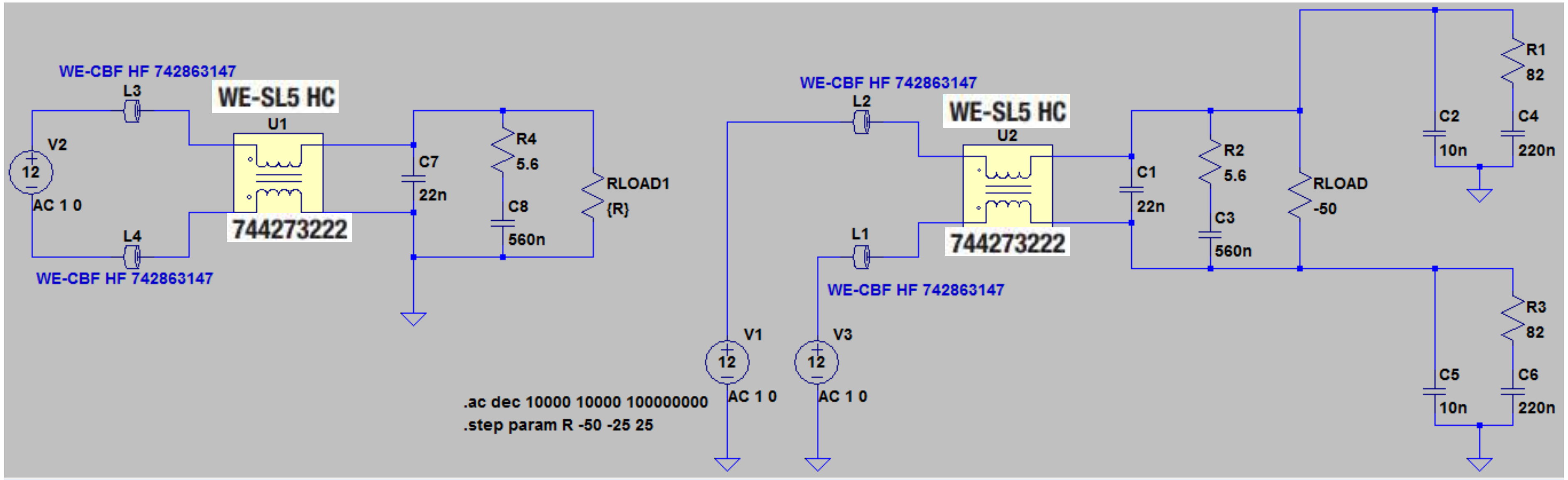
SIMULATIONS

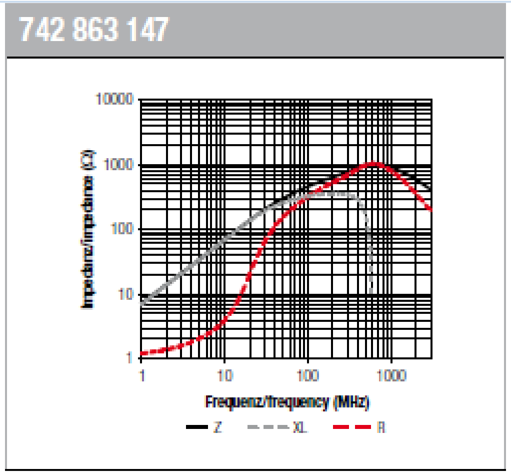
RE DIFFERENTIAL MODE FILTER DESIGN – BUCK EXAMPLE

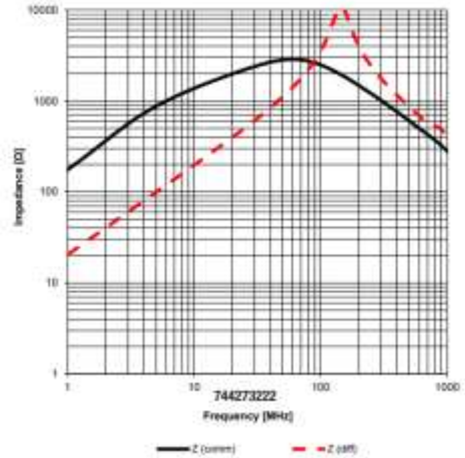


SIMULATIONS

EMI FILTER DESIGN – RE ARCHITECTURE



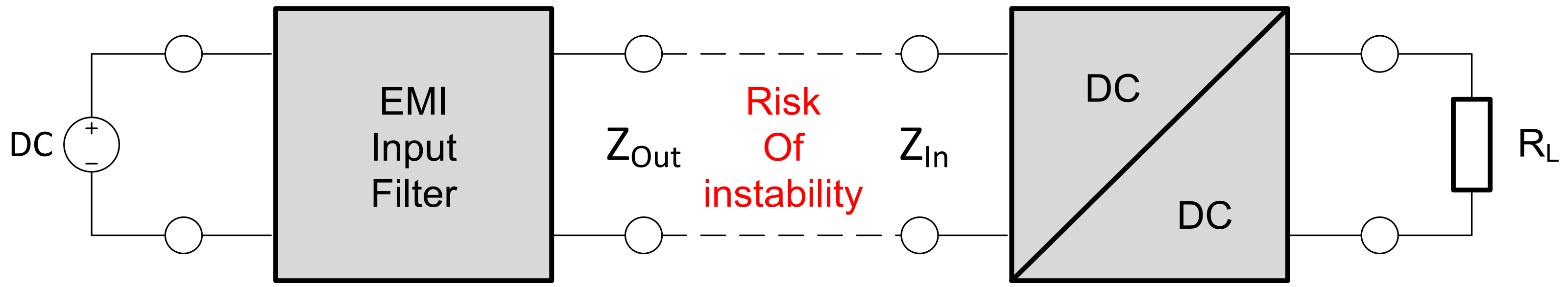




DC/DC INPUT FILTER DESIGN CONSIDERATIONS

Oscillation At Converter Input

CE DIFFERENTIAL MODE INPUT FILTER DESIGN



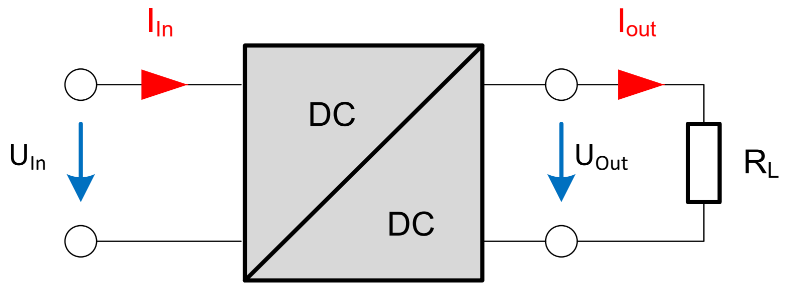
- Adding an input EMI filter to converter input can cause oscillation at converter input
- Problem could arise : the converter no longer meets response specification and may even become unstable!!!

Why????

Input Impedance Of Converter (an explanation)

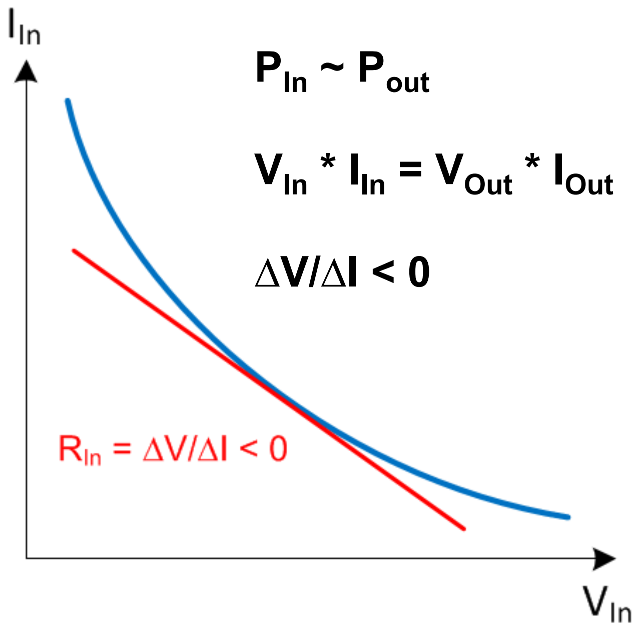
CE DIFFERENTIAL MODE INPUT FILTER DESIGN

- Input and output power of converter is near the same (efficiency drop)
- Under stable conditions output power is constant
- If the input voltage falls, the input current increases
- Voltage-current line has a negative slope



$V_{In}\downarrow$ → $I_{In}\uparrow$ → $R_{In} < 0$

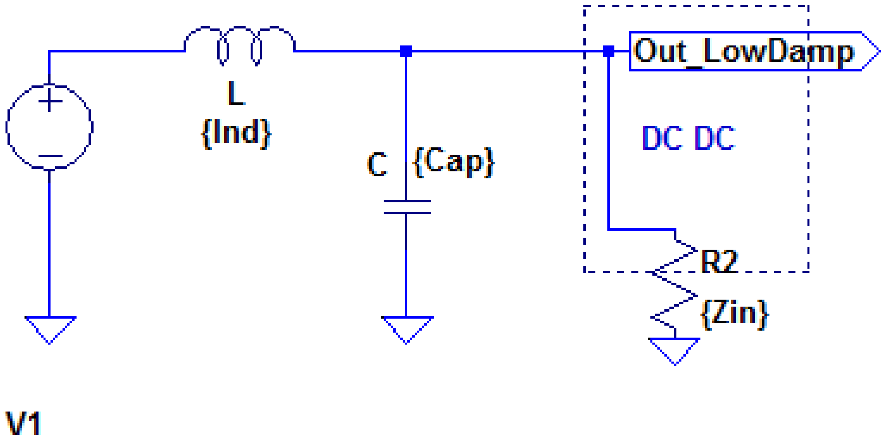
NEGATIVE DC INPUT RESISTANCE



What could happen?

CE DIFFERENTIAL MODE INPUT FILTER DESIGN

- Simplified model



- R_L: Rdc of the inductor
- ESR: serie resisistance of the capacitor
- Input impedance of the buck converter (looking negative – see previous slide)

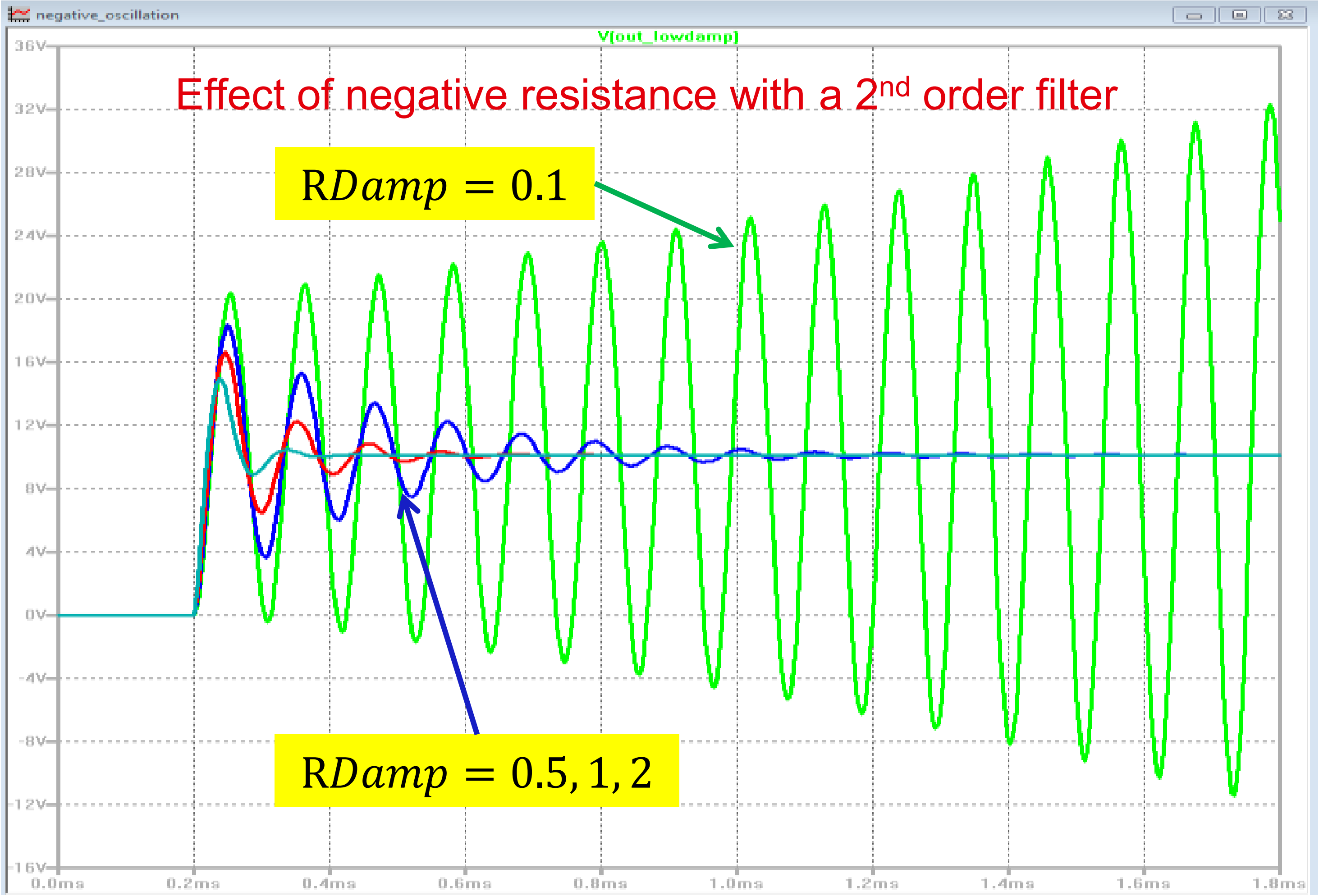
- This is a LC filter loaded by a negative resistance!!!!!

- NICE WAY TO CREATE OSCILLATORS

INSTABILITY

CE DIFFERENTIAL MODE INPUT FILTER DESIGN

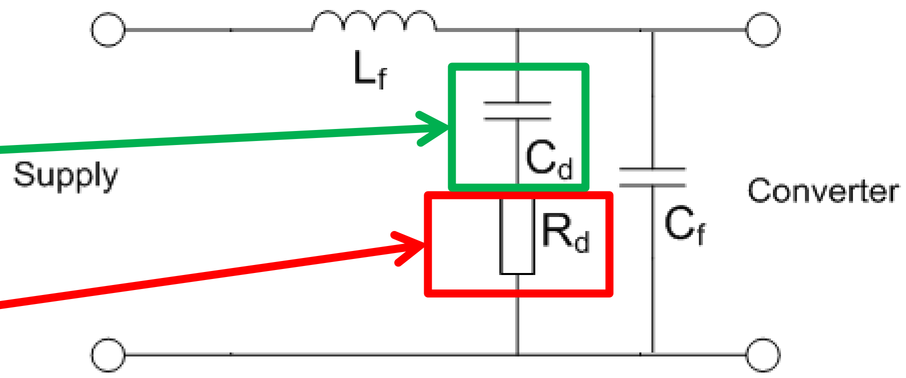
Take care

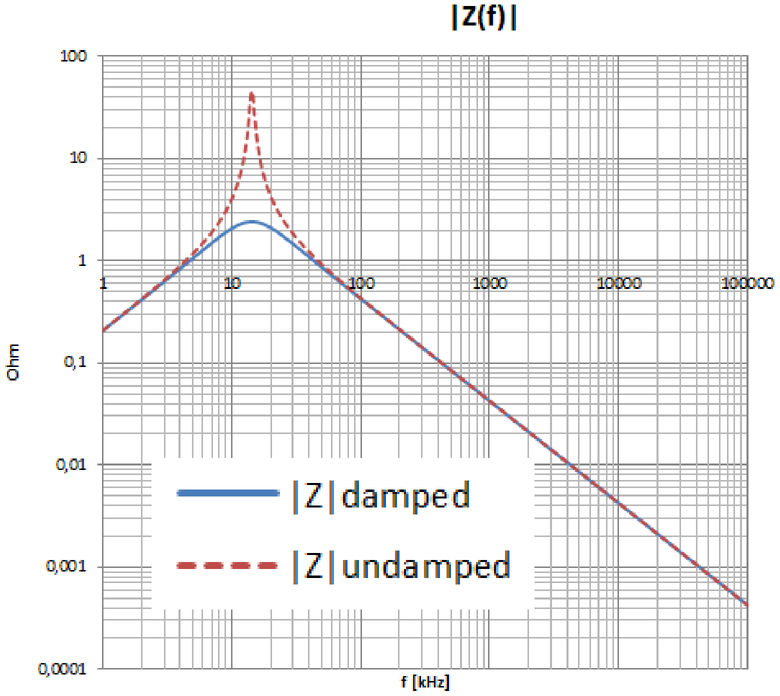


Damping Input Filter

CE DIFFERENTIAL MODE INPUT FILTER DESIGN

- Damping capacitor C_d blocks DC current
- Damping resistor R_d reduces dip magnitude of filter at resonant frequency f_0



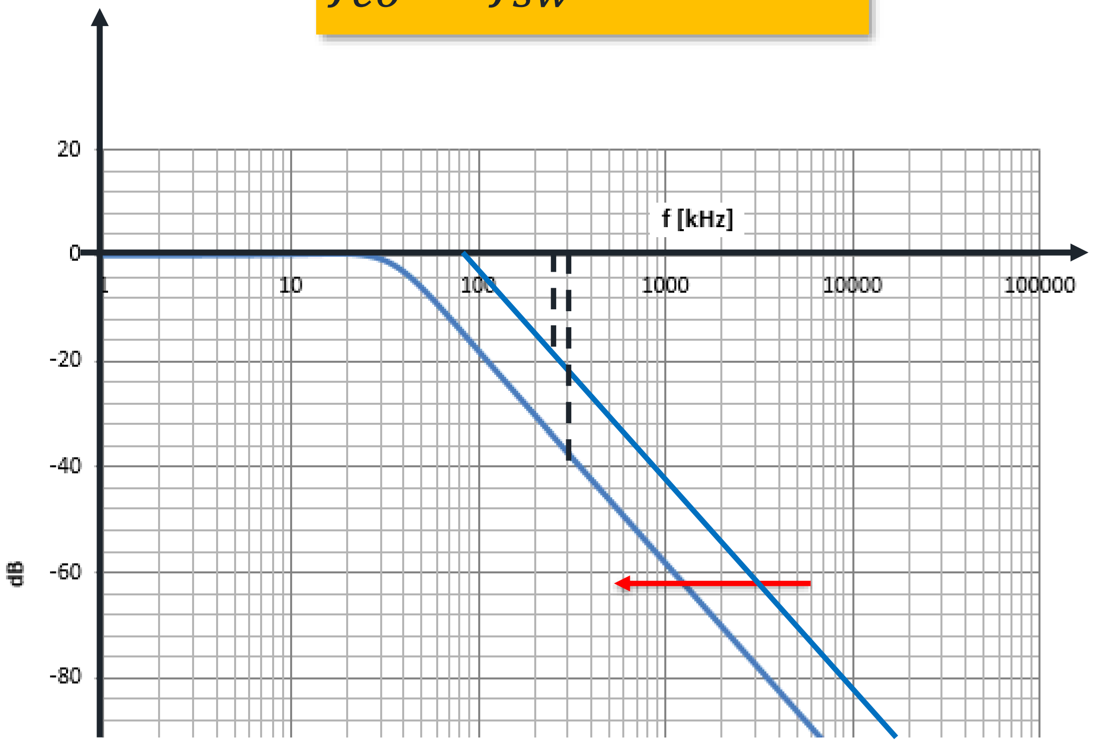


Calculating Input Filter Components values

Gain-Bandwith product

Give the right filter cutoff freq to have the attenuation required with the choosed filter topology (order)

$$f_{co} = f_{sw} \cdot 10^{\left(\frac{-A_{dB}}{n \cdot 20}\right)}$$



- **A(dB)**: attenuation required
- **n**: filter order
- **Fsw**: switching frequency
- **Fco**: filter cut off frequency

Our design:

Adb: 32 dbuV

2nd order filter

Fsw: 150kHz

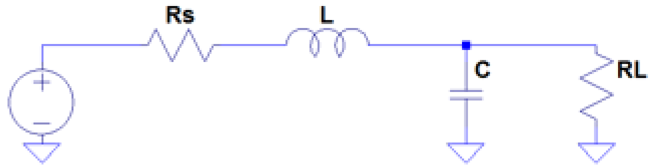
F_{0calc}: 23,77kHz

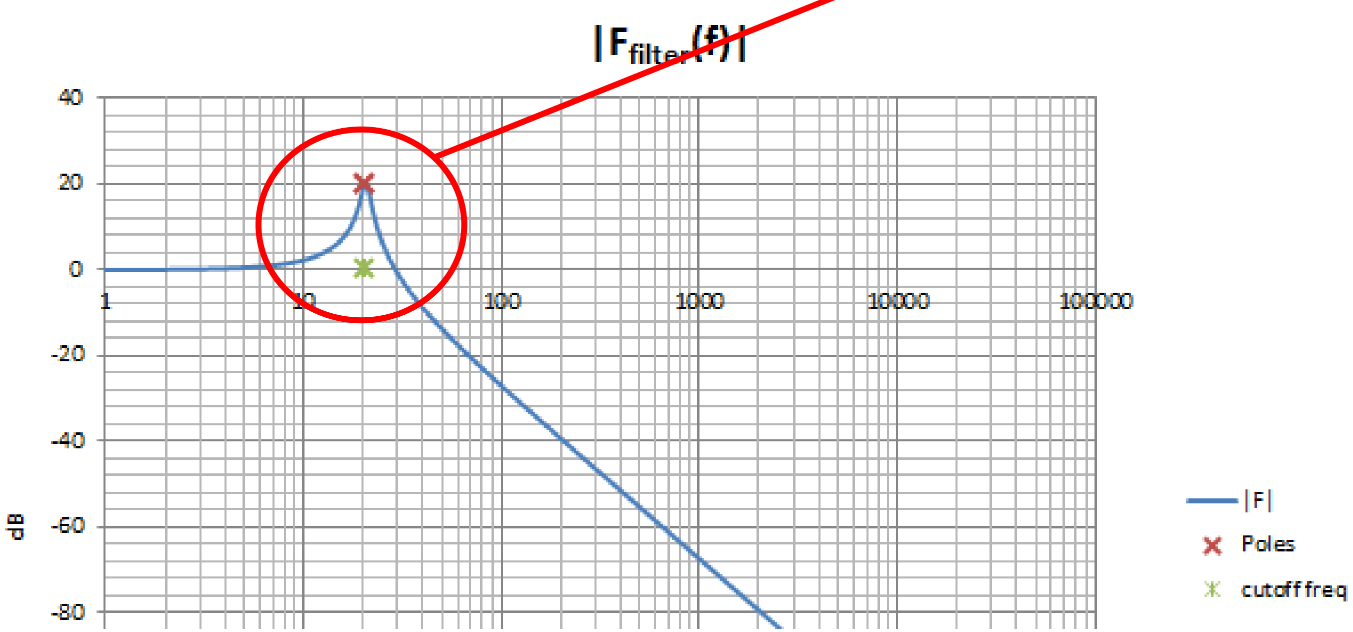
Calculating Input Filter Components values

Selection of the L and C value

Different values for L and C occurs. In our design we can choose as follows:

C	2,2	uF
L	27	uH





In

$$f_0 = \frac{1}{2 \cdot \pi \cdot \sqrt{(L \cdot C)}}$$

≈ 21kHz

(20,65kHz calculated)

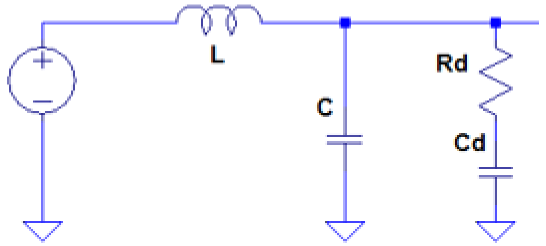
Calculating Input Filter Components values

1) Calculate damping capacitor $$C_d = \mathrm{n} \cdot Cf \qquad with\ n = 4\ or\ 6$$

2) Calculate damping Resistor $$R_d = \sqrt{\frac{L_f}{C_f}\frac{(n+1)}{2n}}\sqrt{\frac{2n^2(4+n)}{(2+n)(4+3n)}}$$

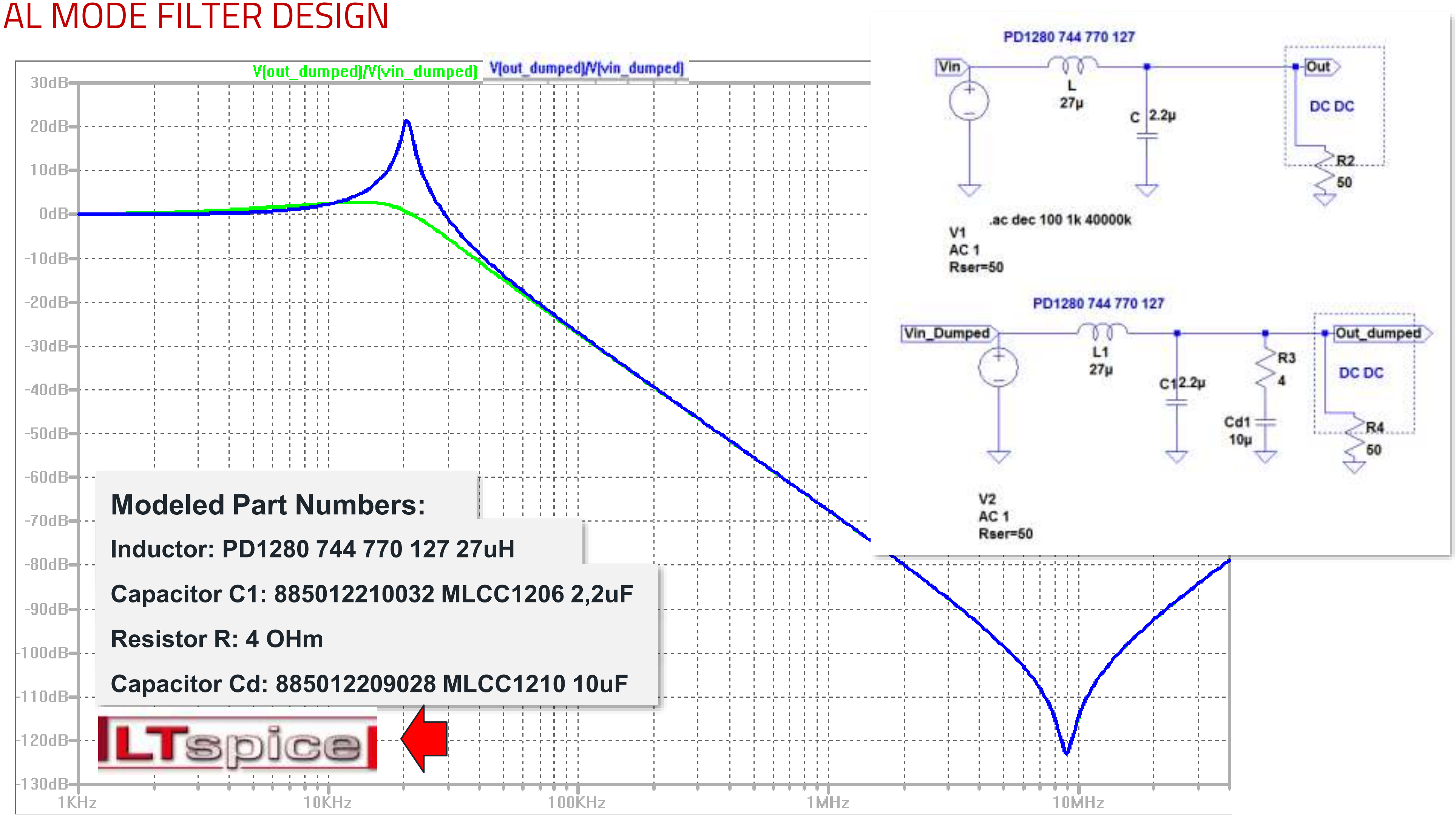
Keeping the same values of undamped filter, we can add an Rd and a Cd as follows:

Rd	3,57548	Ω
Cd	8,8	uF
C	2,2	uF
L	27	uH
n	4	



SIMULATIONS

CE DIFFERENTIAL MODE FILTER DESIGN



Modeled Part Numbers:

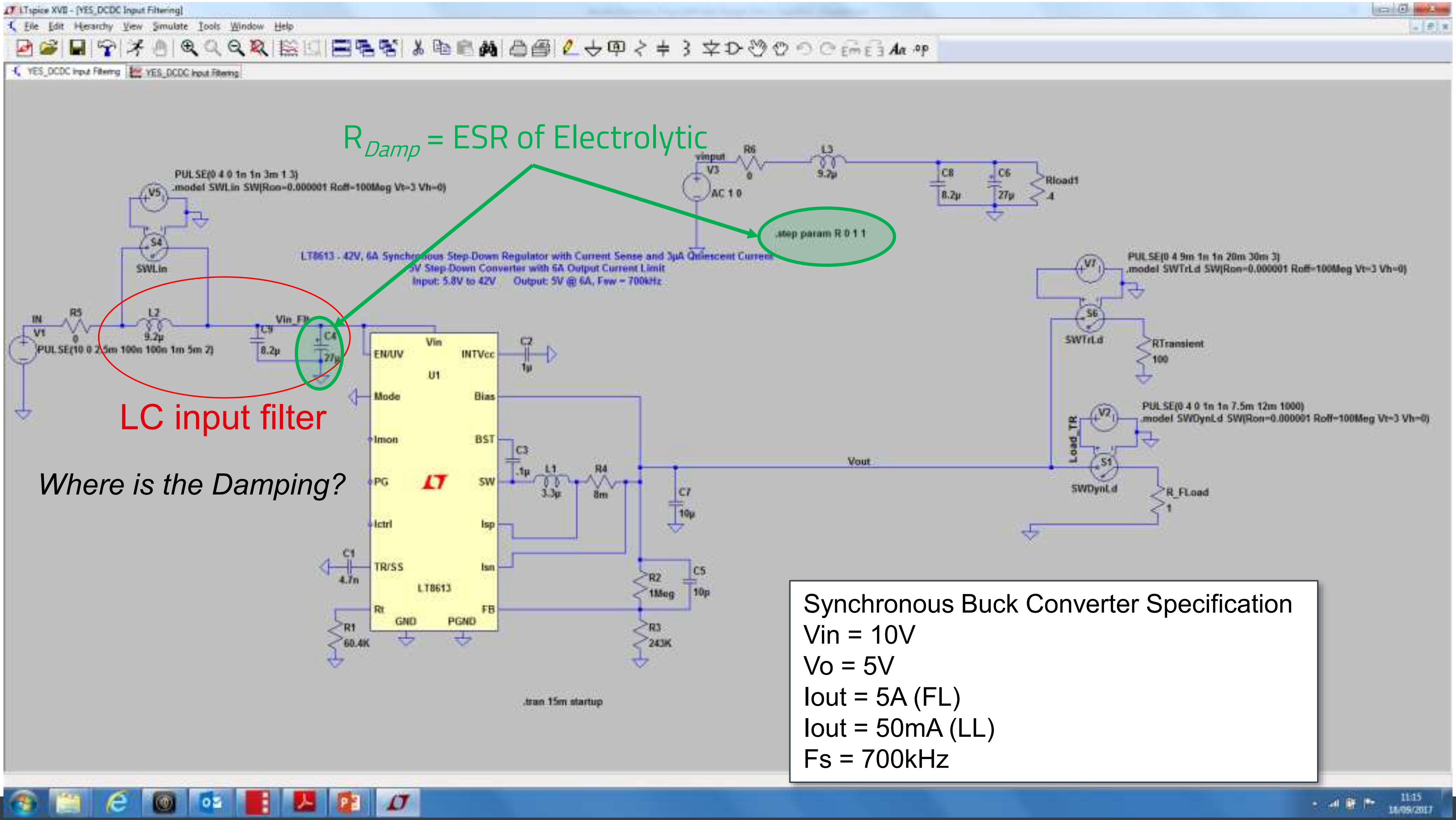
Inductor: PD1280 744 770 127 27uH

Capacitor C1: 885012210032 MLCC1206 2,2uF

Resistor R: 4 OHm

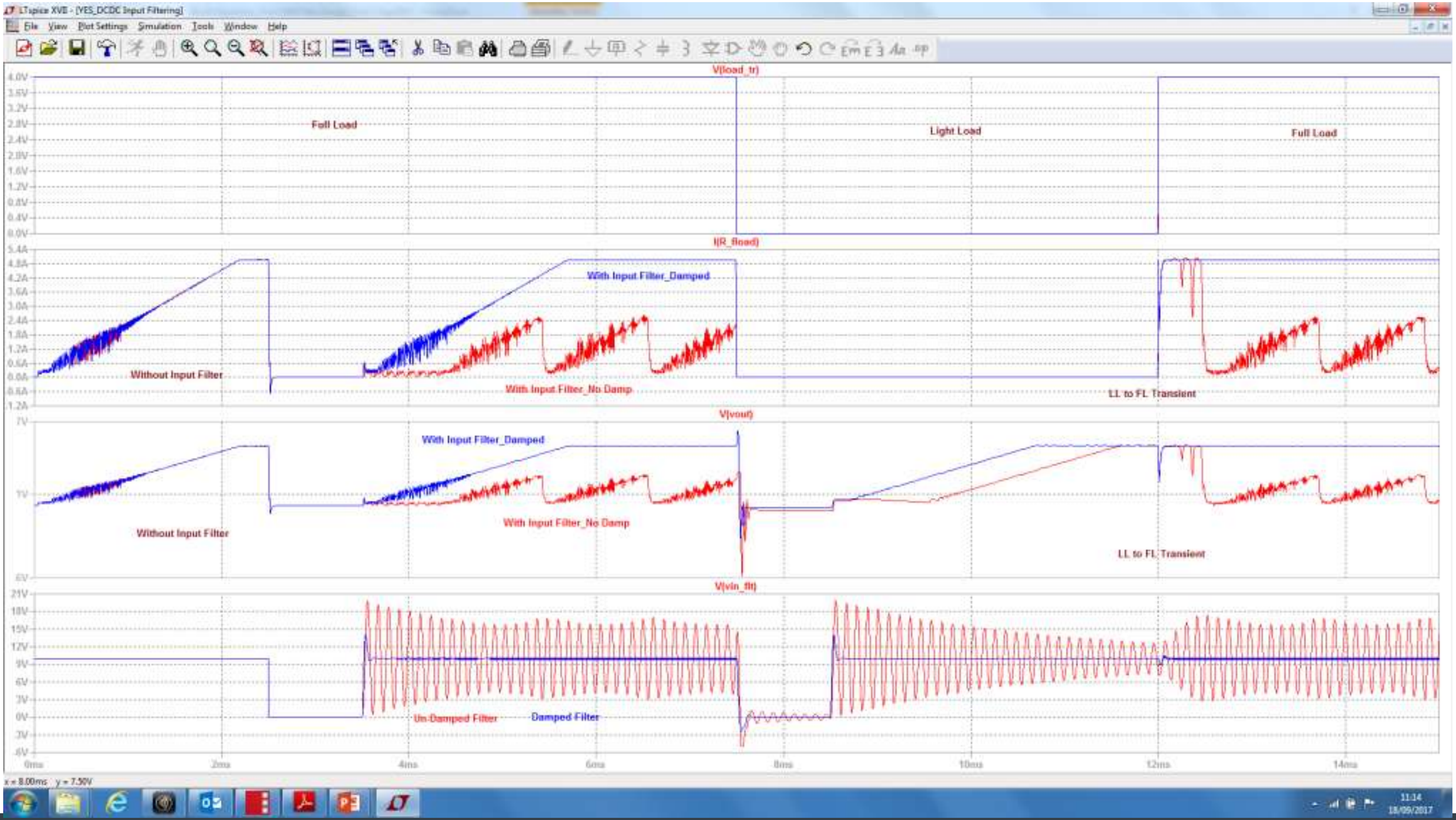
Capacitor Cd: 885012209028 MLCC1210 10uF

CE DIFFERENTIAL MODE FILTER DESIGN – BUCK EXAMPLE



Synchronous Buck Converter Specification
Vin = 10V
Vo = 5V
Iout = 5A (FL)
Iout = 50mA (LL)
Fs = 700kHz

CE DIFFERENTIAL MODE FILTER DESIGN – BUCK EXAMPLE

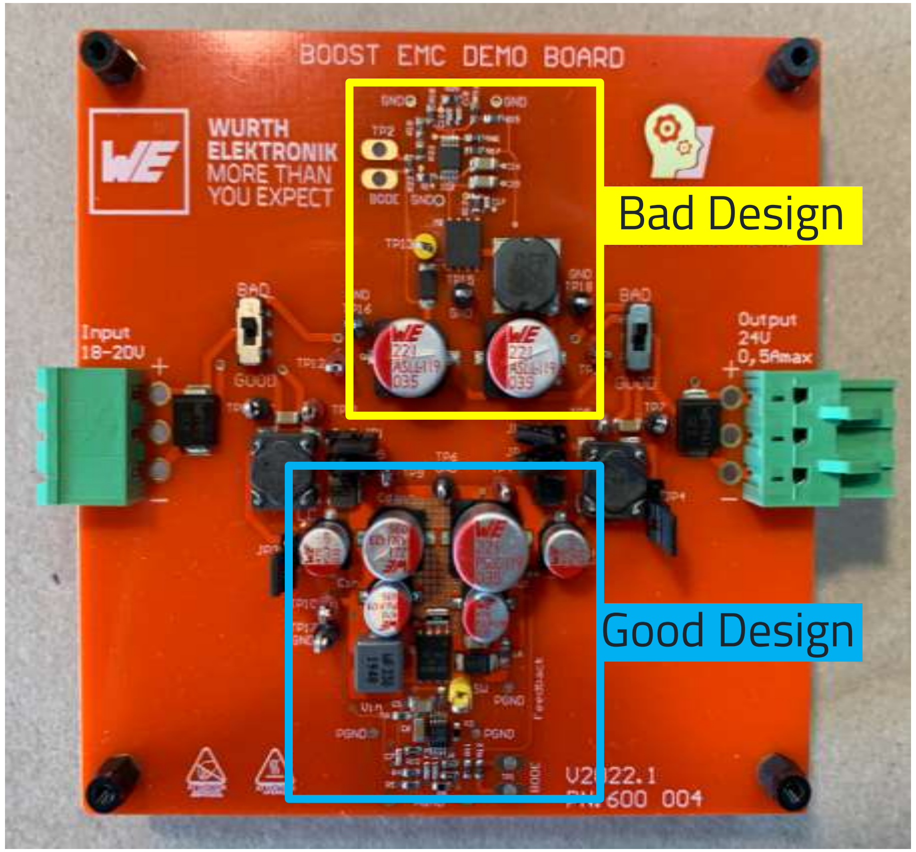


BOOST EMI DEBUGGING EXAMPLE

Objective of the Good and Bad Layout

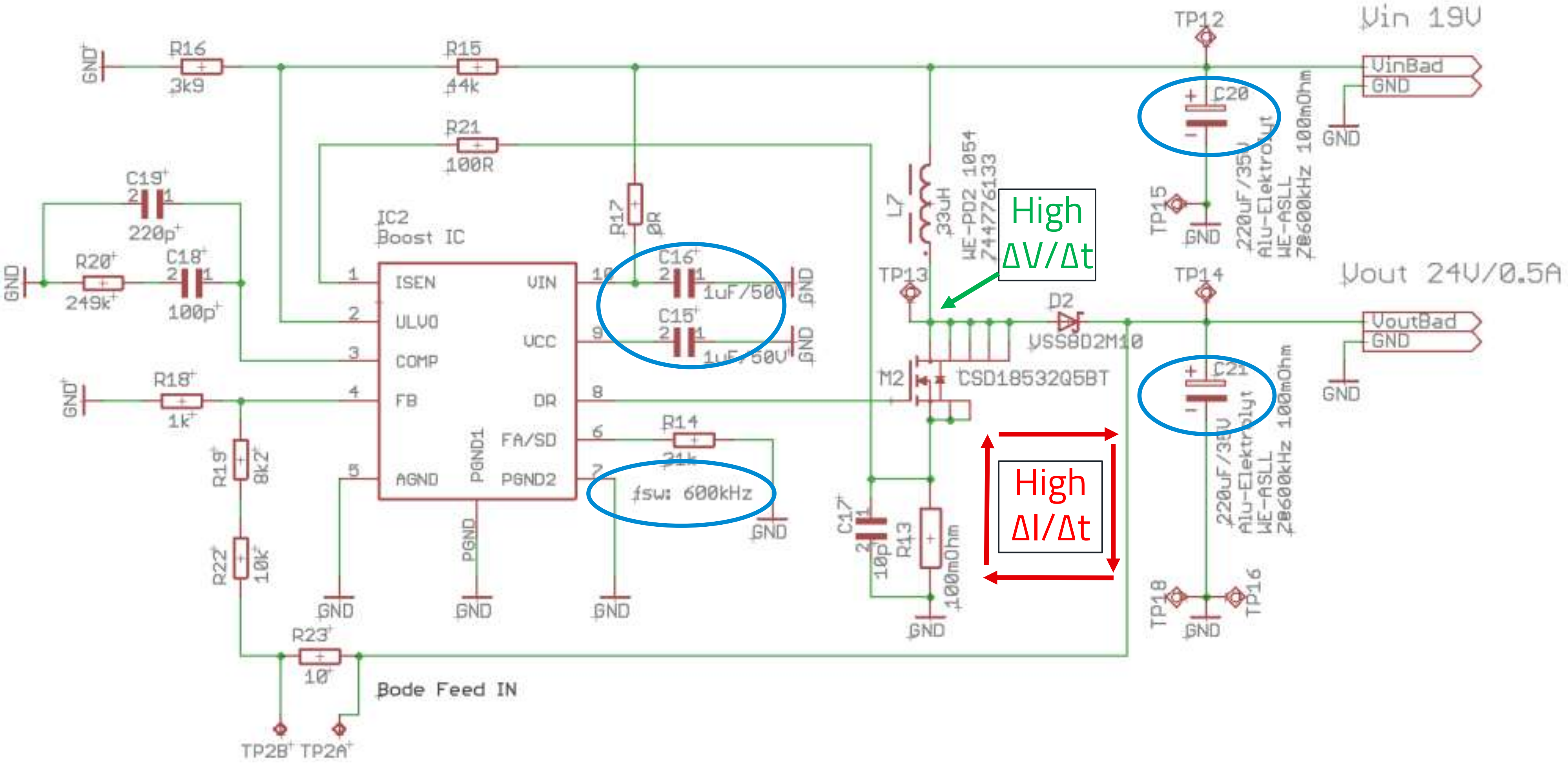
Keypoints

- Single Point PGND vs. big PGND Loop
- Correct vs. Wrong Capacitor Position
- Same Semiconductors, different Passives
- Shielded Choke vs. Unshielded Choke
- Alu-Electrolyte vs. Polymer Caps
- Filter @ I/Os vs. No Filter at all
- Ferrite in the Power Loop of a DCDC

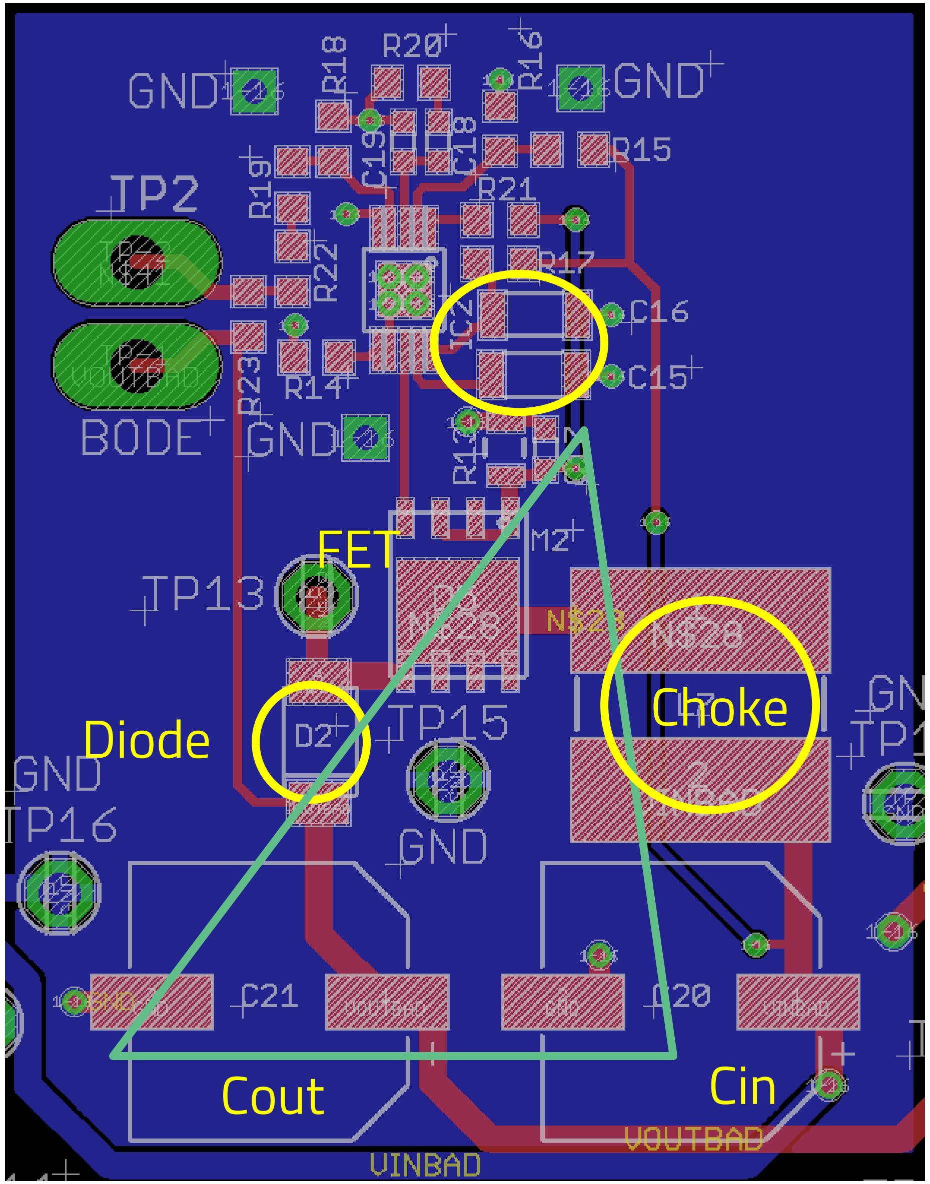


Schematic Bad Design

19V → 24V/0,5A

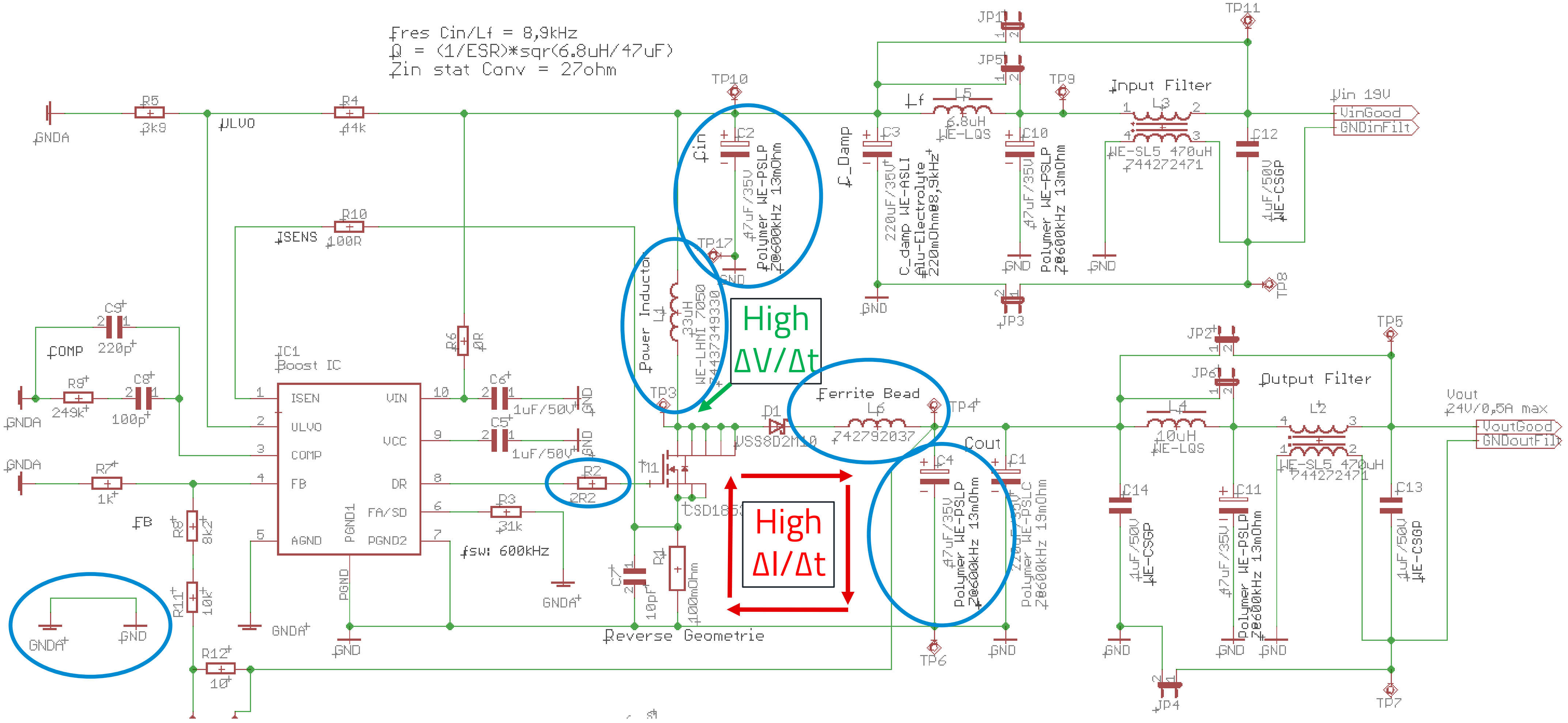


PCB Layout Bad Design

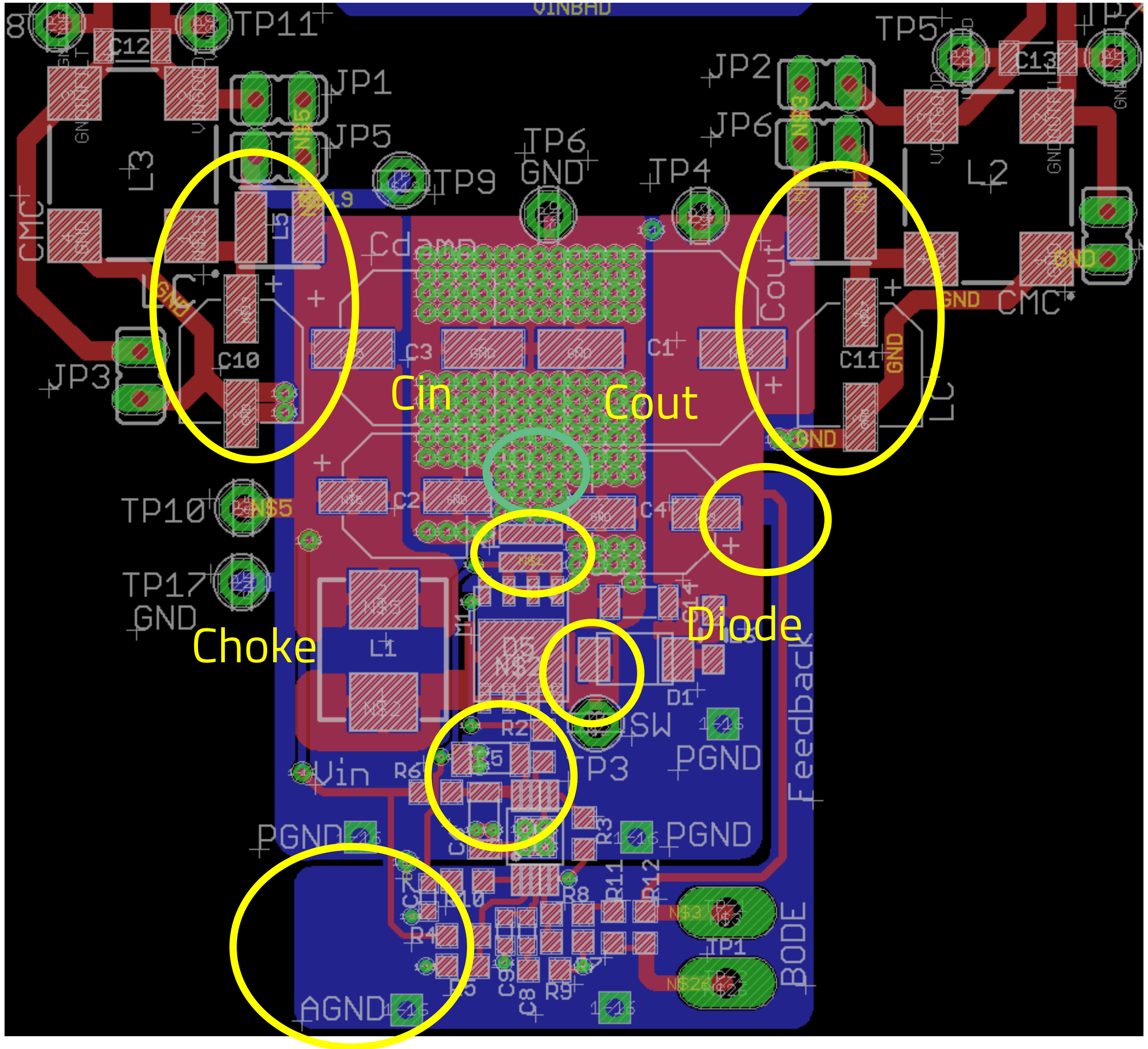


Schematic Good Design

19V → 24V/0,5A

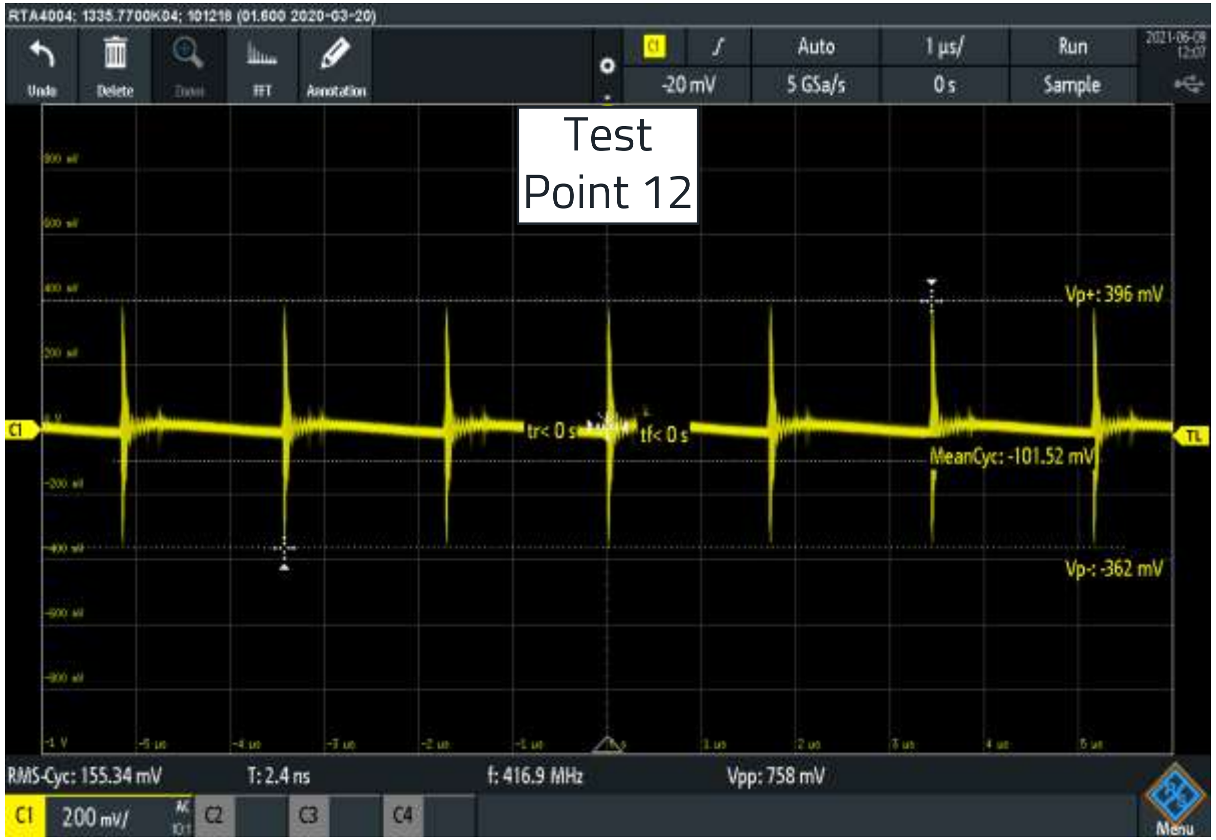


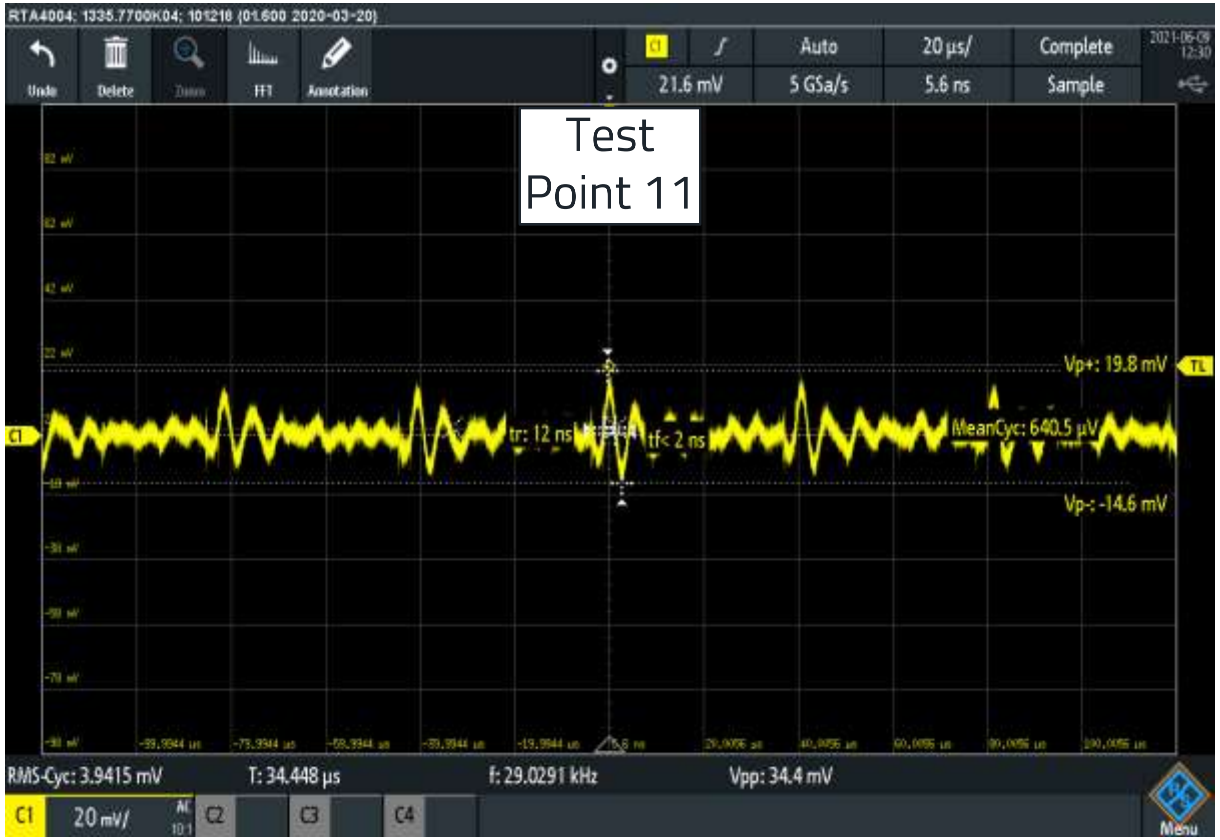
PCB Layout Good Design



Time Domain Measurements

PCB Test Points



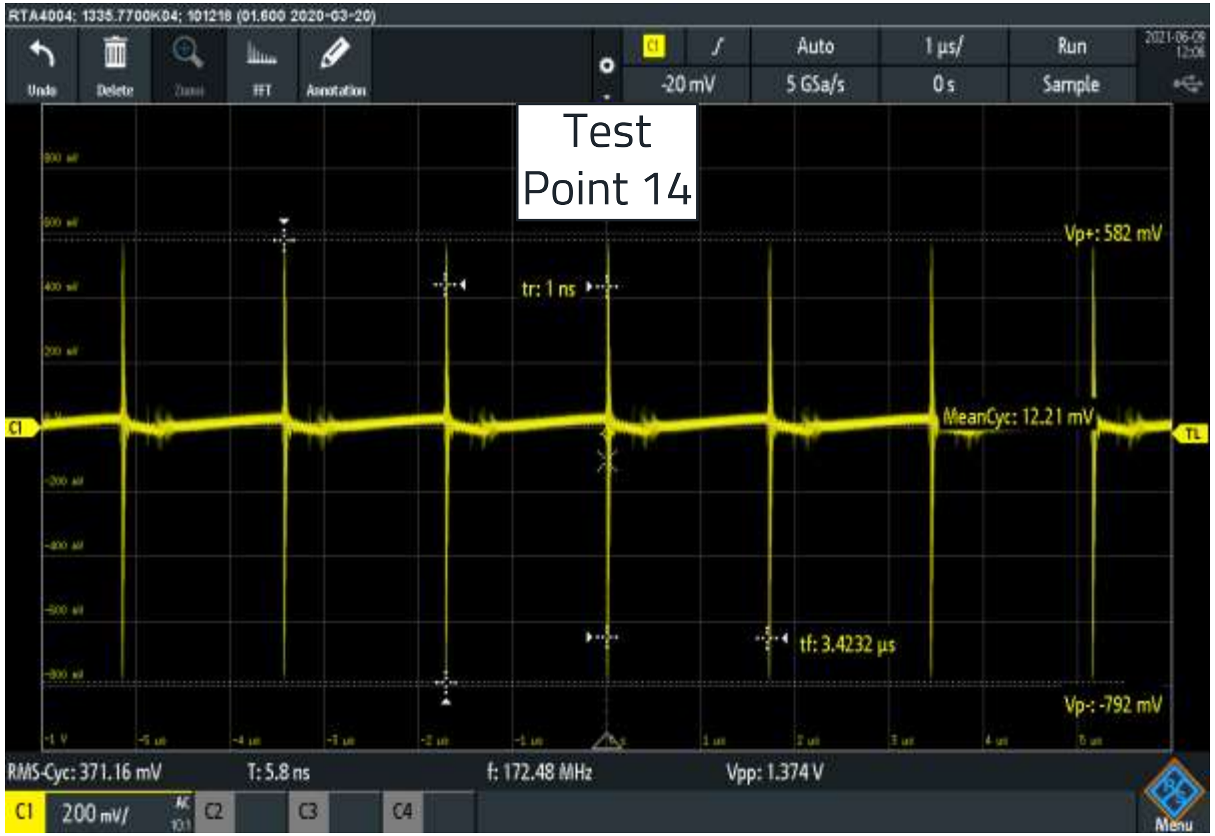


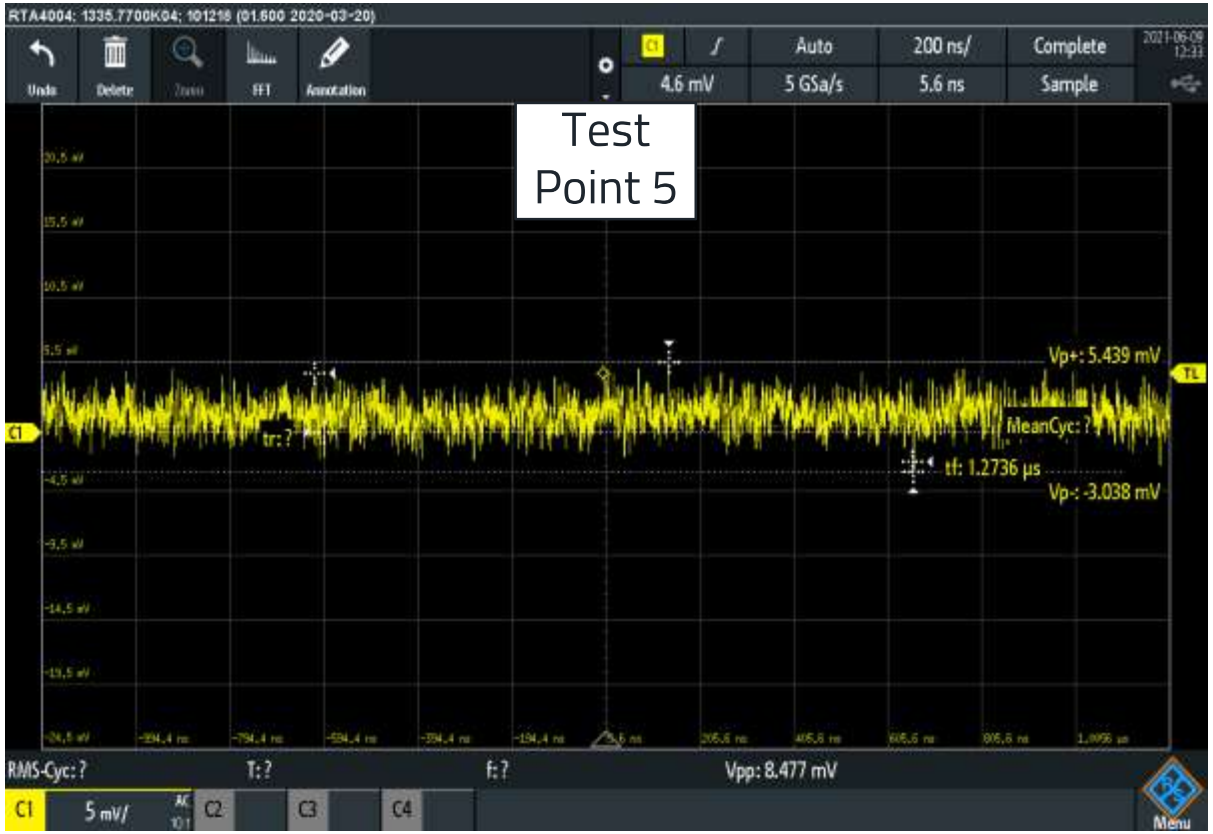
Bad Design Vin Ripple/Noise: 758mVpp

Good Design Vin Ripple/Noise: 34mVpp

Time Domain Measurements

PCB Test Points





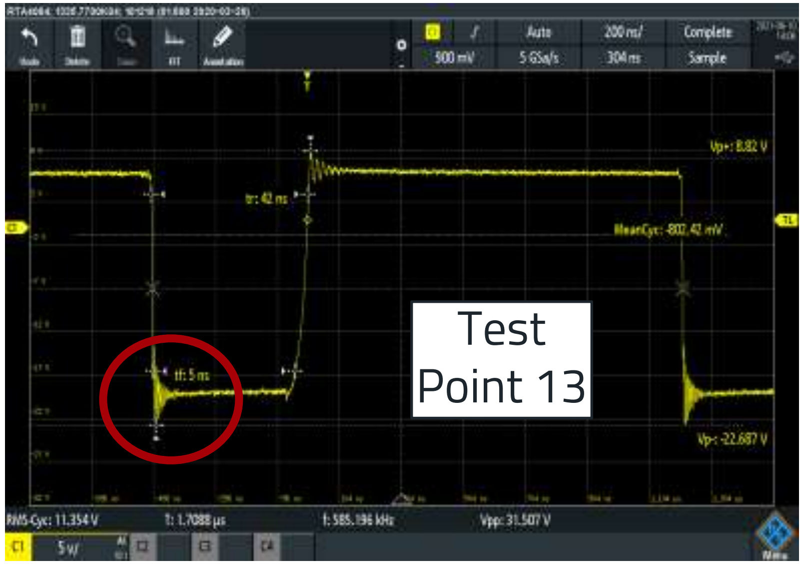
Bad Design Vout Ripple/Noise: 1374mVpp

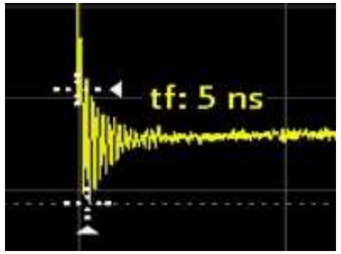
Good Design Vout Ripple/Noise: 8mVpp

Time Domain Measurements

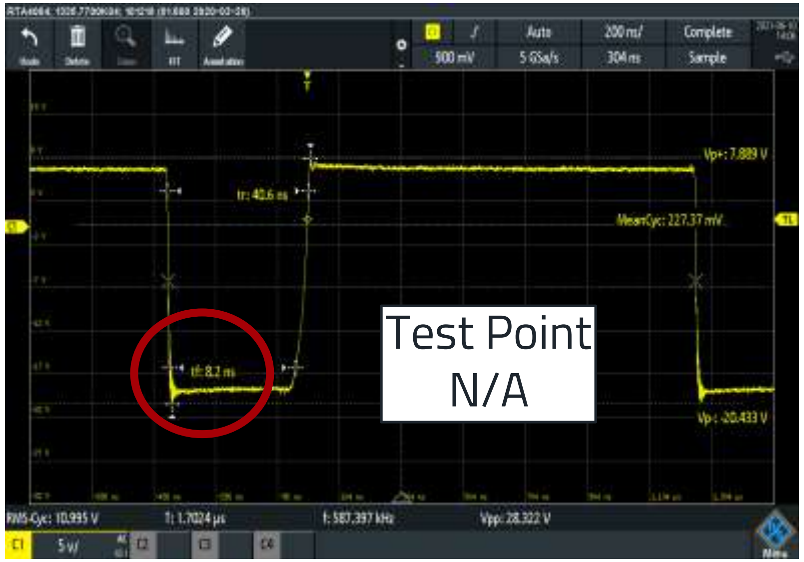
Switch Node Voltage

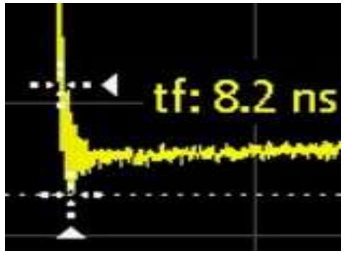
Bad Design



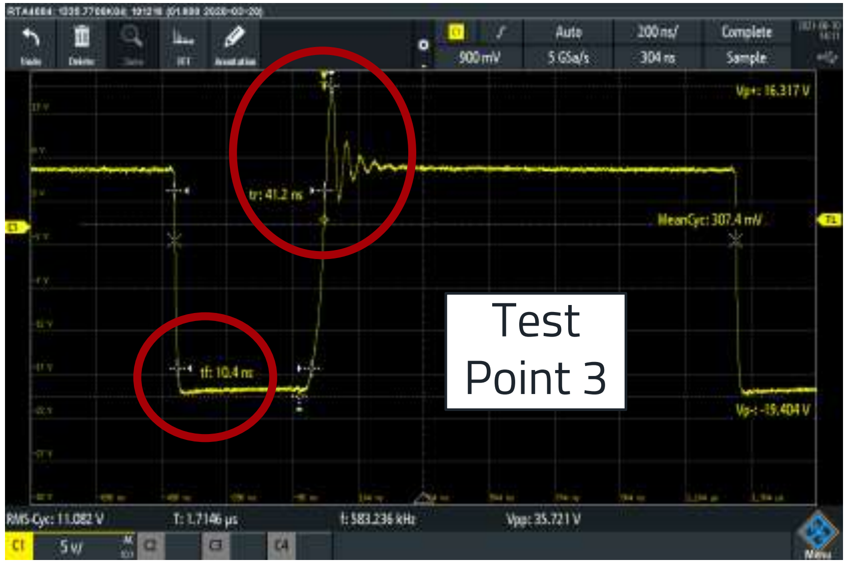


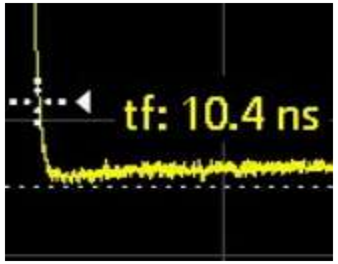
Good Design no Ferrite

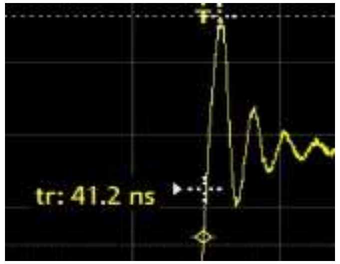




Good Design with Ferrite

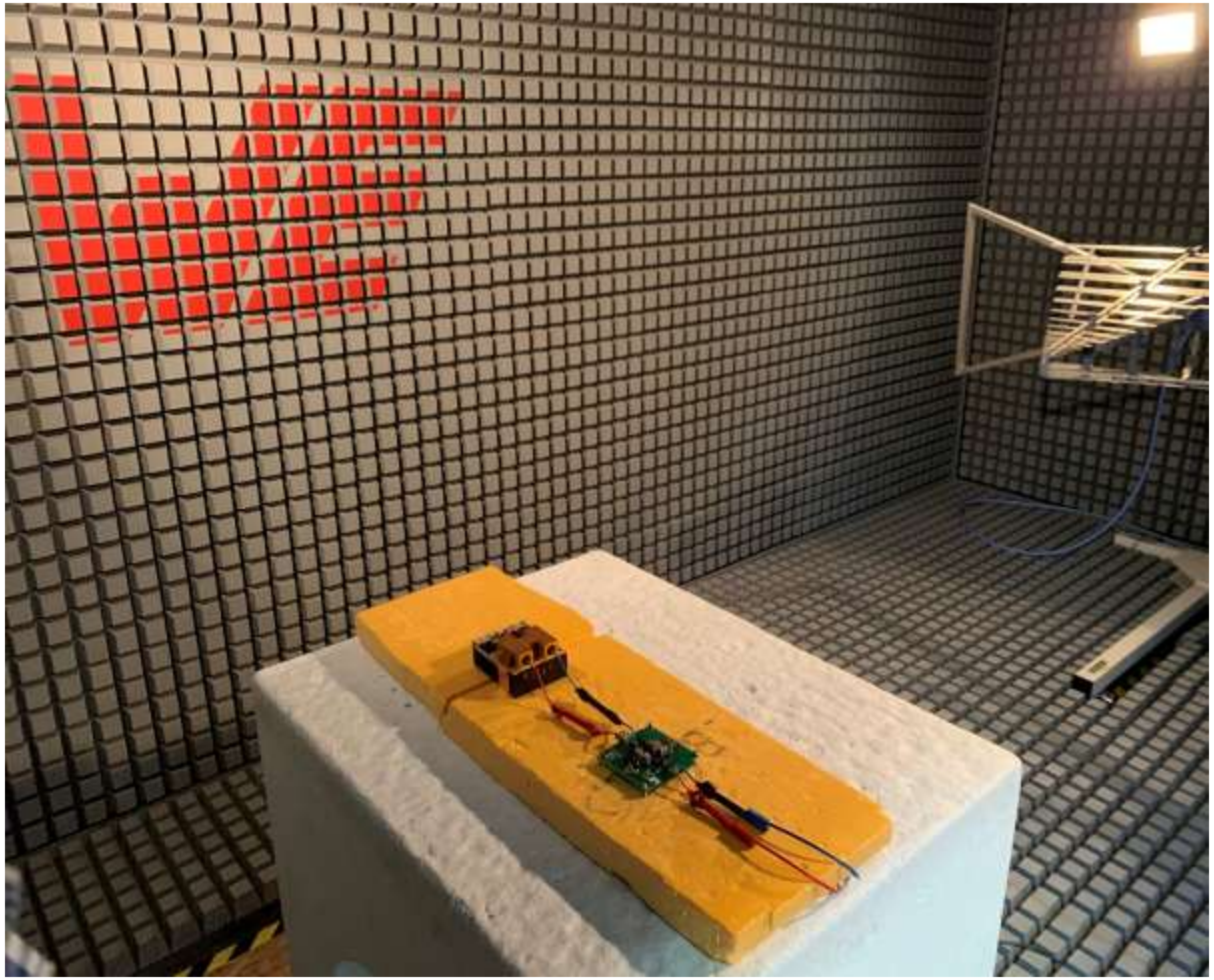


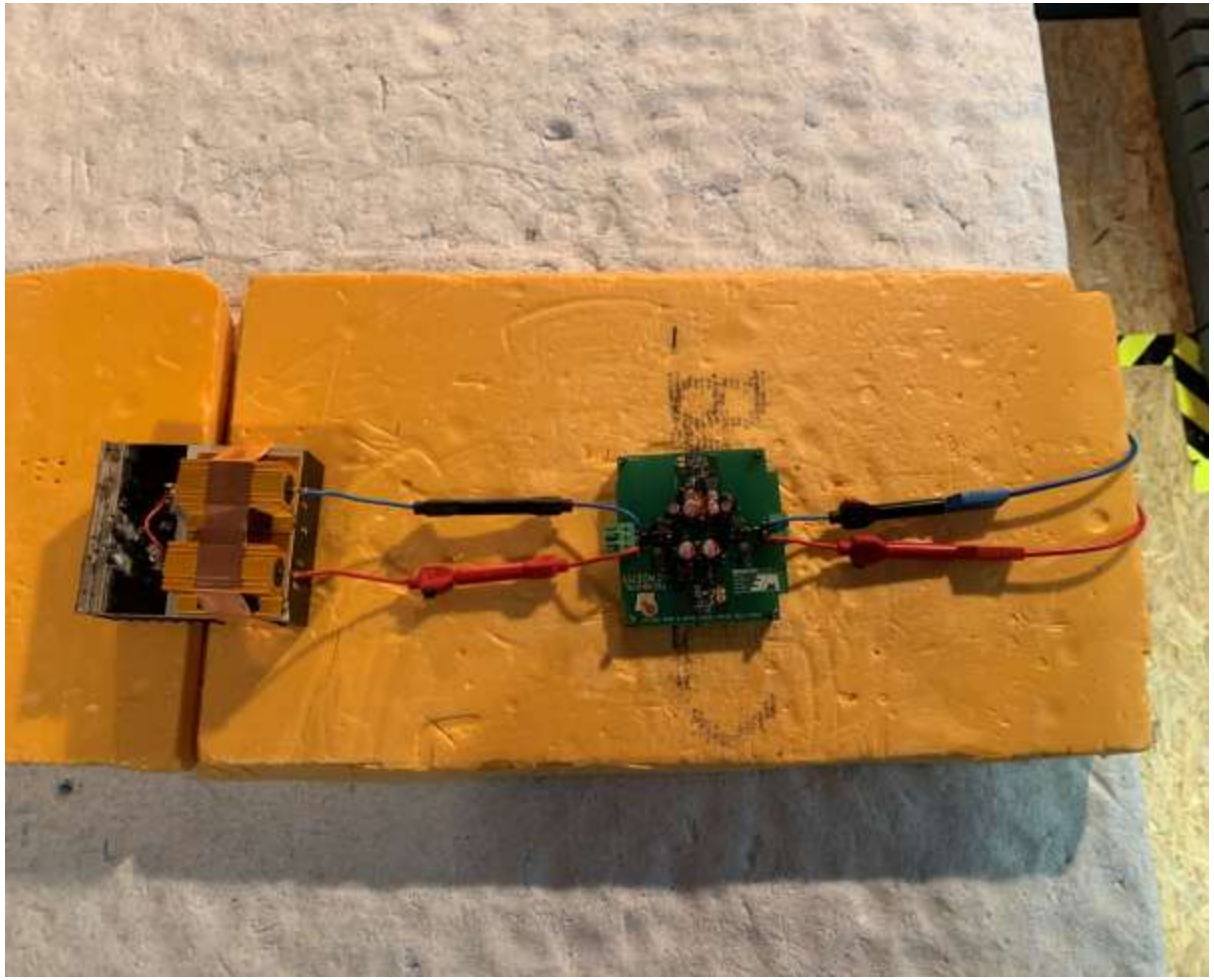




EMC Test Lab

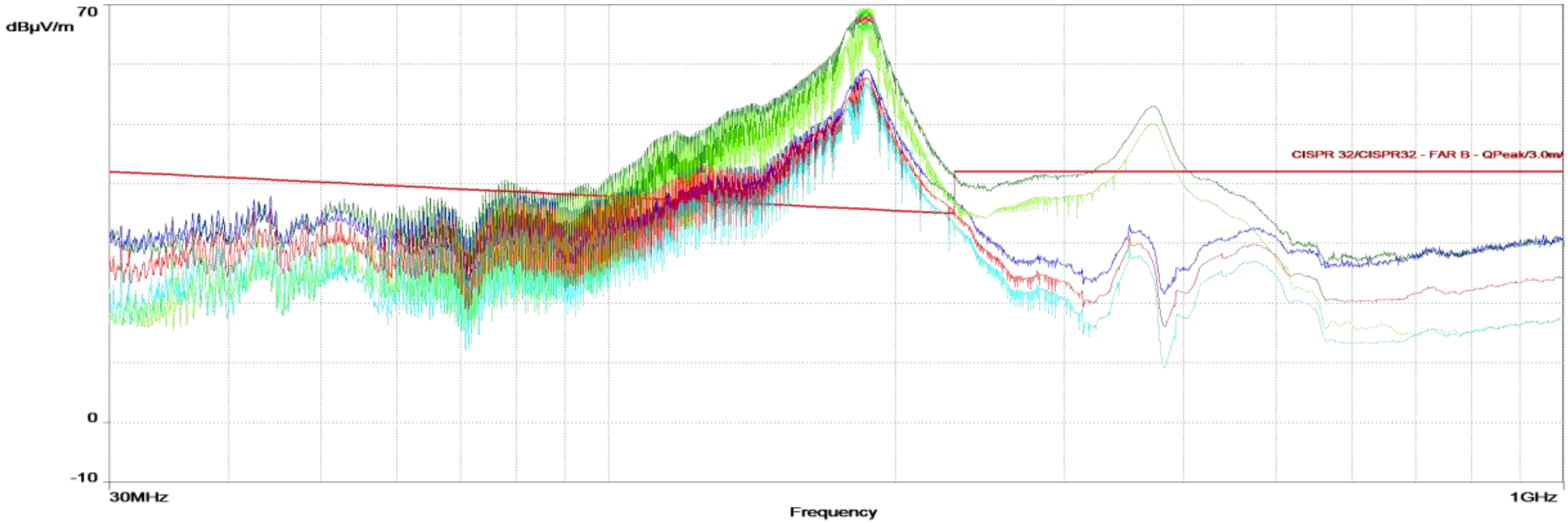
CISPR32 Radiated Emission





EMC Test Lab

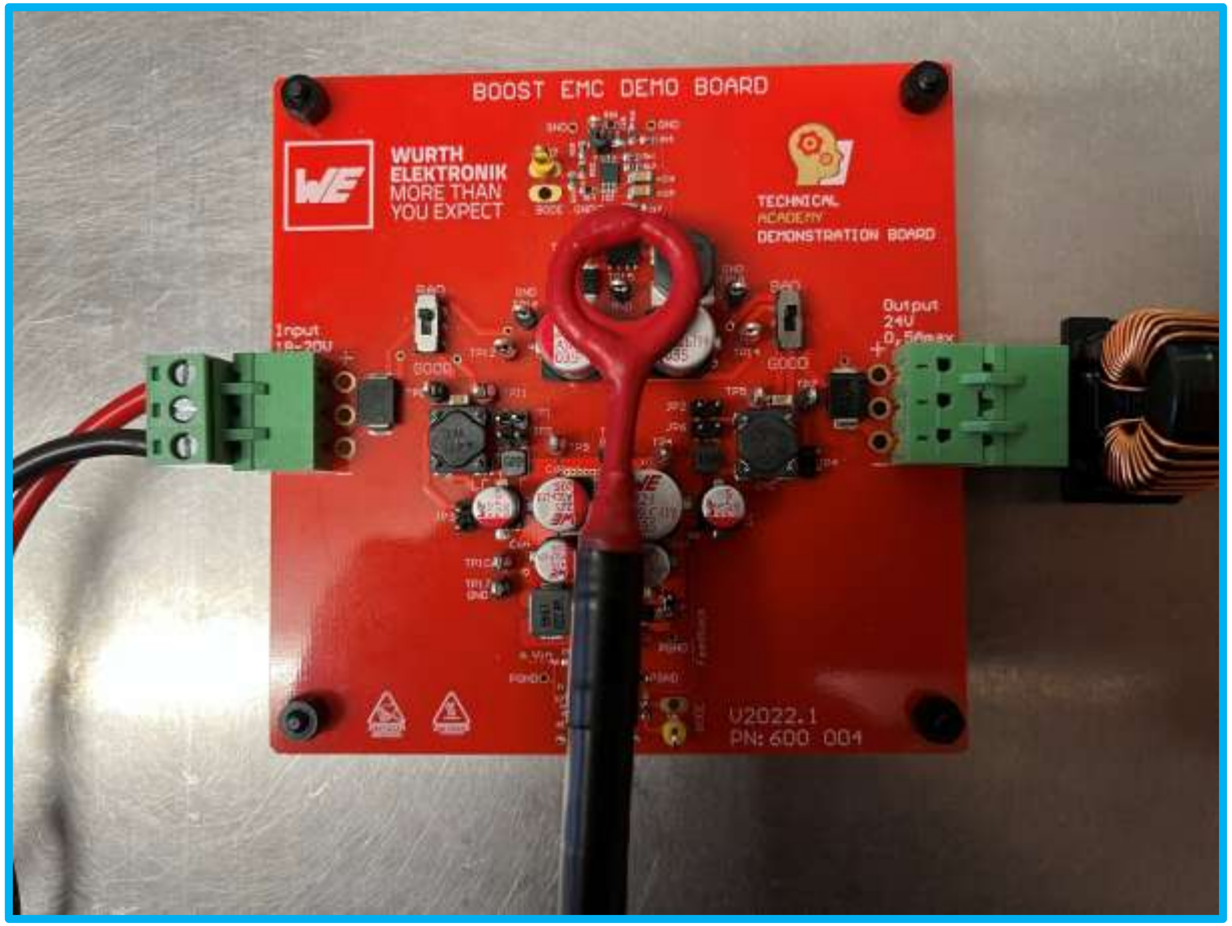
CISPR32 Radiated Emission

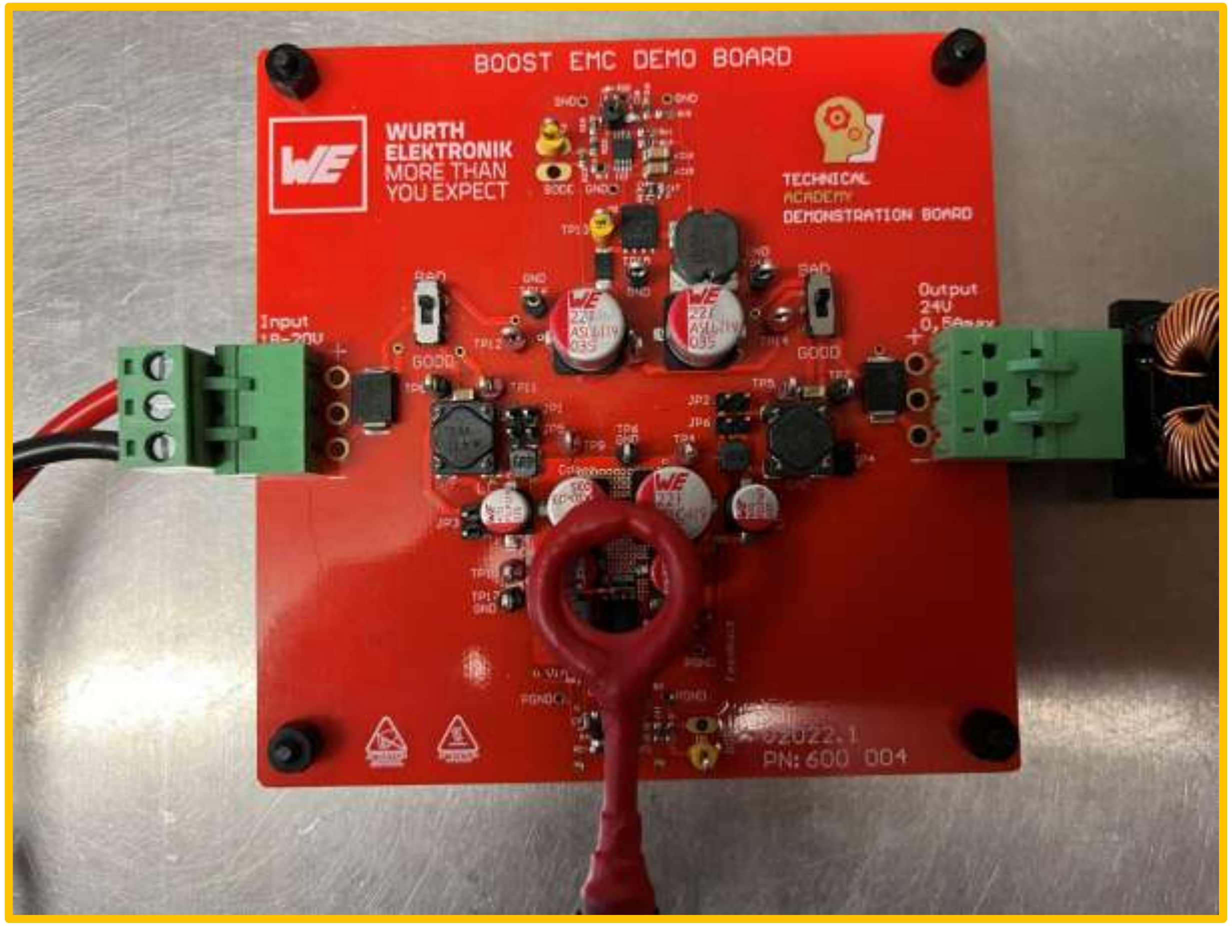


Bad Design

Near Field 1GHz (H-Field Probe)

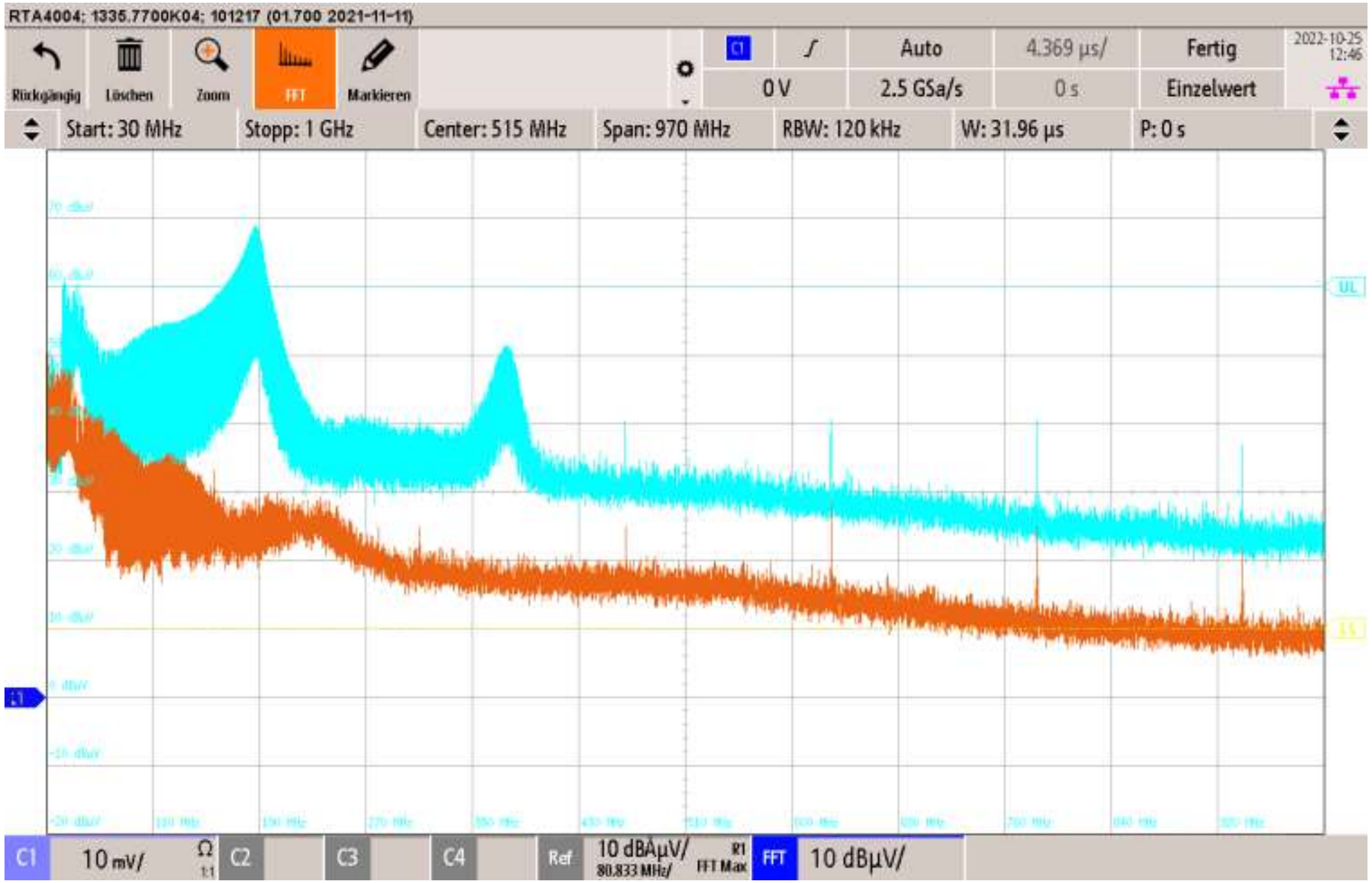
Bad vs. Good





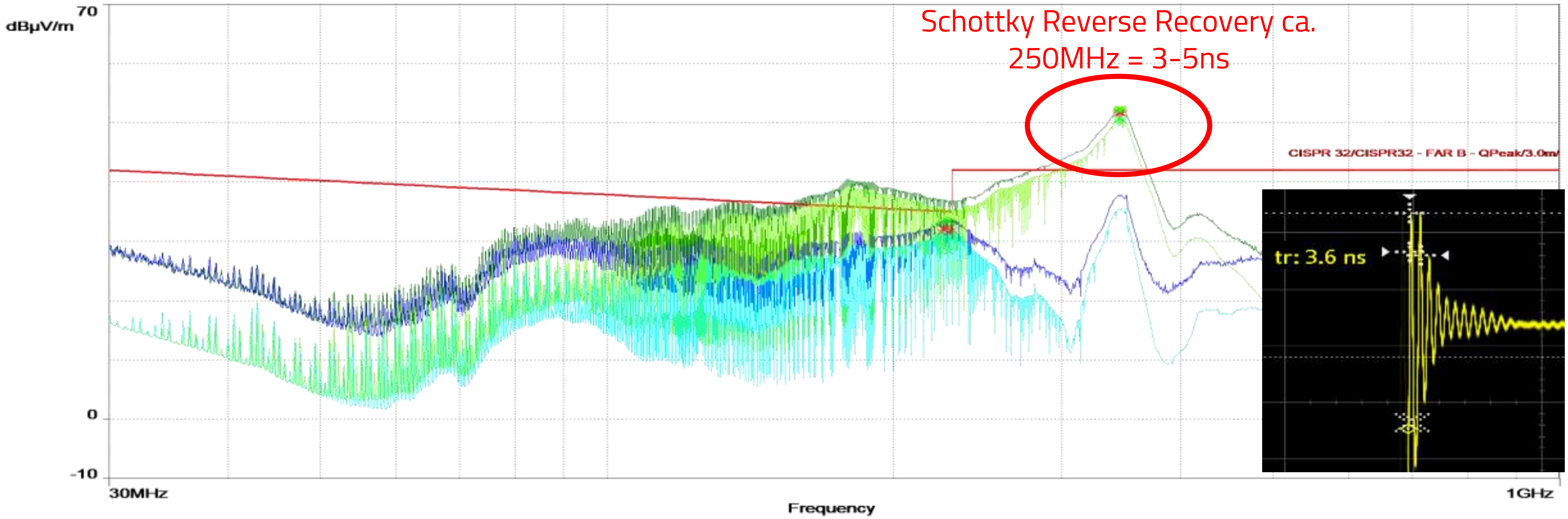
Near Field 1GHz (H-Field Probe - Big Loop)

Bad vs. Good



EMC Test Lab

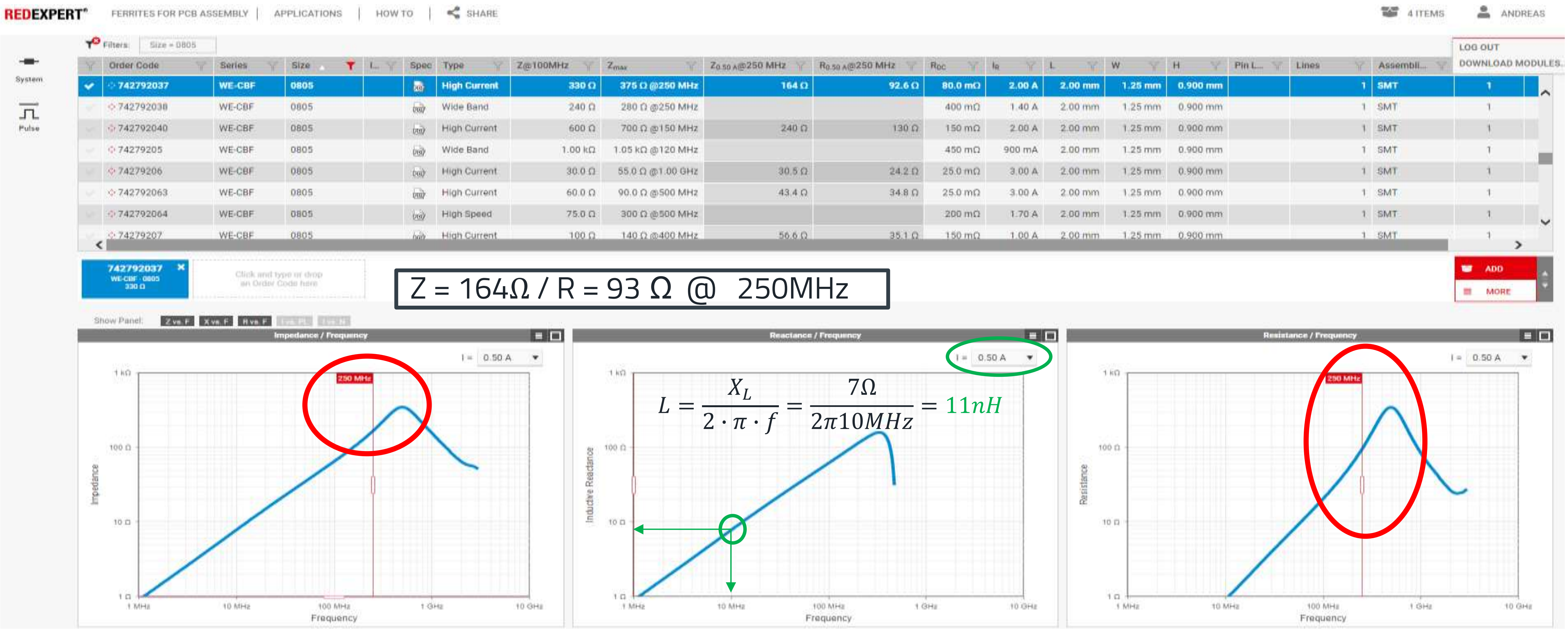
CISPR32 Radiated Emission



Good Design: No Filters and no Chip Bead Ferrite after Schottky Diode

Redexpert

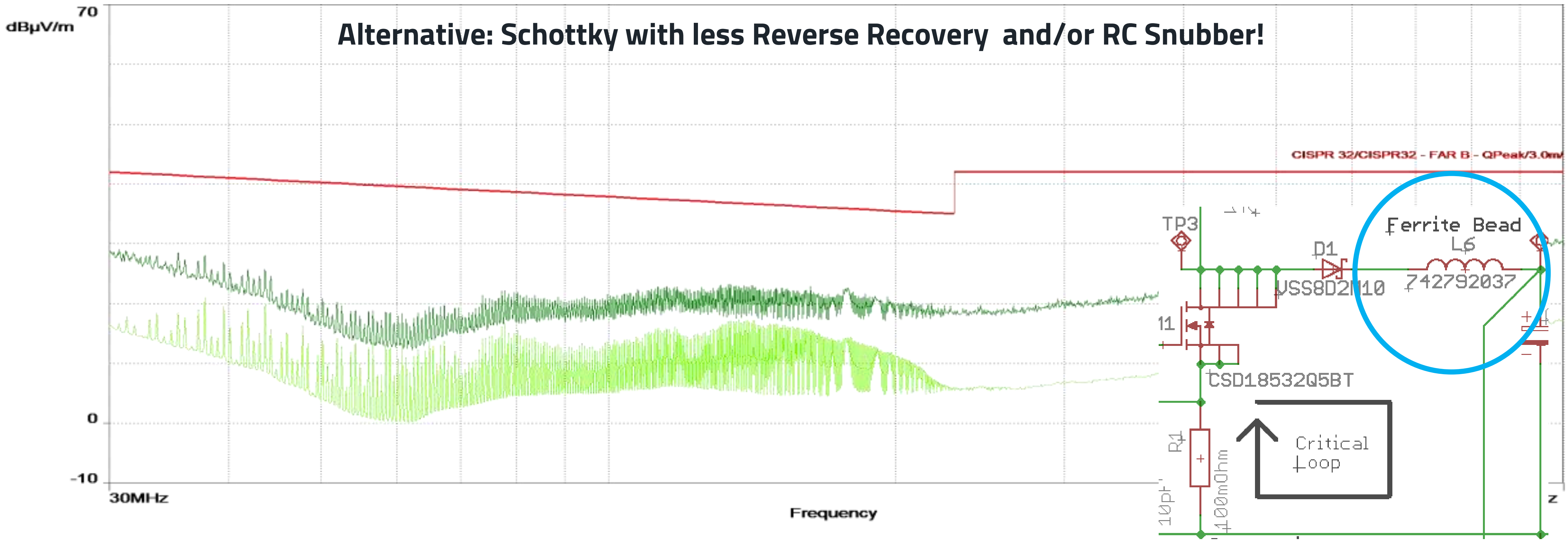
Chip Bead Selection @ 0,5A Iout and 250MHz → Reactance XL under 10MHz as low as possible!



Order Code	Series	Size	L...	Spec	Type	Z@100MHz	Z_{max}	$Z_{0.50\,A}$@250 MHz	$R_{0.50\,A}$@250 MHz	R_{DC}	I_R	L	W	H	Pin L...	Lines	Assembli...	
742792037	WE-CBF	0805			High Current	330 Ω	375 Ω @250 MHz	164 Ω	92.6 Ω	80.0 mΩ	2.00 A	2.00 mm	1.25 mm	0.900 mm		1	SMT	1
742792038	WE-CBF	0805			Wide Band	240 Ω	280 Ω @250 MHz			400 mΩ	1.40 A	2.00 mm	1.25 mm	0.900 mm		1	SMT	1
742792040	WE-CBF	0805			High Current	600 Ω	700 Ω @150 MHz	240 Ω	130 Ω	150 mΩ	2.00 A	2.00 mm	1.25 mm	0.900 mm		1	SMT	1
74279205	WE-CBF	0805			Wide Band	1.00 kΩ	1.05 kΩ @120 MHz			450 mΩ	900 mA	2.00 mm	1.25 mm	0.900 mm		1	SMT	1
74279206	WE-CBF	0805			High Current	30.0 Ω	55.0 Ω @1.00 GHz	30.5 Ω	24.2 Ω	25.0 mΩ	3.00 A	2.00 mm	1.25 mm	0.900 mm		1	SMT	1
742792063	WE-CBF	0805			High Current	60.0 Ω	90.0 Ω @500 MHz	43.4 Ω	34.8 Ω	25.0 mΩ	3.00 A	2.00 mm	1.25 mm	0.900 mm		1	SMT	1
742792064	WE-CBF	0805			High Speed	75.0 Ω	300 Ω @500 MHz			200 mΩ	1.70 A	2.00 mm	1.25 mm	0.900 mm		1	SMT	1
74279207	WE-CBF	0805			High Current	100 Ω	140 Ω @400 MHz	56.6 Ω	35.1 Ω	150 mΩ	1.00 A	2.00 mm	1.25 mm	0.900 mm		1	SMT	1

EMC Test Lab

CISPR32 Radiated Emission



Good Design: No Filters but with Chip Bead Ferrite after Schottky Diode

SEPIC SNUBBER DESIGN

SEPIC using LM5155

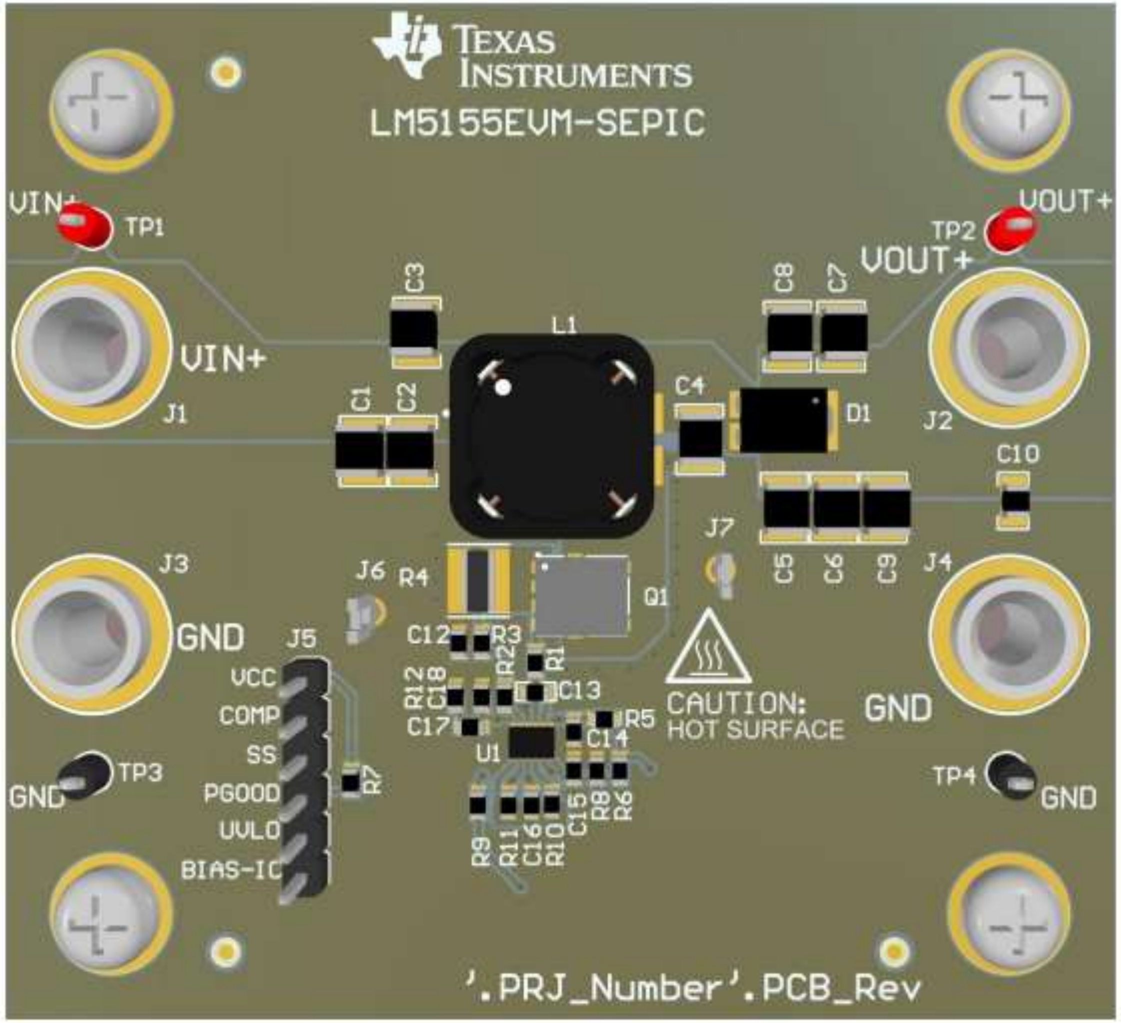
LM5155 SEPIC Calculator

LM5155EVM - Overview

General Specification

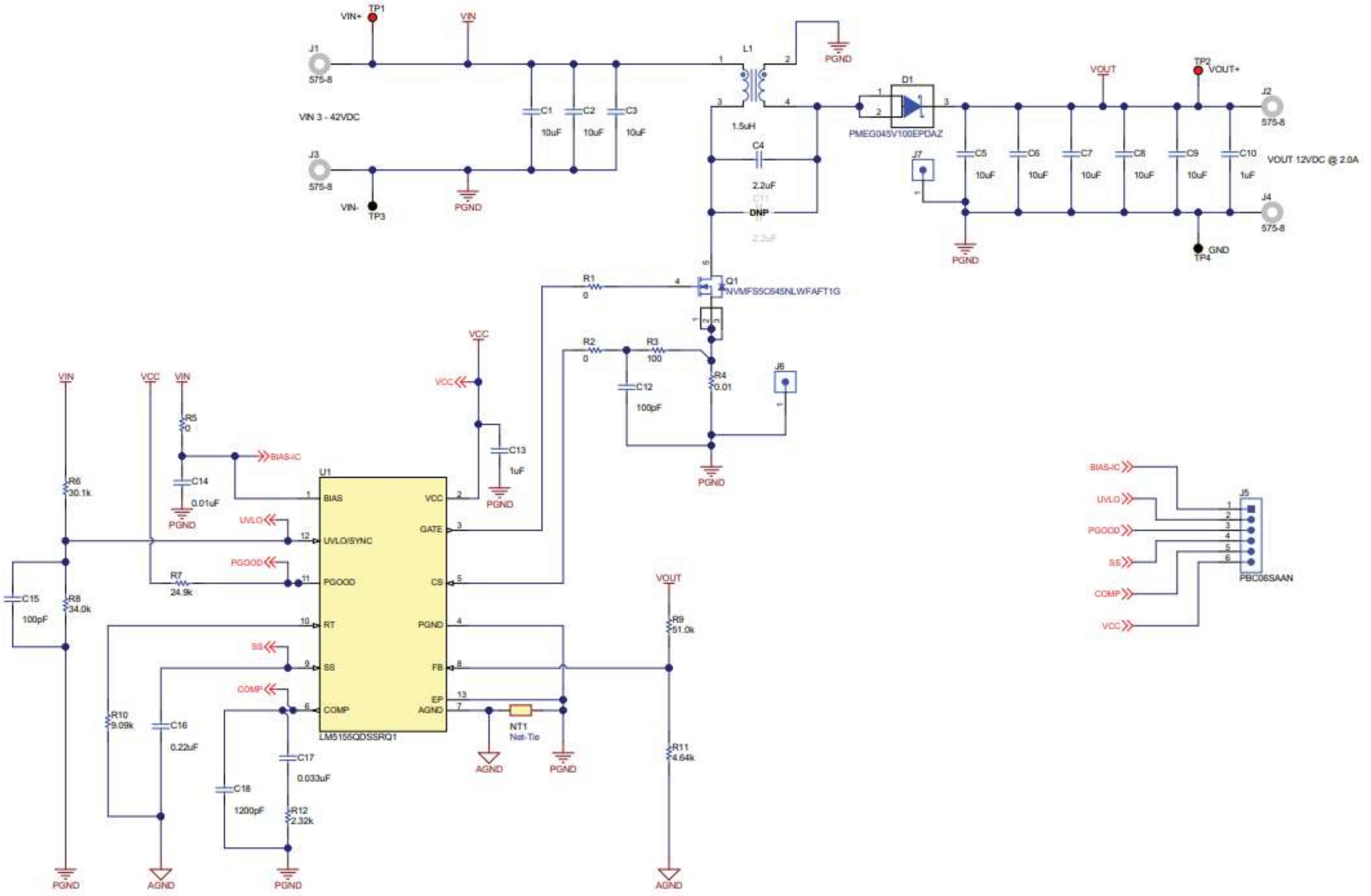
- DC/DC SEPIC Converter
  - V_{in} = 6-42V
  - V_{out} = 12V
  - $I_{out,max}$ = 2A
  - $P_{out,max}$ = 24W
  - f_{sw} ≈ 2.2MHz

- Inductor: 1.5uH WE-DD 7448700015



SEPIC using LM5155

LM5155EVM - Schematic

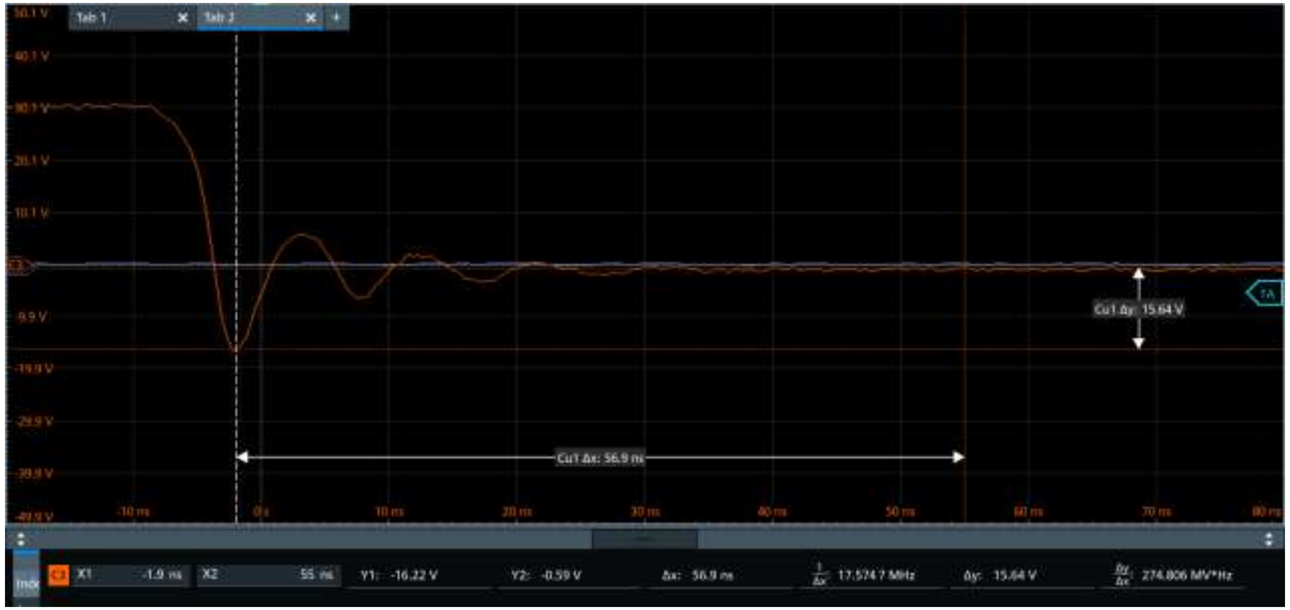


SEPIC using LM5155

Snubber Circuit Design & Testing

- Time domain investigation:
  - Noisy reverse recovery of diode.
  - Measure frequency of ringing -> fo = 136MHz
  - Introduce an external cap in // with Diode -> C1 = 110pF
  - Measure new frequency of ringing -> f1 = 111MHz
  - Calculate the ratio m = fo/f1 = 1.225
  - Calculate parasitic Co = C1/(m^2-1) = 219.48pF
  - Calculate parasitic Lo = 1/[(2πfo)^2 x Co] = 6.24nH
  - Calculate Rsnub = $\sqrt{L_o/C_o}$ = 5.33Ω
  - Used Csnub = 220pF and Rsnub = 4.4Ω

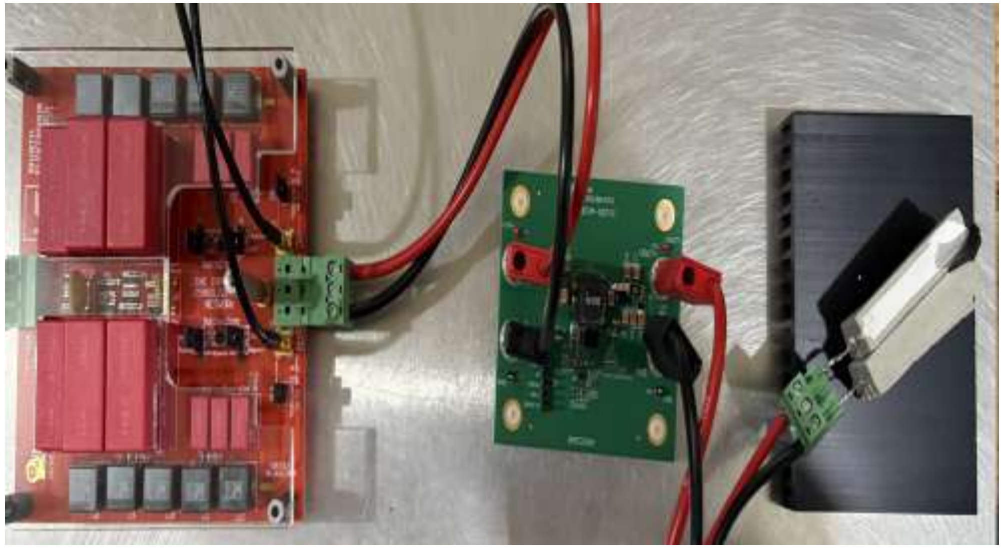
Qs: Initial reverse spike can be reduced by ……..?



Sources:
https://www.ti.com/document-viewer/lit/html/SSZTBC7
https://www.eetimes.com/calculating-an-r-c-snubber/?_ga

SEPIC using LM5155

PRACTICAL DEMO



SNUBBER Design

Loop Current low coupling factor k

Loop Current high coupling factor k

- Modified Board:
  - V_{in} = 10-32V
  - V_{out} = 12V
  - $I_{out,max}$ = 2A
  - $P_{out,max}$ = 24W
  - f_{sw} ≈ 500kHz
- Inductor:
  - 15uH WE-MCRI 7448990150
  - K = 0.995
- Cac = 2.2uF vs (// ≈ 22uF)

- NEW Inductor:
  - 15uH WE-MCRI
  - EXTENDED SERIES k = 0.7
- Cac = 2.2uF

ÇOK TEŞEKKÜR EDERİM

Mohamed Alalami
Technical Specialist