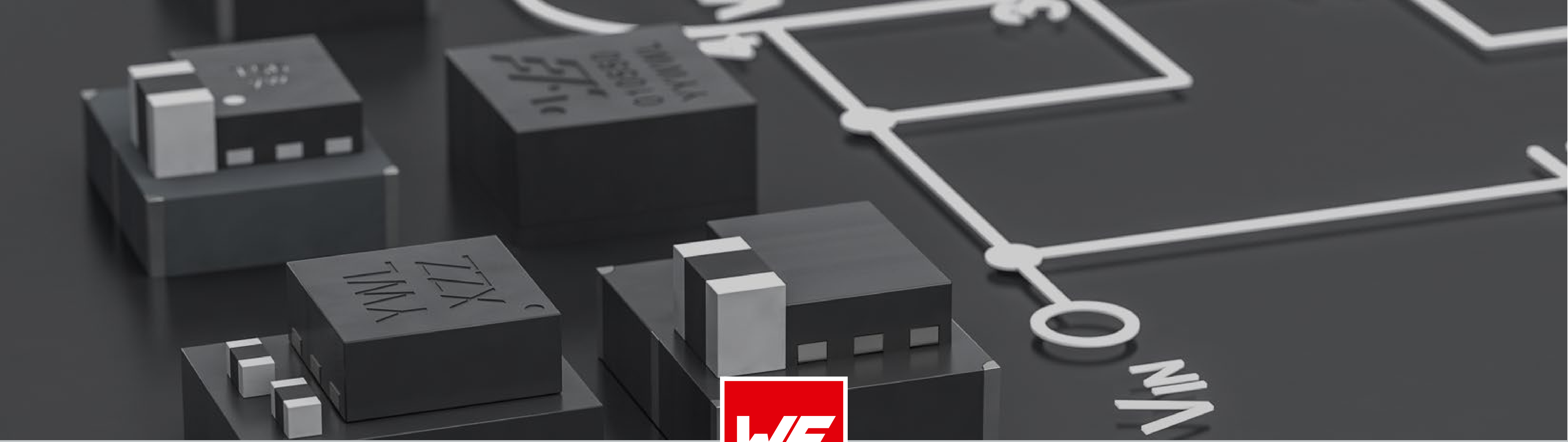

# DECREASING THE BOM AND IMPROVING COMMON MODE NOISE REDUCTION

Timur Uludag

**WÜRTH ELEKTRONIK** MORE THAN YOU EXPECT


NICHOLSON'S
FREEHOUSE
THE WALRUS & THE CARPENTER
DINING UPSTAIRS
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AIR-CONDITIONED BAR
DINING ROOM
FUNCTION ROOM
Available for Hire

# EMI-BASICS

# EMI-Basics

Differential Mode & Common Disturbances

## Differential Mode Disturbances

- Current in the supply lines in the opposite direction
- Input current from power module
- Dominant in non-isolated power modules

## Common Mode Disturbances

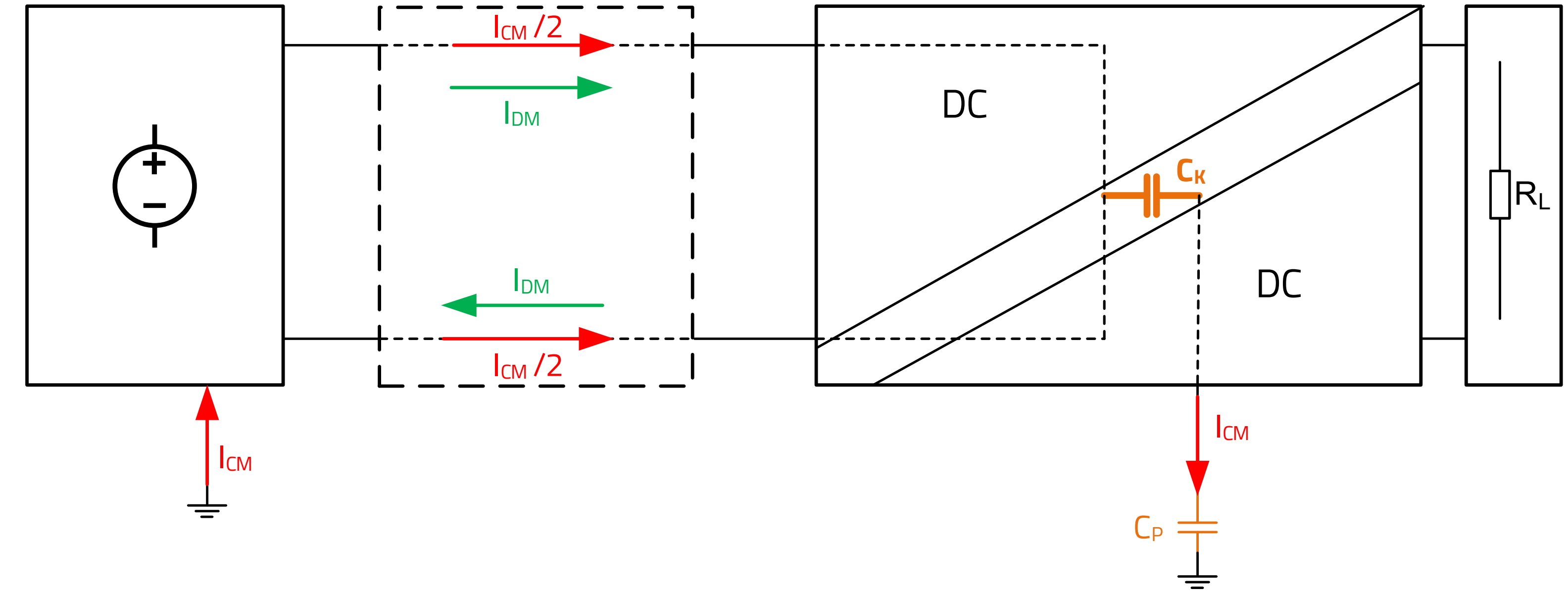
- Current in the supply lines in the same direction
- Mainly due to a high dv/dt of the switching elements
- Dominant for isolated modules

Power Supply / Disturbance source

Conductor / Coupling mechanism

Isolated Power Module / Disturbance source

Load



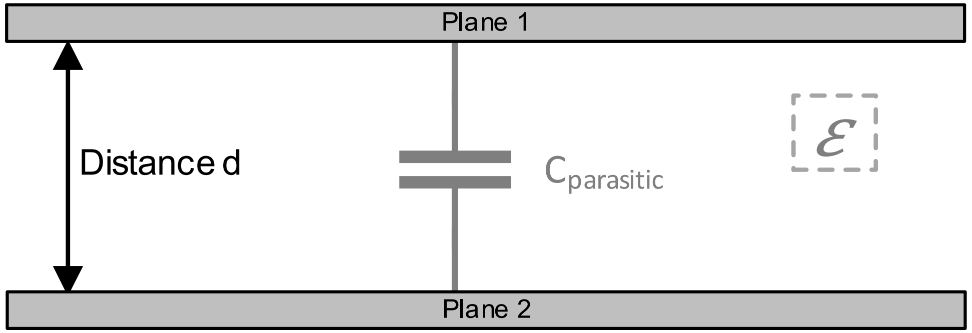
# EMI-Basics

Parasitics, parasitics and again parasitics

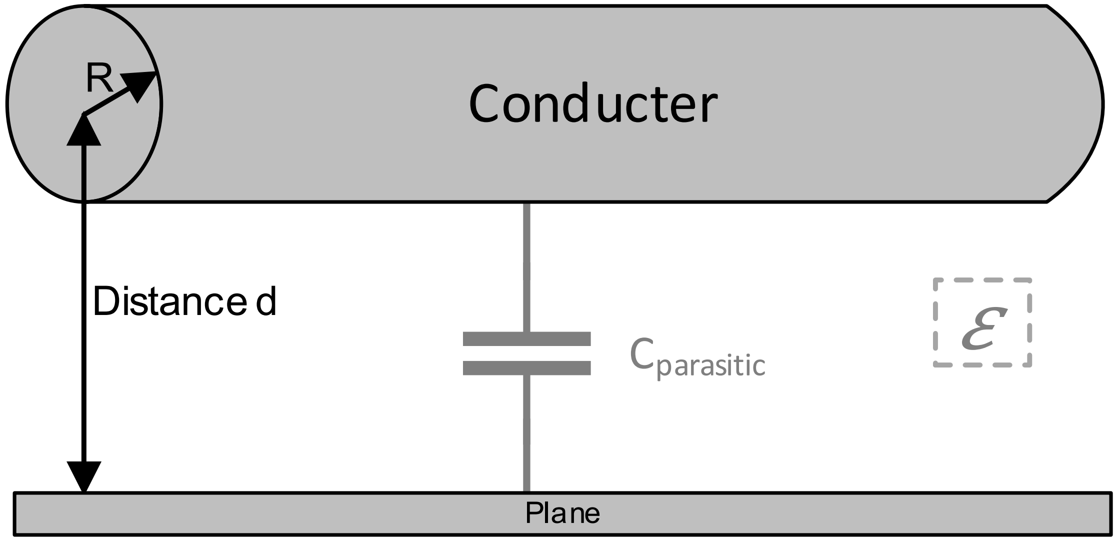
**Keep in mind:**

In every circuit, parasitic capacitances are present between different elements with different potentials.

Example 1: Two parallel planes



Example 2: One conductor parallel over a flat surface

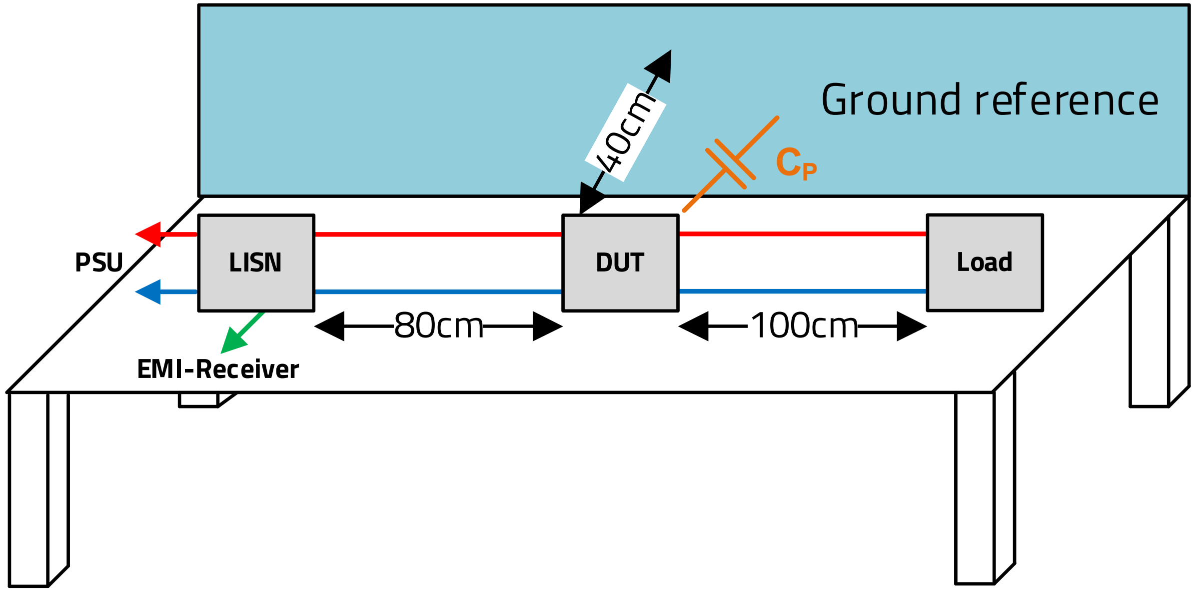


# EMI-Basics

## Defined EMI Test Setup

**Basic considerations:**

- Each application reshuffles the common mode cards
- That is why no general recipe can work
- For the time being, the consideration must be decoupled from the application
- Structure according to CISPR16-2-1is a sufficiently good compromise for the following considerations

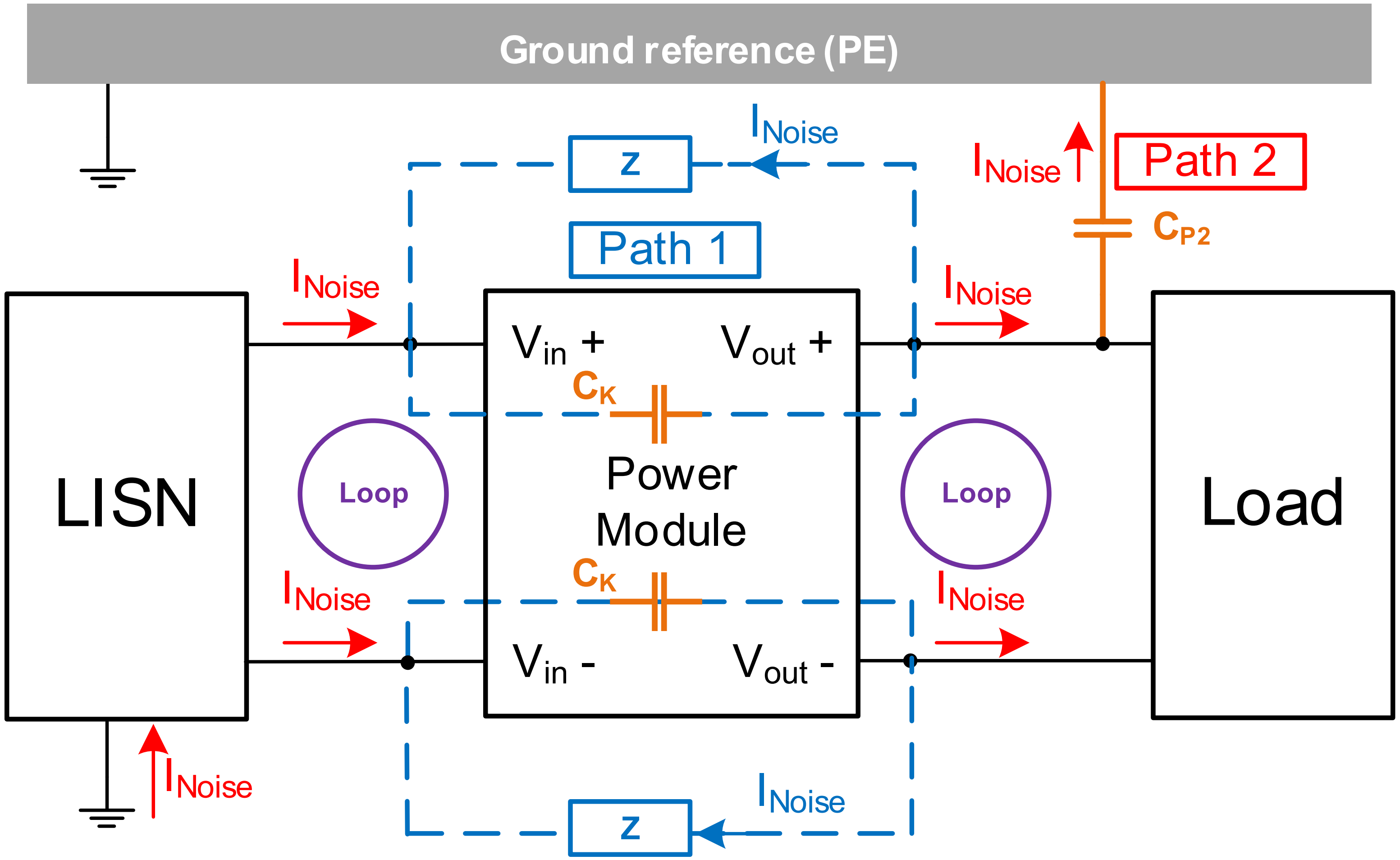


**EMI test setup structure based on CISPR16-2-1:**

- Power supply unit (PSU)
- EMI-Receiver
- Power Module (DUT)
- Electric load
- Line Impedance Stabilisation Network (LISN)

# EMI-Basics

Intention - Don´t let the Noise reach the LISN

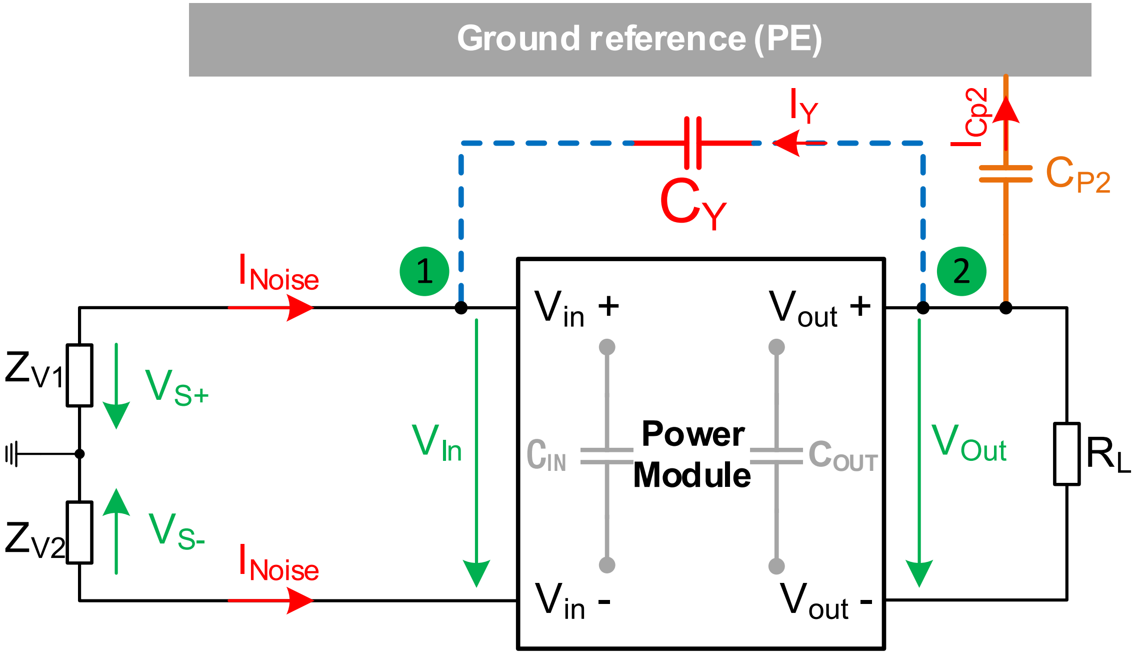


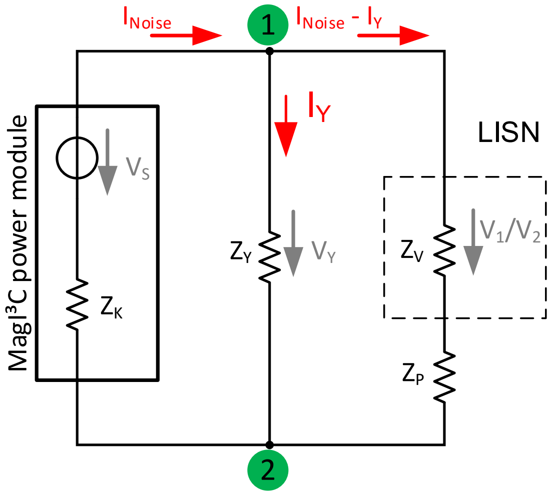
**1** **Common mode current with branch**

**2** **Common mode current with out branch**

# EMI MEETS KIRCHHOFF

## Electrical Equivalent Circuit - Simplified





**Between ① and ② additional bridging capacitor!**

# EMI-Basics

## Kirchhoff equations

### Voltage drop without Y capacitor:

$$V_1 = V_S \cdot \frac{Z_V}{Z_K + Z_P + Z_V}$$

### Voltage drop with Y capacitor:

$$V_2 = V_S \cdot \frac{Z_Y}{Z_K + Z_Y II (Z_V + Z_P)} \cdot \frac{Z_V}{Z_P + Z_V}$$

$V_1$, $V_2$ – voltage drop LISN

$Z_K$ – impedance interwinding coupling capacity

$Z_P$ – impedance parasitic coupling capacity

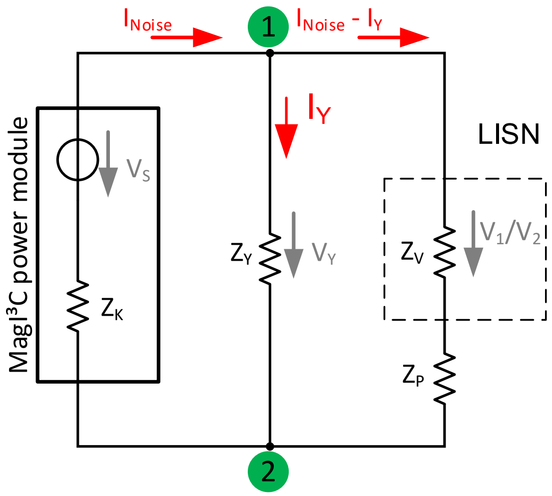
$Z_V$ – impedance LISN

$V_Y$ – voltage drop Y capacitor

$Z_Y$ – impedance of the Y capacitor

**→ Equation for attenuation**

$$d = \frac{Z_Y \cdot (Z_K + Z_P + Z_V)}{(Z_K + Z_Y II (Z_V + Z_P)) \cdot (Z_V + Z_P)}$$



# EMI-Basics

Gap Overlap Stitching - effective capacity based on the overlapping area

*Equation for capacitance C:*

$$C = \frac{A \cdot \varepsilon}{d} = \frac{l \cdot w \cdot \varepsilon}{d} \qquad \epsilon = \varepsilon_0 \cdot \varepsilon_r$$

C is the total ‘stitching’ capacity

d is the thickness of the insulating layer in the printed circuit board

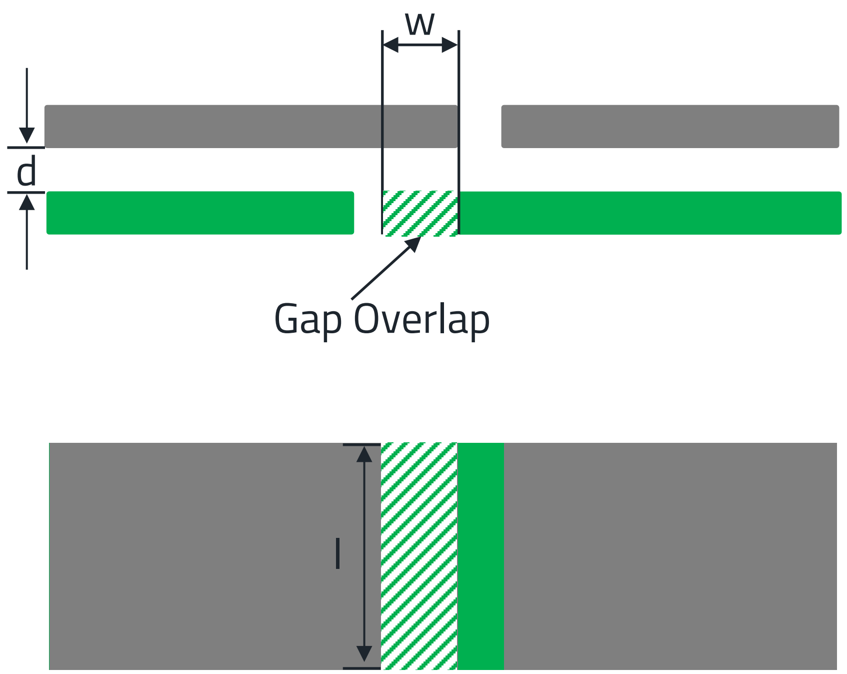
$\varepsilon_0$ is the permittivity of free space

$\varepsilon_r$ is the relative dielectric constant of the insulating material of the printed circuit board

w Width of the overlapping area

l Length of the overlapping area

*Geometric principle*



# EMI-Basics

## Design basis - realised layouts

**Based on an evaluation board PCB size of 80x80mm, 2- and 4-layer design is used to achieve the maximum capacity.**

The following variants are therefore compared::

- Two layers “without” Y capacitor
- Two layers with integrated Y capacitor while maintaining creepage distances equal to the module creepage distances
- Four layers with separate primary GND area on TOP and BOTTOM layer
- Four layers with max. capacity.

*→ More than 4 layers are not considered !!*

# REALISED DESIGNS- POWER MODULES

# Realised Designs-Power Modules

Power module for the layout

**Short specification:**

- Typ. 8pF parasitic coupling capacitance
- Small design (9 x 7 x 3.1mm)
- No external circuitry ($C_{in}$ and $C_{out}$ integrated)
- Functional isolation
- Short circuit protected
- UL62368 recognized

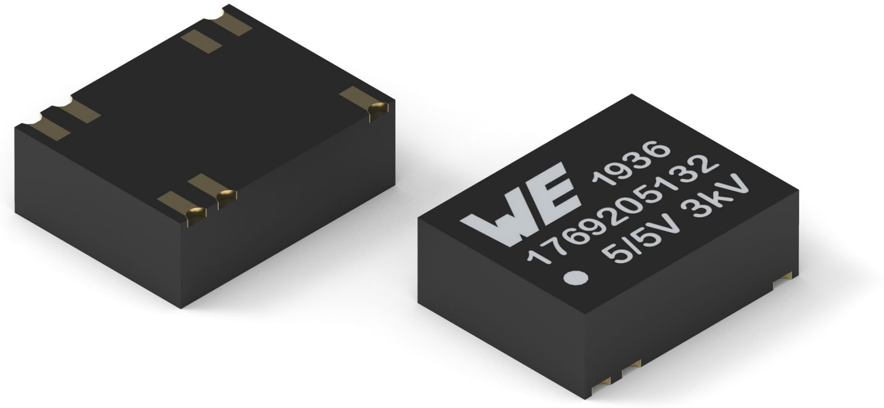
FIMM MagI³C Power Module

EN55032 Class B

FIX FREQ.

SCP

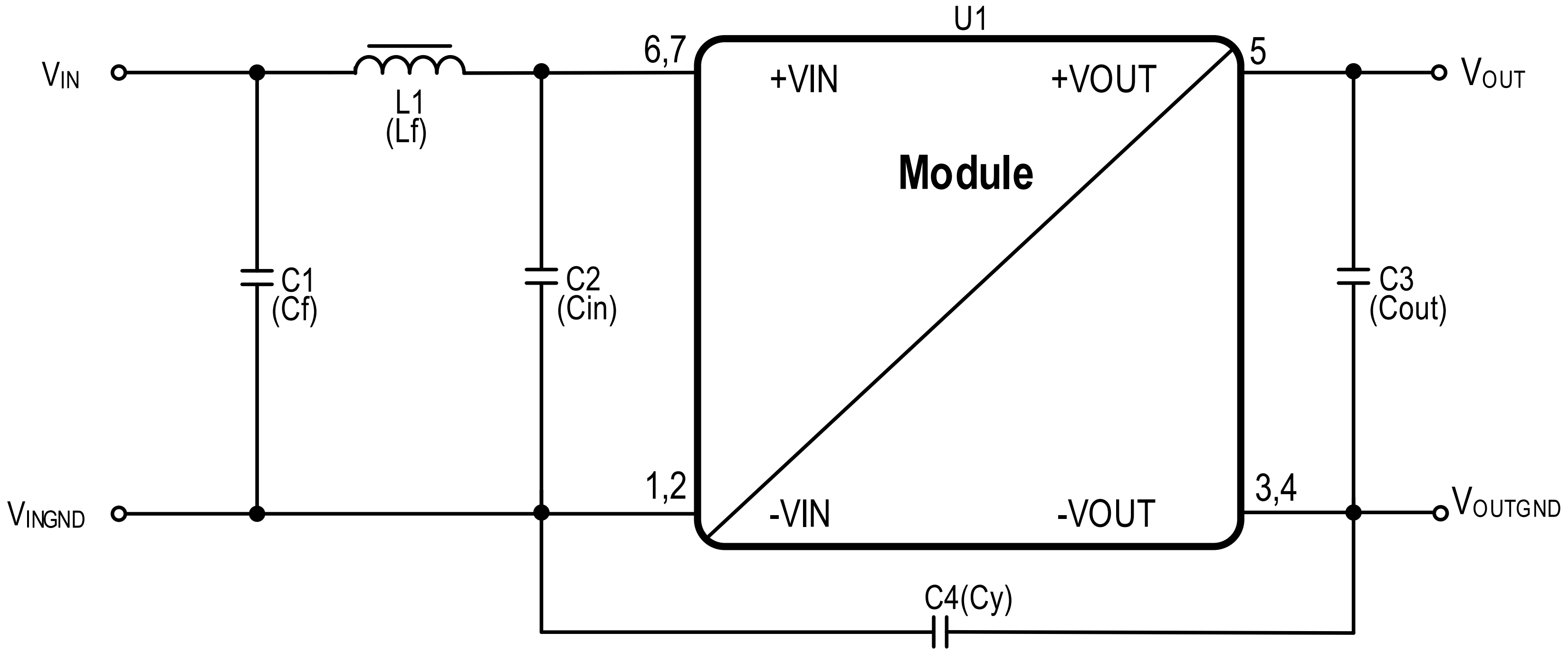
$T_a$105°C



**FIMM LGA-7 (1769205132)**

# Realised Designs-Power Modules

## EMI-Test Setup



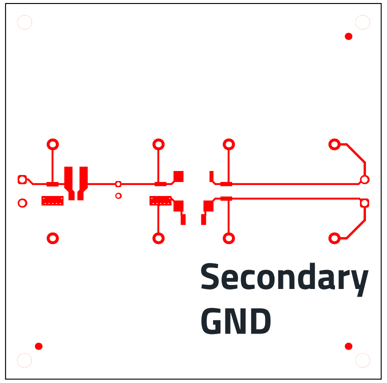
**Description:**

- Differential mode filter populated
- Output capacitor populated

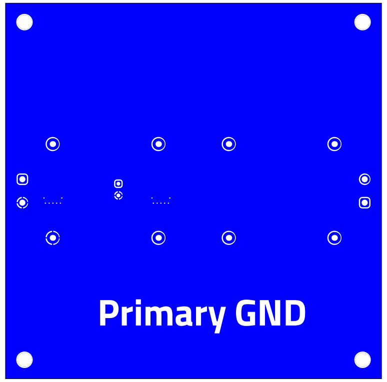
# Realised Designs-Power Modules

Layout Version 1 – 2 layers without Y capacitor

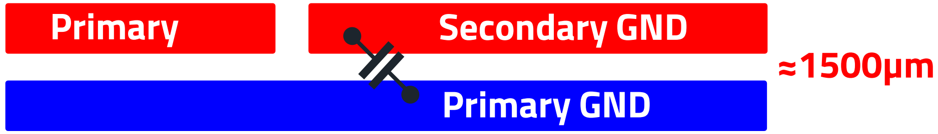
**TOP Layer**



**BOTTOM Layer**



Schematic structure:

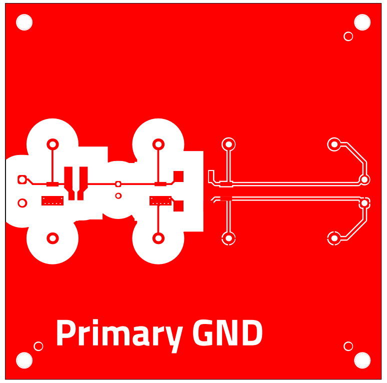


Effective capacity
→ $C_{PCB}$: ca. 14pF = Y-Cap

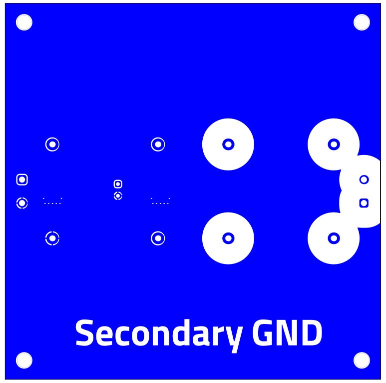
# Realised Designs-Power Modules

Layout Version 2 – 2 layers with 130pF integrated Y capacitor

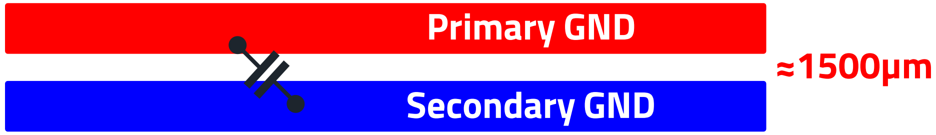
**TOP Layer**



**BOTTOM Layer**



Schematic structure:



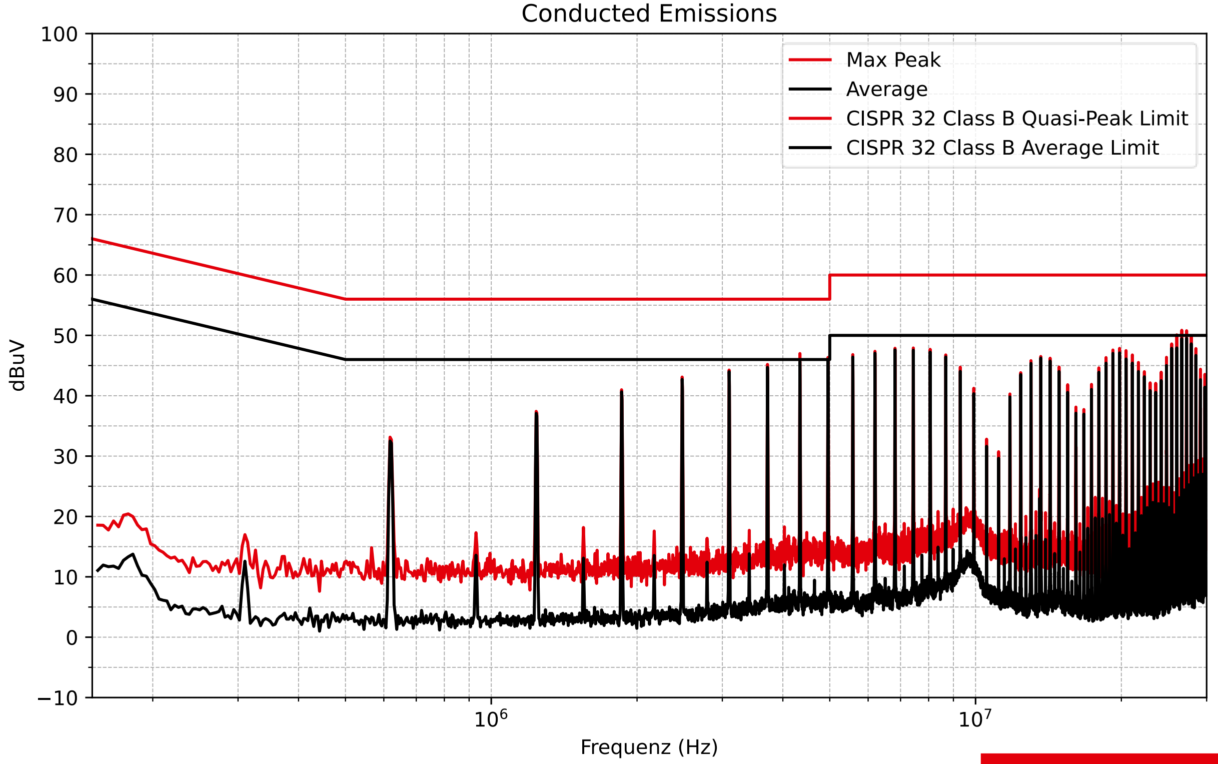
Effective capacity

→ $C_{PCB}$: ca. 130pF = Y-Cap

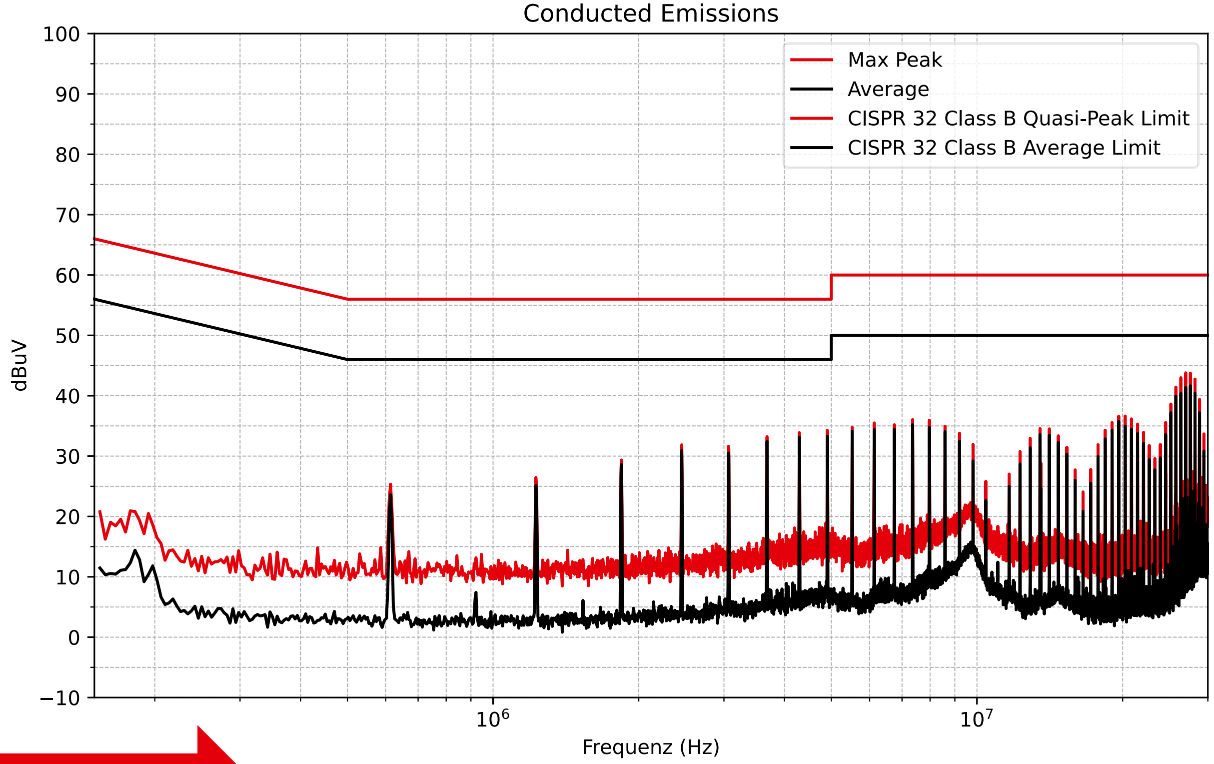
# Realised Designs-Power Modules

2-layer layout without Y capacitor / with integrated Y capacitor

## 2 layers without Y capacitor



## 2 layers with integrated 130pF Y capacitor



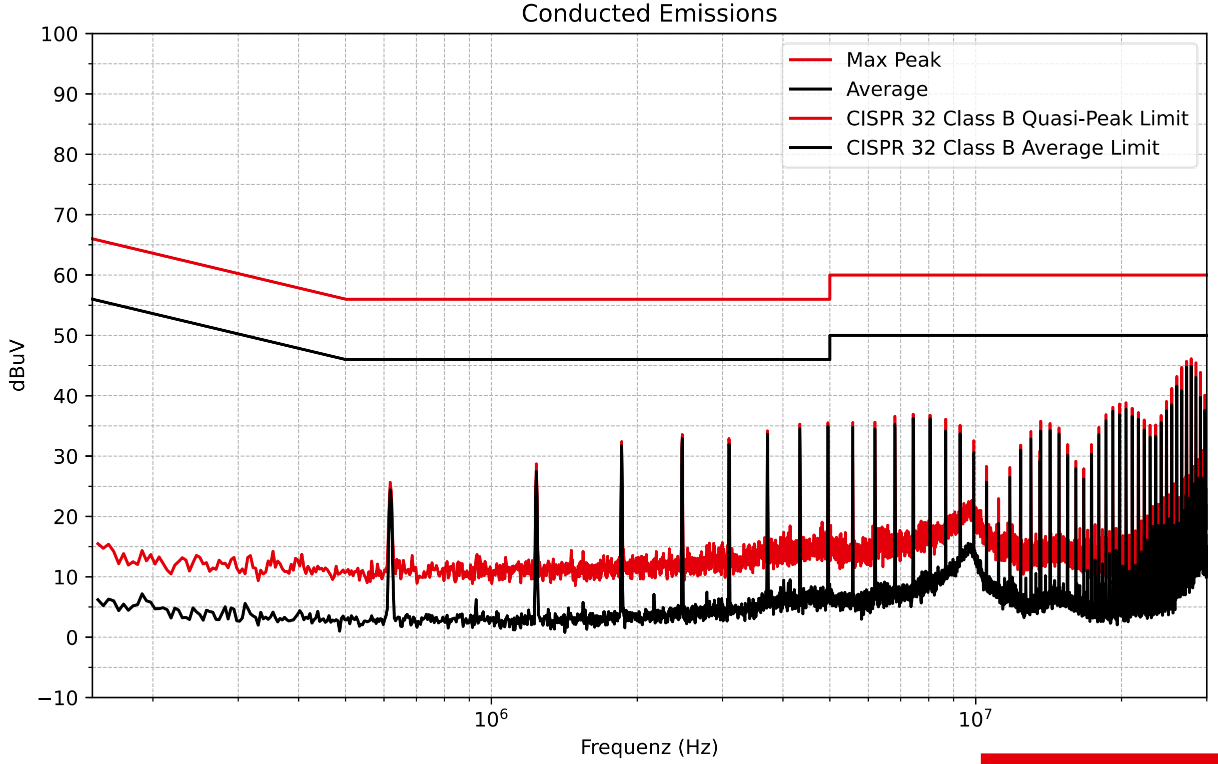
**≈ 10dB**

Based on the calculation for d you get approx.
12dB attenuation with 130pF Y capacitor

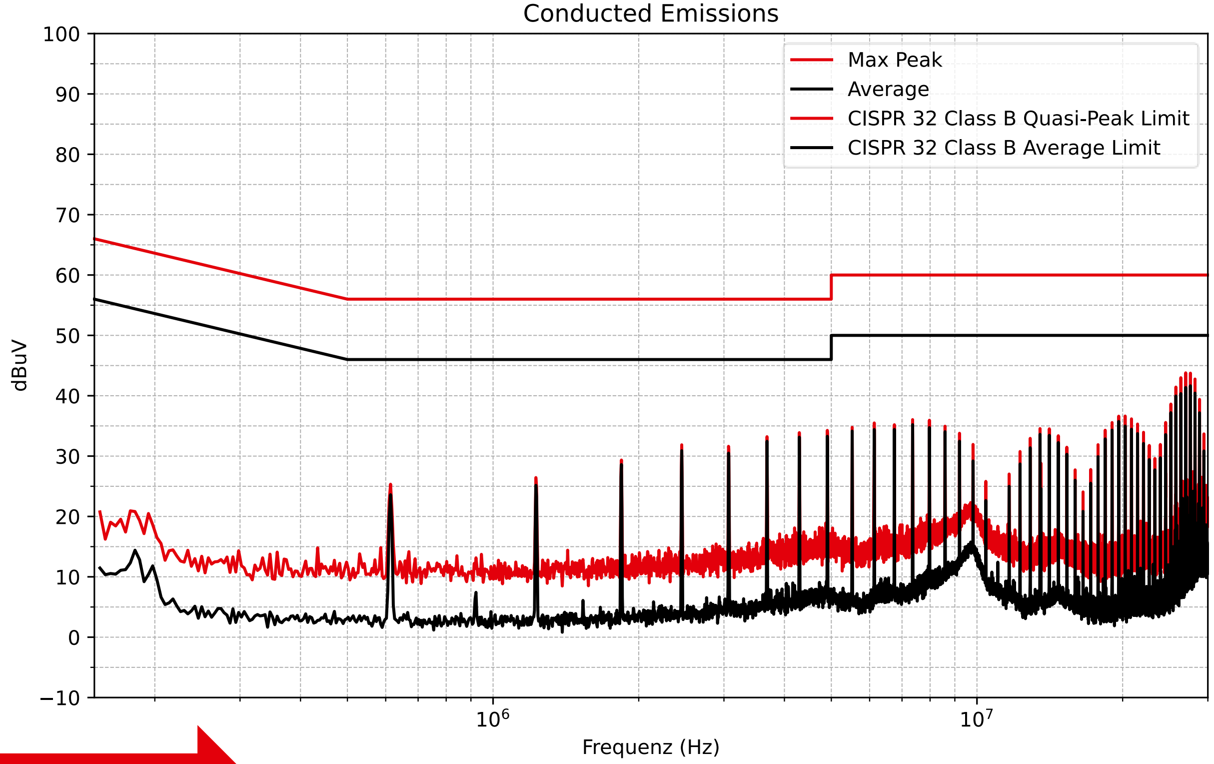
# Realised Designs-Power Modules

2 layers with discrete Y capacitor / with integrated Y capacitor

## 2 layers with 100pF discrete Y capacitor



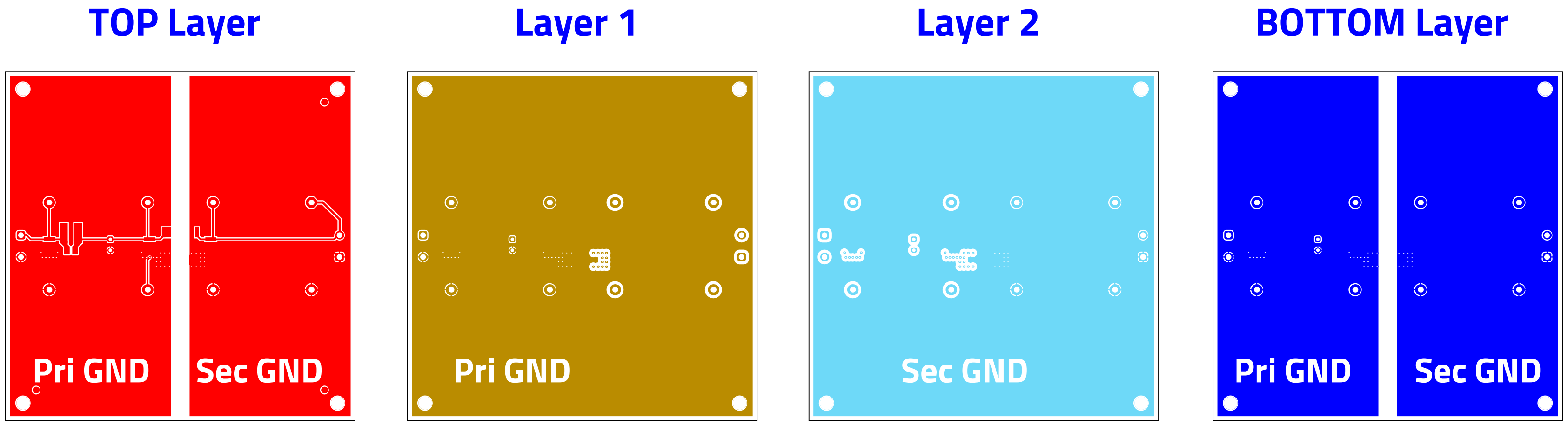
## 2 layers with integrated 130pF Y capacitor



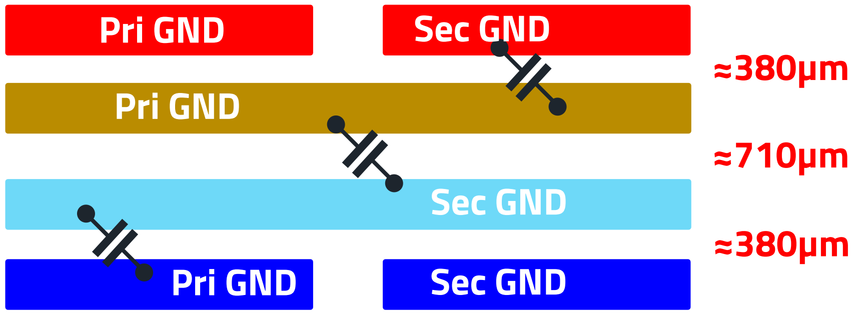
**≈ 0dB**

# Realised Designs-Power Modules

Layout version 3 - 4 layers with 920pF integrated Y capacitor



Schematic structure:



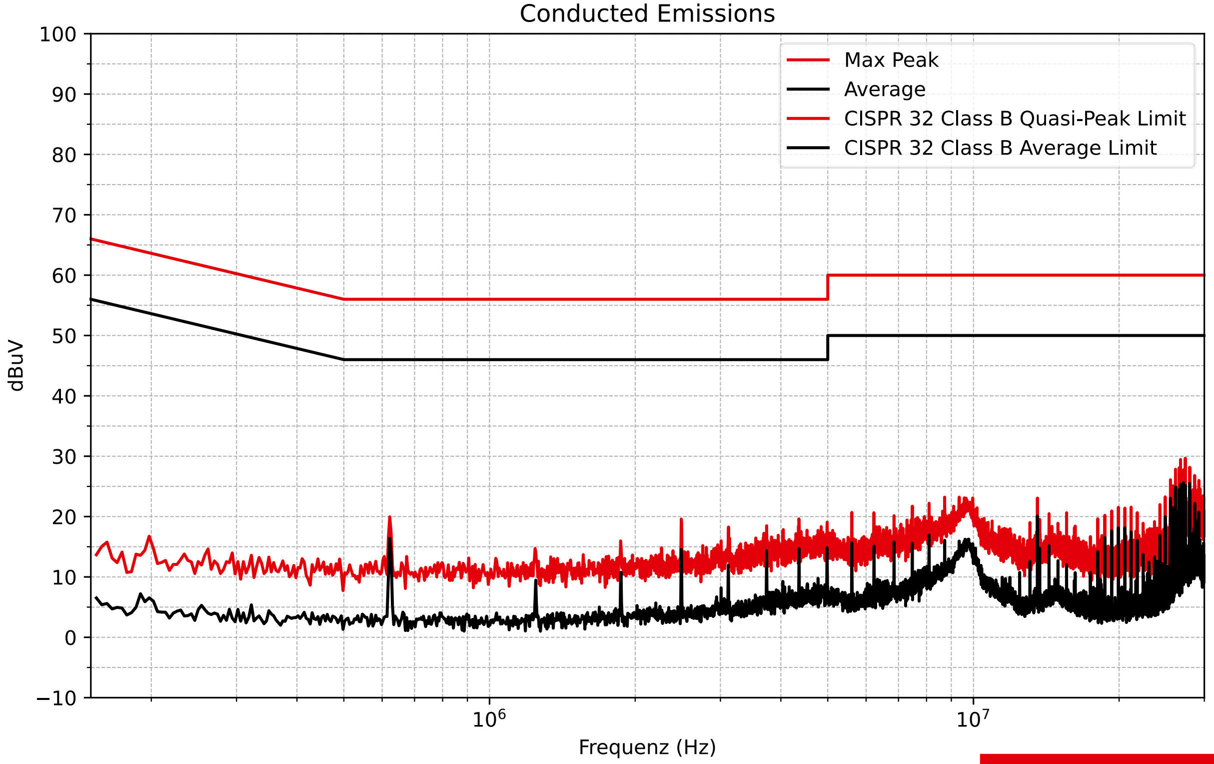
Effective capacity

→ $C_{PCB}$: ca. 920pF = Y-Cap

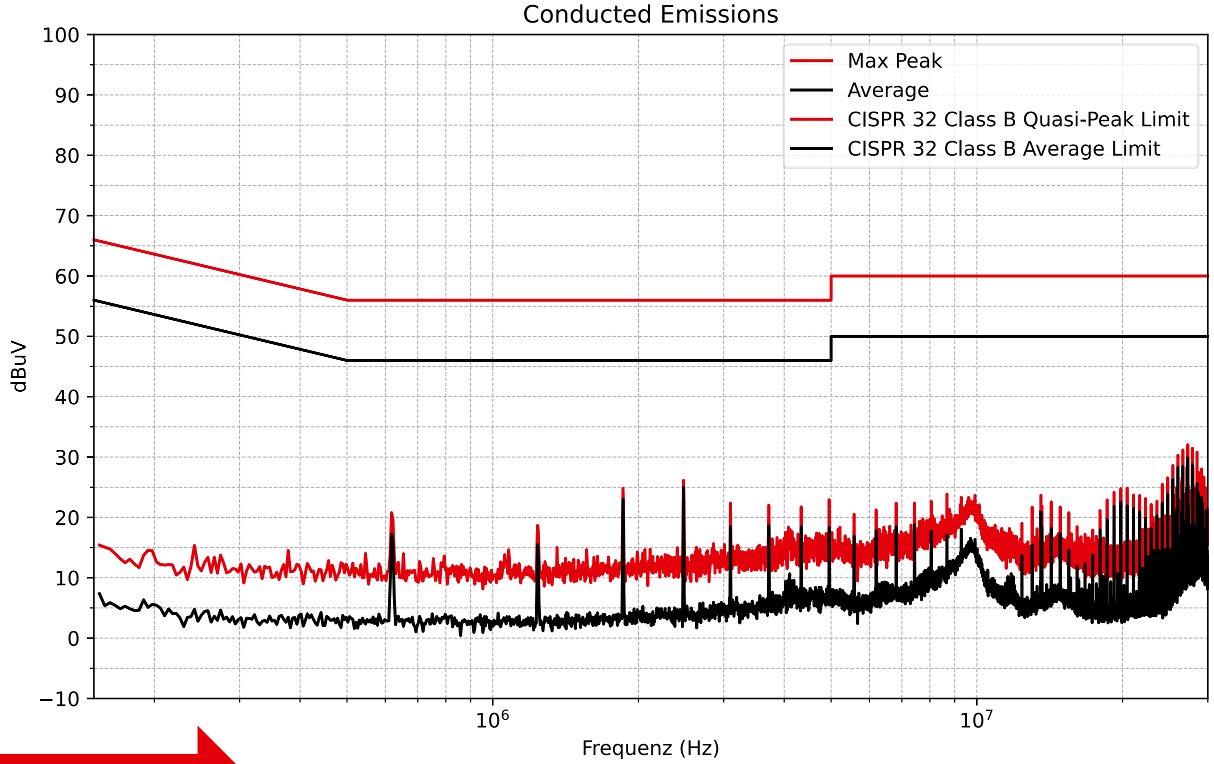
# Realised Designs-Power Modules

4 layers with integrated Y capacitor / 2 layers with discrete Y capacitor

## 4 layers with integrated 920pF Y capacitor



## 2 layers with 1000pF discrete Y capacitor

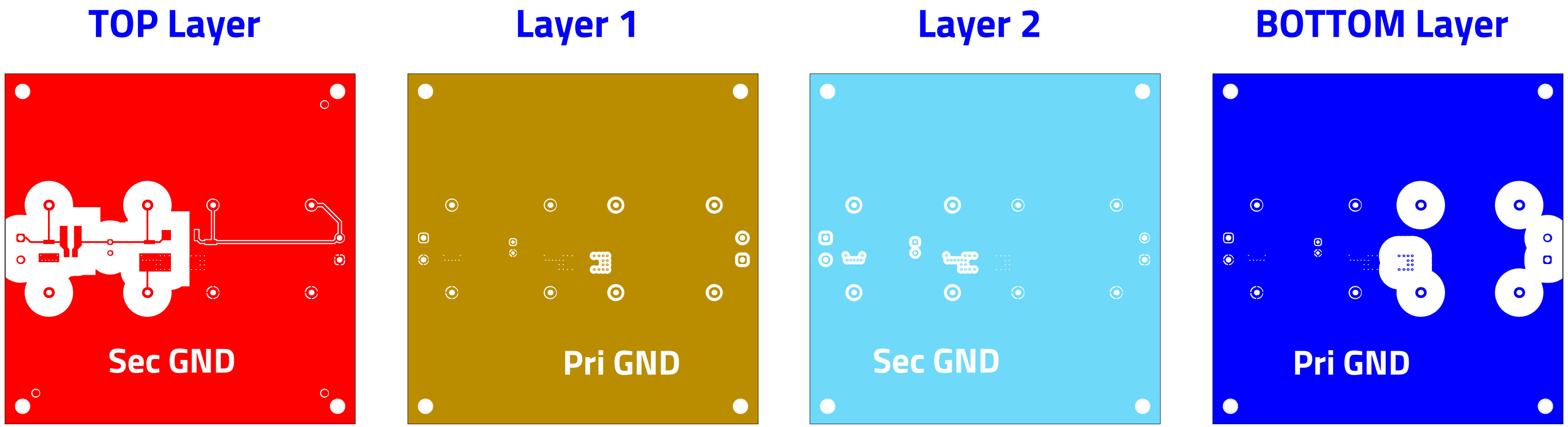


Based on the calculation you get approx. 28dB attenuation with 1000pF Y capacitor

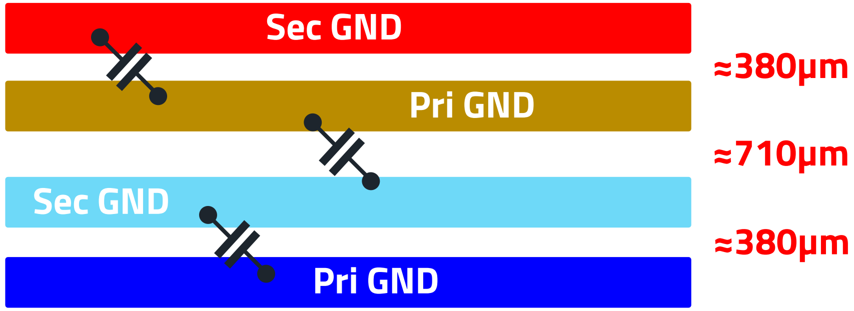
≈ 0dB

# Realised Designs-Power Modules

Layout version 4 - 4 layers with 1400pF integrated Y capacitor



Schematic structure:



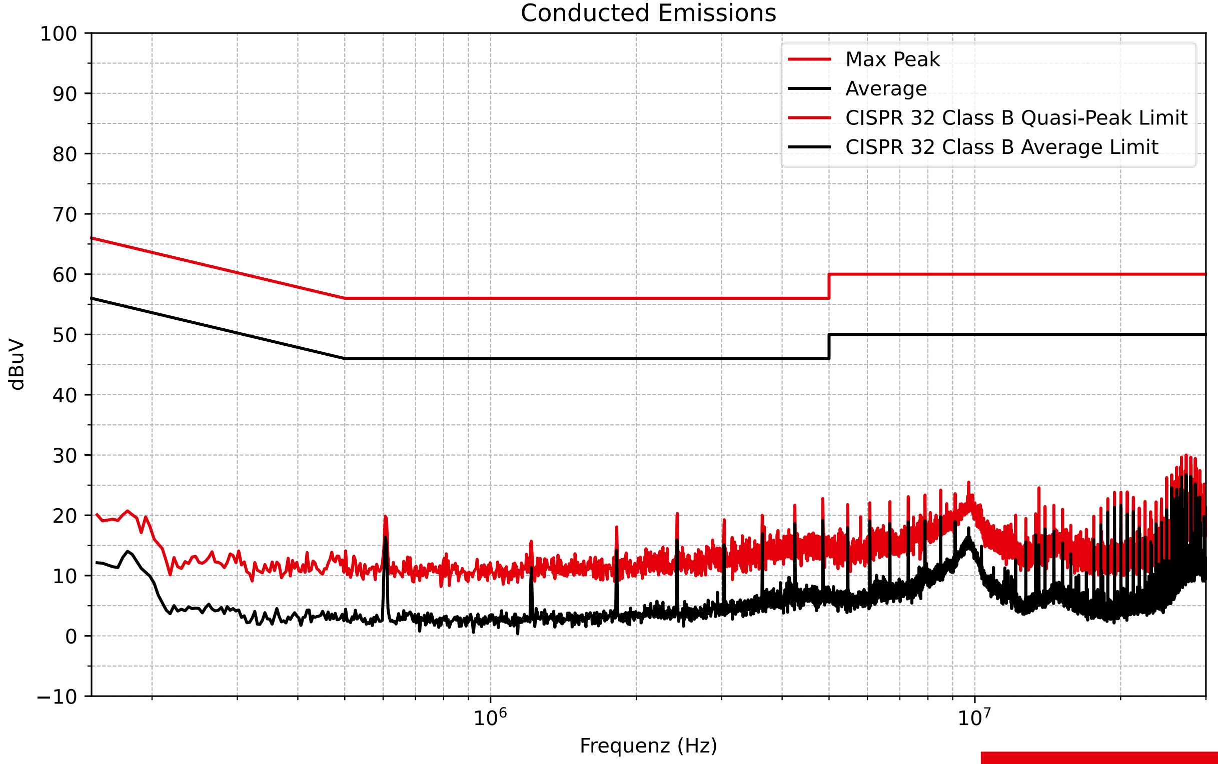
Effective capacity

→ $C_{PCB}$: ca. 1400pF = Y-Cap

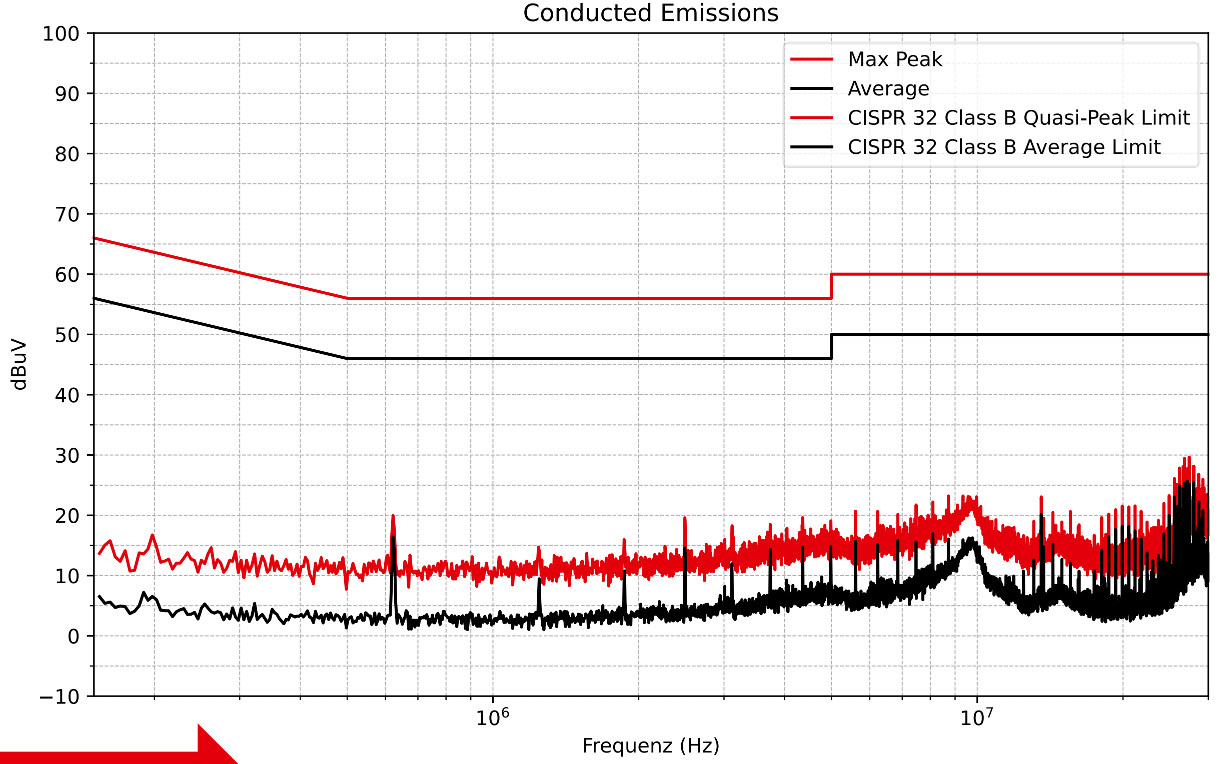
# Realised Designs-Power Modules

## 4 layers with integrated Y capacitor

### 4 layers with integrated 1400pF Y capacitor



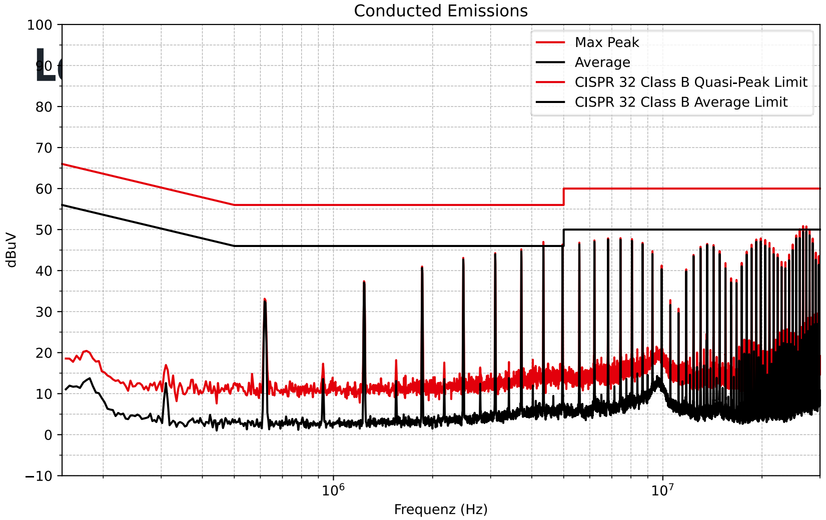
### 4 layers with integrated 920pF Y capacitor



≈ 0dB

# Realised Designs-Power Modules

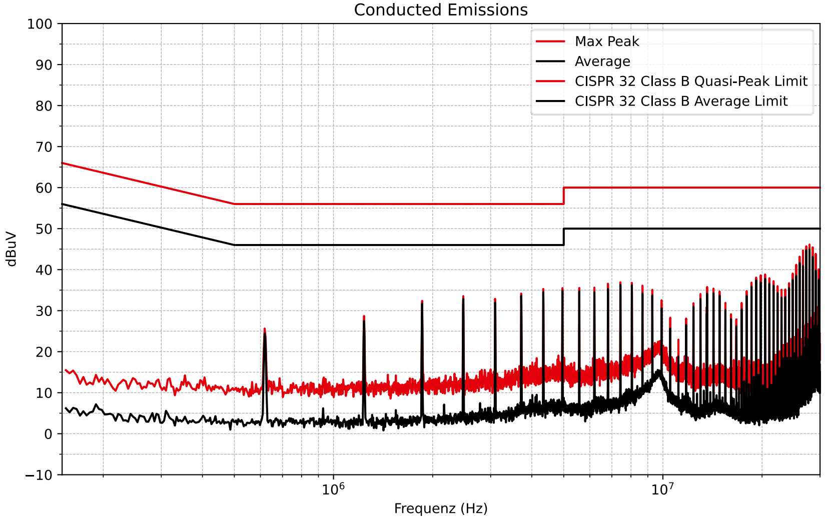
Conducted EMI - 2 layers without Y capacitor → with discrete Y capacitor → Evaluation Board

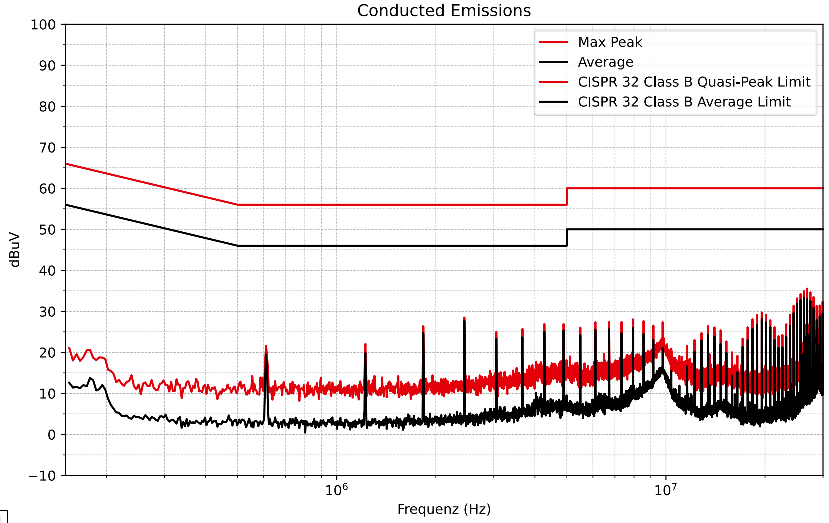


→ $C_Y$ = ca. 14pF

≈ 10dB

→ $C_Y$ = ca. 100pF





→ $C_Y$ = ca. 470pF

≈ 20dB

# Realised Designs-Power Modules

Summary: EMI behaviour stitching Y capacitor

| Version | Description | Capacity | EMI-Judgement |
|---|---|---|---|
| 1 | Two layers without Y capacitor | ≈14 pF | Not enough |
| 2 | Two layers with integrated Y capacitor while maintaining creepage distances equal to the module creepage distances | ≈130 pF | Good |
| 3 | Four layers with separate primary GND area on TOP and BOTTOM layer | ≈920 pF | Better |
| 4 | Four layers with max. capacity. | ≈1400 pF | Better, nearly no difference to 3 |

# Realised Designs-Power Modules

Summary: Discrete or stitching Y capacitor

## Y capacitor: discrete compared to stitching capacitor!

→ Stitching capacitor can always be used.

**Advantages:**

- **The BOM is reduced.**
- **Is always available as an integral part of the layout.**
- **No additional costs.**
- **The insulation distances can be maintained in a more defined manner.**
- **Insulation types such as 'reinforced insulation' can be easily realised.**

**Disadvantages:**

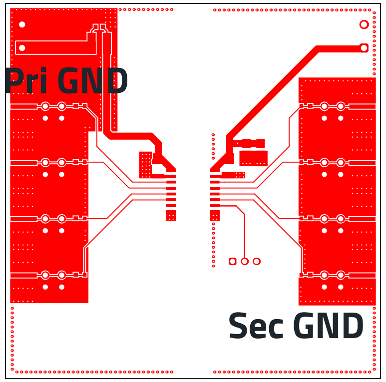
- **Must be considered in the layout right from the start.**
- **Replacement is only possible with a new layout.**
- **More or less easy to realise depending on the layout.**
- **PCB and not only in the BOM.**

# REALISED DESIGNS DIGITAL ISOLATOR

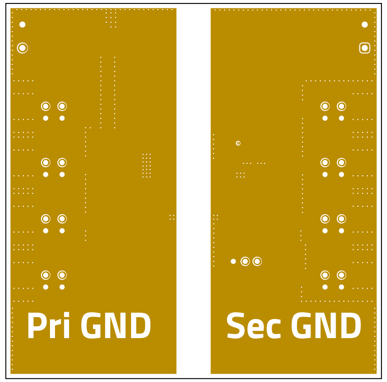
# Realised Designs-Digital Isolators

Layout version 1 - 4 layers with 600pF integrated Y capacitor

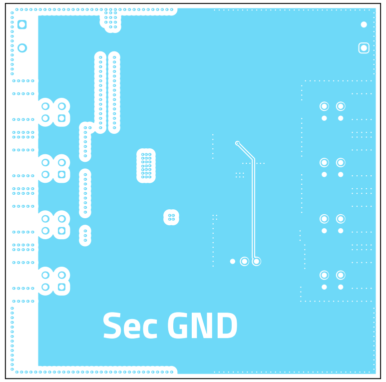
**TOP Layer**



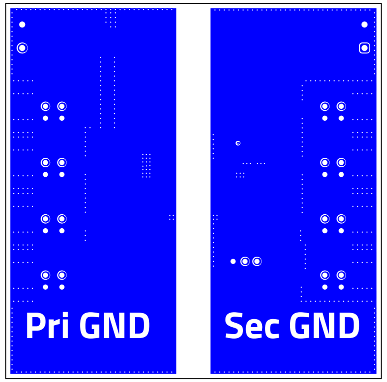
**Layer 1**



**Layer 2**



**BOTTOM Layer**



Schematic structure:

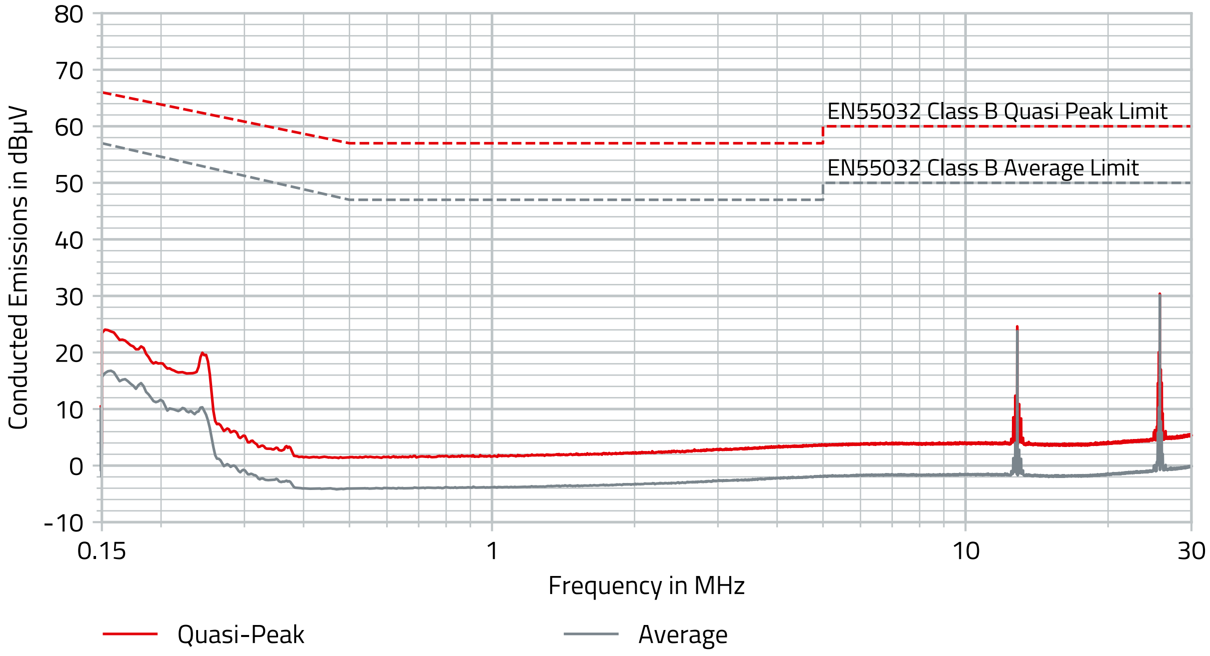
Effective capacity

→ $C_{PCB}$: ca. 600pF = Y-Cap

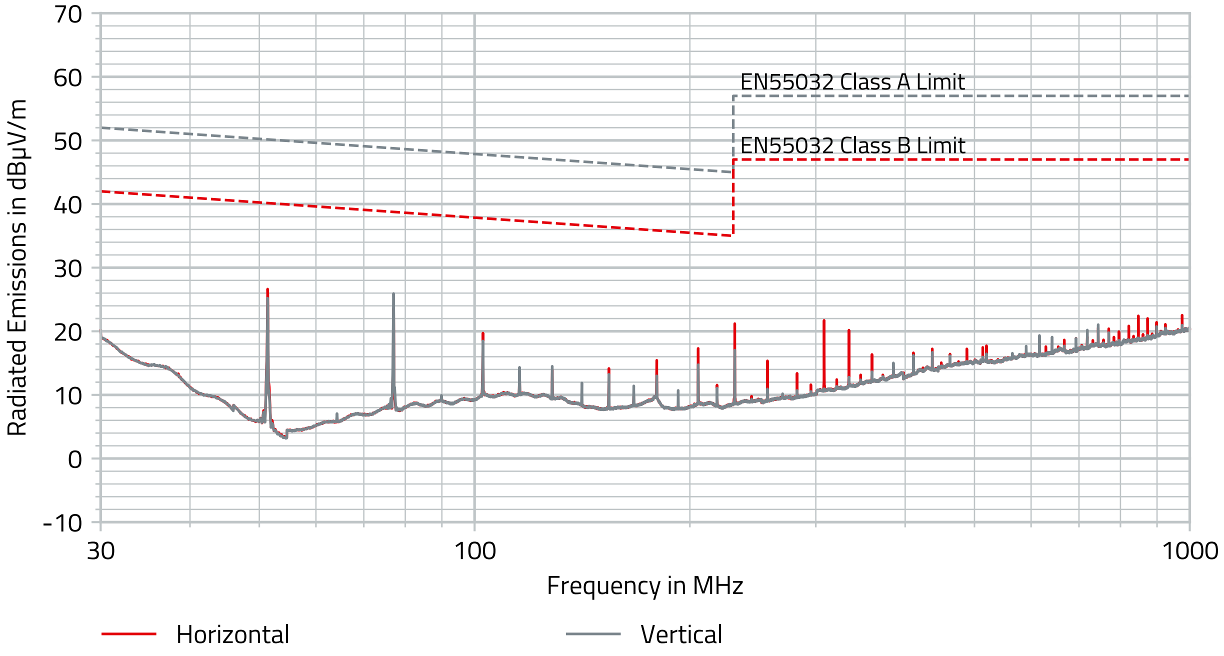
# Realised Designs-Digital Isolators

4 layers with 600pF integrated Y capacitor

## Conducted emissions

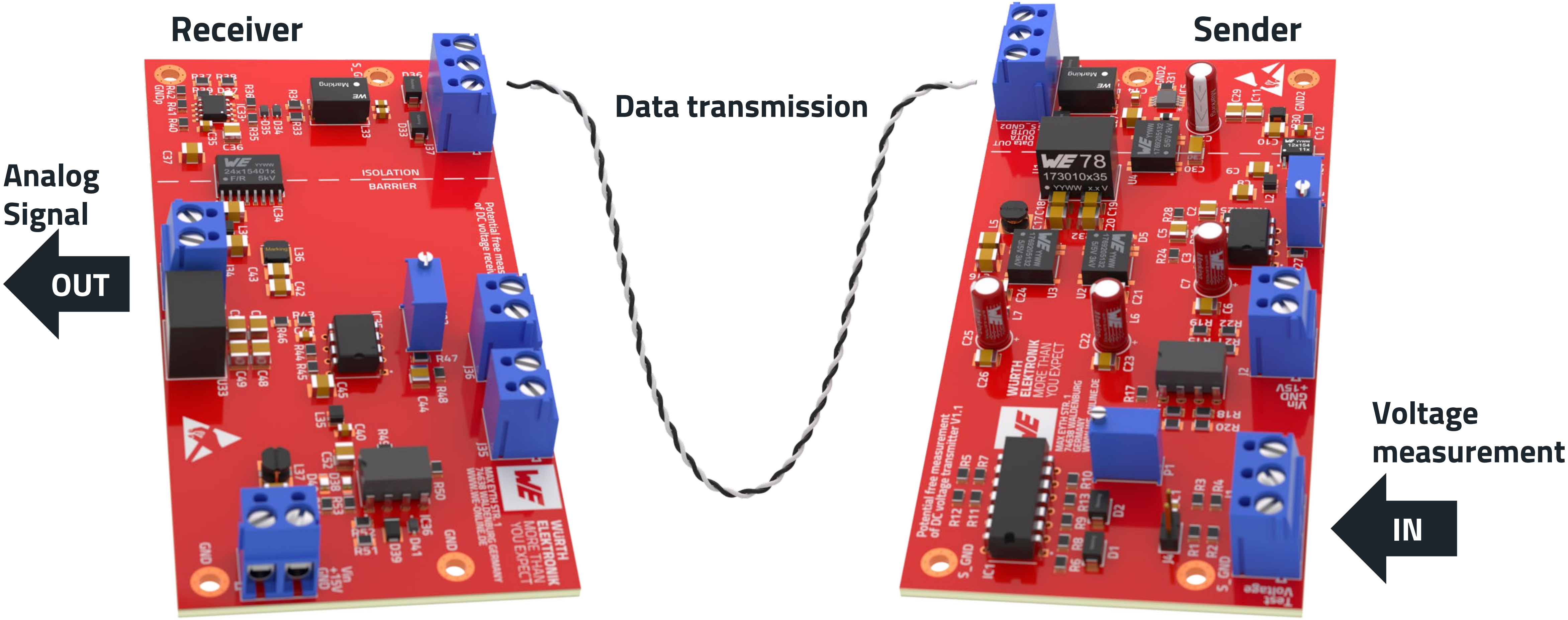


## Radiated emissions



# Realised Designs-Digital Isolators

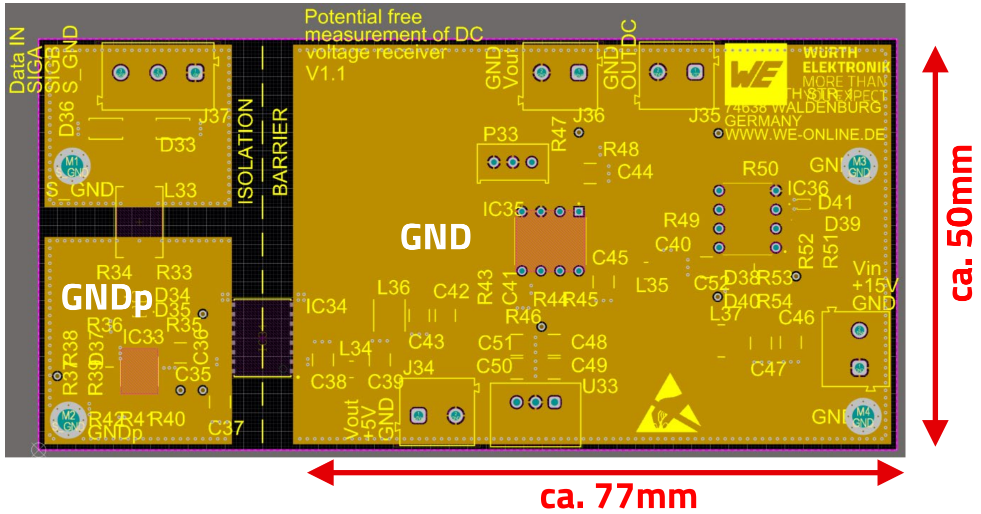
Potential-free voltage measurement - transmitter and receiver circuit

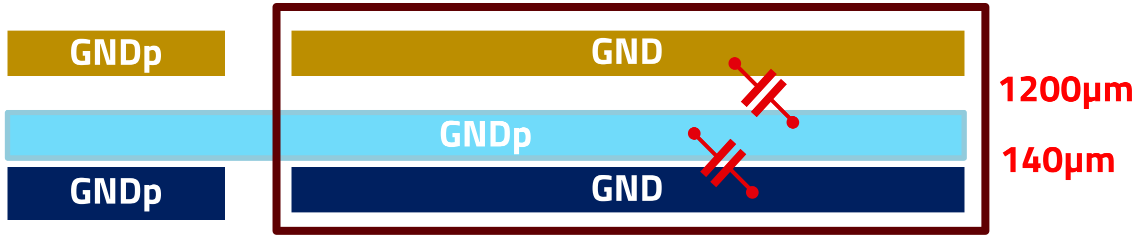


# Realised Designs-Digital Isolators

Layout version 2 - 4 layers with approx. 1000pF integrated Y capacitor - Receiver

**Internal 1 Layer**

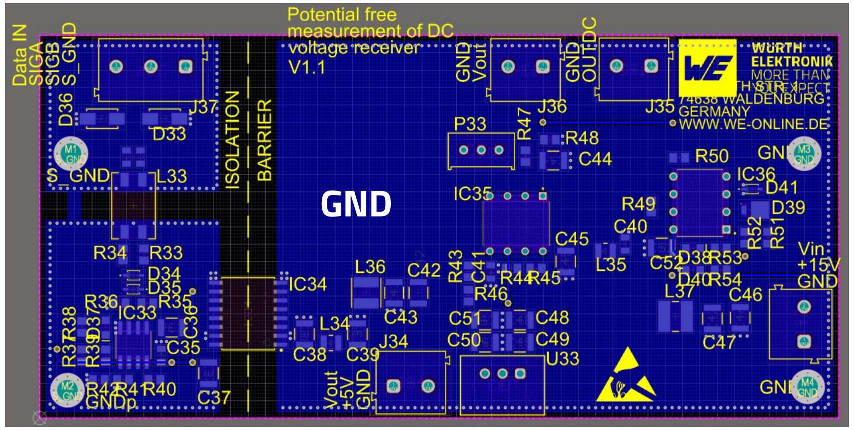




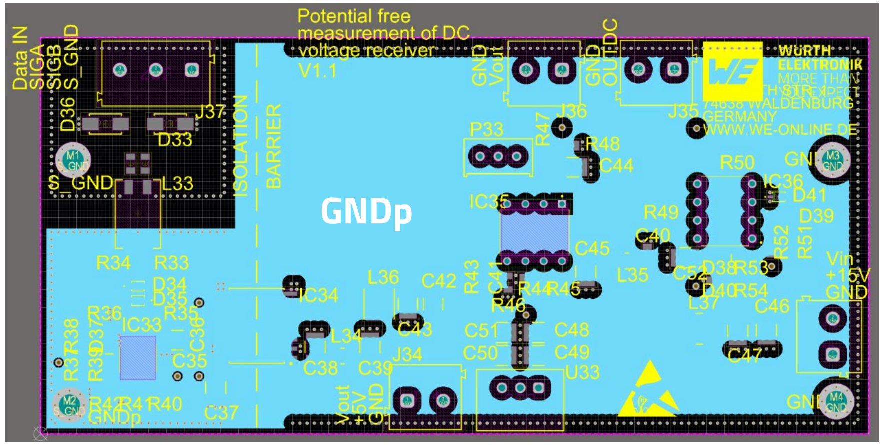
Effective capacity:

→ $C_{PCB}$: ca. 1nF = Y-Cap

**BOTTOM Layer**



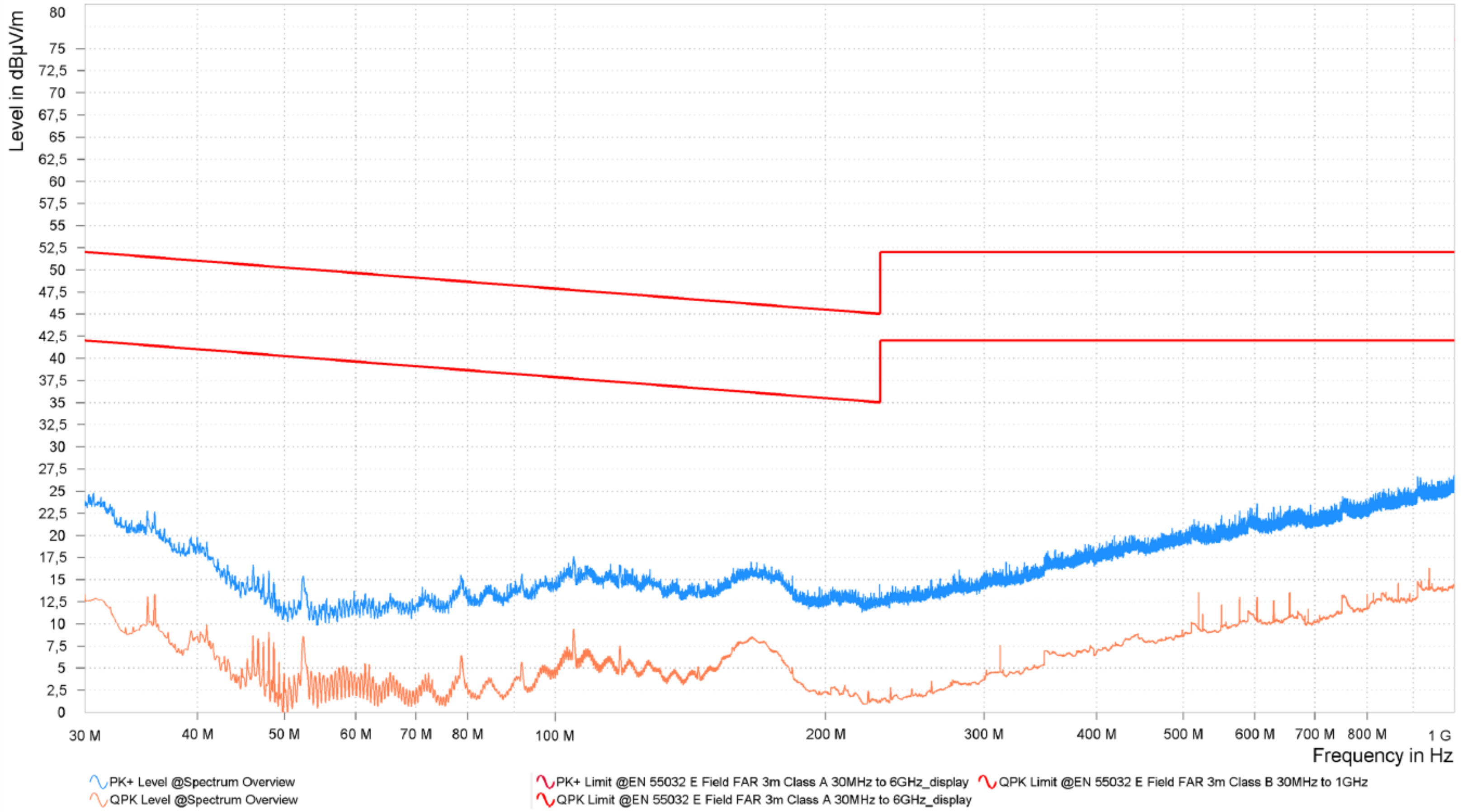
**Internal 2 Layer**



# Realised Designs-Digital Isolators

## Results EMC measurement (radiated) 4-layer with PCB coupling capacitance as Y-capacitance

### Receiver



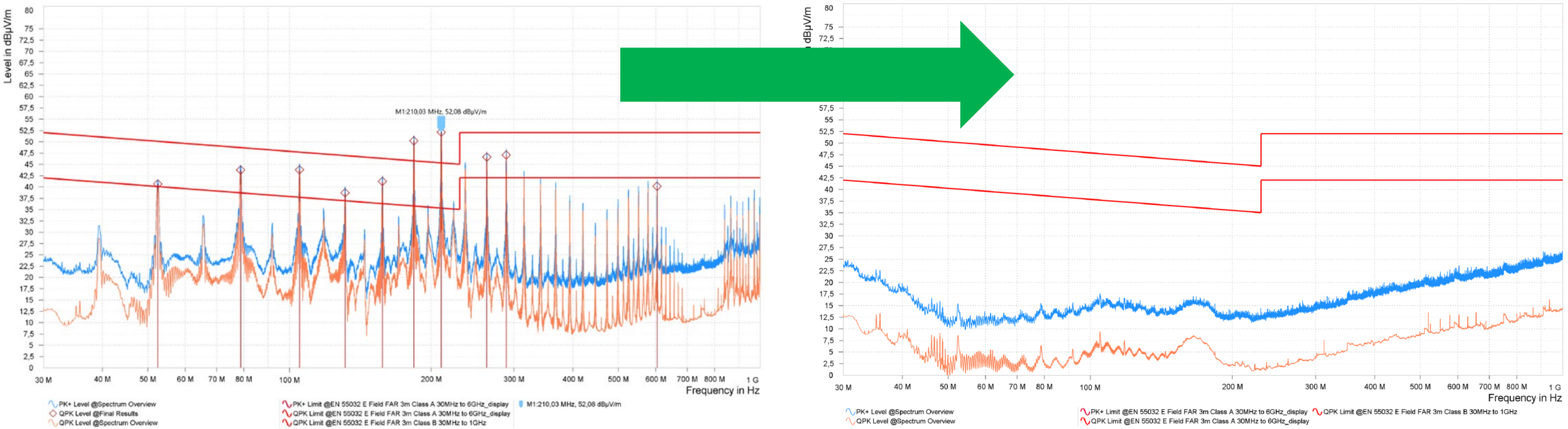
- 4-Layer PCB
- Y-Cap approx. 1nF by superimposing the layers

# Realised Designs-Digital Isolators

Results EMC measurement 4-layer with PCB coupling capacitance as Y-capacitance

**Receiver**

**Receiver**



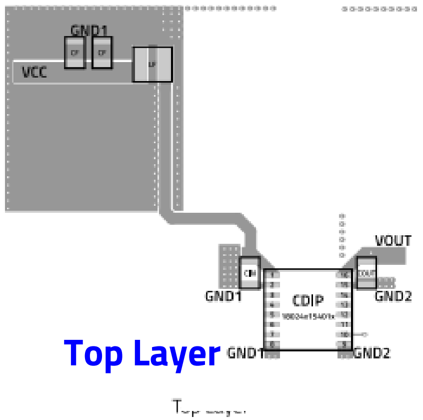
- Battery powered
- Transmitter outside the chamber
- 2-layer PCB

- 4-layer PCB Y-Cap approx.
- 1nF by superimposing the layers

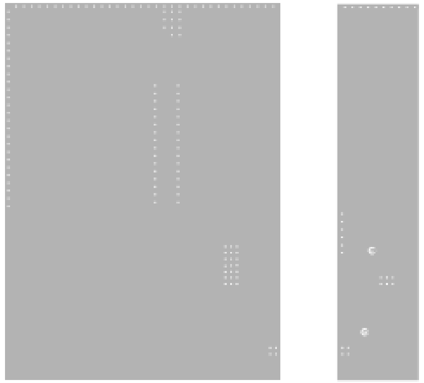
# DESIGN-IN SUPPORT

# Service & Support

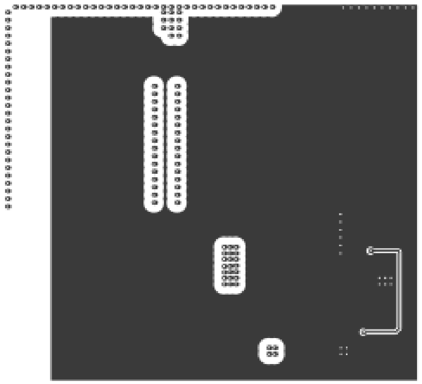
## Design Example - Layout recommendation from the data sheet



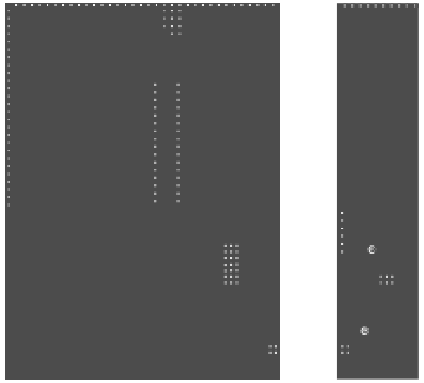
**Top Layer**



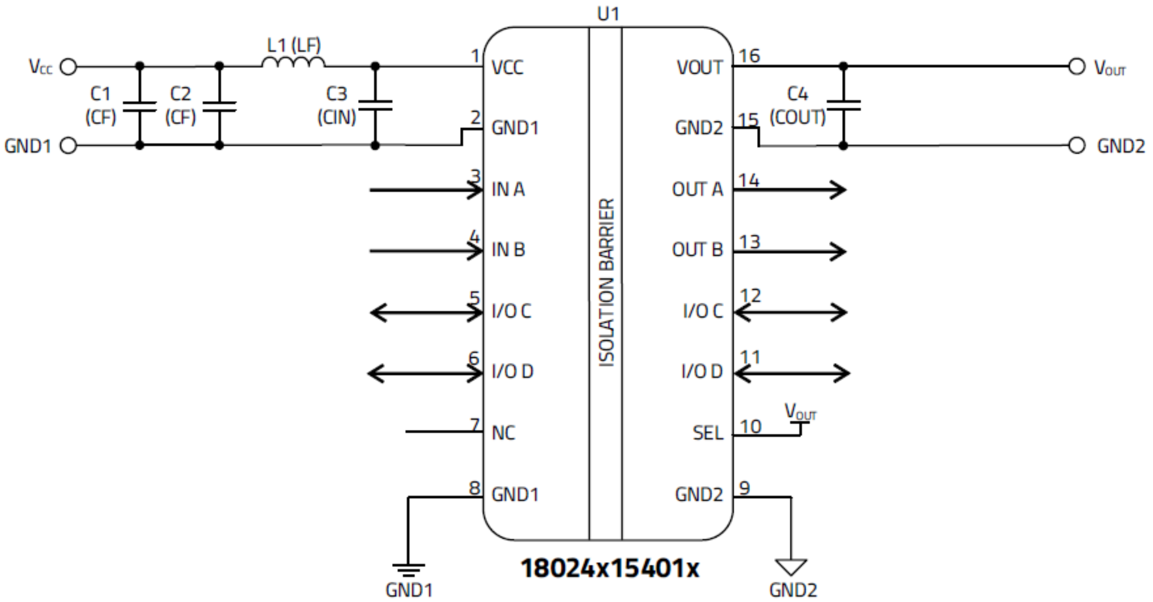
**Second Layer**



**Third Layer**



**Bottom Layer**



| DESIGNATOR | DESCRIPTION | FUNCTION |
|---|---|---|
| U1 | Digital Isolator | Digital Isolator |
| L1 | Filter inductor, 4.7µH, PD2 family, $I_{SAT}$ = 2.46A, $I_R$ = 1.82A | Input Filter |
| C1, C2, C3, C4 | Ceramic chip capacitor 10µF/15V X7R, 1210 | Input and Output Filter |

# Service & Support

## Contacts Support Hotline


Roland Kratz


Martin Sittner


Alexander Zeller

## Contacts BDM


Steffen.Wolf@we-online.de


Dimitri.Kozlov@we-online.de


Kaveri.Onkar@we-online.de


Arndt.Schmidt@we-online.de

## Services

powermodules@we-online.de

Design-In Support

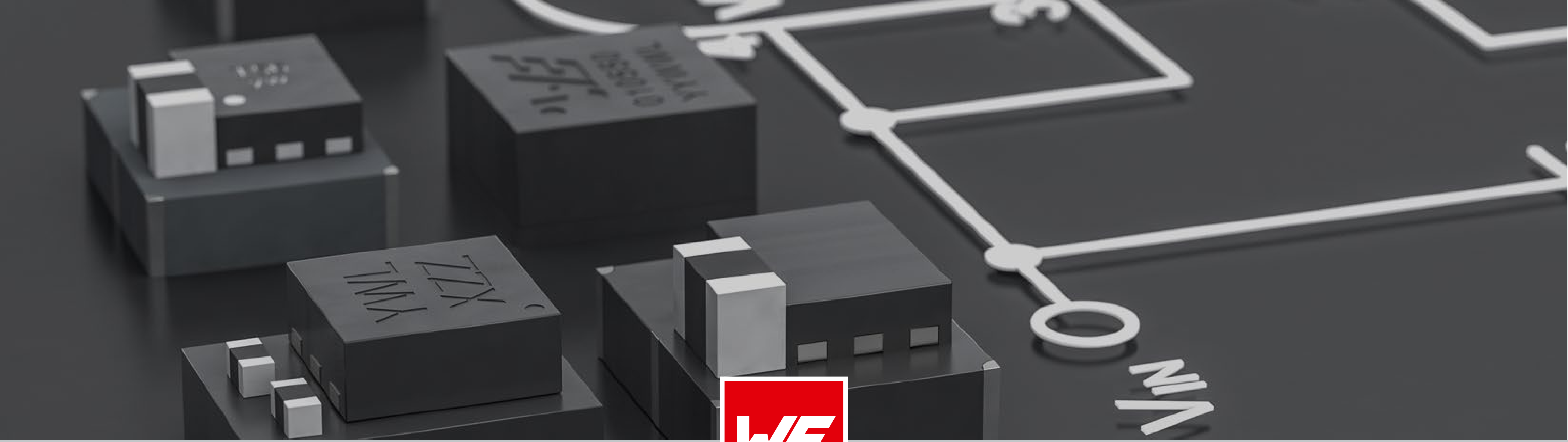
EMC Filter Design Support

Layout Review Support

Thermal Design Support

## Services

- **ADM trainings**
- **ADM basic technical support**
- **ADM pricing and lead time support**
- **Customer trainings/seminars**
- **Visit focus customers**
- **Business tracking / reports**
- **Sales app (define and provide content)**
- **Sales tools (Product Overview, Show Boards)**



Thank you for your attention!

# DECREASING THE BOM AND IMPROVING COMMON MODE NOISE REDUCTION

Timur Uludag

**WÜRTH ELEKTRONIK** MORE THAN YOU EXPECT