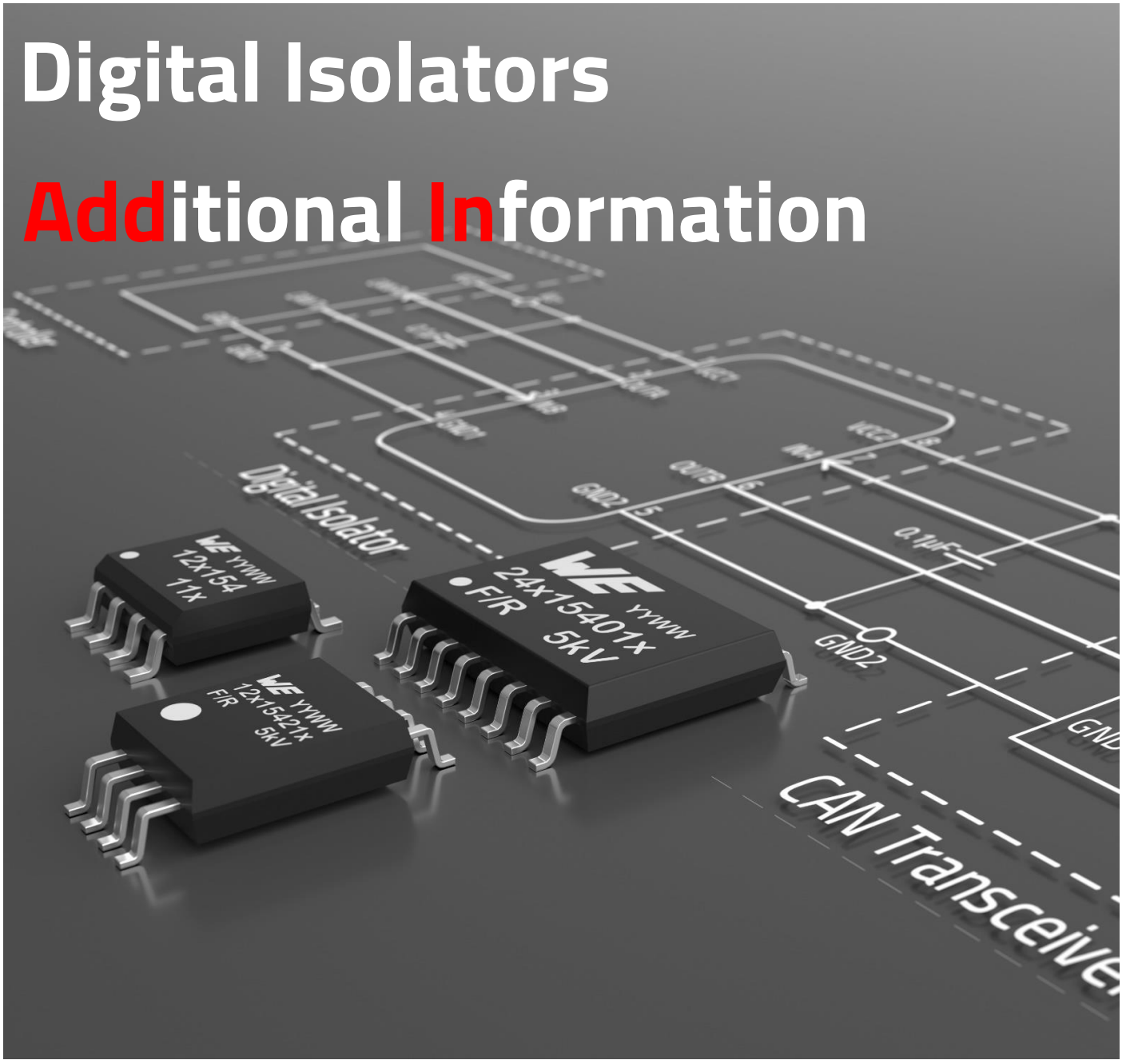
Digital Isolators

Additional Information



Digital Isolators are the reliable solution for galvanic isolation of digital signals. They provide a reliable transmission of high-speed signals, prevent ground potential differences and the appearance of data communication errors or data corruption, and improve noise immunity.

For more information, please visit:
www.we-online.com/digitalisolators

- Simple design-in process
- Design and layout support
- EMI filter design for EN55032 class B
- Evaluation boards for isolators with integrated DC/DC converters
- REDEXPERT for selection

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1. TYPICAL CIRCUIT DIAGRAMS AND STRUCTURES

Table 1: 2-Channel Digital Isolators without Integrated DC/DC Converters (CDIS)

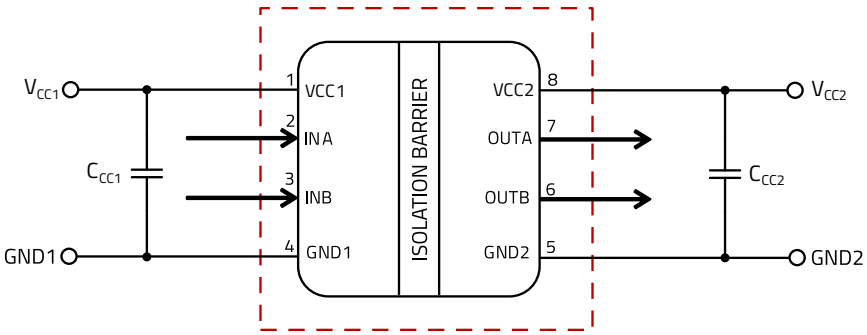
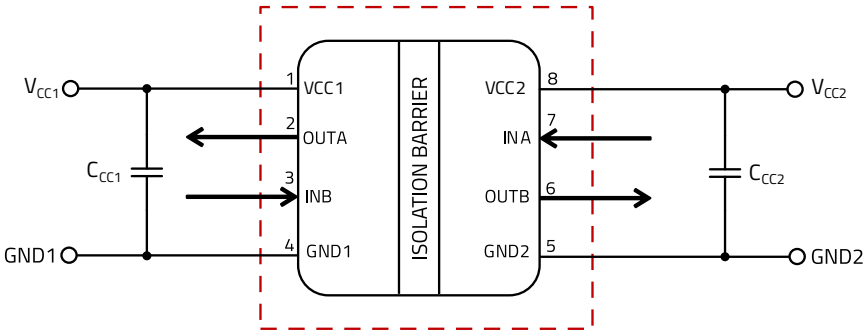
Order Code	Channel Config.	Package	Typical Circuit Diagram
18012015411H	2/0	SOIC-8NB	
18012015411L			
18012015421H		SOIC-8WB	
18012015421L			
18012115411H	1/1	SOIC-8NB	
18012115411L			
18012115421H		SOIC-8WB	
18012115421L			

Table 2: 4-Channel Digital Isolators without Integrated DC/DC Converters (CDIS)

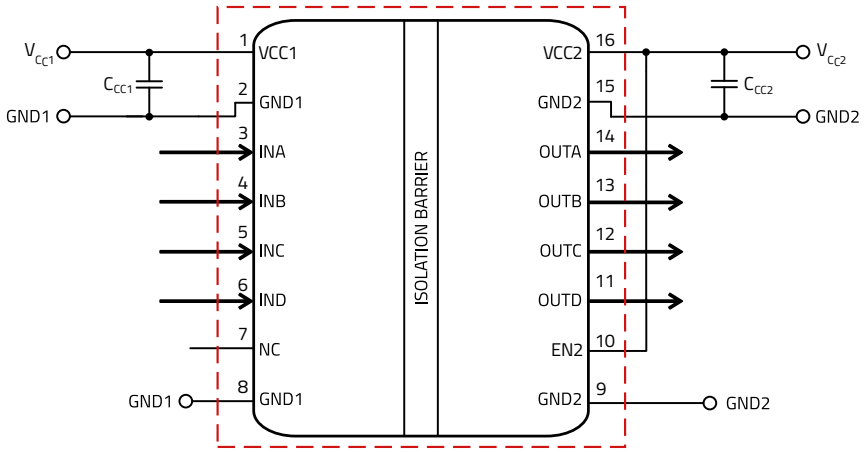
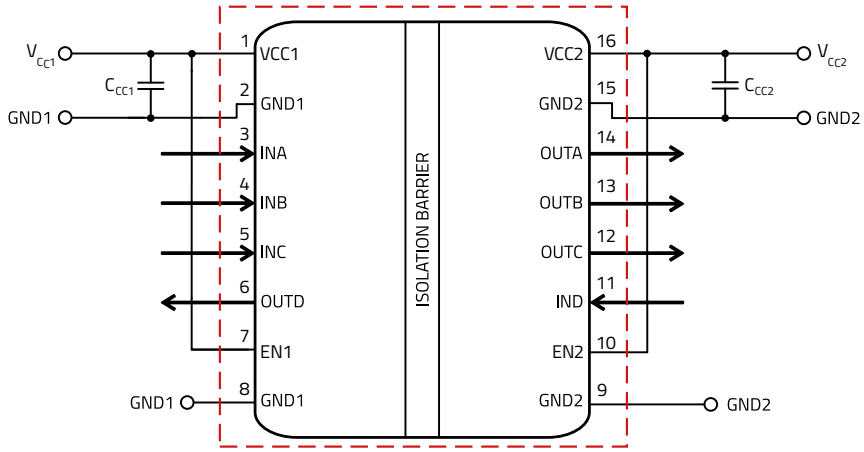
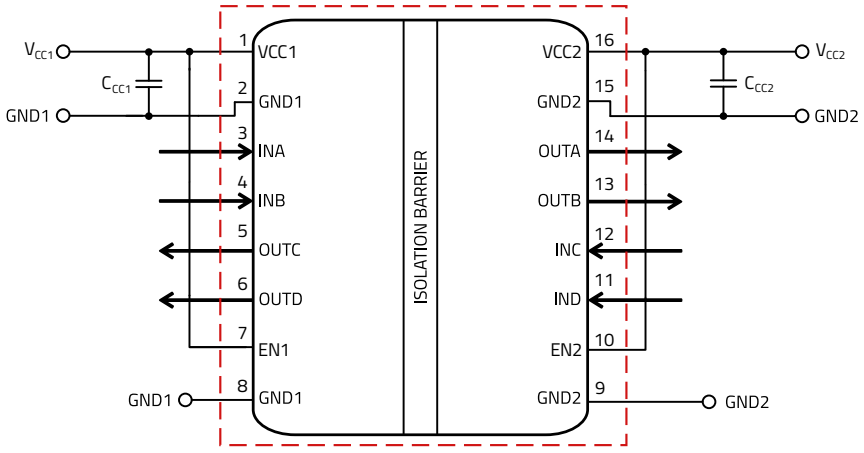
Order Code	Channel Config.	Package	Typical Circuit Diagram
18014015401H	4/0	SOIC-16WB	
18014015401L			
18014115401H	3/1		
18014115401L			
18014215401H	2/2		
18014215401L			

Table 3: 6-Channel Digital Isolators without Integrated DC/DC Converters (CDIS)

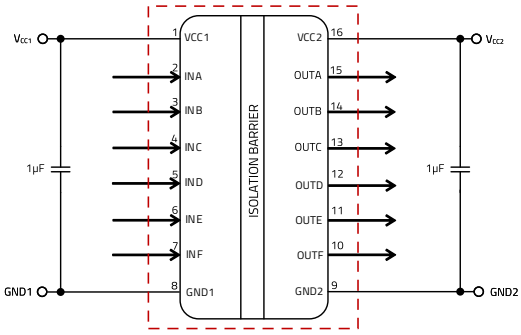
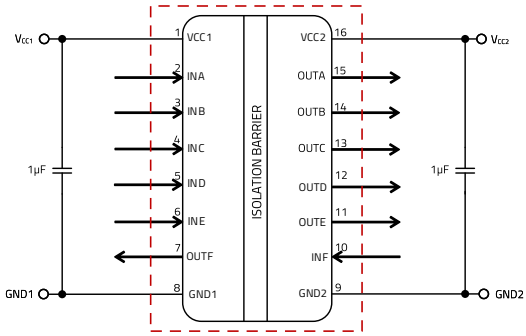
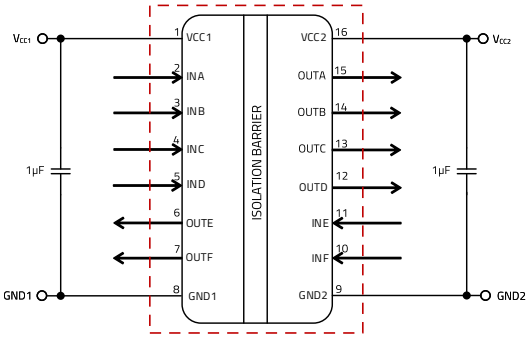
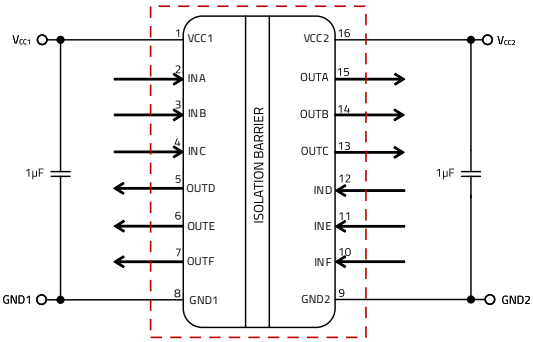
Order Code	Channel Config.	Package	Typical Circuit Diagram
18016004401H	6/0	SOIC-16WB	
18016004401L			
18016104401H	5/1		
18016104401L			
18016204401H	4/2		
18016204401L			
18016304401H	3/3		
18016304401L			

Table 4: 4-Channel Digital Isolators with Integrated DC/DC Converters (CDIP)

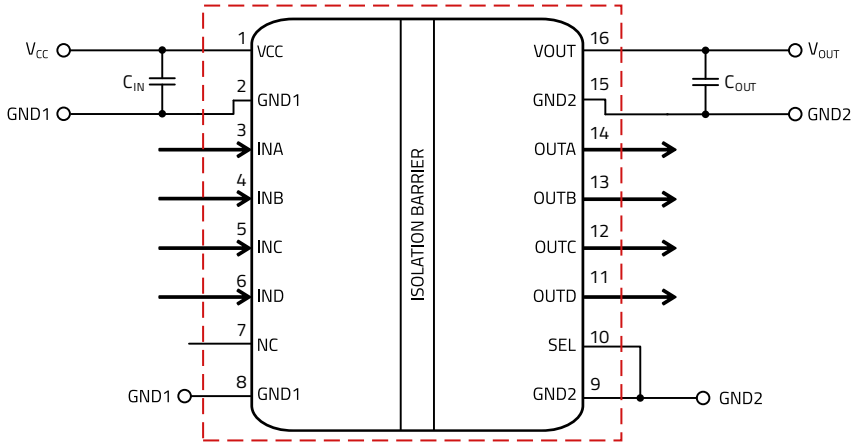
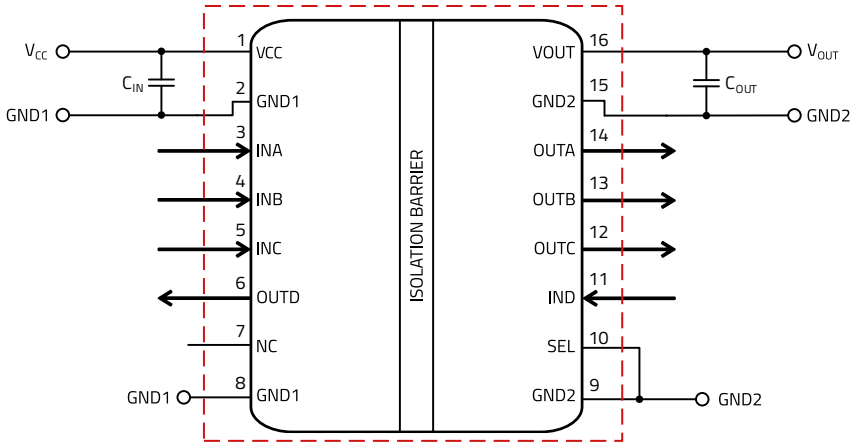
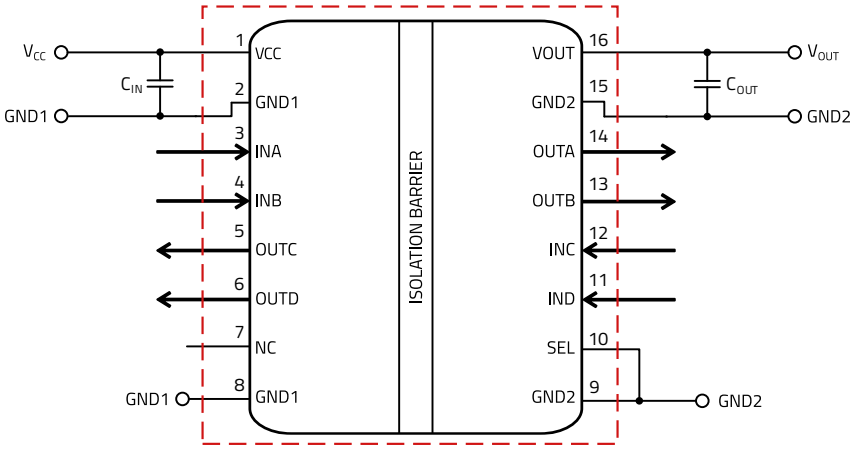
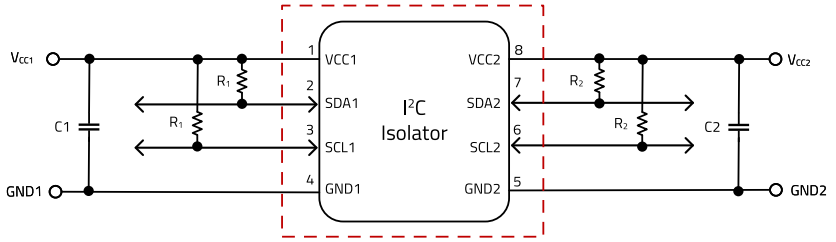
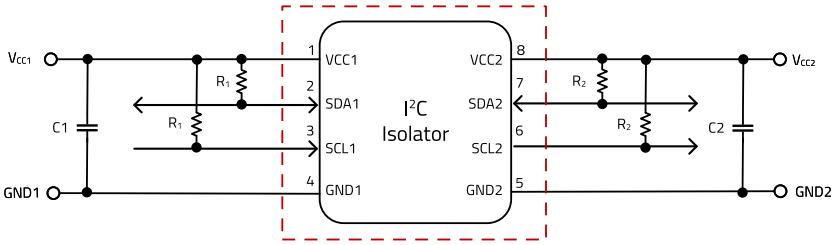
Order Code	Channel Config.	Package	Typical Circuit Diagram
18024015401H 18024015401L	4/0	SOIC-16WB	
18024115401H 18024115401L	3/1		
18024215401H 18024215401L	2/2		

Table 5: 2-Channel Bidirectional I²C Isolators (**CDI2C**)

Order Code	Channel Config.	Package	Typical Circuit Diagram
18032011	2/0	SOIC-8NB	
18032111	1/1		

2. FEATURES

Table 6: Features

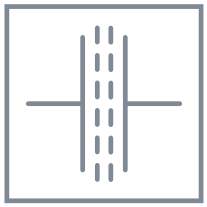
	**Isolation Voltage 3750 V** The digital isolators in the SOIC-8NB package are certified under UL 1577. ❖ Maximum Isolation Voltage V_{ISO}=3750 V_{RMS} for 1 minute ❖ UL File No: E535458
	**Basic Insulation** The digital isolators in SOIC-8NB are certified according to DIN EN IEC 60747-17 (VDE 0884-17). ❖ Maximum repetitive peak isolation voltage V_{IORM}=566 V_{PK} ❖ Maximum working isolation voltage V_{IOWM}=400 V_{RMS} / 566 V_{DC} ❖ Maximum transient isolation voltage V_{IOTM}=5300 V_{PK} ❖ Maximum surge isolation voltage V_{IOSM}=5000 V_{PK} ❖ VDE certification number: 40058073
	**Isolation Voltage 5000 V** The digital isolators in SOIC-8WB and SOIC-16WB are certified under UL 1577. ❖ Maximum Isolation Voltage V_{ISO}=5000 V_{RMS} for 1 minute ❖ UL File No: E535458
	**Reinforced Insulation** The isolators in SOIC-8WB/-16WB are certified according to DIN EN IEC 60747-17 (VDE 0884-17). ❖ Maximum repetitive peak isolation voltage V_{IORM}=1414 V_{PK} ❖ Maximum working isolation voltage V_{IOWM}=1000 V_{RMS} / 1414 V_{DC} ❖ Maximum transient isolation voltage V_{IOTM}=7070 V_{PK} ❖ Maximum surge isolation voltage V_{IOSM}=7070 V_{PK} ❖ VDE certification number: 40058069
	**Data Rate 100 Mbps** Data Rate up to 100 Mbps for 4-channel digital isolators with integrated DC/DC converters ❖ Possibility to transfer digital signals with high-speed data rate up to 100 Mbps
	**Data Rate 150 Mbps** Data Rate up to 150 Mbps for 2- and 4-channel digital isolators without integrated DC/DC converters ❖ Possibility to transfer digital signals with high-speed data rate up to 150 Mbps

Table 7: Features

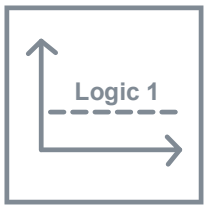
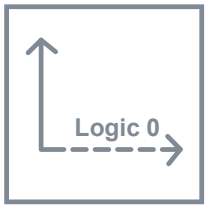
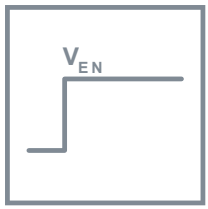
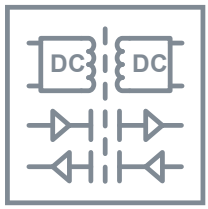
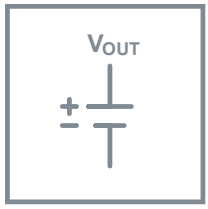
	**Common Mode Transient Immunity (CMTI)** High common mode transient immunity ±150 kV/µs (typical). ❖ Indicates the isolator's ability to maintain reliable operation during rapid common-mode voltage changes ❖ Prevents fast transient noise from coupling through the isolation barrier and affecting signal integrity
	**Default Output High** The predefined state of the default output is **high** when the input channels of the digital isolator are unpowered or the input pins are floating. ❖ The internal high-frequency signal modulator of a digital isolator with a **high** default output state does not operate when the input signal is at a **high** level
	**Default Output Low** The predefined state of the default output is **low** when the input channels of the digital isolator are unpowered or the input pins are floating. ❖ The internal high-frequency signal modulator of a digital isolator with a **low** default output state does not operate when the input signal is at a **low** level
	**Enable** Applicable to 4-channel digital isolators without integrated DC/DC converters. ❖ The output pins on the primary side of the digital isolator are enabled when EN1 is high or open and are in a high-impedance state when EN1 is low. ❖ The output pins on the secondary side of the digital isolator are enabled when EN2 is high or open and are in a high-impedance state when EN2 is low.
	**Integrated Isolated DC/DC converter** The integrated DC/DC converters of the 4-channel digital isolators support up to 650 mW of power.
	**Output Voltage Selection** Allows selection of the output voltage level of the integrated DC/DC converter 3.3 V or 5 V.
	**Fixed Soft Start** The slope of the rise of the output voltage of the integrated DC/DC converter during start-up is fixed. ❖ No overshoot

Table 8: Features

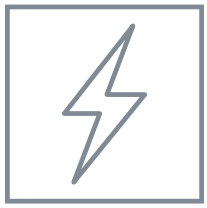
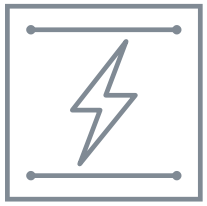
	**Overcurrent Protection** During an overcurrent condition of the integrated DC/DC converter, the output current is limited. ❖ Limits overheating of the device
	**Short-Circuit Protection** The output voltage is continuously monitored and when it drops below a certain threshold, the PFM controller of the integrated DC/DC converter stops switching. ❖ Limits overheating of the device
	**Undervoltage Lockout** The gating pulses for the secondary and primary side full bridges of the integrated DC/DC converter are inhibited in the event of an input voltage below the recommended values. ❖ Avoids undefined behavior of the integrated DC/DC converter during input voltage failures
	**Over Temperature Protection** Turns off the integrated DC/DC converter when the junction temperature exceeds a dangerous limit. ❖ Prevents catastrophic failures during accidental device overheating
	**Low Radiation** The digital isolators with integrated DC/DC converter are compliant with the European standard: EN 55032 class B (CISPR 32) conducted and radiated. ❖ Time-saving design (with the reference layout specified in the data sheet)

Table 9: Features of 2-, 4- and 6-Channel Digital Isolators without Integrated DC/DC Converters (CDIS)

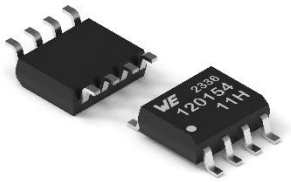
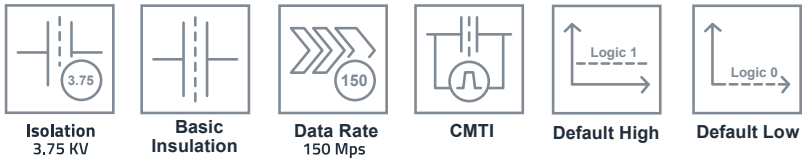
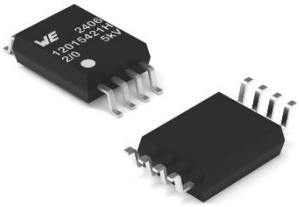
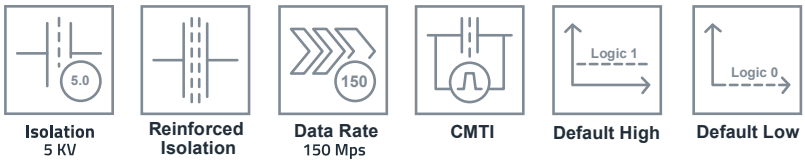
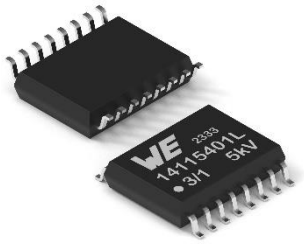
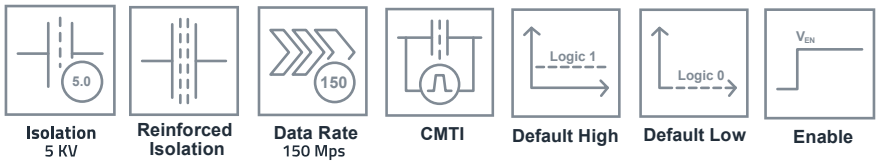
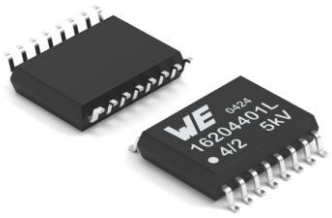
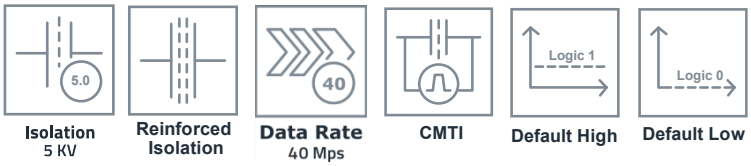
2-Channel Unpowered in SOIC-8NB	
	
2-Channel Unpowered in SOIC-8WB	
	
4-Channel Unpowered in SOIC-16WB	
	
6-Channel Unpowered in SOIC-16WB	
	

Table 10: Features of 4-Channel Digital Isolators with Integrated DC/DC Converters (CDIP)

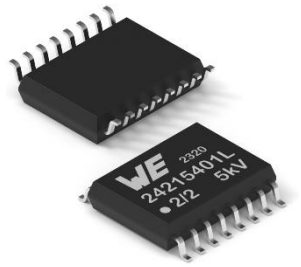
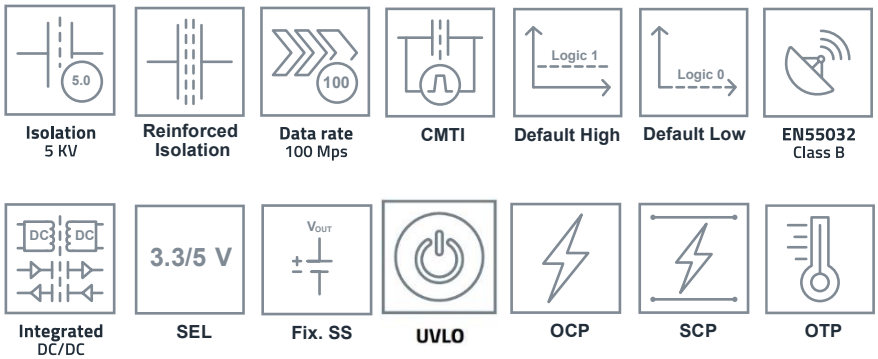
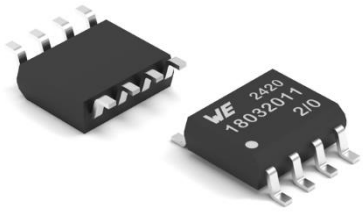
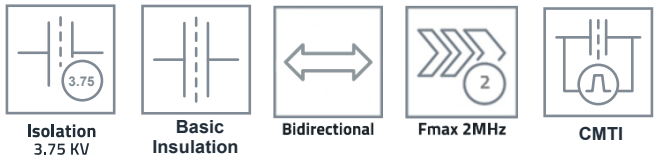
4-Channel Powered in SOIC-16WB	
	

Table 11: Features of 2-Channel Bidirectional I²C Isolators (CDI2C)

2-Channel Bidirectional in SOIC-8NB	
	

3. APPLICATIONS

Table 12: Isolation of **CAN Interface** (2-Channel Unpowered Digital Isolators 180121154x1x)

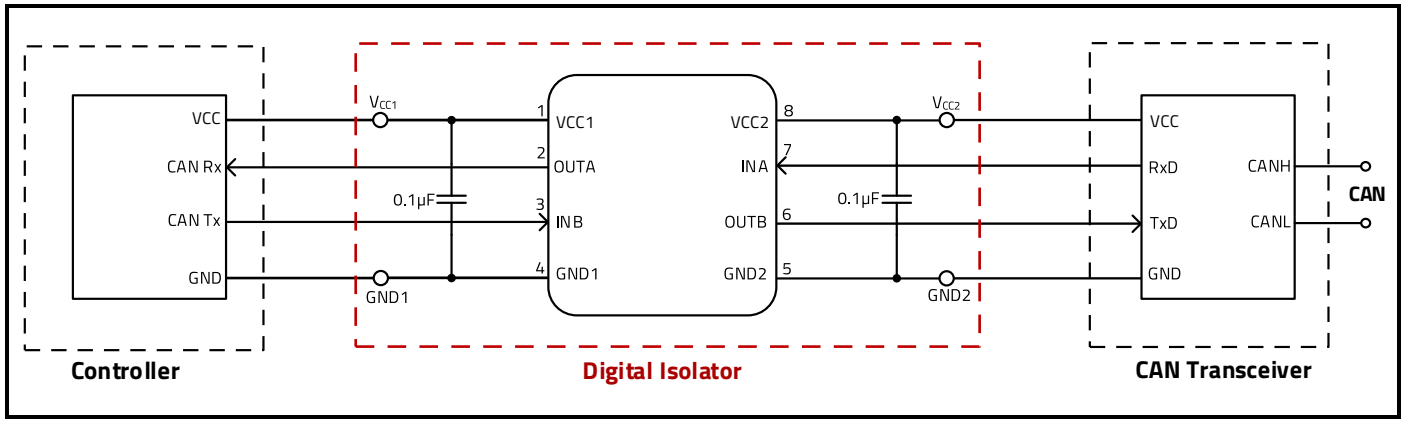


Table 13: Isolation of **RS-232 Interface** (4-Channel Unpowered Digital Isolators 18014215401x)

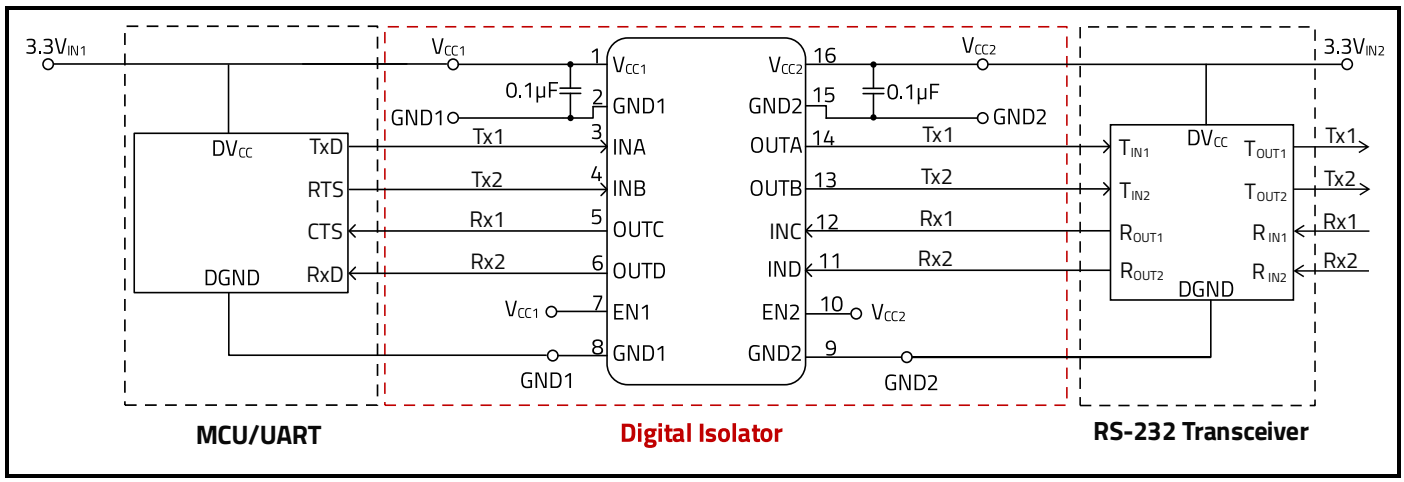


Table 14: Isolation of **RS-485 Interface** (4-Channel Powered Digital Isolators 18024115401x)

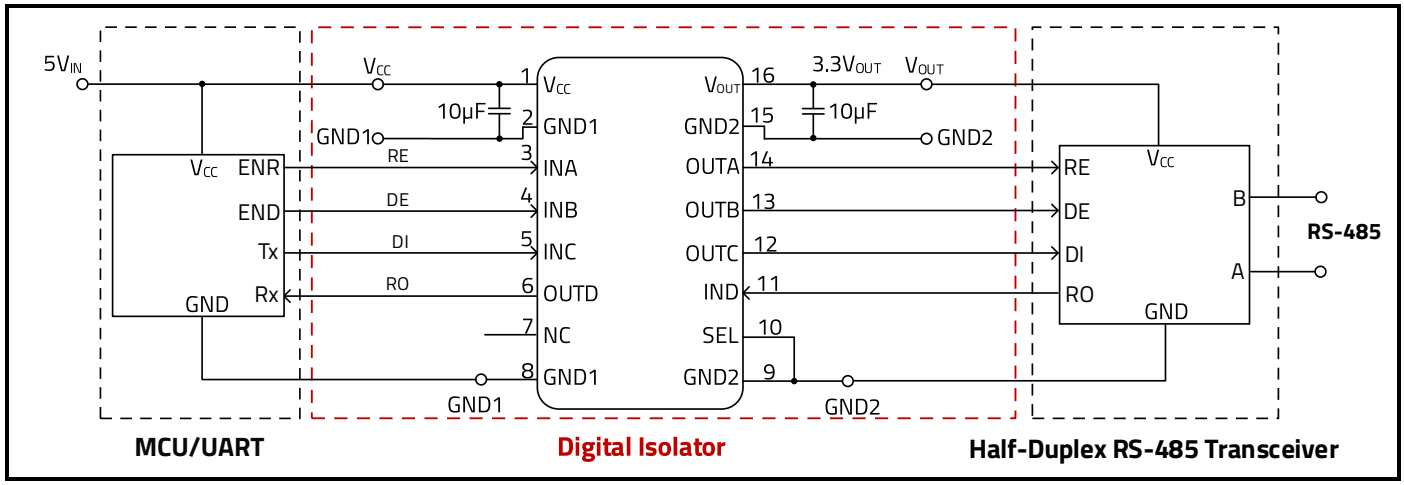


Table 15: Isolation of **SPI Interface** (4-Channel Powered Digital Isolators 18024115401x)

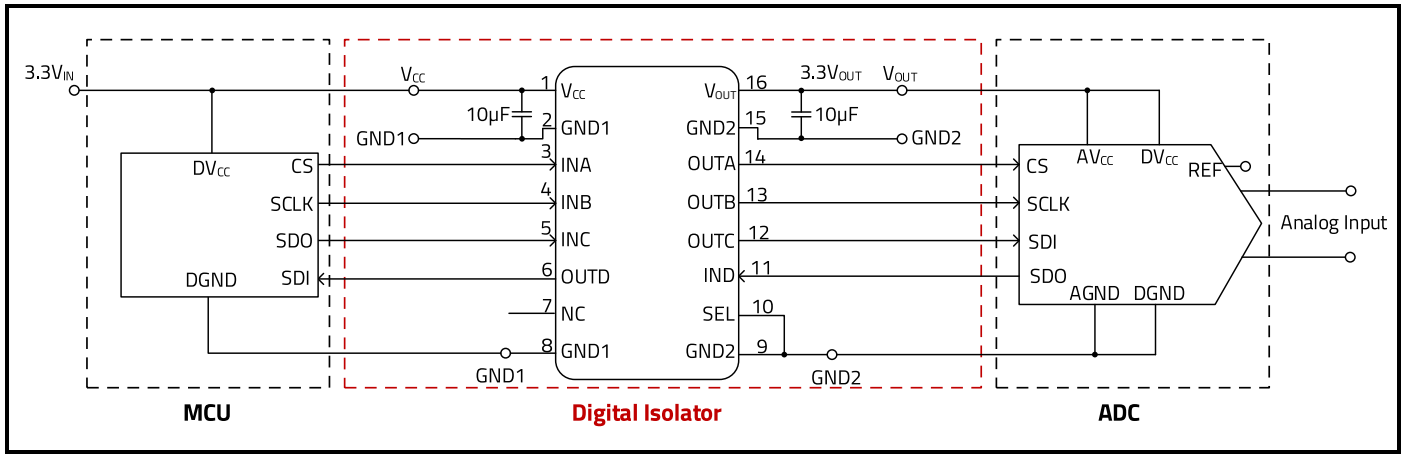


Table 16: Isolation of **Gate Drivers for Power Transistors in SMPS** (4-Channel Unpowered Digital Isolator 18014015401L)

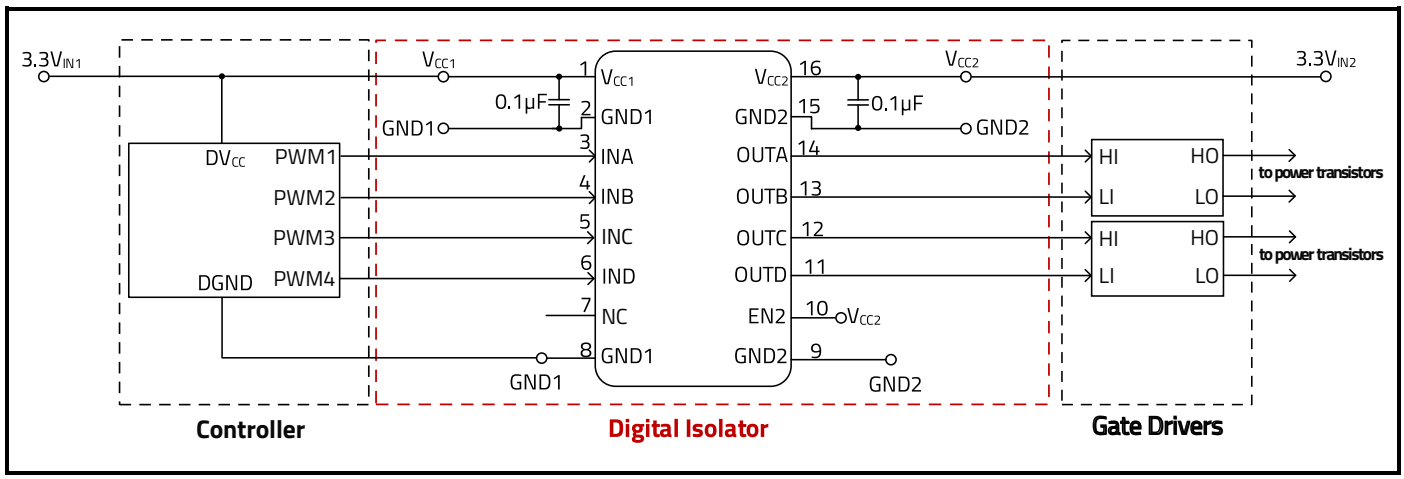


Table 17: **Isolated I² C Communication for ADC Applications** (2-Channel Bidirectional Isolator 18032011)

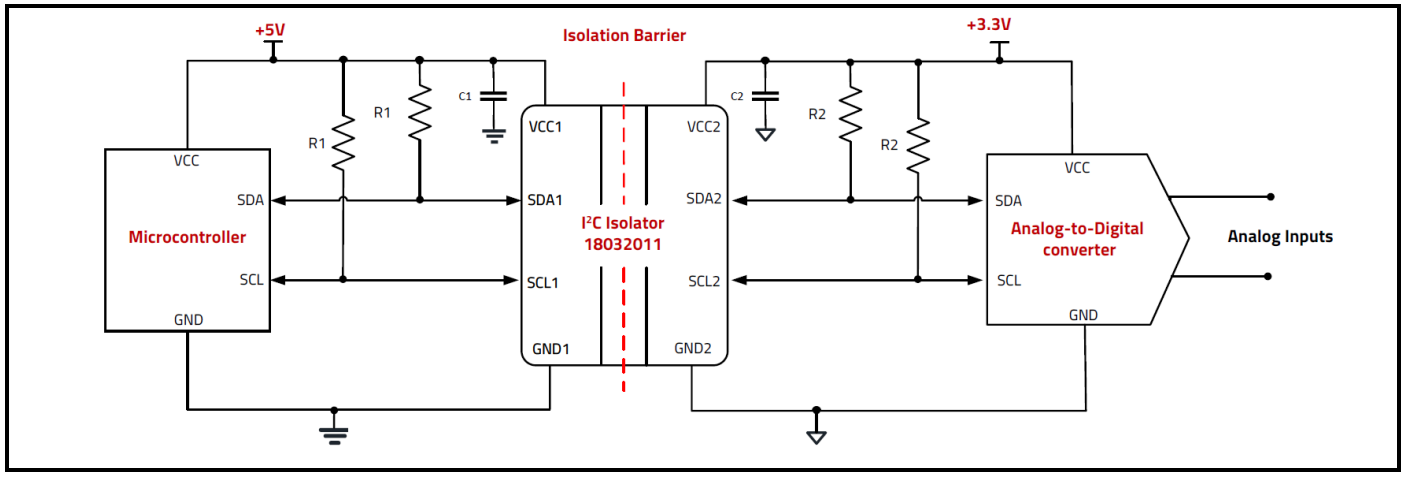
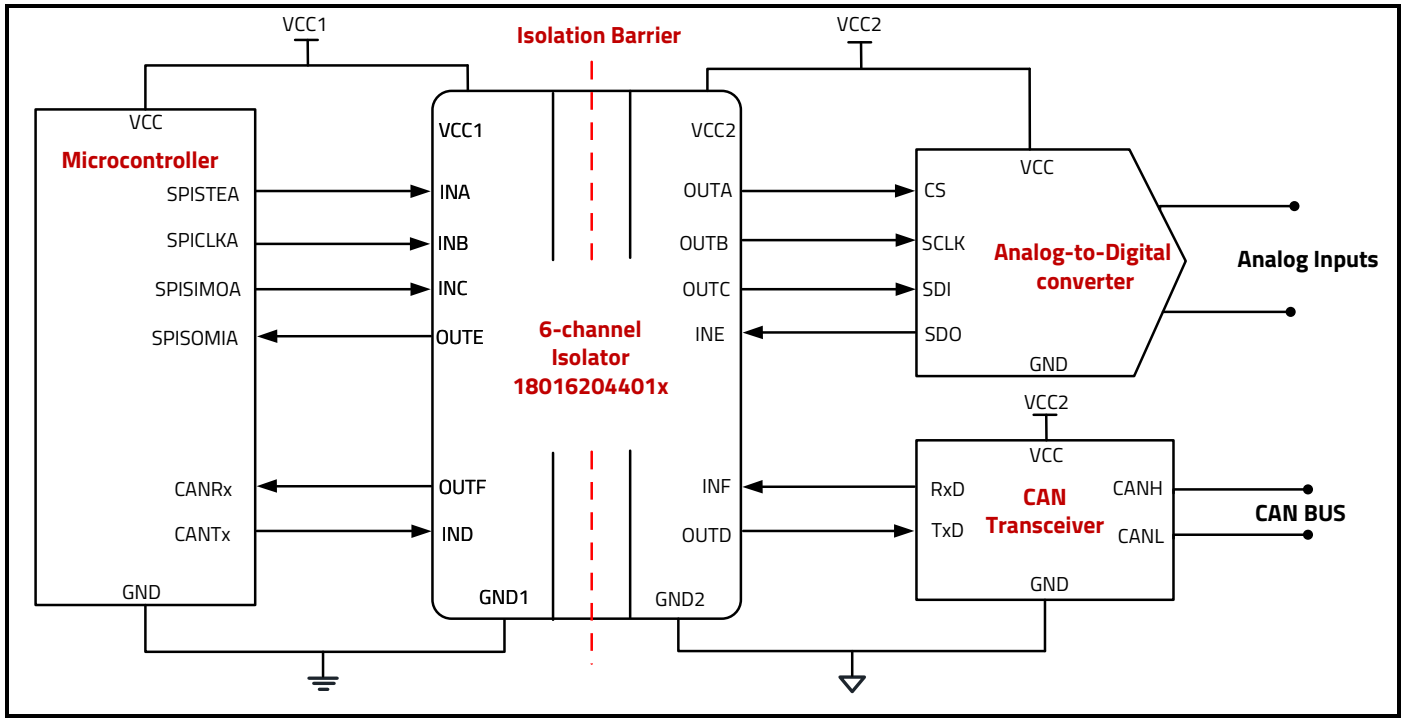


Table 18: **Isolated CAN and SPI interfaces** (6-Channel Unpowered Digital Isolator 18016204401x)



4. MEAN TIME BETWEEN FAILURES (MTBF) AND FAILURE IN TIME (FIT)

Table 19: MTBF and FIT Values of Digital Isolators without Integrated DC/DC Converters (CDIS)

MTBF and FIT data								
MTBF (Hours)	FIT	Usage temp. (°C)	Conf. level (%)	Activation energy (eV)	Test temp. (°C)	Test duration (Hours)	Sample size	Fails
4.10E+08	2.439	55	60	0.7	125	1000	4820	0
1.63E+08	6.129	55	90	0.7				

Table 20: MTBF and FIT Values of Digital Isolators with Integrated DC/DC Converters (CDIP)

MTBF and FIT data								
MTBF (Hours)	FIT	Usage temp. (°C)	Conf. level (%)	Activation energy (eV)	Test temp. (°C)	Test duration (Hours)	Sample size	Fails
2.73E+08	3.660	55	60	0.7	125	1000	3210	0
1.09E+08	9.200	55	90	0.7				

Table 21: MTBF and FIT Values of Bidirectional I^2C Isolators (CDI2C)

MTBF and FIT data								
MTBF (Hours)	FIT	Usage temp. (°C)	Conf. level (%)	Activation energy (eV)	Test temp. (°C)	Test duration (Hours)	Sample size	Fails
4.10E+08	2.44	55	60	0.7	125	1000	4822	0

5. RELIABILITY

Table 22: Reliability Test Overview for Powered (**CDIP**) and Unpowered (**CDIS**) Digital Isolators, I2C Isolators (**CDI2C**)

Test	Reference	Test Conditions
Temperature Cycling	JESD22 Method JA-104	-65°C ~ 150°C 2 cycles per hour 500 cycles
High Temperature Operational Life	JESD22-A108	CDIS/CDIP: 5.5Vin, 1MHz, 50% DC, load capacitance of 15pF, load current is 50%, 5Vout, 105°C, 1000h, daisy chained CDI2C: 5.5Vin, 400 KHz with 50% duty cycle, 125°C, 1000h
Unbiased Highly Accelerated Stress Test	JESD22-A118B	Temperature: 110°C Humidity: 85% R.H. Testing Time: 264h
External Visual	MIL-STD-883-2009	
Physical Dimension	JESD22 Method JB-100	
Mechanical Shock	MIL-STD-202-213	3 shocks in each direction (x, -x, y, -y, z, -z), peak value 100g's, duration 6ms, half-sine, velocity change 12.3ft/sec.
Vibration	MIL-STD-202-204	5g's for 20min, 12 cycles each of 3 orientations, test from 10 Hz to 2000Hz
High Temperature Storage Life	JESD22-A103	Tamb=150°C, 1000h
Low Temperature Storage Life	JESD22-A119	-65°C, 1000h
Five times Reflow	Internal	260°C peak temp.

6. INSULATION SPECIFICATION NUMBERS

Table 23: Insulation Specification Numbers

Match code	Package	Certification Number	
		DIN EN IEC 60747-17 (VDE 0884-17):2021-10	UL 1577
CDIS & CDI2C	SOIC-8NB	40058073	E535458
CDIS	SOIC-8WB	40058069	
	SOIC-16WB		
CDIP	SOIC-16WB		

7. MOISTURE SENSITIVITY LEVEL (MSL)

Table 24: Moisture Sensitivity Level Description

MSL	Floor Life	
	Time	Condition
1	Unlimited	≤ 30° / 85% RH
2	1 Year	≤ 30° / 60% RH
2a	4 Weeks	≤ 30° / 60% RH
3	**168 Hours**	**≤ 30° / 60% RH**
4	72 Hours	≤ 30° / 60% RH
5	48 Hours	≤ 30° / 60% RH
5a	24 Hours	≤ 30° / 60% RH
6	TOL (time of label)	≤ 30° / 60% RH

Table 25: Marking Description

Match code	Package	Mounting	MSL
CDIS & CDI2C	SOIC-8NB	SMD	3
CDIS	SOIC-8WB		
	SOIC-16WB		
CDIP	SOIC-16WB		

8. SOLDERING PROFILE & SOLDERING CYCLES

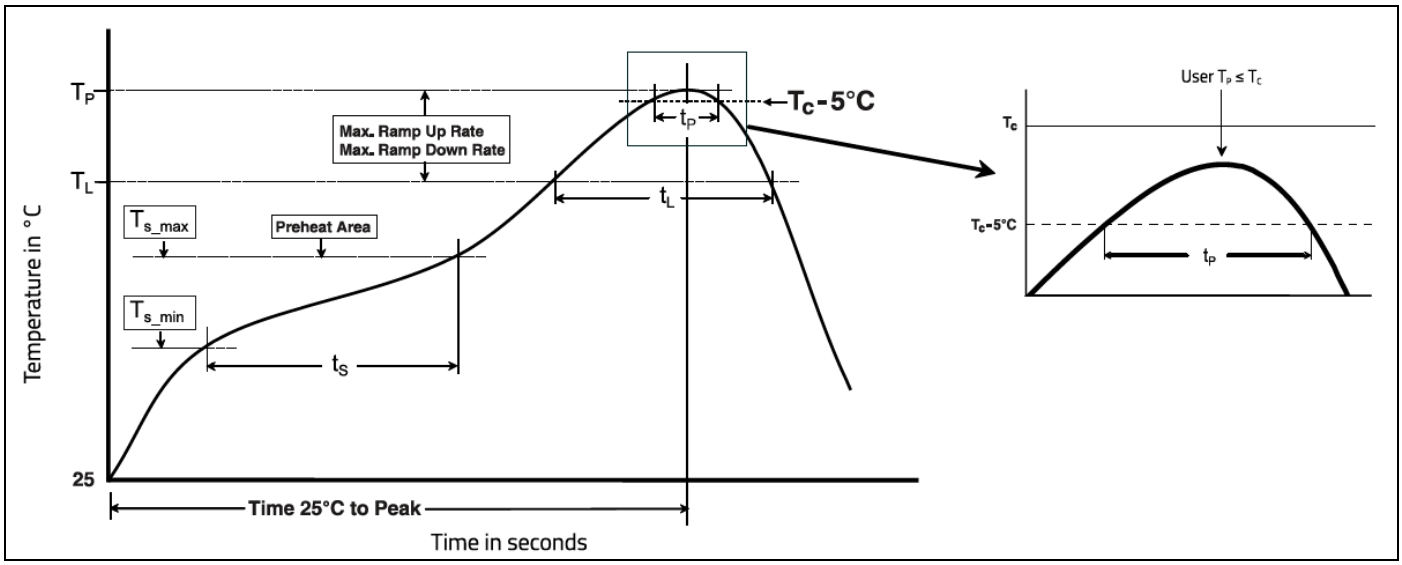


Figure 1: Soldering profile

Table 26: Soldering Profile & Soldering Cycles

Profile Feature	Symbol	Value
Preheat temperature minimum	T_{s_min}	150°C
Preheat temperature maximum	T_{s_max}	200°C
Maximum preheat time from T_{s_min} to T_{s_max}	t_s	60-120 seconds
Liquidus temperature	T_L	217°C
Time maintained above T_L	t_L	60-90 seconds
Classification temperature	T_C	260°C
Peak package body temperature	T_P	$T_P \le T_C$
Time within T_C - 5°C and T_C	t_P	$t_P \le 30$ seconds
Ramp-up rate (T_L to T_p)		3°C/second maximum
Ramp-down rate (T_P to T_L)		6°C/second maximum
Time 25°C to peak temperature		8 minutes maximum

Please refer to JEDEC J-STD020 for further information pertaining to reflow soldering of electronic components.

9. LIFETIME VS STRESS VOLTAGE

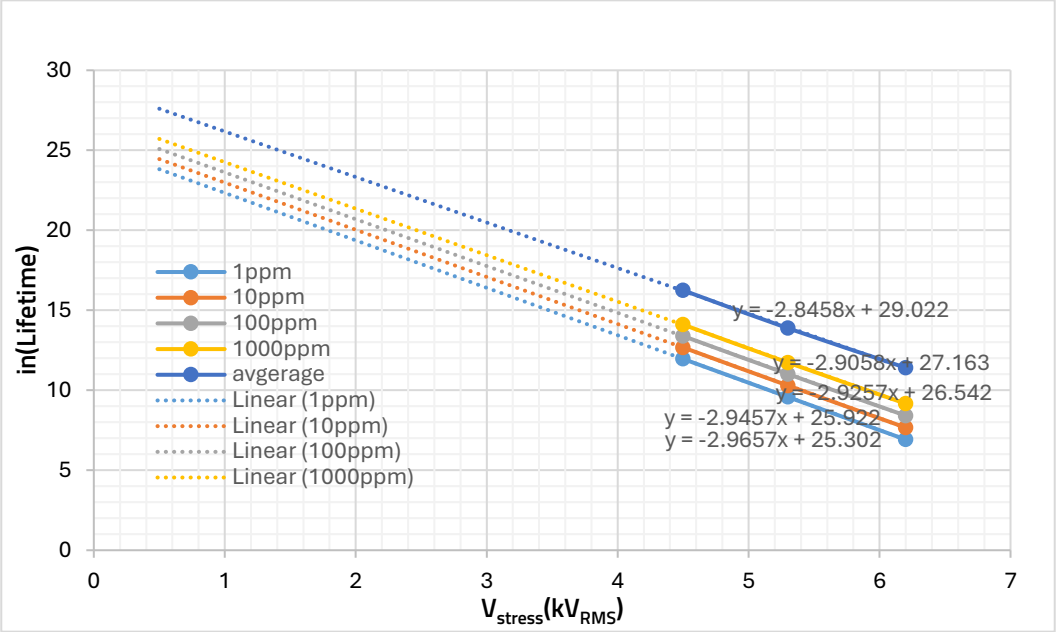


Figure 2: Lifetime vs. V_{stress} for 2- and 4-channel digital isolators without integrated DC/DC converters (CDIS)

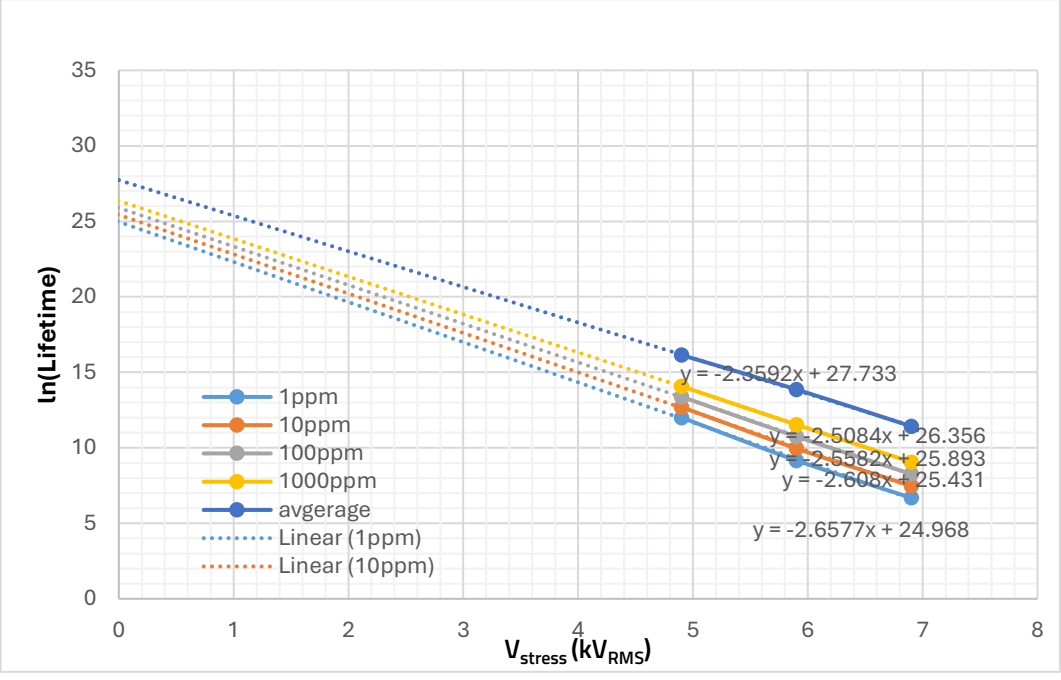


Figure 3: Lifetime vs. V_{Stress} for 4-channel digital isolators with integrated DC/DC converters (CDIP)

Lifetime charts explanation:

- **X-axis:** Continuous stress voltage (Vrms)
- **Y-axis:** Logarithm of working time (dimensionless, converted to time in seconds)

The equation to convert Y-axis values to actual lifetime in years is:

$$n(years) = \frac{e^{y}}{365 \times 24 \times 60 \times 60}$$

Where e^{y} gives time in seconds, dividing by 365×24×60×60 converts seconds into years.

For example, for V_{Stress} = 1 kV_{RMS}, the Y-axis value at 1 ppm failure rate is about 22 for the 4-channel powered and unpowered digital isolators.

$$n(years) = \frac{e^{22}}{365 \times 24 \times 60 \times 60} \approx 113\ years$$

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