APPLICATION NOTE

ANO016 | Opto-triac operation and design guide

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01. INTRODUCTION AND THEORETICAL BACKGROUND

Optocouplers using a photosensitive TRIAC as the output device are popularly known as 'phototriacs' or 'opto-triacs'. They are commonly used as an isolated AC solid-state switch in applications required to control loads fed from domestic or industrial AC-mains voltages, like valves, pumps, heaters, lamps or AC motors in home appliances, HVAC systems as well as industrial automation and construction machinery, amongst others.

Compliance to safety standards, like IEC-60335 for home appliances or IEC-60204 for electrical equipment, require that end users and maintenance operators be protected from hazardous voltages. Galvanically isolating high voltage nodes from accessible low-voltage circuitry and user interfaces helps in this endeavor. Beyond safety, it can also break ground loops, improving noise immunity in systems where the loads are at a large distance from the control circuits.

Opto-triacs are widely used to reliably bridge the isolation barrier in such cases, offering high isolation voltage ratings in a small form factor (e.g. 5 kV for WL-OCTR™ series), while still allowing 'communication' between the low and high voltage sides. However, their power dissipation capability is very low, making them unsuitable to directly control most AC-loads. For this, a high-power TRIAC or two back-to-back thyristors are commonly used together with the opto-triac, which acts as their gate driver, controlling turn-on while providing galvanic isolation between the low-power, low-voltage side and the high-power, high-voltage side. Therefore, a good understanding of the operation of all these devices is essential to design AC power control circuits.

Against this background, this application note starts with a review of thyristors and TRIACs, followed by an analysis of the operation, parameters and types of opto-triacs. Design guidance for typical application circuits is provided, supported by extensive measurements with WL-OCTR™ devices. In addition, EMC performance tests and SPICE models are also included.

RISK OF INJURY OR DEATH
RISK OF DAMAGE TO PROPERTY

Circuits and Measurements shown throughout this document use hazardous voltage levels.

The reference circuit schematics provided are simplified and do not show all components/safeguards required to safely perform high-voltage measurements.

Only qualified technical personnel familiar with the risks associated with handling high-voltage assemblies and the required safety measures should work with voltage levels above 60 V.

02. REVIEW OF THYRISTOR/SCR AND TRIAC DEVICES

Before delving into the study of opto-triacs, the basics of standalone TRIACs must be understood. For this, the fundamentals of thyristors, also referred to as silicon-controlled-rectifiers (SCRs), from which TRIACs are derived, must be revisited first.

Thyristors/SCRs

SCRs are solid-state devices first introduced in the late 1950s, shortly after the inventions of the PN junction diode and bipolar junction transistor (BJT). They gradually replaced gas-discharge tubes (thyratrons) for line voltage rectification purposes (AC to DC) and ushered in a new era by enabling accurate speed control of AC motors, among other applications for which they are still essential these days.

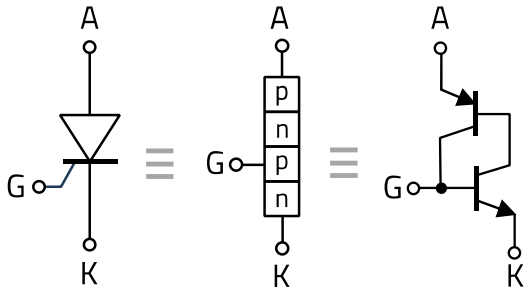

Figure 1*: SCR symbol (left), semiconductor structure (center) and equivalent circuit (right)*

The electrical symbol of a thyristor is shown on Figure 1 left. It is similar to a diode with an additional control terminal, called the 'gate'. Its simplified semiconductor structure appears at the center of Figure 1.

An SCR will conduct current if the voltage across anode and cathode (V_{AK}) is positive and higher than a threshold value (V_{fmin}), but only if sufficient current is provided through its gate-cathode PN junction. Thus, it behaves like a 'controlled turn-on diode'.

At the instant when the gate current is removed, the device will only remain in conduction if the anode current (I_A) is higher than the 'latching current (I_L)' level. Otherwise, it will turn off again. Once in conduction, the thyristor will conduct until I_A falls below the 'holding current (I_H)' level.

The simplified equivalent circuit of an SCR is shown in Figure 1 right: two NPN and a PNP bipolar transistors with base-collector terminals interconnected.

In simple terms, as soon as the NPN transistor is turned-on, so does the complementary PNP transistor, and a current (I_A) starts to flow from anode (A) to cathode (K). With enough gate bias current provided, once I_A rises sufficiently to set the combined current gain of both transistors above '1' (i.e. $I_A>I_L$) the circuit is 'self-sustaining' and will remain in conduction even after removing the gate current. Once I_A falls below I_H, the current gain will fall below unity and the transistors will turn-off.

The waveforms of Figure 3 illustrate the basic operation of an SCR based on the test circuit of Figure 2 with a resistive load. Here, its forward conduction voltage is neglected. The analysis at different time intervals is as follows:

t_0 – t_4 : before t_1, the gate current is zero and the device remains off despite positive V_{AK}. At t_1, sufficient gate current is applied. The current rises very quickly to around $V_{AC}(t_1)/R_{load}$. From here, the load current follows the expression $V_{AC}(t)/R_{load}$. At instant t_2, the gate current is removed, but as $I_{load}(t_2)>I_L$, the device remains in conduction.

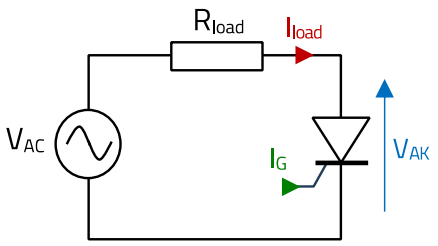

Figure 2*: SCR basic test circuit schematic*

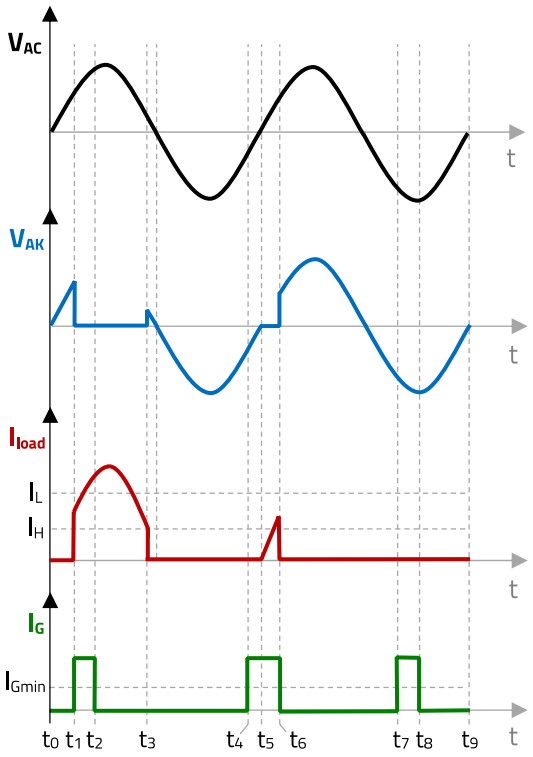

Figure 3*: SCR basic operation waveforms*

At t_3, the load current falls below the holding current $I_{load}<I_H$ and the device turns off.

t_4 – t_7 : from t_4 to t_5, the device is in reverse blocking state ($V_{AK}<0$) and it remains off even though sufficient gate current is being applied. At t_5, V_{AK} becomes positive and current builds up. At instant t_6, the gate current is removed but since $I_{load}(t_6)<I_L$, the device cannot remain in conduction and goes back to off-state..

t_7 – t_9 : between t_7 and t_8, despite enough gate current being sourced, the device is in reverse blocking state and remains off, as SCRs are unidirectional conduction devices.

The characteristic I-V curve of a thyristor is shown in Figure 4, with the following operating states: conduction (ON state), blocking (OFF state) and reverse avalanche (not used except in specialized devices). Observe how, in addition to the usual gate triggering method described above, thyristors can also be turned on in the absence of gate current, when the voltage across them exceeds their breakover voltage level (V_{BO}).

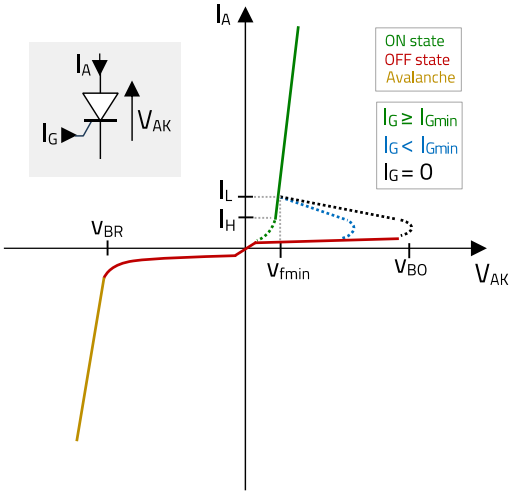

Figure 4: *SCR-Thyristor I-V characteristic curve*

However, to prevent device degradation, manufacturers do not usually recommend turning the device on in such way. Observe also in Figure 4 how, the higher the applied V_{AK} level at turn-on, the lower the necessary gate current to trigger the device into conduction.

In addition to this, SCRs suffer from a spurious turn-on mechanism occurring when an excessive rate-of-rise of voltage is applied across its anode and cathode (dV_{AK}/dt) while the device is in the off state. Such an event is commonly known as 'static dV/dt spurious turn-on'. Another important consideration is to limit the maximum dI_A/dt through the device at turn-on. Otherwise, quick degradation of the thyristor may occur due to hot spots in the semiconductor structure, compromising its long-term reliability.

TRIACs

The term 'TRIAC' is the acronym for 'TRIode for Alternating Current'. It was introduced shortly after SCRs, driven by the need for a single device capable of bidirectional current control of AC-loads, that is, capable of conducting on the positive and negative cycles of the AC mains waveform.

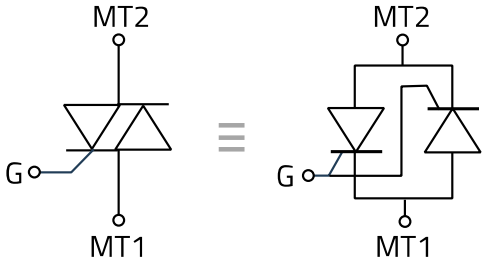

Figure 5: *TRIAC symbol (left) and equivalent circuit (right)*

Like SCRs, TRIACs remain essential devices in many AC power control applications today.

The electrical symbol of a TRIAC is shown in Figure 5 left. Note how it resembles two back-to-back SCRs and has three terminals: the control gate, MT2 and MT1. This is not a coincidence, as TRIACs behave similarly to two SCRs in an anti-parallel configuration, both controlled by a single gate terminal, as illustrated in Figure 5 right. However, they are not functionally identical solutions, and some differences need to be considered in a design.

The basic operation of a TRIAC is illustrated in the waveforms of Figure 7, based on the test circuit of Figure 6. The main difference compared to the waveforms of Figure 3 is the bidirectional versus unidirectional operation of TRIACs and SCRs.

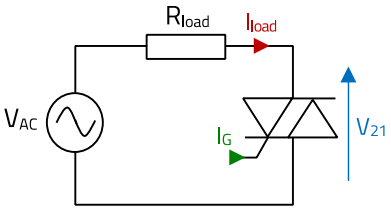

Figure 6: *TRIAC basic test circuit schematic*

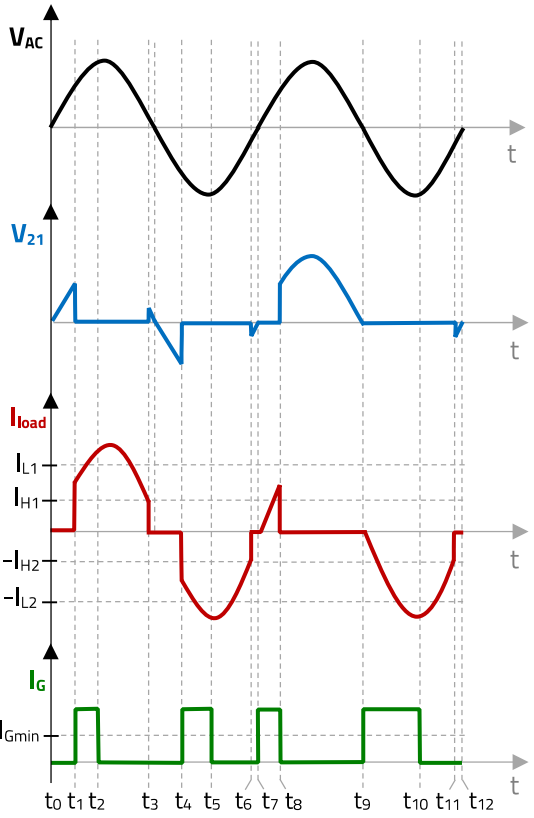

Figure 7: *TRIAC basic operation waveforms*

For completeness, the analysis is as follows:

$t_0 - t_7$: Sufficient gate current is applied at t_1, the device starts to conduct and remains in conduction after removing the gate current at t_2, since $I_{load}(t_2)>I_L$. After t_3, the current falls below I_H and the device stops conducting. The same is repeated during the negative AC cycle from t_4 through to t_7.

$t_7 - t_{12}$: At t_7, sufficient gate current is applied, the load current builds up but lies below I_L at the instant when the gate current is removed (t_8), and the device turns off again. At t_9, gate current is applied coinciding with the beginning of the positive cycle, and the device conducts until its current falls below I_H at t_{11}.

The characteristic I-V curve of a TRIAC is shown in Figure 8. It is like that of an SCR but with conduction also on negative V_{AK}. Observe also the additional turn-on mechanism by exceeding the negative breakover voltage of the device.

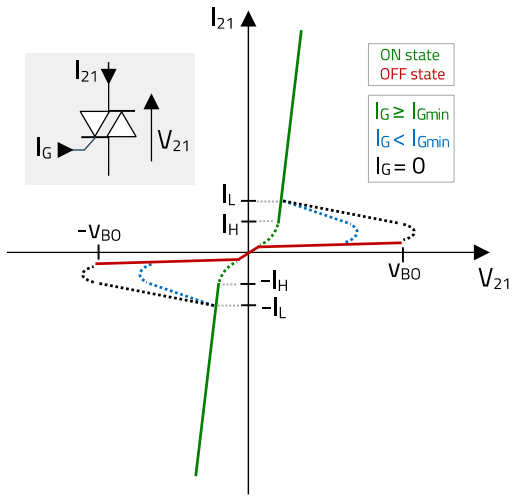

Figure 8*: TRIAC I-V characteristic curve*

The same limitations of thyristors regarding static dV/dt spurious turn-on and dI/dt limiting on turn-on also apply to TRIACs. Additionally, a TRIAC can be spuriously turned on by an excessive dV/dt and dI/dt applied across MT1 and MT2 (in either polarity) during its turn-off transition, losing control of the load. Opto-triacs also suffer from this spurious turn-on mechanism, which will be covered in more detail in section 4.2.

Another important difference of TRIAC operation compared to discrete back-to-back thyristors is that a TRIAC can be triggered by both: a positive or a negative gate current pulse (and subsequently, gate voltage (V_G)). Thus, four different triggering quadrants can be identified for a TRIAC, based on its gate current direction as well as voltage polarity across MT2 and MT1 at turn-on, as illustrated in Figure 9.

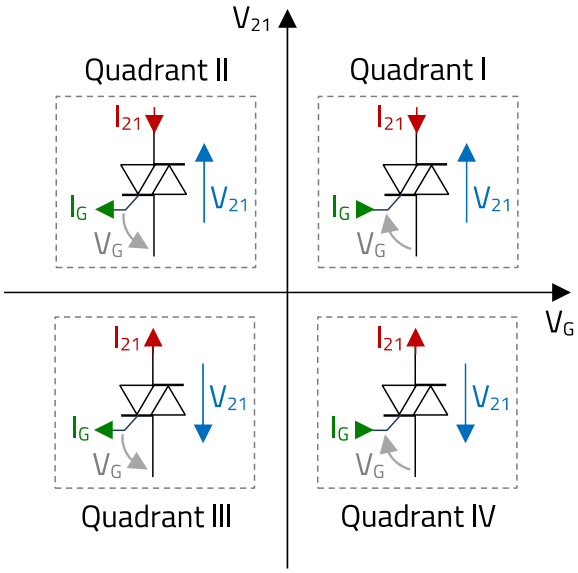

Figure 9*: Operation quadrants of a TRIAC*

Note that each quadrant has different behavior, such as required gate current, latching current and holding current levels as well as spurious turn-on sensitivity. From these, quadrant IV has the worst characteristic, requiring higher triggering current as well as being more prone to spurious turn on by commutating dV/dt and dI/dt, an important limitation when controlling inductive loads.

In most applications, the device operates in quadrants I and III, where the gate voltage polarity coincides with that of the voltage across MT2 and MT1 of the device (V_{21}). This simplifies the design of the gate driver circuit, and it is the case in the common application where a power TRIAC is driven by an opto-triac, as covered in section 05.

03. OPTO-TRIAC TYPES AND OPERATION

An opto-triac consists of a GaAs light-emitting diode (LED) optically coupled to a photosensitive TRIAC receptor (phototriac). Its electrical symbol is as shown in Figure 10.

Functionally, an opto-triac is equivalent to a very low-power TRIAC controlled by a galvanically-isolated gate terminal with unidirectional gate current.

Opto-triacs offered by Würth Elektronik are of two types: Random-Phase / Non-Zero-Cross (RP/NZC) and Zero-Cross (ZC).

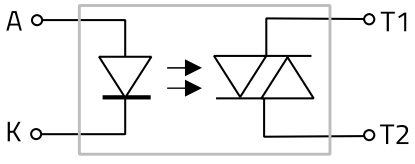

Figure 10*: Electrical symbol of opto-triac (a.k.a. phototriac)*

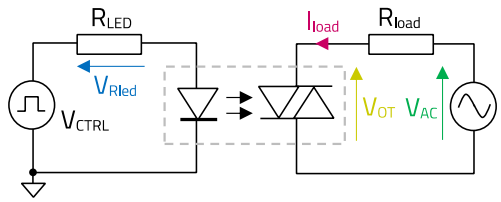

Figure 11*: Circuit of opto-triac directly controlling a resistive load*

The simplified circuit used to illustrate the behavior of the two types of opto-triacs is shown in Figure 11, with V_{CTRL}=9 V, R_{LED}=390 Ω, R_{load}=3.3 kΩ and V_{AC}=230 V. A reminder that Figure 11 is a simple functional schematic, not showing components and safety measures (e.g. fuse, isolation cabinet, etc.) required to protect against high-voltage hazards, but which are necessary to safely perform measurements.

3.1 Random-phase opto-triacs (RP)

Random-Phase (RP) are the standard type of opto-triacs, also known as 'Non-Zero-Cross' (NZC). As their name hints, they can be turned on at any phase angle of the AC voltage.

In Figure 12, example waveforms with random triggering angles are shown for a WL-OCTR 14230514010 device . Although this shows their basic functionality, they are not usually controlled in such a way, but by adjusting the triggering angle (from 0° to 180°) after the voltage crosses zero volts for the positive and/or negative half-cycles.

With this, the rms current and the amount of power delivered to the load can be precisely controlled every half-cycle of the AC-line. Example waveforms with this approach are shown in Figure 13, with a triggering angle of around 90° after AC-voltage zero-cross.

3.2 Zero-cross opto-triacs (ZC)

In a Zero-Cross device (ZC), the output phototriac turns on only when the voltage appearing across its terminals crosses zero volts, even if enough LED current was already being sourced prior to this, hence their name. This behavior is illustrated in the measured waveforms of Figure 14, obtained with a WL-OCTR 14230614010 device.

3.3 Random-phase vs Zero-cross opto-triacs

The smallest control step of a ZC opto-triac is half a line cycle (i.e. 10 ms for 50 Hz). Thus, the amount of power supplied to the load is adjusted over several half-cycles of the AC-line with an ON-OFF type of control as shown in Figure 15. This limitation makes ZC devices only suitable to control loads (via a high-power TRIAC) in which the parameter being controlled changes slowly enough, that is, has a time constant considerably larger than the AC-line period (15 to 20 ms). An example of such loads are high-power resistors adjusting the temperature in ovens and/or heating appliances.

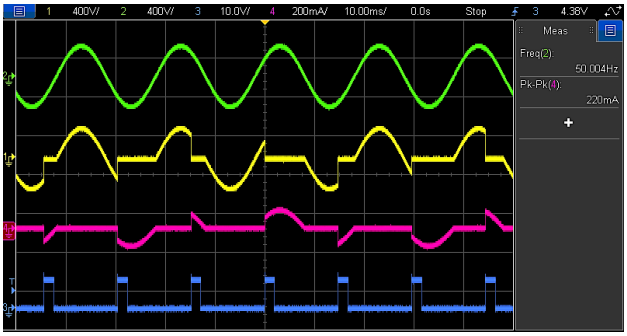

Figure 12*: RP opto-triac random control waveforms with resistive load (V_{AC} (I), V_{OT} (), I_{load} (I), V_{Rled} (I)) (DANGER: HIGH VOLTAGE)*

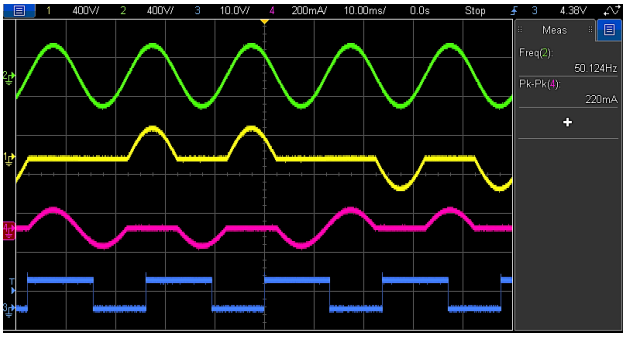

Figure 14*: ZC opto-triac waveforms with resistive load (V_{AC} (I), V_{OT} (), I_{load} (I), V_{Rled} (I)) (DANGER: HIGH VOLTAGE)*

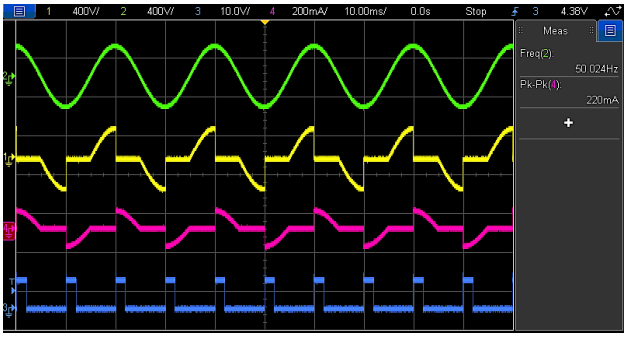

Figure 13*: RP opto-triac phase-control waveforms with resistive load (V_{AC} (I), V_{OT} (), I_{load} (I), V_{Rled} (I)) (DANGER: HIGH VOLTAGE)*

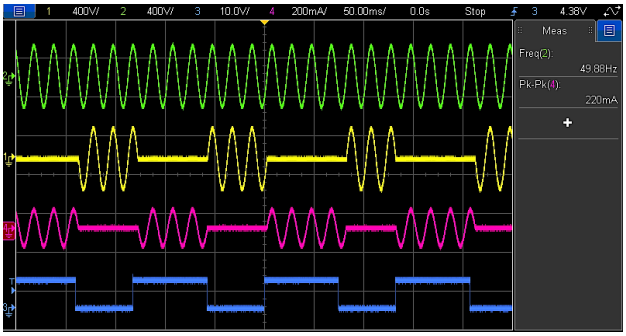

Figure 15*: ZC opto-triac waveforms with resistive load (typical control) (V_{AC} (I), V_{OT} (), I_{load} (I), V_{Rled} (I)) (DANGER: HIGH VOLTAGE)*

Contrary to this, RP opto-triacs provide faster control steps, and are then suitable for applications with short time constants like lamp dimming or speed control of universal motors, widely used in home appliances.

Note that RP devices could still be used to control the same loads as their ZC counterparts, with the control technique shown in Figure 13. But the advantage of ZC opto-triacs is their 'soft-switching' of such resistive loads, meaning that the device switches on when the load current is close to zero, resulting in low dV/dt and dI/dt on turn-on. Conversely, Figure 13 shows much higher dV/dt and dI/dt events at the turn-on of the RP opto-triac, which has severe consequences for EMI emissions, as shown in later section 06.

Using a RP opto-triac with the same slow ON-OFF control technique as in Figure 15 will still require external zero-cross detection circuitry, resulting in added solution space and cost, while this is already integrated in the ZC opto-triacs.

04. OPTO-TRIAC CHARACTERISTICS

The most important parameters and functional behavior characteristics of opto-triacs are explained in this section.

4.1 Turn-on behavior

In opto-coupler devices, the operating life of the LED emitter shortens as its operating temperature and/or its current increase [1], this being the main aspect affecting long-term reliability of the device. Therefore, keeping its conduction time short and its average current low are usual design targets. However, there are minimum levels below which the turn-on of the receiver phototriac is no longer guaranteed.

The minimum guaranteed LED current which will trigger the phototriac into conduction is known as the 'Trigger LED current' (I_{FT}). However, the datasheet value is typically specified for a pulse duration/width (PW) longer than 100 µs. For a shorter PW, especially below 20 µs, the minimum LED current required to trigger the phototriac increases dramatically.

Figure 16 shows this characteristic for a WL-OCTR 14230234010 opto-triac with I_{FT} normalized to the device's guaranteed trigger level (e.g. 5 mA at 25 °C for PW > 100 µs). Observe how the trigger LED current increases 4-fold from 5 to 20 mA as the pulse-width is reduced to 3 µs.

To better understand this behavior, measurement waveforms are provided based on the test circuit of Figure 17, with R_{LED}=100 Ω, V_D=6 V, R_{load}=100 Ω and WL-OCTR 14230234010.

With I_{LED}=5 mA and PW=100 µs, a normal triggering of the phototriac is observed in Figure 18. But after reducing the pulse width down to 12 µs, the phototriac no longer triggers (Figure 19) (note here the 10-fold reduction in the x-axis scale in Figure 19 (5 µs/div) versus Figure 18 (50 µs/div)).

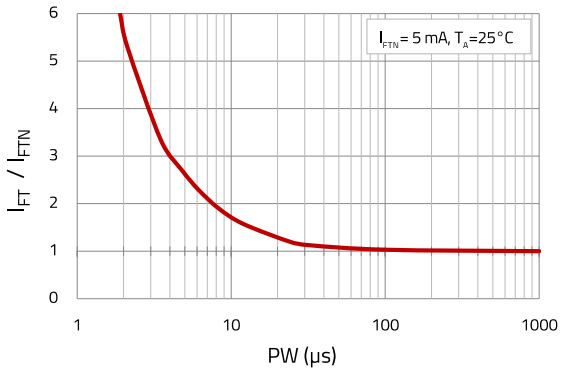

Figure 16: *Normalized I_{FT} vs PW (µs) for WL-OCTR 14230234010*

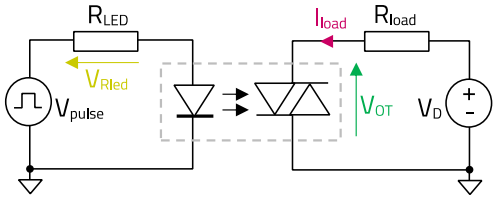

Figure 17: *Opto-triac test circuit for turn-on evaluation*

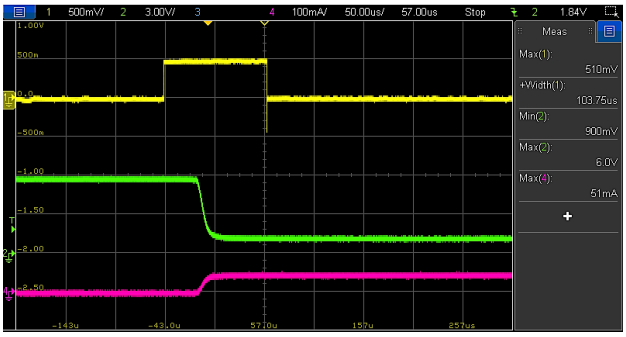

Figure 18 *Turn-on measurement for WL-OCTR 14230234010 (I_{LED}=5 mA, PW=100 µs) (V_{Rled} (), V_{OT} (), I_{load} ())*

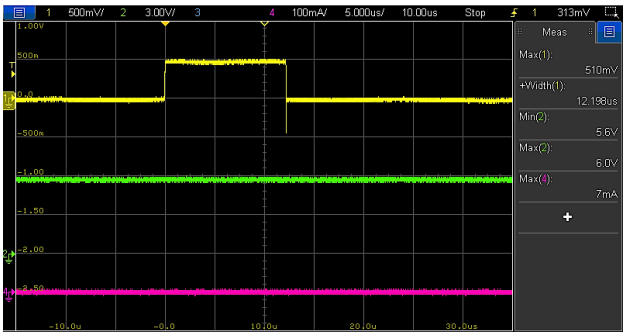

Figure 19: *Turn-on measurement for WL-OCTR 14230234010 (I_{LED}=5 mA, PW=12 µs) (V_{Rled} (), V_{OT} (), I_{load} ())*

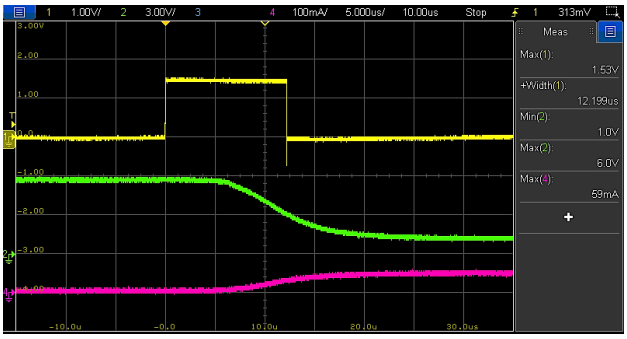

Figure 20*: Turn-on measurement for WL-OCTR 14230234010 (I_{LED}=15 mA, PW=12 µs) (V_{RLed} (), V_{OT} (), I_{load} ())*

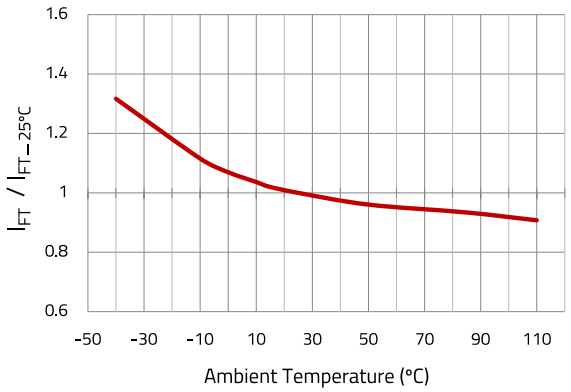

Figure 21*: Normalized I_{FT} vs Temp (°C) for WL-OCTR 14230234010*

For such a short PW, a current above 8 mA would be required (based on Figure 16). By applying I_{LED}=15 mA for 12 µs, the phototriac now turns on (Figure 20).

In addition to the dependence upon the pulse width, the minimum LED triggering current (I_{FT}) decreases with temperature, as seen in the characteristic curve of Figure 21 for the same WL-OCTR device and with I_{FT} normalized to its value at 25 °C (I_{FT_25}).

Regarding the opto-triac's switching speed, it is dependent upon the amount of photons reaching the phototriac's light-sensitive area, and in turn, upon the LED current.

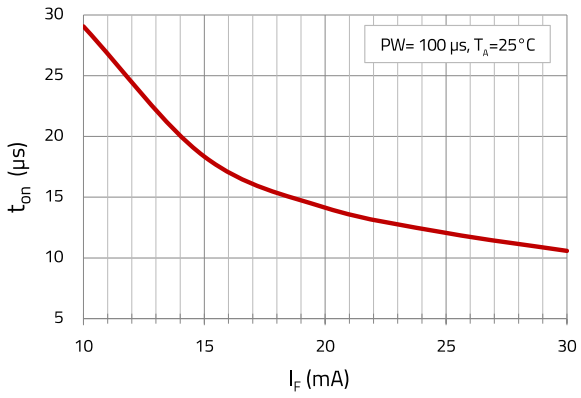

Figure 22*: t_{on} vs I_{FT} (PW=100 µs, 25 °C) for WL-OCTR 14230234010*

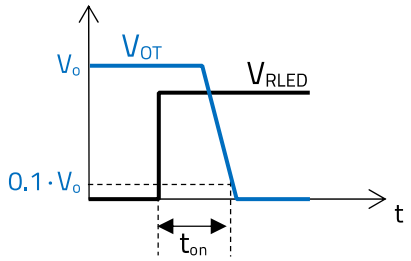

Figure 23*: Turn-on time (t_{on}) definition for opto-triac*

This behavior is shown in Figure 22 for the same WL-OCTR 14230234010 sample using a fixed current pulse-width of 100 µs. The commutation time of the opto-triac decreases as the applied LED current increases.

Note that, in these results, the turn-on time (t_{on}) is taken as the time window spanning from the instant the LED current is applied until the voltage across the phototriac falls to 10 % of its off-state level, as illustrated in Figure 23.

4.2 Spurious turn-on events

The phototriac can be spuriously turned on by similar events as for SCRs and TRIACs.

4.2.1. Spurious turn-on due to static dV/dt

A high rate of change of voltage (dV/dt) across the phototriac's terminals can cause unintended triggering while in the off state. As with SCRs and TRIACs, this event is known as spurious 'static' dV/dt turn-on.

Example sources of such static dV/dt events are sudden voltage transients and spikes appearing on the AC-mains lines. These may be caused, for example, by lightning or by the opening of electromechanical switches interrupting current to highly-inductive loads like AC-motors or solenoids, which either share the same AC-mains network as the opto-triac circuit or that are the AC-load of the high-power TRIAC that the opto-triac is in turn controlling.

The simplified test circuit used to characterize the static dV/dt capability of the WL-OCTR opto-triacs – featuring a guaranteed dV/dt capability of 1000 V/µs - is shown in Figure 24.

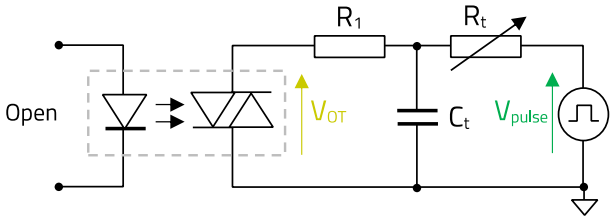

Figure 24*: Simplified opto-triac test circuit for static dV/dt turn-on*

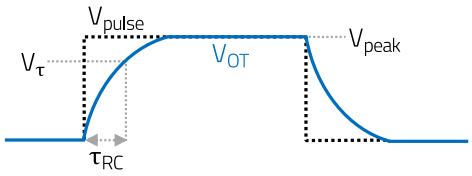

Figure 25: *Opto-triac static dV/dt waveform*

In the circuit, the network formed by R_t and C_t slows down the rise time of the voltage appearing across the opto-triac after a very fast input voltage step (V_{pulse}) is applied, as shown in Figure 25. With this, the dV/dt appearing across the device can be adjusted.

Note that the voltage pulse amplitude (V_{peak}) is set at or close to the rated breakdown voltage of the opto-triac (V_{DRM}). This represents the worst-case scenario, since for a given load, the static dV/dt that the opto-triac can withstand without spuriously turning on decreases as the applied voltage peak increases.

In the circuit, R_1=10 kΩ limits the worst-case peak current through the opto-triac (e.g. to 60 mA for a 600 V device), also protecting it when the capacitor C_t discharges every cycle.

Back to Figure 25, τ_{RC} is the time constant of the R_t-C_t network, as follows:

$$V_\tau = 0.632 \cdot V_{peak} \quad \text{(E.1)}$$

$$\tau_{RC} = R_t \cdot C_t \quad \text{(E.2)}$$

The static dV/dt across the opto-triac can be then set as:

$$\frac{dv}{dt} = \frac{V_\tau}{\tau_{RC}} \quad \text{(E.3)}$$

In Figure 26, measurements are shown for a WL-OCTR 14230514010 sample opto-triac withstanding a dV/dt of 3000 V/µs without spurious turn-on (see ΔY/ΔX). Here, V_{peak}=V_{DRM}=600 V (thus ΔY=V_τ=385 V) and ΔX=τ_{RC}=128 ns. In Figure 27, a spurious turn-on event for the same device caused by a higher static dV/dt of 11000 V/µs can be observed.

Note that the static dV/dt rating given in the WL-OCTR datasheet of 1000 V/µs is an absolute worst-case level, already factoring in effects of tolerance and temperature variations, as the withstanding static dV/dt capability of the device also decreases as the operating temperature increases. This means that these devices will withstand a higher static dV/dt when just tested 'on the bench', as these results confirm.

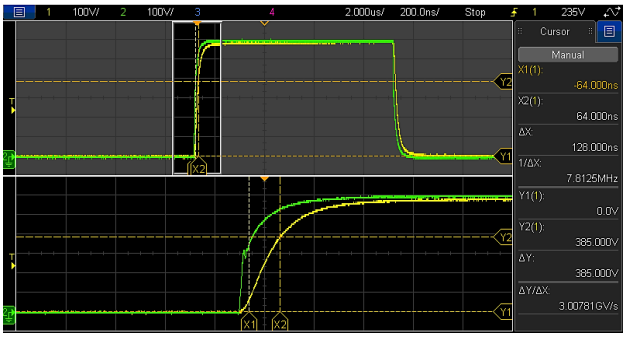

Figure 26: *WL-OCTR 14230514010 results with applied static dV/dt of 3 kV/µs at V_{peak}=600 V (V_{OT} (I), V_{pulse} (I)) (DANGER: HIGH VOLTAGE)*

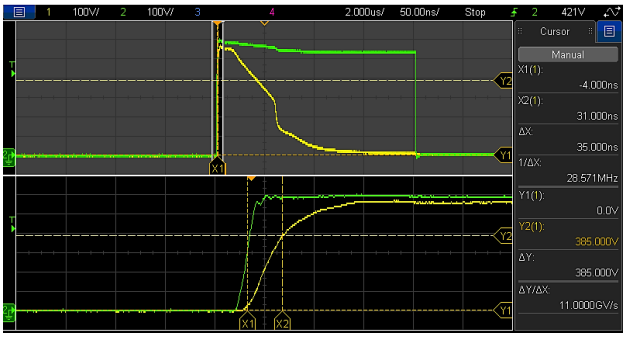

Figure 27: *WL-OCTR 14230514010 results with applied static dV/dt of 11 kV/µs at V_{peak}=600 V (V_{OT} (I), V_{pulse} (I)) (DANGER: HIGH VOLTAGE)*

4.2.2. Spurious turn-on due to commutating dV/dt and dI/dt

As in the case of standalone TRIACs, phototriacs may not turn off if the rate of change of voltage (dV/dt) across its terminals and/or current (dI/dt) through the device during the turn-off transition exceed certain levels.

This characteristic is somewhat complex, as the minimum dV/dt causing spurious turn-on of the phototriac is, in turn, dependent upon the rate of change of current (dI/dt) through the device as well as its operating temperature. Generally, the higher the dI/dt while the device is turning off and the higher its operating temperature, the lower the dV/dt that will trigger the opto-triac into conduction again. In contrast to the static dV/dt turn-on, this event is referred to as 'dynamic' or 'commutating' dV/dt and dI/dt spurious turn-on.

Loads with dominant inductive elements are the main concern for these events, due to the substantial phase shift between voltage and current waveforms on turn-off. However, this behavior can also be studied using the previous circuit of Figure 11 with a simple resistive load and sinusoidal waveforms, despite the voltage and current being (almost) in phase.

The dV/dt of a sinusoidal voltage waveform as it crosses through zero Volts can be approximated as in Figure 28.

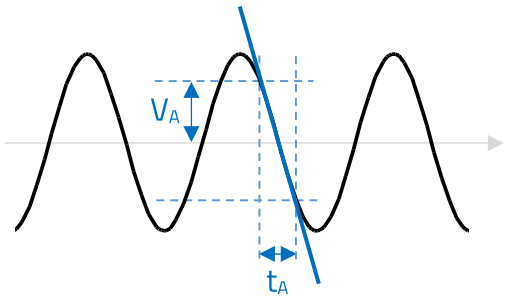

Figure 28: *Accurate dV/dt approximation of a sinusoidal voltage*

Here, V_A is set to around 70% of the peak voltage (V_{pk}), a value almost the same as its V_{rms} level:

$$V_A \approx 0.7 \cdot V_{pk} \approx \frac{V_{pk}}{\sqrt{2}} = V_{rms} \quad \text{(E.4)}$$

The interval t_A can be obtained as follows:

$$t_A = \frac{\sin^{-1} 0.7}{\pi \cdot f} \approx \frac{0.25}{f} \quad \text{(E.5)}$$

Where 'f' is the frequency. The dV/dt is then approximated as below:

$$\frac{dV}{dt} \approx \frac{2 \cdot V_A}{t_A} \approx 8 \cdot V_{rms} \cdot f \quad \text{(E.6)}$$

For a purely resistive load, the resulting dI/dt is:

$$\frac{dI}{dt} \approx \frac{dV/dt}{R_{load}} \quad \text{(E.7)}$$

E.6 and E.7 show that the frequency, the AC voltage amplitude and the load resistance can be separately adjusted to set different rates of change of voltage and current.

Taking the circuit of previous Figure 11 as reference with a WL-OCTR 14230224010 sample, Figure 29 shows measurements for V_{rms}=60 V, f=150 Hz and R_{load}=900 Ω, resulting in dV/dt=72 kV/s and dI/dt=80 A/s. The opto-triac operates correctly under these conditions.

If for the same V_{rms}=60 V, f=150 Hz and dV/dt=72 kV/s, the load resistor is reduced from 900 Ω down to 600 Ω, the RMS load current is increased to around 100 mA and with it, the dI/dt increases from 80 A/s up to 120 A/s. Figure 30 shows how the phototriac no longer turns off when the load current goes to zero after the LED current has been removed. Control has been lost due to the higher commutating dI/dt applied.

However, if the voltage is now decreased from 60 V down to 30 V, the dV/dt is also reduced by half from 71 kV/s down to 36 kV/s. To set the same dI/dt of 120 A/s as in the previous case, R_{load} must now be set to 300 Ω.

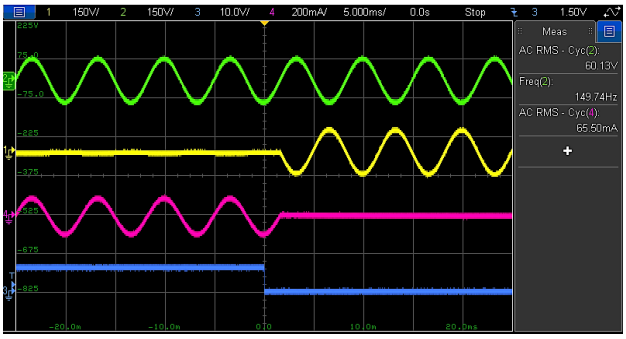

Figure 29: *WL-OCTR 14230224010 with commutating dV/dt of 72 kV/s and dI/dt of 80 A/s applied (V_{AC} (I), V_{OT} (I), I_{load} (I), V_{RIed} (I))*

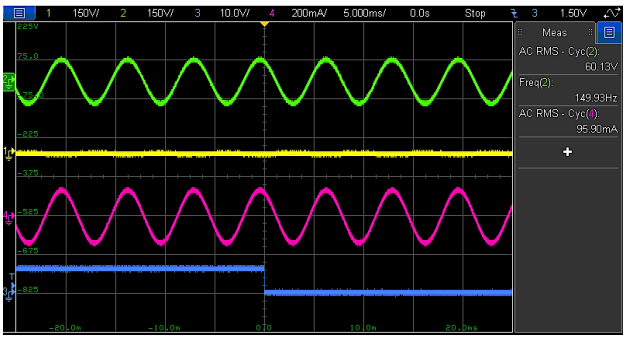

Figure 30: *WL-OCTR 14230224010 with commutating dV/dt of 72 kV/s and dI/dt of 120 A/s applied (V_{AC} (I), V_{OT} (I), I_{load} (I), V_{RIed} (I))*

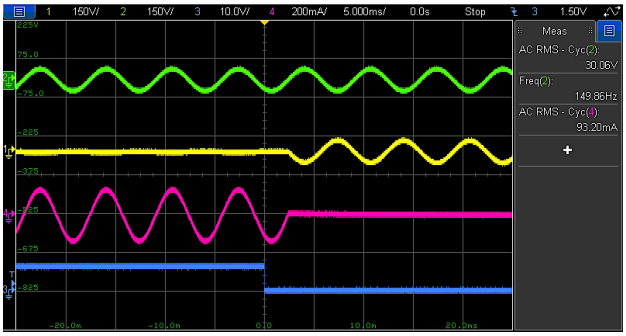

Figure 31: *WL-OCTR 14230224010 with dV/dt of 36 kV/s and dI/dt of 120 A/s applied (V_{AC} (I), V_{OT} (I), I_{load} (I), V_{RIed} (I))*

Figure 31 shows how, after the reduction in dV/dt, correct functionality has been restored even with the higher dI/dt of 120 A/s. These measurements show the interdependence between commutating dV/dt and dI/dt levels causing spurious turn-on.

It must be noted that opto-triacs are much more sensitive to such spurious turn-on events than high-power TRIACs. Especially when attempting to directly control a low-power, highly-inductive load with a WL-OCTR device, this behavior must be carefully assessed. Note that there are many low-power, synchronous AC-motors (<10 W) with very high winding resistance in the kΩ range, appearing more resistive than inductive to the phototriac.

4.3 Opto-triac in conduction

The instantaneous voltage drop across the phototriac as a function of the instantaneous current flowing through it is shown in Figure 32.

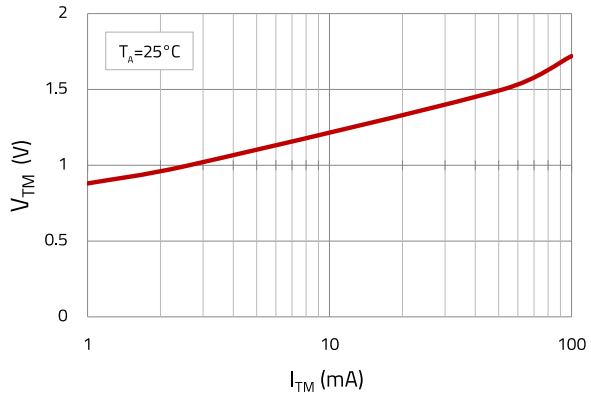

Figure 32: *V_{TM} vs I_{TM} at 25 °C for WL-OCTR series*

This was measured at room temperature (25 °C), but the maximum on-state voltage of the phototriac can be as high as 2.5 V when the influence of tolerance spreads is factored in (maximum V_{TM} specified on WL-OCTR datasheet). Therefore, this value should be used for worst-case power dissipation calculations.

4.4 Off-state considerations

The instantaneous maximum voltage that the phototriac can safely block each cycle is referred to as its 'repetitive peak off-state voltage' rating (V_{DRM}).

The WL-OCTR opto-triacs are offered with different V_{DRM} ratings of 250 V, 400 V and 600 V at 25 °C, covering different AC-mains peak voltages around the world.

The dependence of the V_{DRM} rating with temperature is shown in Figure 33. Considering an ambient temperature range from -40°C to 110 °C, a maximum V_{DRM} deviation of around ±10% from the nominal level (25 °C) can be expected.

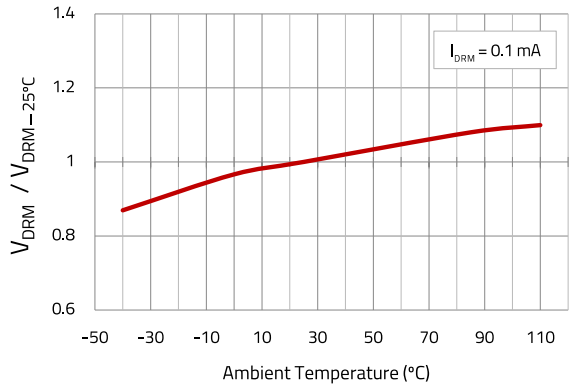

Figure 33: *Normalized V_{DRM} vs T_{amb} at 0.1 mA for WL-OCTR series*

When the phototriac is in off-state and a voltage is applied across its terminals without any LED current, a small leakage current (I_{DRM}) will flow. As the temperature and/or the applied voltage increase, so does the leakage current level, as shown in Figure 34.

Generally, I_{DRM} is an important parameter to consider when an opto-triac is used to drive a high-power TRIAC, especially those with highly-sensitive gates. In such case, the maximum I_{DRM} must be lower than the minimum gate triggering current of the TRIAC. However, with a maximum leakage current around 1 µA, this is hardly an issue with the WL-OCTR devices and modern-day TRIACs.

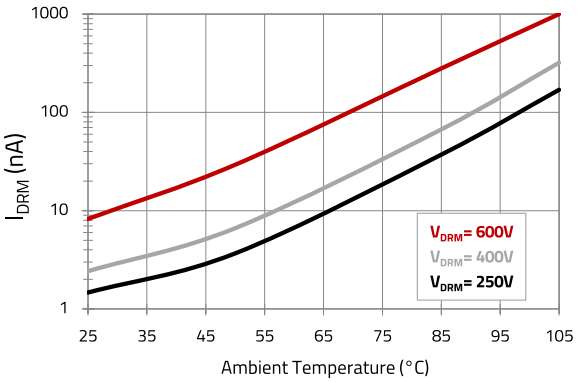

Figure 34: *I_{DRM} vs T_{amb} at different V_{DRM} for WL-OCTR series*

4.5 Other parameters

A similar IR-LED device is used for the WL-OCTP phototransistor optocoupler series and the WL-OCTR phototriac optocoupler series, whose parameters are already covered in the application note ANO007 [2]. In addition to these, parameters related to the isolation barrier, like isolation voltage (V_{ISO}), floating capacitance (C_{IO}) and isolation resistance (R_{ISO}) are also equivalent and explained in the above reference.

The following two parameters are specific to the phototriac receiver:

Holding current (I_H) – As in standalone TRIACs, once the current through the phototriac falls below this level, it will stop conducting and go into off state. This current is in the order of 200-400 µA for the WL-OCTR series.

Peak non-repetitive surge current (I_{TSM}) – Specified for a pulse-width of 100 µs and 120 pps (pulses-per-second) (i.e. corresponding to 60 Hz line frequency). It is the maximum guaranteed peak current that the phototriac can withstand for the mentioned conditions, and key to consider in the target application of the WL-OCTR opto-triac as a TRIAC gate driver, explained in next section.

05. DESIGNING WITH OPTO-TRIACS

Opto-triacs within the WL-OCTR series have power dissipation ratings of just a few hundreds of milliwatts (e.g. around 300 mW), so they would only be capable of controlling loads drawing a maximum steady-state current below 100-150 mA (considering V_{TM_max} = 2.5 V). Examples of such loads are buzzers, indicator lamps and low-power AC-motors (below typ. 10 W). However, limitations regarding commutating spurious turn-on events as well as maximum inrush/surge currents, among others, must be carefully characterized and considered in the design.

In most cases, the load is controlled directly by standalone TRIACs, with the opto-triac controlling the TRIAC turn-on while providing galvanic isolation between the low-voltage and high-voltage sides. This is the main application of the WL-OCTR series, and it will be covered here in more detail.

5.1 Opto-triac as TRIAC driver

Figure 35 shows the simplified circuit schematic of an isolated AC-load control circuit with TRIAC and opto-triac.

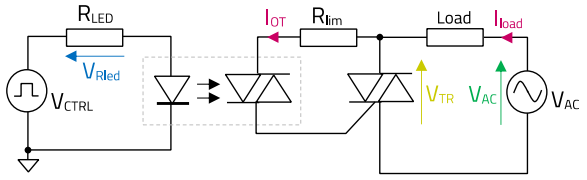

Figure 35: *Opto-triac as an isolated TRIAC driver (basic circuit)*

Observe how the gate current of the TRIAC flows through the phototriac. This gate current is set by the AC voltage appearing across the load and the limiting resistor R_{lim}. Ignoring the voltage drop across the load and phototriac, the minimum R_{lim} that keeps the maximum phototriac peak current below its rating (I_{TSM_OT}) is approximated as follows:

$$R_{lim} > \frac{V_{rms} \cdot \sqrt{2}}{I_{TSM\_OT}} \qquad (E.8)$$

Note that the schematic in Figure 35 only shows the basic functional circuit, but additional components may be required for protection and reliable operation depending on the load as well as TRIAC and opto-triac ratings, as explained later.

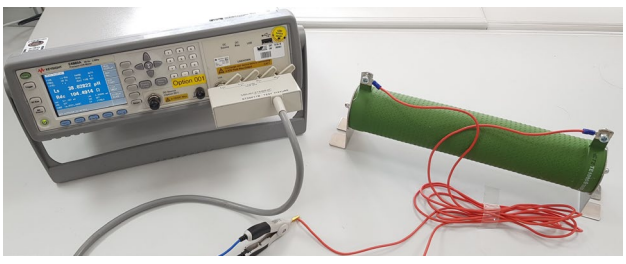

Figure 36: *L-R measurement of the resistive load used (100 Ω, 1 kW)*

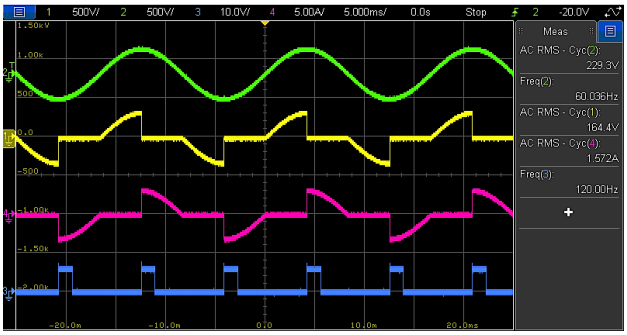

Figure 37: *Circuit waveforms for TRIAC driven by RP opto-triac at $\Phi_{trigger}$ ~ 90° with resistive load (V_{AC} (I), V_{TR} (), I_{load} (I), V_{RLed} (I)) (DANGER: HIGH VOLTAGE)*

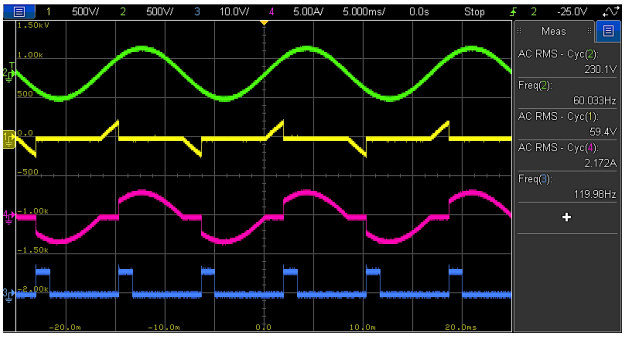

Figure 38: *Circuit waveforms for TRIAC driven by RP opto-triac at $\Phi_{trigger}$ ~ 30° with resistive load (V_{AC} (I), V_{TR} (), I_{load} (I), V_{RLed} (I)) (DANGER: HIGH VOLTAGE)*

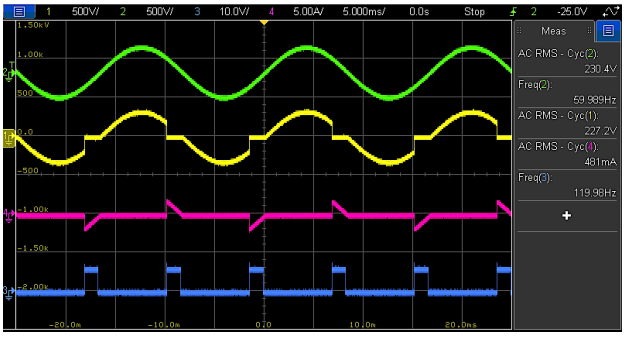

Figure 39: *Circuit waveforms for TRIAC driven by RP opto-triac at $\Phi_{trigger}$ ~ 150° with resistive load (V_{AC} (I), V_{TR} (), I_{load} (I), V_{RLed} (I)) (DANGER: HIGH VOLTAGE)*

Measurement waveforms obtained with V_{rms}=230 V / 60 Hz, R_{lim} = 440 Ω, Load = 100 Ω / 40 µH at 50 Hz (Figure 36), a random-phase opto-triac (WL-OCTR 14230234010) and the TRIAC BTA16-600BWRG [3] from STMicro are shown in Figure 37 for a triggering phase angle of around 90°. Note how the TRIAC waveforms are equivalent to those of the phototriac in previous Figure 13, albeit with the TRIAC now conducting the higher load current.

In Figure 38 and Figure 39, the equivalent waveforms for phase control angles of 30° and 150° are shown for further insight on the adjustment of the load power.

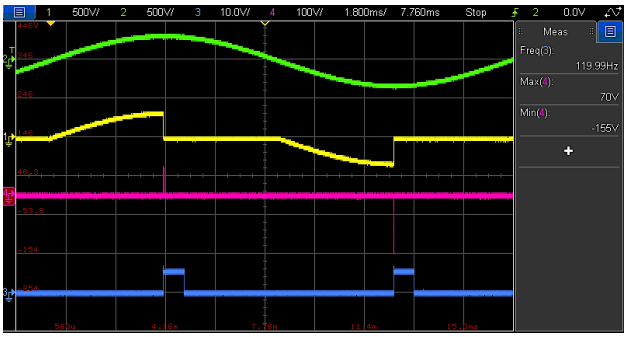

Figure 40: *Detail of TRIAC turn-on ($\Phi_{trigger}$ ~90°) and RP phototriac current for positive and negative AC-line cycles with resistive load (V_{AC} (I), V_{TR} (), I_{OT} (I), V_{Rled} (I)) (DANGER: HIGH VOLTAGE)*

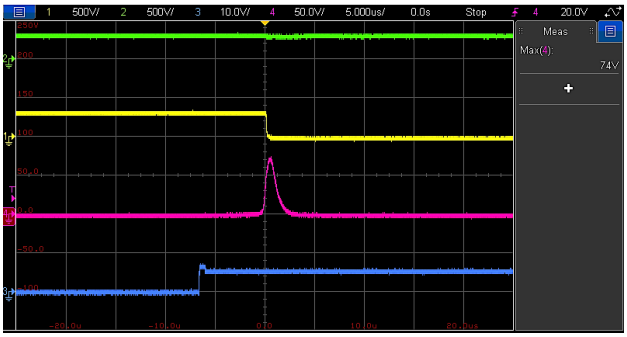

Figure 41: *Zoomed-in detail of TRIAC turn-on at $\Phi_{trigger}$ ~90° with RP opto-triac and resistive load (V_{AC} (I), V_{TR} (), I_{OT} (I), V_{Rled} (I)) (DANGER: HIGH VOLTAGE)*

In Figure 40, the TRIAC gate current is shown instead of the load current. Observe how the phototriac only conducts for a very short time window (~2 µs), until the TRIAC turns on.

Due to its very low level, the phototriac current is indirectly obtained from the voltage drop across R_{lim} (440 Ω). With this, measured peak values of 70 V and -155 V on the positive and negative half-cycles equate to 160 mA and 350 mA phototriac peak currents, well below its peak rating of 1 A.

Figure 41 shows a close-up capture of the turn-on event during the positive cycle. Based on previous Figure 9, the TRIAC operates in quadrants I and III when driven by an opto-triac as in the schematic of Figure 35.

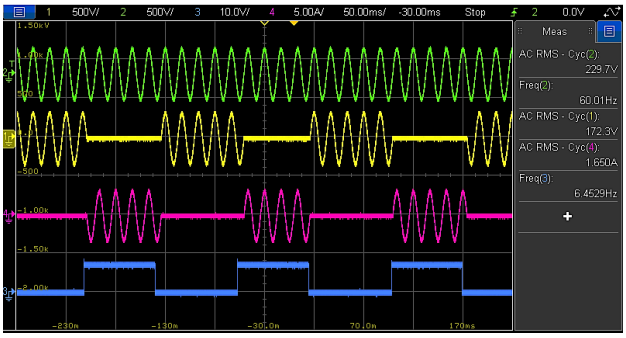

Figure 42: *Circuit waveforms for TRIAC driven by ZC opto-triac with resistive load (V_{AC} (I), V_{TR} (), I_{load} (I), V_{Rled} (I)) (DANGER: HIGH VOLTAGE)*

Figure 43: *Circuit waveforms for TRIAC driven by ZC opto-triac zoomed in on TRIAC conduction cycles with resistive load (V_{TR} (I), V_{TR} (), I_{OT} (I), V_{Rled} (I)) (DANGER: HIGH VOLTAGE)*

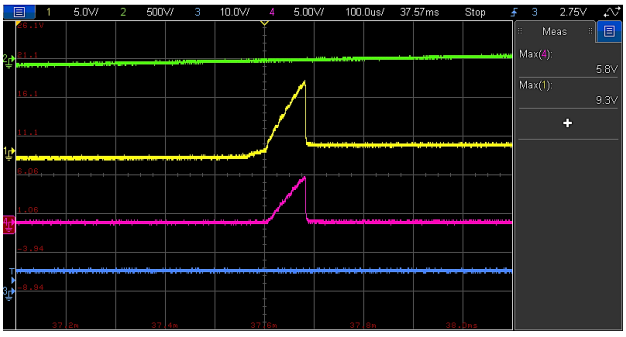

Figure 44: *Zoomed-in detail of TRIAC turn-on with ZC opto-triac and resistive load (V_{AC} (I), V_{TR} (), I_{OT} (I), V_{Rled} (I)) (DANGER: HIGH VOLTAGE)*

Considering now a ZC opto-triac (WL-OCTR-14230434010), the respective measurements are shown in Figure 42, where the equivalence to the waveforms of previous Figure 15 can be corroborated. Figure 43 shows the waveforms zoomed in over the five AC-line cycles during which the TRIAC conducts in this example. The small voltage scale (5 V/div) allows to observe the positive and negative forward voltage drop of the TRIAC (top-half of the oscilloscope capture), corresponding to the positive and negative conduction cycles, respectively.

At the beginning of every half-cycle, small spikes of voltage and current are observed on the TRIAC and phototriac, respectively. Zooming in on the bottom half of Figure 43, and further in Figure 44 shows the detail of the turn-on event during the positive-going zero-crossing of the AC-line voltage.

Based on the circuit of Figure 45, the AC-line voltage appears across R_{load}, R_{lim}, the phototriac terminals and the G-A1 connection of the TRIAC at the beginning of every half-cycle. As this voltage rises (in absolute value), so does the TRIAC's gate current (I_{GT}), whose instantaneous value can be approximated as below:

$$I_{GT}(t) = \frac{(V_{AC}(t)-V_{OT}(t)-V_{G1}(t))}{(R_{lim}+R_{load})} \qquad (E.9)$$

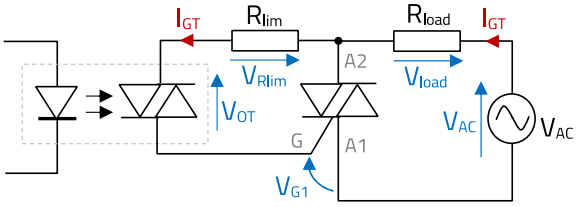

Figure 45*: Reference loop of voltages and gate current with ZC opto-triac before TRIAC turn-on after AC-line zero-crossing*

As soon as $I_{GT}(t)$ reaches the TRIAC trigger level, the device starts to conduct and the impedance across it dramatically reduces far below the value of R_{lim}. With this, the voltage appearing across R_{lim} and the phototriac falls below the TRIAC forward conduction voltage (V_{TR}), which in turn causes the phototriac current to fall below its holding current level, turning the device off. With a ZC opto-triac, this repeats at the start of every half-cycle of the line voltage as long as enough LED current is being sourced.

In the results of Figure 44, the TRIAC voltage reached 9 to 10 V and the gate current around 13 mA (i.e. 5.8 V across 440 Ω). Considering a total voltage drop of 2 V for V_{OT}+V_{G1} at the triggering point, the remaining 7 V appearing across R_{lim} (440 Ω) and the load resistor (100 Ω) would correspond to the measured 13 mA peak gate current based on E.9.

Note that the gate triggering current of the TRIAC used (BTA16-600BWRG [3]) is actually specified to be 50 mA . However, this is a worst-case guaranteed trigger level, meaning that many devices may also trigger at a lower gate current when tested 'on-the-bench', as in this case.

So far in the analysis and tests, a predominantly resistive load has been considered, with current and voltage waveforms being almost in phase. Contrary to this, loads with dominant reactive elements (i.e. inductive or capacitive) will cause a phase shift between voltage and current, reaching up to 90° in the complete absence of any resistive element.

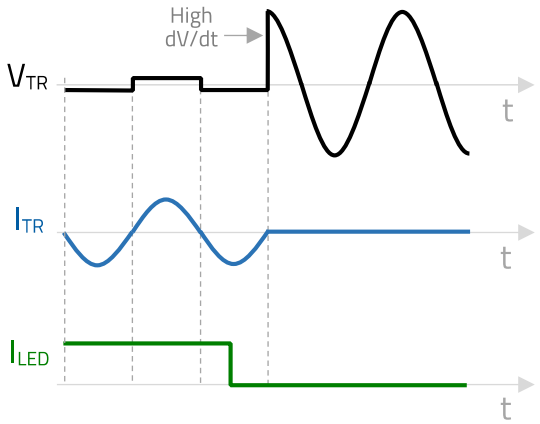

Figure 46*: TRIAC waveforms with a purely inductive load*

Among these, inductive loads like solenoid valves/switches and AC-motors are very common in industrial and domestic environments. In a purely inductive load, the current lags the voltage by 90°, meaning that as the load current approaches zero, the AC-line voltage is near its maximum (Figure 46). As a result, when the TRIAC starts to turn off as the load current falls below its holding level, the voltage across its terminals rises sharply. If the slew-rate exceeds the TRIAC's commutating dV/dt rating, the device may become spuriously triggered into conduction again. As mentioned in previous section 4.2.2 for a phototriac, the critical dV/dt level of a TRIAC is also dependent on the rate of change of current (dI/dt) through the device during the turn-off transition as well as on its operating temperature.

Regarding the opto-triac, be it RP/NZC or ZC type, it is already off when the TRIAC current falls to zero (see Figures 40 to 43), and this event appears as a static dV/dt across it. With ratings of 1 kV/µs for the WL-OCTR series, this is not an issue for the device, and the much lower commutating dV/dt and dI/dt ratings of the power TRIAC become the limiting factor.

Note that, although the commutating dV/dt can be reduced by adding an RC snubber across the TRIAC terminals, the dI/dt is just determined by the load characteristic, and it is more difficult to influence. Furthermore, there is a maximum dI/dt above which the TRIAC will be triggered into conduction no matter how low the dV/dt is, making the load uncontrollable. It is therefore essential to test this behavior at the worst-case condition of the application.

To illustrate the functioning of the circuit under inductive loading, a single-phase synchronous AC-motor, rated at 220-240 VAC, 50 Hz, 4.5 A and 550 W will be used. The measured inductance and DCR values of its running-coil are L ≈120 mH and R ≈ 6 Ω at 50 Hz, respectively (Figure 47).

The waveforms obtained in steady-state operation are shown in Figure 48, based on the reference schematic of previous Figure 35. Note how the current waveform is not a clean sinusoid as in the ideal case of Figure 46, as the load is not purely inductive.

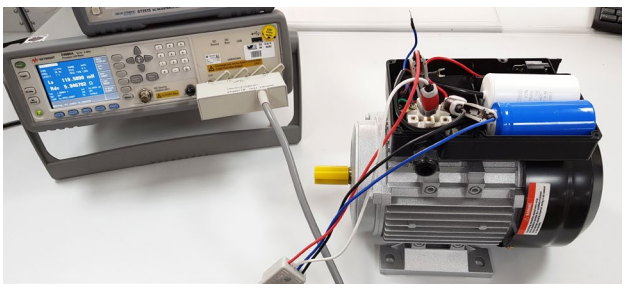

Figure 47*: L-R measurement of the AC-Motor used (running-coil)*

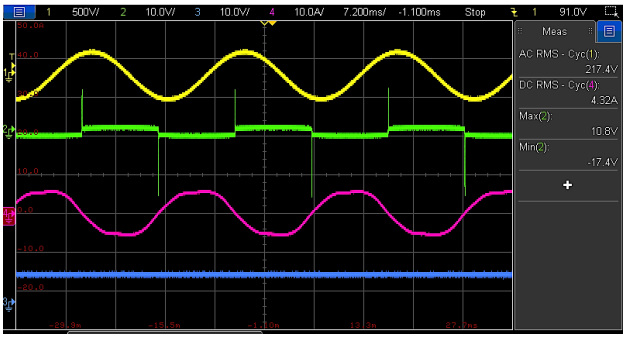

Figure 48: *Circuit waveforms for TRIAC driven by WL-OCTR opto-triac with 550 W AC-motor load (V_{AC} (), V_{TR} (), I_{load} (), V_{Rled} ()) (DANGER: HIGH VOLTAGE)*

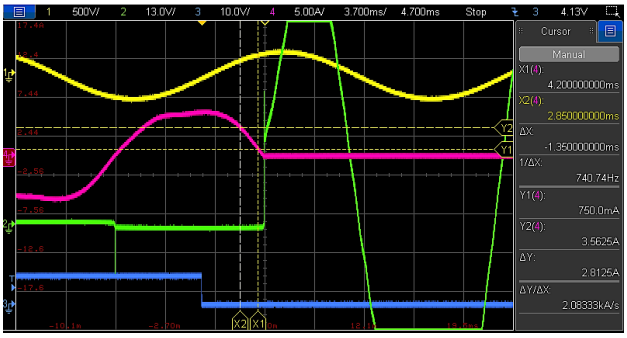

Figure 49: *Circuit waveforms with 550 W AC-motor load and zoomed-in dI/dt detail on turn-off (V_{AC} (), V_{TR} (), I_{load} (), V_{Rled} ()) (DANGER: HIGH VOLTAGE)*

Figure 50: *Circuit waveforms with 550 W AC-motor load and zoomed-in dV/dt detail on turn-off (V_{AC} (), V_{TR} (), I_{load} (), V_{Rled} ()) (DANGER: HIGH VOLTAGE)*

Figure 49 shows the turn-off transition with a measured dI/dt slightly exceeding 2 A/ms, while the sharp voltage spike occurring at commutation is measured and zoomed in Figure 50, reaching a dV/dt of around 8 V/µs.

A zero-cross WL-OCTR opto-triac and a properly rated TRIAC were used for the measurements, and the circuit operates normally. If spurious triggering were observed, a TRIAC optimized for inductive loads (a.k.a. 'snubberless' type) or an RC snubber connected across the device (R_S, C_S) (Figure 51) could be used.

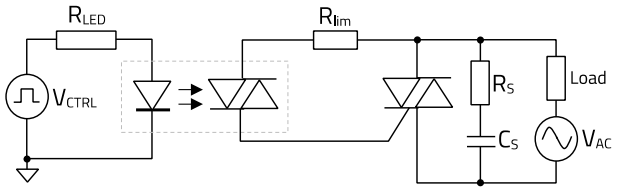

Figure 51: *Opto-triac as TRIAC driver with Rs-Cs snubber across TRIAC*

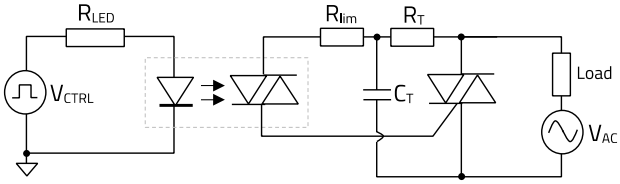

Figure 52: *Opto-triac as TRIAC driver with R_T-C_T network for phototriac dV/dt limiting and TRIAC snubber*

Note that, even when using a 'snubberless' TRIAC, adding an RC snubber is still recommended in applications where the load is unknown. The procedure to design such a snubber is well documented in references [4] and [5] and it will not be covered here.

In Figure 52, an alternative configuration with R_T and C_T is shown, very similar to the test circuit of previous Figure 24. Its main purpose is to limit the static dV/dt appearing across the phototriac, but as R_T and C_T are also parallel to the TRIAC, they also contribute to some dV/dt reduction across it.

This configuration helps to improve the robustness and reliability of systems operating in very noisy environments, preventing frequent spurious turn-on events of the phototriac and, in turn, of the TRIAC.

Considering V_{AC}=230 V and a maximum slew-rate limit of 500 V/µs (half of the WL-OCTR series rating), the required time constant of the R_T-C_T network would be:

$$\tau_{RC} > \frac{0.63 \cdot V_{AC} \cdot \sqrt{2}\ V}{500\ V/\mu s} \approx 400\ ns \qquad (E.10)$$

By setting C_T, the minimum R_T is calculated as:

$$R_T > \frac{\tau_{RC}}{C_T} \qquad (E.11)$$

Note that there are some trade-offs to consider in the selection of R_T and C_T, as in addition to static and commutating (turn-off) dV/dt and dI/dt ratings, TRIACs also have a maximum dI/dt rating during turn-on of the device which must not be exceeded in order to avoid hot-spots on the die during switching transitions, leading to premature degradation and lower reliability of the device.

With the TRIAC turned-off, the capacitor C_T charges to the AC-line voltage and, as soon as the TRIAC turns on with an RP device, it discharges through the phototriac and TRIAC via R_{lim} and R_T, respectively.

The resistor R_T needs to be high enough to limit the peak discharge current from C_T and subsequent dI/dt through the TRIAC to within its ratings. However, as R_T is in series with R_{lim}, a higher R_T will result in a higher AC-line voltage required for TRIAC triggering (E.12), increasing conducted EMI emissions.

$$V_{AC\_TRIG} \approx I_{GT} \cdot (R_{lim} + R_T + R_{load}) \quad \text{(E.12)}$$

Thus, the optimal pair of values for R_T and C_T will depend on the ratings of the TRIAC selected, and must be evaluated and adjusted in every case understanding these trade-offs.

06. EMC PERFORMANCE WITH RANDOM-PHASE AND ZERO-CROSS OPTO-TRIACS

In the previous sections, the circuit operation and characteristic waveforms with each type of opto-triac have been shown. Here, the conducted and radiated EMI emissions with the corresponding EMI filtering solution required for each opto-triac type will be studied.
For this, the same configuration as in Figure 37 (RP opto-triac) and Figure 42 (ZC opto-triac) with the 100 Ω resistive load shown in Figure 36 is used.

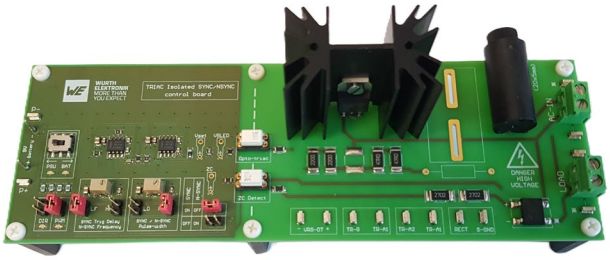

Figure 53*: Isolated AC power control board used for tests*

The experimentation board is shown in Figure 53 as a reference. On the left-side of the isolation barrier, a hardware-based, adjustable PWM generator powered by a 9V battery (placed under the board) is used to generate the control signal driving the LED of the WL-OCTR opto-triac. In addition, the PWM generator can be synchronized to the AC-line zero-crossing by means of an isolated zero-cross detection circuit based on a WL-OCPT phototransistor optocoupler, which is required to accurately control the phase triggering angle with the RP opto-triac. The high-voltage area is found on the right-side of the isolation barrier, where the TRIAC, fuse, snubber placeholder and zero-cross detection circuit are located.

On the board, a socket helps to swap the opto-triacs, and the PWM signal is adjusted in each case to provide a similar amount of power to the load at the worst-case condition for EMI. This will be around 50% of the full power, since for RP opto-triacs, a 90° triggering angle represents the worst-case for EMI, as it generates the highest dV/dt and dI/dt on the switching transitions.

6.1 Conducted Emissions

The conducted EMI emissions test is carried out in accordance with the test setup and emission limits of the EN61000-6-3 standard (i.e. residential, commercial and light-industrial environments). The results obtained without any EMI filter are shown in Figure 54 for both: RP (black) and ZC (red) opto-triacs.

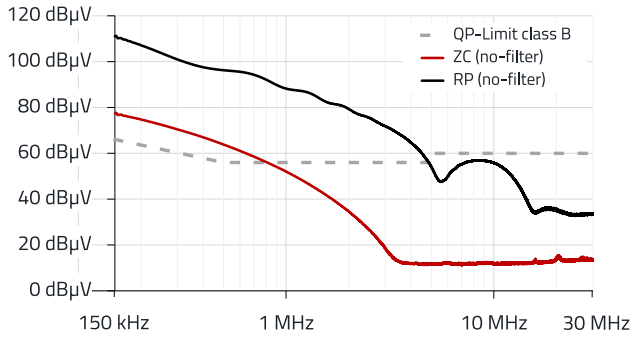

Figure 54: *Conducted emissions for RP and ZC opto-triac designs*

The emission limits are exceeded in both cases in the lower frequency range. Between 150 and 500 kHz, quasi-peak (QP) results with the random-phase device are 45 dB above the limit, but around 10-12 dB for the zero-cross one. Considering the entire conducted emissions frequency range, an improvement of 20 to 50 dB is obtained with the ZC opto-triac for the same load and output power. For this device, conducted emissions fall below the limit above 1 MHz, whereas for the RP opto-triac, the emissions do not fall to comfortably low levels until above 10 MHz.

6.2 Radiated Emissions

For the radiated emissions test, CISPR32 class B limits are also considered, and the results are shown in Figure 55. The emissions are negligible in both cases, staying more than 20 dB below the limit over the entire frequency range of the test.

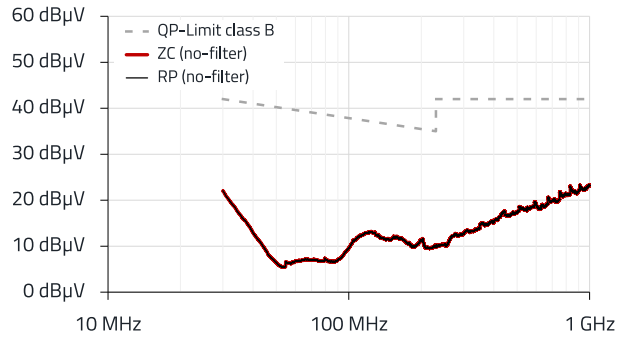

Figure 55: *Radiated emissions for RP and ZC opto-triac designs*

6.3 EMC Solution – Zero-cross opto-triac design

The design with a ZC opto-triac needs a reduction of the conducted noise level of up to 20 dB between 150 kHz and 1 MHz to pass the test with comfortable margins.

Before designing the EMI filter, the dominant type of noise should be found. For this, measurement of the differential-mode (DM) (green) and common-mode (CM) (yellow) currents into the LISN are shown in Figure 56, showing how the noise is predominantly DM, with negligible CM contribution.

As shown in previous Figure 44, the TRIAC does not turn on instantaneously at the zero crossing of the AC-line voltage, but depending on the device, load and gate resistor used, it could turn on at an AC-line voltage even above 50 V. Note how, immediately after zero-crossing, the load current follows the slope of the 50-60 Hz sinusoid, with its level limited by the 100 Ω of the load and R_{lim} (around 500 Ω in this example). However, as soon as the TRIAC turns on, the impedance across its terminals reduces and the load current is only limited by the 100 Ω load. The result is a load current step resulting in higher dI/dt, in addition to the high dV/dt appearing across the TRIAC at turn-on as it stops blocking the AC-line voltage (Figure 57).

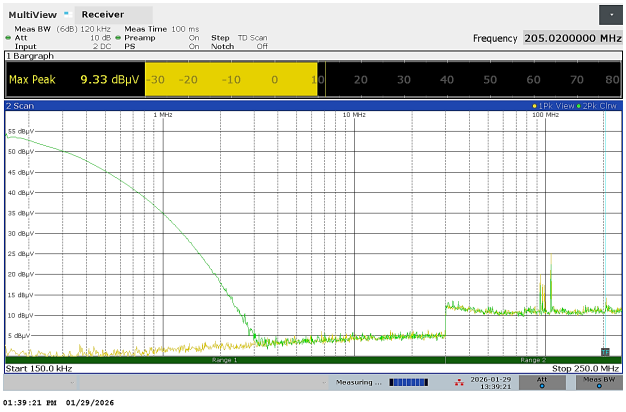

Figure 56: *Differential-mode (I) and Common-mode (I) noise currents for ZC opto-triac design without filter (1 dBµV ≡ 1 dBµA)*

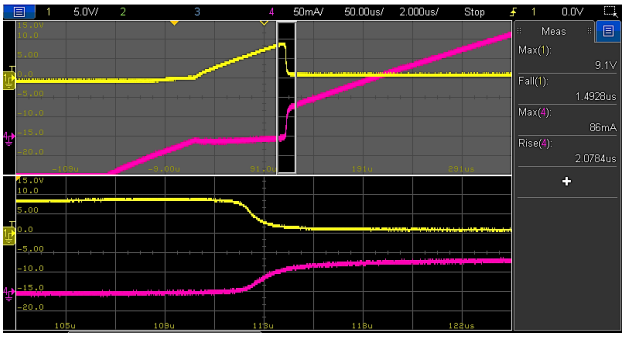

Figure 57: *dV/dt and dI/dt on TRIAC turn-on with ZC opto-triac*

Without any input capacitor, the DC-blocking capacitors of the LISN (100 nF or 250 nF, depending on type) need to source this higher dI/dt current, as the LISN inductors (L_{LISN}) prevent the AC-source from doing this (Figure 58). For DM noise, these capacitors are in series with the VNA channels of 50 Ω (L and N measurement sides), leading to the failed EMC test.

Node 'C' in Figure 58 exhibits high dV/dt with reference to all other nodes and LISN-GND, and it couples CM currents to the LISN via the parasitic/distributed capacitance to the GND plane of the chamber wall and floor. However, its effect is negligible in this case, and requires no filtering considerations.

To pass the EMC test, the impedance across the LISN nodes A and B in Figure 58 needs to be reduced.

In other words, the LISN capacitors need to be bypassed by a lower-impedance capacitor which will source the high dI/dt currents instead.

Thanks to the moderate amount of attenuation needed, a single X-type film capacitor will suffice for this, and the WCAP-FTX2 890324025045 (680 nF, 275 VAC) is selected. With this 'Filter-1', the EMC test is passed with a minimum of 20 dB margin to the limit over the full frequency range of the conducted emissions test (Figure 59). For safety, a properly rated, so-called 'bleed' resistor needs to be connected in parallel to this capacitor to discharge it when power is removed.

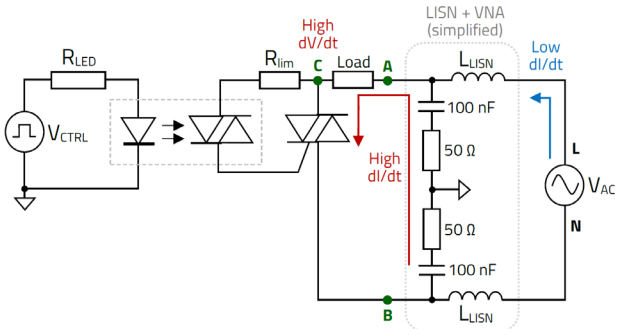

Figure 58: *Circuit with LISN connected and DM dI/dt currents*

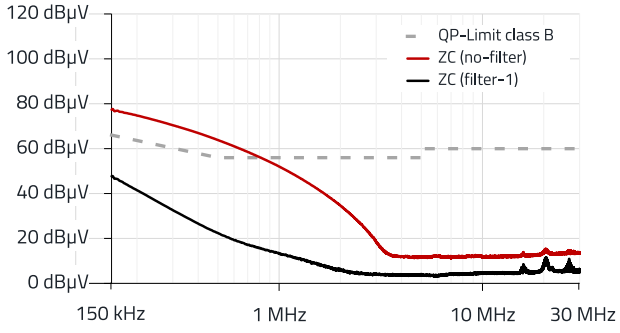

Figure 59: *Conducted EMI results for ZC opto-triac design with and without Filter-1 (WCAP-FTX2 890324025045)*

6.4 EMC Solution – Random-phase opto-triac design

Based on the results of Figure 54, to pass the conducted EMI test (including some headroom) with a random-phase opto-triac and cycle-by-cycle phase angle control at 90° in this example design, over 60 dB noise attenuation is required below 1 MHz. Furthermore, between 1 MHz and 10 MHz, attenuation levels between 45 dB and 20 dB are necessary.

As with the ZC design, the DM and CM noise currents into the LISN without filter are measured first (Figure 60). In this case, the DM noise also dominates, but it has a much higher amplitude compared to the ZC design, due to the larger load current step: from a few tens of mA to the maximum peak of around 3 A (Figure 61). Furthermore, there is also a non-negligible CM noise contribution, as the voltage step on turn-on is also of much higher amplitude (over 300 V) than in the ZC case, as Figure 61 shows.

However, the DM noise still dominates, and a DM PI-filter will be designed as a first approach, referred to as 'Filter-2' from now on (Figure 62). This is implemented with X-capacitors C_{f1} = WCAP-FTX2 890324025045 (680 nF, 275 VAC), C_{f2} = WCAP-FTX2 890324026027 (1 µF, 275 V) as well as the line choke L_f = WE-FI 7447013 (90 µH, 4.6 A). A discharge/bleed resistor (R_b) is also added for safety, as mentioned before.

Figure 60: *Differential-mode (I) and Common-mode (I) noise currents for RP opto-triac circuit without filter*

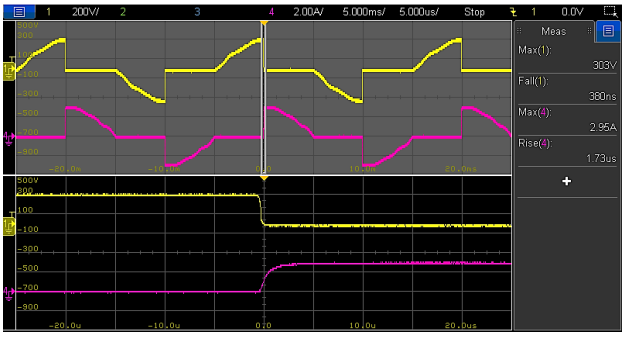

Figure 61: *dV/dt and dI/dt on TRIAC turn-on with RP opto-triac*

With this EMI filter, the EMC test is passed with a minimum margin of around 4 dB to the limit between 400 kHz and 1 MHz (Figure 63).

As Figure 64 shows, the DM noise has been practically eliminated above 300 kHz, leaving only the unfiltered CM noise. Finally, Figure 65 shows the boards for Filter-1 (ZC solution) and Filter-2 (RP solution). Despite being bulkier, the RP design with Filter-2 achieved much lower headroom to the EMI limits compared to the ZC design with Filter-1.

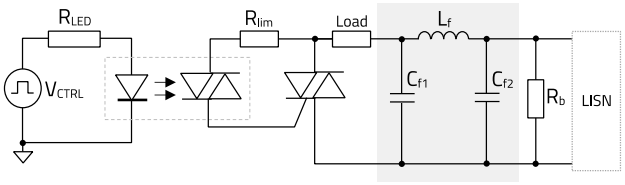

Figure 62*: Schematic with Filter-2 for RP opto-triac design*

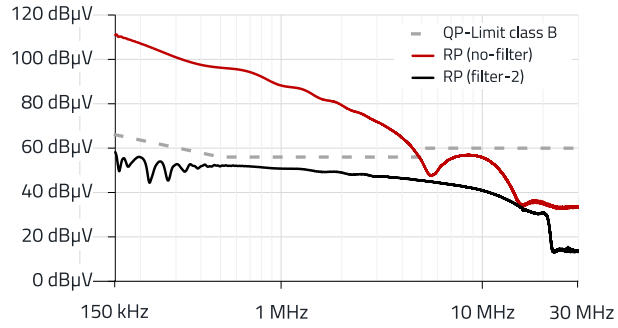

Figure 63*: Conducted EMI results for RP design with and without Filter-2*

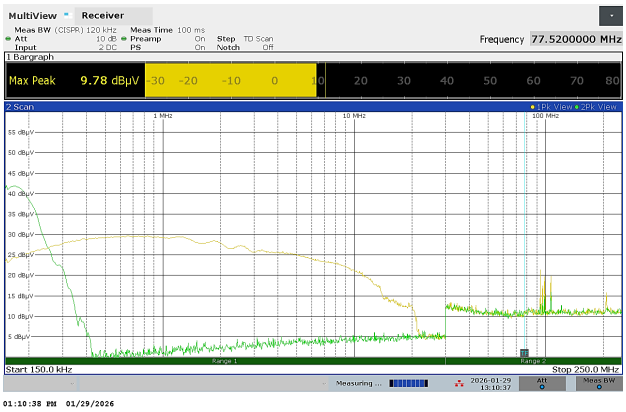

Figure 64*: Differential-mode (I) and Common-mode (I) noise currents for RP design with Filter-2*

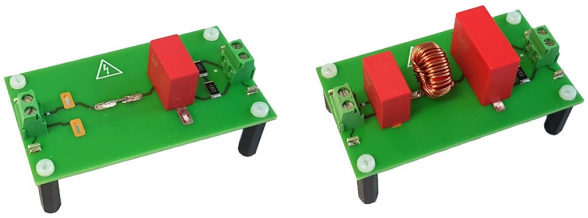

Figure 65*: Images of EMI Filter-1 (left) and EMI Filter-2 (right)*

6.5 Additional considerations

Here, the two design extremes regarding EMI performance were compared: an ON-OFF approach with a ZC opto-triac and a cycle-by-cycle phase angle control/modulation at 90° with a RP opto-triac, both delivering the same amount of power to the load. This showed how an ON-OFF technique with a ZC device should be used so long as the load type and time constants involved allow.

Note that the same type of ON-OFF control could also be implemented with an RP device for low EMI, but this would require an external zero-cross detection circuit to synchronize the triggering angle to the start of every half-cycle of the AC-line voltage, all of which is already implemented within the ZC opto-triac device. Furthermore, the EMI performance of the ZC design could be improved even further by using a TRIAC with a lower gate triggering current (a.k.a. 'logic' or 'sensitive' TRIAC type), unlike the robust 'snubberless' TRIAC used in this case. However, lower triggering current comes at the expense of higher sensitivity to spurious turn-on due to commutating dV/dt and dI/dt, although when controlling a mostly-resistive load as in this case, that will rarely become an issue.

For more information, reference [6] provides guidance on the design of a single-phase line filter, whereas reference [7] provides further insights on EMI performance and EFT (Electrical Fast Transient) tests of a similar TRIAC application.

07. SPICE SIMULATION WITH WL-OCTR OPTO-TRIACS

7.1 WL-OCTR SPICE Models

Würth Elektronik provides SPICE models for its random-phase and zero-cross WL-OCTR opto-triacs in LTspice, which can be freely downloaded here. Different models are provided not only based on the opto-triac type, but also on the LED triggering current (5 mA, 10 mA, 15 mA) as well as blocking voltage rating (250 V, 400 V, 600 V) of the respective device (see Table 1). In LTspice, after right-clicking on the symbol, the specific device can be selected from the drop-down menu as shown in Figure 66.

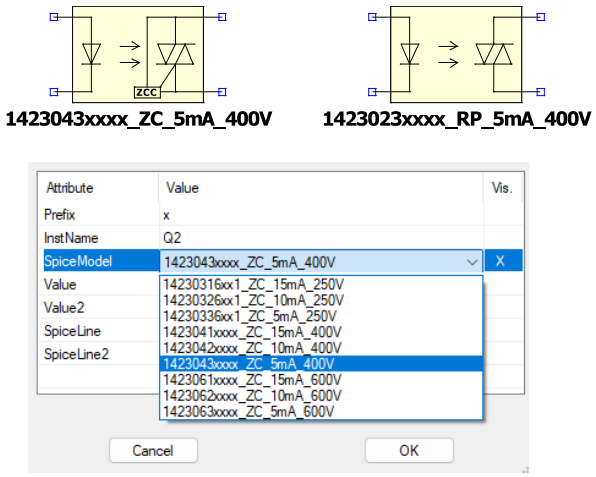

Figure 66: *WL-OCTR opto-triac model selection in LTspice*

7.2 Special considerations of WL-OCTR Models

The WL-OCTR SPICE simulation models provide an approximation of the real behavior of the device, but not all characteristics are modelled, nor are the influences of some factors, such as tolerances and temperature.

The relationship between LED triggering current amplitude and pulse duration required to trigger the device into conduction is modelled as shown in previous Figure 16. This means that the nominal LED triggering currents of 5 mA, 10 mA and 15 mA are only valid when applied for longer than around 100 µs, while a higher LED current will be required for shorter pulse-widths.

Regarding the blocking voltage, if the instantaneous voltage across the device exceeds its corresponding rated blocking voltage by around 10-20%, the opto-triac is modelled to spuriously turn on, even in the absence of LED current. This behavior is illustrated in the simulation results of Figure 68, with reference to the simulation schematic of Figure 67.

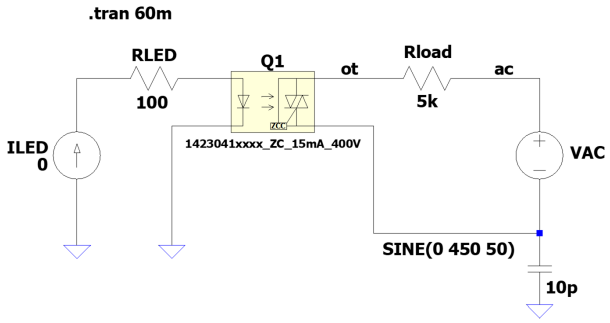

Figure 67: *LTspice simulation schematic for 400 V WL-OCTR opto-triac with applied overvoltage*

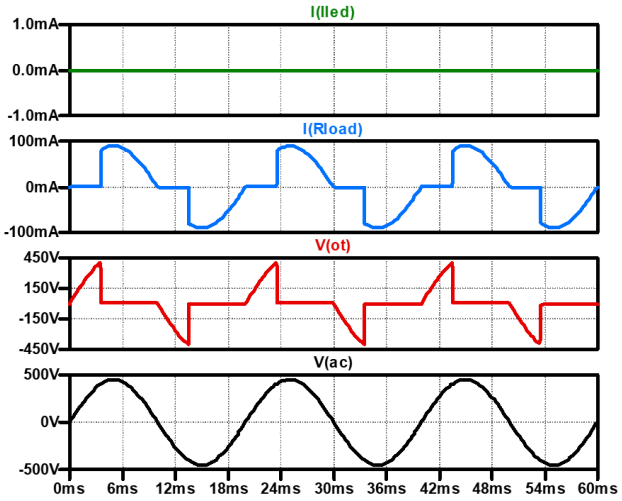

Figure 68: *LTspice simulation results for 400 V WL-OCTR opto-triac with applied overvoltage*

A forward conduction characteristic of the phototriac similar to that shown in Figure 32 is also modelled, in addition to characteristics like the LED I-V and phototriac leakage current. Note that the static dV/dt spurious turn-on as well as commutating dV/dt and dI/dt behaviors are not modelled.

7.3 LTspice simulation examples

Some example simulation results in LTspice are shown here with the WL-OCTR SPICE models in their target application as TRIAC drivers. The simplified simulation schematic and example results using a random-phase opto-triac are shown in Figure 69 and Figure 70, respectively, whereas Figure 71 and Figure 72 show the results obtained with a zero-cross device.

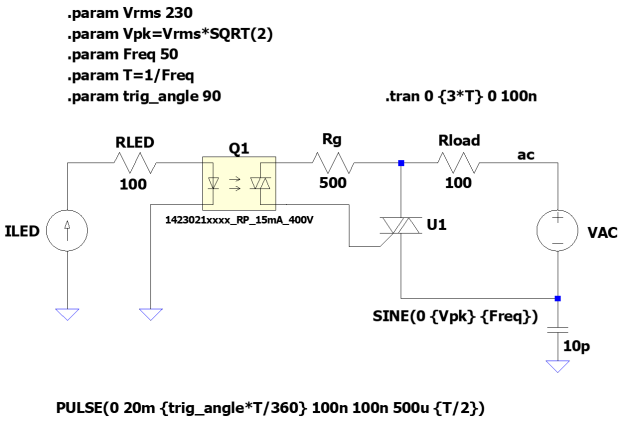

Figure 69: *LTspice simulation schematic with WL-OCTR random-phase opto-triac and TRIAC*

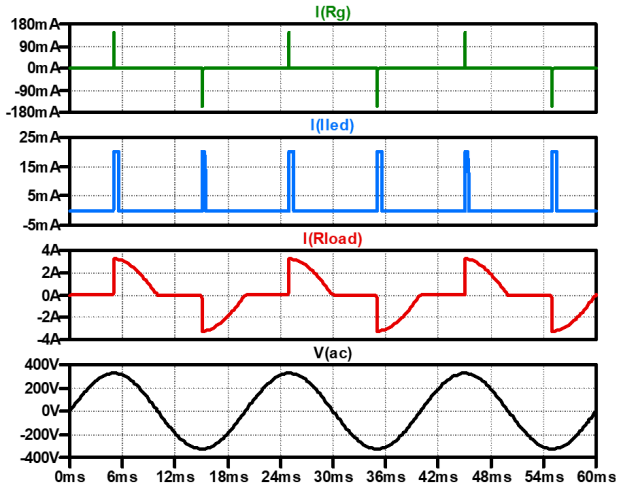

Figure 70: *LTspice simulation results with WL-OCTR random-phase opto-triac and TRIAC with a 90° triggering angle*

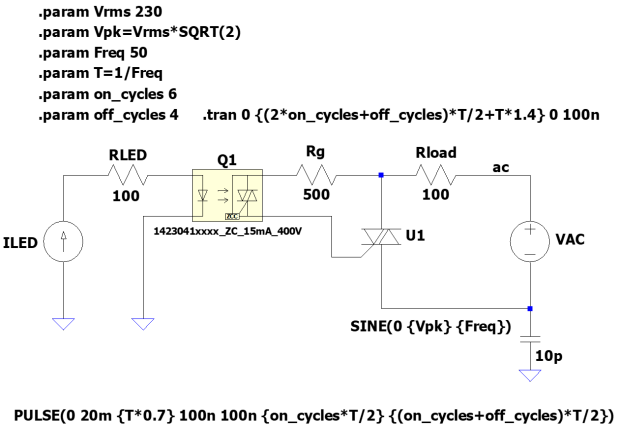

Figure 71: *LTspice simulation schematic with WL-OCTR zero-cross opto-triac and TRIAC*

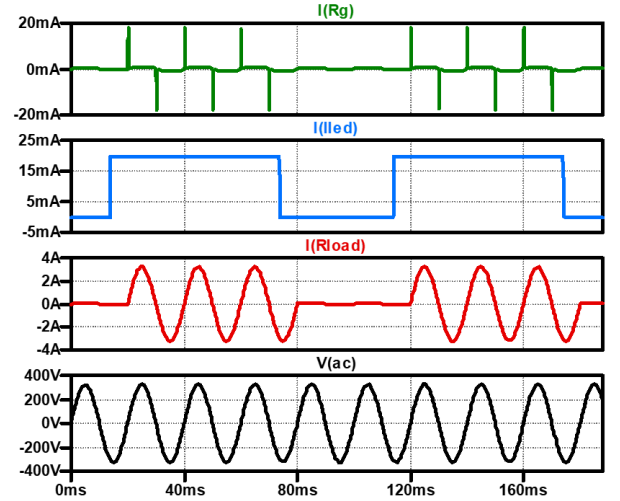

Figure 72: *LTspice simulation results with WL-OCTR zero-cross opto-triac and TRIAC with 6 half-cycles ON and 4 half-cycles OFF*

08. WÜRTH ELEKTRONIK OPTO-TRIAC PORTFOLIO

The WL-OCTR opto-triac series from Würth Elektronik are offered in various packages and mounting types. An overview of these is provided in Figure 73. In Table 1, zero-cross and random-phase opto-triacs are categorized based on their LED triggering current (I_F), maximum repetitive blocking voltage (V_{DRM}), and the package type(s) offered in each case.

(*) For special requests not covered in the standard catalog, please contact your WE sales representative.

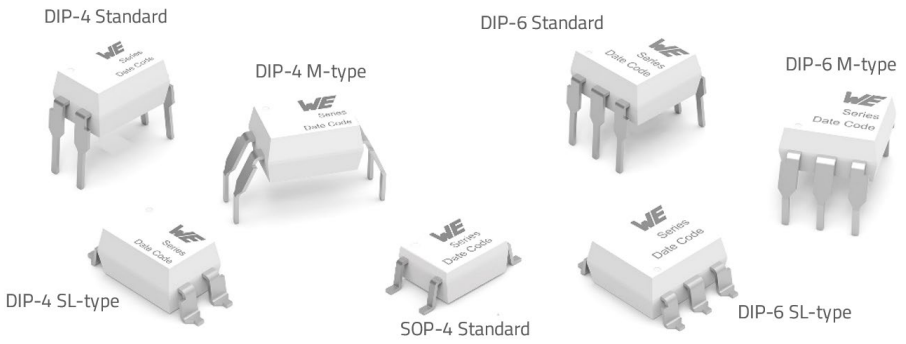

Figure 73: *WL-OCTR opto-triac series – Detail of package types (DIP-4, SOP-4, DIP-6) and subtypes (Standard, M, SL)*

Type	I_F (mA)	V_{DRM} (V)	Package
Zero-cross (ZC)	5	250	DIP-6
		400	DIP-4, SOP-4, DIP-6
		600	DIP-4, SOP-4, DIP-6
	10	250	DIP-6
		400	DIP-4, SOP-4, DIP-6
		600	DIP-4, SOP-4, DIP-6
	15	250	DIP-6
		400	DIP-4, SOP-4, DIP-6
		600	DIP-4, SOP-4, DIP-6

Type	I_F (mA)	V_{DRM} (V)	Package
Random-phase (RP/NZC)	5	250	SOP-4, DIP-6
		400	DIP-4, SOP-4, DIP-6
		600	DIP-4, SOP-4, DIP-6
	10	250	SOP-4, DIP-6
		400	DIP-4, SOP-4, DIP-6
		600	DIP-4, SOP-4, DIP-6
	15	250	DIP-6
		400	DIP-4, SOP-4, DIP-6
		600	DIP-4, SOP-4, DIP-6

Table 1: Zero-cross and Random-phase WL-OCTR opto-triac series overview

09. REFERENCES

[1] *ANO006: Lifetime of Optocouplers,* Application note, Würth Elektronik

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[3] *BTA16-600BWRG* Datasheet, ST Microelectronics

[4] AN437: *RC snubber circuit design for triacs*, Application note, ST Microelectronics

[5] AN1048/D: *RC snubber networks for thyristor power control and transient suppression*, Application note, Onsemi

[6] *ANP015: Line filter – The last barrier in the switch mode power supply,* Application note, Würth Elektronik

[7] *AN5114: Controlling a TRIAC with a phototriac,* Application note, ST Microelectronics

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