

APPLICATION NOTE

ANP085 | Single Pair Ethernet for Industrial Applications



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1. EVOLUTION OF ETHERNET - FROM 4 PAIRS TO 1 SINGLE PAIR

Starting in the early 1980s as a communication protocol for computer networks, Ethernet and its associated standards has become the most used protocol in industry communication. Copper cables with 2-pairs for Fast Ethernet and 4-pairs cables for Gigabit Ethernet are the core elements in enterprise and industrial networks. With the new Single Pair Ethernet (SPE) technology driven from the car industry, many new use cases are possible to replace analog sensor applications or industrial bus systems.



Figure 1: IP20 version of the SPE connector acc. to IEC 63171-6.

In 2019 about 59% of all industrial communication protocols were based on LAN. Still, a high percentage of field bus systems like Profibus or CC-Link (Control and Communication) are in use as well. Many sensors or actuators inside production facilities don't have a requirement for a high data rate. But as the distance between these devices and the field switches often is more than 200 m, Ethernet with a maximum cable length of 100 m comes to its limits.

Besides cable length, the (cable)weight, mechanical connector stability and PCB size reduction were the drivers to create a new standard beyond the RJ45 based multi-pair Ethernet. Single Pair Ethernet (SPE) was developed to fulfil these market requirements and enable borderless IP based communication from the cloud to any sensor or actuator.

This Application Note describes the components needed for Single Pair Ethernet from the cable to the PHY chip. The focus

will be set for the right EMI filter design for 10BASE-T1L and 100BASE-T1 and to fulfil communication safety requirements according to IEC 62368-1. This will be demonstrated in a PCB to characterize the effectiveness of the components.

2. SPE - HARDWARE AND COMPONENTS

The new SPE physical layer needs new components like cable connectors, magnetics, semiconductors and other devices. The international standards organisations and the allied companies for SPE have invested a lot of time and money in the last years to make all these parts available. The main standards are already publicly available. Also first components are ready to use and in this way the design of new devices with SPE connectivity is possible.

The SPE electrical requirements are specified in the following IEEE standards:

- IEEE 802.3cg (10BASE-T1) with bandwidth from 0.1 to 20 MHz and reach up to 1000 m.
- IEEE 802.3bw (100BASE-T1) with bandwidth 0.3 to 66 MHz and reach up to 40 m.
- IEEE 802.3bp, (1000BASE-T1) with bandwidth 1 to 600 MHz and reach up to 40 m.

2.1 Cable

Based on the needed transmission speed and link length, two basic types of SPE cables are available and standardized. For 10 Mbit/s networks of up to 1000 m cable length, the following standards specify the cable design:

- IEC 61156-13 - SPE data cable up to 20 MHz bandwidth for fixed installation,
- IEC 61156-14 - SPE data cable up to 20 MHz bandwidth for flexible installation.

For 1 Gbit/s networks up to 40 m these standards are available:

- IEC 61156-11 - SPE data cable up to 600 MHz bandwidth for fixed installation,
- IEC 61156-12 - SPE data cable up to 600 MHz bandwidth for flexible installation.

APPLICATION NOTE

ANP085 | Single Pair Ethernet for Industrial Applications

Compared to traditional Category 5e industrial Ethernet cables with four pairs for 1 GBit/s transmission, there is a significant reduction in space and weight of the cable. Please refer to Table 1 for more details.

Dimension	Industrial Ethernet Cat 5e (4 x 2 x 24 AWG)	SPE (1 x 2 x 22 AWG)	Reduction
Outer diameter	7.8 mm	5.8 mm	26%
Weight	79 kg/km	42 kg/km	47%

Table 1: Dimension comparison SPE cable.

All these cables are shielded to provide the needed crosstalk resistance for the 40 m 1GBASE-T1 and the 1000 m 10BASE-T1L as demonstrated in Figure 2.

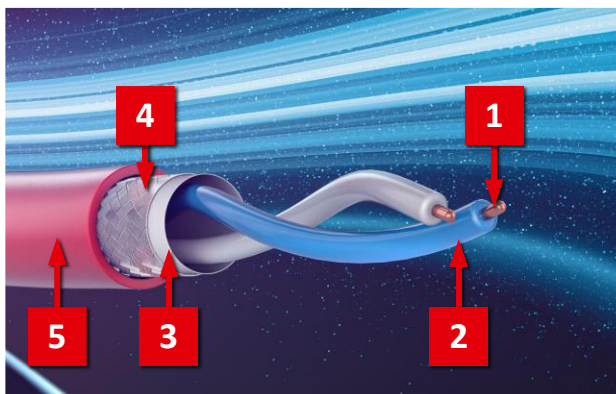


Figure 2: Design for a typical SPE cable (1-copper wire, 2-wire isolation, 3-shielding foil, 4-shielding braid, 5-cable jacket).

Depending on the use case, different cable jacket materials are possible. The copper cross-section of the cable must be selected according to the link length needed and the Power over Data Line (PoDL) requirement. No. 26 AWG and 22 AWG wires are typically taken for link lengths of up to 20 m and 40 m, respectively. For longer link lengths up to 1.000 m, 16 AWG or 18 AWG cables must be used.

To realize the 1 Gbit/s transmission rate over a single pair, the standards define strict requirements for the electrical properties of an SPE cable.

Those include the s-parameters insertion loss (IL), return loss (RL) and alien crosstalk (AXT) over a frequency range up to 600 MHz.

Insertion loss describes the logarithmic ratio between power fed into the cable and the power transmitted through the line. The high demands on IL are necessary to realize the long transmission distances of SPE.

Return loss and the impedance of the cable are important for the reflection behaviour of the overall system. Reflections are interferences on the line. Those interferences could disturb transmitters and receivers. To minimize the reflections, the overall SPE system should have the same characteristic impedance of 100 Ω and low RL values.

For cables with more than one pair, crosstalk describes the signals transmitted between the pairs over inductive and capacitive coupling. This crosstalk disturbs the actual transmission signals on the line. SPE has the advantage that there could be no crosstalk from other pairs, but SPE has to deal with alien crosstalk. ANEXT is crosstalk from other cables in the near environment. To protect the transmission from disturbing ANEXT industrial SPE cables should be well shielded with a combined foil and braid shield.

The foil shield provides a high shielding effectiveness against high frequency electromagnetic fields. The braided shield is used for mechanical stabilization and shielding of low frequency electromagnetic fields. The effect of a braid depends on the thickness of individual wires and on the degree of coverage. SPE cables for industrial environments should provide a coverage of a minimum 85%. The braiding of a cable also mainly defines the values for the transfer impedance of a cable shielding.

The shielding effect of a cable works in both directions, which means that the shielding attenuation reduces both the radiation of disturbances of the cable signal as well as disturbances of other devices acting on the cable from outside.

2.2 Connector

For SPE completely new types of connectors are needed. These connectors are smaller compared to the typical RJ45 and offer the same robustness as the often used industrial style M12 D- and X-coded connectors. This new SPE interface is defined in the IEC 63171-6 standard and includes different M8/M12 versions for very harsh industrial applications and an IP20 interface for in cabinet use cases (see Figure 3). All these connector types are based on the same terminal inserts and use a robust pin and socket contact system. This modular design concept with identical terminal inserts in all versions allow the mating of IP20 plugs to IP65/67 jacks for testing or set up.

This SPE connector series is specified for 60 V_{DC}/4 A @ 60°C and fulfills the requirements for all Power over Data Line (PoDL) classes.

APPLICATION NOTE

ANP085 | Single Pair Ethernet for Industrial Applications

For harsh industrial environments with a heavy EMC disturbance, the connector has a 360° shielding shell to provide the shielding connection from the cable shielding to the PCB with four shielding pins. These Through Hole Reflow (THR) solder pins also offer a robust mechanical connection between the jacks and the PCB (Figure 3).



Figure 3: Different recommended SPE connector acc. to IEC 63171-6.

The connector mating face design is symmetrical and the contacts are arranged in parallel with the identical contact length. The RF compliant connector technology enables signal transmissions of up to 1 Gbit/s for 1000BASE T1 (Figure 4).

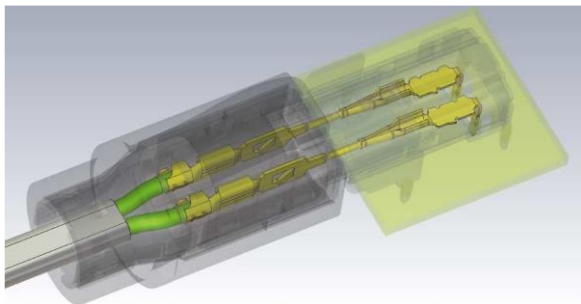


Figure 4: Identical length of the signal paths to avoid runtime differences of the signals.

3. FILTER TOPOLOGIES

The MDI (Medium Dependent Interface) forms the connection between cable and the physical medium, the PHY chip, which generates bits from data signals and passes them on for further processing.

The passive components of the MDI have various tasks, such as correct forwarding of data signals, signal interference suppression, electrical isolation or transport of electrical energy up to 60 W in the case of Power over Data Line (PoDL).

To ensure error-free data communication, limits for return loss and mode conversion loss have been defined in various IEEE 802.3 standards.

Figure 5 illustrates the MDI limits for 10BASE-T1 according to IEEE 802.3cg and 100BASE-T1 according to IEEE 802.3bw.

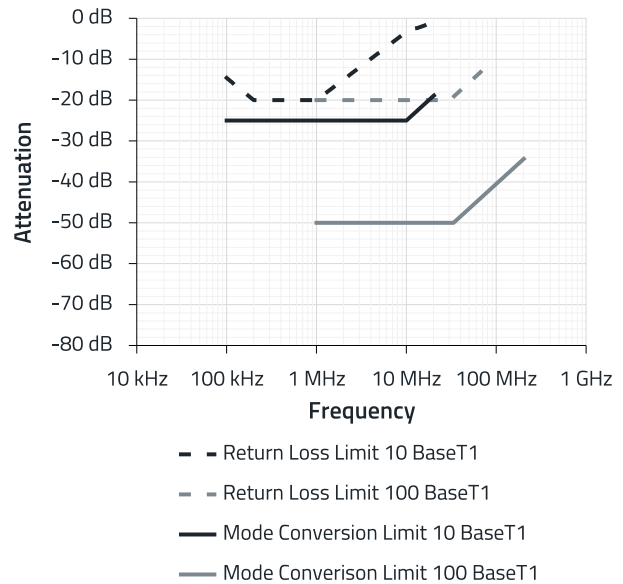


Figure 5: Limits of return loss and mode conversion for the for MDI 10BASE-T1 (black) and 100BASE-T1 (grey).

3.1 State of the art

Coming from the automotive sector, there are already finished circuit diagrams for Single Pair Ethernet for 100BASE-T1 (see Figure 6) with a common mode choke, two capacitors connected in series and a termination network for CM interference from the cable.

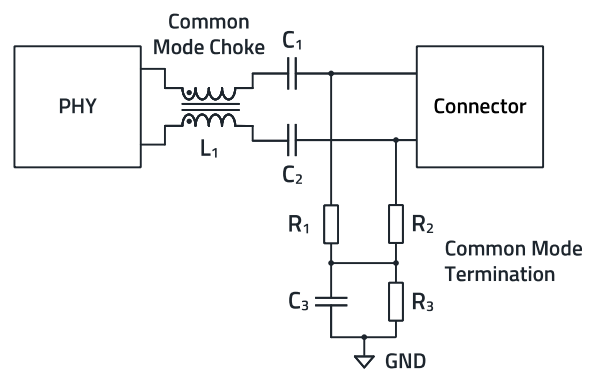


Figure 6: Single Pair Ethernet schematic for automotive Ethernet 100BASE-T1.

The common mode choke not only provides filtering of interfering common mode signals but also helps to improve mode conversion loss and return loss in certain frequency ranges.

APPLICATION NOTE

ANP085 | Single Pair Ethernet for Industrial Applications

Due to the lower cut-off frequency at 100BASE-T1 of 1 MHz, the impedance of the choke must be high in low frequencies and, if possible, also cover higher frequencies up to 200 MHz. The number of windings and core size is correspondingly larger.

The matching network to ground (GND) typically consists of three resistors and one capacitor. The two 1 kΩ - resistors (R_1 , R_2 in Figure 6) terminate the pair of wires balanced to ground and thus reduce interfering common mode signals. The 100 nF capacitor (C_3) with the 100 kΩ discharge resistor (R_3) ensures decoupling of direct currents.

The coupling capacitors have capacitances of typically 100 nF and come with 50 V isolation voltage. They are comparatively small and cost-effective, which is why they are used in automotive applications with low-voltage environments and a maximum cable length of 15 m.

3.2 Isolation requirements

Outside the automobile, the IEEE 802.3 standard for signaling systems stipulates the insulation requirement according to IEC 62368-1, which corresponds to 1500 V_{AC} for 60 seconds. A DC voltage of 2250 V_{DC} for 60 seconds or specific test voltage pulses are also permitted. These high insulation voltages cannot be maintained by the 50 V capacitors, so alternative solutions must be sought. The following section therefore describes a solution using a transformer. Detailed measurements and a comparison with capacitors with 2000 V insulation voltage follow in the section 3.7

Performance Comparison SPE automotive vs. SPE industrial Solutions.

At 1 – 66 MHz, the frequency range for SPE 100BASE-T1 is in the Gigabit Multipair Ethernet (1 – 62.5 MHz) range. It is therefore obvious to design a circuit for SPE that is based on the circuit diagram of Gigabit Ethernet, see Figure 7.

The central element of the circuit is a signal transformer, which provides the galvanic isolation and ideally does not influence the data signals. The transformer is terminated at its center pins with capacitors to GND. A common mode choke is used for common mode interference suppression. To ensure that the Phy is also protected against ESD pulses, a **TVS diode** array is placed between the transformer and the PHY. Primary transient protection should also be provided between the connector and the transformer. However, in order not to cause a short circuit between signal pins and GND during hipot tests, this protection must be disconnected from GND during the test. Figure 7 illustrates the setup without primary protection once again.

The following section describes the individual components of the circuit in more detail.

3.3 Galvanic isolation with a transformer

For SPE a signal transmitter of the **WE-STST** series is selected. Its compact design compared to conventionally manufactured LAN transformers, together with high inductance of 350 μH, offers good signal characteristics even at lower frequencies.

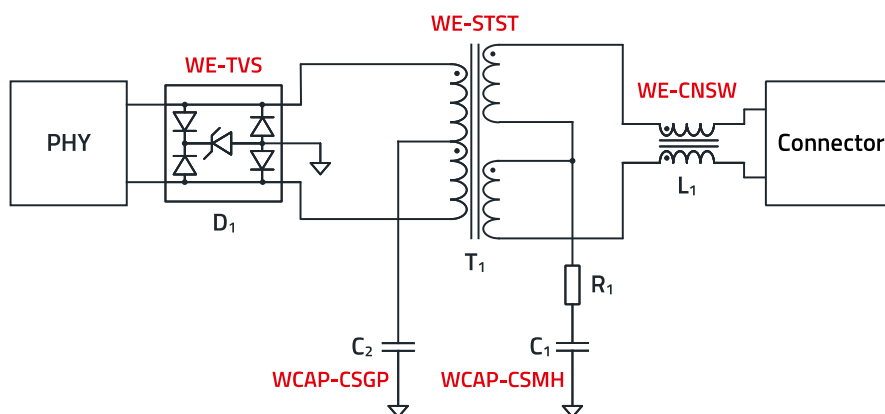


Figure 7: SPE schematic with a transformer solution.

APPLICATION NOTE

ANP085 | Single Pair Ethernet for Industrial Applications

In addition, it is SMT mountable and is manufactured 100% automatically (Figure 8).

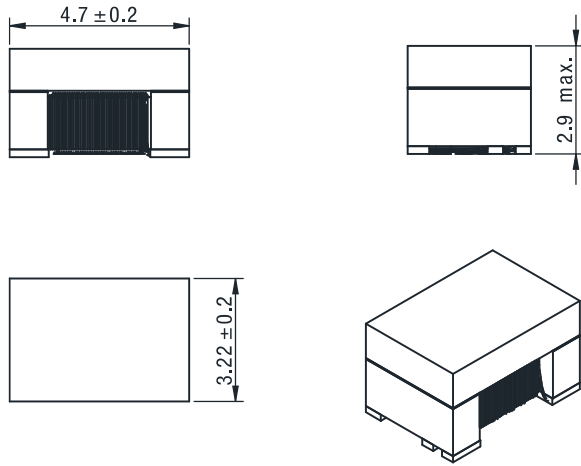


Figure 8: WE-STST shapes and dimensions.

The transformer consists of a MnZn core with bifilar windings for both primary and secondary on top of each other for signal coupling. Insulation is provided by an enamel coating of the wires, both on the primary and secondary side. Due to the direct coupling and the transmission ratio of 1:1, differential signals are transmitted with very little attenuation; DC signals are blocked by the galvanic isolation. For Single Pair Ethernet, the signal transmitter must transmit data in the frequency range of 0.1 MHz to 20 MHz for 10BASE-T1 and 1 MHz – 66 MHz for 100BASE-T1. As later measurements show, the same transformer can be used for 10BASE-T1 and 100BASE-T1. In addition to the Return Loss (RL), another parameter for signal integrity is the Insertion Loss (IL). Over the complete signal frequency range, the IL should not exceed -3 dB. IL and RL curves for the WE-STST series can be seen in Figure 9.

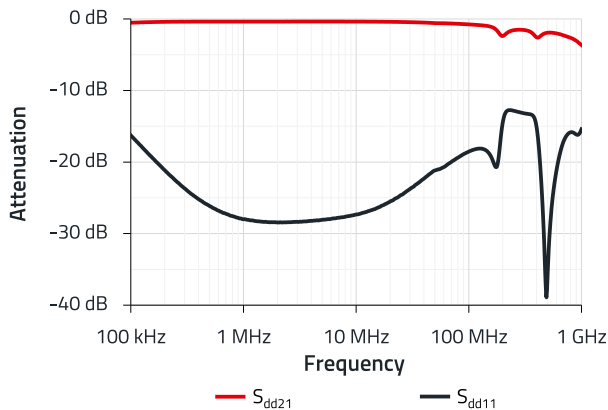


Figure 9: Insertion Loss (red) and Return Loss (black).

More information about the WE STST can be found here:

[SNO16b](#).

3.4 Transformer GND termination

The common mode rejection ratio (CMRR) is a parameter that indicates how well common mode signals are attenuated. Even though IEEE 802.3cg or IEEE 802.3bw do not specify any requirements in this respect, a high CMRR over the entire frequency range is important, as excessive common mode signals are the main cause of data failures. The CMRR of the transformer depends heavily on the winding capacitance between the primary and secondary wire layers of the transformer. The CMRR values can significantly be improved by connecting the transformer center tap to ground.

In this way, the center tap GND connection offers an excellent low impedance path for common mode signals (see Figure 10).

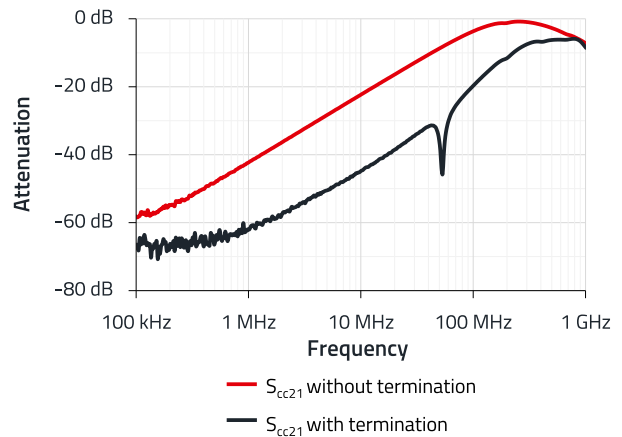


Figure 10: Common Mode Rejection of WE-STST with (black) and without (red) GND connection of the transformer.

On the cable side, the GND connection consists of a termination resistor connected via a 1 nF capacitor. The resistor terminates the SPE signal path with 100 Ω, while the capacitor provides a low impedance path to GND for AC signals and also ensures galvanic isolation of 2 kV.

The capacitor C_2 at the center tap of the transformer shown in Figure 7 has two tasks. On one hand, it prevents a short circuit of the offset voltage to GND, which the PHY generates and over which the data signal is superimposed. On the other hand, it provides a RF connection to ground, so that common-mode interference is dissipated. The signals are balanced around 0 V via the transformer, as it only transmits the AC voltage component of the signal.

In addition to the split primary and secondary windings with center tap pins, the common mode behavior also depends on the parasitic effects between the windings, as explained above. By placing windings on top of each other and thus ensuring close inductive coupling between them, an attempt

APPLICATION NOTE

ANP085 | Single Pair Ethernet for Industrial Applications

is made to keep the so-called leakage inductance as low as possible. However, this increases the parasitic capacity between the windings. The parasitic effects can be reduced to a minimum by selecting the insulation material, the arrangement of the windings and other constructional measures, so that the transformer can be used up to the frequency range of over 60 MHz.

3.5 Noise suppression with common mode choke

The target of the common mode choke is to balance signal, i.e. to symmetrize the signal in such a way, that no common mode energy is disturbing the information transmitted (the differential mode portion of the signal). To reach this target, the common mode components of the signal should be removed without affecting the integrity of the differential signal. That is why using a common-mode choke with large common mode impedance and low differential-mode impedance within the signal frequency range is essential.

Based on the graph results and knowing the limits to keep for each of the Ethernet protocols, part number [744232222](#) for 100BASE T1 is chosen. It comes in a **1206** package and has an impedance of almost 50 Ω at 1 MHz and 2200 Ω at 100 MHz.

The choice of the common mode choke also has an influence on the mode conversion. The higher the number of turns in a choke with the same winding technology, the higher (worse for signal integrity) the mode conversion between differential and common mode will be. Mode conversion means that a portion of the differential signal is converted into an interfering common mode signal, possibly non-linearly over the frequency.

Electrical characteristics of the current-compensated choke part number [744232222](#) are shown in Table 2.

Properties	Test conditions	Value	Tolerance
Z	100 MHz	2200 Ω	± 25%
U _R		20 V	Typ.
I _R	ΔT = 20 K	200 mA	Max.
R _{Dc}	T = 20°C	1200 mΩ	Max.

Table 2: Electrical characteristics of the current-compensated choke.

The higher the number of turns of a choke with the same winding technology, the higher (worse for signal integrity) the mode conversion between differential and common mode (Figure 11).

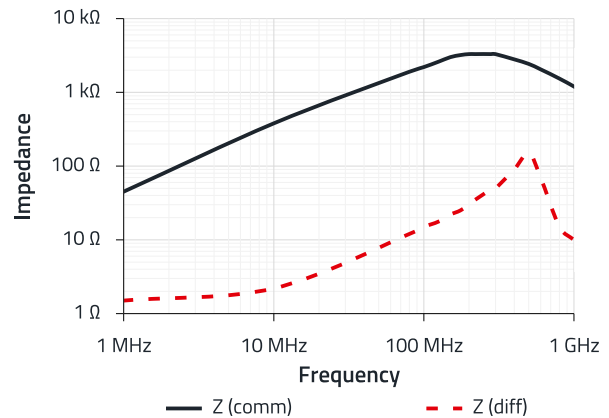


Figure 11: Common mode and differential mode impedance [744232222](#).

3.6 Protecting the interface from ESD

TVS diodes can reduce transient over voltages to a level that is not critical for ICs and that does not cause these transient interference signals to couple into other traces. Besides the clamping effect, however, the TVS diodes shouldn't influence the data signal.

To ensure the SPE data signal is not disturbed by the parasitic capacitance of the TVS diode, the capacitance value of the TVS diode should not exceed 2 pF.

For SPE systems the part number [824012823](#) from the WE-TV Super Speed series can be used; the TVS diode array loads the signal lines with only 0.27 pF each. The lines are connected to the two pins for signal input (I/O 1 and I/O 2). The signal amplitude should not exceed 3.3 V_{PEAK} (Figure 12).

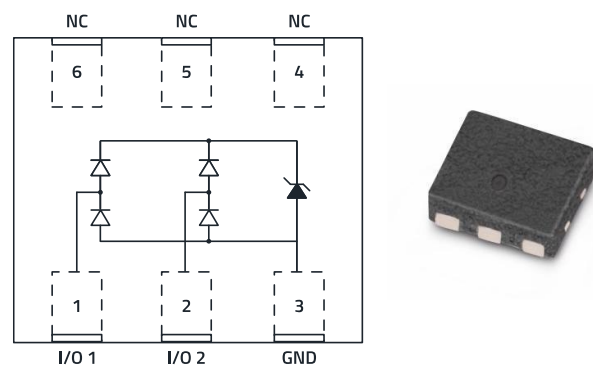


Figure 12: TVS diode schematic and product.

At 10 GHz (i.e. far higher than the required 66 MHz) the IL value of the array is -1.57 dB. The TVS Diode is therefore almost "invisible" for the data signal.

APPLICATION NOTE

ANP085 | Single Pair Ethernet for Industrial Applications

Figure 13 shows the clamping behavior during an ESD event.

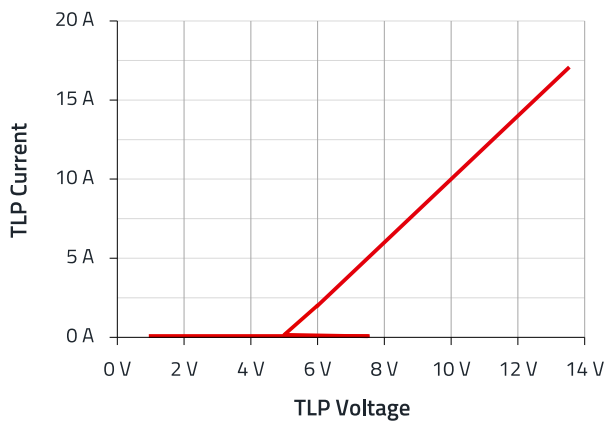


Figure 13: TLP Measurement.

The Transmission Line Pulse (TLP)-method is a test method used to simulate loads with short pulse widths and fast rise times, as typically occur in ESD events. In our case, this means switching from 0 A to 13.5 A with 100 ns pulses. A 4 kV ESD pulse in accordance with IEC 61000-4-2 generates a current of 8 A after 30 ns. If this pulse is clamped with the TVS diode array mentioned above, the clamping voltage at the diode is 6 V according to the data sheet. The IC therefore only has a voltage of 6 V at the signal pin instead of 4 kV.

In general, the TVS diode should be placed as close as possible to the interface connector, as this limits the high-frequency ESD pulse directly at the device interface and prevents it from being coupled into other signal lines. During a hipot test, however, the TVS diode can trigger incorrectly and switch to the conductive (low-impedance) state. To avoid short circuits or damage to the diode due to the high-test current, the diode is either placed between transformer and PHY or (if placed between socket and transformer) galvanically isolated from GND during the test.

3.7 Performance Comparison SPE automotive vs. SPE industrial

In the following section, the performance of the transformer circuit is compared with two other circuits. Variant 2 uses 100 nF capacitors with a dielectric strength of 50 V for galvanic isolation, as typically used in the Automotive Ethernet sector. In variant 3, capacitors with 100 nF are also used, but they have a dielectric strength of 2 kV. The high return loss requirements of 10BASE-T1 and the mode conversion loss for 100BASE-T1 lead to different design approaches for each variant. The main difference between 10BASE-T1 and 100BASE-T1 designs lies in the use of common mode chokes (CMC) for common mode filtering:

while they are typically used with 100BASE-T1, they are often not used with 10BASE-T1. With 100BASE-T1, the use of a CMC is usually necessary – also due to the stricter specifications and higher frequencies.

For SPE 10BASE-T1 the circuit diagram with two parallel capacitors, as described in section 3.1, is used.

Although 10BASE-T1 uses a data rate of only 10 Mbit/s, the symbol rate is 7.5 Mbaud due to the PAM-3 modulation. This results in a necessary bandwidth of up to 20 MHz. The selection of a suitable common mode choke is therefore not based on the low data rate, but on the high frequency signal components and possible interference in the range up to 20 MHz. A choke with a resonant frequency that is too low would be unsuitable in this case, as it would not sufficiently suppress the relevant frequency range or even distort the useful signal. The common mode choke [744272222](#) from WE-SL5 series is selected because it not only offers effective common mode suppression, but also has a positive influence on return loss and mode conversion loss. Due to the low cut-off frequency, both the dimensions (10 mm x 8.7 mm) and inductance value (2 x 2200 µH) of the common mode choke are correspondingly large. Figure 14 shows the impedance curve over the frequency for the [744272222](#).

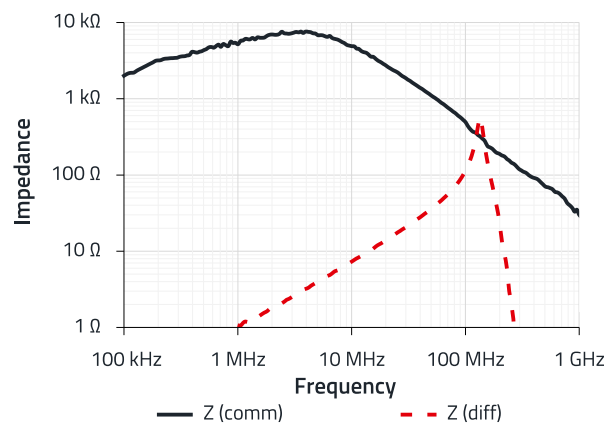


Figure 14: Common mode and differential mode impedance for WE-SL5 [744272222](#).

The alternative design solution with a transformer is shown in Figure 15. In contrast to the variants described in sections 3.1 and the following, no common mode choke is required for this 10 Mbit/s design. The main reason for this is the effective interference suppression of the transformer in the low frequency range. Another difference is an additional capacitor C_3 on the two center tap pins. This significantly improves the insertion loss and return loss up to the frequency range of around 35 kHz, resulting in significantly improved signal behavior.

APPLICATION NOTE

ANP085 | Single Pair Ethernet for Industrial Applications

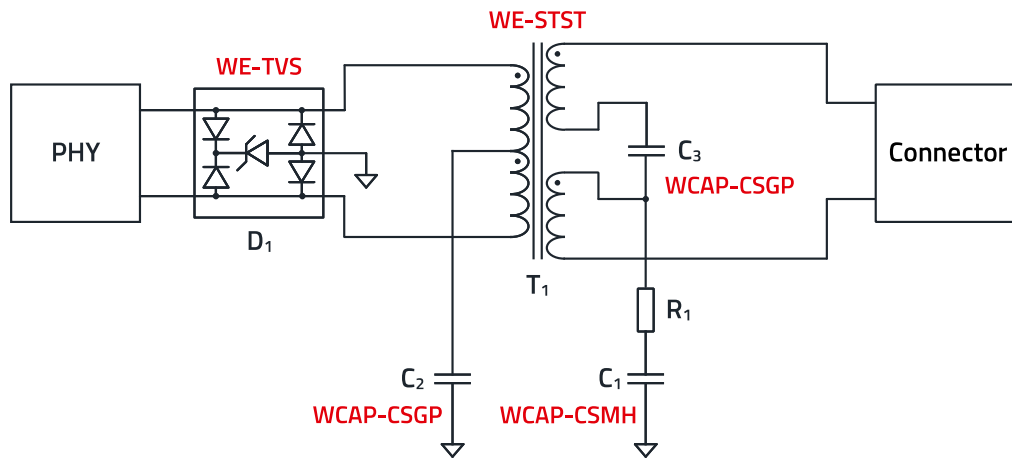


Figure 15: 10BASE-T1 transformer design.

Since it is not possible to split the center tap pin on all transformer types, the capacitor C_3 between the center pins cannot always be implemented. In this case, galvanic isolation can alternatively be achieved by using two capacitors on the outer connection of the windings. This design enlarges the circuit minimally, but has the advantage, that in a Power over Dataline (PoDL) application, the voltage at both capacitors only drops by half, thereby reducing the risk of DC bias voltage saturation of the MLCC capacitors. If only data is transmitted, capacitors with an isolation voltage of 100 V are still necessary, as the standard in section 146.8.5 requires DC insulation of 60 V for an indefinite period of time (Figure 16).

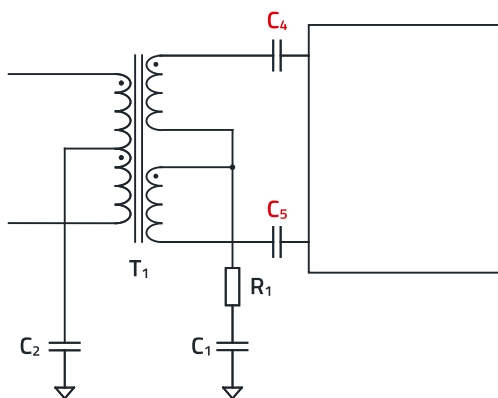


Figure 16: Capacitors C_4 and C_5 on the outer transformer pins serve as an alternative to C_3 in the circuit shown in Figure 15.

In addition to the insulation voltage of the capacitors, their capacitance is also of decisive importance in the two circuit diagrams. Simulations and measurements show that at least 100 nF are required to fulfill the limit values of IEEE802.3cg. In section "146.5.4.2 Transmitter output droop", however a

maximum voltage drop of 10% between 133.3 ns and 800 ns is required for a test signal from the PHY chip. For SPoE (Single Pair Power over Ethernet, also known as PoDL), the standard allows a significantly higher voltage drop of up to 25%. But the underlying measurement method differs from the case described above: the droop is determined here between the voltage value 400 ns after the zero crossing and the voltage value 1066.7 ns after the zero crossing. There are two ways to fulfil this requirement. Either the inductance of the transformer is increased, which results in a larger design, or capacitors with larger capacitance values are used. The second possibility is more space-saving, cheaper and easier to implement. In this case 470 nF capacitors are used to achieve the best compromise between the droop and return loss requirements. As Figure 17 and the following equation (1) shows, this circuit design achieves a maximum voltage droop of only 8.3% and is therefore within the standard.

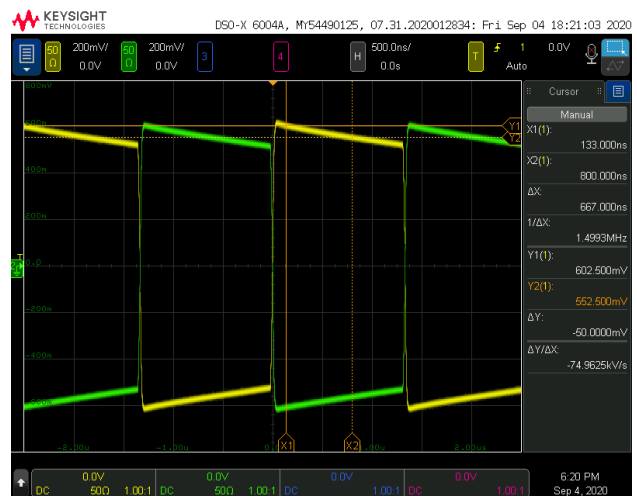


Figure 17: Measurement with the oscilloscope: The voltage droop on the signal plateau represents the voltage drop.

APPLICATION NOTE

ANP085 | Single Pair Ethernet for Industrial Applications

$$U_{\Delta\%} = \frac{100\%}{U_{133\text{ ns}}} \cdot (U_{133\text{ ns}} - U_{800\text{ ns}})$$

$$U_{\Delta\%} = \frac{100\%}{602.5\text{ mV}} \cdot (602.5\text{ mV} - 552\text{ mV}) \quad (1)$$

$$U_{\Delta\%} = 8.3\%$$

Figure 18 illustrates the differences in size of the three circuit variants.

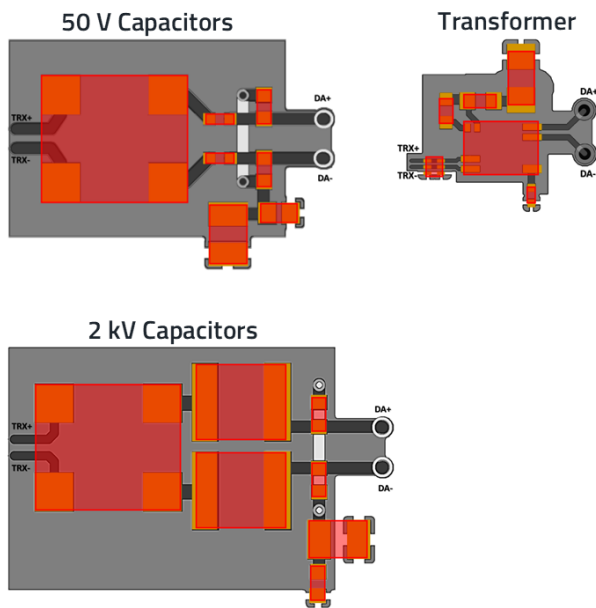


Figure 18: Footprints of the different SPE variants of galvanic isolation. Top left with 50 V capacitors, top right the transformer design, bottom with 2 kV capacitors.

The common mode choke takes up the most space on the PCB of the two 10 MBit designs with capacitor. The 100 nF capacitors with a dielectric strength of 2 kV are also relatively large.

3.8 10BASE-T1 Measurement

As the Return Loss measurement in Figure 19 shows, the values of the capacitor solutions (shown as grey dashed lines and black dotted lines in the image) are almost exactly the same. The RL readings for both cap solutions come very close to the IEEE limit line between 100 kHz and 200 kHz.

Significantly better values are achieved by the transformer design (red curve), which also achieves better results than the capacitor solution in the frequency range above 5 MHz.

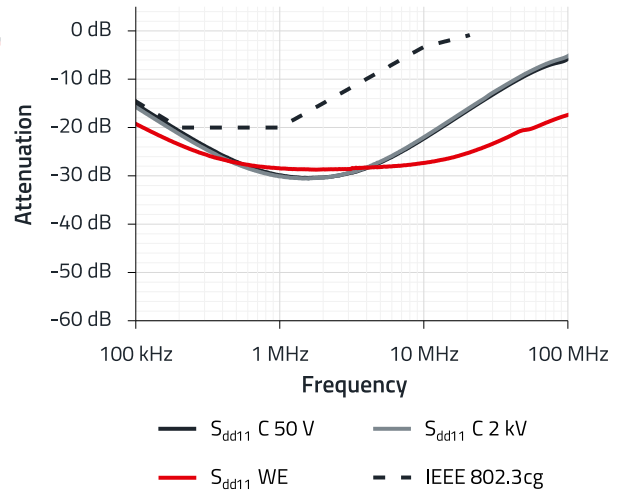


Figure 19: 10BASE-T1 return loss measurement with 50 V capacitors (grey); 2 kV capacitors (black) and transformers (red).

All three measurements show very good values for the mode conversion loss. This can be seen from the fact that the distance between target and actual values is always between 30 and 40 dB. The capacitor solutions are slightly better in the frequency range between 0.1 and 6 MHz, while the transformer solution achieves better results in the range between 6 and 20 MHz (Figure 20).

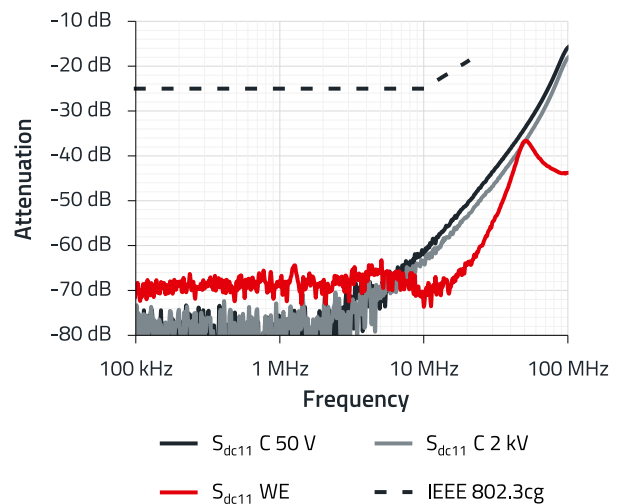


Figure 20: 10BASE-T1 mode conversion loss measurement.

APPLICATION NOTE

ANP085 | Single Pair Ethernet for Industrial Applications

3.9 100BASE-T1 Structure

The 50 V capacitor design corresponds to the 10BASE T1 design from section 3.1. The common mode choke can be dimensioned much smaller compared to the 10BASE-T1 design, because interference suppression in low frequencies between 0.1 and 1 MHz is not necessary. By reducing the size reduction of the Common Mode Choke, the 50 V solution is the most compact of all three designs.

Even if the smaller choke significantly reduces the size of the design, the footprint of the 2 kV capacitor design remains the largest of all designs in terms of area (see Figure 21).

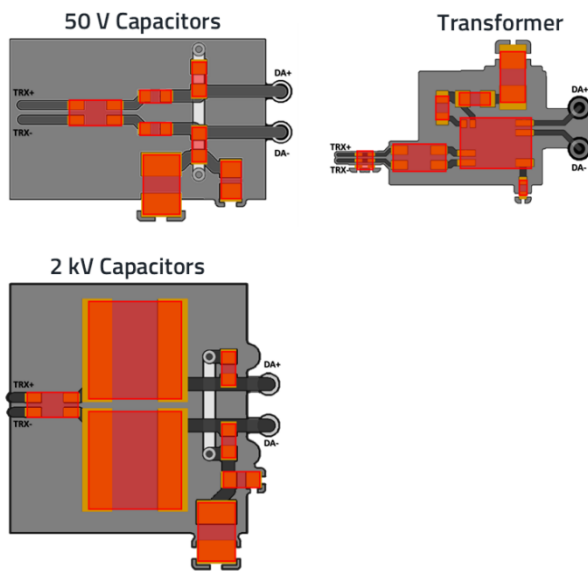


Figure 21: Size comparison of different footprints on the PCB for Single Pair Ethernet 100BASE-T1.

Apart from the large capacitors, there are no differences to the 50 V automotive Ethernet design.

In contrast to 10BASE-T1, the transformer design requires a common mode choke for interference suppression at frequencies up to 200 MHz. The circuit diagram corresponds to that in section 3.2. The common mode choke reduces both the mode conversion and common-mode signals in the higher frequency range.

The results will be discussed in more detail in the next section "100BASE-T1 Measurement".

3.10 100BASE-T1 Measurement

From Figure 22 can be seen that when measuring the return loss, the values in the frequency range between 1 - 20 MHz are closer to the target curve for the transformer solution than for the other two designs.

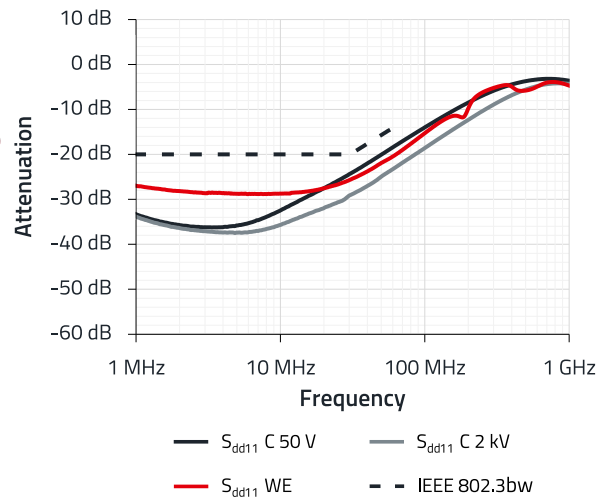


Figure 22: 100BASE-T1 Return Loss measurement.

However, the solution with the 2 kV capacitors achieves the best results. Overall, the values of all measurement traces are within a sufficient safety margin of at least 3 dB from the return loss limit.

In the case of mode conversion loss, the measured values in the design with the 50 V capacitors are very close to the limit of the IEEE standard from 25 MHz and in some cases exceed it (Figure 23).

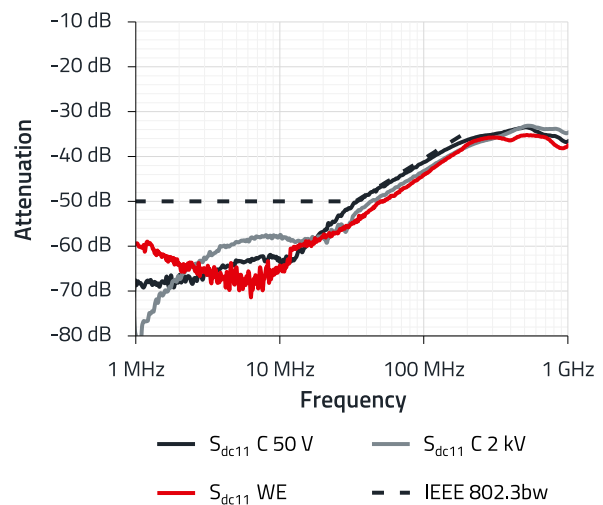


Figure 23: 100BASE-T1 mode conversion loss measurement results.

APPLICATION NOTE

ANP085 | Single Pair Ethernet for Industrial Applications

The transformer design and the variant with the 2 kV capacitors prove to be a better alternative here, as their measurements curves in this frequency range show a significantly greater distance to the target curve of around 3 dB.

4. SUMMARY/CONCLUSION

With both capacitor designs, it is not possible to ensure that the return loss of the circuit reliably fulfils the requirements of IEEE 802.3cz for 10BASE-T1 due to the expected component tolerances. In addition, the space required for both the common mode choke and the 2 kV capacitors solution is significantly greater than for the transformer solution.

For the 100BASE-T1 designs, the 50 V capacitor solution also proves to be only partially suitable to meet the mode conversion loss requirement in the frequency range above 30 MHz. Even if the mandatory galvanic isolation according to IEC 62368-1 is disregarded, the transformer solution is the most compact variant and also offers the best signal stability for Single Pair Ethernet, both 10BASE-T1 and 100BASE-T1.

APPLICATION NOTE

ANP085 | Single Pair Ethernet for Industrial Applications

A APPENDIX

A.1 BOM

Description	Package	Electrical Specification	Manufacturer	Order Code
SPE cable IP20		4 A/60 V _{DC} /600 MHz	Harting	33280101001
SPE jack		4 A/60 V _{DC} /600 MHz	Harting	09452812800
TVS Diode	DFN1210	3.3 V _{DC} ; 0.18 pF	Würth Elektronik	824012823
Common Mode Choke	1206	Z = 2200 Ω @ 100 MHz	Würth Elektronik	744232222
Signal Transformer	1812	2250 V(DC); 350 μH	Würth Elektronik	74930000
Capacitor 1	1206	1 nF, 2000 V _{DC}	Würth Elektronik	885342208024
Capacitor 2	0402	100 nF; 50 V _{DC}	Würth Elektronik	885012205086
Capacitor 3	0603	470 nF; 25 V _{DC}	Würth Elektronik	885012206075
Resistor	0603	100 Ω		---

APPLICATION NOTE

ANP085 | Single Pair Ethernet for Industrial Applications

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REVISION HISTORY

Document Version	Release Date	Changes
AN085a	2021/03/21	Initial release of the application note
AN085b	2022/22/09	Text revision
AN085c	2026/03/12	General text revision. Figure 08 with CMC on the connector side. New template.

Note: The current version of the document and the release date are indicated in the footer of each page of this document.