4 Channel Digital Isolator with Integrated 0.65W Isolated DC/DC Power Module

DESCRIPTION

The CDIP 18024x15401x is a 4 channel digital isolator that includes an integrated isolated DC/DC converter.

A single supply voltage is necessary to power both the primary side channels and the integrated isolated power supply. The integrated power supply generates the required isolated secondary supply voltage.

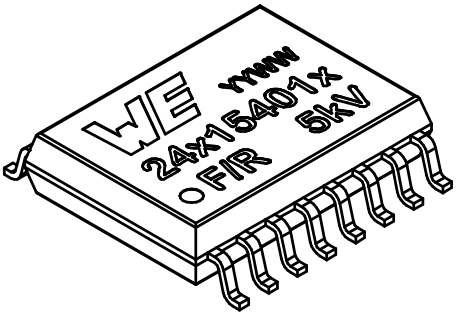
The integrated power module has integrated protection systems that guard against thermal overstress with thermal shutdown and protect against electrical damage using overcurrent, short-circuit and undervoltage circuitry.

The CDIP digital isolator ensures fast time to market and low development costs.

The digital isolator is available in an SOIC-16WB package (10.3 x 10.3 x 2.65)mm.

FEATURES

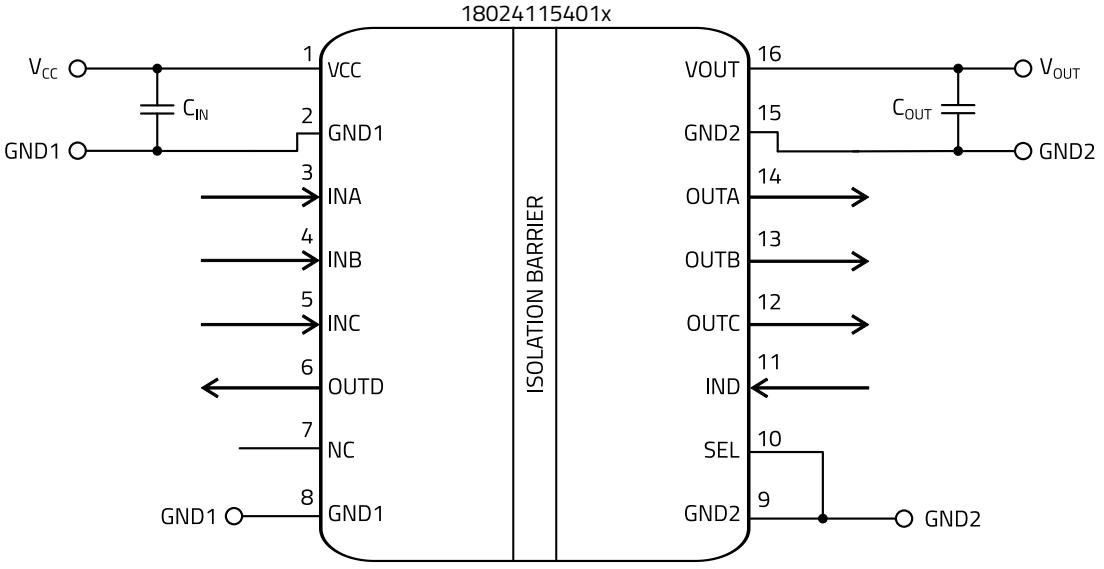
- 5kV$_{RMS}$ for 60s
- Reinforced isolation
- Input voltage range: 3.15V to 5.5V
- User-selectable output voltage: 5V or 3.3V
- Data rate up to 100Mbps
- ±150kV/µs typ. CMTI
- Available channel configurations: 4/0, 3/1 and 2/2
- Default channel output status: high or low
- Low propagation delay: 10ns typ.
- Ambient temperature range: -40°C to 125°C
- RoHS and REACh compliant
- Complies with EN55032 (CISPR-32) class B conducted and radiated emissions standard
- UL1577 recognized
- DIN EN IEC 60747-17 (VDE 0884-17):2021-10 certified



TYPICAL APPLICATIONS

- Isolated communication interfaces (SPI, CAN, RS-232, RS-485)
- Motor control
- Battery management systems
- Solar inverters
- Test and measurement systems
- Programmable logic controller (PLC) interfaces

TYPICAL CIRCUIT DIAGRAM



The above diagram indicates only one of the possible channel configurations available.

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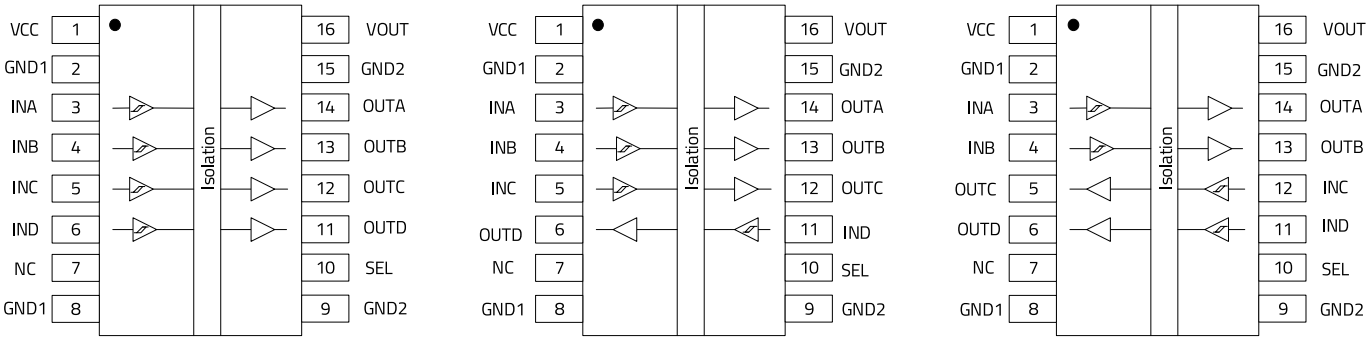
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1 PINOUT



18024015401(H/L) 18024115401(H/L) 18024215401(H/L)

Figure 1: Pinout.

Table 1: Marking description.

MARKING	DESCRIPTION
WE	Würth Elektronik eiSos GmbH & Co. KG
YYWW	Year and calendar week
24x15401x	Order code
F/R	Number of forward/reverse channels
5kV	5kV isolation voltage

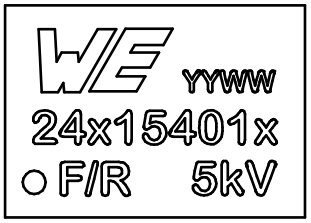


Figure 2: Marking.

Table 2: Pin description.

SYMBOL	NUMBER	TYPE	DESCRIPTION
VCC	1	Power	Integrated power module voltage input.
GND1	2	Power	Primary side ground connection.
INA	3	I/O	Digital input A.
INB	4	I/O	Digital input B.
INC/OUTC	5	I/O	Digital input/output C.
IND/OUTD	6	I/O	Digital input/output D.
NC	7	NC	Not internally connected.
GND1	8	Power	Primary side ground connection.
GND2	9	Power	Secondary side ground connection.
SEL	10	Input	Output voltage selection pin. Connect to VOUT pin for 5V. Connect to GND2 for 3.3V.
OUTD/IND	11	I/O	Digital input/output D.
OUTC/INC	12	I/O	Digital input/output C.
OUTB	13	I/O	Digital output B.
OUTA	14	I/O	Digital output A.
GND2	15	Power	Secondary side ground connection.
VOUT	16	Power	Integrated power module voltage output. Either 5V or 3.3V, depending on the state applied to SEL pin.

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2 ORDERING INFORMATION

Table 3: Ordering information.

ORDER CODE	SPECIFICATIONS	PACKAGE	PACKAGING UNIT
18024015401H	4 forward, 0 reverse, default high	SOIC-16WB	13" Reel (1000 pieces)
18024015401L	4 forward, 0 reverse, default low		
18024115401H	3 forward, 1 reverse, default high		
18024115401L	3 forward, 1 reverse, default low		
18024215401H	2 forward, 2 reverse, default high		
18024215401L	2 forward, 2 reverse, default low		
18824x15401x	—	Eval Board	1 piece

3 SALES INFORMATION

SALES CONTACT
Würth Elektronik eiSos GmbH & Co. KG EMC and Inductive Solutions Max-Eyth-Str. 1 74638 Waldenburg Germany Tel. +49 (0) 7942 945 0 www.we-online.com/digitalisolators Technical support: powermodules@we-online.com

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4 ABSOLUTE MAXIMUM RATINGS

Caution:
Exceeding the listed absolute maximum ratings may affect the device negatively and may cause permanent damage.

Table 4: Absolute maximum ratings.

SYMBOL	PARAMETER	LIMIT		UNIT
		MIN[1]	MAX[1]	
VCC	Supply pin voltage	-0.5	6	V
VOUT	Isolated supply output voltage pin	-0.5	6	V
INX, OUTX	Voltage at INX, OUTX, SEL pins	-0.5	V_{CC} + 0.5[2]	V
I_{OUTX}	Channel output current	-20	20	mA
$T_{storage}$	Assembled, non-operating storage temperature	-65	150	°C
V_{ESD}	ESD voltage (HBM)[4]	-6	6	kV
V_{ESD}	ESD voltage (CDM)[4]	-2	2	kV

5 OPERATING CONDITIONS

Operating conditions are conditions under which the device is intended to be functional. All values are either referenced to GND1 or GND2.

MIN and MAX limits are valid for the recommended ambient temperature range of -40°C to 125°C.

Table 5: Operating conditions.

SYMBOL	PARAMETER	MIN[1]	TYP[3]	MAX[1]	UNIT
V_{CC}	Supply voltage [9]	3.15	—	5.5	V
V_{INX_H}	Logic input high threshold	2.0	—	—	V
V_{INX_L}	Logic input low threshold	—	—	0.8	V
I_{OH}	High-level channel output current V_{OUT} = 5V	-4	—	—	mA
	High-level channel output current V_{OUT} = 3.3V	-2	—	—	mA
I_{OL}	Low-level channel output current V_{OUT} = 5V	—	—	4	mA
	Low-level channel output current V_{OUT} = 3.3V	—	—	2	mA
DR	Data rate	0	—	100	Mbps
PW	Signal pulse width	5	—	—	ns
T_a	Ambient temperature range	-40	—	125	°C

6 THERMAL SPECIFICATIONS

Caution:
Exceeding the listed absolute maximum ratings may affect the device negatively and may cause permanent damage.

Table 6: Thermal specifications.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN[1]	TYP[3]	MAX[1]	UNIT
Θ_{JA}	Junction-to-ambient thermal resistance [5]		—	68.5	—	°C/W
P_D	Maximum power dissipation	V_{CC}=5.5V, V_{OUT}=5V, I_{OUT}=0.13A, 50% duty cycle square signal on all channels with C_L=15pF	—	—	1	W

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7 ELECTRICAL SPECIFICATIONS

Caution:
MIN and MAX limits are valid for the recommended ambient temperature range of -40°C to 125°C. Typical values represent statistically the utmost probable values at the following conditions: V_{CC} = 5V or 3.3V, T_A = 25°C, unless otherwise noted.

Table 7: Electrical specifications part 1.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN[1]	TYP[3]	MAX[1]	UNIT
Integrated Isolated Power Supply Output Voltage						
V_{OUT}	Integrated isolated supply regulated output voltage	V_{SEL} = 0V	3.13	3.3	3.47	V
		V_{CC} = 5V, V_{SEL} = V_{OUT}	4.75	5	5.25	V
	DC line regulation	V_{CC} = 4.5V to 5.5V or 3V to 3.6V, I_{OUT} = 50mA	—	2	—	mV/V
	DC load regulation	V_{CC} = 5V, I_{OUT} = 0A to 0.13A	—	1	—	%
	Output voltage ripple		—	50	—	mV
V_{UVLO}	Undervoltage lockout falling threshold		2.0	2.35	—	V
	Undervoltage lockout rising threshold		—	2.75	3.05	V
	Undervoltage lockout hysteresis		—	400	—	mV
I_{OUT}	Output current[7]	V_{CC} = 5V	—	0.13	—	A
		V_{CC} = 3.3V	—	0.075	—	A
η	Efficiency	V_{CC} = 5V, V_{OUT} = 5V, I_{OUT} = 0.13A	—	54	—	%
Channel Characteristics						
I_{IH}	High-level input leakage current	V_{INX} = V_{CC} or V_{OUT}	—	—	20	µA
I_{IL}	Low-level input leakage current	V_{INX} = 0V	-20	—	—	µA
V_{OH}	High-level output voltage	I_{OH} = -4mA	—	$V_{CC\ or\ OUT}$ - 0.2	—	V
V_{OL}	Low-level output voltage	I_{OL} = 4mA	—	0.2	—	V
CMTI	Common-mode transient immunity	V_{INX} = V_{CC} or 0V, V_{CM} = 1500V	—	150	—	kV/µs
Timing Characteristics						
t_r	Output signal rise time	10% to 90% of V_{OUTX}	—	2.5	4.0	ns
t_f	Output signal fall time	90% to 10% of V_{OUTX}	—	2.5	4.0	ns
t_{PLH}, t_{PHL}	Propagation delay time	50% of V_{INX} to 50% of V_{OUTX}	—	10	20	ns
PWD	Pulse width distortion $\lvert t_{PLH} - t_{PHL} \rvert$		—	0.2	4.5	ns
$t_{SK(C-C)}$	Channel-to-channel output skew time		—	0.4	2.5	ns
$t_{SK(P-P)}$	Part-to-part output skew time		—	2.0	4.5	ns

Parameters indicated in electrical specifications part 1 are applicable across all part numbers with all input/output conditions unless otherwise specified.

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Table 8: Electrical specifications part 2.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN[1]	TYP[3]	MAX[1]	UNIT
18024015401x V_{CC} = 5V and V_{OUT} = 5V						
I_{CC}	Integrated isolated power supply input current[8]	V_{INX} = channel default	—	11	—	mA
		$V_{INX} \neq$ channel default	—	15.5	—	mA
		1Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	13.6	—	mA
		10Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	17.9	—	mA
		100Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	58.6	—	mA
I_{OUT}	Integrated isolated power supply output current[8]	100Mbps	—	80	—	mA
18024115401x V_{CC} = 5V and V_{OUT} = 5V						
I_{CC}	Integrated isolated power supply input current[8]	V_{INX} = channel default	—	10	—	mA
		$V_{INX} \neq$ channel default	—	15	—	mA
		1Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	13.7	—	mA
		10Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	17.8	—	mA
		100Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	56.2	—	mA
I_{OUT}	Integrated isolated power supply output current[8]	100Mbps	—	90	—	mA
18024215401x V_{CC} = 5V and V_{OUT} = 5V						
I_{CC}	Integrated isolated power supply input current[8]	V_{INX} = channel default	—	9.8	—	mA
		$V_{INX} \neq$ channel default	—	15.9	—	mA
		1Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	13.6	—	mA
		10Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	17.2	—	mA
		100Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	50.3	—	mA
I_{OUT}	Integrated isolated power supply output current[8]	100Mbps	—	100	—	mA

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Table 9: Electrical specifications part 3.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN[1]	TYP[3]	MAX[1]	UNIT
18024015401x V_{CC} = 5V and V_{OUT} = 3.3V						
I_{CC}	Integrated isolated power supply input current[8]	V_{INX} = channel default	—	9.3	—	mA
		$V_{INX} \neq$ channel default	—	13.7	—	mA
		1Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	11.7	—	mA
		10Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	14.3	—	mA
		100Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	36	—	mA
I_{OUT}	Integrated isolated power supply output current[8]	100Mbps	—	80	—	mA
18024115401x V_{CC} = 5V and V_{OUT} = 3.3V						
I_{CC}	Integrated isolated power supply input current[8]	V_{INX} = channel default	—	8.6	—	mA
		$V_{INX} \neq$ channel default	—	13.2	—	mA
		1Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	11.8	—	mA
		10Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	14.4	—	mA
		100Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	40	—	mA
I_{OUT}	Integrated isolated power supply output current[8]	100Mbps	—	90	—	mA
18024215401x V_{CC} = 5V and V_{OUT} = 3.3V						
I_{CC}	Integrated isolated power supply input current[8]	V_{INX} = channel default	—	8.6	—	mA
		$V_{INX} \neq$ channel default	—	14	—	mA
		1Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	11.9	—	mA
		10Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	14.4	—	mA
		100Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	40.5	—	mA
I_{OUT}	Integrated isolated power supply output current[8]	100Mbps	—	100	—	mA

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Table 10: Electrical specifications part 4.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN[1]	TYP[3]	MAX[1]	UNIT
18024015401x V_{CC} = 3.3V and V_{OUT} = 3.3V						
I_{CC}	Integrated isolated power supply input current[8]	V_{INX} = channel default	—	10.7	—	mA
		$V_{INX} \neq$ channel default	—	15.5	—	mA
		1Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	13.3	—	mA
		10Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	16.3	—	mA
		100Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	46.7	—	mA
I_{OUT}	Integrated isolated power supply output current[8]	100Mbps	—	45	—	mA
18024115401x V_{CC} = 3.3V and V_{OUT} = 3.3V						
I_{CC}	Integrated isolated power supply input current[8]	V_{INX} = channel default	—	10	—	mA
		$V_{INX} \neq$ channel default	—	15.3	—	mA
		1Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	13.3	—	mA
		10Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	16.1	—	mA
		100Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	44.4	—	mA
I_{OUT}	Integrated isolated power supply output current[8]	100Mbps	—	50	—	mA
18024215401x V_{CC} = 3.3V and V_{OUT} = 3.3V						
I_{CC}	Integrated isolated power supply input current[8]	V_{INX} = channel default	—	9.7	—	mA
		$V_{INX} \neq$ channel default	—	15.7	—	mA
		1Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	13.3	—	mA
		10Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	15.8	—	mA
		100Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	41.5	—	mA
I_{OUT}	Integrated isolated power supply output current[8]	100Mbps	—	55	—	mA

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8 ISOLATION SPECIFICATIONS

Table 11: Isolation specification table.

SYMBOL	PARAMETER	TEST CONDITIONS	VALUE	UNIT
CLR	External clearance	Shortest distance through air between terminals	8	mm
CPG	External creepage	Shortest distance across package surface between terminals	8	mm
C_{IO}	Barrier capacitance, input to output	V_{IO} = 0.4 x sin (2πft), f = 1MHz	3.5	pF
R_{IO}	Isolation resistance	V_{IO} = 500V, T_A = 25°C	>10^{12}	Ω
		V_{IO} = 500V, 100°C≤T_A ≤ 125°C	>10^{11}	Ω
		V_{IO} = 500V at T_A = 150°C	>10^{9}	Ω
DTI	Distance through the insulation	Minimum internal clearance	19	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	IEC 60664-1 material group		I	
	IEC 60664-1 overvoltage category	Rated mains voltage ≤300 V_{RMS}	I-IV	
		Rated mains voltage ≤600 V_{RMS}	I-IV	
		Rated mains voltage ≤1000 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17):2021-10				
V_{IORM}	Max. repetitive peak isolation voltage	AC voltage (bipolar)	1414	V_{PK}
V_{IOWM}	Max. working isolation voltage	AC voltage; Time-dependent dielectric breakdown (TDDB) test	1000	V_{RMS}
		DC voltage	1414	V_{DC}
V_{IOTM}	Max. transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1s (100% production)	7070	V_{PK}
V_{IOSM}	Max. surge isolation voltage	Test method per IEC 60065, 1.2/50 µs waveform, V_{TEST} = 1.6 x V_{IOSM} (qualification)	7070	V_{PK}
q_{pd}	Apparent charge	Method a, after input/output safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.2 x V_{IORM}, t_m = 10s	≤5	pC
		Method a, after environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.6 x V_{IORM}, t_m = 10s	≤5	pC
		Method b1, at routine test (100% production) and preconditioning (type test), V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1s; $V_{pd(m)}$ = 1.875 x V_{IORM}, t_m = 1s	≤5	pC
	Pollution degree		2	
UL1577				
$V_{ISO(max)}$	Max. withstanding isolation voltage	V_{TEST} = V_{ISO}, t = 60s (qualification), V_{TEST} = 1.2 x V_{ISO}, t = 1s (100% production)	5000	V_{RMS}

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9 APPROVALS

Table 12: Approvals.

STANDARD	DESCRIPTION
UL 1577	UL File No: E535458
DIN EN IEC 60747-17 (VDE 0884-17):2021-10	VDE certification number: 40058069

10 RoHS, REACh

Table 13: RoHS, REACh.

RoHS directive	COMPLIANT RoHS&REACH WÜRTH ELEKTRONIK	Directive 2011/65/EU of the European Parliament and the Council of June 8th, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.
REACh directive		Directive 1907/2006/EU of the European Parliament and the Council of June 1st, 2007 regarding the Registration, Evaluation, Authorization and Restriction of Chemicals (REACh).

11 PACKAGE SPECIFICATIONS

Table 14: Package specifications.

ITEM	PARAMETER	TYP[3]	UNIT
Lead finish	Matte Sn	—	—
Weight	—	0.42	g

12 NOTES

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

(2) This value must never exceed 6V.

(3) Typical numbers are valid at 25°C ambient temperature and represent statistically the utmost probability assuming the Gaussian distribution.

(4) The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD-22-114. The charged device model test method is per JESD22-C101.

(5) Measured without heatsink, still air. (0 - 20LFM / 0 - 0.1m/s) Test PCB 80mm x 80mm horizontal orientation 35µm copper on top and bottom.

(6) 100% final production tested value. The qualified isolation voltage value is 5kV$_{RMS}$. For detailed isolation characteristics see the isolation specification table (Isolation specification table).

(7) Depending on ambient temperature, see thermal derating diagram (Thermal Derating).

(8) Supply current measurements are made with no external load connected to the integrated isolated power supply. The indicated values only describe the current required to supply the internal circuitry and external capacitive loads on the channel outputs based on the signal described in the test conditions.

(9) The supply voltage must always be equal to or greater than the selected output voltage. The device is incapable of boost operation (e.g. V_{CC} = 3.3V and V_{OUT} = 5V) and should never be used in such a configuration.

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13 TYPICAL PERFORMANCE CURVES

If not otherwise specified, the following conditions apply: T_A = 25 °C.

13.1 Radiated and Conducted Emissions (With EMI Input Filter)

The 18024x15401x digital isolators were tested in several EMC configurations to give more realistic information about implementation in the applications. The test setup is based on CISPR16 with the limit values of CISPR32. All measurements were performed with the layout and components shown in DESIGN EXAMPLE

13.1.1 Radiated Emissions EN55032 (CISPR-32) Class B Complaint Test Setup

- Measured in a Fully Anechoic Room (FAR) at 3m antenna distance.
- Input wire length: 160cm (80cm horizontal + 80cm vertical)
- Load directly on board

13.1.2 Conducted Emissions EN55032 (CISPR-32) Class B Complaint Test Setup

- Measurement input wire length: 80cm
- Load directly on board

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13.1.3 Radiated and Conducted Emissions - 18024x15401x

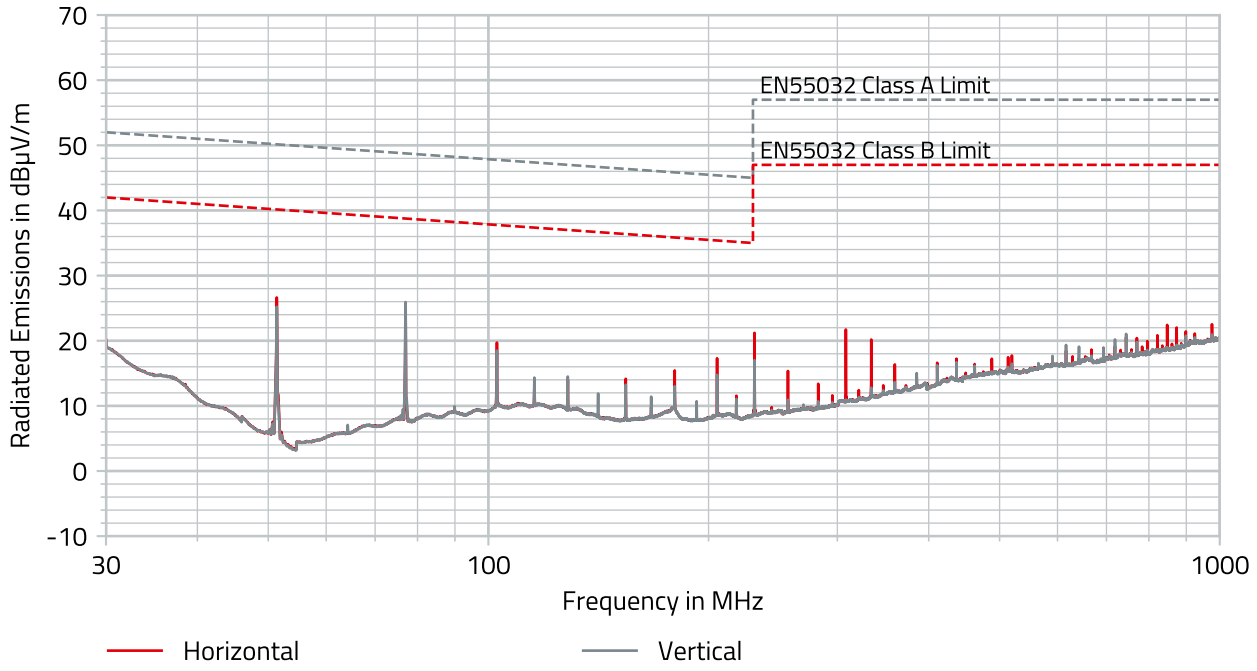


Figure 3: 18024015401H radiated EMI V_{CC} = 5V, V_{OUT} = 5V, I_{OUT} = 0.13, with input filter.

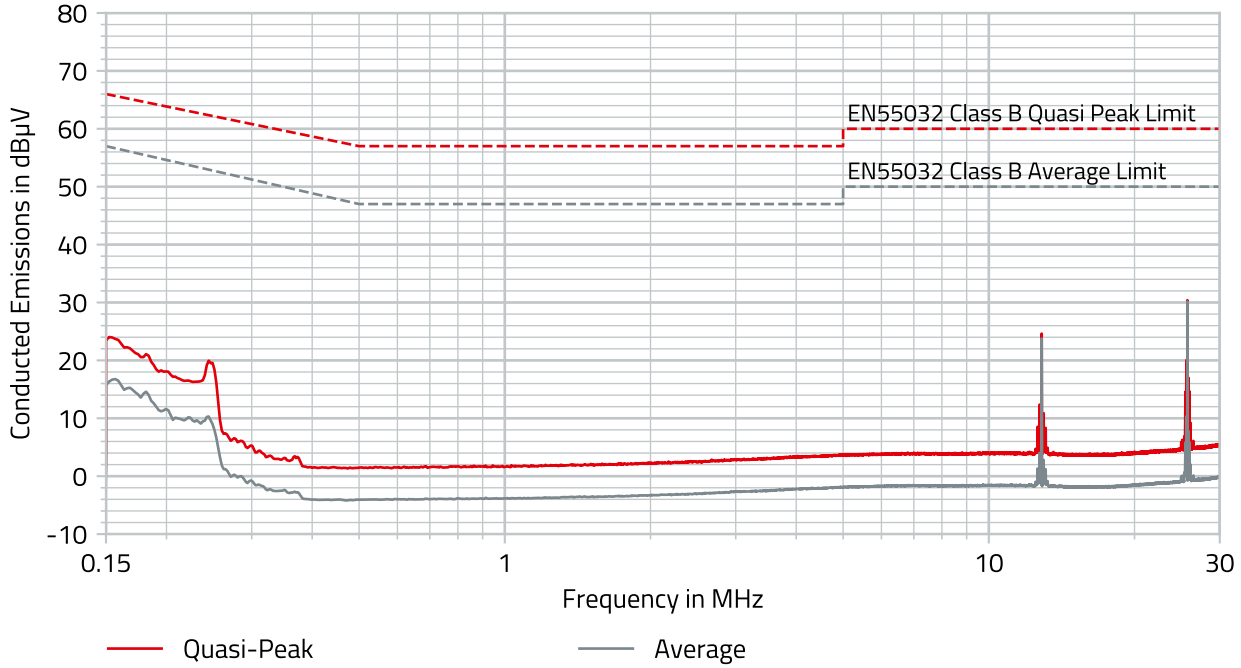


Figure 4: 18024015401H conducted EMI V_{CC} = 5V, V_{OUT} = 5V, I_{OUT} = 0.13, with input filter.

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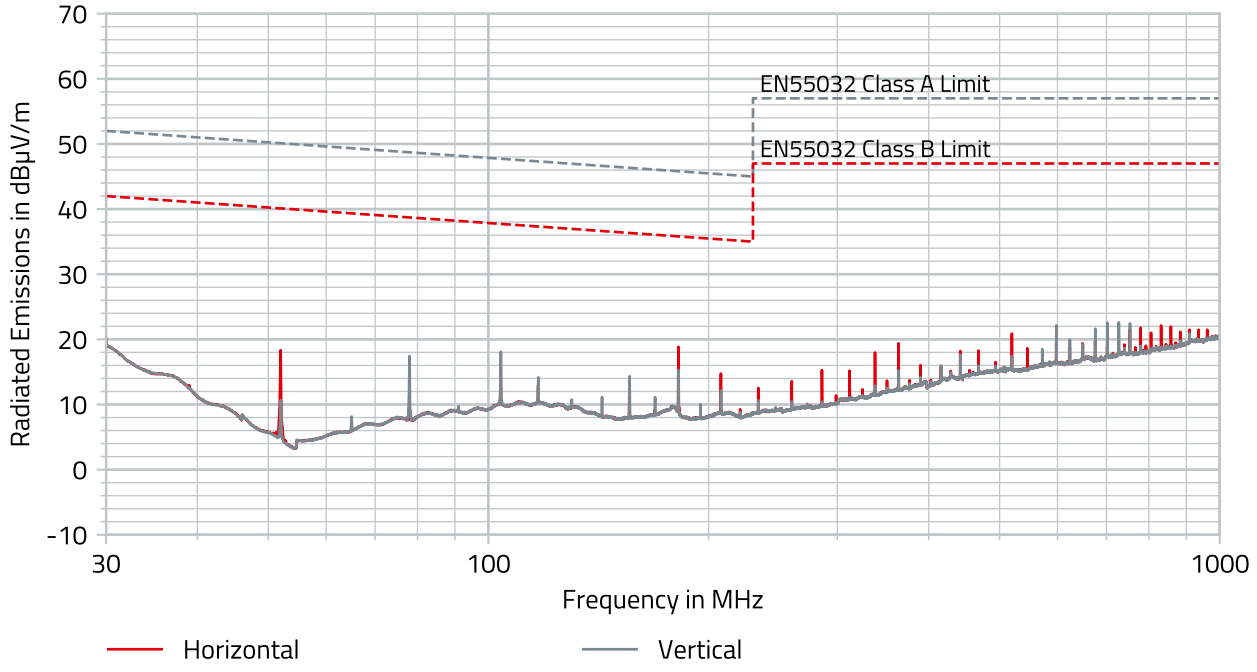


Figure 5: 18024015401L radiated EMI V_{CC} = 5V, V_{OUT} = 5V, I_{OUT} = 0.13, with input filter.

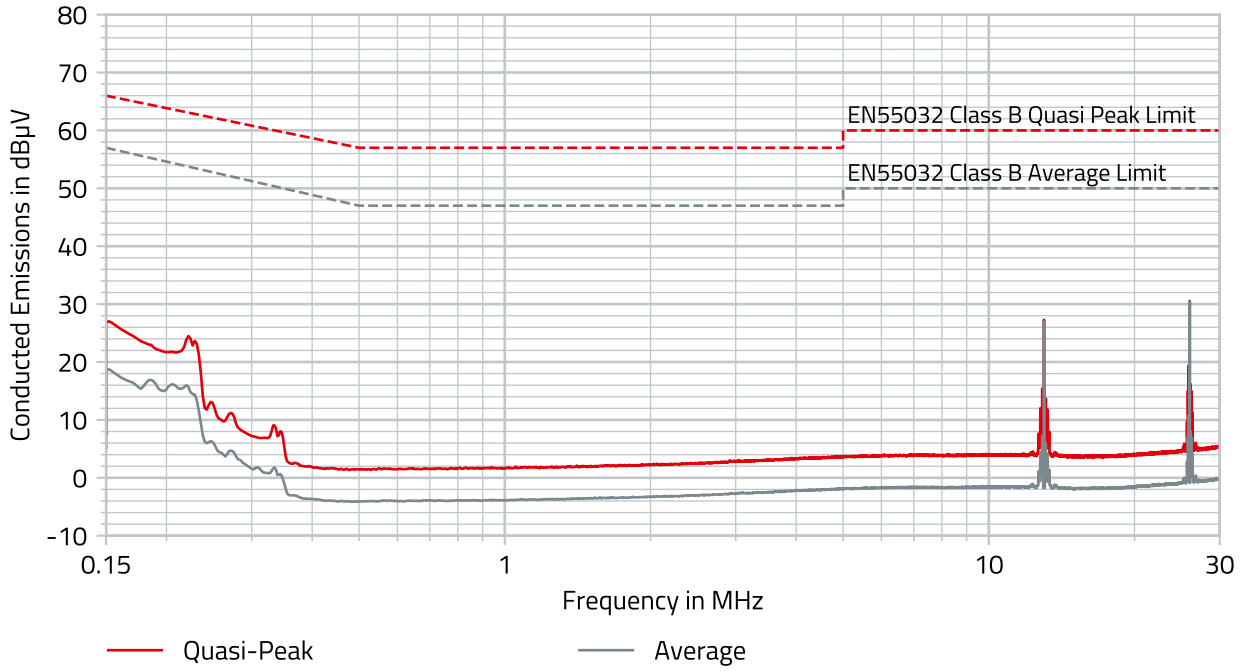


Figure 6: 18024015401L conducted EMI V_{CC} = 5V, V_{OUT} = 5V, I_{OUT} = 0.13, with input filter.

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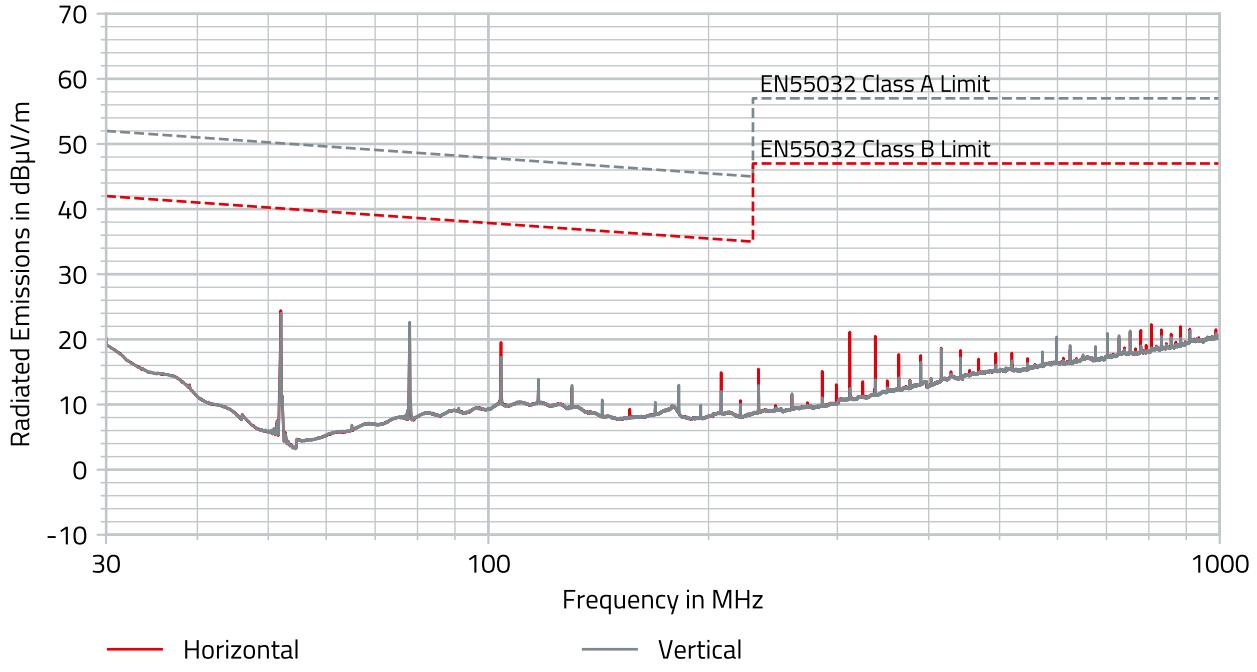


Figure 7: 18024115401H radiated EMI V_{CC} = 5V, V_{OUT} = 5V, I_{OUT} = 0.13, with input filter.

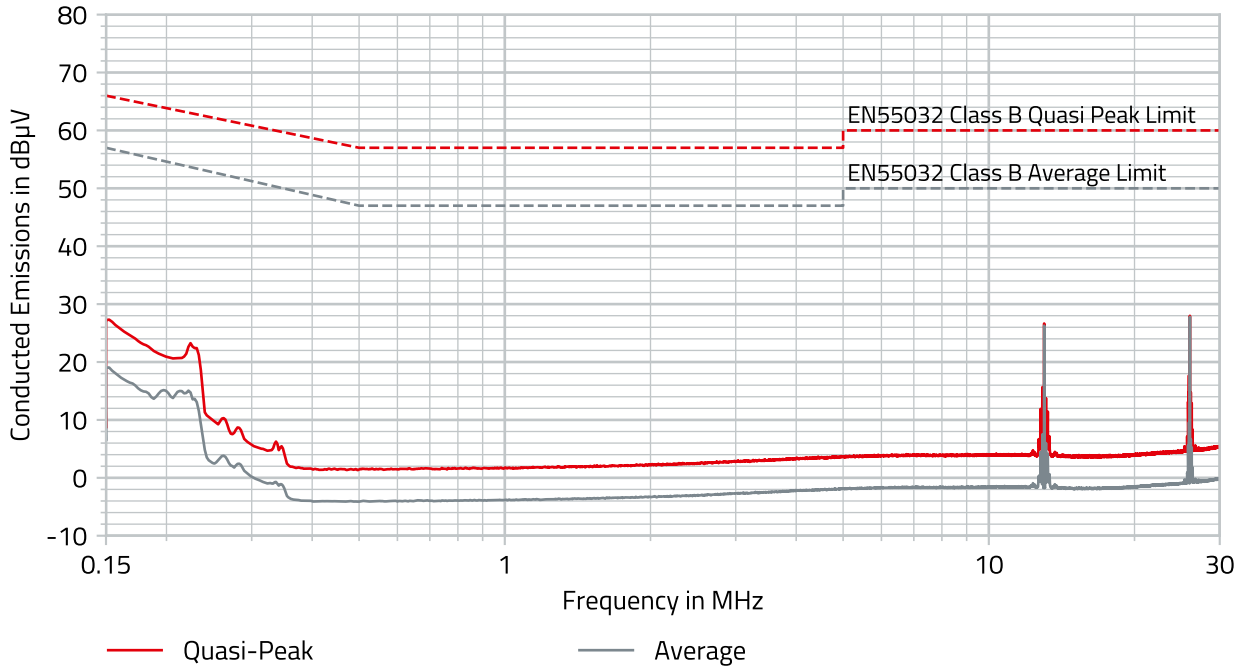


Figure 8: 18024115401H conducted EMI V_{CC} = 5V, V_{OUT} = 5V, I_{OUT} = 0.13, with input filter.

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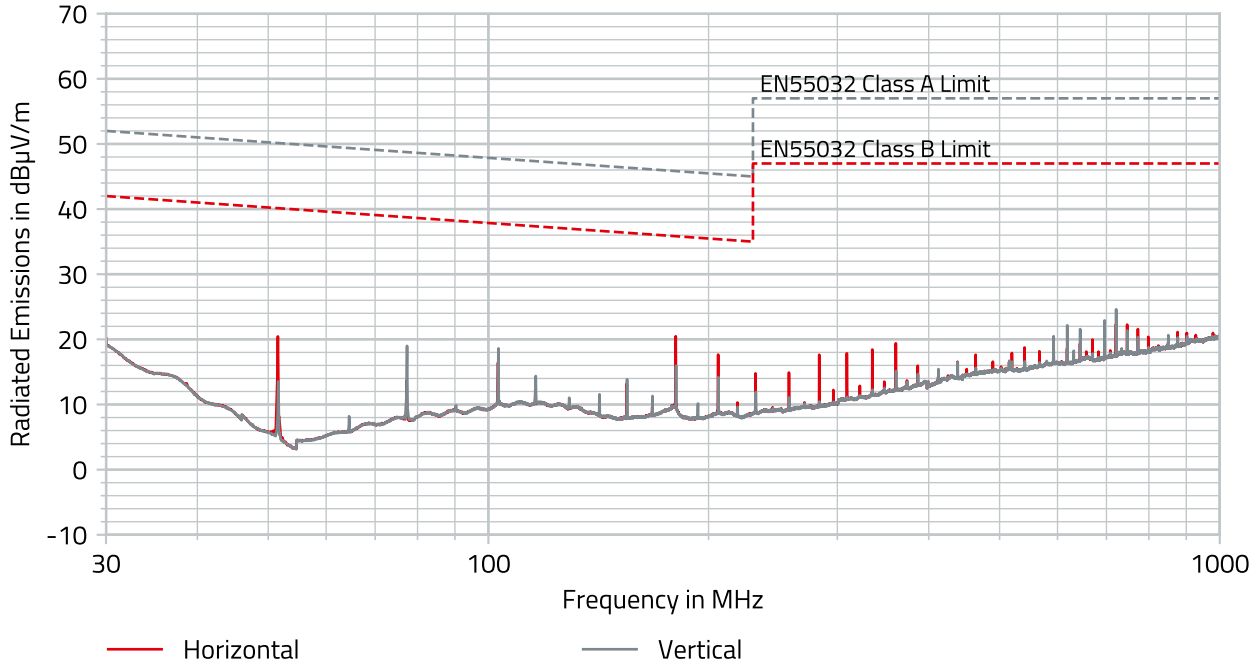


Figure 9: 18024115401L radiated EMI V_{CC} = 5V, V_{OUT} = 5V, I_{OUT} = 0.13, with input filter.

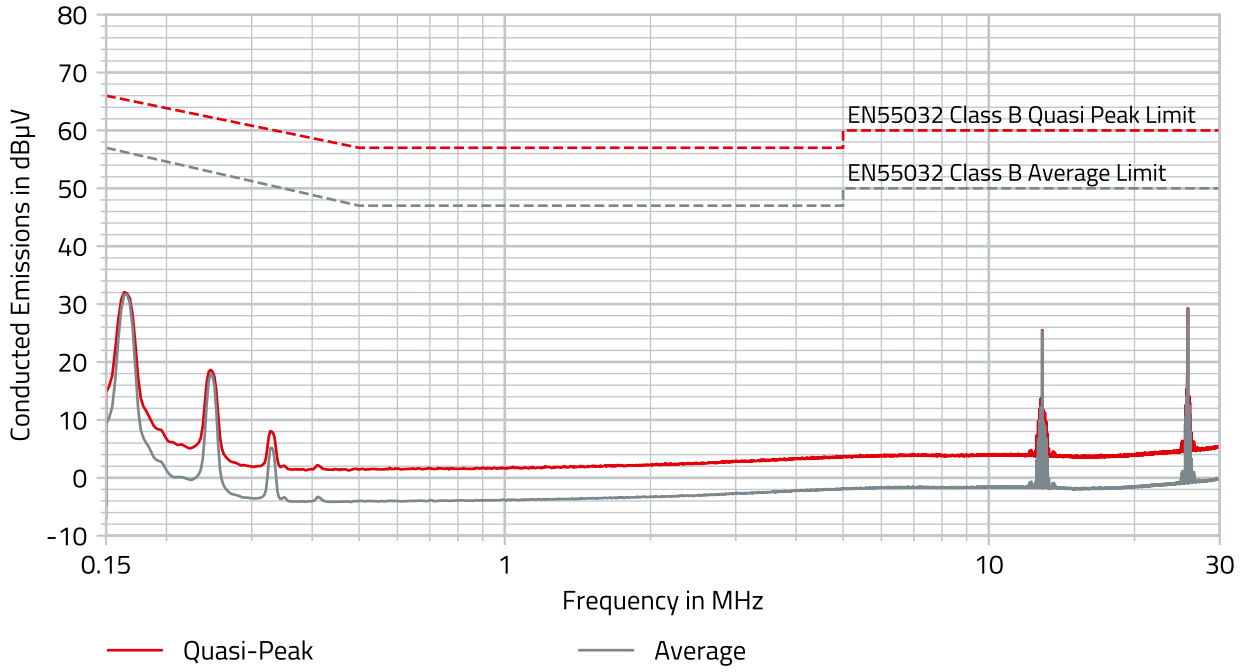


Figure 10: 18024115401L conducted EMI V_{CC} = 5V, V_{OUT} = 5V, I_{OUT} = 0.13, with input filter.

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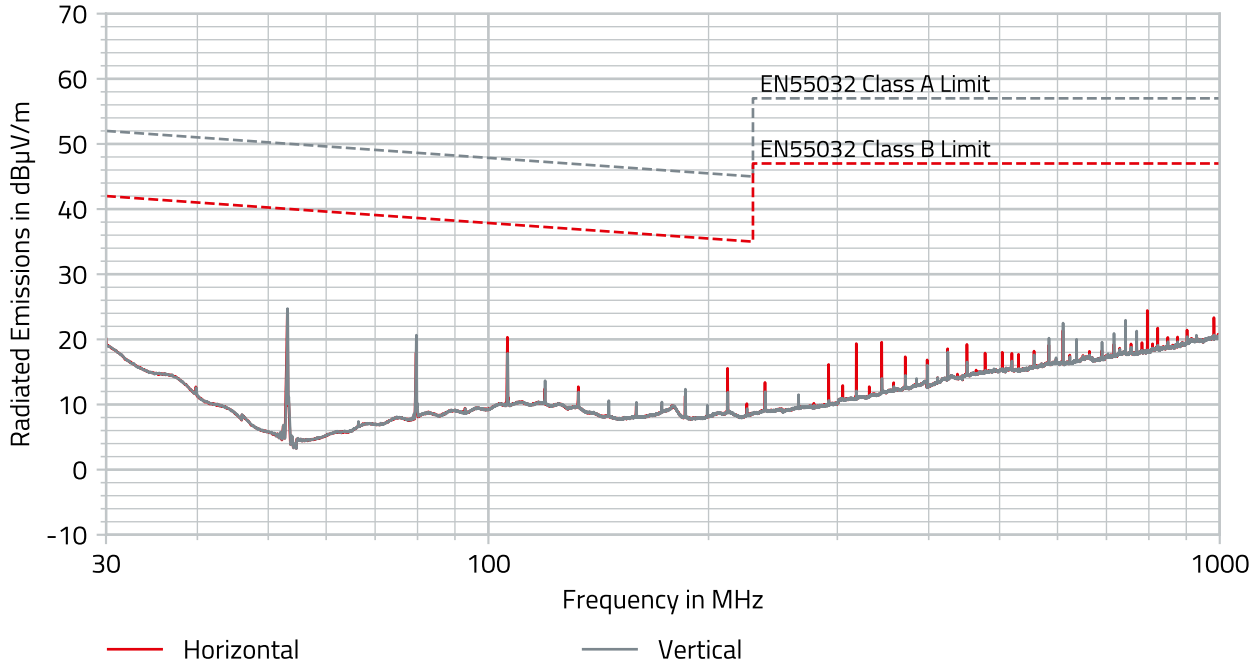


Figure 11: 18024215401H radiated EMI V_{CC} = 5V, V_{OUT} = 5V, I_{OUT} = 0.13, with input filter.

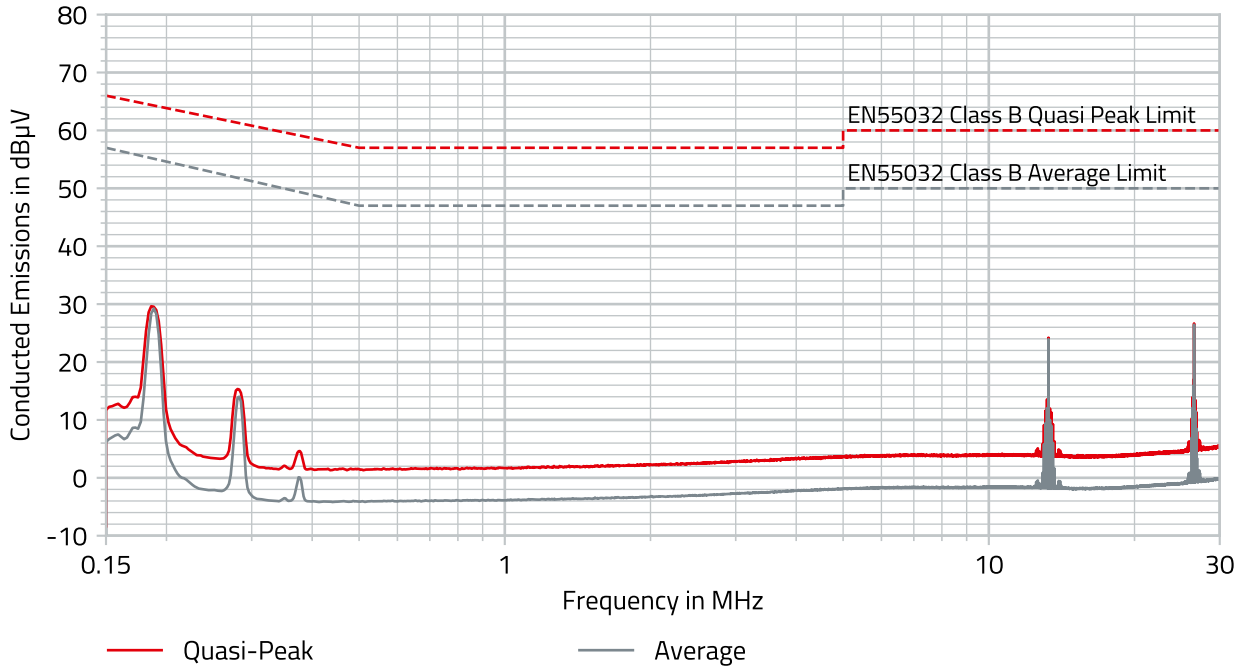


Figure 12: 18024215401H conducted EMI V_{CC} = 5V, V_{OUT} = 5V, I_{OUT} = 0.13, with input filter.

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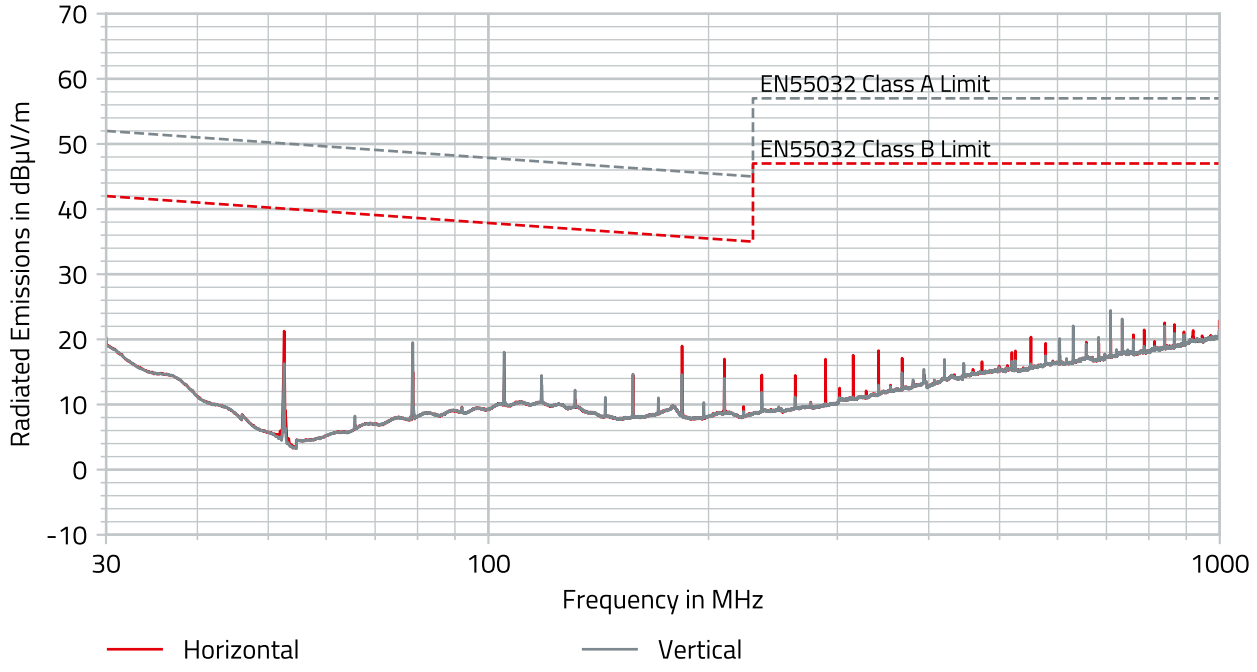


Figure 13: 18024215401L radiated EMI V_{CC} = 5V, V_{OUT} = 5V, I_{OUT} = 0.13, with input filter.

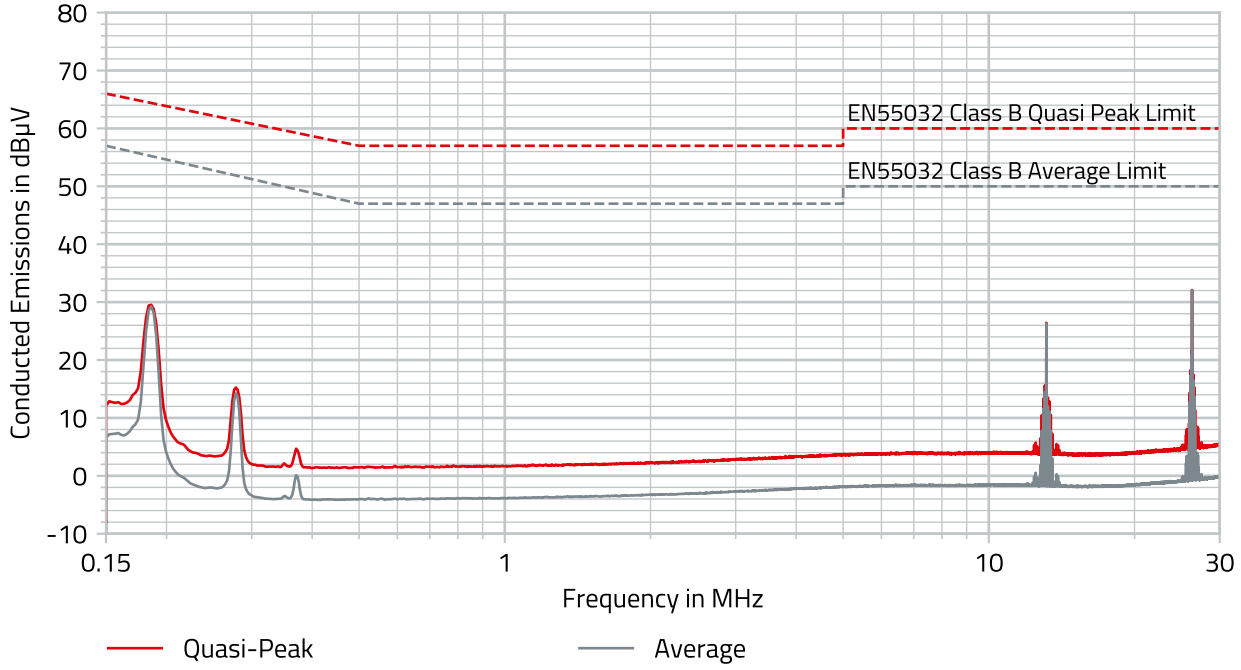


Figure 14: 18024215401L conducted EMI V_{CC} = 5V, V_{OUT} = 5V, I_{OUT} = 0.13, with input filter.

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13.2 DC Performance Curves

13.2.1 Efficiency

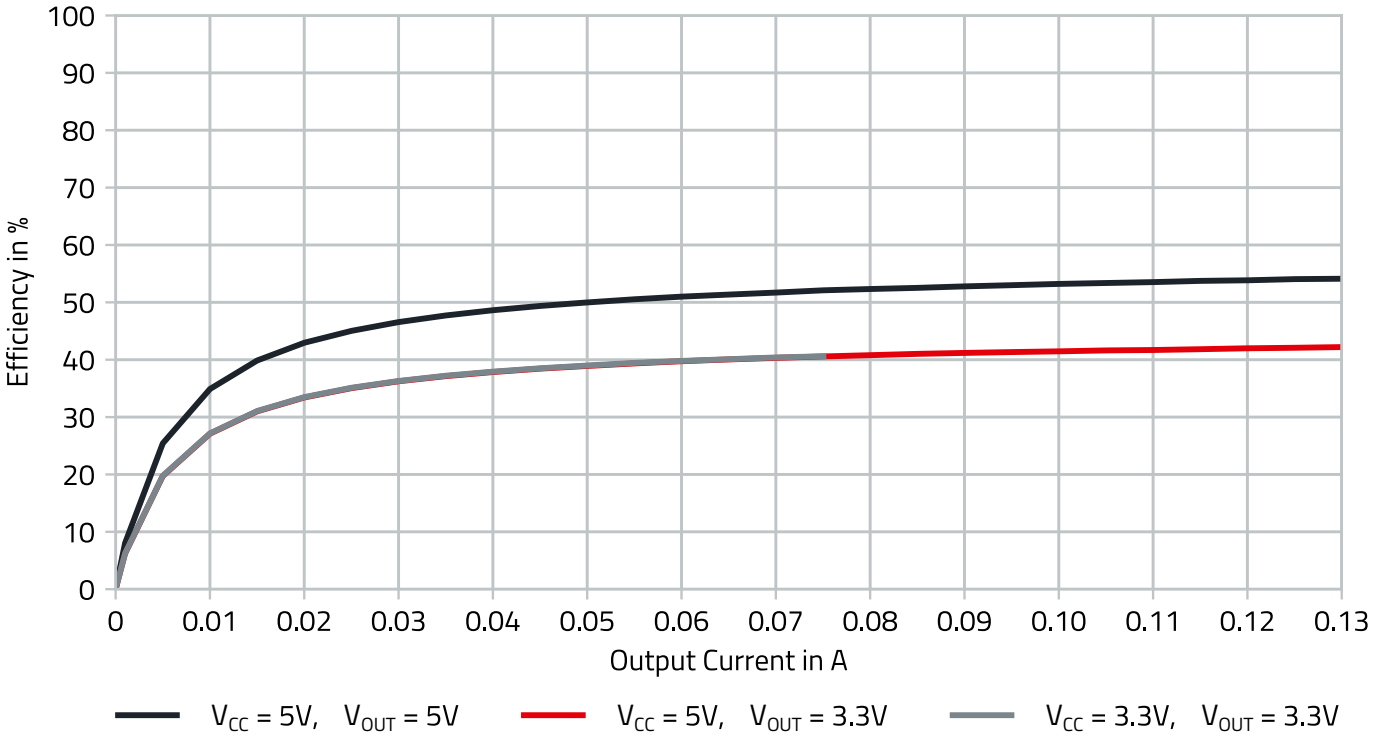


Figure 15: 18024x15401x efficiency.

13.2.2 Load Regulation

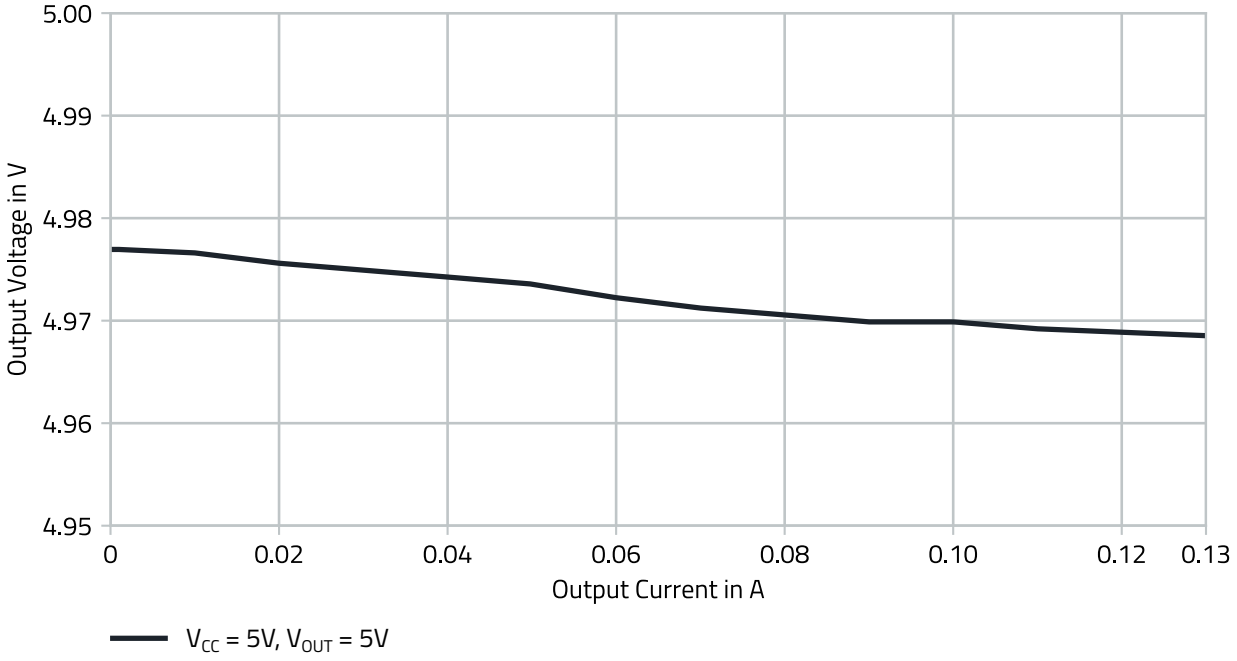


Figure 16: 18024x15401x load regulation V_{OUT} = 5V.

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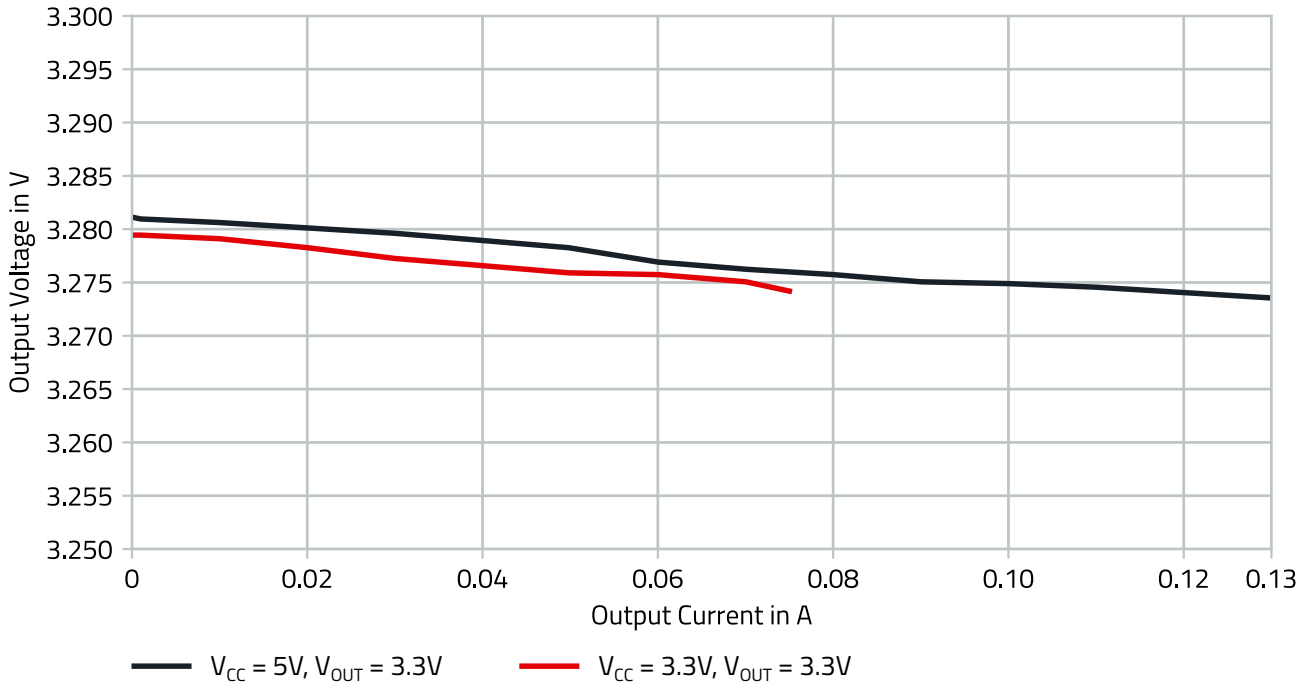


Figure 17: 18024x15401x load regulation V_{OUT} = 3.3V.

13.2.3 Load Transients

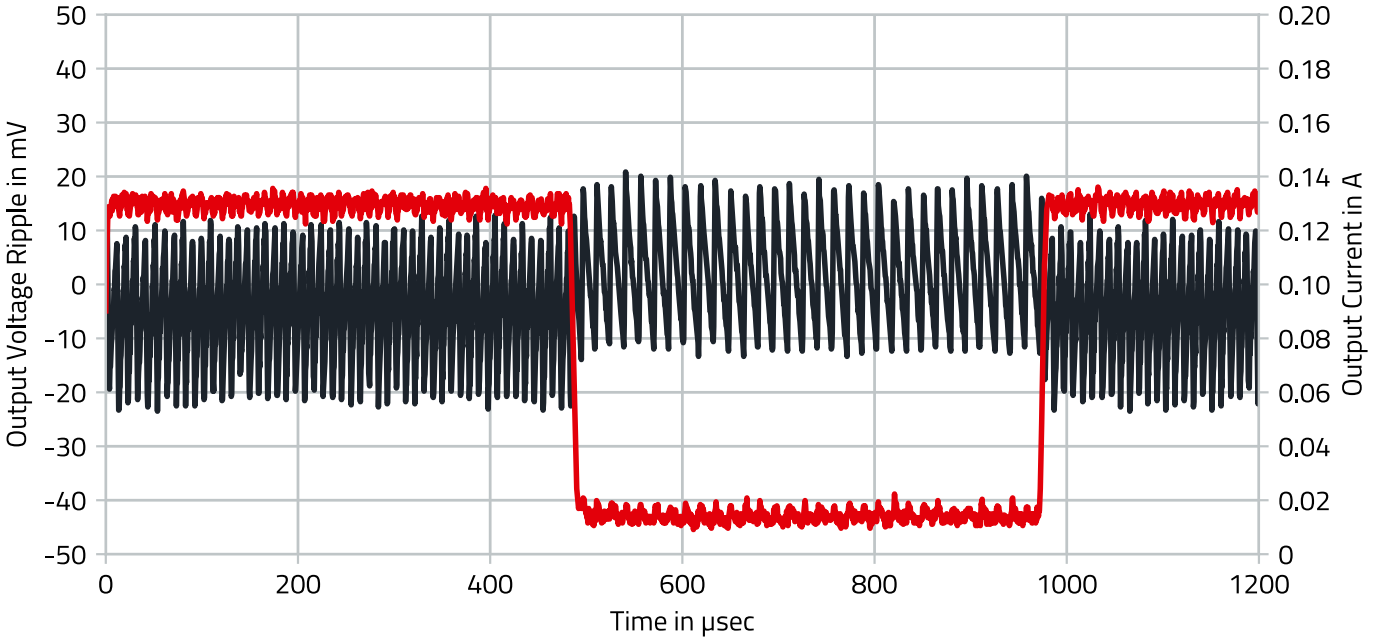


Figure 18: 18024x15401x load transient V_{CC} = 5V, V_{OUT} = 5V, I_{OUT} = 13mA to 130mA.

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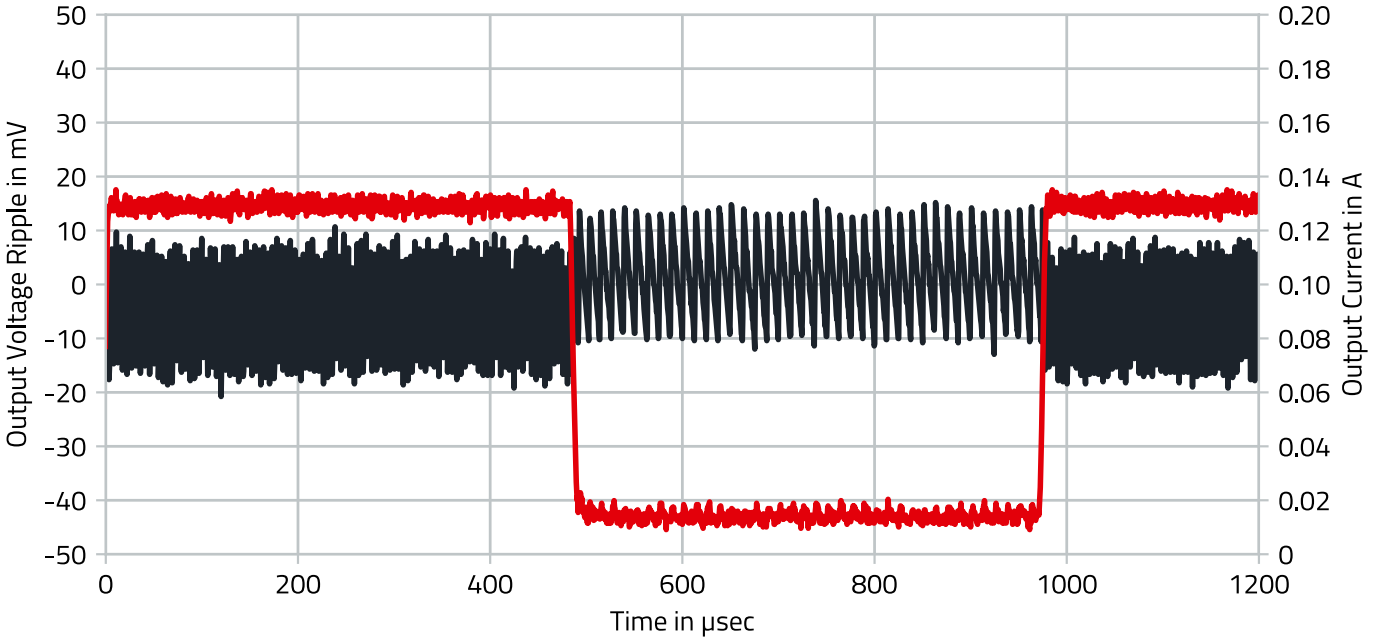


Figure 19: 18024x15401x load transient V_{CC} = 5V, V_{OUT} = 3.3V, I_{OUT} = 13mA to 130mA.

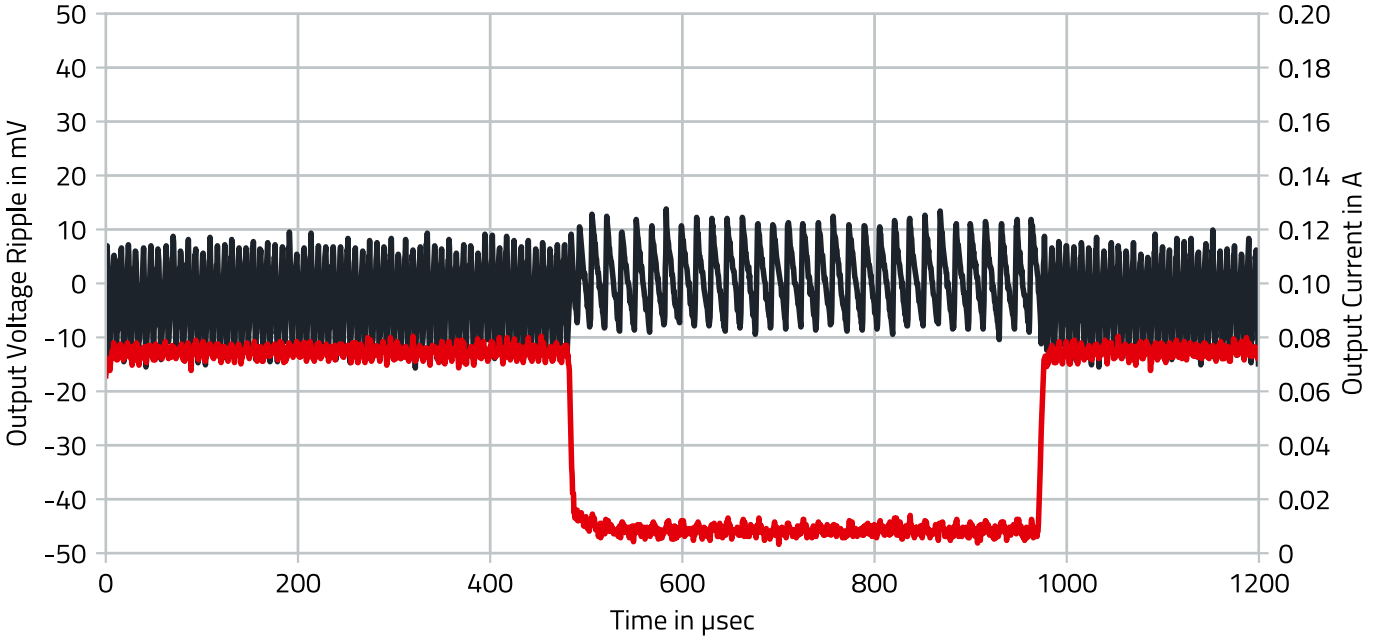


Figure 20: 18024x15401x load transient V_{CC} = 3.3V, V_{OUT} = 3.3V, I_{OUT} = 7.5mA to 75mA.

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13.2.4 Output Voltage Ripple

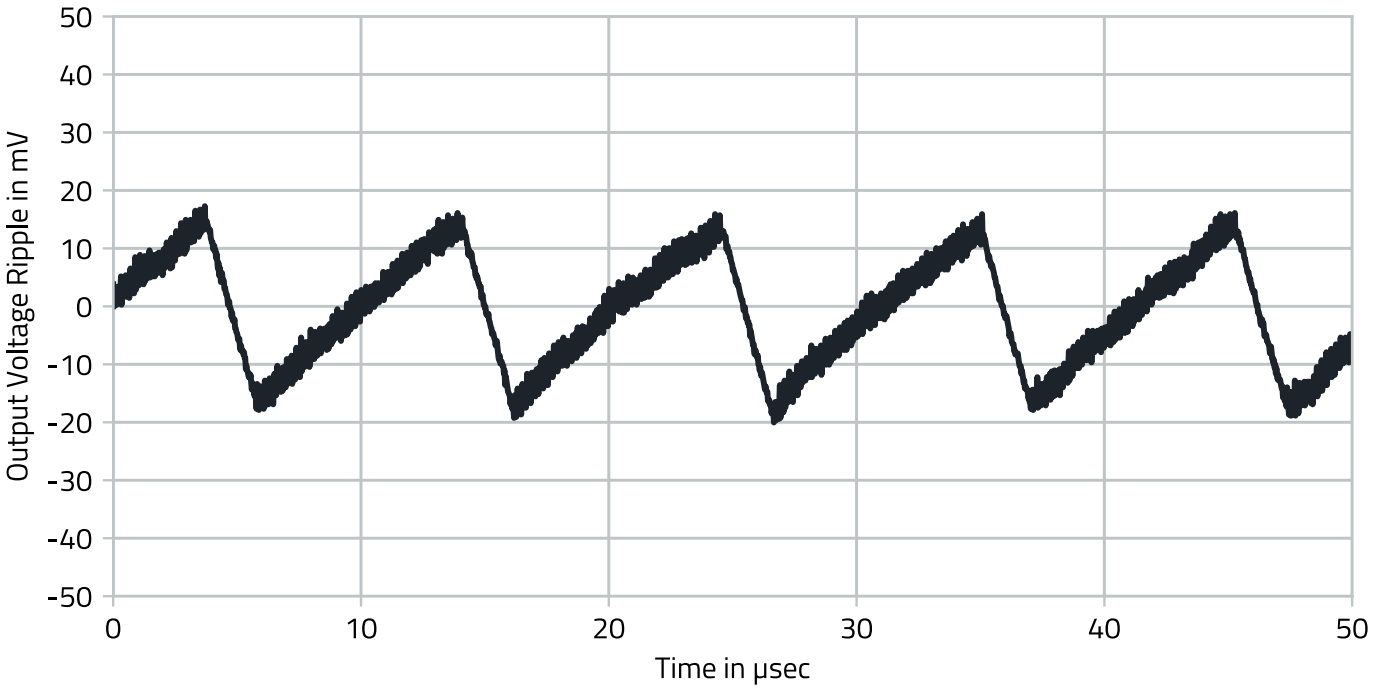


Figure 21: 18024x15401x output voltage ripple V_{CC} = 5V, V_{OUT} = 5V, I_{OUT} = 130mA.

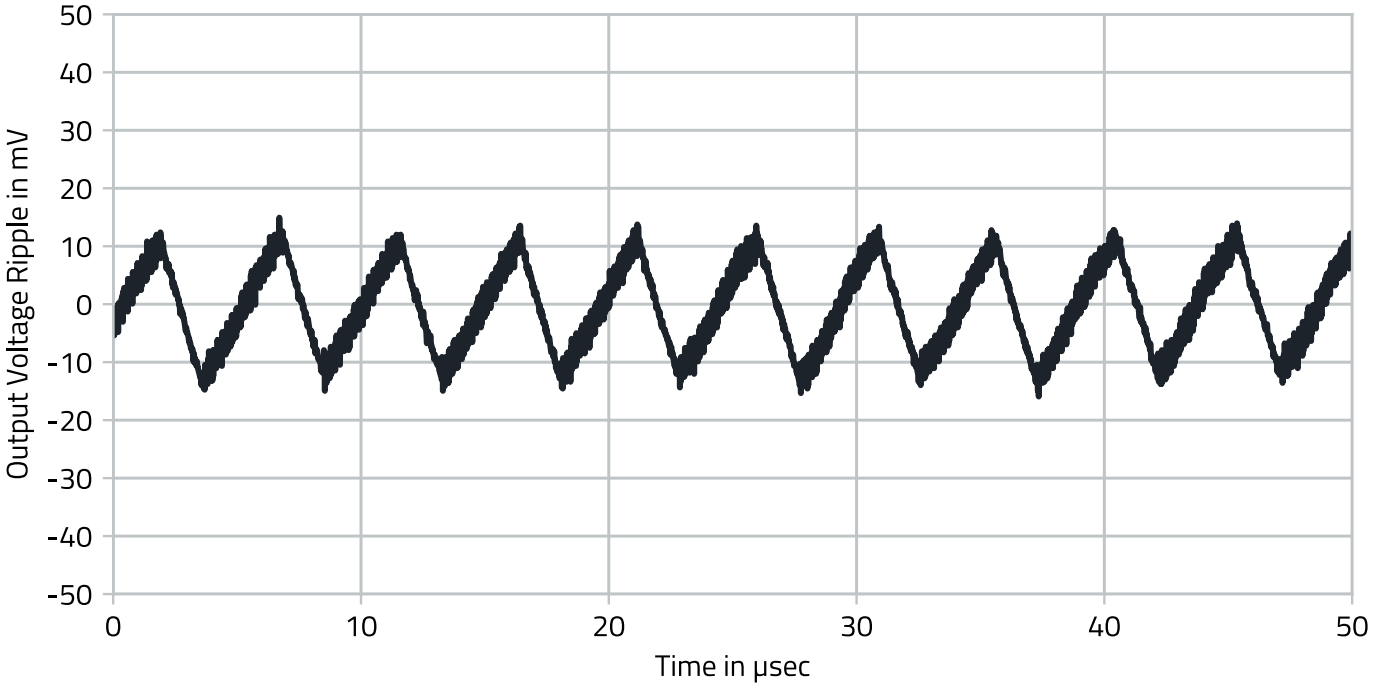


Figure 22: 18024x15401x output voltage ripple V_{CC} = 5V, V_{OUT} = 3.3V, I_{OUT} = 130mA.

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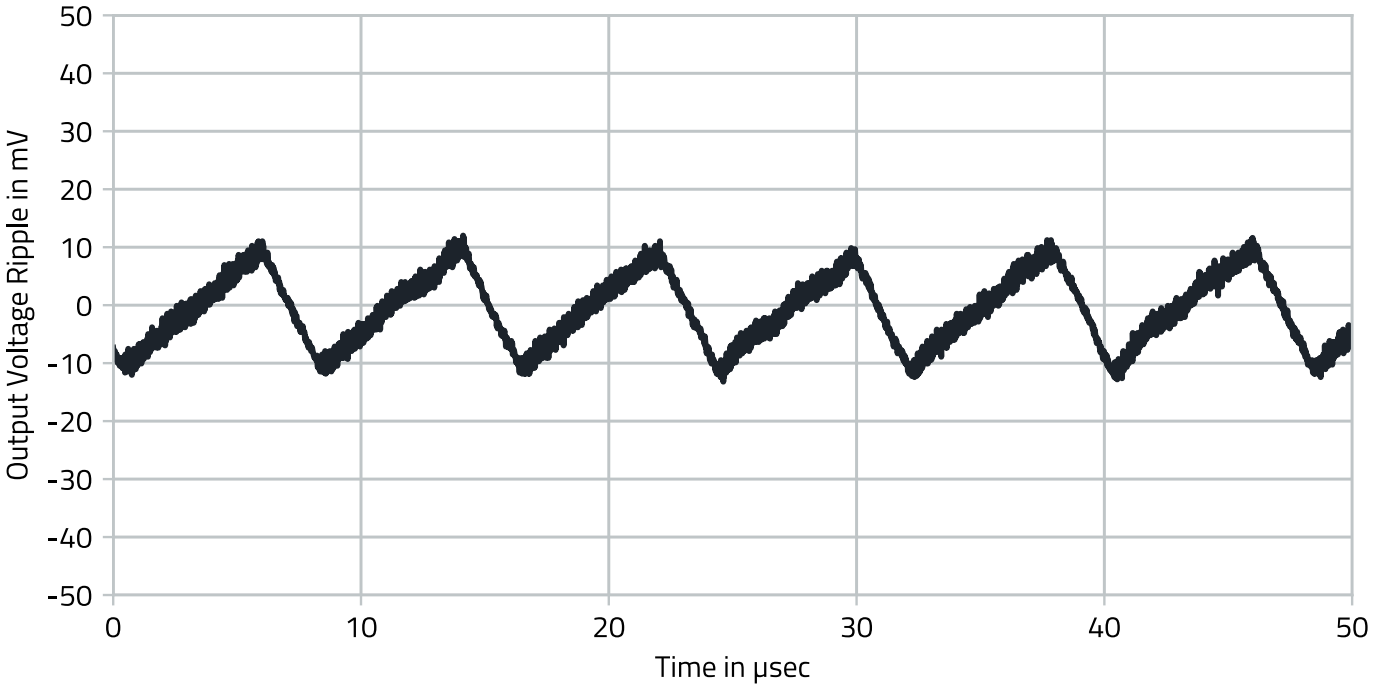


Figure 23: 18024x15401x output voltage ripple V_{CC} = 3.3V, V_{OUT} = 3.3V, I_{OUT} = 75mA.

13.2.5 Thermal Derating

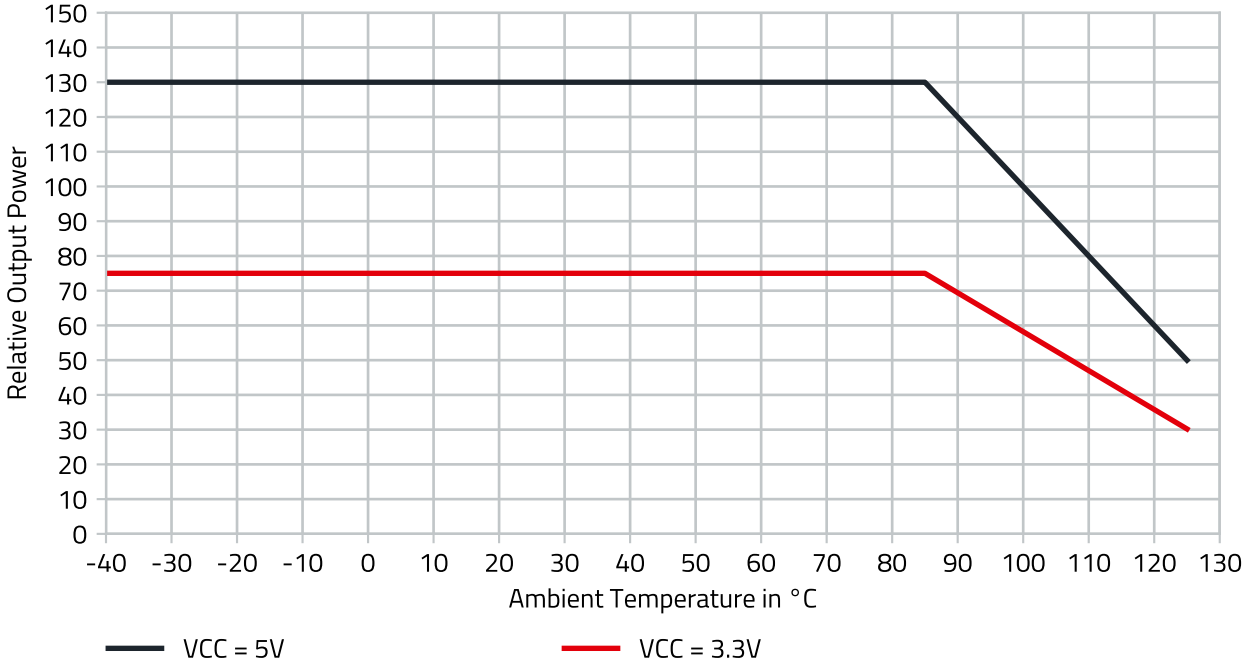


Figure 24: 18024x15401x thermal derating, data rate ≤ 1Mbps.

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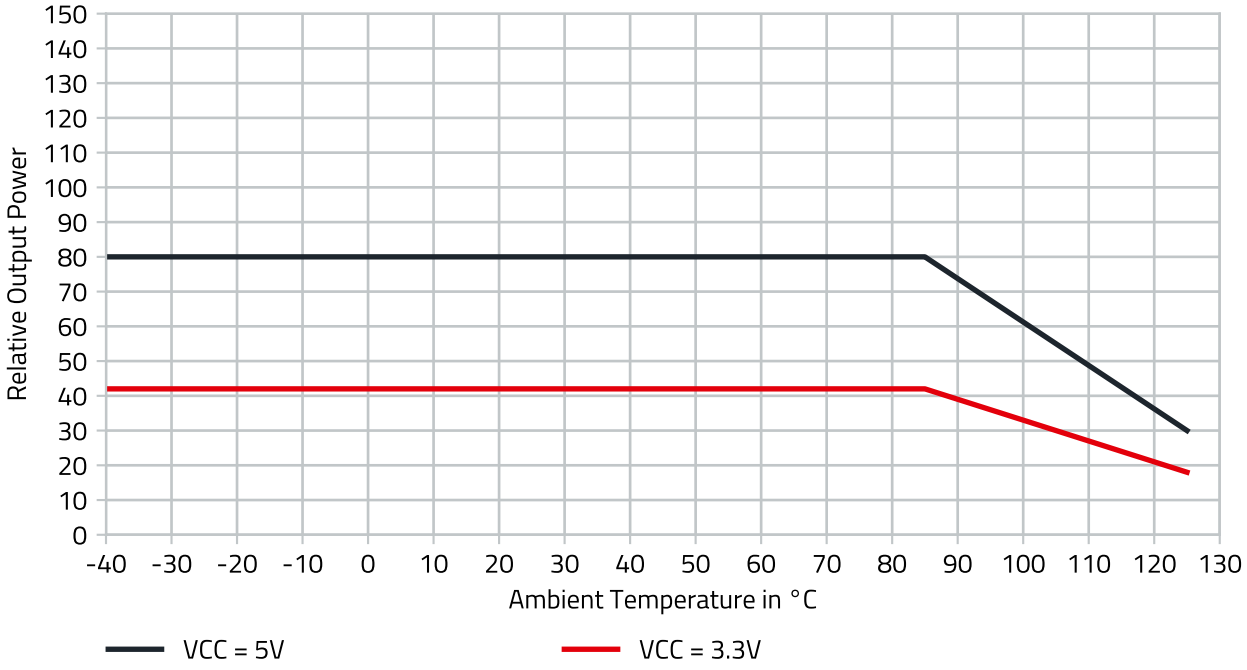


Figure 25: 18024015401x thermal derating, data rate = 100Mbps.

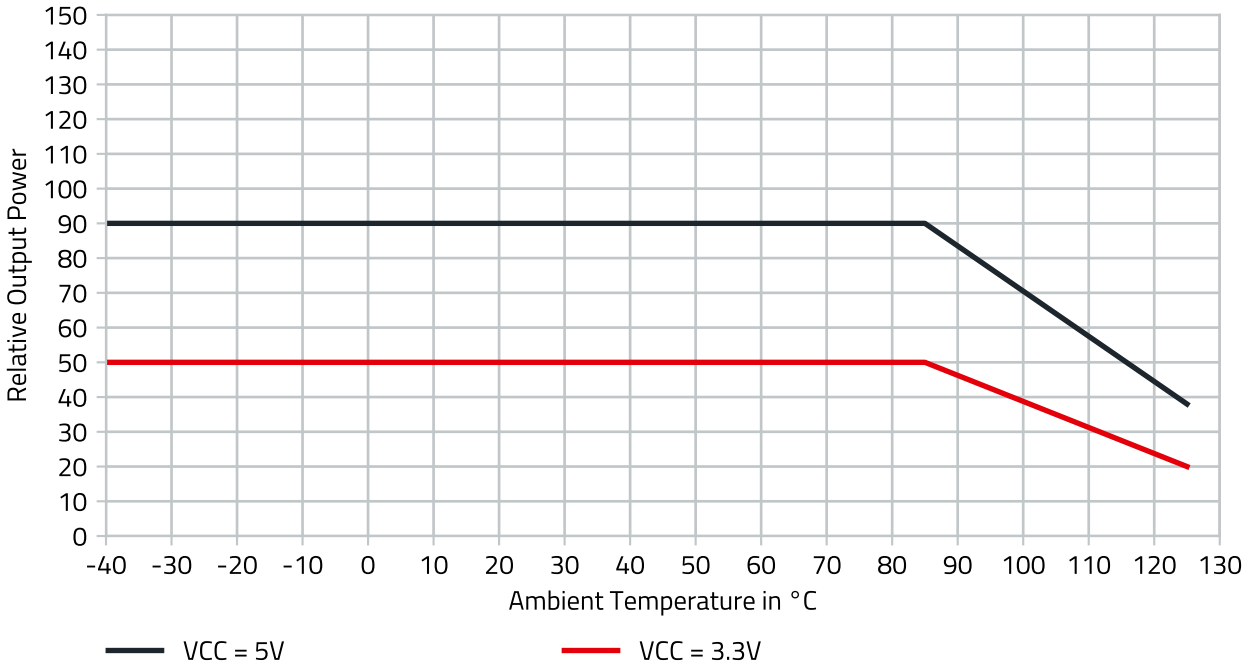


Figure 26: 18024115401x thermal derating, data rate = 100Mbps.

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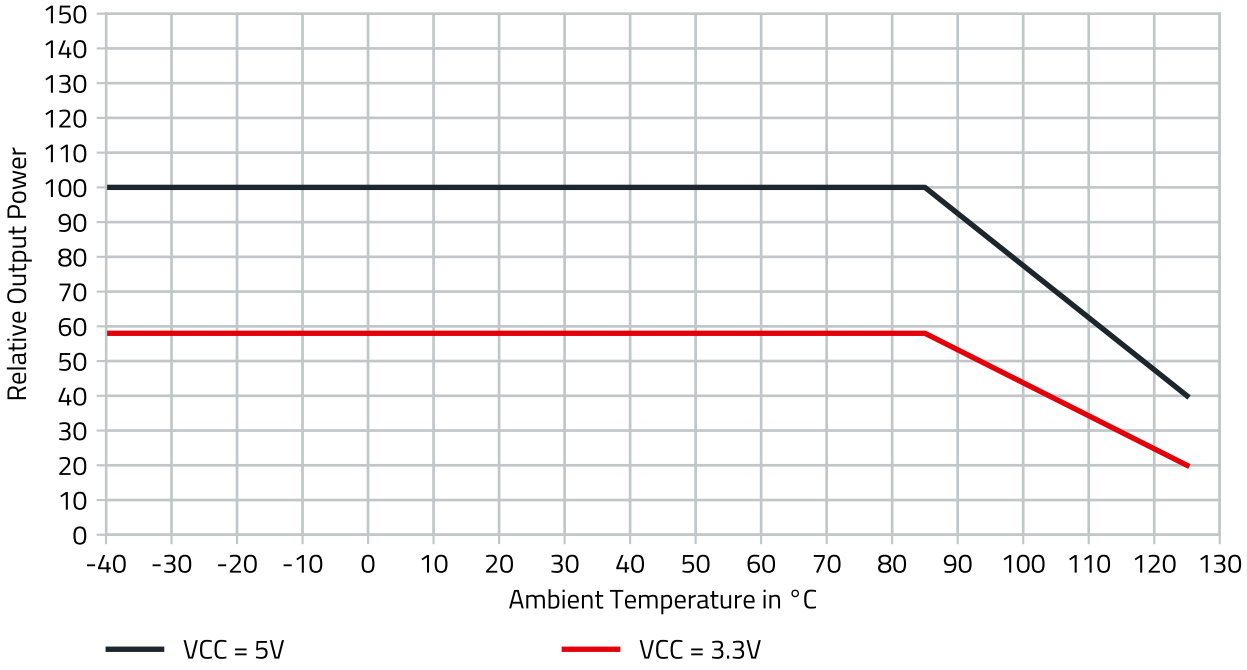


Figure 27: 18024215401x thermal derating, data rate = 100Mbps.

13.2.6 Propagation Delay vs. Ambient Temperature

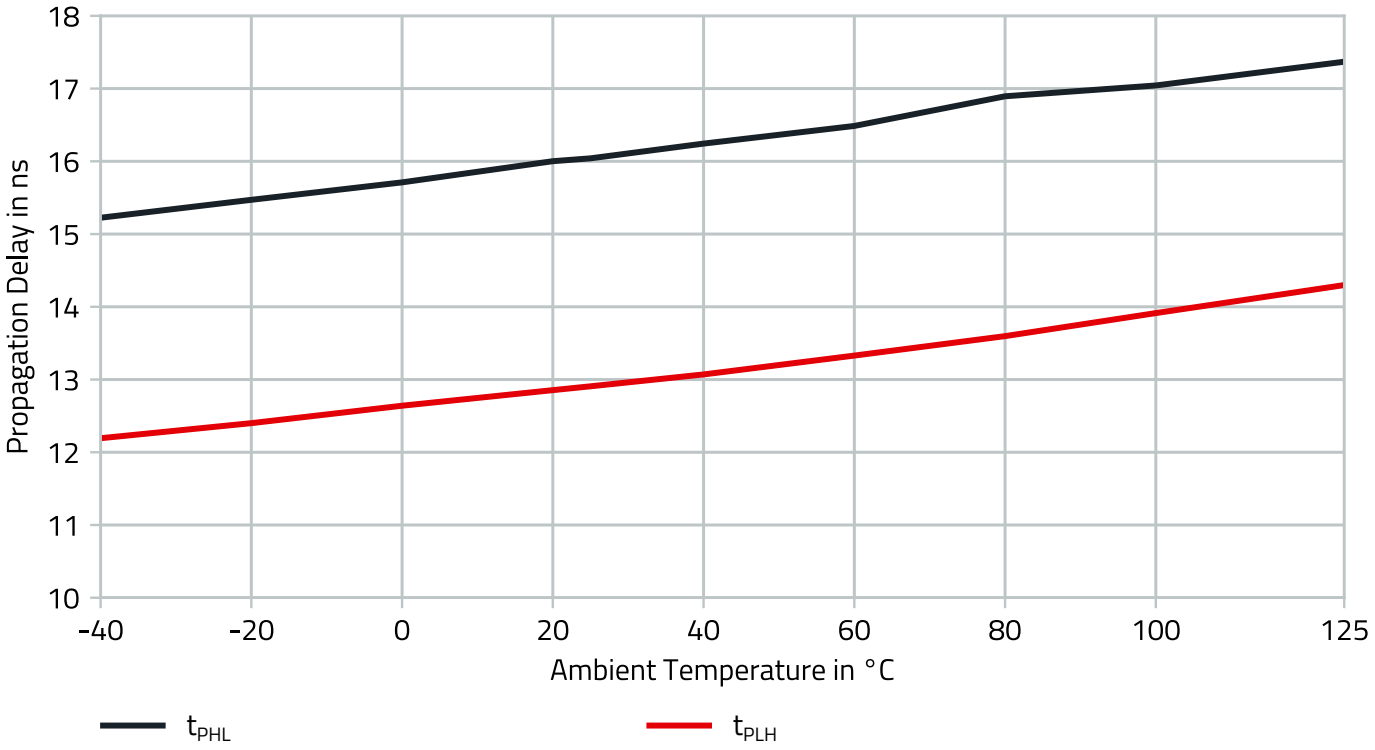


Figure 28: 18024x15401x propagation delay $5V_{CC}$ to $5V_{OUT}$ with C_{LOAD} = 15pF.

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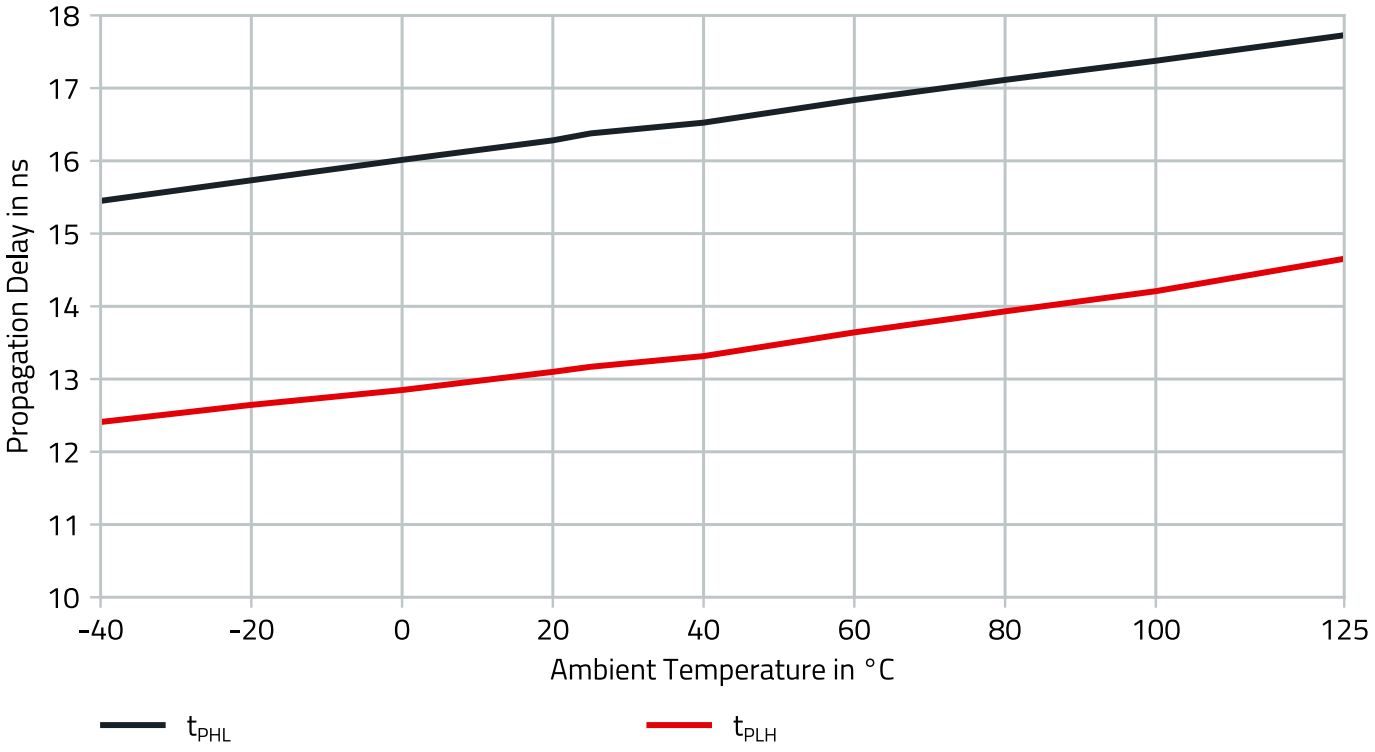


Figure 29: 18024x15401x propagation delay $5V_{CC}$ to $3.3V_{OUT}$ with C_{LOAD} = 15pF.

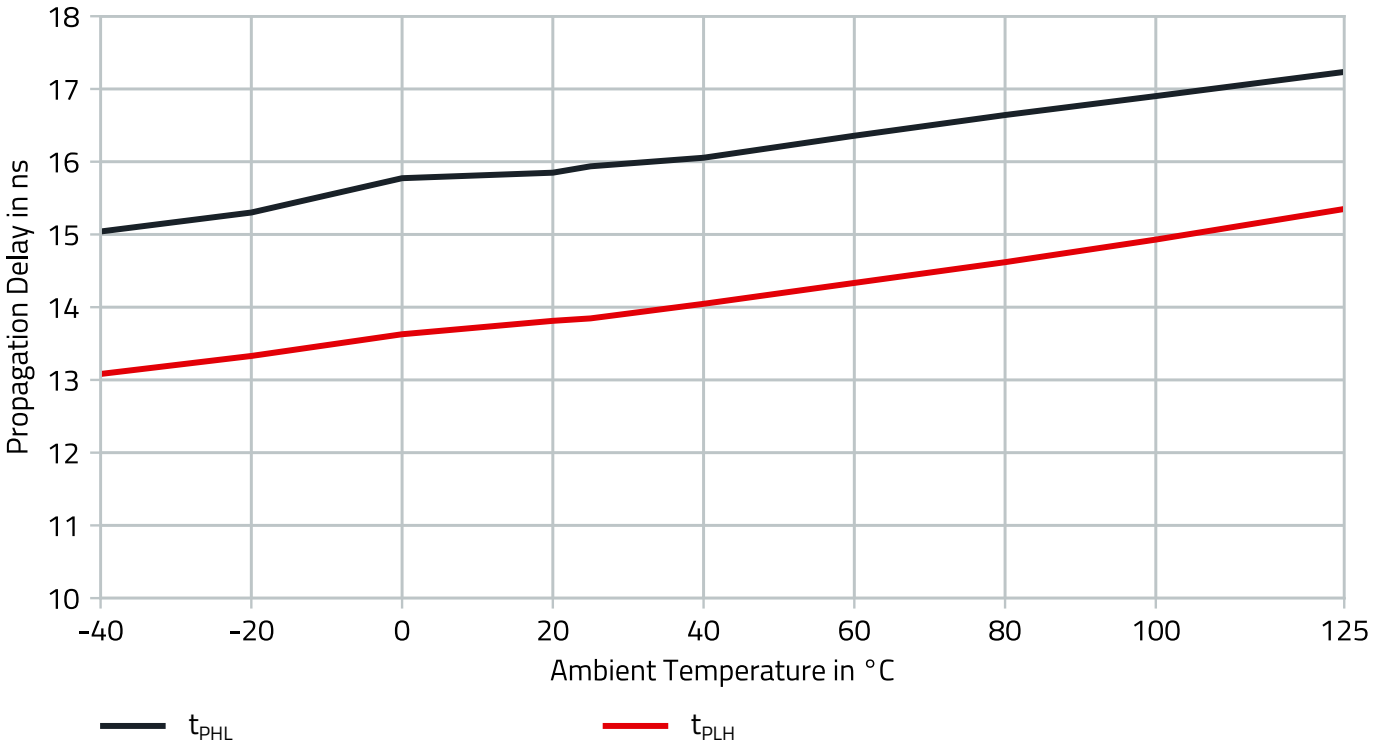


Figure 30: 18024x15401x propagation delay $3.3V_{CC}$ to $3.3V_{OUT}$.

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13.2.7 Quiescent Current vs. Ambient Temperature

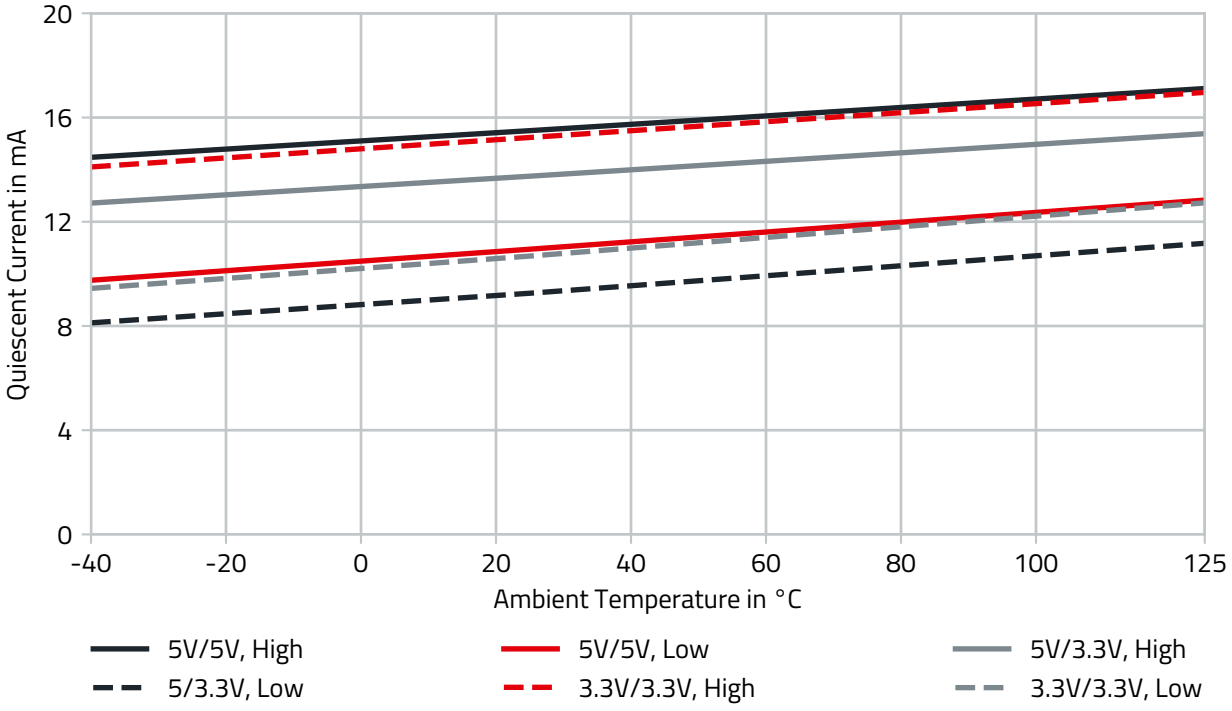


Figure 31: 18024015401L quiescent current, channel inputs set to either high or low.

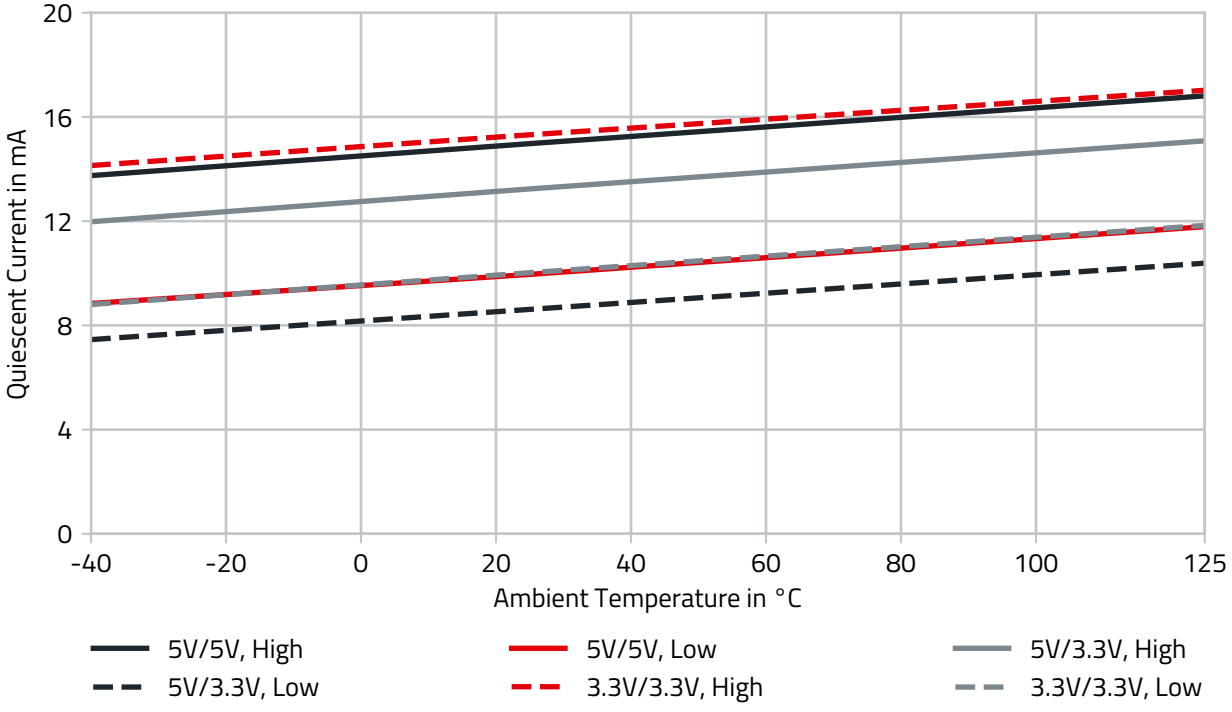


Figure 32: 18024115401L quiescent current, channel inputs set to either high or low.

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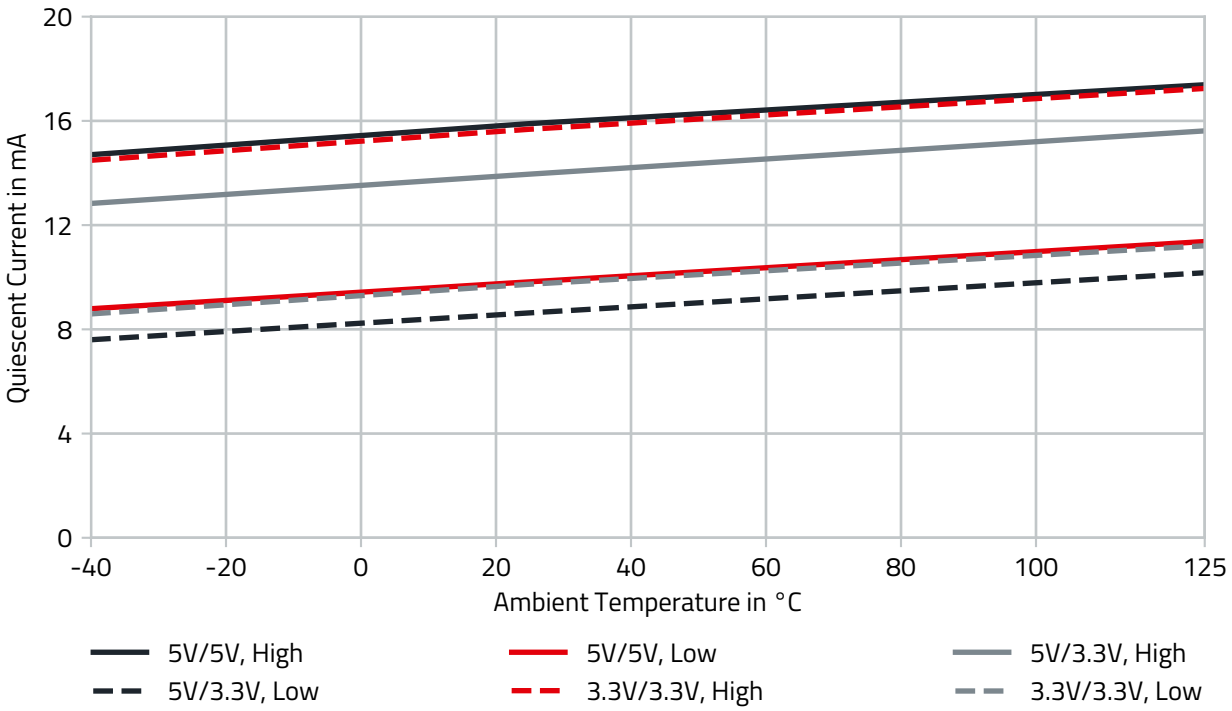


Figure 33: 18024215401L quiescent current, channel inputs set to either high or low.

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13.2.8 Supply Current vs. Ambient Temperature

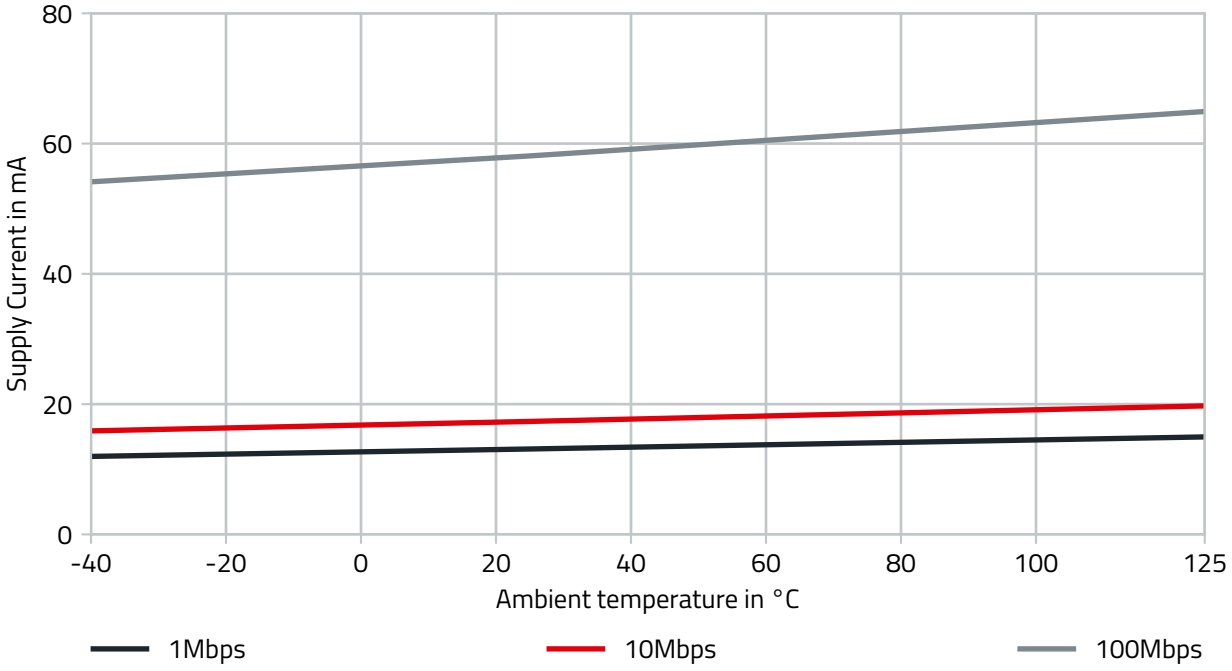


Figure 34: 18024015401x supply current vs. ambient temperature V_{CC} = 5V, V_{OUT} = 5V.

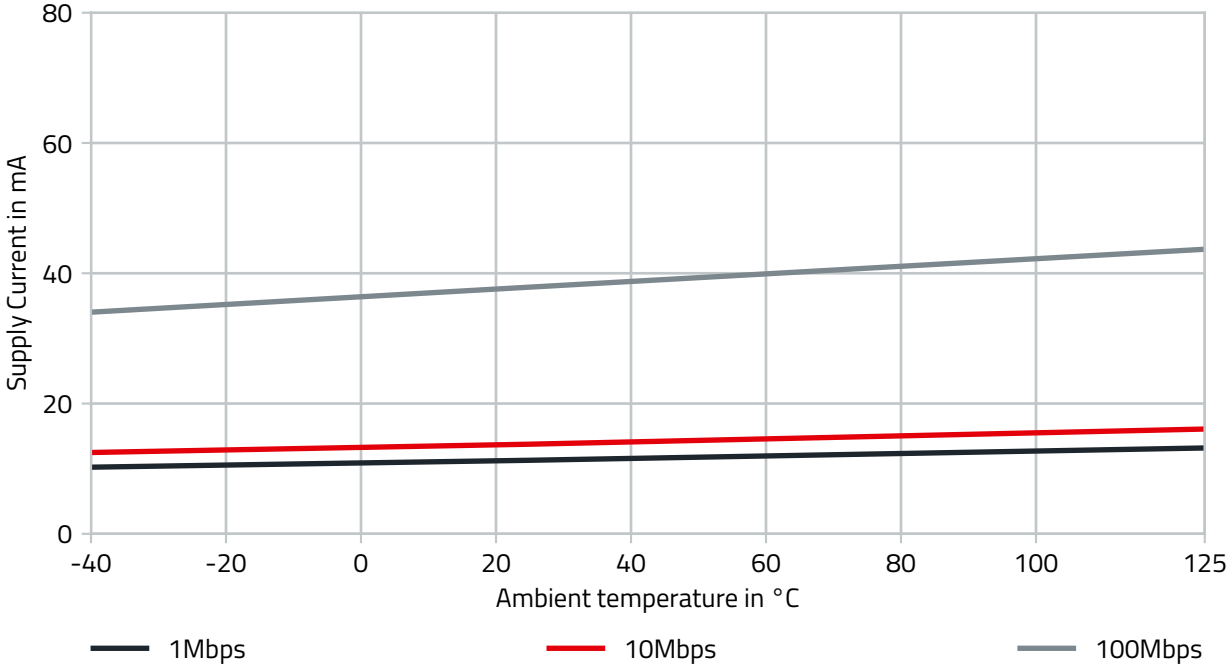


Figure 35: 18024015401x supply current vs. ambient temperature V_{CC} = 5V, V_{OUT} = 3.3V.

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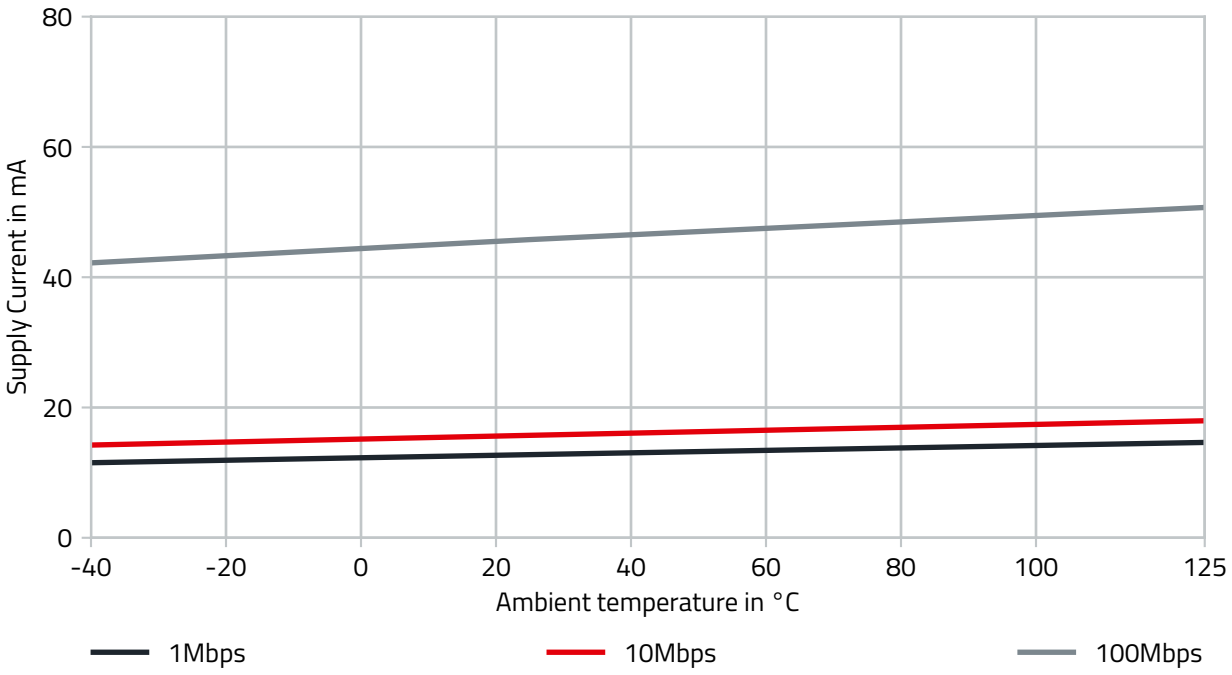


Figure 36: 18024015401x supply current vs. ambient temperature V_{CC} = 3.3V, V_{OUT} = 3.3V.

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13.2.9 Supply Current vs. Data Rate

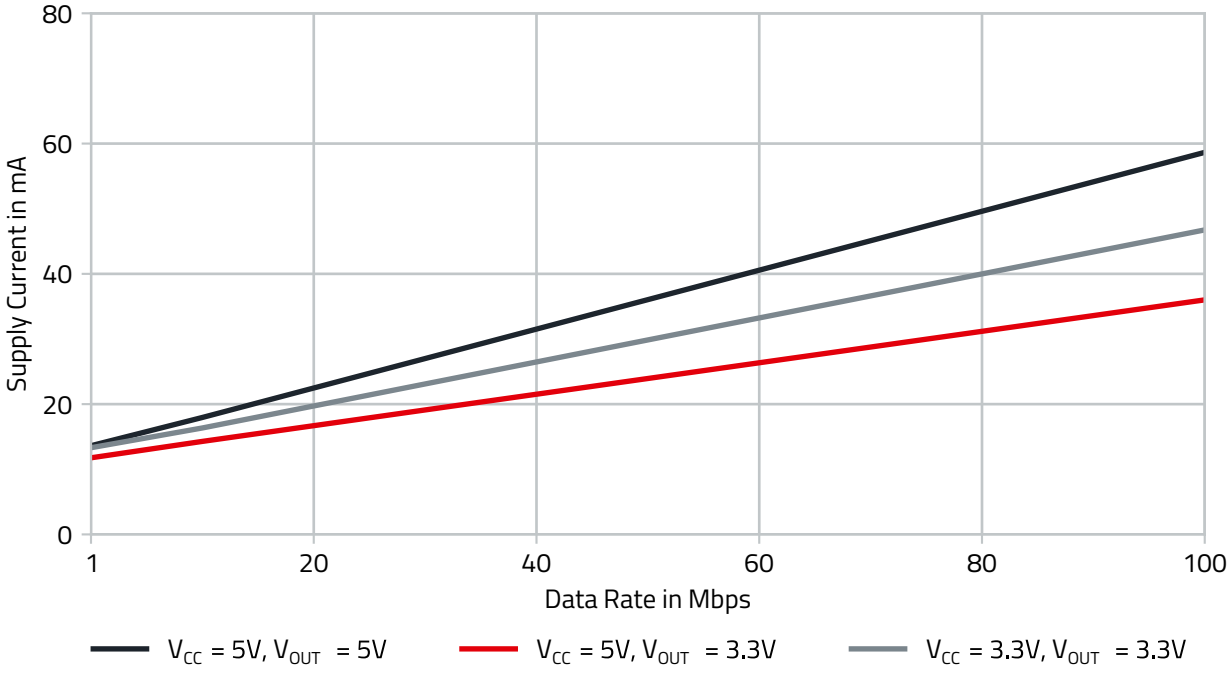


Figure 37: 18024015401x supply current vs. data rate.

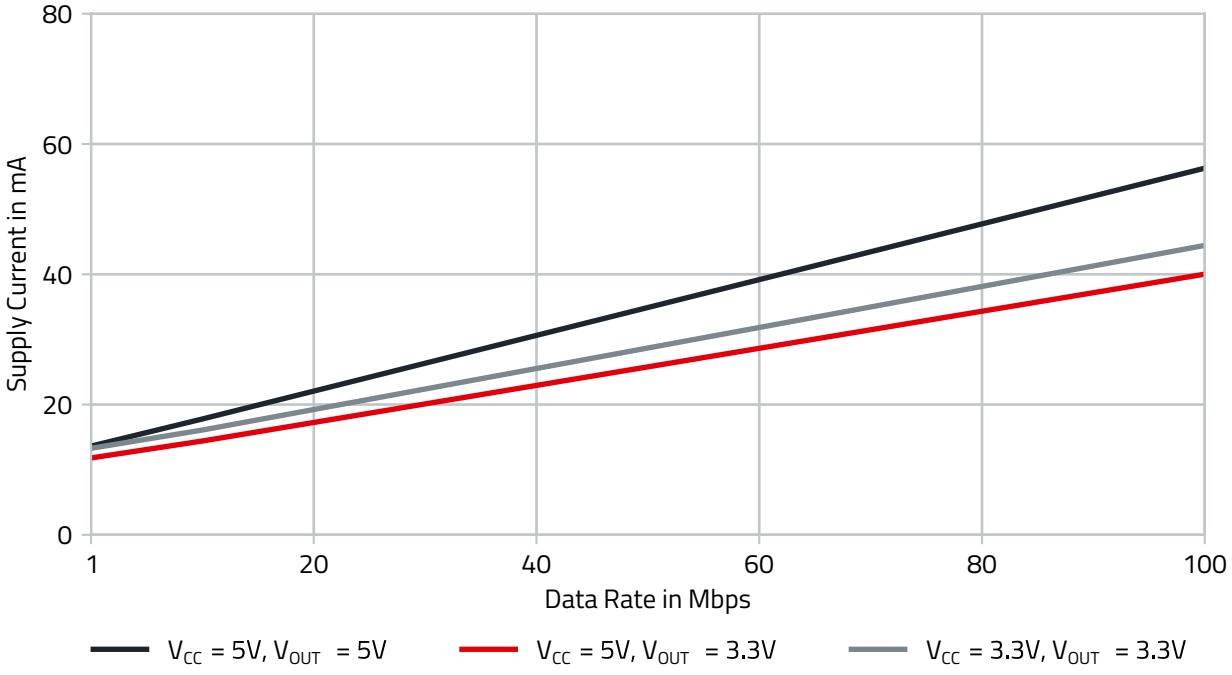


Figure 38: 18024115401x supply current vs. data rate.

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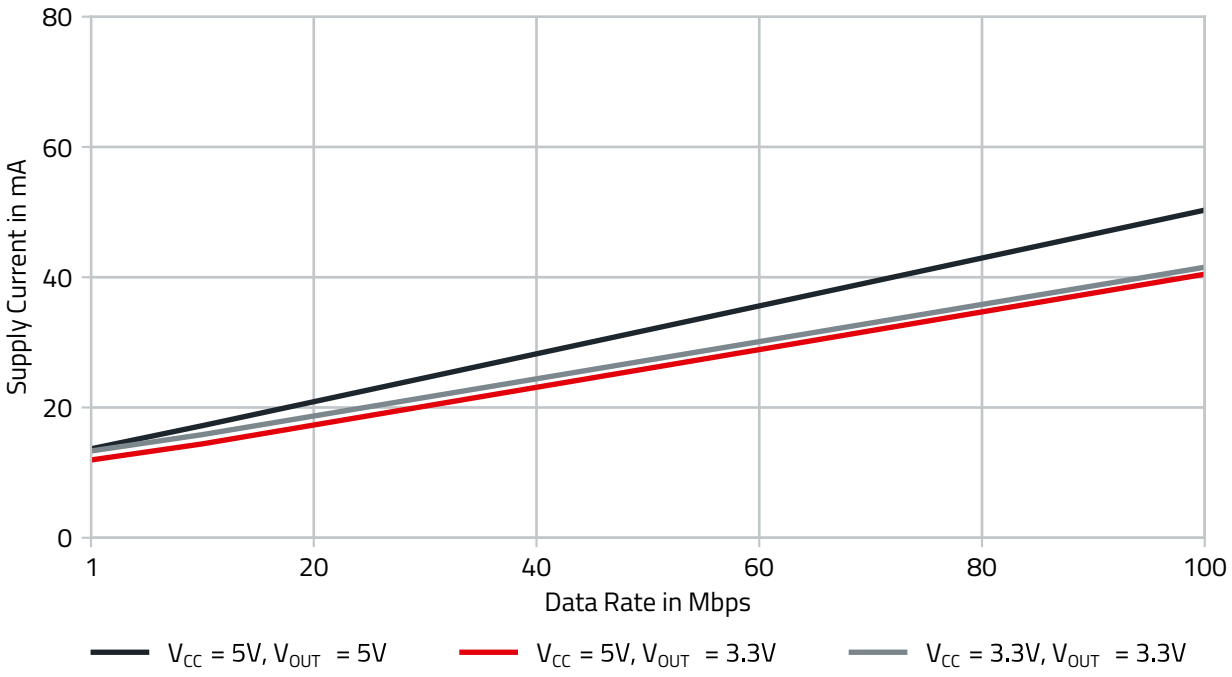


Figure 39: 18024215401x supply current vs. data rate.

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13.2.10 High and Low Voltage Levels vs. Output Current

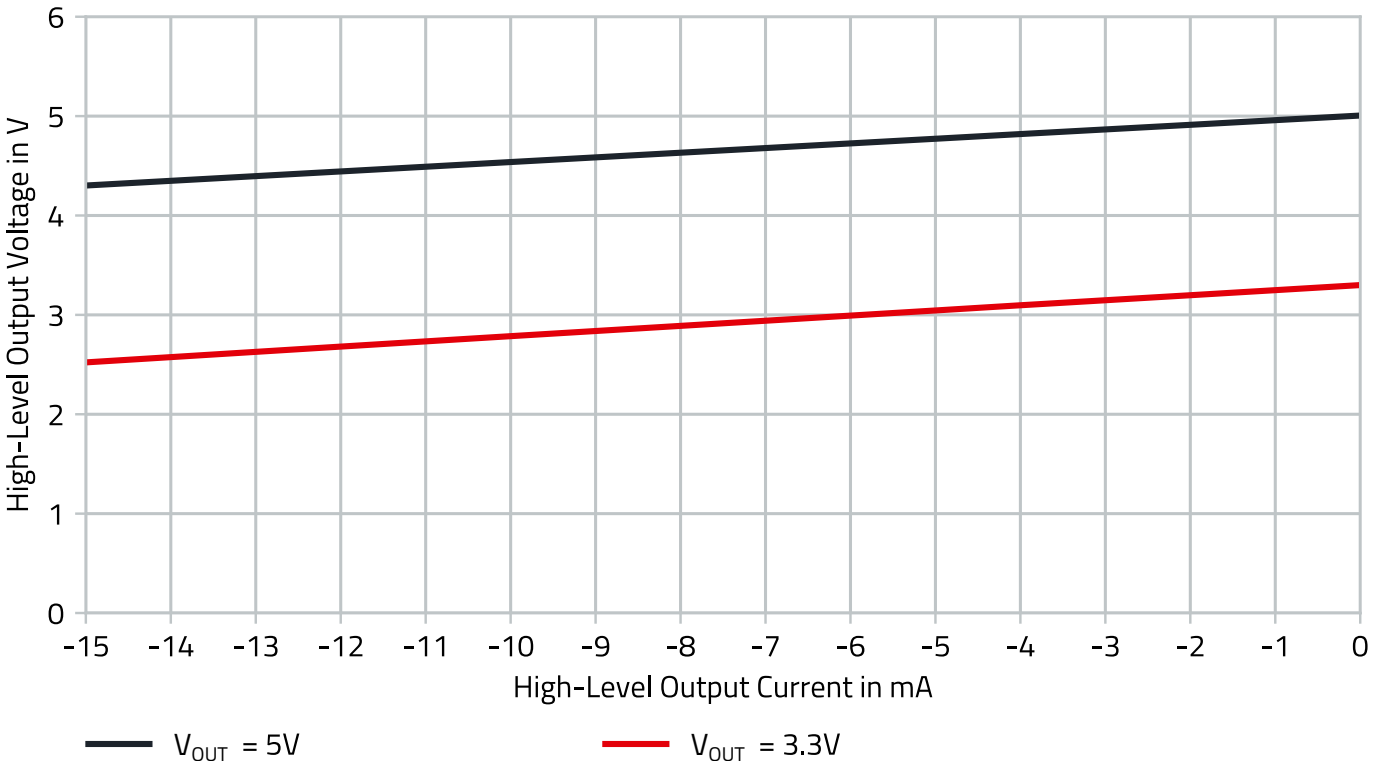


Figure 40: 18024x15401x high-level output voltage vs. high-level output current.

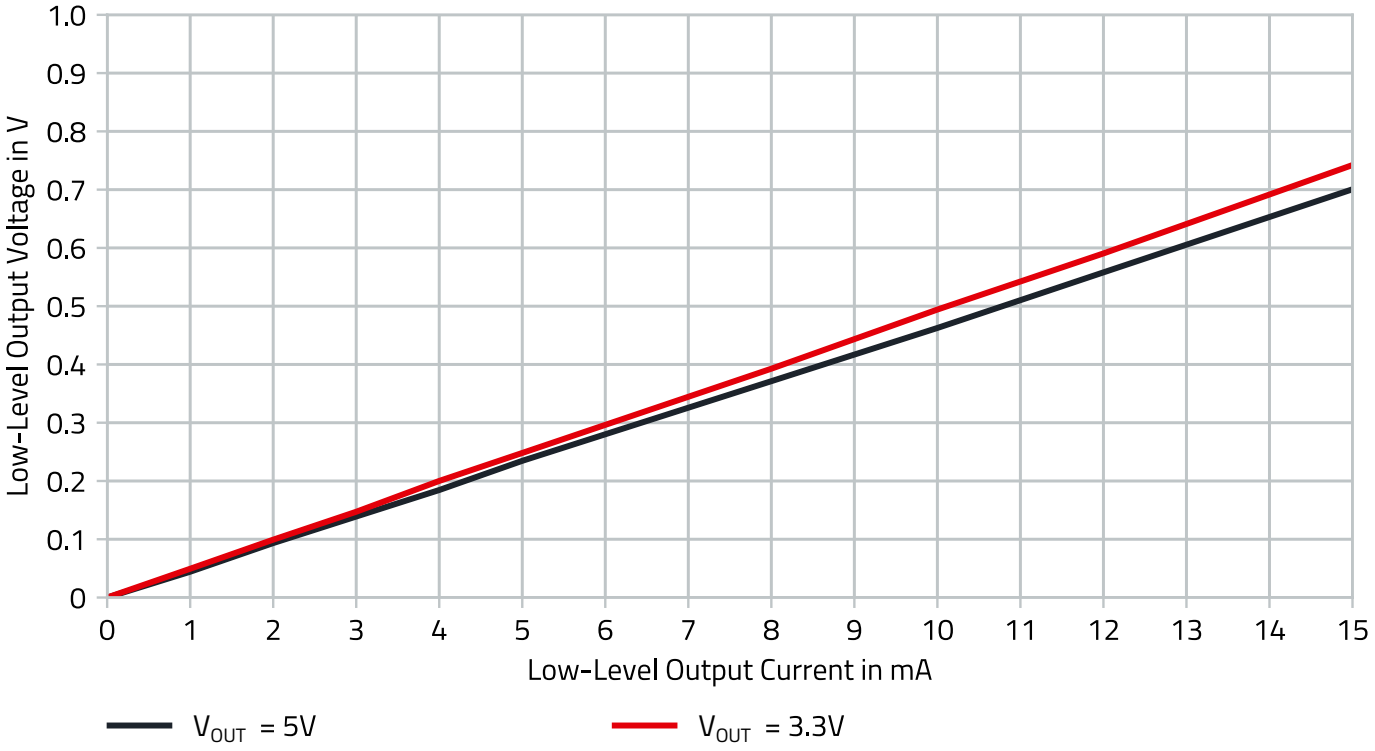


Figure 41: 18024x15401x low-level output voltage vs. low-level output current.

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13.2.11 Safety Limiting Curves

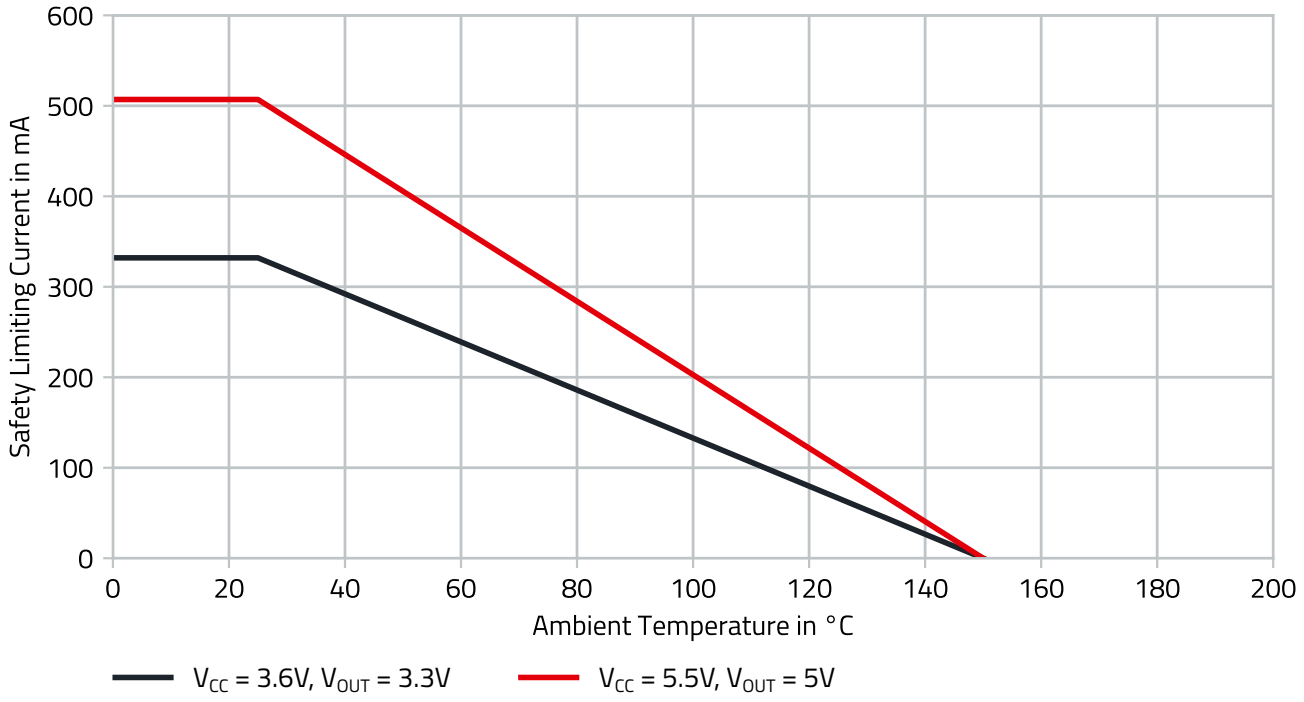


Figure 42: 18024x15401x safety limiting current.

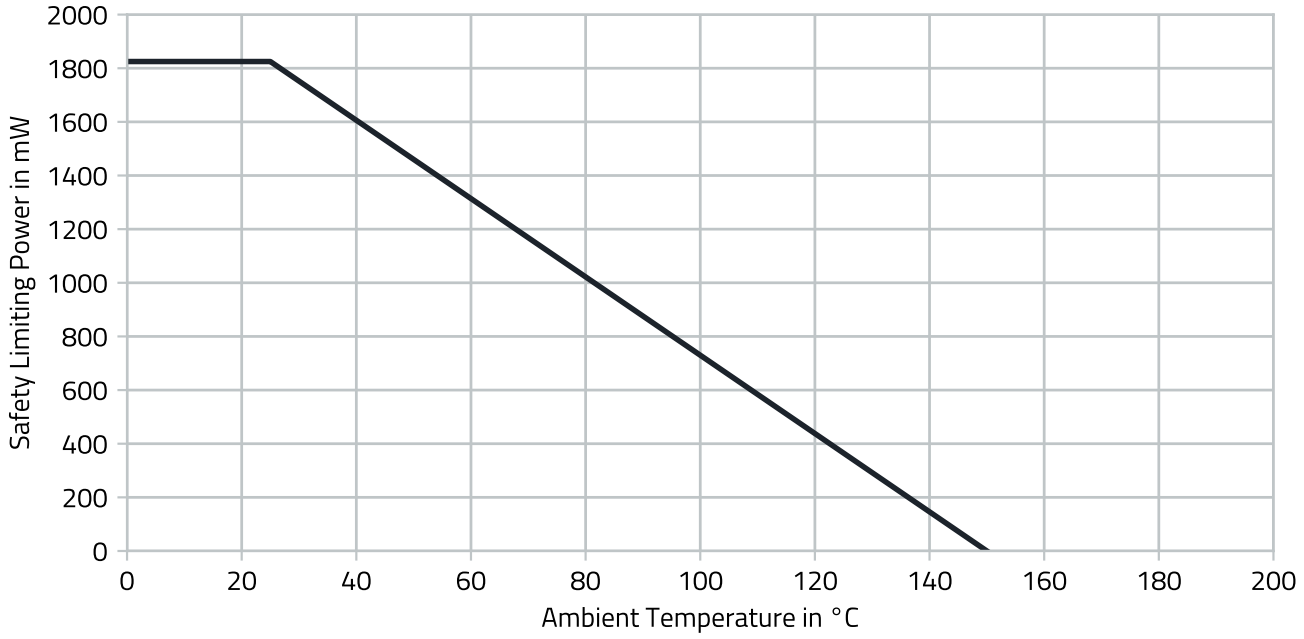


Figure 43: 18024x15401x safety limiting power.

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14 I/O TRUTH TABLE

Table 15: Truth table.

V_{CC}	Input V_{INX}	Output V_{OUTX}	Operation
≥ 3.15V	H	H	Normal operation mode: The channel output follows the logic state of its input
	L	L	
	Open	Default	Default mode: When input V_{INX} is open, the corresponding channel output goes to its default logic state.
≤ 2.0V	X	Undetermined	If the V_{CC} is unpowered, the channel output is undetermined

X = Don´t care; H = High level; L = Low level. The outputs are in undetermined state when V_{CC} < 2.0V

15 I/O DESCRIPTION

Table 16: IO schematics.

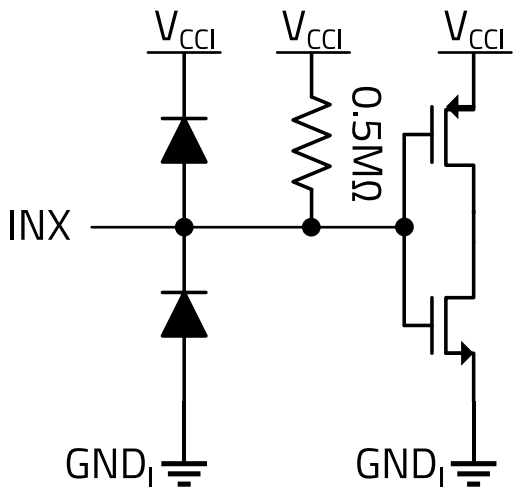


Figure 44: Default high channel input internal structure.

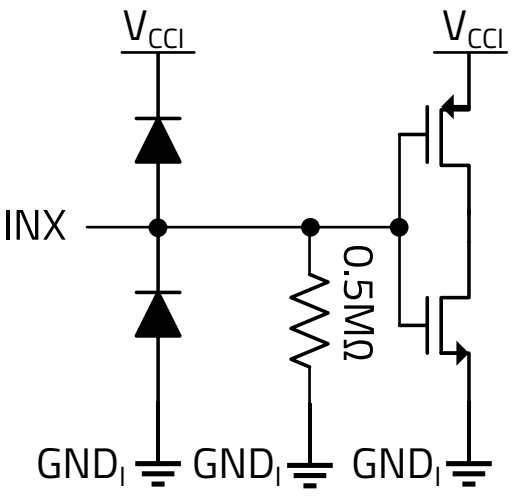


Figure 45: Default low channel input internal structure.

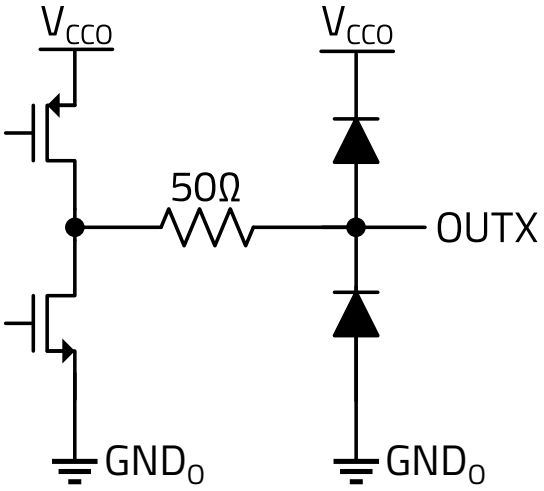


Figure 46: Channel output internal structure.

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16 TEST SCHEMATICS

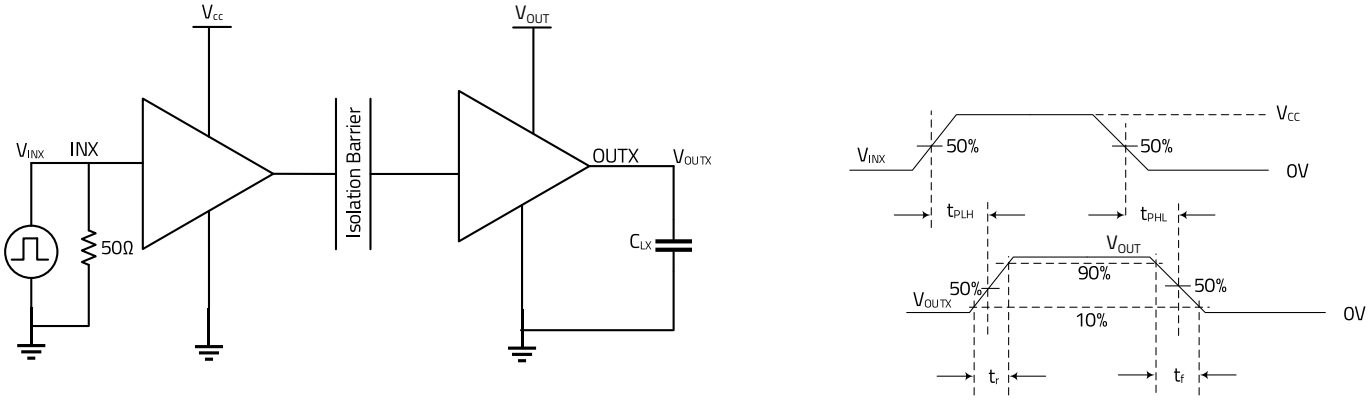


Figure 47: Propagation delay test schematic.

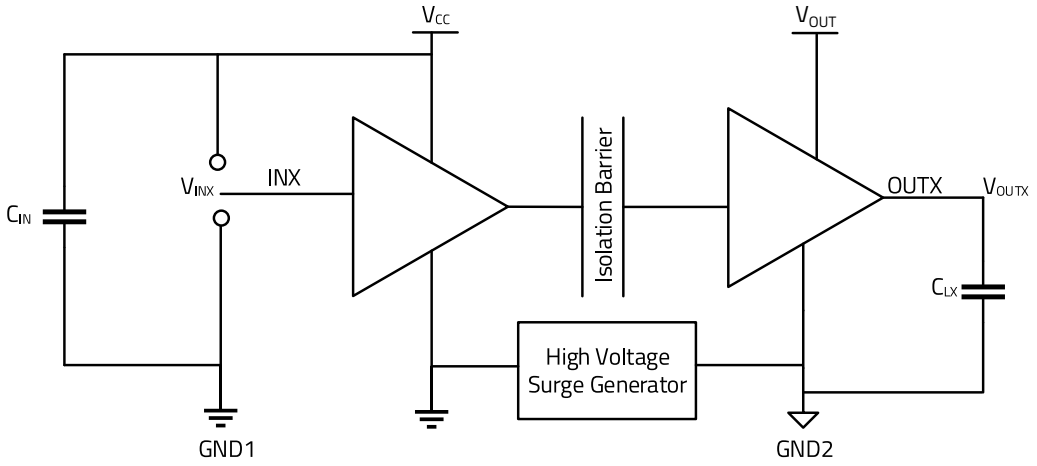


Figure 48: CMTI test schematic.

Note: C_{LX} = 15 pF and includes instrumentation and fixture capacitance within ±20%.

17 BLOCK DIAGRAM

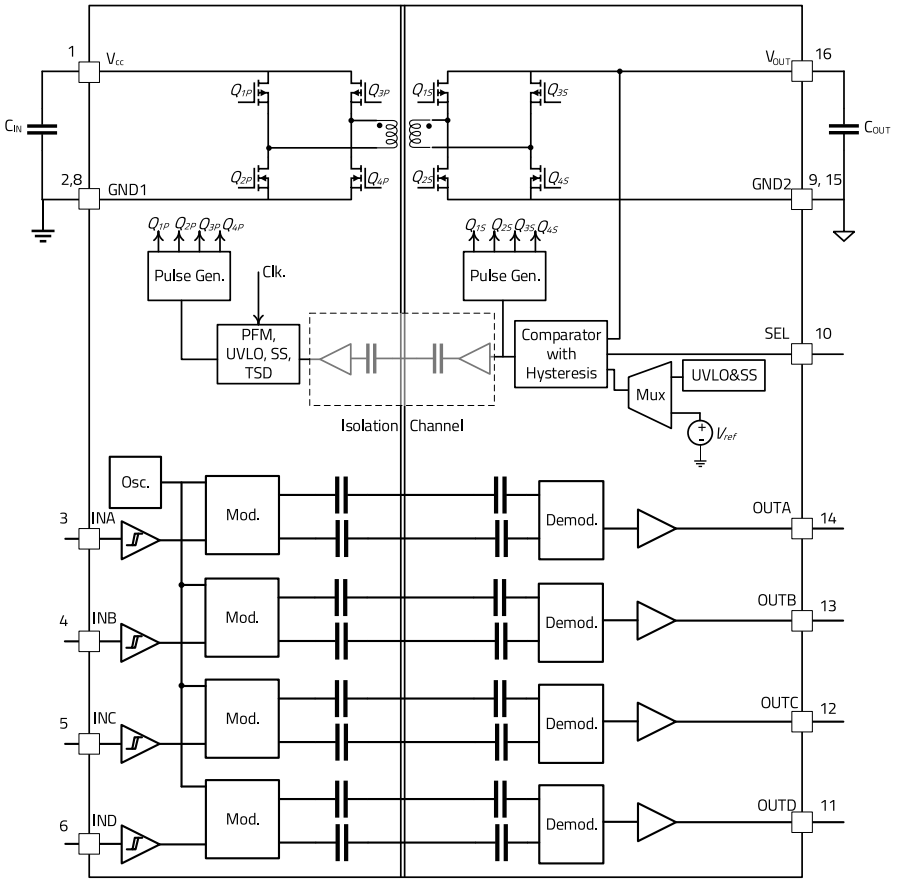


Figure 49: 18024015401x block diagram.

18 CIRCUIT DESCRIPTION

The WPME-CDIP digital isolator with integrated power consists of four capacitive isolated digital channels that are powered internally by an integrated dc-dc power module. The power module integrates primary and secondary side controllers, primary and secondary full bridges and a very high frequency transformer. The WPME-CDIP integrates the isolation capacitors in addition to the modulators and demodulators needed to construct the four isolated channels.

The output voltage of the integrated power module (V_{OUT}) is regulated through pulse frequency modulation (PFM). The output voltage is compared to an internal secondary side reference. When the output voltage is higher than the reference value, the primary and secondary switches are disabled. When the output voltage is lower than the internal reference with hysteresis, the comparator produces a high output signal, which enables the pulses on both the primary and secondary sides. The pulses are of a fixed frequency of around 13MHz with 50% duty cycle. The comparator signal is transferred to the primary side through an additional isolated channel. This channel is not accessible from the outside of the module. The SEL pin is used to choose between two different fixed output voltages, 3.3V or 5V. The integrated power module integrates soft start, undervoltage lockout, short-circuit protection, overcurrent protection and thermal shutdown protection features. The integrated power module only requires external input and output capacitors for functionality.

The isolation channels are realized using on/off key (OOK) modulation to transmit high or low speed signals through silicon dioxide isolation barriers. The on-chip oscillator is used to modulate the schmitt-triggered input signal. The modulator generates a differential signal that is transmitted through the capacitive isolation lines. The demodulator is located on the output side of the signal channel and used to amplify, filter and reconstruct the input signal with minimum propagation delay and distortion. Finally, the output of the demodulator is given to the output through buffer to improve the driving strength.

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19 PROTECTION FEATURES

19.1 Soft-Start

When the input voltage applied at the primary side of the dc-dc power module reaches the UVLO rising threshold (typ. 2.75V) the primary controller starts to operate and send pulses to the primary side full bridge. The output voltage starts to rise through charging of the output capacitor through the body diodes of the secondary side bridge rectifier. When the output voltage reaches the UVLO rising threshold (typ. 2.75V) the secondary side controller starts to give pulses to the secondary side bridge rectifier and the output voltage tracks the linear internal reference to achieve a soft-start time of 1ms. When the output voltage gets close to the desired set point the soft-start mode is over and the output voltage is kept in regulation by the normal voltage reference on the secondary side controller.

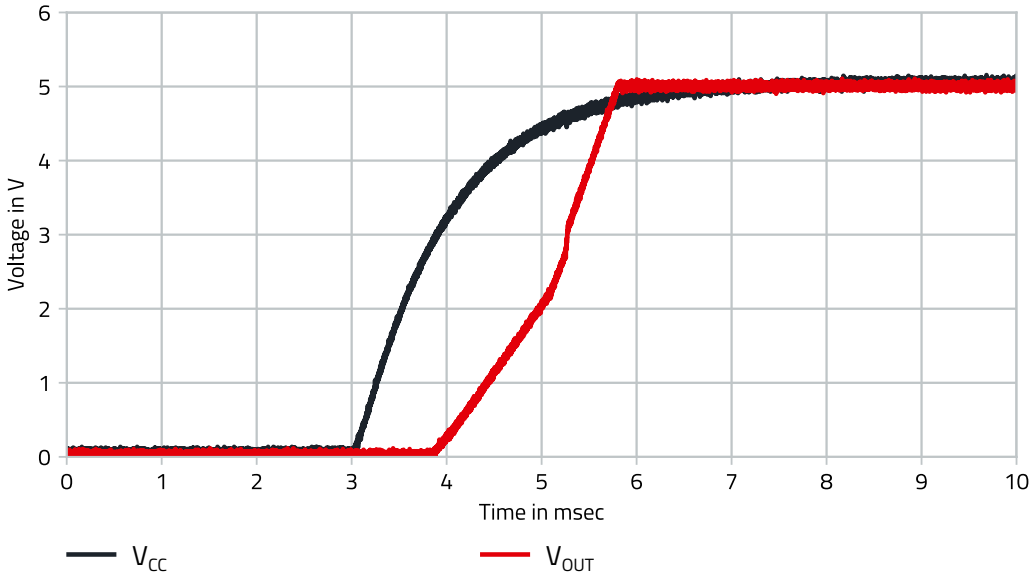


Figure 50: 18024x15401x soft-start.

19.2 Overcurrent Protection (OCP)

The overcurrent protection feature is realized through the resistance of the primary and secondary switches and windings. If the output current increases above certain limit the output voltage starts to drop and to limit the power losses within the converter. When the output voltage continues to drop to the short-circuit protection limit the hiccup mode kicks in as described before.

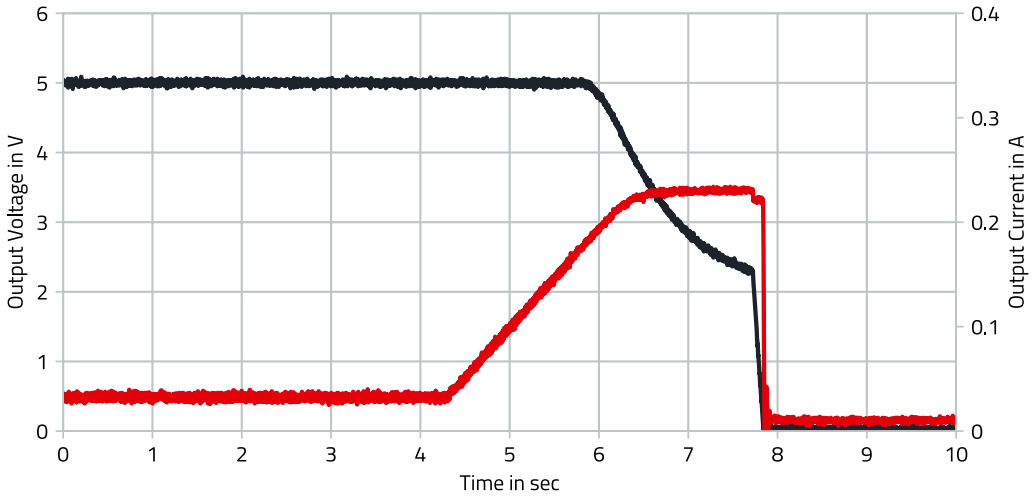


Figure 51: 18024x15401x overcurrent protection.

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19.3 Short-Circuit Protection (SCP)

The integrated power module implements short-circuit protection feature through hiccup operation. The output voltage is continuously monitored and when it drops below a certain threshold, the PFM controller stops switching for 4ms. After the 4ms time period is finished the controller soft-starts the converter again. If the output voltage reaches the desired value within the soft-start design value of 1ms that means the short-circuit is removed and the converter continues its normal operation. If the output voltage cannot reach the desired value within 1ms the converter goes again into hiccup mode.

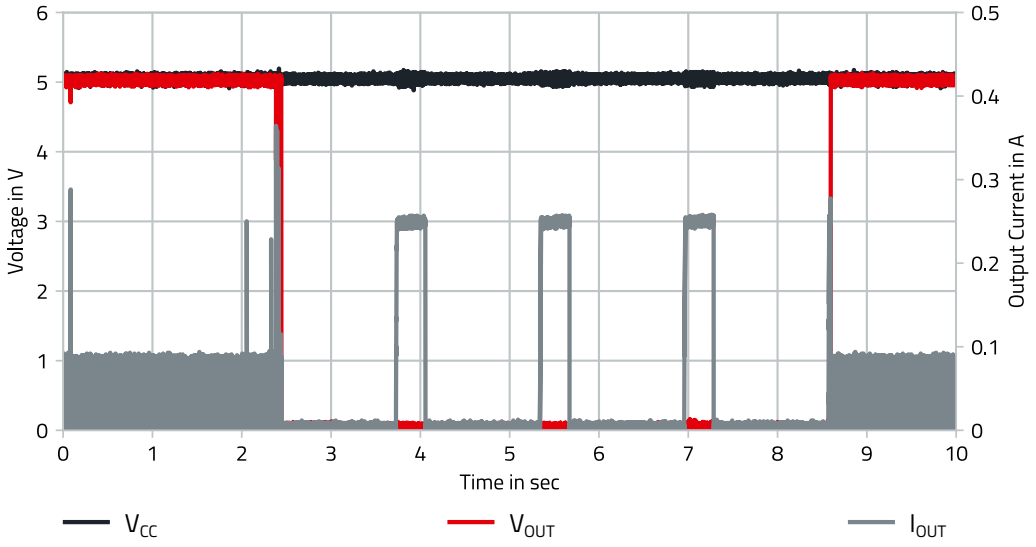


Figure 52: 18024x15401x short-circuit protection.

19.4 Input/Output Undervoltage Lockout (UVLO)

The device incorporates input and output undervoltage lockout (UVLO) to protect from unexpected behavior at input voltages below the recommended values. Beyond this value the gating pulses for the secondary and primary side full bridges are inhibited. The thresholds of the UVLO are indicated in the ELECTRICAL SPECIFICATIONS.

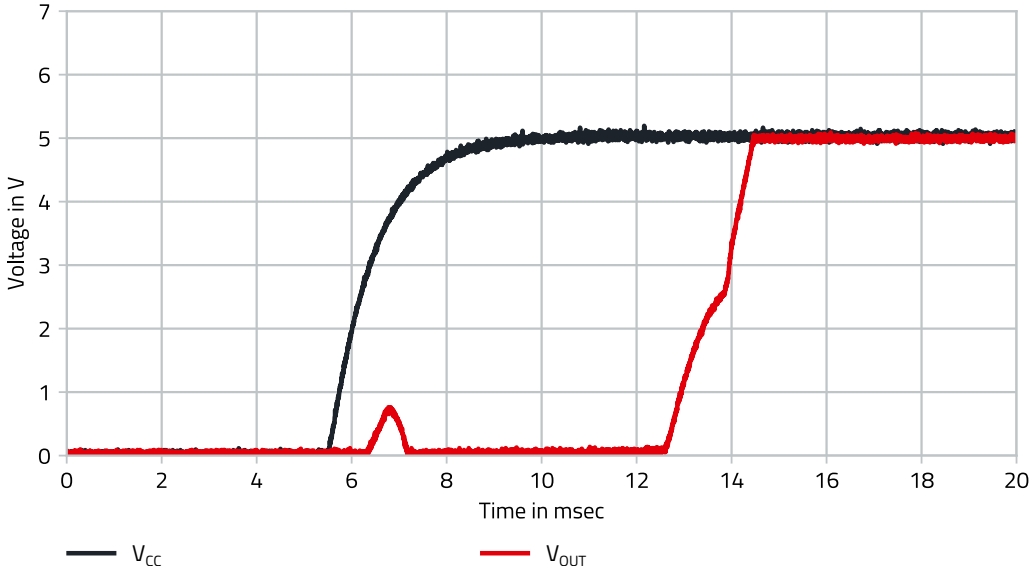


Figure 53: 18024x15401x input/output undervoltage lockout.

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19.5 Overtemperature Protection (OTP)

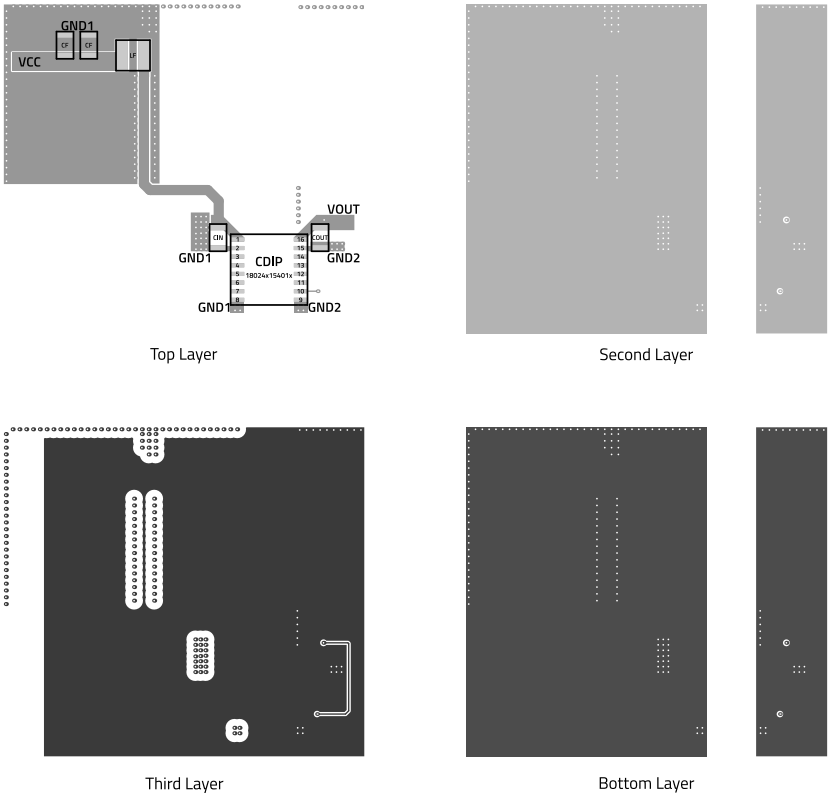
Thermal protection helps prevent catastrophic failures due to accidental device overheating. The junction temperature of the power module should not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal thermal shutdown circuit, which activates when the junction temperature reaches 180 °C (typ). Under the thermal shutdown condition the primary side controller prohibits the gating pulses of the primary side full bridge, causing the output voltage to drop. When the junction temperature falls below 140 °C (typ) the internal soft-start is released, V_{OUT} rises smoothly, and normal operation resumes.

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20 DESIGN EXAMPLE

The design example shows a possible solution for an input voltage range of 3.15V to 5.5V to 5V or 3.3V and with a max. POUT of 0.65W. All of the necessary components to fullfill the requirements of the CISPR 32 EMI conducted- and radiatedemissions tests are included in the design example. It passes the conducted emissions class B with 0.8m input- and 1m output lines and passes the radiated emissions class B in a FAR at 3m measurement distance with 0.8m horizontal, 0.8m vertical input- and 1m horizontal output lines. In the final application filter components may be omitted depending on the requirements.

20.1 Layout



Top Layer | Second Layer

Third Layer | Bottom Layer

The layout above has been evaluated to provide the optimal performance in terms of signal performance, transient response, efficiency, output ripple and EMI. The design footprint can be reduced but only at the expense of performance in these parameters. The following recommendations should be followed when designing the layout:

1. 1. Signal traces should be impedance matched to 50W, especially if the trace length exceeds l*1/16.
2. A reference GND should always be placed below any signal traces.
3. The input and output capacitors should be placed as close to the VCC and VOUT pins as possible.
4. The filter components should be placed as far from the device as possible.
5. Any feature traces, such as SEL, should be routed between layers 2 and 4 to avoid interrupting signal references.
6. Avoid sharp corners when routing signal traces.

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20.2 Schematic

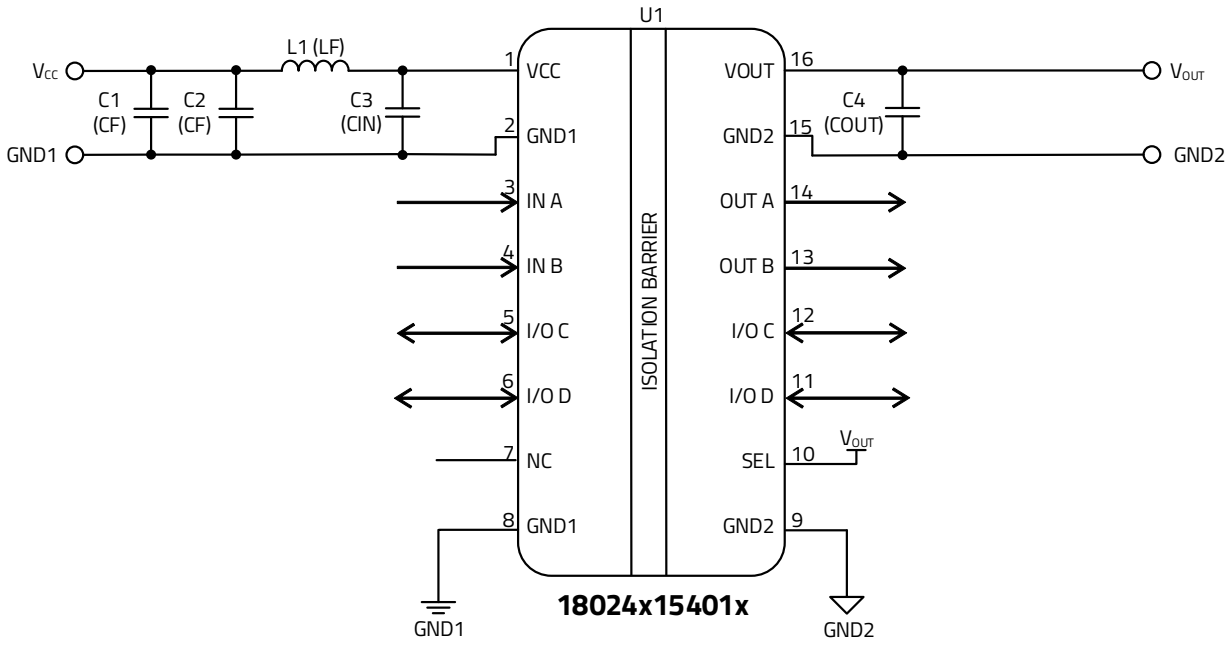


Figure 54: 18024x15401x design example schematic.

20.3 Bill of Materials

Table 17: 18024x15401x design example bill of materials.

DESIGNATOR	DESCRIPTION	FUNCTION	QUANTITY	ORDER CODE	MANUFACTURER
U1	Digital Isolator	Digital Isolator	1	18024x15401x	WE
L1	Filter inductor, 4.7µH, PD2 family, I_{SAT} = 2.46A, I_R = 1.82A	Input Filter	1	744773047	WE
C1, C2, C3, C4	Ceramic chip capacitor 10µF/16V X7R, 1210	Input and Output Filter	1	885012209014	WE

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21 TYPICAL APPLICATION

The figure below depicts a typical application for a digital isolator used in serial port interface (SPI) communication between a microcontroller and analog to digital converter (ADC). The digital isolator has an integrated power module which can be used to power the ADC.

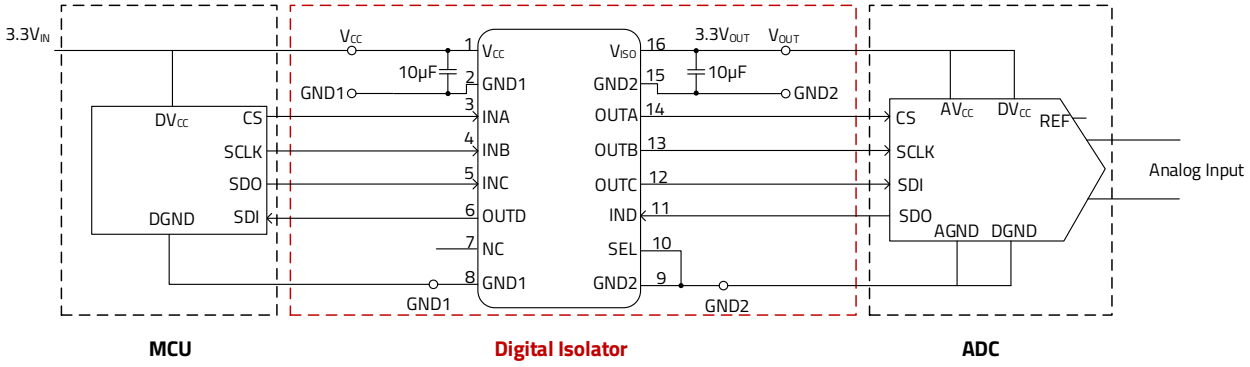


Figure 55: Typical application: SPI bus.

The 18024115401H and 18024115401L are shown in the above diagram in a conventional SPI implementation. The channel configuration allows for appropriate isolation and communication between the controller and peripheral.

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22 HANDLING RECOMMENDATIONS

1. The digital isolator is classified as MSL3 (JEDEC Moisture Sensitivity Level 3) and requires special handling due to moisture sensitivity (JEDEC J-STD033D).
2. The parts are delivered in a sealed bag (Moisture Barrier Bag = MBB) and should be processed within one year.
3. When opening the moisture barrier bag, check the Humidity Indicator Card (HIC) for the color status. Bake parts prior to soldering in case indicator color has changed according to the notes on the card.
4. Parts must be processed after 168 hour (7 days) of floor life. Once this time has been exceeded, bake parts prior to soldering per JEDEC J-STD033D recommendation.
5. Maximum number of soldering cycles is two.
6. For minimum risk, solder the device in the last solder cycle of the PCB production.
7. The component lead material is copper (Cu) and the lead finish is Matte Tin (Matte Sn).
8. For solder paste use a standard SAC Alloy such as SAC 305, type 3 or higher.
9. The profile below is valid for convection reflow only.
10. Other soldering methods (e.g. vapor phase) are not verified and have to be validated by the customer at their own risk.

22.1 Soldering Profile

Table 18: Reflow solder profile.

Profile Feature	Symbol	Value
Preheat temperature minimum	T_{s_min}	150 °C
Preheat temperature maximum	T_{s_max}	200 °C
Preheat time from T_{s_min} to T_{s_max}	t_s	60-120 seconds
Liquidous temperature	T_L	217 °C
Time maintained above T_L	t_L	60-90 seconds
Classification temperature	T_C	260 °C
Peak package body temperature	T_P	$T_P \leq T_C$
Time within T_C - 5 °C and T_C	t_P	$t_P \leq 30$ seconds
Ramp-up Rate (T_L to T_p)		3 °C/second maximum
Ramp-down rate (T_p to T_L)		6 °C/second maximum
Time 25 °C to peak temperature		8 minutes maximum

Please refer to JEDEC J-STD020 for further information pertaining to reflow soldering of electronic components.

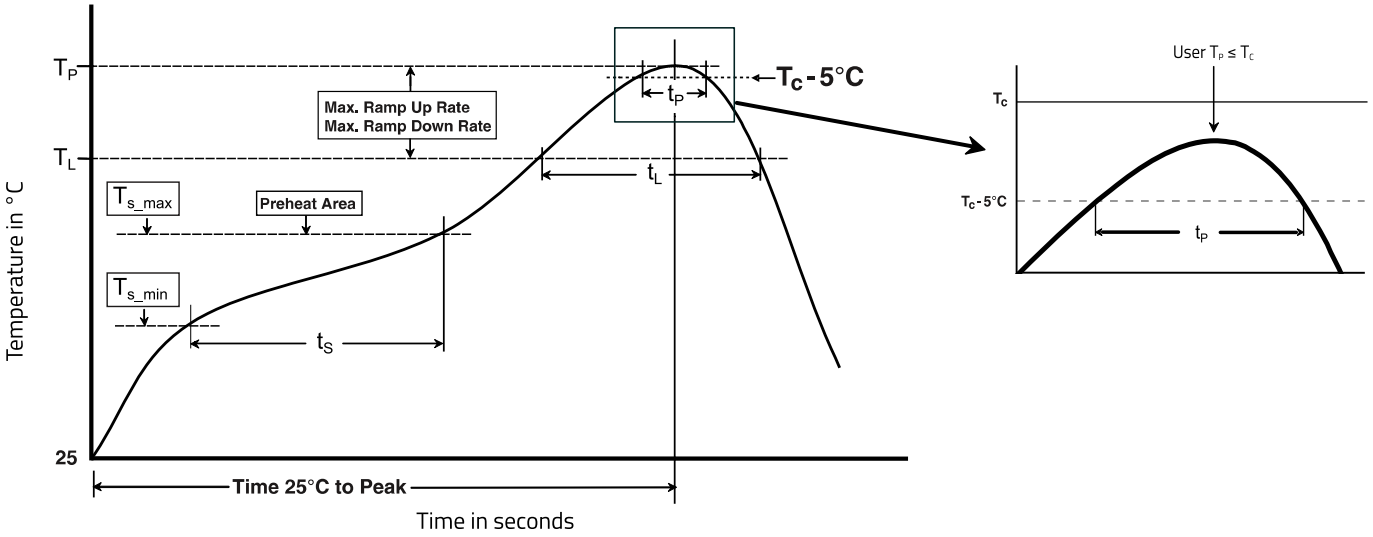


Figure 56: Soldering profile.

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23 PHYSICAL DIMENSIONS

Dimensions do not include mold flash, gate burrs, or protrusions.

23.1 Component

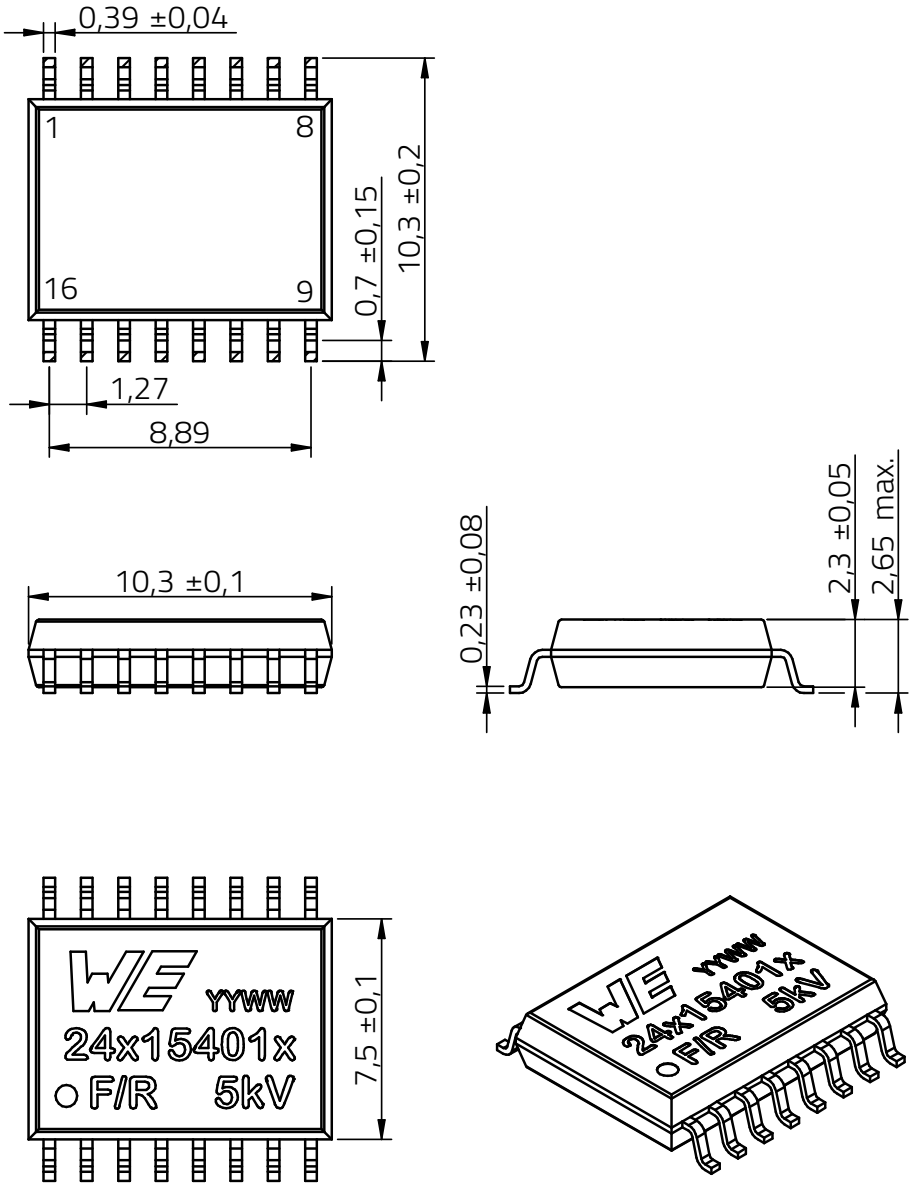


Figure 57: Component dimensions.
All dimensions in mm
Tolerance: xx.x =±0.5mm ; xx.xx = ±0.25mm unless otherwise noted
Dimensions do not include mold flash, gate burrs, or protrusions.

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23.2 Recommended Landpattern

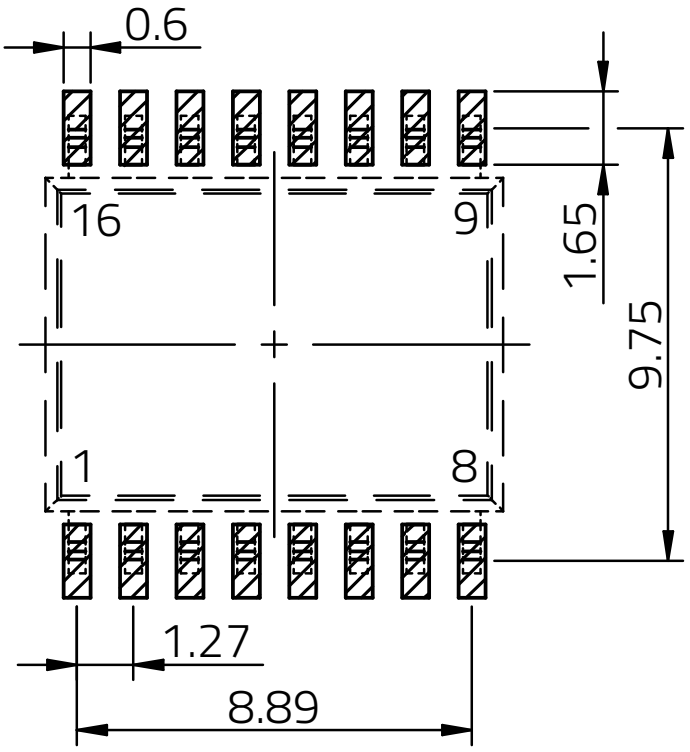


Figure 58: Recommended landpattern dimensions.

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23.3 Packaging

Reel in mm

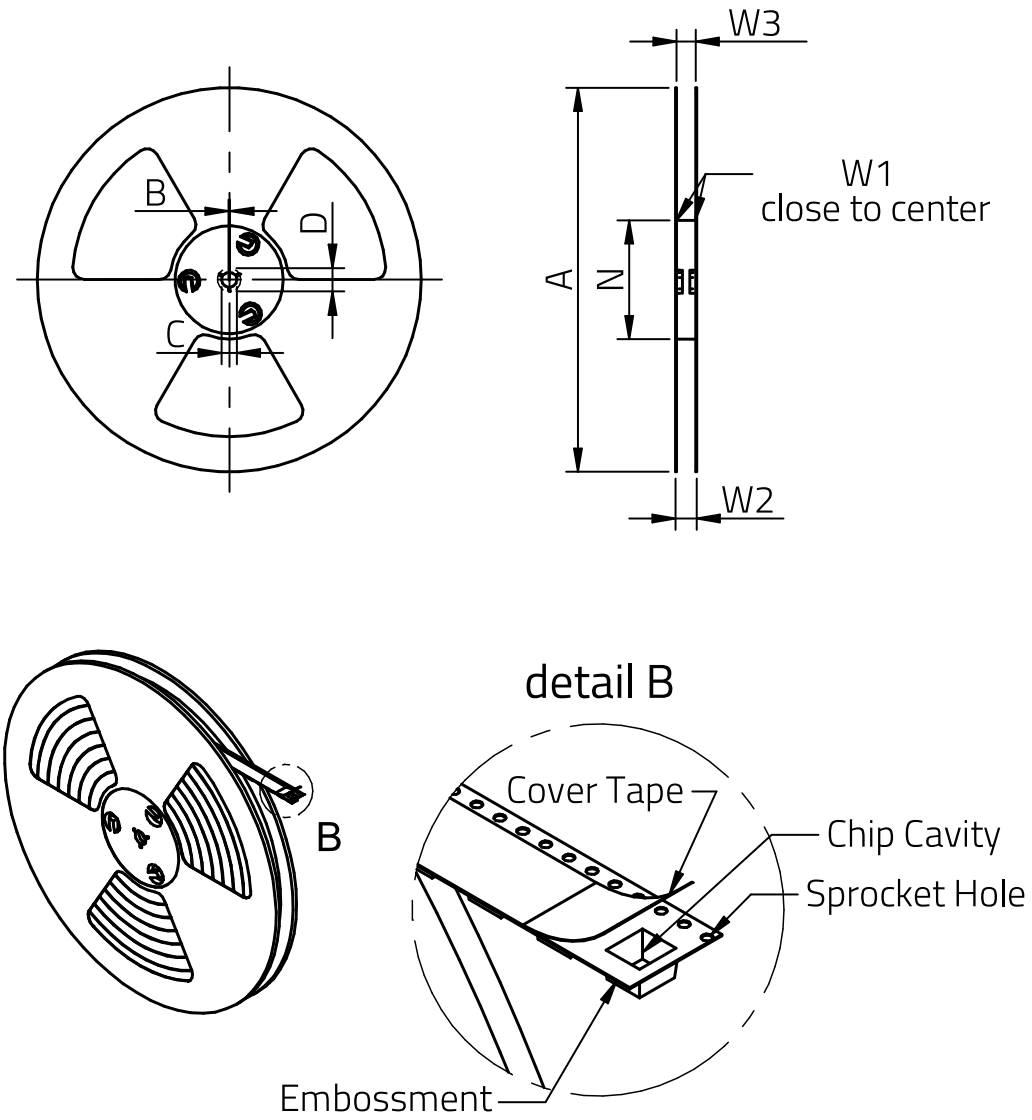


Figure 59: Reel dimensions.

Table 19: Reel dimensions.

A	B	C	D	N	W1	W2	W3	W3
±2.00	min.	min.	min.	min.	+2.00	max.	min.	max.
330.00	1.50	12.80	20.20	60.00	16.40	22.40	15.90	19.40

Reel material is polystyrene.

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Tape in mm

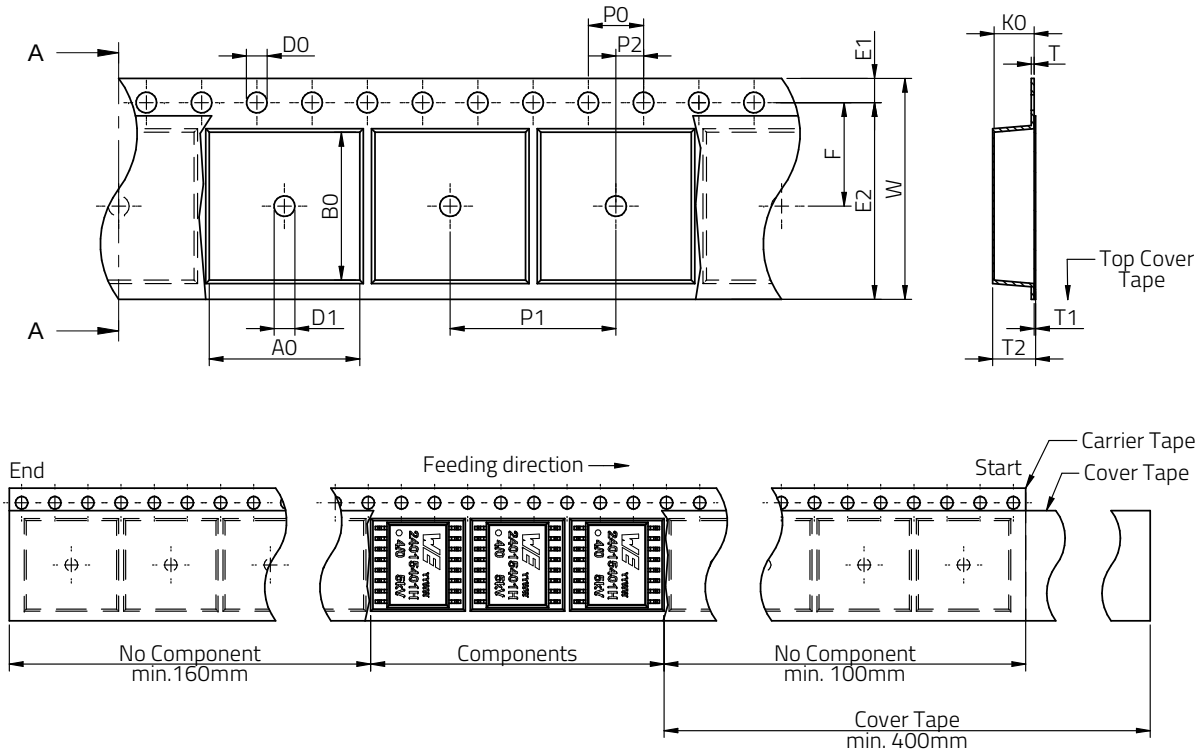


Figure 60: Tape dimensions.

Table 20: Tape dimensions part 1.

A0	B0	D0	D1	E1	E2	F	P0	P1	P2	W
typ.	typ.	min.	±0.10	min.	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10
10.90	10.70	1.50	1.50	1.75	14.25	7.50	4.00	12.00	2.00	16.00

Table 21: Tape dimensions part 2.

K0	T	T1	T2
typ.	typ.	ref.	typ.
3.2	0.35	0.1	3.4

Tape material is polystyrene.

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24 DOCUMENT HISTORY

Table 22: Document history.

Revision	Date	Description	Comment
1.0	October 2023	Initial release of datasheet	
1.1	November 2023	Updated design example layout	
1.2	July 2024	PCN	1. Added VDE 0884-17 reinforced insulation specifications and expanded IEC 60664-1 information in the isolation specification table. 2. Corrected front page dimensions to accurately reflect the physical dimensions of the component. 3. Updated approvals section to show the relevant certification numbers for VDE and UL. 4. Removed Isolation Voltage chapter. 5. Added note to specify allowable input and output voltage combinations. 6. Added safety limiting current and safety limiting power graphs.
1.3	October 2026	Minor PCN	As a datasheet information amendment, Würth Elektronik eiSos has corrected the part number in the typical circuit diagram, has corrected V_{OH} and V_{OL} test conditions to specify channel output load current and referenced V_{OH} to $V_{CC\ or\ OUT}$ instead of V_{INX} in electrical specifications table, has updated the recommended land pattern dimensions, has updated component representation in the “Tape dimensions” figure. There will be no change in form, fit, function, quality or reliability of the product.

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27 CAUTIONS AND WARNINGS

The following conditions apply to all goods within the product series of digital isolators of Würth Elektronik eiSos GmbH & Co. KG:

General:

- All recommendations according to the general technical specifications of the datasheet have to be complied with.
- The usage and operation of the product within ambient conditions which probably alloy or harm the component surface has to be avoided.
- The responsibility for the applicability of customer specific products and use in a particular customer design is always within the authority of the customer. All technical specifications for standard products do also apply for customer specific products
- Residual washing varnish agent that is used during the production to clean the application might change the characteristics of the body, pins or termination. The washing varnish agent could have a negative effect on the long term function of the product. Direct mechanical impact to the product shall be prevented as the material of the body, pins or termination could flake or in the worst case it could break. As these devices are sensitive to electrostatic discharge customer shall follow proper IC Handling Procedures.
- Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Würth Elektronik eiSos GmbH & Co. KG components in its applications, notwithstanding any applications-related information or support that may be provided by Würth Elektronik eiSos GmbH & Co. KG.
- Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences lessen the likelihood of failures that might cause harm and take appropriate remedial actions
- Customer will fully indemnify Würth Elektronik eiSos and its representatives against any damages arising out of the use of any Würth Elektronik eiSos GmbH & Co. KG components in safety-critical applications

Product specific:

Follow all instructions mentioned in the datasheet, especially:

- The solder profile has to comply with the technical reflow or wave soldering specification, otherwise this will void the warranty.
- All products are supposed to be used before the end of the period of 12 months based on the product date-code.
- Violation of the technical product specifications such as exceeding the absolute maximum ratings will void the warranty.
- It is also recommended to return the body to the original moisture proof bag and reseal the moisture proof bag again.
- ESD prevention methods need to be followed for manual handling and processing by machinery.

Disclaimer:

This electronic component has been designed and developed for usage in general electronic equipment only. This product is not authorized for use in equipment where a higher safety standard and reliability standard is especially required or where a failure of the product is reasonably expected to cause severe personal injury or death, unless the parties have executed an agreement specifically governing such use. Moreover Würth Elektronik eiSos GmbH & Co. KG products are neither designed nor intended for use in areas such as military, aerospace, aviation, nuclear control, submarine, transportation (automotive control, train control, ship control), transportation signal, disaster prevention, medical, public information network etc. Würth Elektronik eiSos GmbH & Co. KG must be informed about the intent of such usage before the design-in stage. In addition, sufficient reliability evaluation checks for safety must be performed on every electronic component which is used in electrical circuits that require high safety and reliability functions or performance. These cautions and warnings comply with the state of the scientific and technical knowledge and are believed to be accurate and reliable. However, no responsibility is assumed for inaccuracies or incompleteness.

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28 IMPORTANT NOTES

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Customer Responsibility Related to Specific, in Particular Safety-Relevant, Applications

It has to be clearly pointed out that the possibility of a malfunction of electronic components or failure before the end of the usual lifetime cannot be completely eliminated in the current state of the art, even if the products are operated within the range of the specifications. In certain customer applications requiring a very high level of safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health it must be ensured by most advanced technological aid of suitable design of the customer application that no injury or damage is caused to third parties in the event of malfunction or failure of an electronic component.

Best Care and Attention

Any product-specific notes, warnings and cautions must be strictly observed. Any disregard will result in the loss of warranty.

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Some products within the product range may contain substances which are subject to restrictions in certain jurisdictions in order to serve specific technical requirements. Necessary information is available on request. In this case the field sales engineer or the internal sales person in charge should be contacted who will be happy to support in this matter.

Product R&D

Due to constant product improvement product specifications may change from time to time. As a standard reporting procedure of the Product Change Notification (PCN) according to the JEDEC-Standard we inform about minor and major changes. In case of further queries regarding the PCN, the field sales engineer or the internal sales person in charge should be contacted. The basic responsibility of the customer as per Section 1 and 2 remains unaffected.

Product Life Cycle

Due to technical progress and economical evaluation we also reserve the right to discontinue production and delivery of products. As a standard reporting procedure of the Product Termination Notification (PTN) according to the JEDEC Standard we will inform at an early stage about inevitable product discontinuance. According to this we cannot guarantee that all products within our product range will always be available. Therefore it needs to be verified with the field sales engineer or the internal sales person in charge about the current product availability expectancy before or when the product for application design-in disposal is considered. The approach named above does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.

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