### 4 Channel Digital Isolator

## DESCRIPTION

The CDIS 18014x15401x is a 4 channel digital isolator series that provides capacitive isolation between the primary and secondary sides of the device.

The digital isolator requires two supplies, one for the primary side and one for the secondary side.

The CDIS digital isolator ensures fast time to market and low development costs.

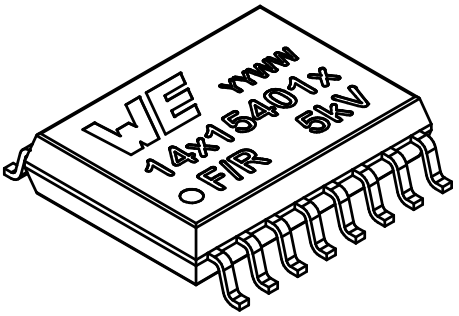
The digital isolator is available in an SOIC-16WB package (10.3 x 7.5 x 2.5)mm.

## FEATURES

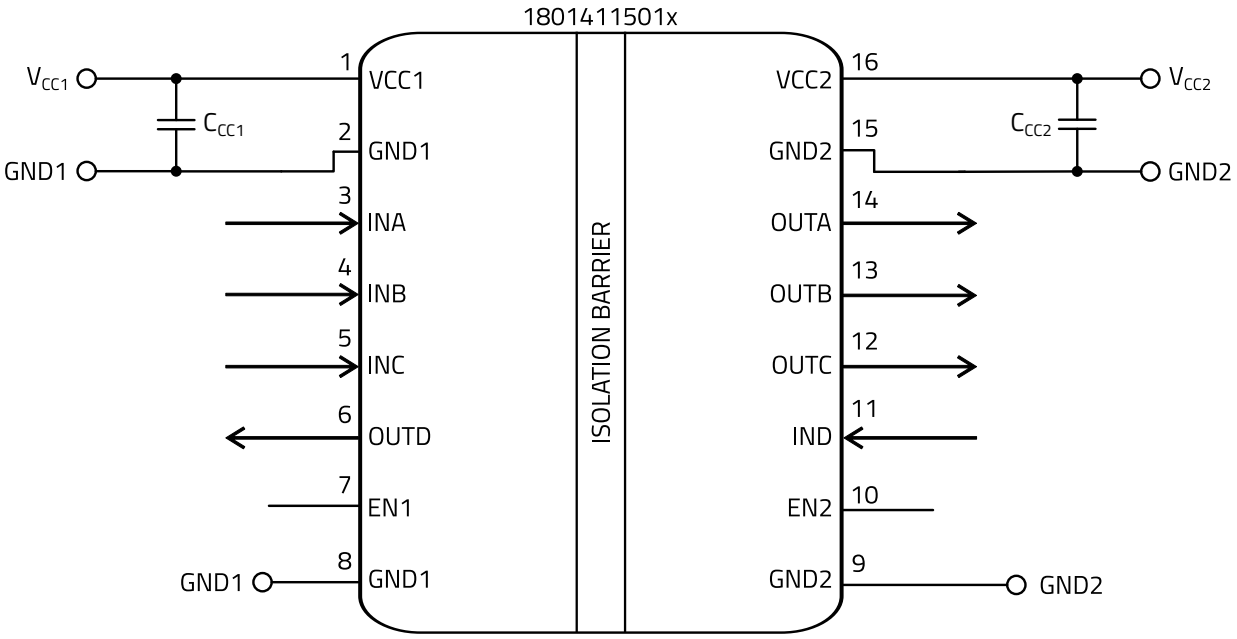
- Available channel configurations: 4/0, 3/1 and 2/2
- Default channel output status: high or low
- Low propagation delay: 12ns typ.
- Input voltage range: 2.375V to 5.5V
- Data rate up to 150Mbps
- CMTI: ±150kV/µs typ.
- Isolation: $5kV_{RMS}$ for 60s
- Ambient temperature range: -40°C to 125°C
- RoHS and REACh compliant
- UL1577 certified
- IEC 60747-17 pending

## TYPICAL APPLICATIONS

- Communication bus isolation
- Motor control
- Battery management systems
- Solar inverters
- Test and measurement systems
- Programmable logic controller (PLC) interfaces




## TYPICAL CIRCUIT DIAGRAM



CONTENTS

## 1 PINOUT

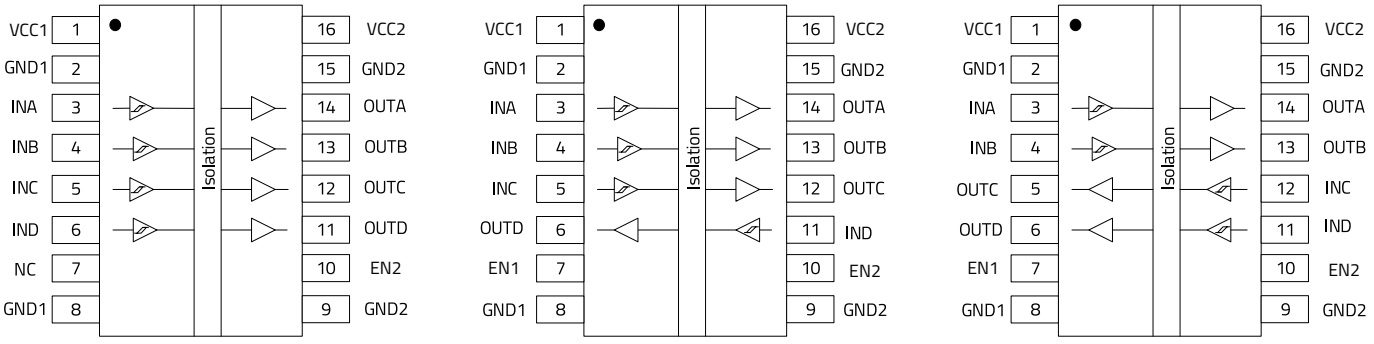



Figure 1: Pinout.

Table 1: Marking description.

| MARKING | DESCRIPTION |
|---|---|
| WE | Würth Elektronik eiSos GmbH & Co. KG |
| YYWW | Year and calendar week |
| 14x15401x | Order code |
| F/R | Number of forward/reverse channels |
| 5kV | 5kV isolation voltage |

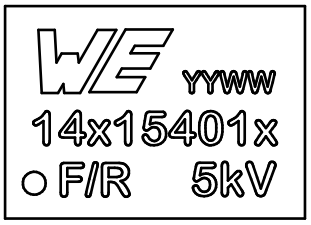



Figure 2: Marking.

Table 2: Pin description.

| SYMBOL | NUMBER | TYPE | DESCRIPTION |
|---|---|---|---|
| VCC1 | 1 | Power | Primary side supply pin. |
| GND1 | 2 | Power | Primary side ground connection. |
| INA | 3 | I/O | Digital input A. |
| INB | 4 | I/O | Digital input B. |
| INC/OUTC | 5 | I/O | Digital input/output C. |
| IND/OUTD | 6 | I/O | Digital input/output D. |
| NC/EN1 | 7 | NC/Input | Not internally connected (18014015401x). Primary side channel output enable. Drive high or leave floating to enable operation. (18014115401x and 18014215401x). |
| GND1 | 8 | Power | Primary side ground connection. |
| GND2 | 9 | Power | Secondary side ground connection. |
| EN2 | 10 | Input | Secondary side channel output enable. Drive high or leave floating to enable operation. |
| OUTD/IND | 11 | I/O | Digital input/output D. |
| OUTC/INC | 12 | I/O | Digital input/output C. |
| OUTB | 13 | I/O | Digital output B. |
| OUTA | 14 | I/O | Digital output A. |
| GND2 | 15 | Power | Secondary side ground connection. |
| VCC2 | 16 | Power | Secondary side supply pin. |

## 2 ORDERING INFORMATION

Table 3: Ordering information.

| ORDER CODE | SPECIFICATIONS | PACKAGE | PACKAGING UNIT |
|---|---|---|---|
| 18014015401H | 4 forward, 0 reverse, default high | SOIC-16WB | 13" Reel (1000 pieces) |
| 18014015401L | 4 forward, 0 reverse, default low | | |
| 18014115401H | 3 forward, 1 reverse, default high | | |
| 18014115401L | 3 forward, 1 reverse, default low | | |
| 18014215401H | 2 forward, 2 reverse, default high | | |
| 18014215401L | 2 forward, 2 reverse, default low | | |

## 3 SALES INFORMATION

| SALES CONTACT |
|---|
| Würth Elektronik eiSos GmbH & Co. KG<br>EMC and Inductive Solutions<br>Max-Eyth-Str. 1<br>74638 Waldenburg<br>Germany<br>Tel. +49 (0) 7942 945 0<br>www.we-online.com/digitalisolators<br>Technical support: powermodules@we-online.com |

## 4 ABSOLUTE MAXIMUM RATINGS

**Caution:**
Exceeding the listed absolute maximum ratings may affect the device negatively and may cause permanent damage.

Table 4: Absolute maximum ratings.

| SYMBOL | PARAMETER | LIMIT | | UNIT |
|---|---|---|---|---|
| | | MIN[1] | MAX[1] | |
| VCC1, VCC2 | Supply voltage pins | -0.5 | 7 | V |
| INX, OUTX | Voltage at INX, OUTX, SEL pins | -0.5 | $V_{CCX}$ + 0.5[2] | V |
| $I_{OUTX}$ | Channel output current | -20 | 20 | mA |
| $T_{storage}$ | Assembled, non-operating storage temperature | -65 | 150 | °C |
| $V_{ESD}$ | ESD voltage (HBM)[4] | -6 | 6 | kV |
| $V_{ESD}$ | ESD voltage (CDM)[4] | -2 | 2 | kV |

## 5 OPERATING CONDITIONS

Operating conditions are conditions under which the device is intended to be functional. All values are either referenced to GND1 or GND2.

MIN and MAX limits are valid for the recommended ambient temperature range of -40°C to 125°C.

Table 5: Operating conditions.

| SYMBOL | PARAMETER | MIN[1] | TYP[3] | MAX[1] | UNIT |
|---|---|---|---|---|---|
| $V_{CC1}$, $V_{CC2}$ | Supply voltage | 2.375 | — | 5.5 | V |
| $V_{INX\_H}$ | Logic input high threshold | 2.0 | — | — | V |
| $V_{INX\_L}$ | Logic input low threshold | — | — | 0.8 | V |
| $I_{OH}$ | High-level channel output current $V_{CCO}$ = 5V | -4 | — | — | mA |
| | High-level channel output current $V_{CCO}$ = 3.3V | -2 | — | — | mA |
| | High-level channel output current $V_{CCO}$ = 2.5V | -1 | — | — | mA |
| $I_{OL}$ | Low-level channel output current $V_{CCO}$ = 5V | — | — | 4 | mA |
| | Low-level channel output current $V_{CCO}$ = 3.3V | — | — | 2 | mA |
| | Low-level channel output current $V_{CCO}$ = 2.5V | — | — | 1 | mA |
| DR | Data rate | 0 | — | 150 | Mbps |
| PW | Signal pulse width | 5 | — | — | ns |
| $T_a$ | Ambient temperature range | -40 | — | 125 | °C |

## 6 ELECTRICAL SPECIFICATIONS

**Caution:**
MIN and MAX limits are valid for the recommended ambient temperature range of -40°C to 125°C. Typical values represent statistically the utmost probable values at the following conditions: $V_{CC}$ = 5V, 3.3V or 2.5V, ENX = high, $T_A$ = 25°C, unless otherwise noted.

Table 6: Electrical specifications part 1.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN[1] | TYP[3] | MAX[1] | UNIT |
|---|---|---|---|---|---|---|
| **Supply Characteristics** | | | | | | |
| $V_{CCX\_UVLO}$ | Supply undervoltage lockout falling threshold | | 1.88 | 2.10 | 2.325 | V |
| | Undervoltage lockout rising threshold | | 1.95 | 2.24 | 2.375 | V |
| | Undervoltage lockout hysteresis | | 70 | 140 | 250 | mV |
| **Channel Characteristics** | | | | | | |
| $I_{IH}$ | High-level input leakage current | $V_{INX} = V_{CCI}$ | — | — | 20 | µA |
| $I_{IL}$ | Low-level input leakage current | $V_{INX}$ = 0V | -20 | — | — | µA |
| $V_{OH}$ | High-level output voltage | $V_{INX} = V_{CCI}$ | — | $V_{INX}$ - 0.2 | — | V |
| $V_{OL}$ | Low-level output voltage | V = 0V | — | 0.2 | — | V |
| $V_{EN\_SRMIN}$ | Minimum enable signal slew rate | | — | 1 | — | mV/µs |
| CMTI | Common-mode transient immunity | $V_{INX} = V_{CCI}$ or 0V, $V_{CM}$ = 1500V | — | 150 | — | kV/µs |
| **Timing Characteristics** | | | | | | |
| $t_r$ | Output signal rise time | 10% to 90% of $V_{OUTX}$ | — | 2.5 | 4.0 | ns |
| $t_f$ | Output signal fall time | 90% to 10% of $V_{OUTX}$ | — | 2.5 | 4.0 | ns |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time | 50% of $V_{INX}$ to 50% of $V_{OUTX}$ | 5 | 12 | 16 | ns |
| $t_{PHZ}$ | Disable Propagation Delay, High to High-Z | | — | 8 | 13 | ns |
| PWD | Pulse width distortion $\lvert t_{PLH} - t_{PHL} \rvert$ | | — | 0.2 | 4.5 | ns |
| $t_{SK(C-C)}$ | Channel-to-channel output skew time | | — | 0.4 | 2.5 | ns |
| $t_{SK(P-P)}$ | Part-to-part output skew time | | — | 2.0 | 4.5 | ns |

Parameters indicated in electrical specifications part 1 are applicable across all part numbers with all input/output conditions unless otherwise specified.

Table 7: Electrical specifications part 2.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN[1] | TYP[3] | MAX[1] | UNIT |
|---|---|---|---|---|---|---|
| **18014015401x $V_{CC1}$ = 5V and $V_{CC2}$ = 5V** | | | | | | |
| $I_{CC1}$ | Primary side external power supply input current[5] | $V_{INX}$ = channel default | — | 1.4 | — | mA |
| | | $V_{INX} \neq$ channel default | — | 6 | — | mA |
| | | 1Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 3.7 | — | mA |
| | | 10Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 3.7 | — | mA |
| | | 100Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 4.6 | — | mA |
| $I_{CC2}$ | Secondary side external power supply input current[5] | $V_{INX}$ = channel default | — | 2.7 | — | mA |
| | | $V_{INX} \neq$ channel default | — | 2.8 | — | mA |
| | | 1Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 3.1 | — | mA |
| | | 10Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 6.9 | — | mA |
| | | 100Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 43.2 | — | mA |
| **18014115401x $V_{CC1}$ = 5V and $V_{CC2}$ = 5V** | | | | | | |
| $I_{CC1}$ | Primary side external power supply input current[5] | $V_{INX}$ = channel default | — | 1.9 | — | mA |
| | | $V_{INX} \neq$ channel default | — | 5.5 | — | mA |
| | | 1Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 3.8 | — | mA |
| | | 10Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 4.5 | — | mA |
| | | 100Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 10.6 | — | mA |
| $I_{CC2}$ | Secondary side external power supply input current[5] | $V_{INX}$ = channel default | — | 2.7 | — | mA |
| | | $V_{INX} \neq$ channel default | — | 4.2 | — | mA |
| | | 1Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 3.7 | — | mA |
| | | 10Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 5.3 | — | mA |
| | | 100Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 23.1 | — | mA |
| **18014215401x $V_{CC1}$ = 5V and $V_{CC2}$ = 5V** | | | | | | |
| $I_{CC1}$ | Primary side external power supply input current[5] | $V_{INX}$ = channel default | — | 2.5 | — | mA |
| | | $V_{INX} \neq$ channel default | — | 5.1 | — | mA |
| | | 1Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 3.9 | — | mA |
| | | 10Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 5.2 | — | mA |
| | | 100Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 16.5 | — | mA |

Table 8: Electrical specifications part 3.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN[1] | TYP[3] | MAX[1] | UNIT |
|---|---|---|---|---|---|---|
| $I_{CC2}$ | Secondary side external power supply input current[5] | $V_{INX}$ = channel default | — | 2.4 | — | mA |
| | | $V_{INX} \neq$ channel default | — | 4.9 | — | mA |
| | | 1Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 3.8 | — | mA |
| | | 10Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 4.9 | — | mA |
| | | 100Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 17 | — | mA |
| **18014015401x $V_{CC1}$ = 3.3V and $V_{CC2}$ = 3.3V** | | | | | | |
| $I_{CC1}$ | Primary side external power supply input current[5] | $V_{INX}$ = channel default | — | 1.3 | — | mA |
| | | $V_{INX} \neq$ channel default | — | 6 | — | mA |
| | | 1Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 3.7 | — | mA |
| | | 10Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 3.7 | — | mA |
| | | 100Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 4.7 | — | mA |
| $I_{CC2}$ | Secondary side external power supply input current[5] | $V_{INX}$ = channel default | — | 2.5 | — | mA |
| | | $V_{INX} \neq$ channel default | — | 2.6 | — | mA |
| | | 1Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 2.9 | — | mA |
| | | 10Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 5.4 | — | mA |
| | | 100Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 29.6 | — | mA |
| **18014115401x $V_{CC1}$ = 3.3V and $V_{CC2}$ = 3.3V** | | | | | | |
| $I_{CC1}$ | Primary side external power supply input current[5] | $V_{INX}$ = channel default | — | 1.9 | — | mA |
| | | $V_{INX} \neq$ channel default | — | 5.4 | — | mA |
| | | 1Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 3.7 | — | mA |
| | | 10Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 4.1 | — | mA |
| | | 100Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 8.4 | — | mA |
| $I_{CC2}$ | Secondary side external power supply input current[5] | $V_{INX}$ = channel default | — | 2.8 | — | mA |
| | | $V_{INX} \neq$ channel default | — | 4.1 | — | mA |
| | | 1Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 3.5 | — | mA |
| | | 10Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 4.6 | — | mA |
| | | 100Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 15.9 | — | mA |

Table 9: Electrical specifications part 4.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN[1] | TYP[3] | MAX[1] | UNIT |
|---|---|---|---|---|---|---|
| **18014215401x $V_{CC1}$ = 3.3V and $V_{CC2}$ = 3.3V** | | | | | | |
| $I_{CC1}$ | Primary side external power supply input current[5] | $V_{INX}$ = channel default | — | 2.4 | — | mA |
| | | $V_{INX} \neq$ channel default | — | 5 | — | mA |
| | | 1Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 3.8 | — | mA |
| | | 10Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 4.6 | — | mA |
| | | 100Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 12.5 | — | mA |
| $I_{CC2}$ | Secondary side external power supply input current[5] | $V_{INX}$ = channel default | — | 2.3 | — | mA |
| | | $V_{INX} \neq$ channel default | — | 4.8 | — | mA |
| | | 1Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 3.6 | — | mA |
| | | 10Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 4.3 | — | mA |
| | | 100Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 11.5 | — | mA |
| **18014015401x $V_{CC1}$ = 2.5V and $V_{CC2}$ = 2.5V** | | | | | | |
| $I_{CC1}$ | Primary side external power supply input current[5] | $V_{INX}$ = channel default | — | 1.3 | — | mA |
| | | $V_{INX} \neq$ channel default | — | 6 | — | mA |
| | | 1Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 3.6 | — | mA |
| | | 10Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 3.7 | — | mA |
| | | 100Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 4.8 | — | mA |
| $I_{CC2}$ | Secondary side external power supply input current[5] | $V_{INX}$ = channel default | — | 2.5 | — | mA |
| | | $V_{INX} \neq$ channel default | — | 2.5 | — | mA |
| | | 1Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 2.7 | — | mA |
| | | 10Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 4.6 | — | mA |
| | | 100Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 23.4 | — | mA |
| **18014115401x $V_{CC1}$ = 2.5V and $V_{CC2}$ = 2.5V** | | | | | | |
| $I_{CC1}$ | Primary side external power supply input current[5] | $V_{INX}$ = channel default | — | 1.8 | — | mA |
| | | $V_{INX} \neq$ channel default | — | 5.4 | — | mA |
| | | 1Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 3.6 | — | mA |
| | | 10Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 4 | — | mA |
| | | 100Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 7.5 | — | mA |

Table 10: Electrical specifications part 5.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN[1] | TYP[3] | MAX[1] | UNIT |
|---|---|---|---|---|---|---|
| $I_{CC2}$ | Secondary side external power supply input current[5] | $V_{INX}$ = channel default | — | 2.7 | — | mA |
| | | $V_{INX} \neq$ channel default | — | 4 | — | mA |
| | | 1Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 3.5 | — | mA |
| | | 10Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 4.3 | — | mA |
| | | 100Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 11.8 | — | mA |
| **18014215401x $V_{CC1}$ = 2.5V and $V_{CC2}$ = 2.5V** | | | | | | |
| $I_{CC1}$ | Primary side external power supply input current[5] | $V_{INX}$ = channel default | — | 2.3 | — | mA |
| | | $V_{INX} \neq$ channel default | — | 5 | — | mA |
| | | 1Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 3.7 | — | mA |
| | | 10Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 4.4 | — | mA |
| | | 100Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 10.6 | — | mA |
| $I_{CC2}$ | Secondary side external power supply input current[5] | $V_{INX}$ = channel default | — | 2.3 | — | mA |
| | | $V_{INX} \neq$ channel default | — | 4.8 | — | mA |
| | | 1Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 3.6 | — | mA |
| | | 10Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 4.1 | — | mA |
| | | 100Mbps, $C_L$ = 15pF, 50% duty cycle square wave input signal | — | 9.7 | — | mA |

## 7 ISOLATION SPECIFICATIONS

Table 11: Isolation specification table.

| SYMBOL | PARAMETER | TEST CONDITIONS | TYP[3] | UNIT |
|---|---|---|---|---|
| CLR | External clearance | Shortest distance through air between terminals | 8 | mm |
| CPG | External creepage | Shortest distance across package surface between terminals | 8 | mm |
| DTI | Distance through the insulation | Minimum internal clearance | 28 | µm |
| CTI | Comparative tracking index | DIN EN 60112 (VDE 0303-11); IEC 60112 | >600 | V |
| | IEC 60664-1 overvoltage category | Rated mains voltage ≤300 $V_{RMS}$ | I-IV | |
| | | Rated mains voltage ≤400 $V_{RMS}$ | I-IV | |
| | | Rated mains voltage ≤600 $V_{RMS}$ | I-IV | |
| | | Rated mains voltage ≤1000 $V_{RMS}$ | I-III | |
| **UL1577** | | | | |
| $V_{ISO(max)}$ | Max. withstanding isolation voltage | $V_{TEST}$ = $V_{ISO}$, t = 60s (qualification), $V_{TEST}$ = 1.2 x $V_{ISO}$, t = 1s (100% production) | 5000 | $V_{RMS}$ |

## 8 APPROVALS

Table 12: Approvals.

| SYMBOL | STANDARD | DESCRIPTION |
|---|---|---|
| c UL us | UL 1577, 5th Edition | Nonoptical Isolating Devices – Component<br>UL Category: FPPT2 & FPPT8<br>UL File No: E535458<br>Applicable for altitudes up to 2000m |

## 9 RoHS, REACh

Table 13: RoHS, REACh.

| | | |
|---|---|---|
| RoHS directive | COMPLIANT RoHS&REACH WÜRTH ELEKTRONIK | Directive 2011/65/EU of the European Parliament and the Council of June 8th, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment. |
| REACh directive | | Directive 1907/2006/EU of the European Parliament and the Council of June 1st, 2007 regarding the Registration, Evaluation, Authorization and Restriction of Chemicals (REACh). |

## 10 PACKAGE SPECIFICATIONS

Table 14: Package specifications.

| ITEM | PARAMETER | TYP[3] | UNIT |
|---|---|---|---|
| Lead finish | — | Matte Sn | — |
| Weight | — | 0.42 | g |

## 11 NOTES

**(1)** Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

**(2)** This value must never exceed 7V.

**(3)** Typical numbers are valid at 25°C ambient temperature and represent statistically the utmost probability assuming the Gaussian distribution.

**(4)** The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD-22-114. The charged device model test method is per JESD22-C101.

**(5)** Supply current measurements are made with no additional load connected to the primary and secondary external power supplies. The indicated values only describe the current required to supply the internal circuitry and external capacitive loads on the channel outputs based on the signal described in the test conditions.

**(6)** 100% final production tested value. The qualified isolation voltage value is $5kV_{RMS}$. For detailed isolation characteristics see the isolation specification table (Isolation specification table).

## 12 ISOLATION VOLTAGE

### 12.1 Isolation Voltage Testing

To verify the integrity of the isolation a test voltage is applied for a specified time across a component that is designed to provide electrical isolation. This test is known as 'High Pot Test', 'Flash Tested', 'Withstand Voltage', 'Proof Voltage', 'Dielectric Withstand Voltage' or 'Isolation Test Voltage'.

All digital isolators are 100% production tested at their stated isolation voltage. This is 6kV$_{RMS}$ for 1s.[6]

The isolation test voltage indicated in this data sheet is for voltage transient immunity only. It does not allow this part to be used within a safety isolation system.

The digital isolator will function properly with several hundreds of volts applied continuously across the isolation barrier, however surrounding components must be individually analyzed to ensure proper insulation. Isolation measures must be taken into account to prevent any user-accessible circuitry from causing harm.

### 12.2 Dielectric Test Setup (High Pot Test)

Connect all input terminals together then all output terminals together (see figure below) before connecting the supply voltage. When testing, set the cut-off current to 1mA with a test voltage of 6kV$_{RMS}$ and test time of 1s.[6]

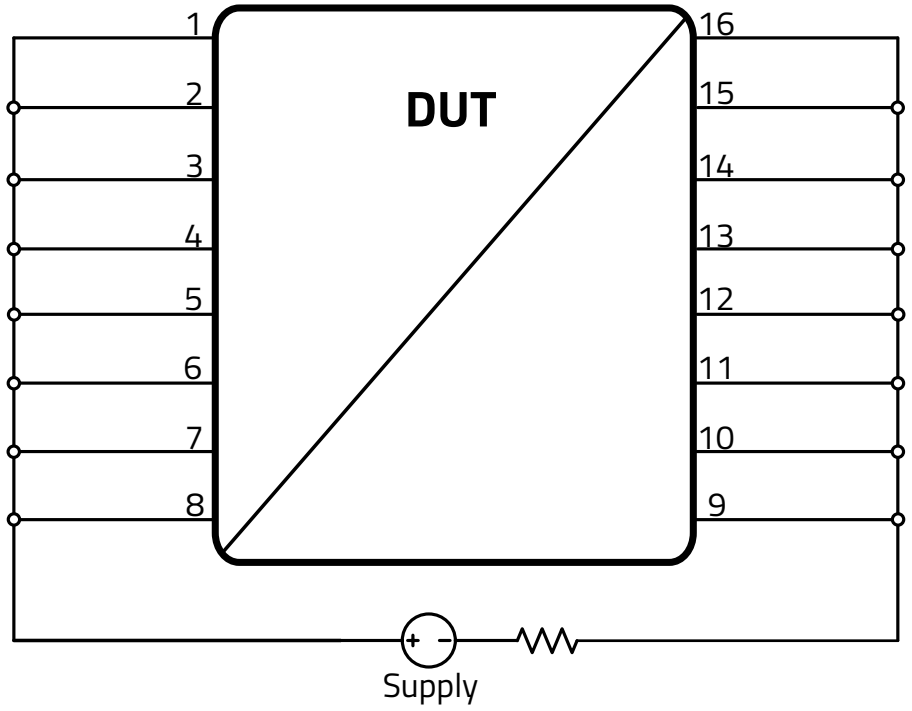



Figure 3: Dielectric test setup.

### 12.3 Repeated High-Voltage Isolation Testing

Typically, parts can withstand multiples of their stated test voltage and still perform optimally. However, repeated exposure to high voltage test conditions will degrade the component's isolation capabilities. It is recommended to keep high voltage isolation testing to a minimum to limit degradation of the device before its installation in an application. If repeated high voltage isolation testing is required, consider reducing the voltage by a significant amount (e.g. 20%) from the stated test voltage within the datasheet.

## 13 TYPICAL PERFORMANCE CURVES

If not otherwise specified, the following conditions apply: $T_A$ = 25°C.

### 13.1 DC Performance Curves

#### 13.1.1 Quiescent Current vs. Ambient Temperature

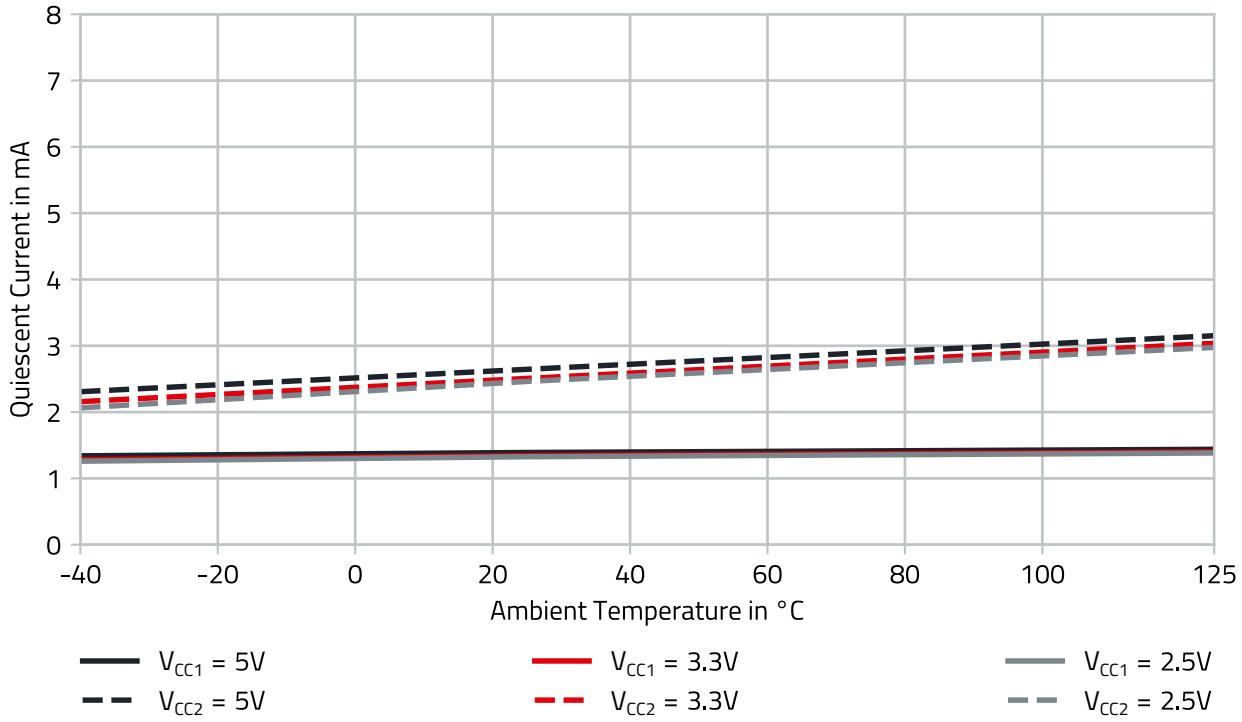



Figure 4: 18014015401H quiescent current, all channel inputs set to logic high.

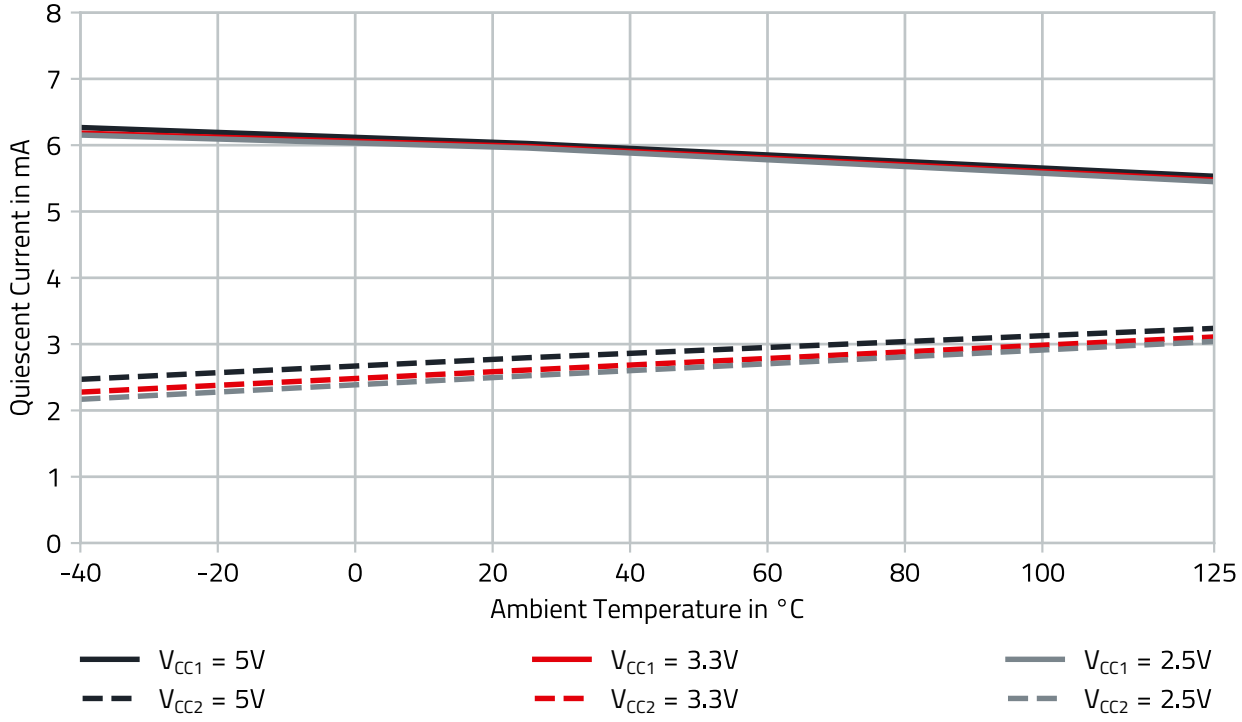



Figure 5: 18014015401H quiescent current, all channel inputs set to logic low.

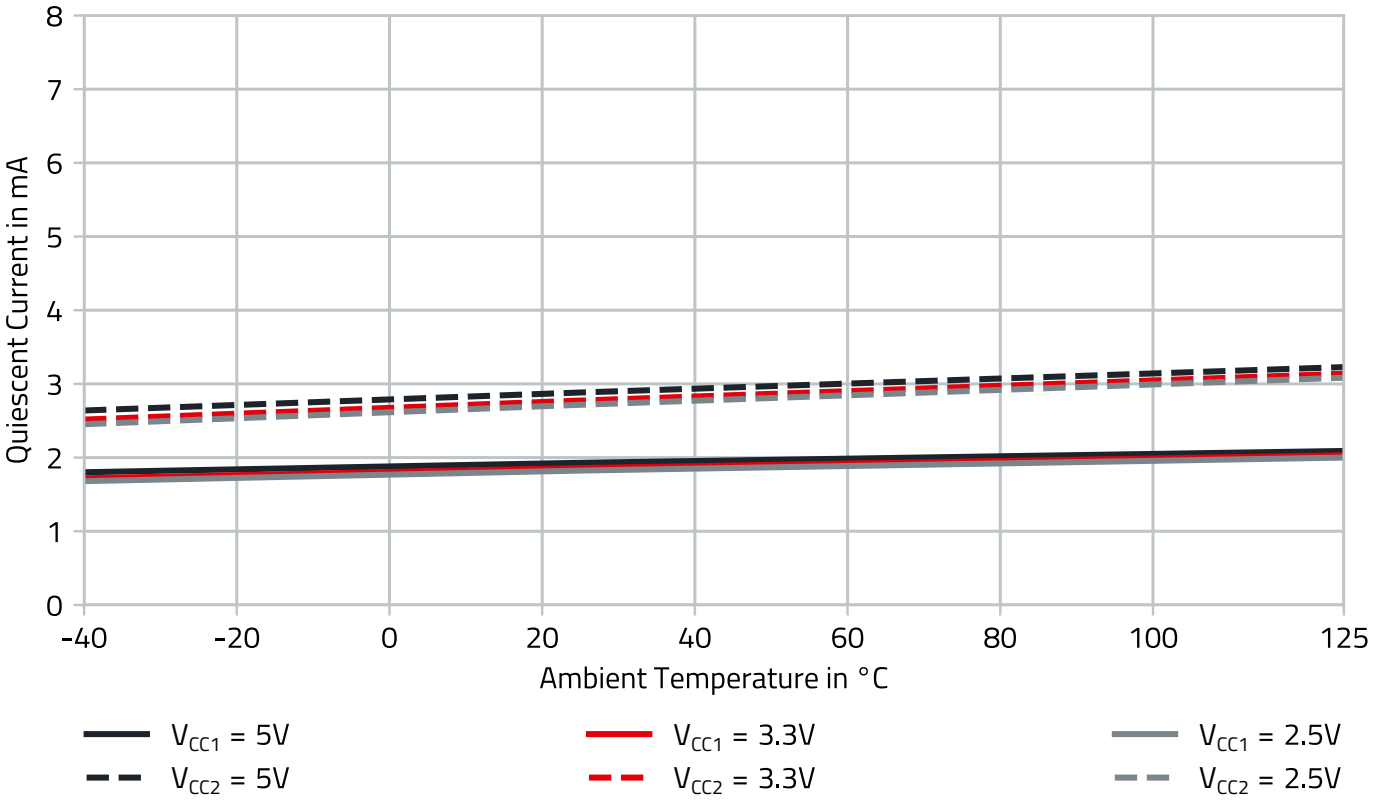



Figure 6: 18014115401H quiescent current, all channel inputs set to logic high.

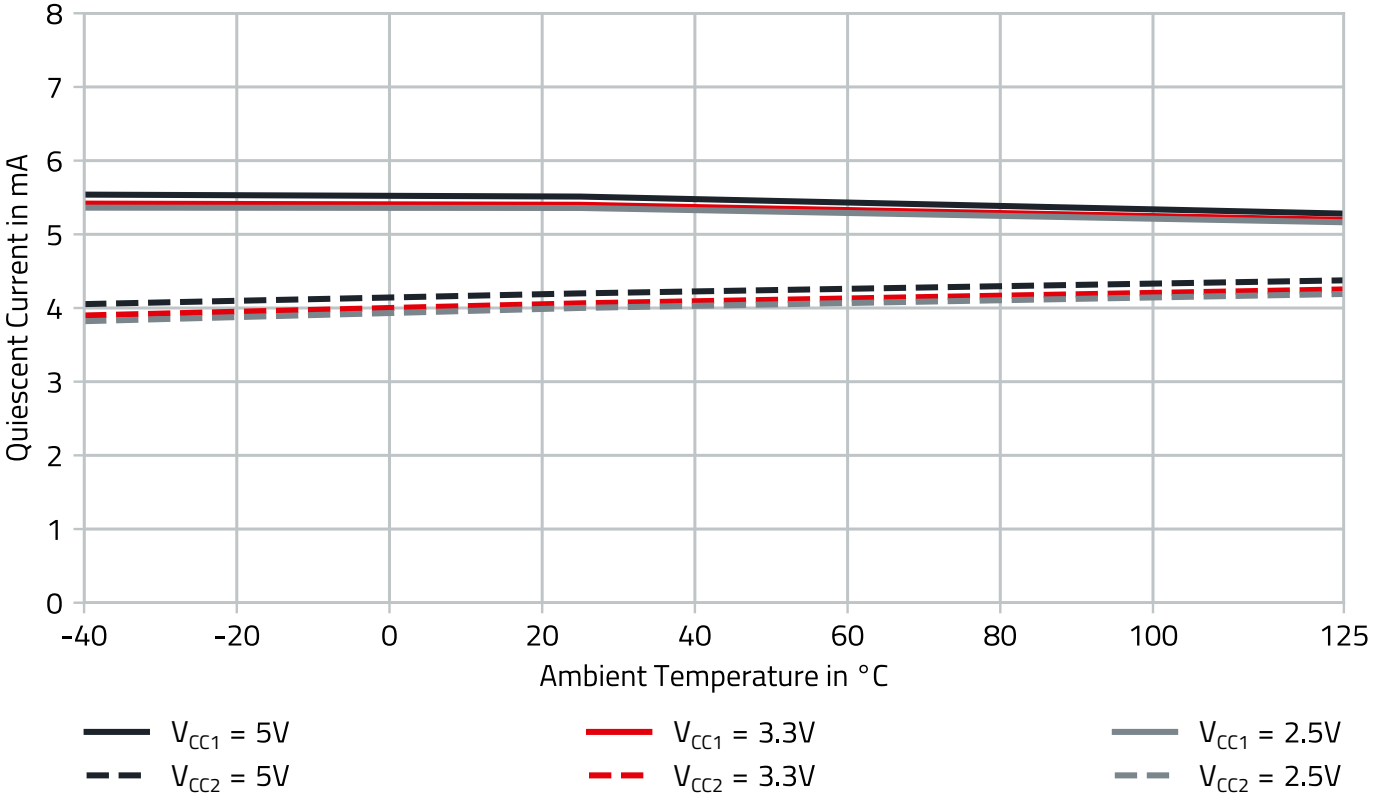



Figure 7: 18014115401H quiescent current, all channel inputs set to logic low.

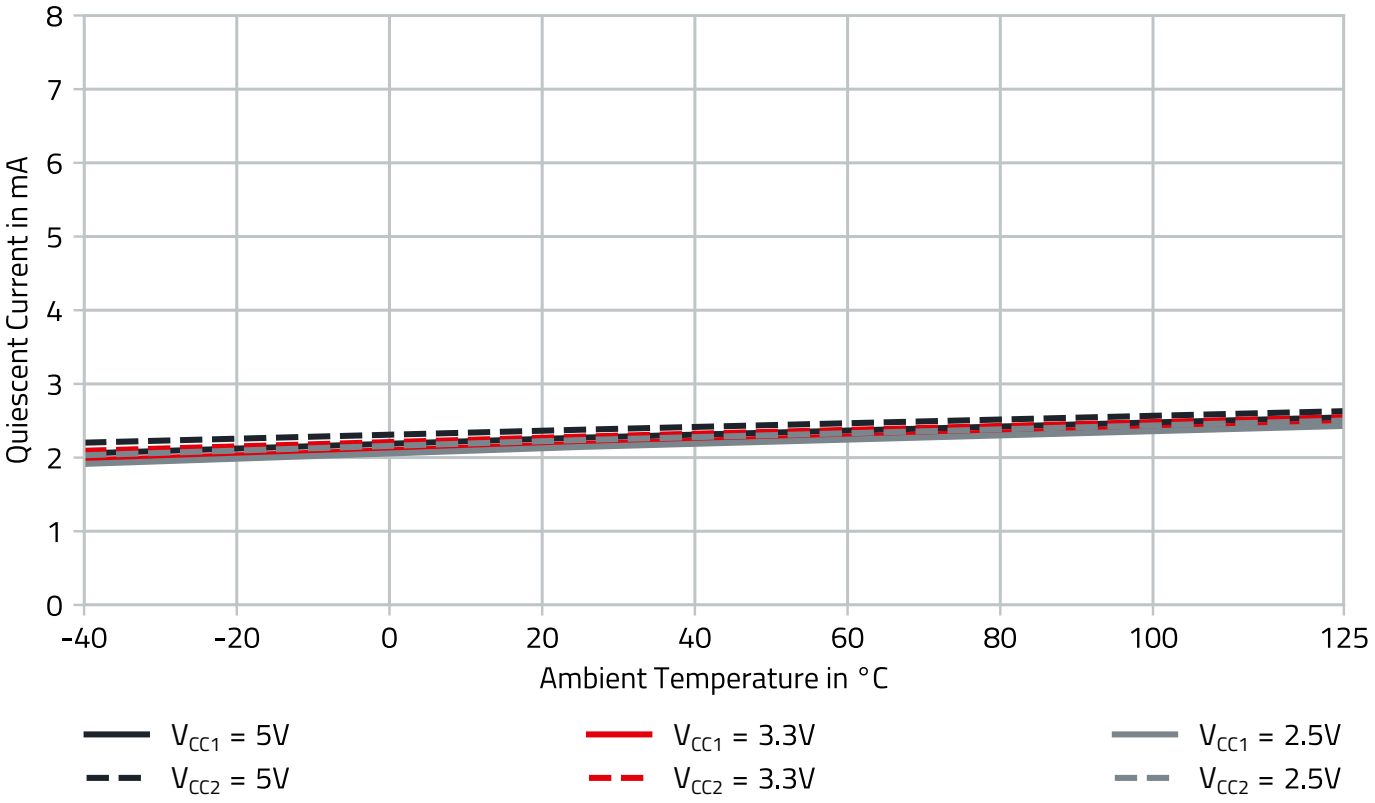



Figure 8: 18014215401H quiescent current, all channel inputs set to logic high.

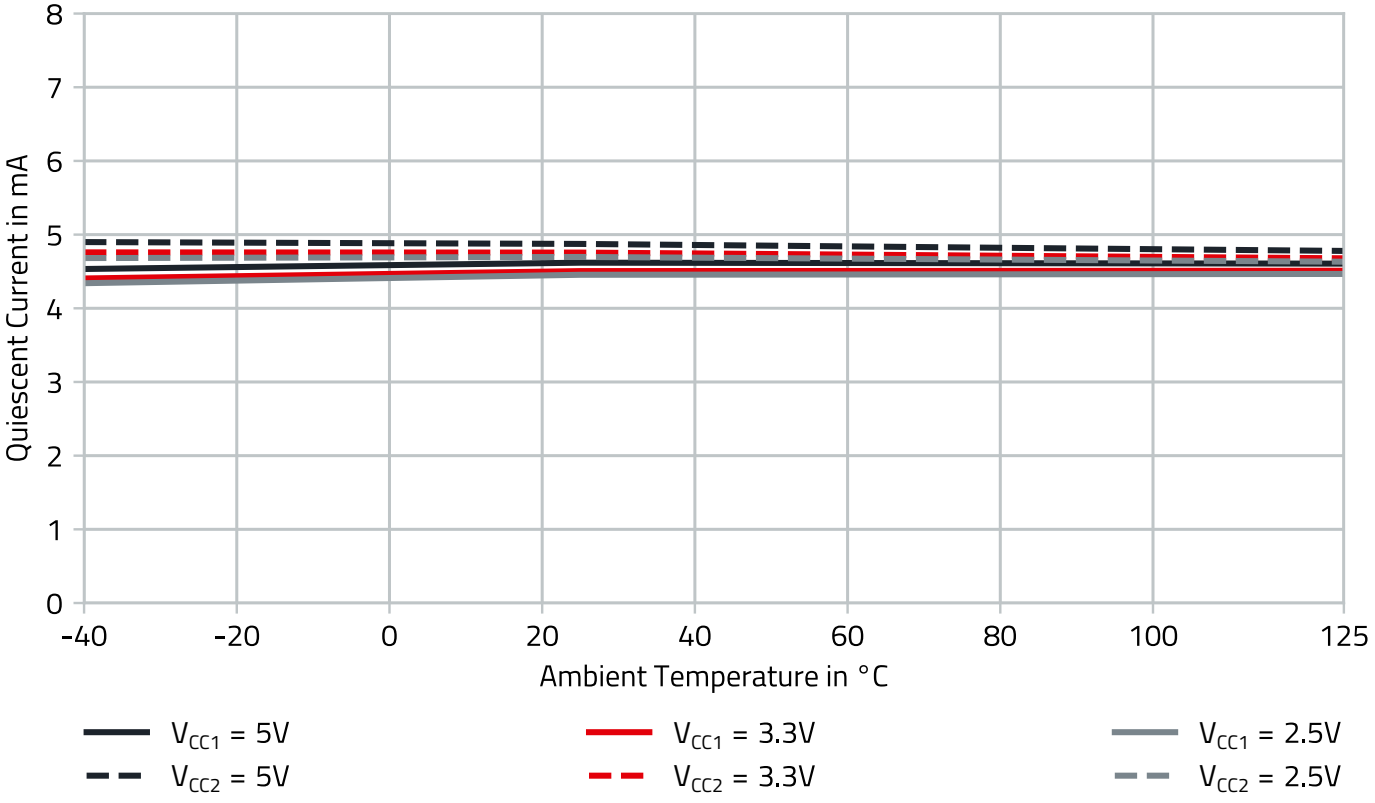



Figure 9: 18014215401H quiescent current, all channel inputs set to logic low.

### 13.1.2 Propagation Delay vs. Ambient Temperature

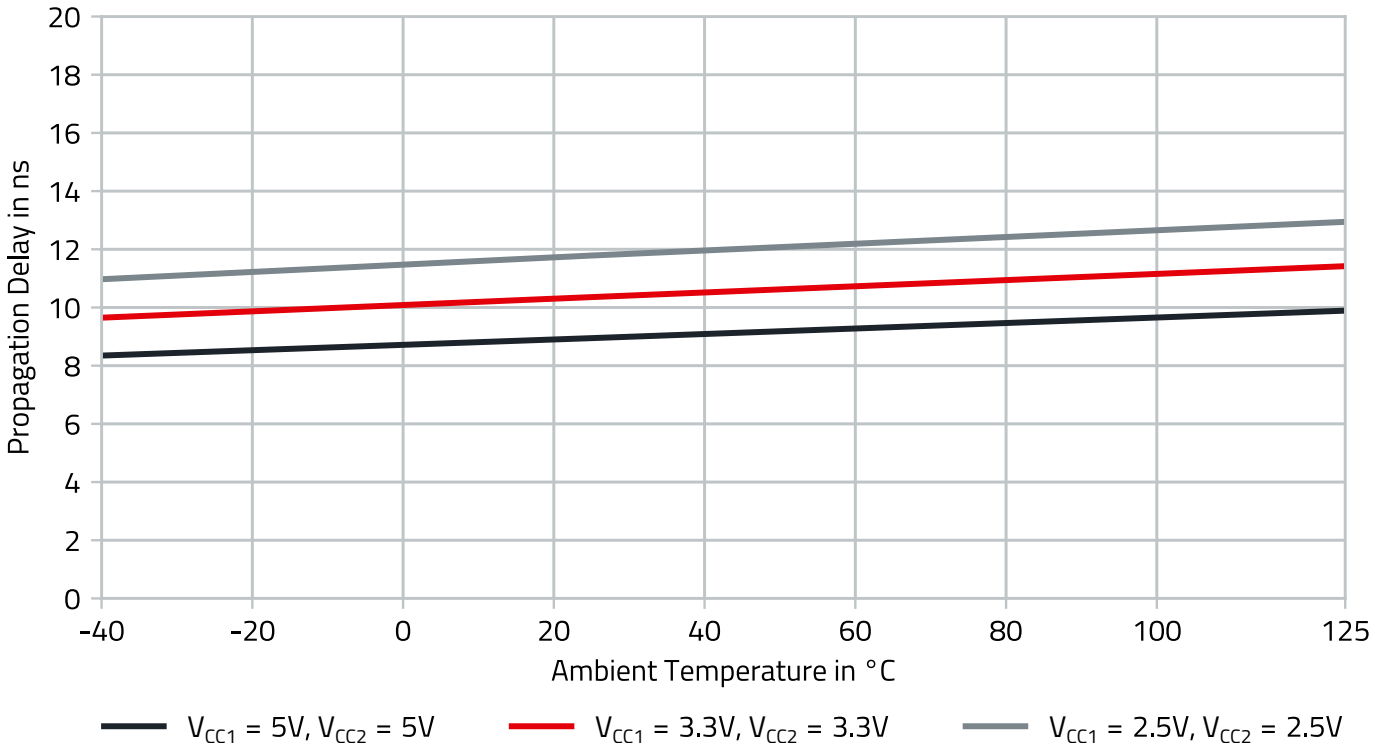



Figure 10: 18014x15401x propagation delay, all channels with low to high transition, $C_{LOAD}$ = 15pF.

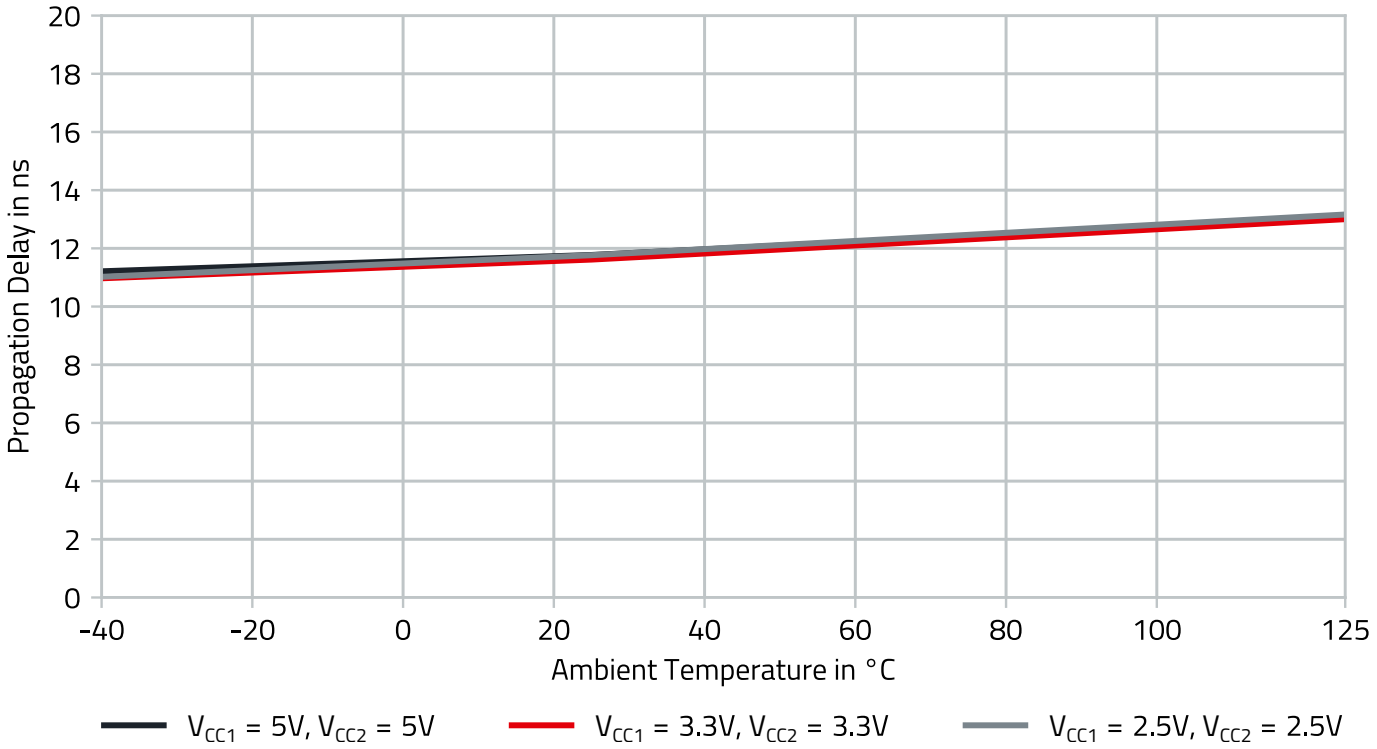



Figure 11: 18014x15401x propagation delay, all channels with high to low transition, $C_{LOAD}$ = 15pF.

### 13.1.3 Supply Current vs. Ambient Temperature

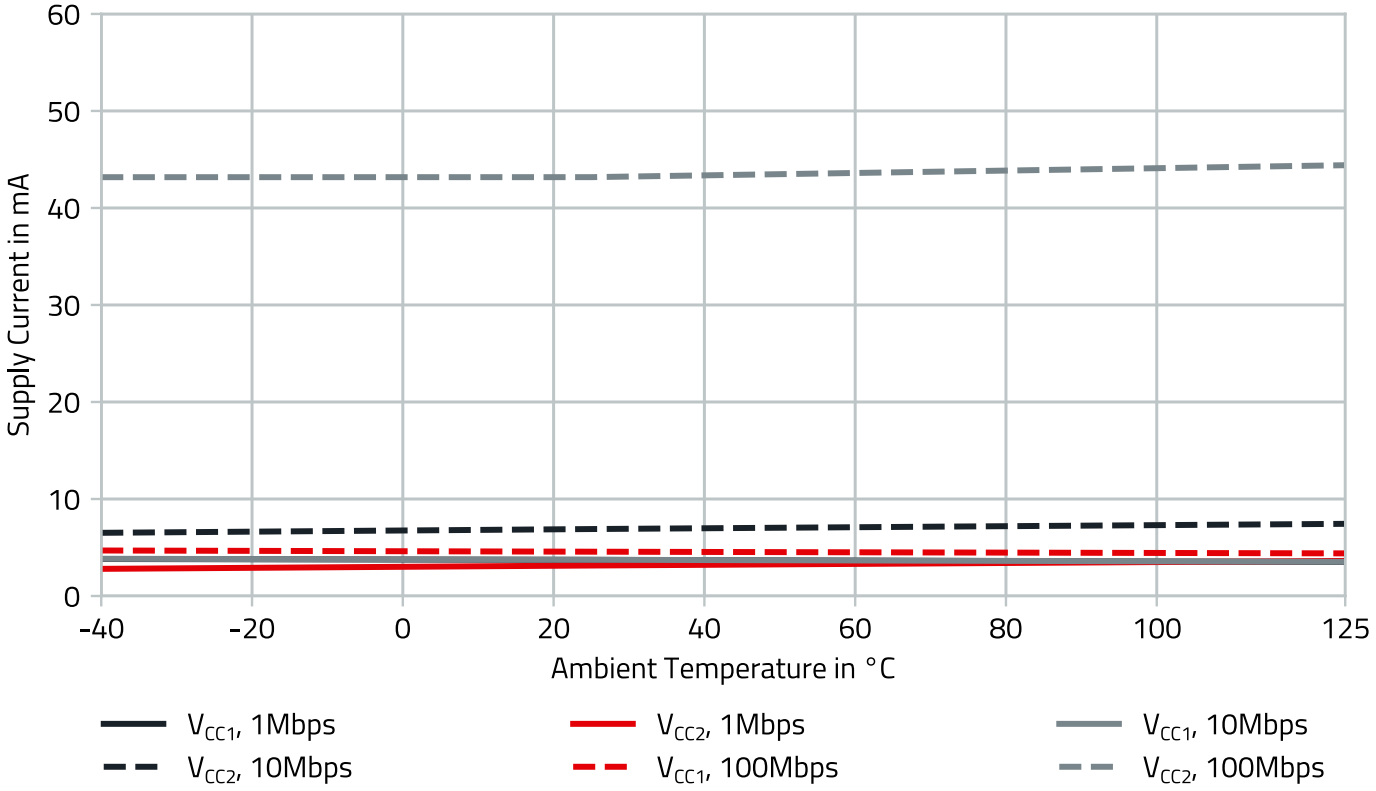



Figure 12: 18014015401x supply current $V_{CC1}$ = $V_{CC2}$ = 5V.

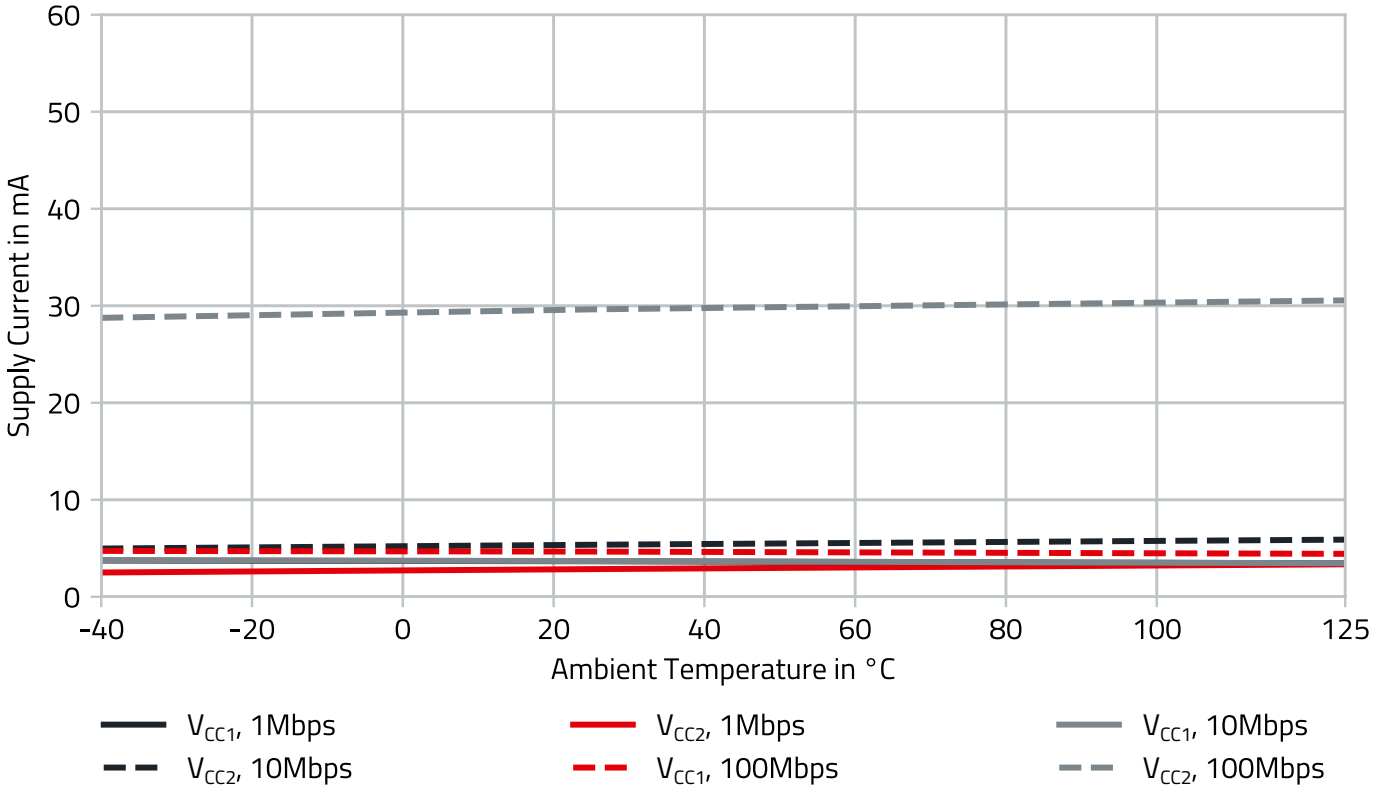



Figure 13: 18014015401x supply current $V_{CC1}$ = $V_{CC2}$ = 3.3V.

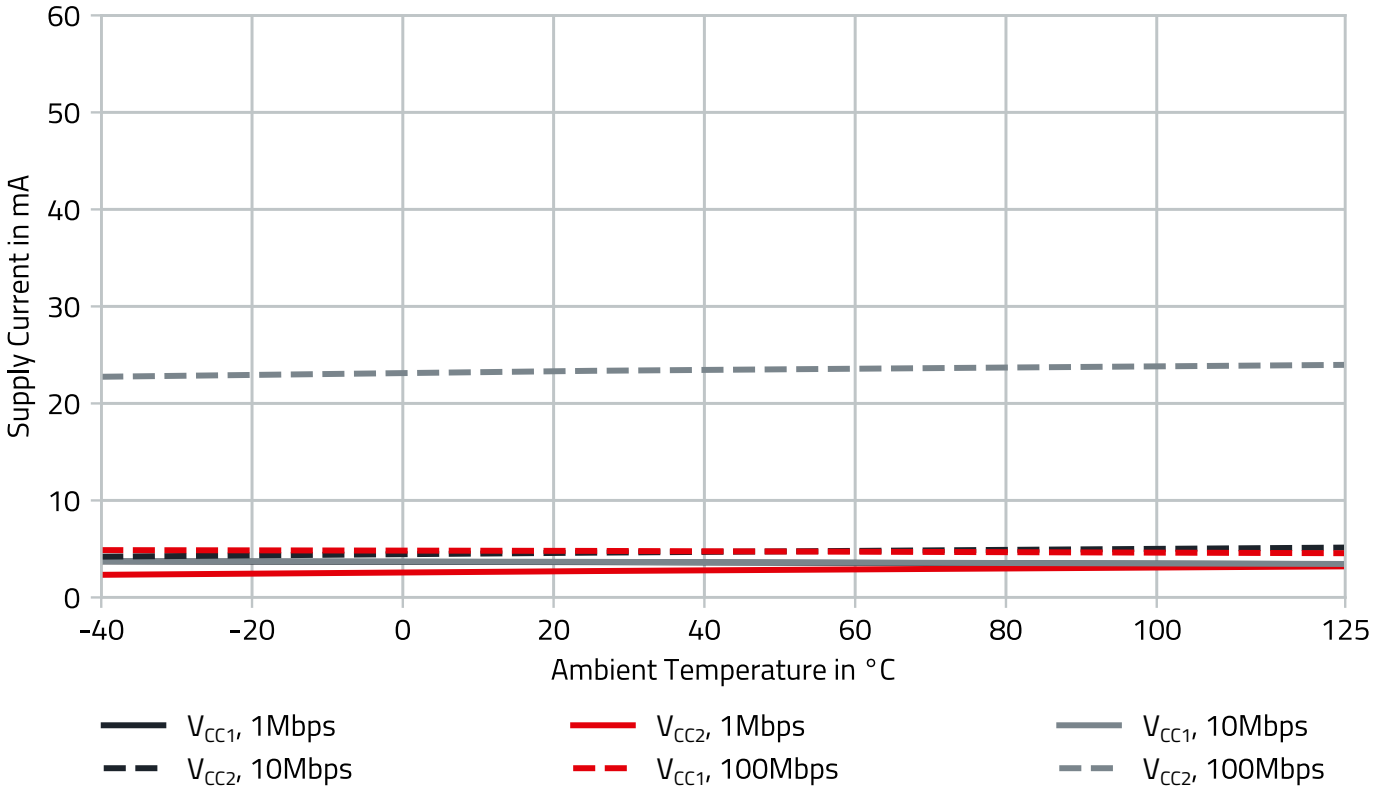



Figure 14: 18014015401x supply current $V_{CC1}$ = $V_{CC2}$ = 2.5V.

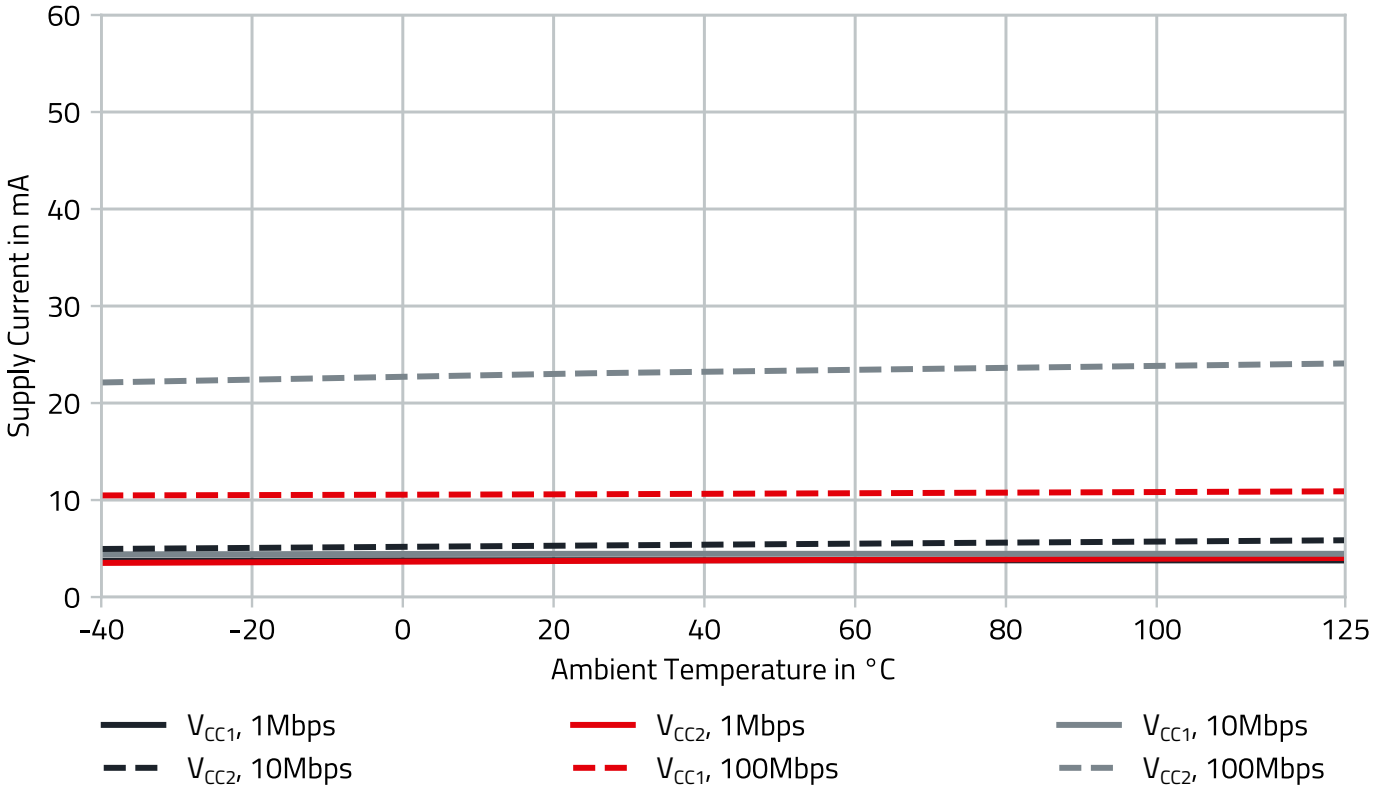



Figure 15: 18014115401x supply current $V_{CC1}$ = $V_{CC2}$ = 5V.

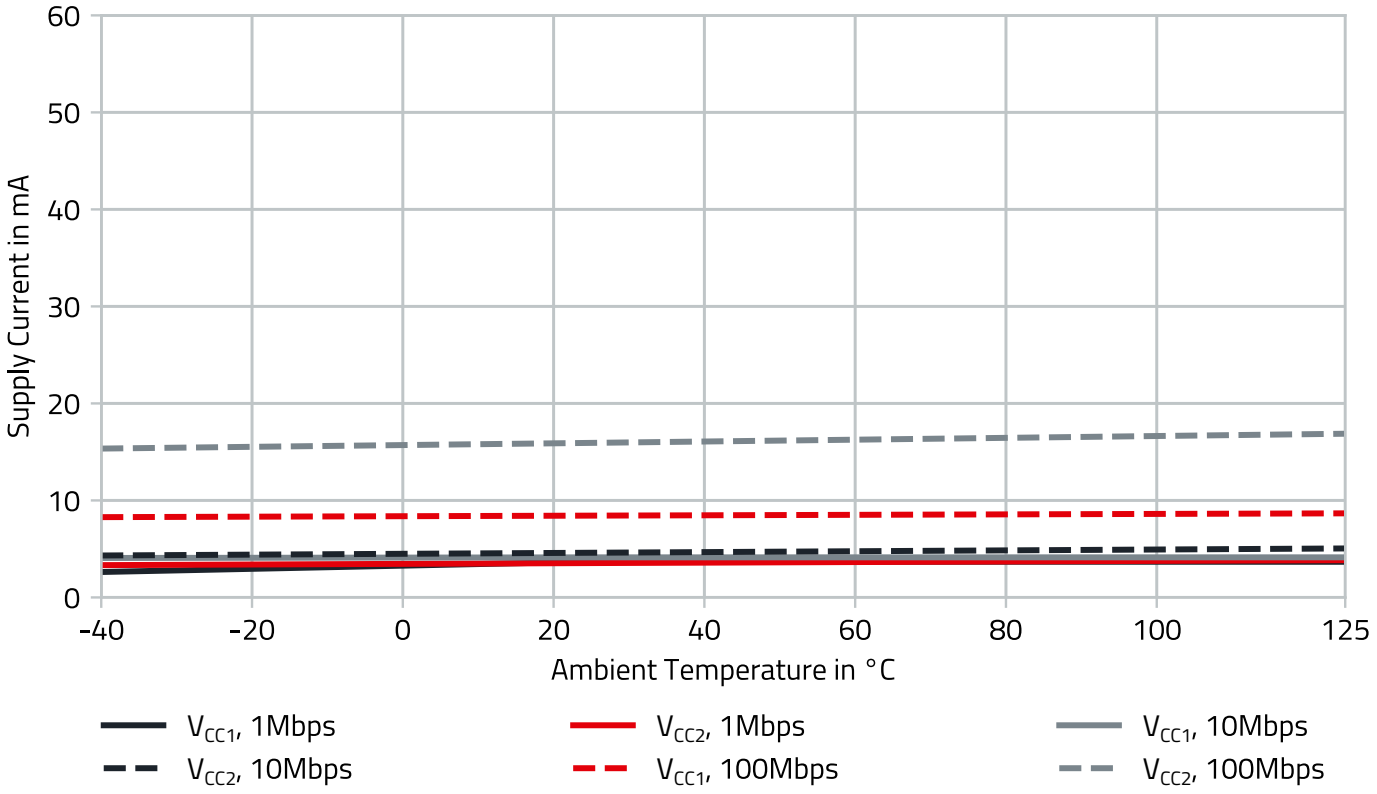



Figure 16: 18014115401x supply current $V_{CC1}$ = $V_{CC2}$ = 3.3V.

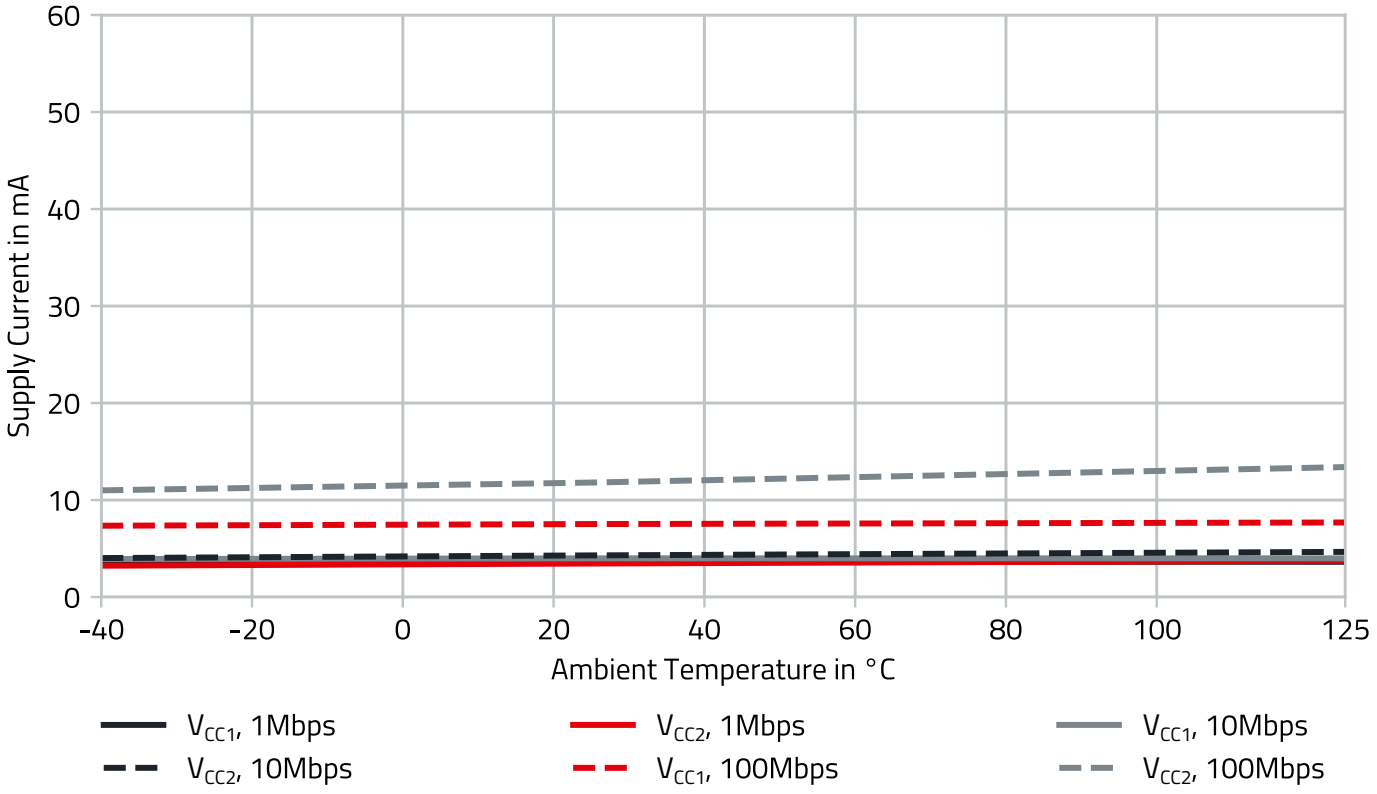



Figure 17: 18014115401x supply current $V_{CC1}$ = $V_{CC2}$ = 2.5V.

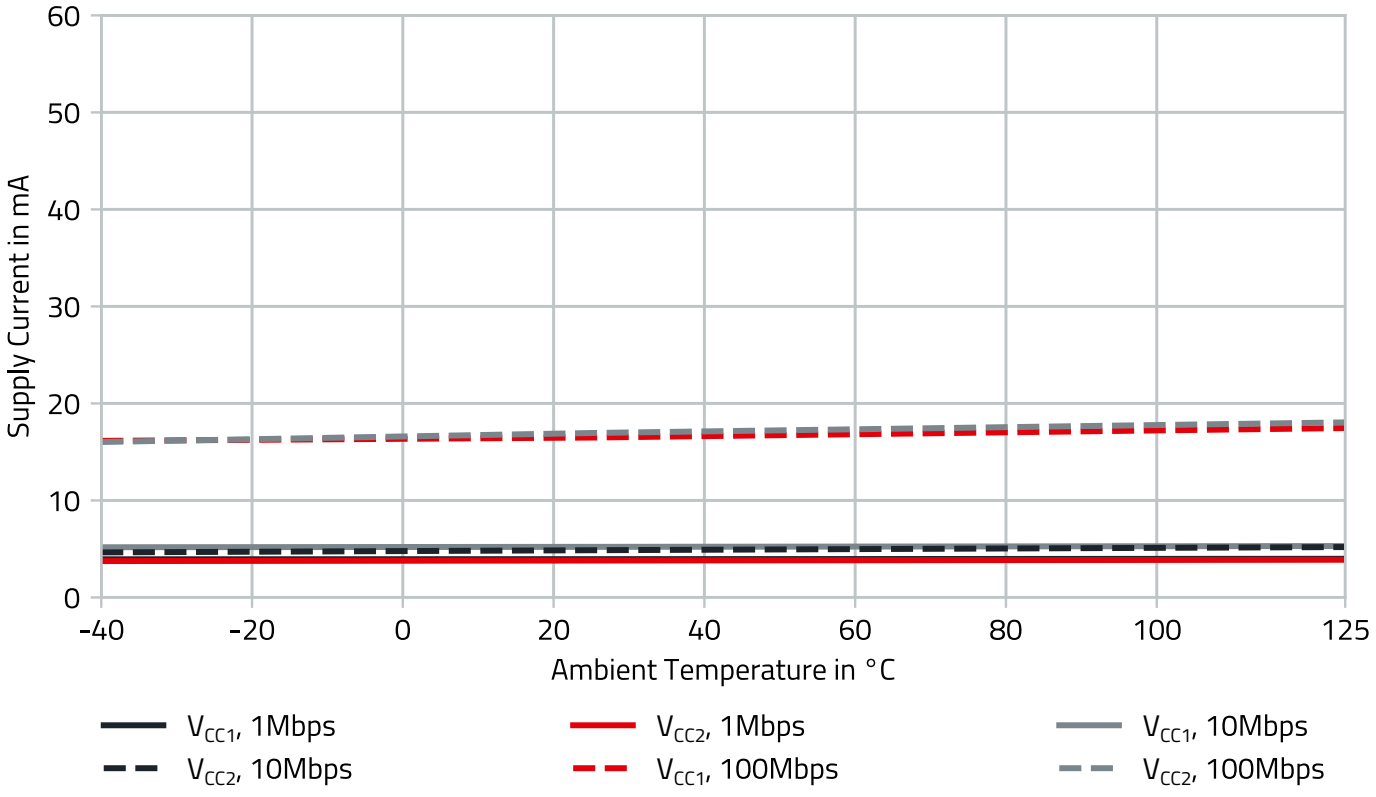



Figure 18: 18014215401x supply current $V_{CC1}$ = $V_{CC2}$ = 5V.

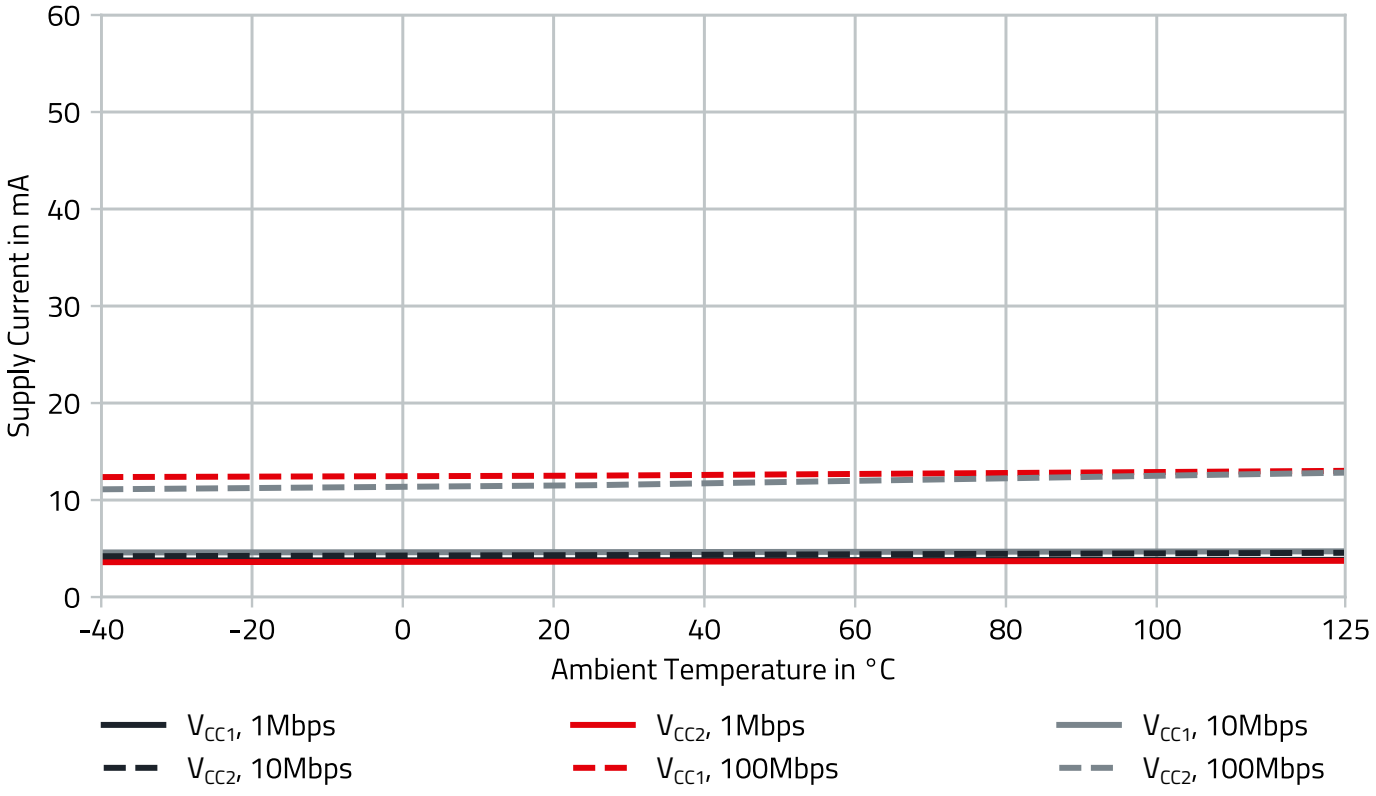



Figure 19: 18014215401x supply current $V_{CC1}$ = $V_{CC2}$ = 3.3V.

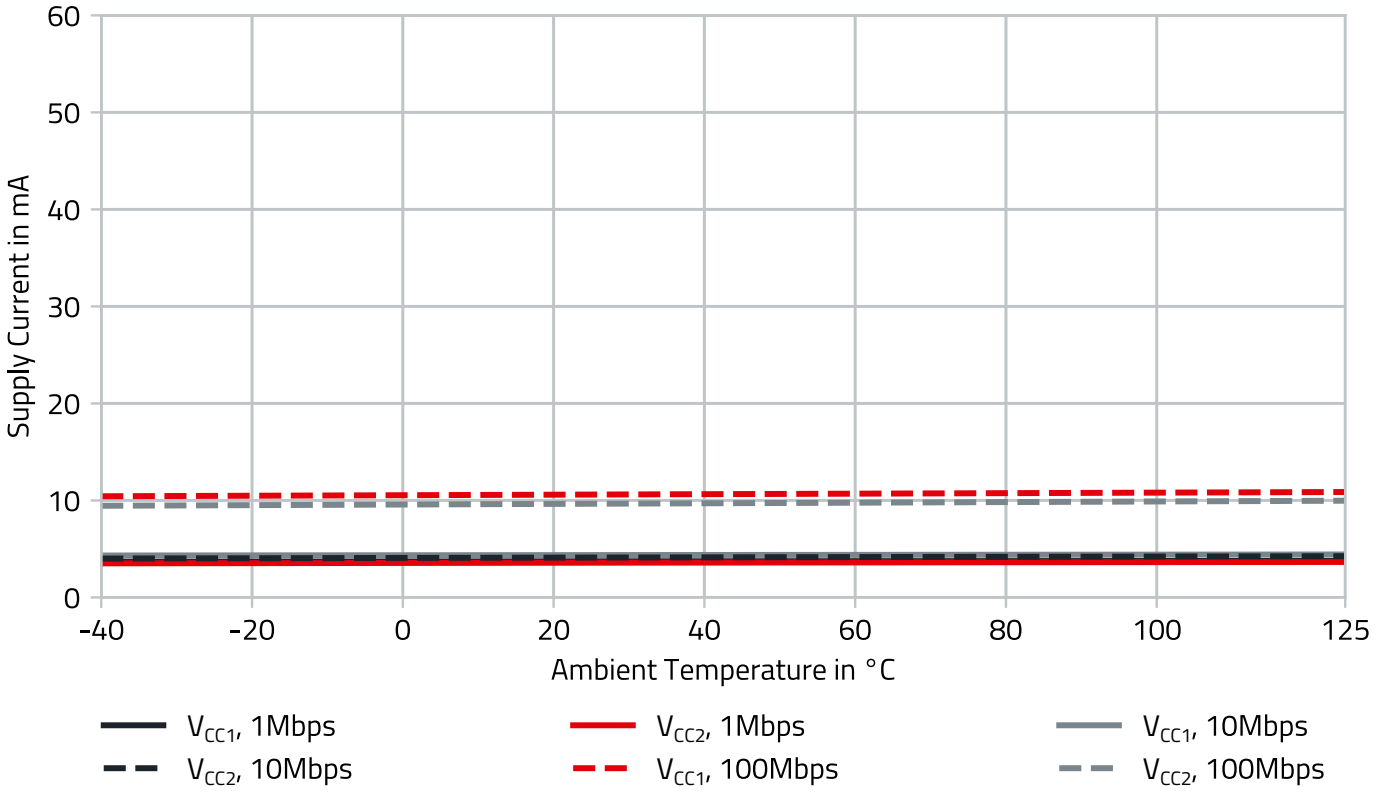



Figure 20: 18014215401x supply current $V_{CC1}$ = $V_{CC2}$ = 2.5V.

### 13.1.4 Supply Current vs. Data Rate

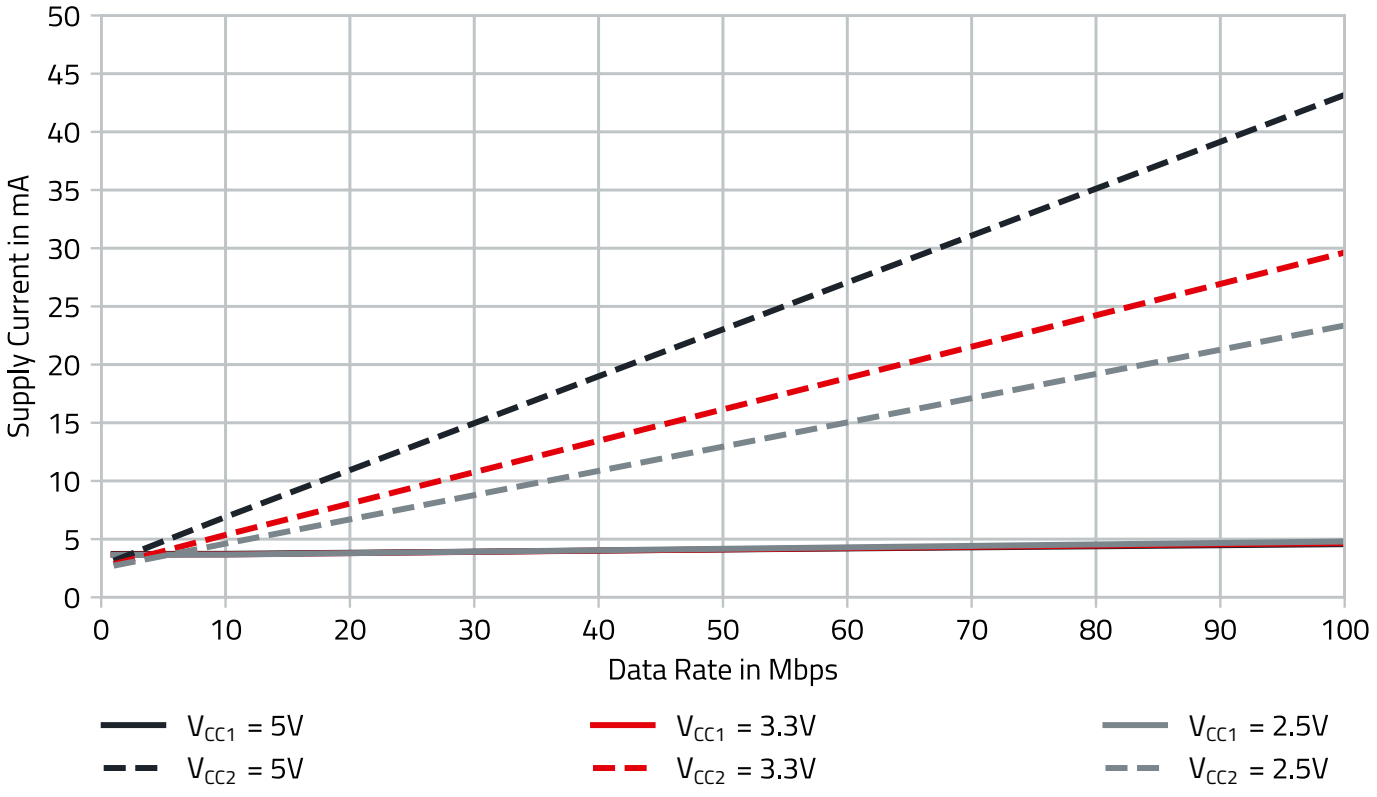



Figure 21: 18014015401x Supply current vs. data rate.

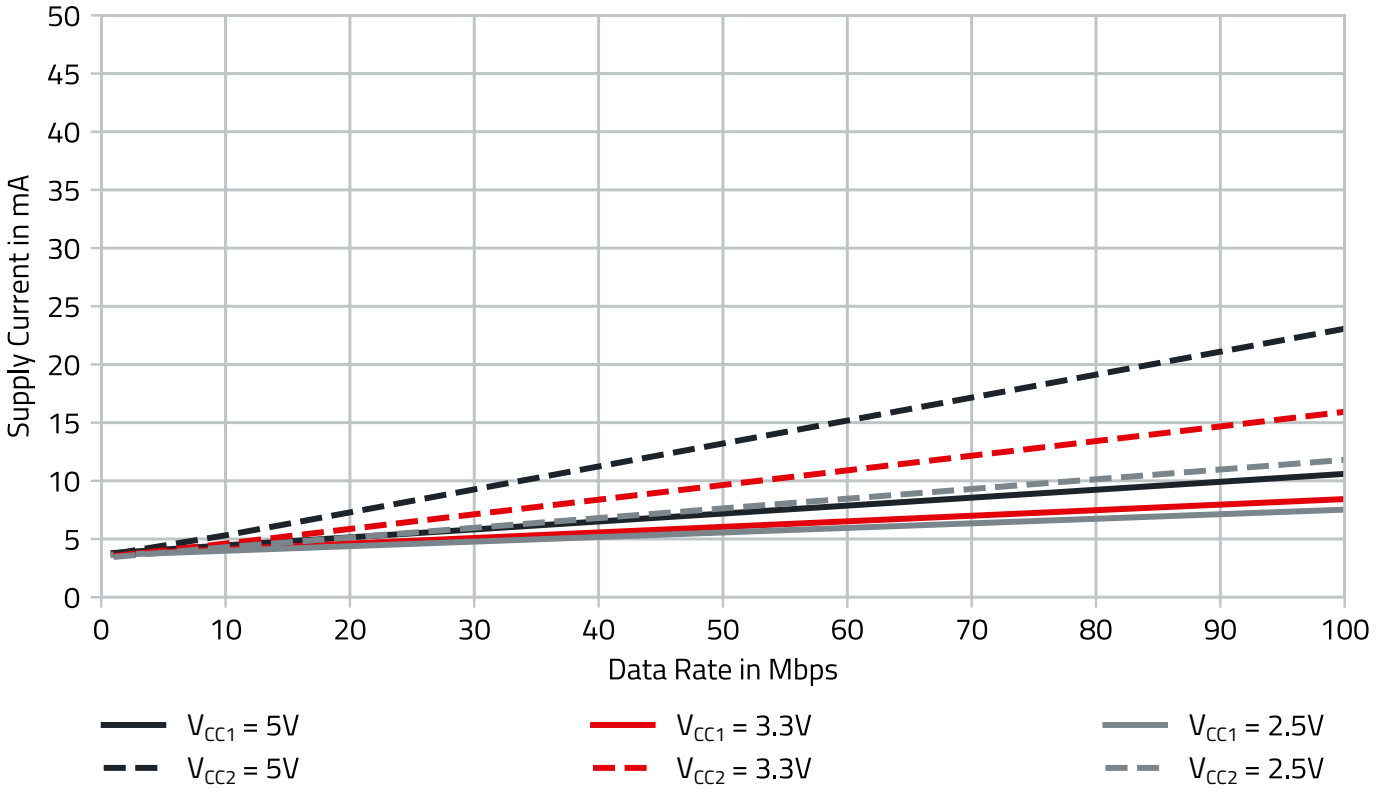



Figure 22: 18014115401x Supply current vs. data rate.

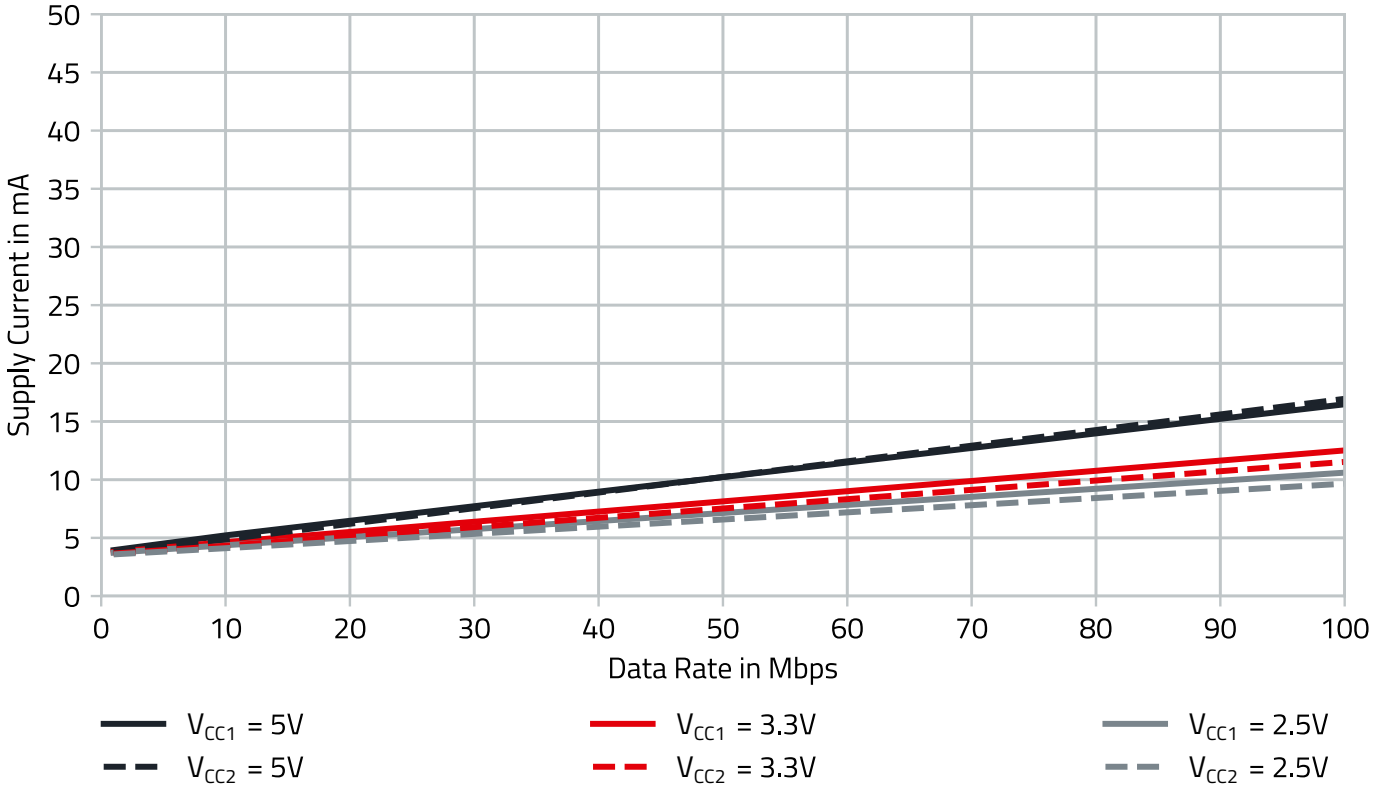



Figure 23: 18014215401x Supply current vs. data rate.

### 13.1.5 High and Low Voltage Levels vs. Output Current

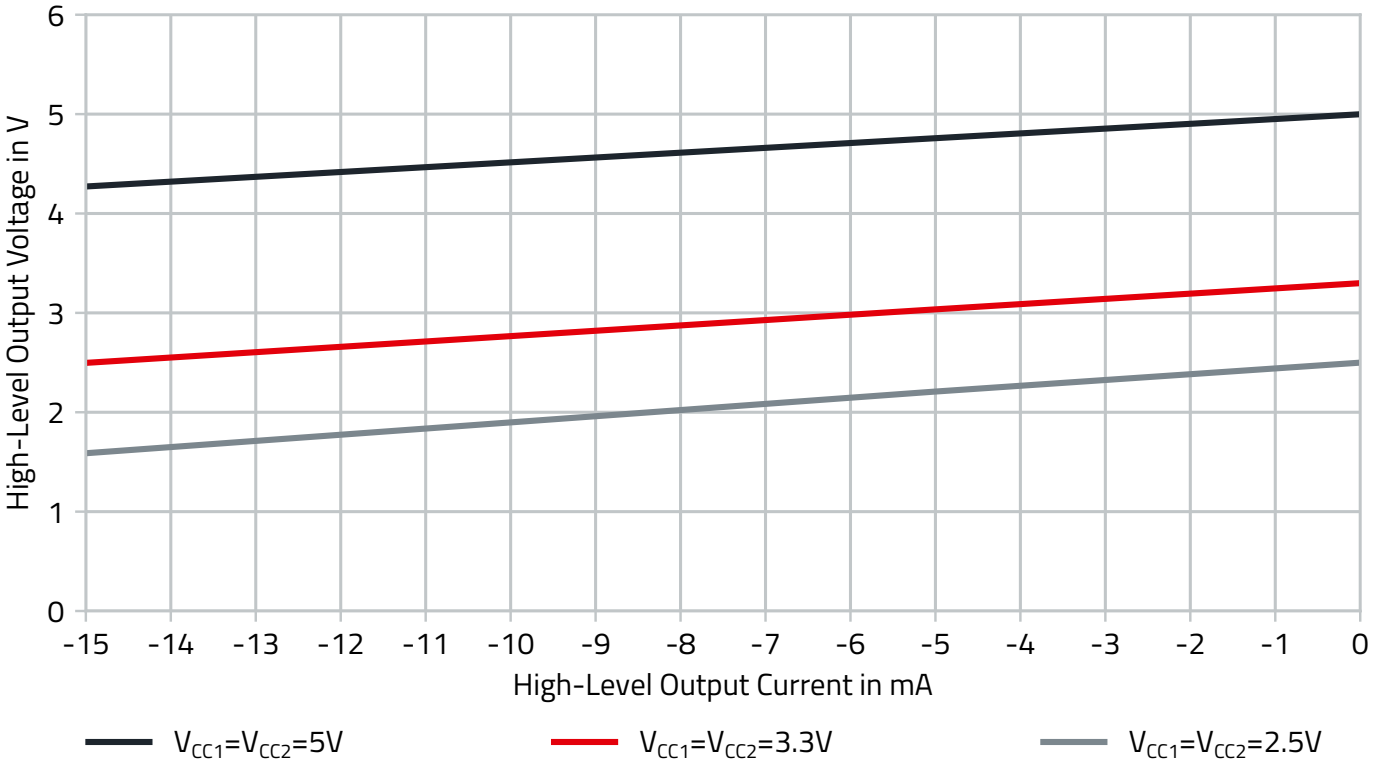



Figure 24: 18014x15401x high-level output voltage vs. high-level output current.

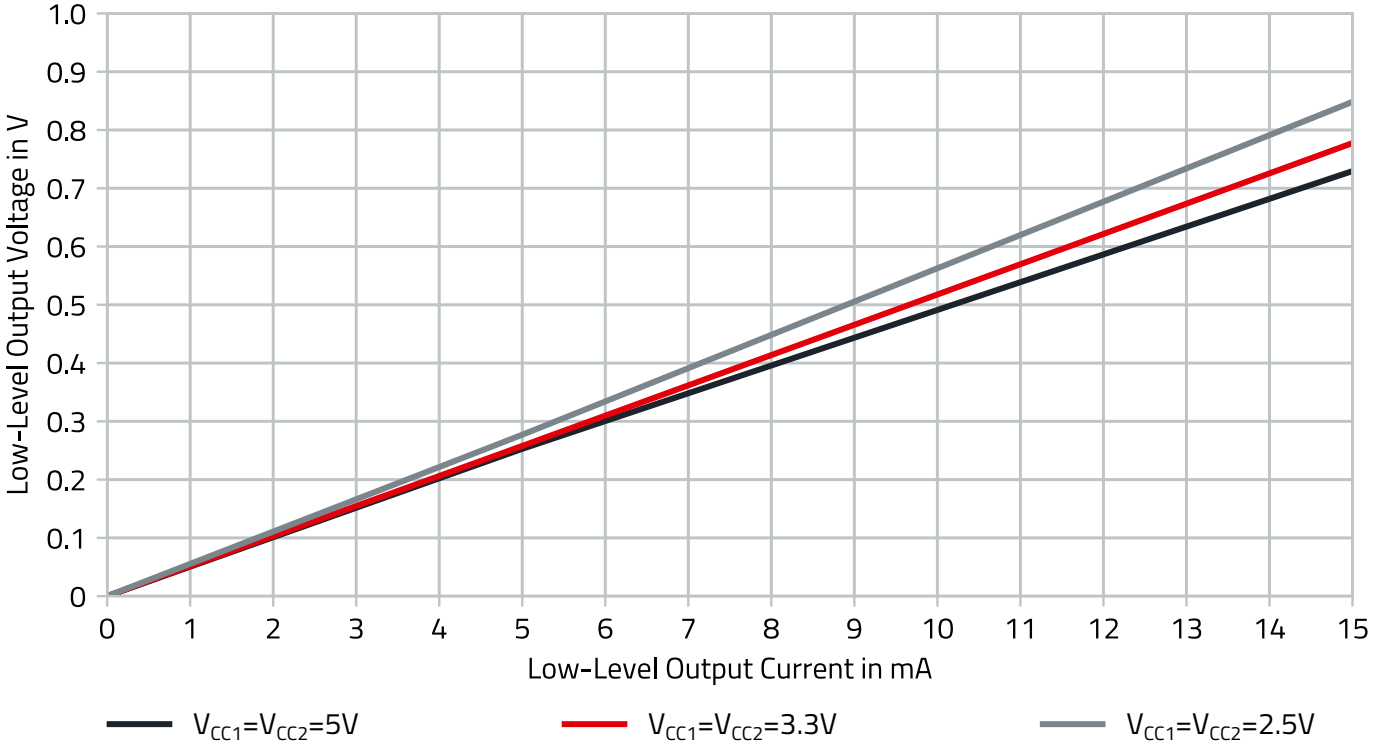



Figure 25: 18014x15401x low-level output voltage vs. low-level output current.

## 14 TRUTH TABLES

Table 15: I/O truth table.

| $V_{CC1}$ | $V_{CC2}$ | Enable ENX | Input $V_{INX}$ | Output $V_{OUTX}$ | Operation |
|---|---|---|---|---|---|
| ≥2.375V | ≥2.375V | H or open | H | H | Normal operation: The channel output follows the logic state of its input. |
| | | H or open | L | L | |
| | | H or open | Open | Default | Default output: When input $V_{INX}$ is open, the corresponding channel output goes to its default logic state. |
| X | ≥2.375V | L | X | Z | High impedance: A low level at the Enable pin causes the channel output to enter a high impedance state. |
| ≤2V | ≥2.375V | H or Open | X | Default | Default output: When the primary supply is unpowered, a channel output assumes the logic state based on its default configuration. Parts with H have a default of high while parts with L have a default of low. |
| X | ≤2V | X | X | Undetermined | If $V_{CC2}$ is unpowered, the channel output is undetermined. |

Table 16: Enable truth table.

| Part Number | EN1 | EN2 | Operation |
|---|---|---|---|
| 18014015401x | — | H | Secondary side outputs $V_{OUTX}$ are enabled and each output follows the logic state of its corresponding input. |
| | — | L | Secondary side outputs $V_{OUTX}$ are disabled and each output will exhibit a high impedance state. |
| 18014115401x | H | X | Primary side outputs $V_{OUT4}$ is enabled and follows the logic state of its corresponding input. |
| | L | X | Primary side outputs $V_{OUT4}$ is disabled and the output will exhibit a high impedance state. |
| | X | H | Secondary side outputs $V_{OUT1}$, $V_{OUT2}$ and $V_{OUT3}$ are enabled and each output follows the logic state of its corresponding input. |
| | X | L | Secondary side outputs $V_{OUT1}$, $V_{OUT2}$ and $V_{OUT3}$ are disabled and each output will exhibit a high impedance state. |
| 18014215401x | H | X | Primary side outputs $V_{OUT3}$ and $V_{OUT4}$ are enabled and follows the logic state of its corresponding input. |
| | L | X | Primary side outputs $V_{OUT3}$ and $V_{OUT4}$ are disabled and the output will exhibit a high impedance state. |
| | X | H | Secondary side outputs $V_{OUT1}$ and $V_{OUT2}$ are enabled and each output follows the logic state of its corresponding input. |
| | X | L | Secondary side outputs $V_{OUT1}$ and $V_{OUT2}$ are disabled and each output will exhibit a high impedance state. |

Note: The enable signal must follow the limitations specified in the ELECTRICAL SPECIFICATIONS.

## 15 I/O DESCRIPTION

Table 17: I/O schematics.

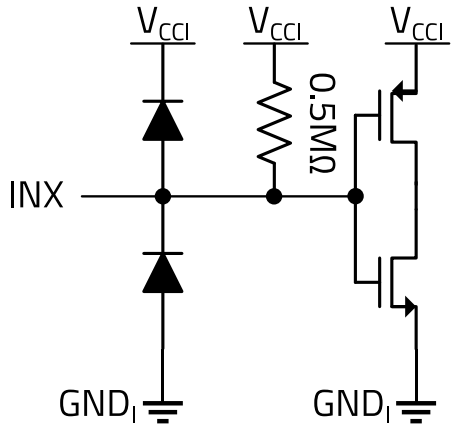



Figure 26: Default high channel input internal structure.

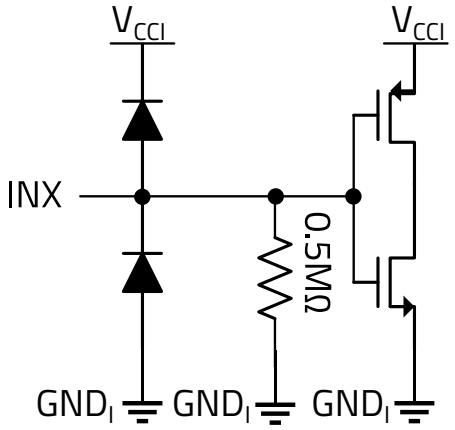



Figure 27: Default low channel input internal structure.

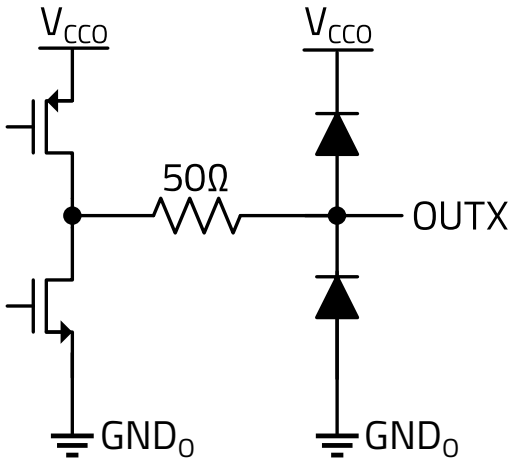



Figure 28: Channel output internal structure.

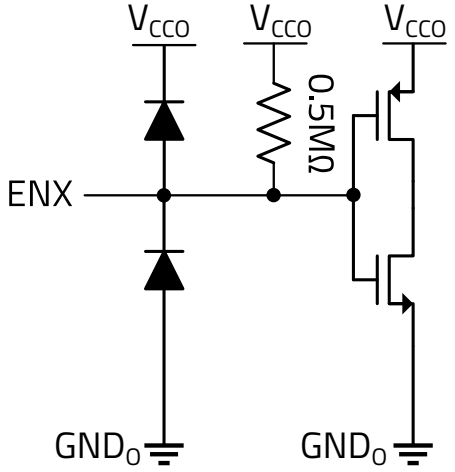



Figure 29: Channel enable internal structure.

NOTE: For forward channels $V_{CCI} = V_{CC1}$, $V_{CCO} = V_{CC2}$, $GND_I$ = GND1 and $GND_O$ = GND2.
For reverse channels $V_{CCI} = V_{CC2}$, $V_{CCO} = V_{CC1}$, $GND_I$ = GND2 and $GND_O$ = GND1.

## 16 TEST SCHEMATICS

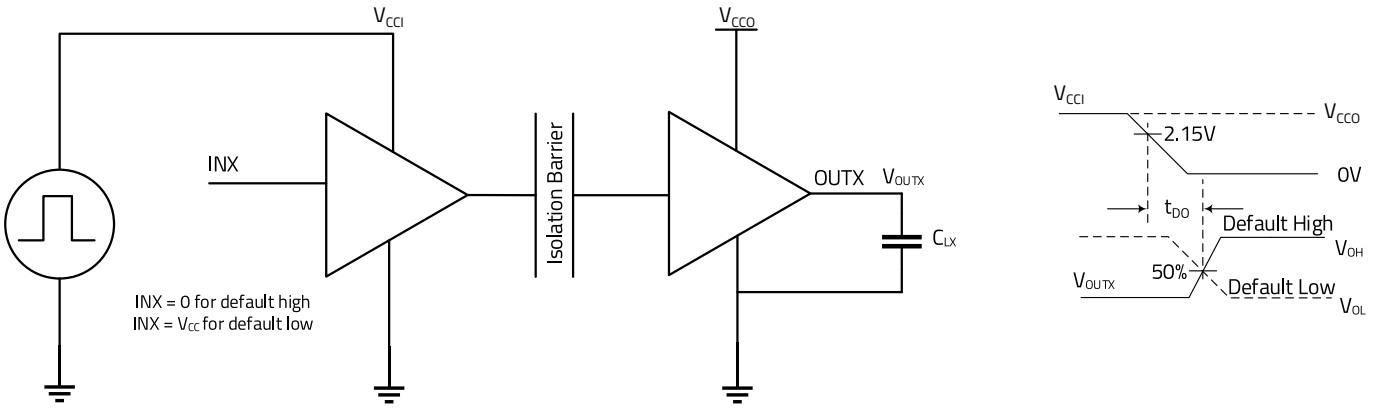



Figure 30: Default output delay test schematic.

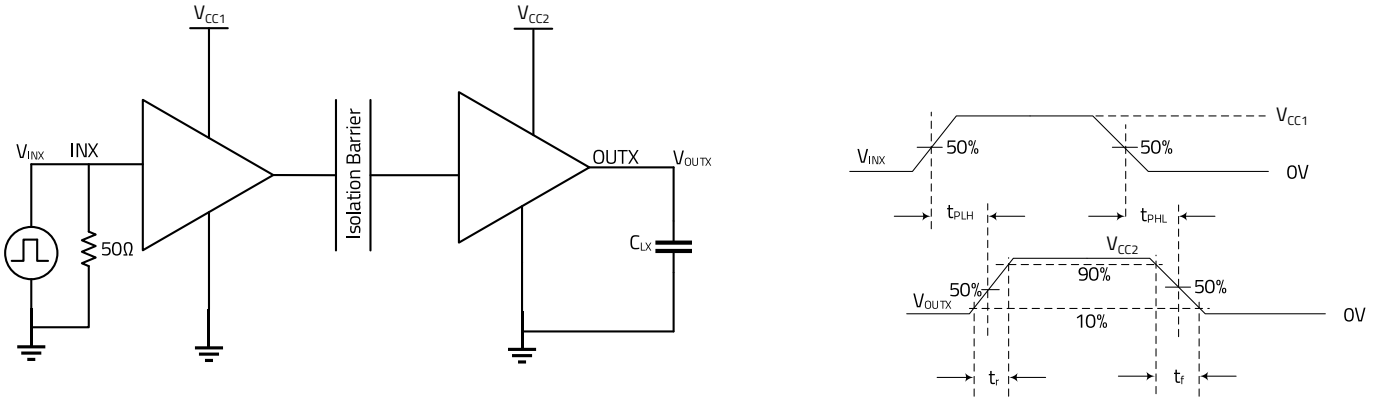



Figure 31: Propagation delay test schematic.

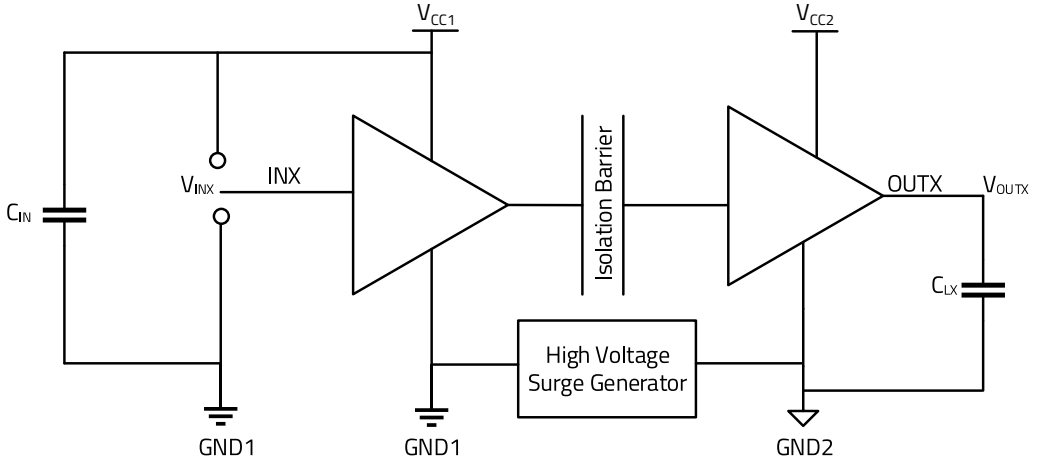



Figure 32: CMTI test schematic.

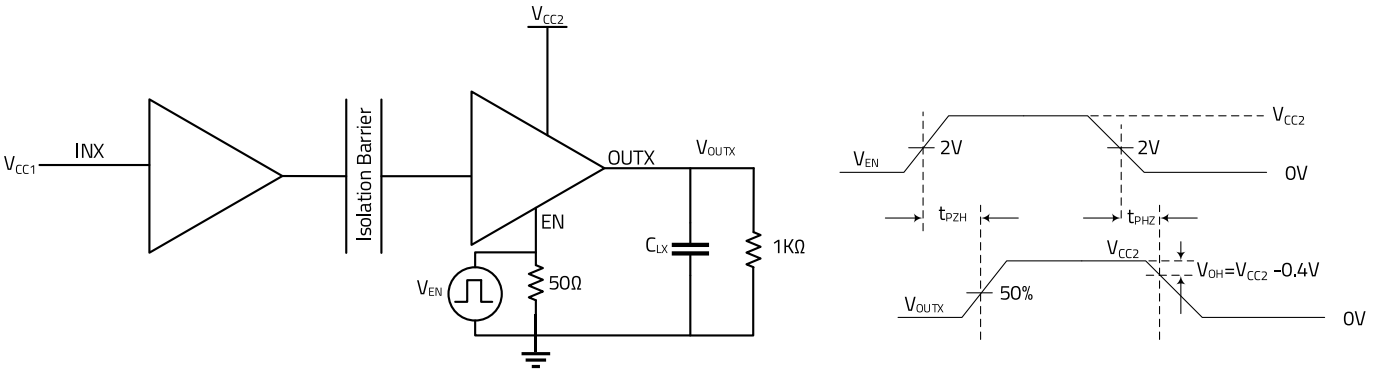



Figure 33: Enable/disable channel input high test schematic.

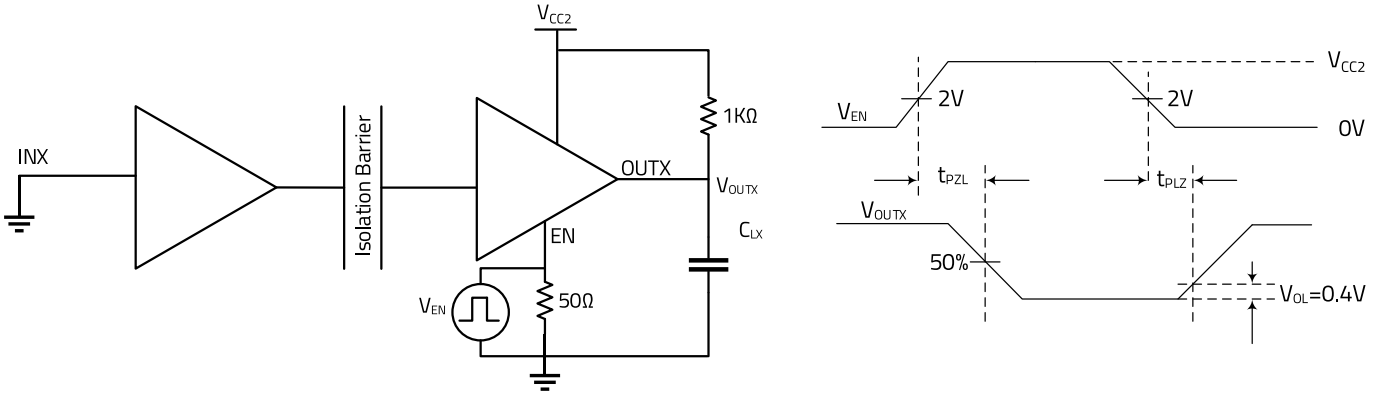



Figure 34: Enable/disable channel input low test schematic.

Note: $C_{LX}$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

## 17 BLOCK DIAGRAM

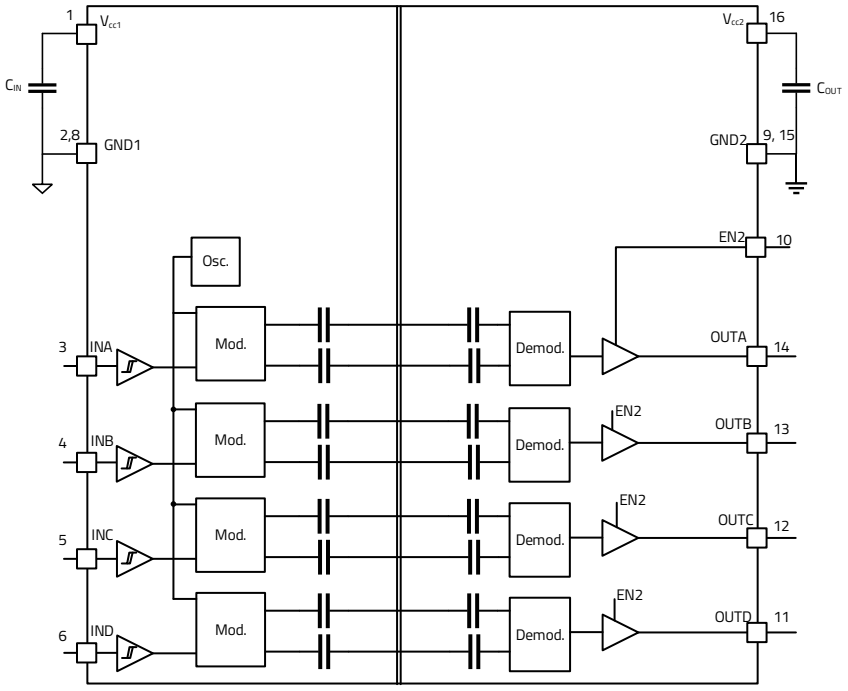



Figure 35: 18014015401x block diagram.

## 18 CIRCUIT DESCRIPTION

The WPME-CDIS digital isolator consists of four capacitive isolated digital channels that must be powered by two isolated supply voltages. The device is typically operated using 5V, 3.3V or 2.5V and the primary and secondary sides can be independently powered with any voltage within the operating conditions. The WPME-CDIS integrates the isolation capacitors in addition to the modulators and demodulators needed to construct the four isolated channels.

The isolation channels are realized using on/off key (OOK) modulation to transmit high or low speed signals through silicon dioxide isolation barriers. The on-chip oscillator is used to modulate the schmitt-triggered input signal. The modulator generates a differential signal that is transmitted through the capacitive isolation lines. The demodulator is located on the output side of the signal channel and used to amplify, filter and reconstruct the input signal with minimum propagation delay and distortion. Finally, the output of the demodulator is given to the output through buffer to improve the driving strength.

## 19 PROTECTION FEATURES

### 19.1 Input/Output Undervoltage Lockout (UVLO)

The device incorporates input and output undervoltage lockout (UVLO) to protect from unexpected behavior at input voltages below the recommended values. The thresholds of the UVLO are indicated in the ELECTRICAL SPECIFICATIONS.

## 20 TYPICAL APPLICATION

The figure below depicts a typical application for a digital isolator used in serial port interface (SPI) communication between a microcontroller and analog to digital converter (ADC).

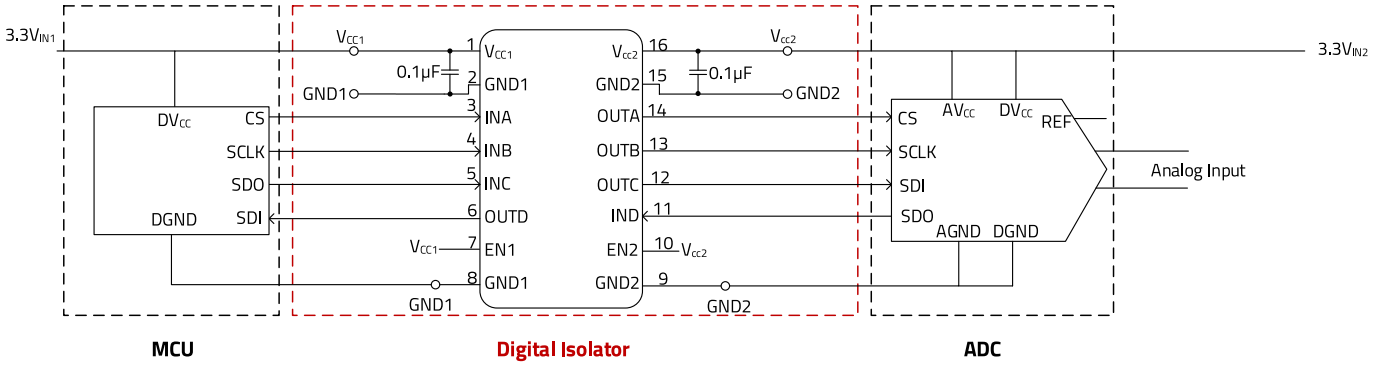



Figure 36: Typical application: SPI bus.

The 18014115401H and 18014115401L are shown in the above diagram in a conventional SPI implementation. The channel configuration allows for appropriate isolation and communication between the controller and peripheral devices.

## 21 HANDLING RECOMMENDATIONS

1. The digital isolator is classified as MSL3 (JEDEC Moisture Sensitivity Level 3) and requires special handling due to moisture sensitivity (JEDEC J-STD033D).
2. The parts are delivered in a sealed bag (Moisture Barrier Bag = MBB) and should be processed within one year.
3. When opening the moisture barrier bag, check the Humidity Indicator Card (HIC) for the color status. Bake parts prior to soldering in case indicator color has changed according to the notes on the card.
4. Parts must be processed after 168 hour (7 days) of floor life. Once this time has been exceeded, bake parts prior to soldering per JEDEC J-STD033D recommendation.
5. Maximum number of soldering cycles is two.
6. For minimum risk, solder the device in the last solder cycle of the PCB production.
7. The component lead material is copper (Cu) and the lead finish is Matte Sn (Matte Sn).
8. For solder paste use a standard SAC Alloy such as SAC 305, type 3 or higher.
9. The profile below is valid for convection reflow only.
10. Other soldering methods (e.g. vapor phase) are not verified and have to be validated by the customer at their own risk.

### 21.1 Soldering Profile

Table 18: Reflow solder profile.

| Profile Feature | Symbol | Value |
|---|---|---|
| Preheat temperature minimum | $T_{s\_min}$ | 150 °C |
| Preheat temperature maximum | $T_{s\_max}$ | 200 °C |
| Preheat time from $T_{s\_min}$ to $T_{s\_max}$ | $t_s$ | 60-120 seconds |
| Liquidous temperature | $T_L$ | 217 °C |
| Time maintained above $T_L$ | $t_L$ | 60-90 seconds |
| Classification temperature | $T_C$ | 260 °C |
| Peak package body temperature | $T_P$ | $T_P \leq T_C$ |
| Time within $T_C$ - 5 °C and $T_C$ | $t_P$ | $t_P \leq 30$ seconds |
| Ramp-up Rate ($T_L$ to $T_p$) | | 3 °C/second maximum |
| Ramp-down rate ($T_p$ to $T_L$) | | 6 °C/second maximum |
| Time 25 °C to peak temperature | | 8 minutes maximum |

Please refer to JEDEC J-STD020 for further information pertaining to reflow soldering of electronic components.

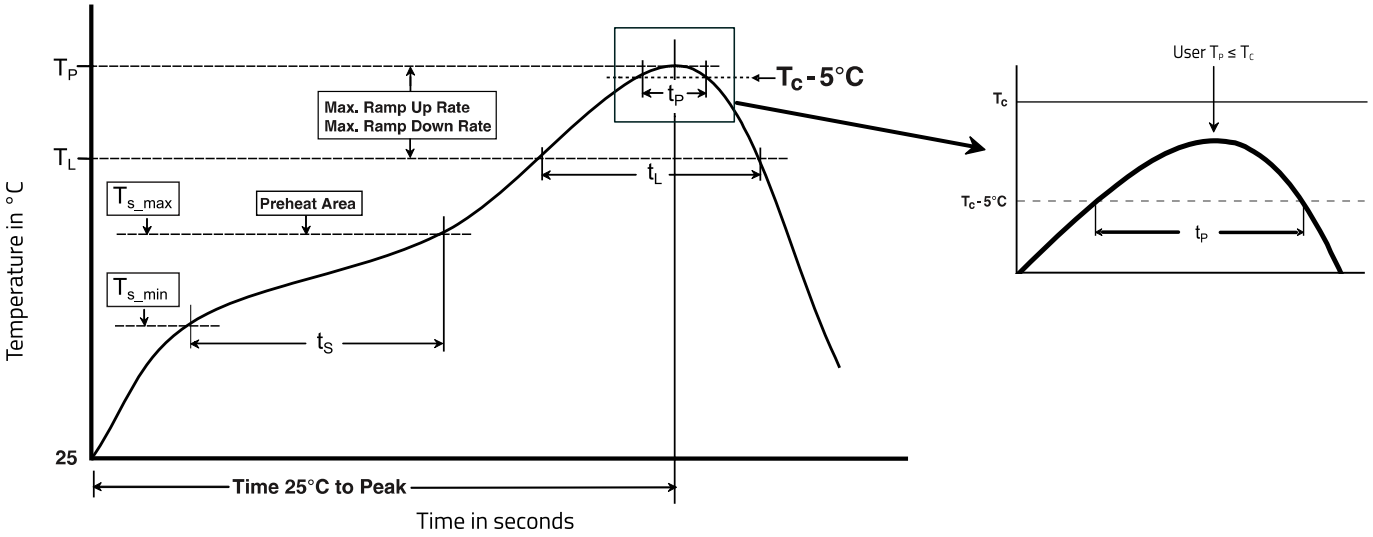



Figure 37: Soldering profile.

## 22 PHYSICAL DIMENSIONS

### 22.1 Component

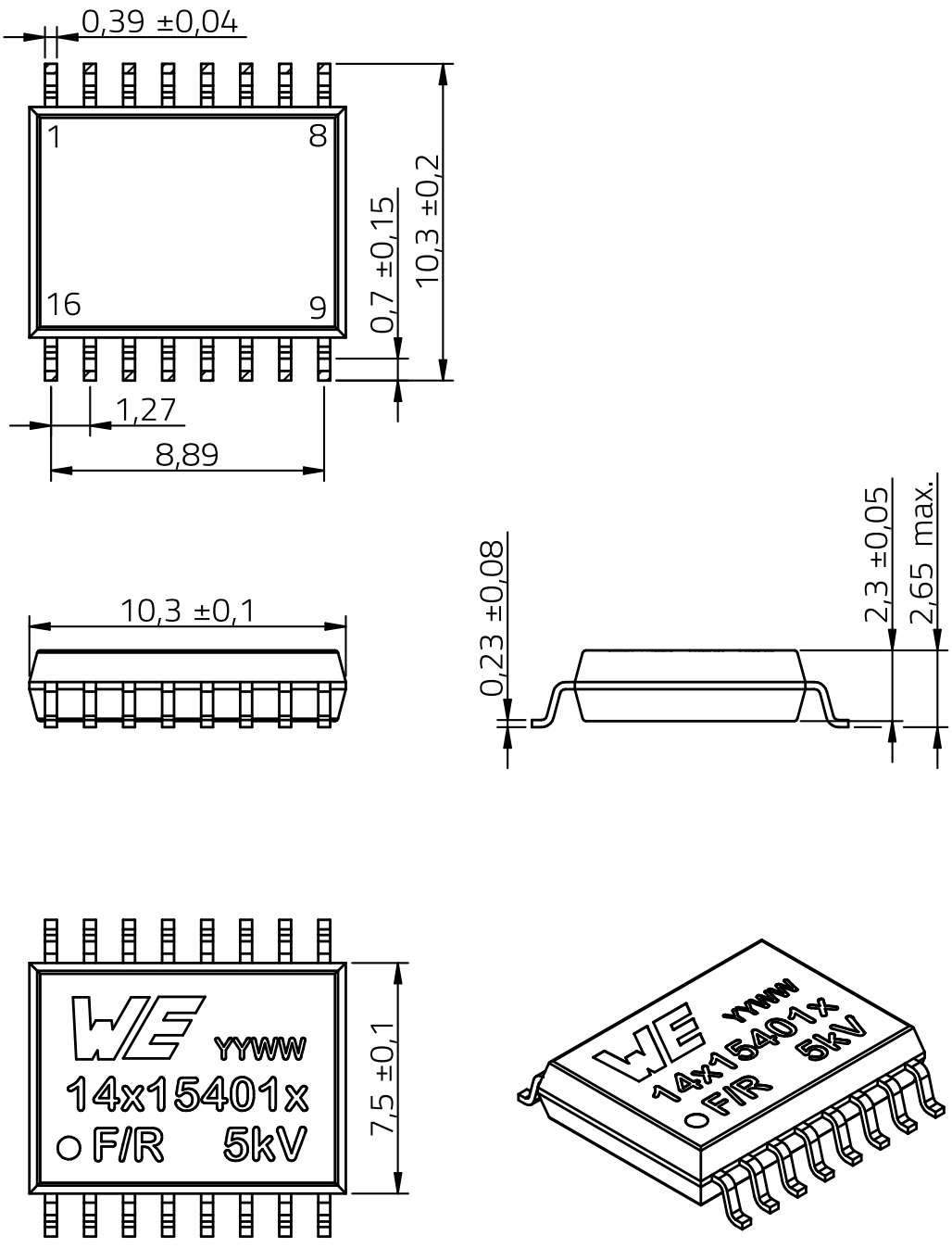



Figure 38: Component dimensions.

All dimensions in mm
Tolerance: xx.x =±0.5mm ; xx.xx = ±0.25mm unless otherwise noted

### 22.2 Recommended Landpattern

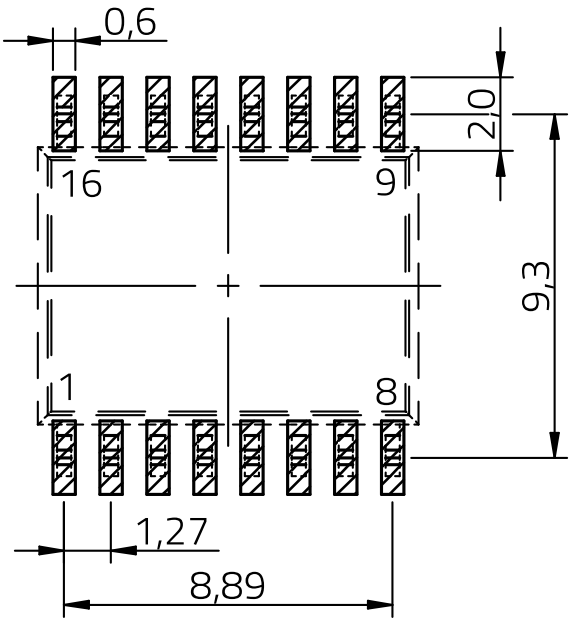



Figure 39: Recommended landpattern dimensions.
All dimensions in mm.

### 22.3 Packaging

**Reel in mm**

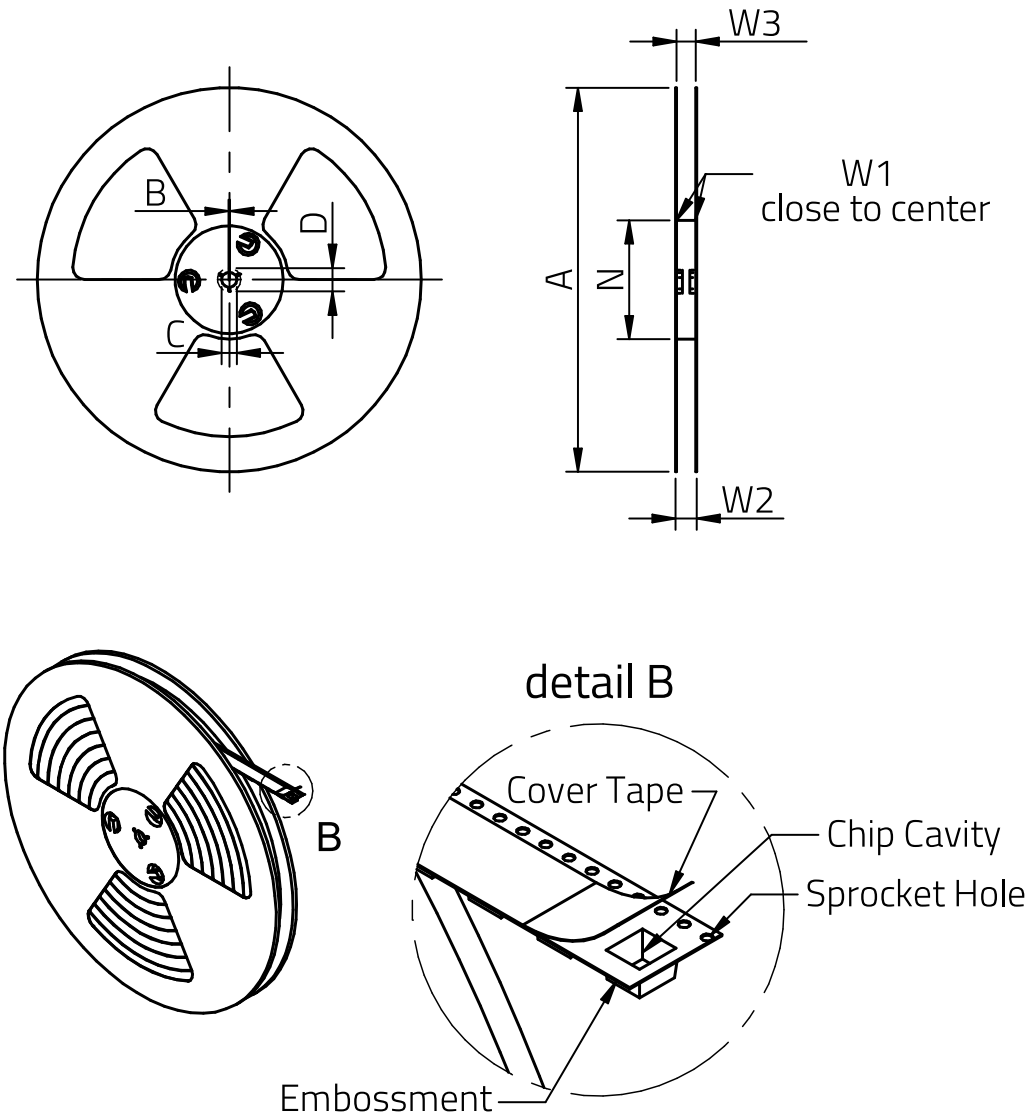



Figure 40: Reel dimensions.

Table 19: Reel dimensions.

| A | B | C | D | N | W1 | W2 | W3 | W3 |
|---|---|---|---|---|---|---|---|---|
| ±2.00 | min. | min. | min. | min. | +2.00 | max. | min. | max. |
| 330.00 | 1.50 | 12.80 | 20.20 | 60.00 | 16.40 | 22.40 | 15.90 | 19.40 |

Reel material is polystyrene.
All dimensions in mm.

### Tape in mm

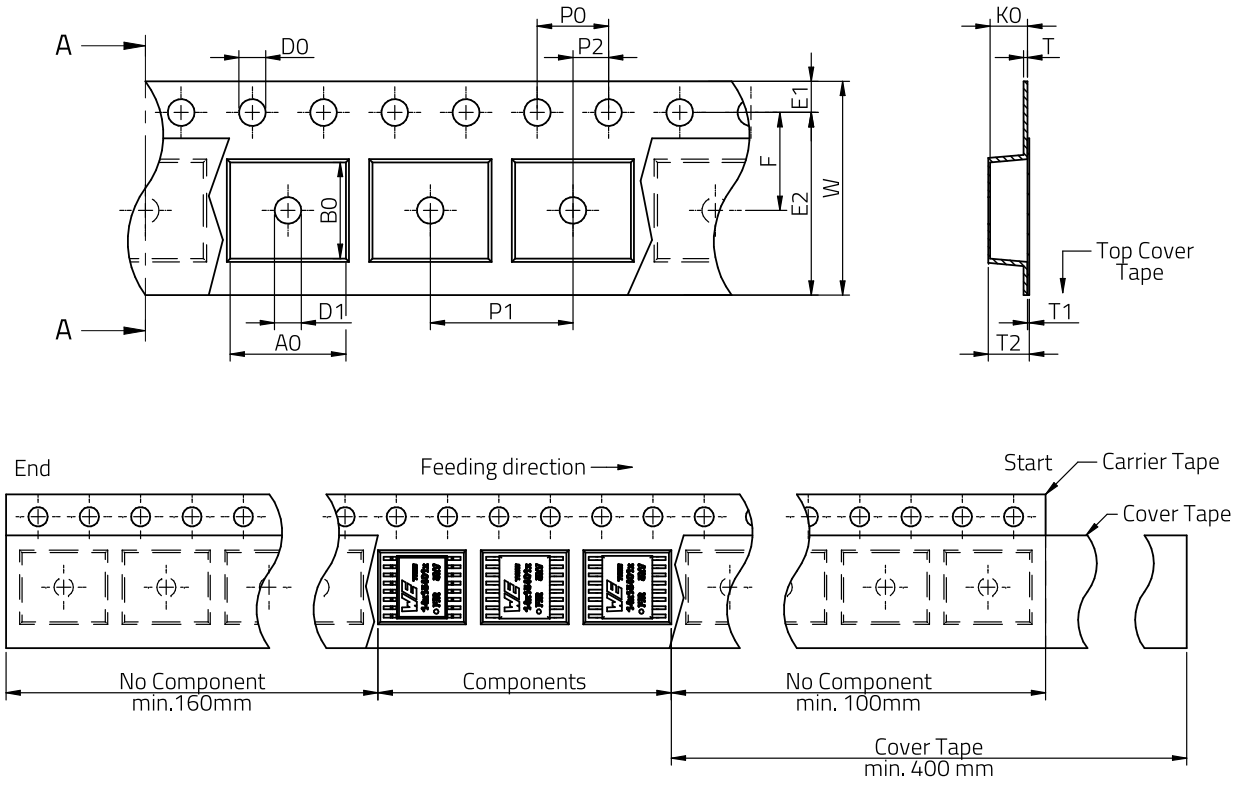



Figure 41: Tape dimensions.

Table 20: Tape dimensions part 1.

| A0 | B0 | D0 | D1 | E1 | E2 | F | P0 | P1 | P2 | W |
|---|---|---|---|---|---|---|---|---|---|---|
| typ. | typ. | min. | ±0.10 | min. | ±0.10 | ±0.10 | ±0.10 | ±0.10 | ±0.10 | ±0.10 |
| 10.90 | 10.70 | 1.50 | 1.50 | 1.75 | 14.25 | 7.50 | 4.00 | 12.00 | 2.00 | 16.00 |

Table 21: Tape dimensions part 2.

| K0 | T | T1 | T2 |
|---|---|---|---|
| typ. | typ. | ref. | typ. |
| 3.2 | 0.35 | 0.1 | 3.4 |

Tape material is polystyrene.
All dimensions in mm.

## 23 DOCUMENT HISTORY

Table 22: Document history.

| Revision | Date | Description | Comment |
|---|---|---|---|
| 1.0 | September 2023 | Initial release of data sheet | |

## 24 LIST OF FIGURES

## 25 LIST OF TABLES

## 26 CAUTIONS AND WARNINGS

**The following conditions apply to all goods within the product series of digital isolators of Würth Elektronik eiSos GmbH & Co. KG:**

**General:**

- All recommendations according to the general technical specifications of the datasheet have to be complied with.
- The usage and operation of the product within ambient conditions which probably alloy or harm the component surface has to be avoided.
- The responsibility for the applicability of customer specific products and use in a particular customer design is always within the authority of the customer. All technical specifications for standard products do also apply for customer specific products
- Residual washing varnish agent that is used during the production to clean the application might change the characteristics of the body, pins or termination. The washing varnish agent could have a negative effect on the long term function of the product. Direct mechanical impact to the product shall be prevented as the material of the body, pins or termination could flake or in the worst case it could break. As these devices are sensitive to electrostatic discharge customer shall follow proper IC Handling Procedures.
- Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Würth Elektronik eiSos GmbH & Co. KG components in its applications, notwithstanding any applications-related information or support that may be provided by Würth Elektronik eiSos GmbH & Co. KG.
- Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences lessen the likelihood of failures that might cause harm and take appropriate remedial actions
- Customer will fully indemnify Würth Elektronik eiSos and its representatives against any damages arising out of the use of any Würth Elektronik eiSos GmbH & Co. KG components in safety-critical applications

**Product specific:**

Follow all instructions mentioned in the datasheet, especially:

- The solder profile has to comply with the technical reflow or wave soldering specification, otherwise this will void the warranty.
- All products are supposed to be used before the end of the period of 12 months based on the product date-code.
- Violation of the technical product specifications such as exceeding the absolute maximum ratings will void the warranty.
- It is also recommended to return the body to the original moisture proof bag and reseal the moisture proof bag again.
- ESD prevention methods need to be followed for manual handling and processing by machinery.

**Disclaimer:**

This electronic component has been designed and developed for usage in general electronic equipment only. This product is not authorized for use in equipment where a higher safety standard and reliability standard is especially required or where a failure of the product is reasonably expected to cause severe personal injury or death, unless the parties have executed an agreement specifically governing such use. Moreover Würth Elektronik eiSos GmbH & Co. KG products are neither designed nor intended for use in areas such as military, aerospace, aviation, nuclear control, submarine, transportation (automotive control, train control, ship control), transportation signal, disaster prevention, medical, public information network etc. Würth Elektronik eiSos GmbH & Co. KG must be informed about the intent of such usage before the design-in stage. In addition, sufficient reliability evaluation checks for safety must be performed on every electronic component which is used in electrical circuits that require high safety and reliability functions or performance. These cautions and warnings comply with the state of the scientific and technical knowledge and are believed to be accurate and reliable. However, no responsibility is assumed for inaccuracies or incompleteness.

## 27 IMPORTANT NOTES

### General Customer Responsibility

Some goods within the product range of Würth Elektronik eiSos GmbH & Co. KG contain statements regarding general suitability for certain application areas. These statements about suitability are based on our knowledge and experience of typical requirements concerning the areas, serve as general guidance and cannot be estimated as binding statements about the suitability for a customer application. The responsibility for the applicability and use in a particular customer design is always solely within the authority of the customer. Due to this fact it is up to the customer to evaluate, where appropriate to investigate and decide whether the device with the specific product characteristics described in the product specification is valid and suitable for the respective customer application or not. Accordingly, the customer is cautioned to verify that the datasheet is current before placing orders.

### Customer Responsibility Related to Specific, in Particular Safety-Relevant, Applications

It has to be clearly pointed out that the possibility of a malfunction of electronic components or failure before the end of the usual lifetime cannot be completely eliminated in the current state of the art, even if the products are operated within the range of the specifications. In certain customer applications requiring a very high level of safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health it must be ensured by most advanced technological aid of suitable design of the customer application that no injury or damage is caused to third parties in the event of malfunction or failure of an electronic component.

### Best Care and Attention

Any product-specific notes, warnings and cautions must be strictly observed. Any disregard will result in the loss of warranty.

### Customer Support for Product Specifications

Some products within the product range may contain substances which are subject to restrictions in certain jurisdictions in order to serve specific technical requirements. Necessary information is available on request. In this case the field sales engineer or the internal sales person in charge should be contacted who will be happy to support in this matter.

### Product R&D

Due to constant product improvement product specifications may change from time to time. As a standard reporting procedure of the Product Change Notification (PCN) according to the JEDEC-Standard we inform about minor and major changes. In case of further queries regarding the PCN, the field sales engineer or the internal sales person in charge should be contacted. The basic responsibility of the customer as per Section 1 and 2 remains unaffected.

### Product Life Cycle

Due to technical progress and economical evaluation we also reserve the right to discontinue production and delivery of products. As a standard reporting procedure of the Product Termination Notification (PTN) according to the JEDEC Standard we will inform at an early stage about inevitable product discontinuance. According to this we cannot guarantee that all products within our product range will always be available. Therefore it needs to be verified with the field sales engineer or the internal sales person in charge about the current product availability expectancy before or when the product for application design-in disposal is considered. The approach named above does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.

### Property Rights

All the rights for contractual products produced by Würth Elektronik eiSos GmbH & Co. KG on the basis of ideas, development contracts as well as models or templates that are subject to copyright, patent or commercial protection supplied to the customer will remain with Würth Elektronik eiSos GmbH & Co. KG. Würth Elektronik eiSos GmbH & Co. KG does not warrant or represent that any license, either expressed or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, application, or process in which Würth Elektronik eiSos GmbH & Co. KG components or services are used.

### General Terms and Conditions

Unless otherwise agreed in individual contracts, all orders are subject to the current version of the “General Terms and Conditions of Würth Elektronik eiSos Group”, last version available at www.we-online.com.