2 Channel Digital Isolator

DESCRIPTION

The CDIS 18012x15421x is a 2 channel digital isolator series that provides capacitive isolation between the primary and secondary sides of the device.

The digital isolator requires two supply voltages, one for the primary side and one for the secondary side.

The CDIS digital isolator ensures fast time to market and low development costs.

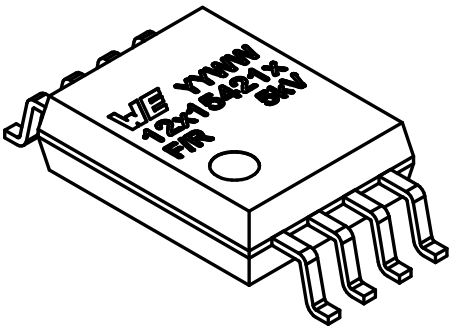
The digital isolator is available in an SOIC-8WB package (5.85 x 11.5 x 2.8)mm.

FEATURES

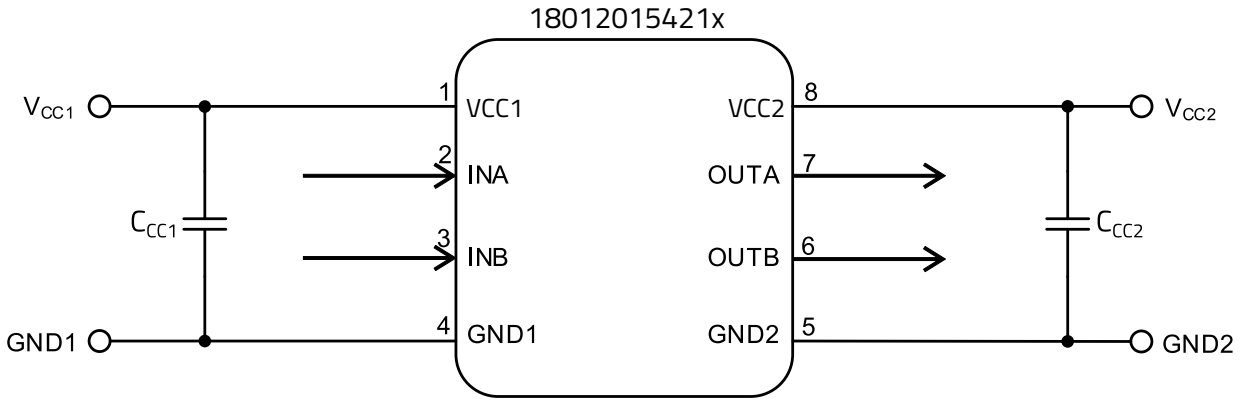
- Isolation Voltage: 5kV$_{RMS}$ for 60s
- Reinforced isolation
- Input voltage range: 2.375V to 5.5V
- Data rate up to 150Mbps
- ±150kV/µs typ. CMTI
- Available channel configurations: 2/0 and 1/1
- Default channel output status: high or low
- Low propagation delay: 12ns typ.
- Ambient temperature range: -40°C to 125°C
- RoHS and REACH compliant
- UL1577 recognized
- DIN EN IEC 60747-17 (VDE 0884-17):2021-10 certified

TYPICAL APPLICATIONS

- Isolated communication interfaces (SPI, CAN, RS-232, RS-485)
- Motor control
- Battery management systems
- Solar inverters
- Test and measurement systems
- Programmable logic controller (PLC) interfaces



TYPICAL CIRCUIT DIAGRAM



The above diagram indicates only one of the possible channel configurations available

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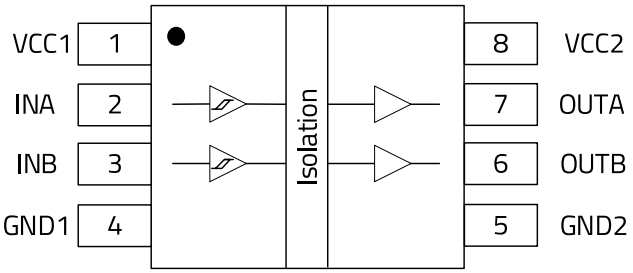
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25 CAUTIONS AND WARNINGS **34**

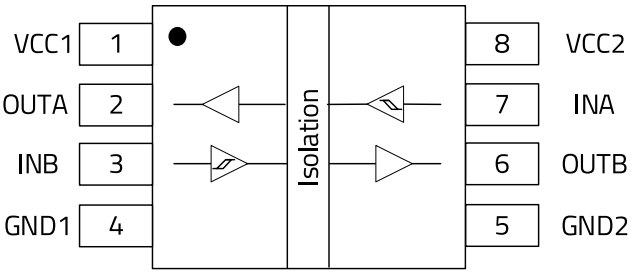
26 IMPORTANT NOTES **35**

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1 PINOUT



18012015421(H/L)



18012115421(H/L)

Figure 1: Pinout.

Table 1: Marking description.

MARKING	DESCRIPTION
WE	Würth Elektronik eiSos GmbH & Co. KG
YYWW	Year and calendar week
12x15421x	Order code

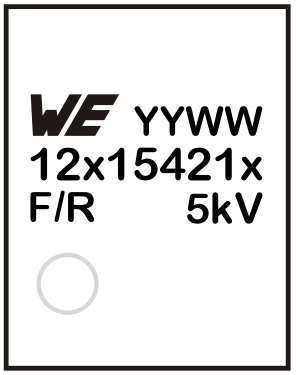


Figure 2: Marking.

Table 2: Pin description.

SYMBOL	NUMBER	TYPE	DESCRIPTION
VCC1	1	Power	Primary side supply pin.
INA/OUTA	2	I/O	Digital input/output A.
INB	3	I/O	Digital input B.
GND1	4	Power	Primary side ground connection.
GND2	5	Power	Secondary side ground connection.
OUTB	6	I/O	Digital output B.
INA/OUTA	7	I/O	Digital input/output A.
VCC2	8	Power	Secondary side supply pin.

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2 ORDERING INFORMATION

Table 3: Ordering information.

ORDER CODE	SPECIFICATIONS	PACKAGE	PACKAGING UNIT
18012015421H	2 forward, 0 reverse, default high	SOIC-8WB	13" Reel (1000 pieces)
18012015421L	2 forward, 0 reverse, default low		
18012115421H	1 forward, 1 reverse, default high		
18012115421L	1 forward, 1 reverse, default low		

3 SALES INFORMATION

SALES CONTACT
Würth Elektronik eiSos GmbH & Co. KG EMC and Inductive Solutions Max-Eyth-Str. 1 74638 Waldenburg Germany Tel. +49 (0) 7942 945 0 www.we-online.com/digitalisolators Technical support: powermodules@we-online.com

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4 ABSOLUTE MAXIMUM RATINGS

Caution:
Exceeding the listed absolute maximum ratings may affect the device negatively and may cause permanent damage.

Table 4: Absolute maximum ratings.

SYMBOL	PARAMETER	LIMIT		UNIT
		MIN[1]	MAX[1]	
VCC1, VCC2	Supply voltage pins	-0.5	7	V
INX, OUTX	Voltage at INX, OUTX, SEL pins	-0.5	V_{CCX} + 0.5[2]	V
I_{OUTX}	Channel output current	-20	20	mA
$T_{storage}$	Assembled, non-operating storage temperature	-65	150	°C
V_{ESD}	ESD voltage (HBM)[4]	-6	6	kV
V_{ESD}	ESD voltage (CDM)[4]	-2	2	kV

5 OPERATING CONDITIONS

Operating conditions are conditions under which the device is intended to be functional. All values are either referenced to GND1 or GND2.

MIN and MAX limits are valid for the recommended ambient temperature range of -40°C to 125°C.

Table 5: Operating conditions.

SYMBOL	PARAMETER	MIN[1]	TYP[3]	MAX[1]	UNIT
V_{CC1}, V_{CC2}	Supply voltage	2.375	—	5.5	V
V_{INX_H}	Logic input high threshold	2.0	—	—	V
V_{INX_L}	Logic input low threshold	—	—	0.8	V
I_{OH}	High-level channel output current V_{CCO} = 5V	-4	—	—	mA
	High-level channel output current V_{CCO} = 3.3V	-2	—	—	mA
	High-level channel output current V_{CCO} = 2.5V	-1	—	—	mA
I_{OL}	Low-level channel output current V_{CCO} = 5V	—	—	4	mA
	Low-level channel output current V_{CCO} = 3.3V	—	—	2	mA
	Low-level channel output current V_{CCO} = 2.5V	—	—	1	mA
DR	Data rate	0	—	150	Mbps
PW	Signal pulse width	5	—	—	ns
T_a	Ambient temperature range	-40	—	125	°C

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6 ELECTRICAL SPECIFICATIONS

Caution:
MIN and MAX limits are valid for the recommended ambient temperature range of -40°C to 125°C. Typical values represent statistically the utmost probable values at the following conditions: V_{CC} = 5V, 3.3V or 2.5V, T_A = 25°C, unless otherwise noted.

Table 6: Electrical specifications part 1.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN[1]	TYP[3]	MAX[1]	UNIT
Supply Characteristics						
V_{CCX_UVLO}	Supply undervoltage lockout falling threshold		1.88	2.10	2.325	V
	Undervoltage lockout rising threshold		1.95	2.24	2.375	V
	Undervoltage lockout hysteresis		70	140	250	mV
Channel Characteristics						
I_{IH}	High-level input leakage current	$V_{INX} = V_{CCI}$	—	—	20	µA
I_{IL}	Low-level input leakage current	V_{INX} = 0V	-20	—	—	µA
V_{OH}	High-level output voltage	I_{OH_5V} = -4mA or $I_{OH_3.3V}$ = -2mA or $I_{OH_2.5V}$ = -1mA	—	V_{CCX} - 0.2	—	V
V_{OL}	Low-level output voltage	I_{OL_5V} = 4mA or $I_{OL_3.3V}$ = 2mA or $I_{OL_2.5V}$ = 1mA	—	0.2	—	V
CMTI	Common-mode transient immunity	$V_{INX} = V_{CCI}$ or 0V, V_{CM} = 1200V	—	150	—	kV/µs
Timing Characteristics						
t_r	Output signal rise time	10% to 90% of V_{OUTX}	—	2.5	4.0	ns
t_f	Output signal fall time	90% to 10% of V_{OUTX}	—	2.5	4.0	ns
t_{PLH}, t_{PHL}	Propagation delay time	50% of V_{INX} to 50% of V_{OUTX}	5	12	15	ns
PWD	Pulse width distortion $\lvert t_{PLH} - t_{PHL} \rvert$		—	0.2	4.5	ns
$t_{SK(C-C)}$	Channel-to-channel output skew time		—	0.4	2.5	ns
$t_{SK(P-P)}$	Part-to-part output skew time		—	2.0	4.5	ns

Parameters indicated in electrical specifications part 1 are applicable across all part numbers with all input/output conditions unless otherwise specified.

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Table 7: Electrical specifications part 2.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN[1]	TYP[3]	MAX[1]	UNIT
18012015421x V_{CC1} = 5V and V_{CC2} = 5V						
I_{CC1}	Primary side external power supply input current[5]	V_{INX} = channel default	—	0.8	—	mA
		$V_{INX} \neq$ channel default	—	3.4	—	mA
		1Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	2.1	—	mA
		10Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	2.2	—	mA
		100Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	2.8	—	mA
I_{CC2}	Secondary side external power supply input current[5]	V_{INX} = channel default	—	1.3	—	mA
		$V_{INX} \neq$ channel default	—	1.4	—	mA
		1Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	1.5	—	mA
		10Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	2.7	—	mA
		100Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	14.2	—	mA
18012115421x V_{CC1} = 5V and V_{CC2} = 5V						
I_{CC1}	Primary side external power supply input current[5]	V_{INX} = channel default	—	1.4	—	mA
		$V_{INX} \neq$ channel default	—	2.8	—	mA
		1Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	2.2	—	mA
		10Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	3.1	—	mA
		100Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	11.1	—	mA
I_{CC2}	Secondary side external power supply input current[5]	V_{INX} = channel default	—	1.3	—	mA
		$V_{INX} \neq$ channel default	—	2.9	—	mA
		1Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	2.3	—	mA
		10Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	3.1	—	mA
		100Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	11.6	—	mA
18012015421x V_{CC1} = 3.3V and V_{CC2} = 3.3V						
I_{CC1}	Primary side external power supply input current[5]	V_{INX} = channel default	—	0.8	—	mA
		$V_{INX} \neq$ channel default	—	3.4	—	mA
		1Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	2.0	—	mA
		10Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	2.1	—	mA
		100Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	2.5	—	mA

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Table 8: Electrical specifications part 3.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN[1]	TYP[3]	MAX[1]	UNIT
I_{CC2}	Secondary side external power supply input current[5]	V_{INX} = channel default	—	1.2	—	mA
		$V_{INX} \neq$ channel default	—	1.3	—	mA
		1Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	1.4	—	mA
		10Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	2.1	—	mA
		100Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	9.6	—	mA
18012115421x V_{CC1} = 3.3V and V_{CC2} = 3.3V						
I_{CC1}	Primary side external power supply input current[5]	V_{INX} = channel default	—	1.4	—	mA
		$V_{INX} \neq$ channel default	—	2.7	—	mA
		1Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	2.1	—	mA
		10Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	2.7	—	mA
		100Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	8	—	mA
I_{CC2}	Secondary side external power supply input current[5]	V_{INX} = channel default	—	1.4	—	mA
		$V_{INX} \neq$ channel default	—	2.9	—	mA
		1Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	2.2	—	mA
		10Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	2.7	—	mA
		100Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	8	—	mA
18012015421x V_{CC1} = 2.5V and V_{CC2} = 2.5V						
I_{CC1}	Primary side external power supply input current[5]	V_{INX} = channel default	—	0.8	—	mA
		$V_{INX} \neq$ channel default	—	3.4	—	mA
		1Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	2.0	—	mA
		10Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	2.1	—	mA
		100Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	2.3	—	mA
I_{CC2}	Secondary side external power supply input current[5]	V_{INX} = channel default	—	1.2	—	mA
		$V_{INX} \neq$ channel default	—	1.3	—	mA
		1Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	1.3	—	mA
		10Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	1.9	—	mA
		100Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	7.5	—	mA

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Table 9: Electrical specifications part 4.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN[1]	TYP[3]	MAX[1]	UNIT
18012115421x V_{CC1} = 2.5V and V_{CC2} = 2.5V						
I_{CC1}	Primary side external power supply input current[5]	V_{INX} = channel default	—	1.3	—	mA
		$V_{INX} \neq$ channel default	—	2.7	—	mA
		1Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	2.1	—	mA
		10Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	2.5	—	mA
		100Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	6.4	—	mA
I_{CC2}	Secondary side external power supply input current[5]	V_{INX} = channel default	—	1.4	—	mA
		$V_{INX} \neq$ channel default	—	2.8	—	mA
		1Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	2.2	—	mA
		10Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	2.5	—	mA
		100Mbps, C_L = 15pF, 50% duty cycle square wave input signal	—	6.4	—	mA

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7 ISOLATION SPECIFICATIONS

Table 10: Isolation specification table.

SYMBOL	PARAMETER	TEST CONDITIONS	VALUE	UNIT
CLR	External clearance	Shortest distance through air between terminals	8	mm
CPG	External creepage	Shortest distance across package surface between terminals	8	mm
DTI	Distance through the insulation	Minimum internal clearance	28	µm
C_{IO}	Barrier capacitance, input to output	V_{IO} = 0.4 x sin (2πft), f = 1MHz	1	pF
R_{IO}	Isolation resistance	V_{IO} = 500V, T_A = 125°C	>10^{12}	Ω
		V_{IO} = 500V, 100°C≤T_A ≤ 125°C	>10^{11}	Ω
		V_{IO} = 500V at T_A = 150°C	>10^{9}	Ω
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	IEC 60664-1 Material group		I	
	IEC 60664-1 overvoltage category	Rated mains voltage ≤150 V_{RMS}	I-IV	
		Rated mains voltage ≤300 V_{RMS}	I-IV	
		Rated mains voltage ≤600 V_{RMS}	I-IV	
		Rated mains voltage ≤1000 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17):2021-10				
V_{IORM}	Max. repetitive peak isolation voltage	AC voltage (bipolar)	1414	V_{PK}
V_{IOWM}	Max. working isolation voltage	AC voltage; Time-dependent dielectric breakdown (TDDB) test	1000	V_{RMS}
		DC voltage	1414	V_{DC}
V_{IOTM}	Max. transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1s (100% production)	7070	V_{PK}
V_{IOSM}	Max. surge isolation voltage	Test method per IEC 60065, 1.2/50 µs waveform, V_{TEST} = 1.6 x V_{IOSM} (qualification)	7070	V_{PK}
q_{pd}	Apparent charge	Method a, after input/output safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.2 x V_{IORM}, t_m = 10s	≤5	pC
		Method a, after environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.6 x V_{IORM}, t_m = 10s	≤5	pC
		Method b, at routine test (100% production) and preconditioning (type test), V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1s; $V_{pd(m)}$ = 1.875 x V_{IORM}, t_m = 1s	≤5	pC
	Pollution degree		2	
UL1577				
$V_{ISO(max)}$	Max. withstanding isolation voltage	V_{TEST} = V_{ISO}, t = 60s (qualification), V_{TEST} = 1.2 x V_{ISO}, t = 1s (100% production)	5000	V_{RMS}

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8 APPROVALS

Table 11: Pin description.

STANDARD	DESCRIPTION
UL 1577	UL File No: E535458
DIN EN IEC 60747-17 (VDE 0884-17):2021-10	VDE certification number: 40058069

9 RoHS, REACH

Table 12: RoHS, REACH.

RoHS directive	COMPLIANT RoHS&REACH WÜRTH ELEKTRONIK	Directive 2011/65/EU of the European Parliament and the Council of June 8th, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.
REACH directive		Directive 1907/2006/EU of the European Parliament and the Council of June 1st, 2007 regarding the Registration, Evaluation, Authorization and Restriction of Chemicals (REACH).

10 PACKAGE SPECIFICATIONS

Table 13: Package specifications.

ITEM	PARAMETER	TYP[(3)]	UNIT
Lead finish	Matte Sn	—	—
Weight	—	0.31	g

11 NOTES

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

(2) This value must never exceed 7V.

(3) Typical numbers are valid at 25°C ambient temperature and represent statistically the utmost probability assuming the Gaussian distribution.

(4) The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD-22-114. The charged device model test method is per JESD22-C101.

(5) Supply current measurements are made with no additional load connected to the primary and secondary external power supplies. The indicated values only describe the current required to supply the internal circuitry and external capacitive loads on the channel outputs based on the signal described in the test conditions.

(6) 100% final production tested value. The qualified isolation voltage value is $5kV_{RMS}$. For detailed isolation characteristics see the isolation specification table (Isolation specification table).

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12 TYPICAL PERFORMANCE CURVES

If not otherwise specified, the following conditions apply: T_A = 25°C.

12.1 DC Performance Curves

12.1.1 Quiescent Current vs. Ambient Temperature

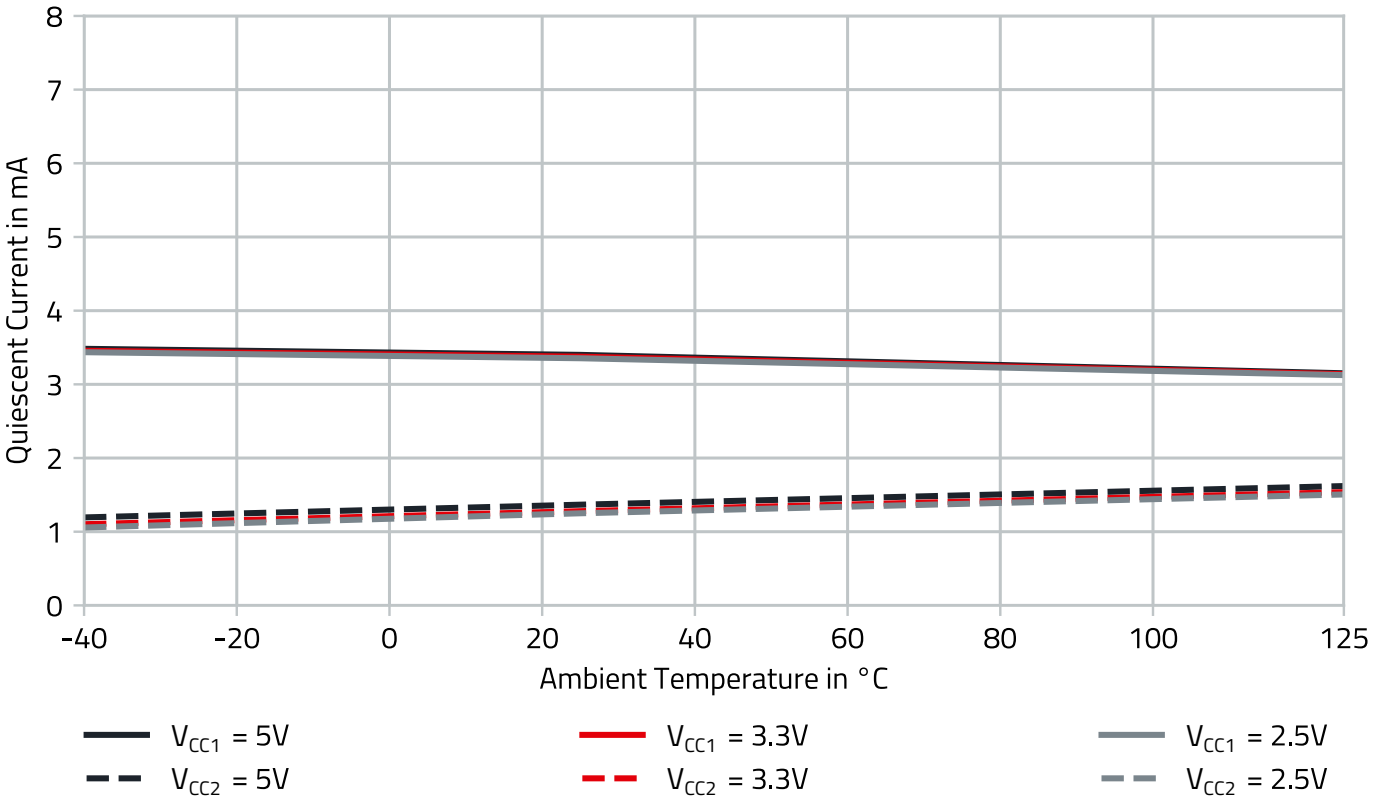


Figure 3: 18012015421H quiescent current, all channel inputs set to logic high.

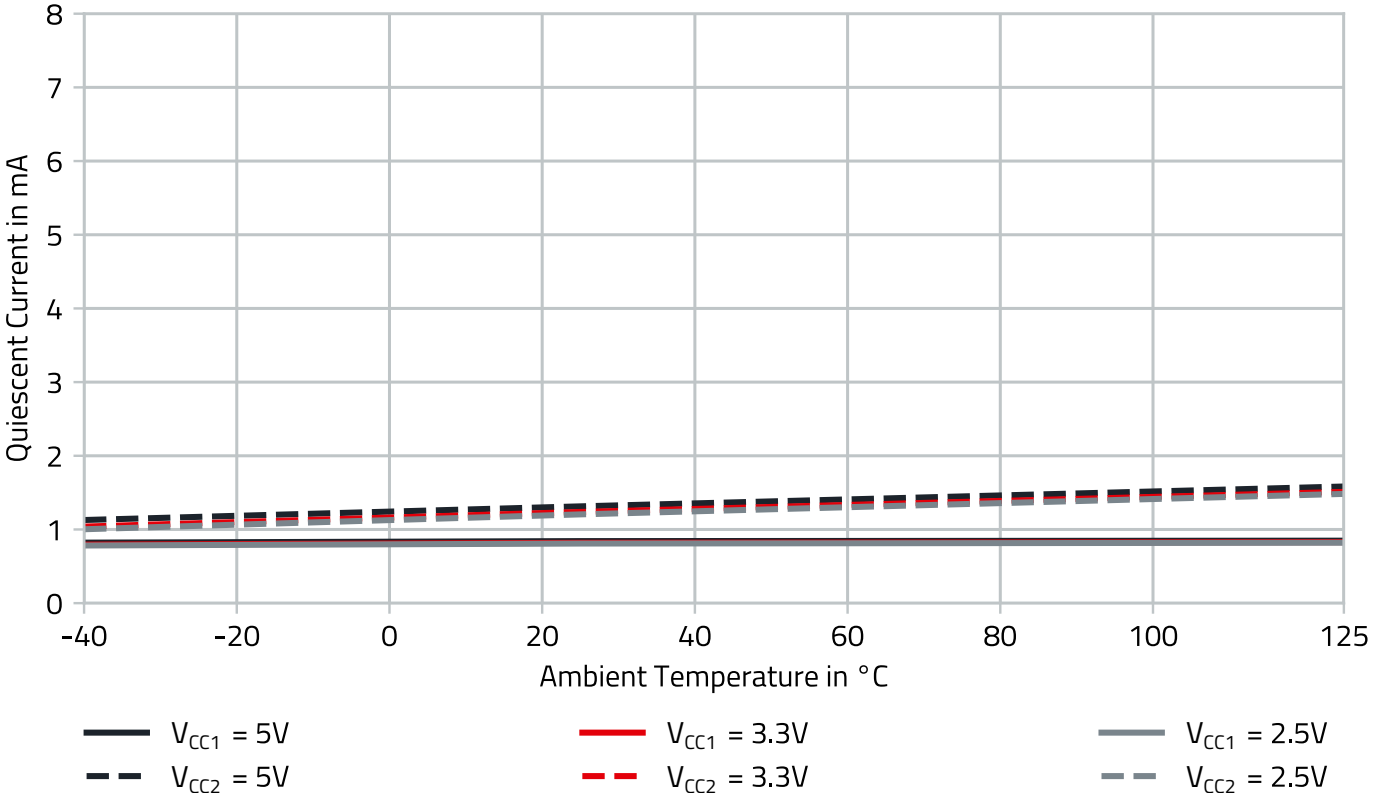


Figure 4: 18012015421H quiescent current, all channel inputs set to logic low.

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12.1.2 Propagation Delay vs. Ambient Temperature

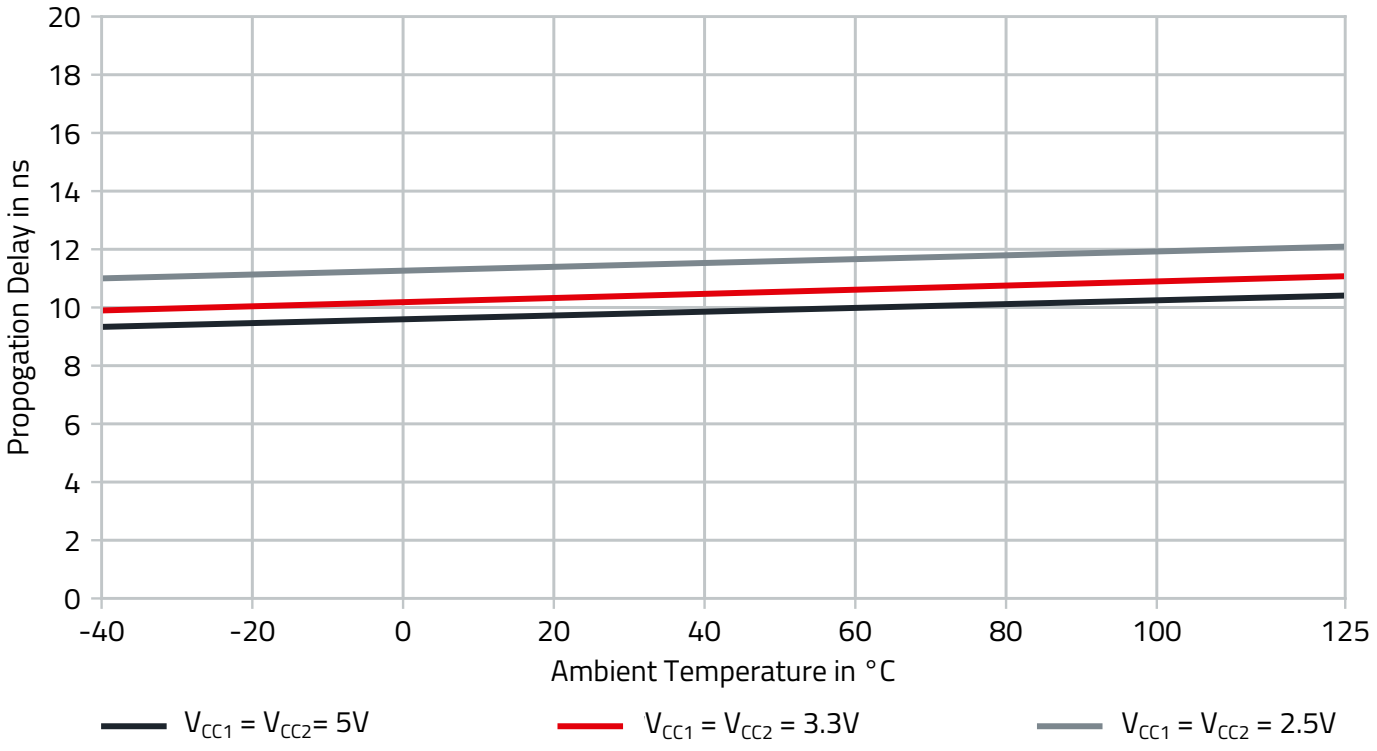


Figure 5: 18012x15421x propagation delay, all channels with low to high transition, C_{LOAD} = 15pF.

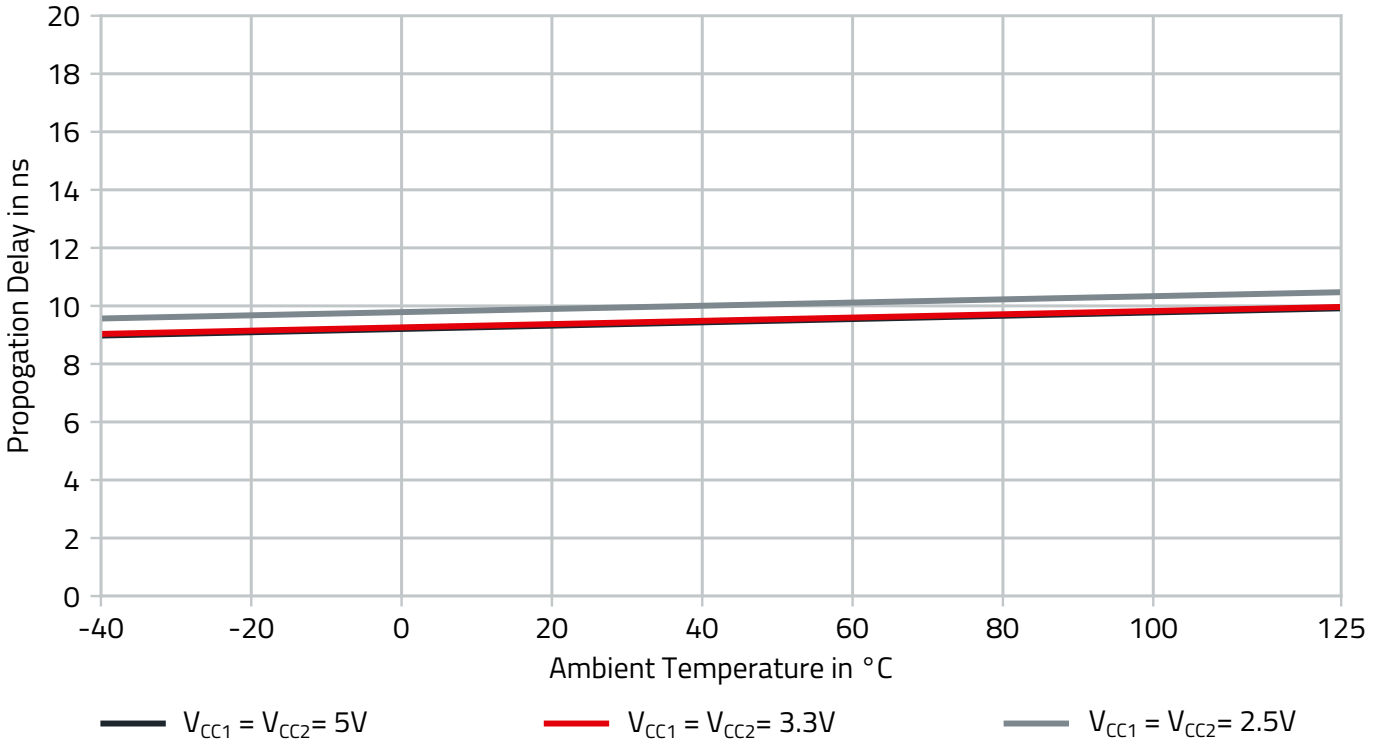


Figure 6: 18012x15421x propagation delay, all channels with high to low transition, C_{LOAD} = 15pF.

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12.1.3 Supply Current vs. Ambient Temperature

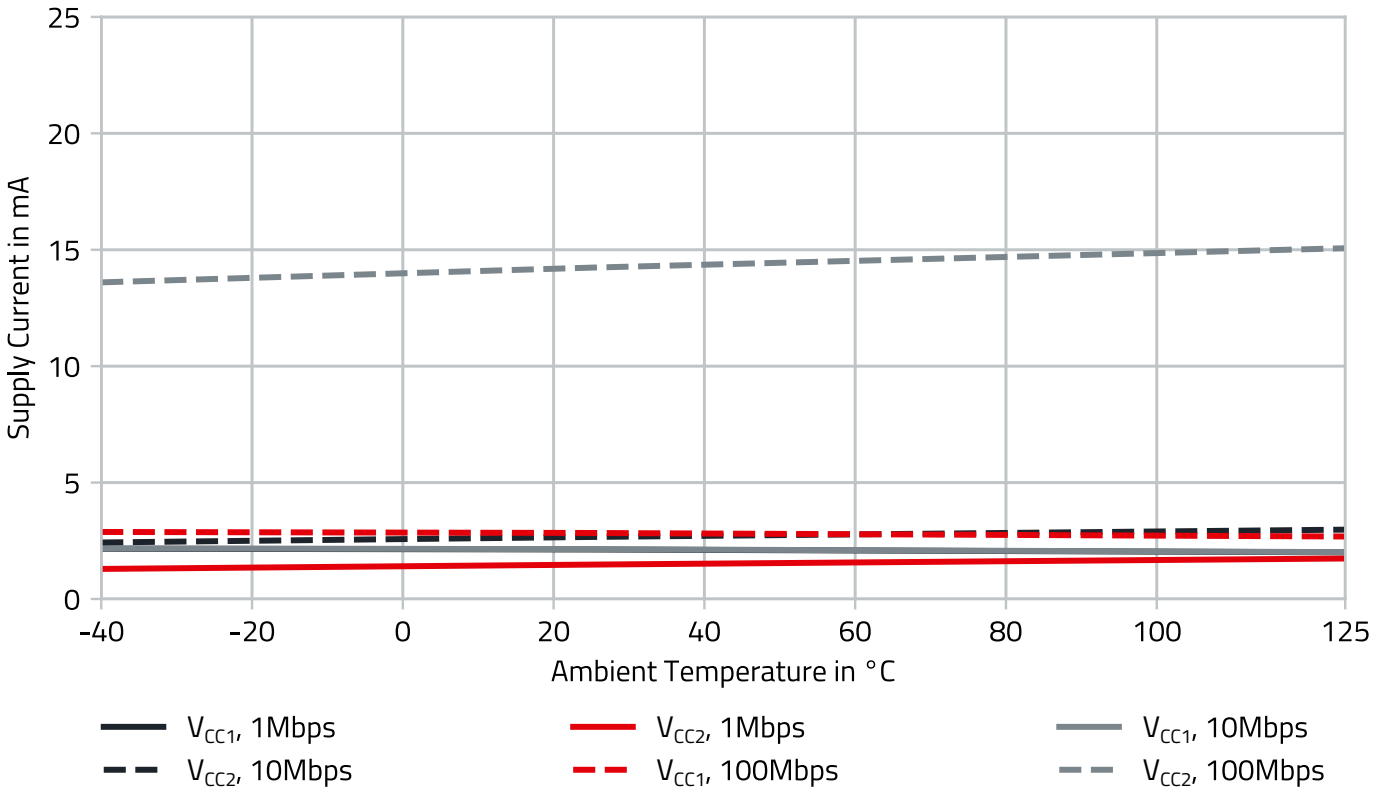


Figure 7: 18012015421x supply current V_{CC1} = V_{CC2} = 5V.

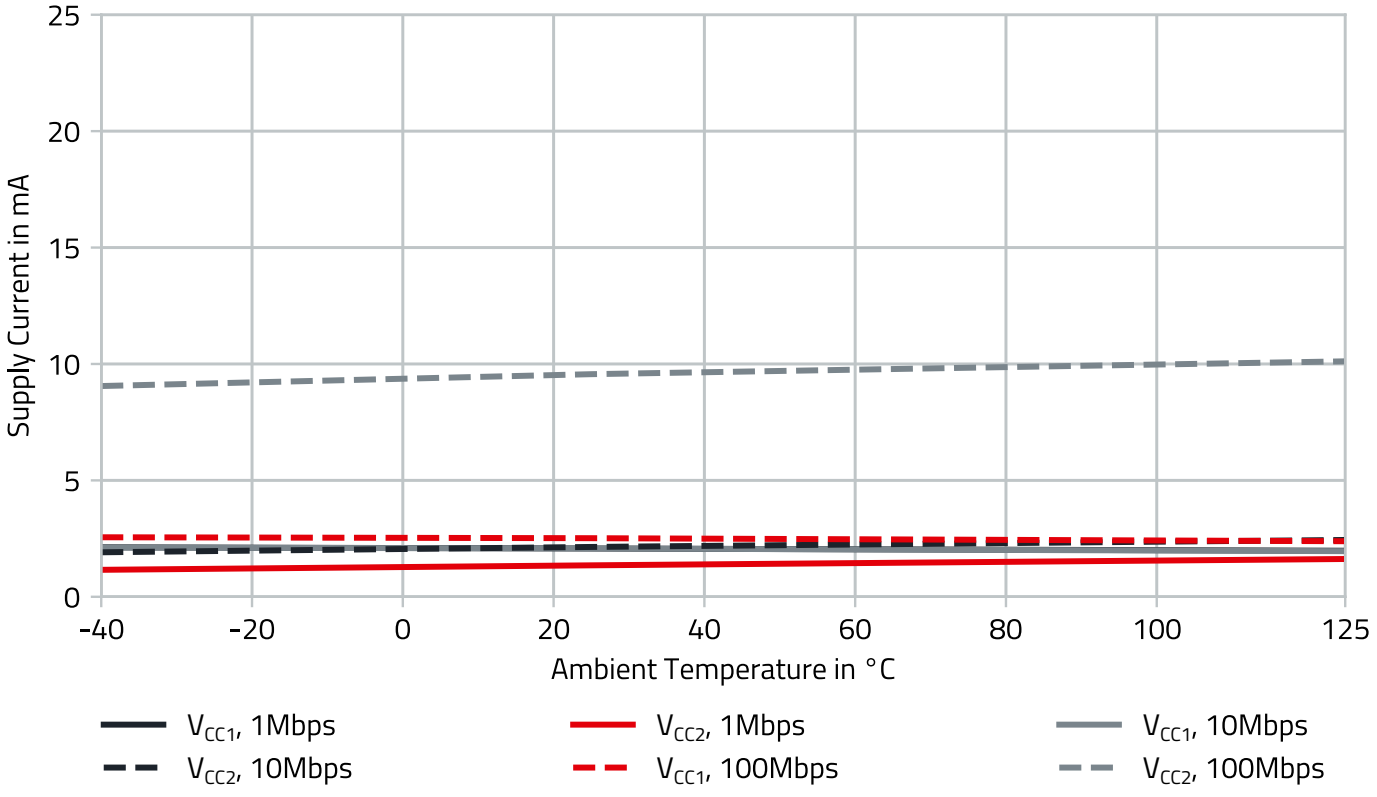


Figure 8: 18012015421x supply current V_{CC1} = V_{CC2} = 3.3V.

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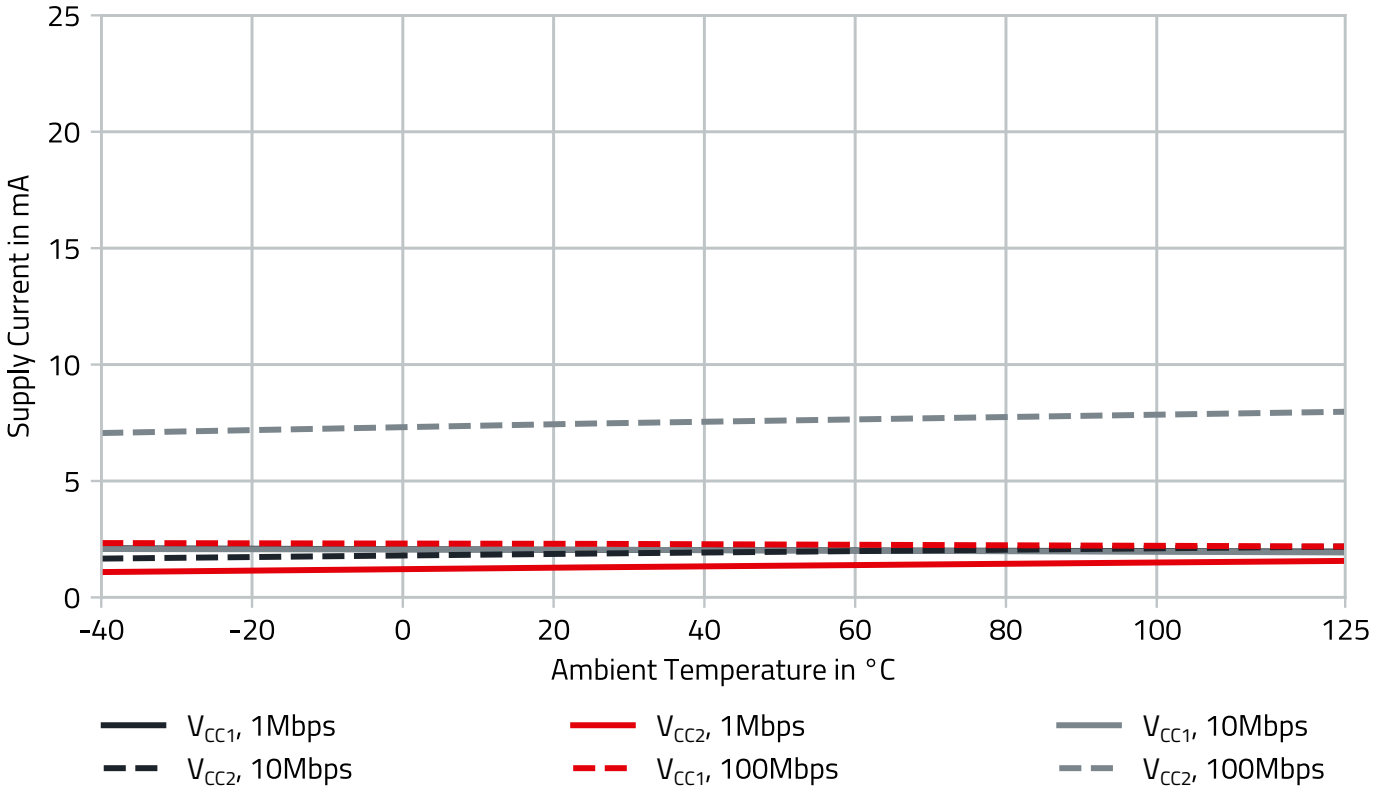


Figure 9: 18012015421x supply current V_{CC1} = V_{CC2} = 2.5V.

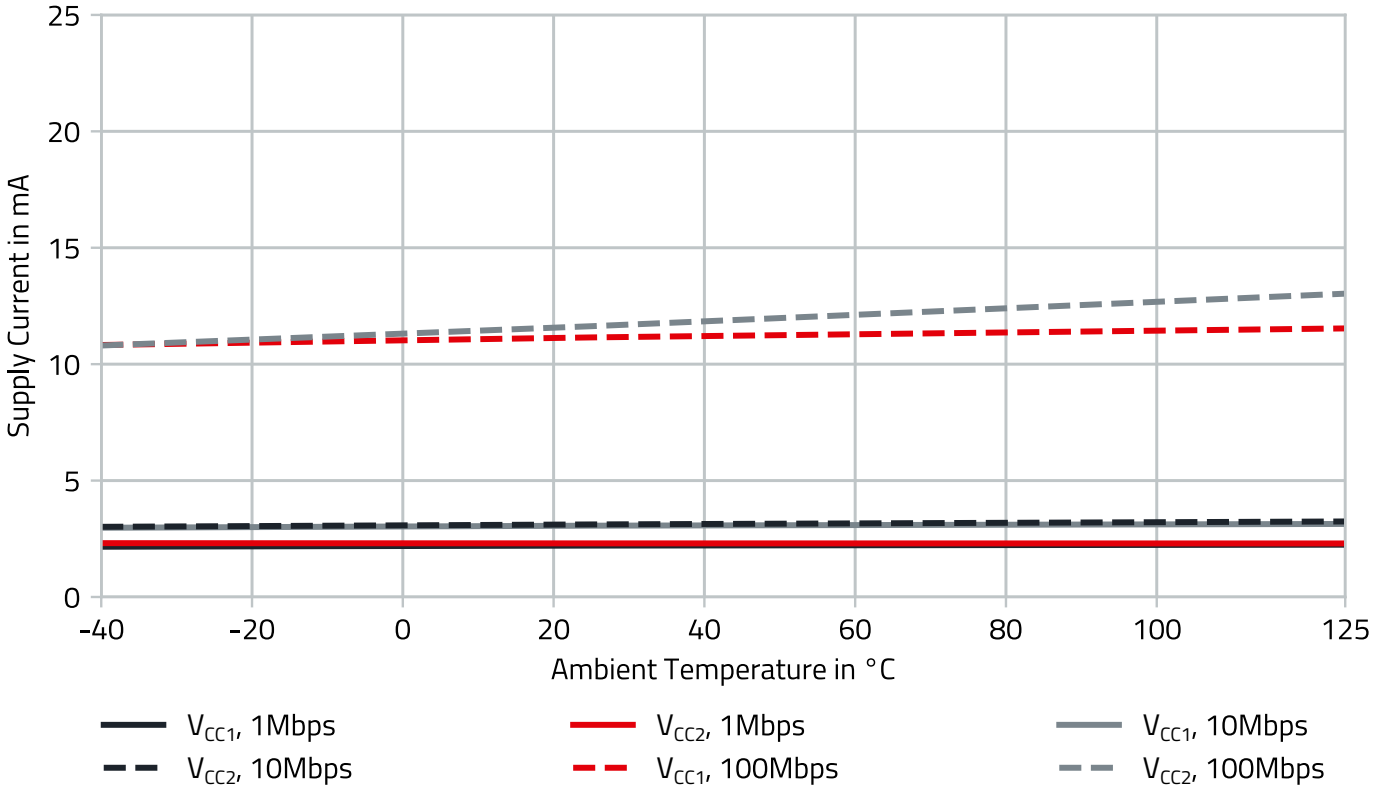


Figure 10: 18012115421x supply current V_{CC1} = V_{CC2} = 5V.

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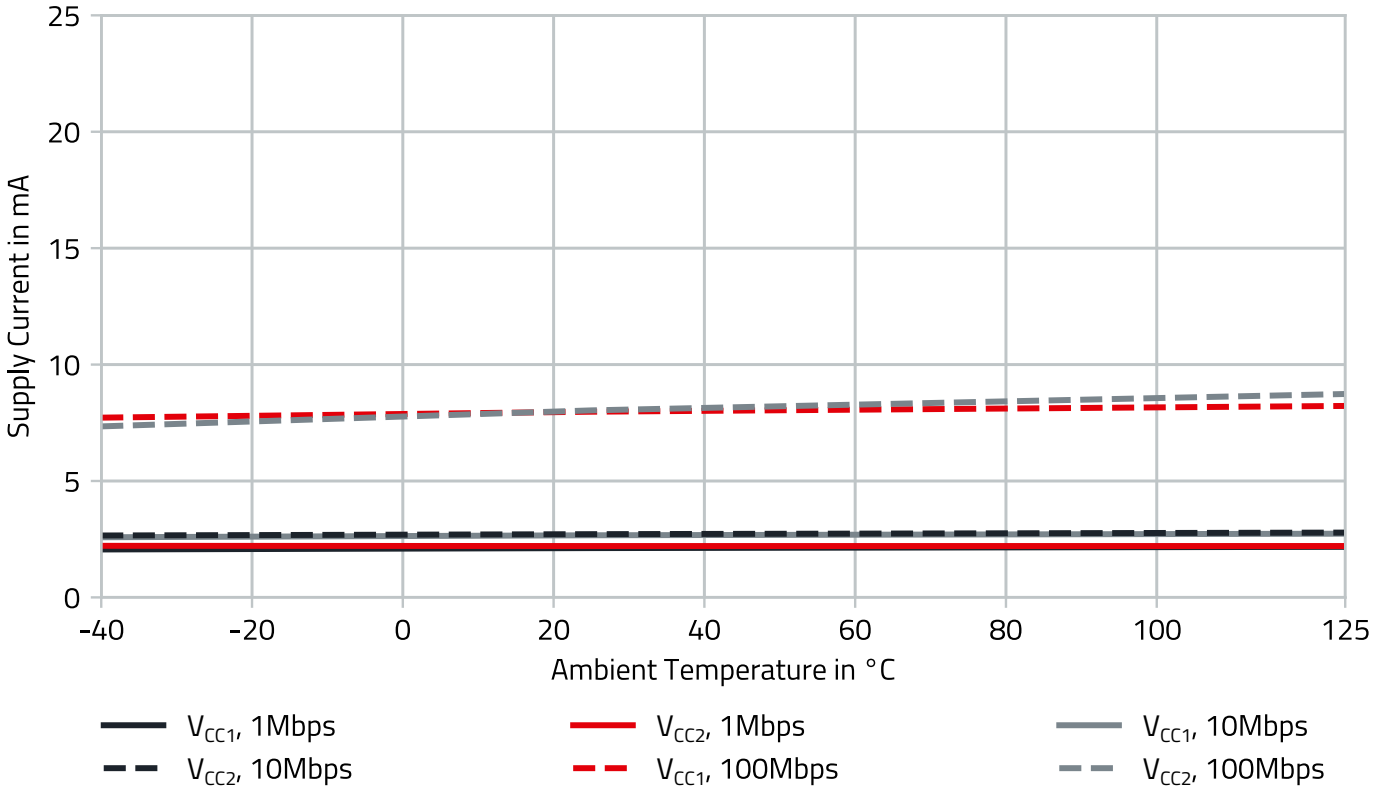


Figure 11: 18012115421x supply current V_{CC1} = V_{CC2} = 3.3V.

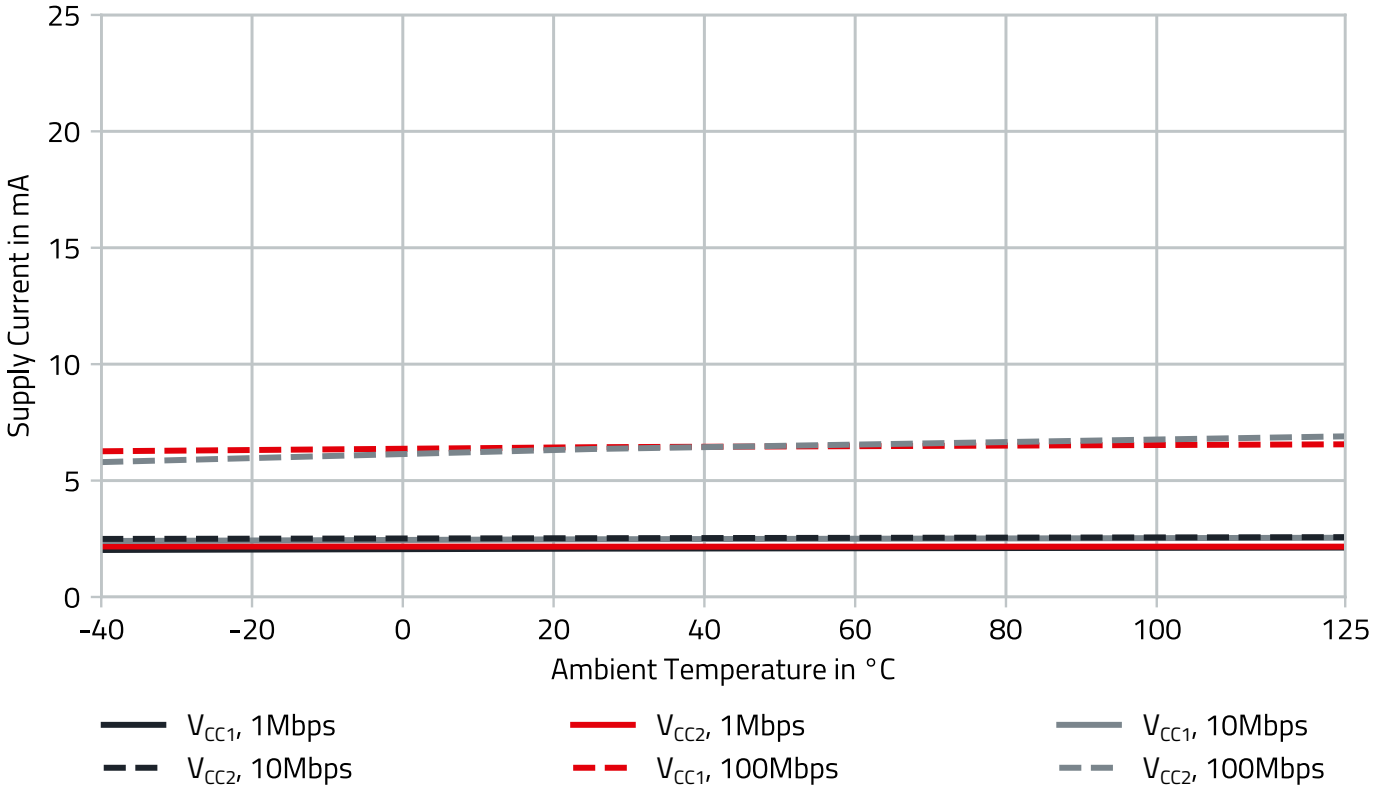


Figure 12: 18012115421x supply current V_{CC1} = V_{CC2} = 2.5V.

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12.1.4 Supply Current vs. Data Rate

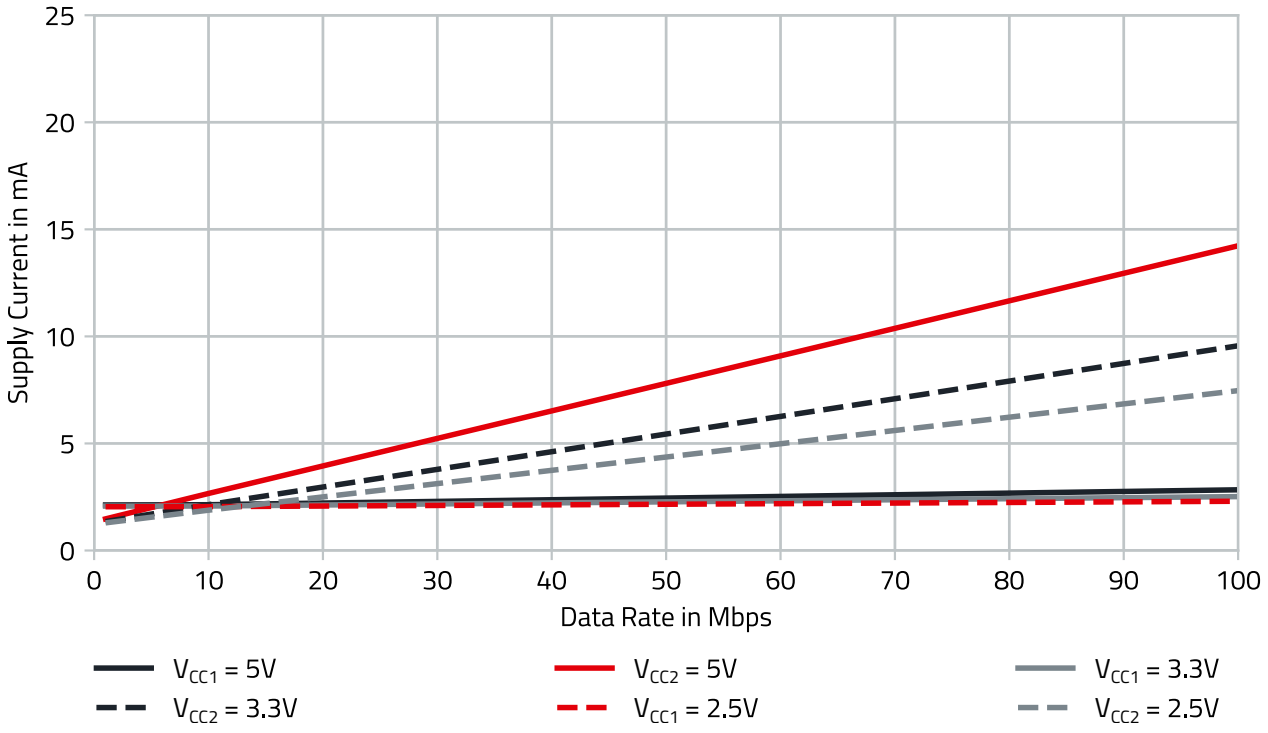


Figure 13: 18012015421x supply current vs. data rate.

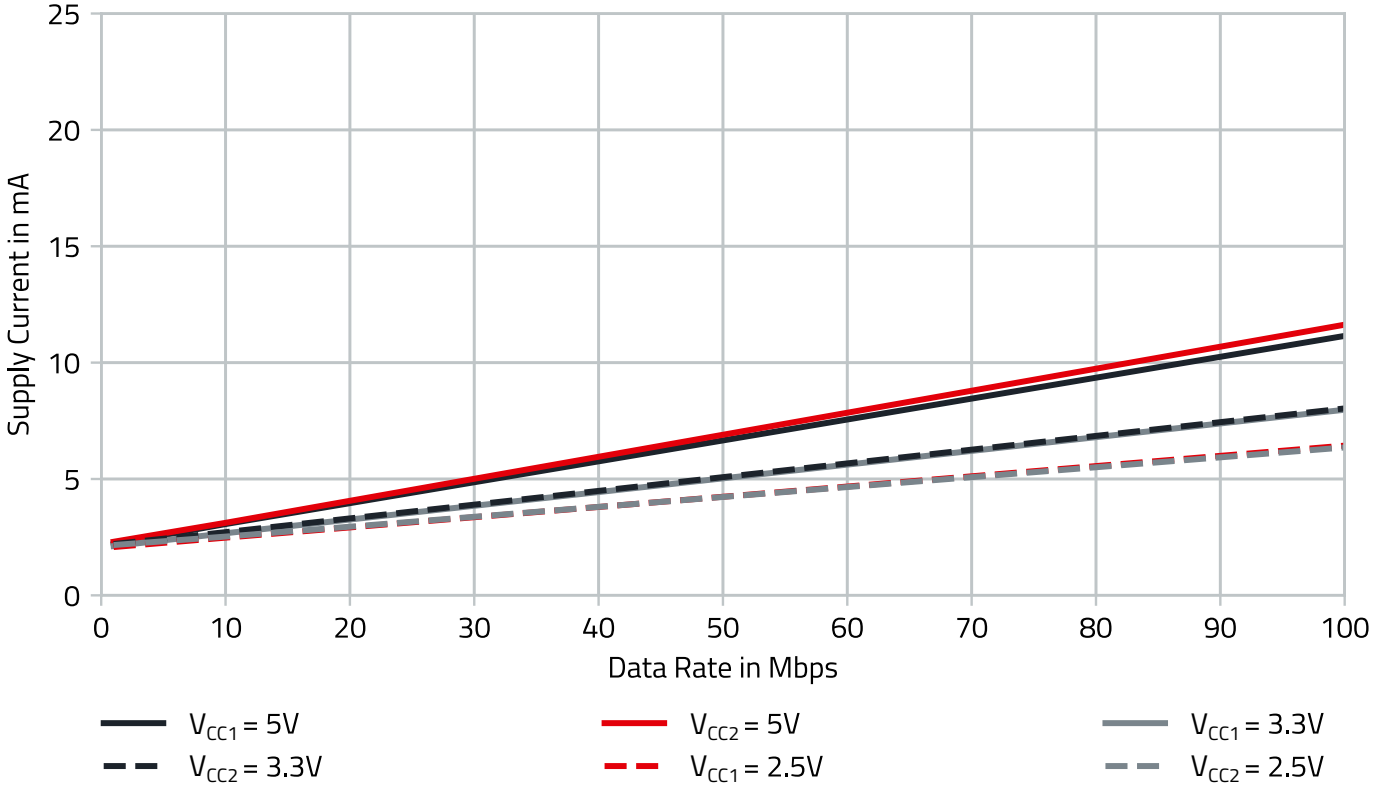


Figure 14: 18012115421x supply current vs. data rate.

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12.1.5 High and Low Voltage Levels vs. Output Current

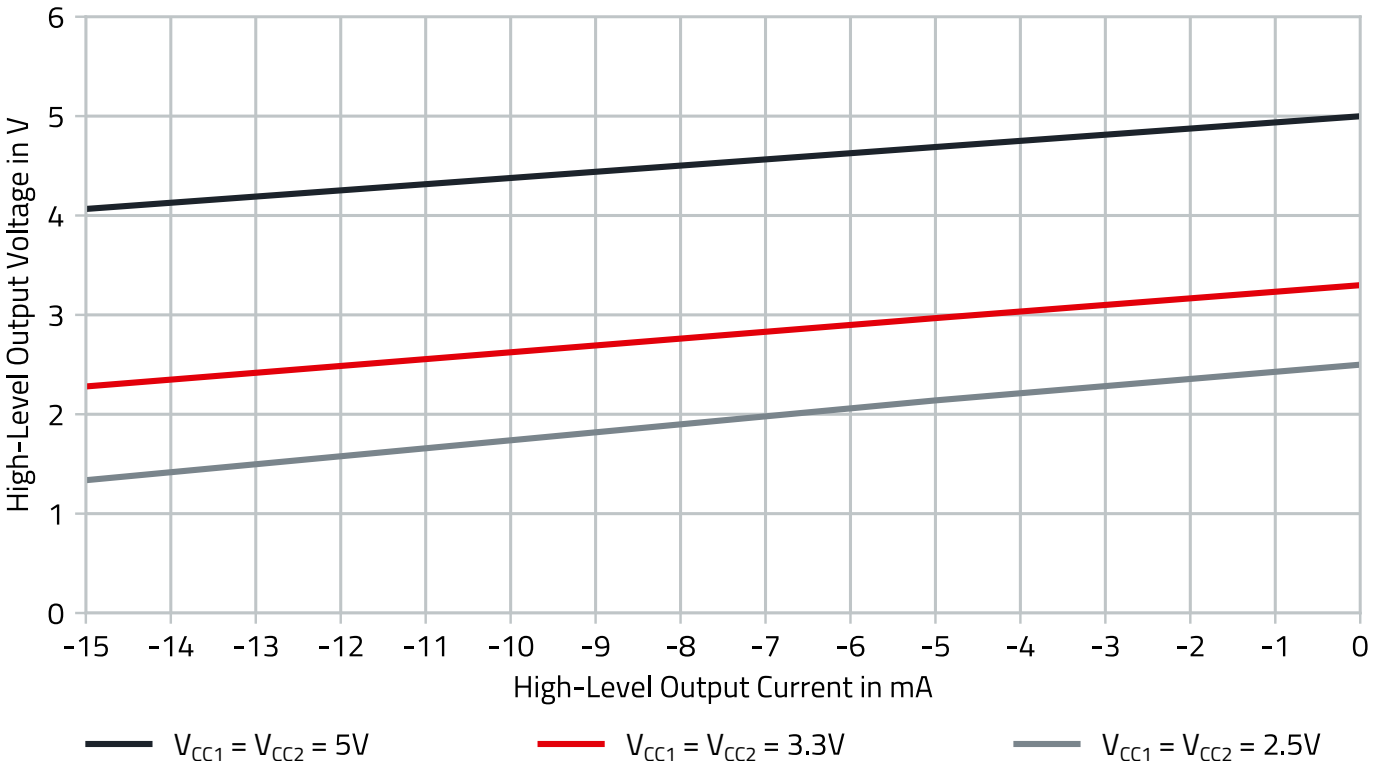


Figure 15: 18012x15421x high-level output voltage vs. high-level output current.

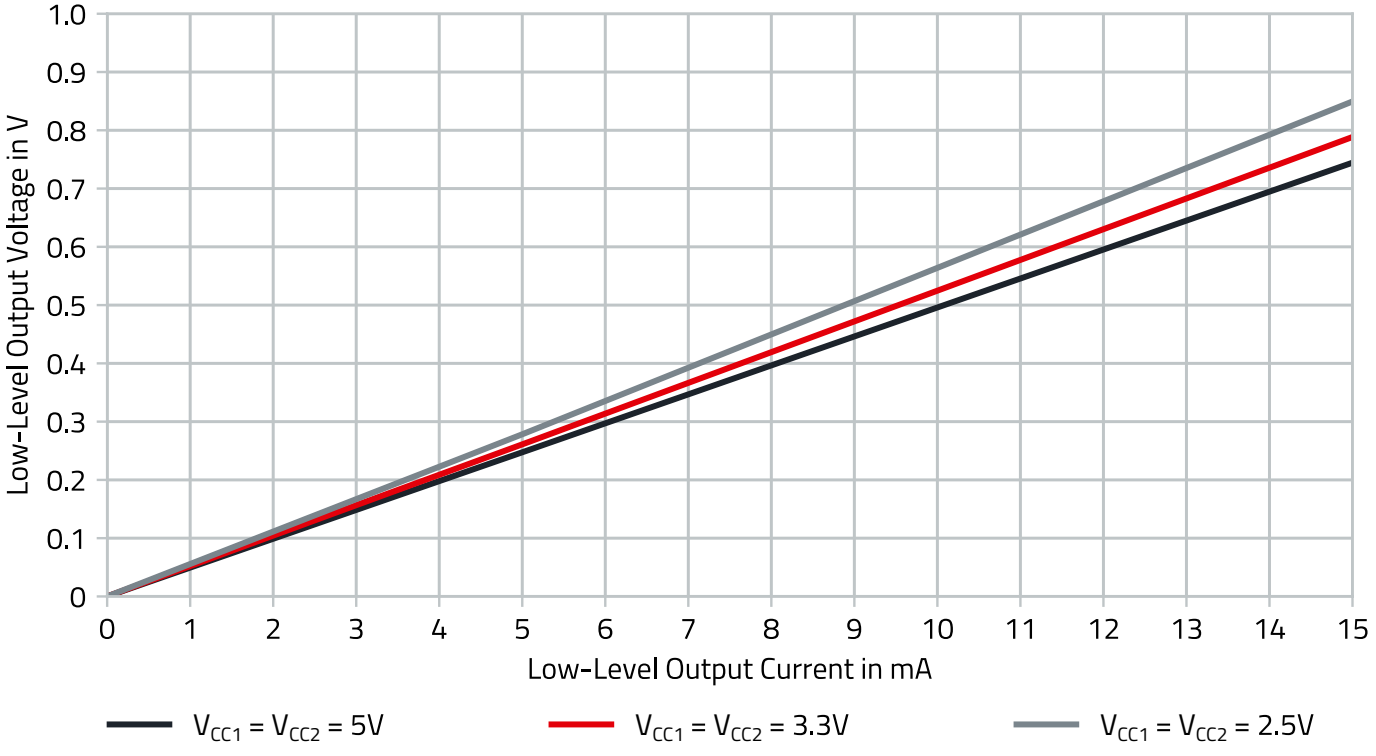


Figure 16: 18012x15421x low-level output voltage vs. low-level output current.

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12.1.6 Safety Limiting Curves

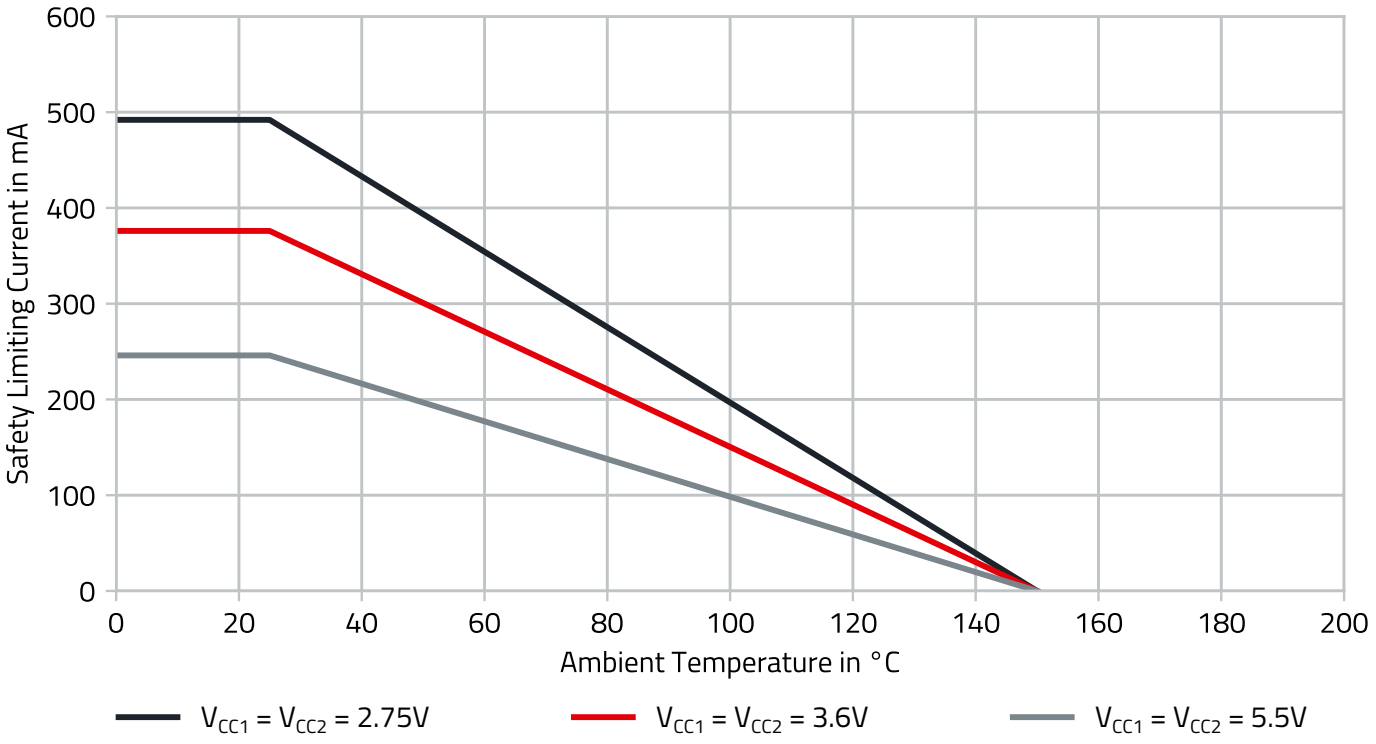


Figure 17: 18012x15421x safety limiting current.

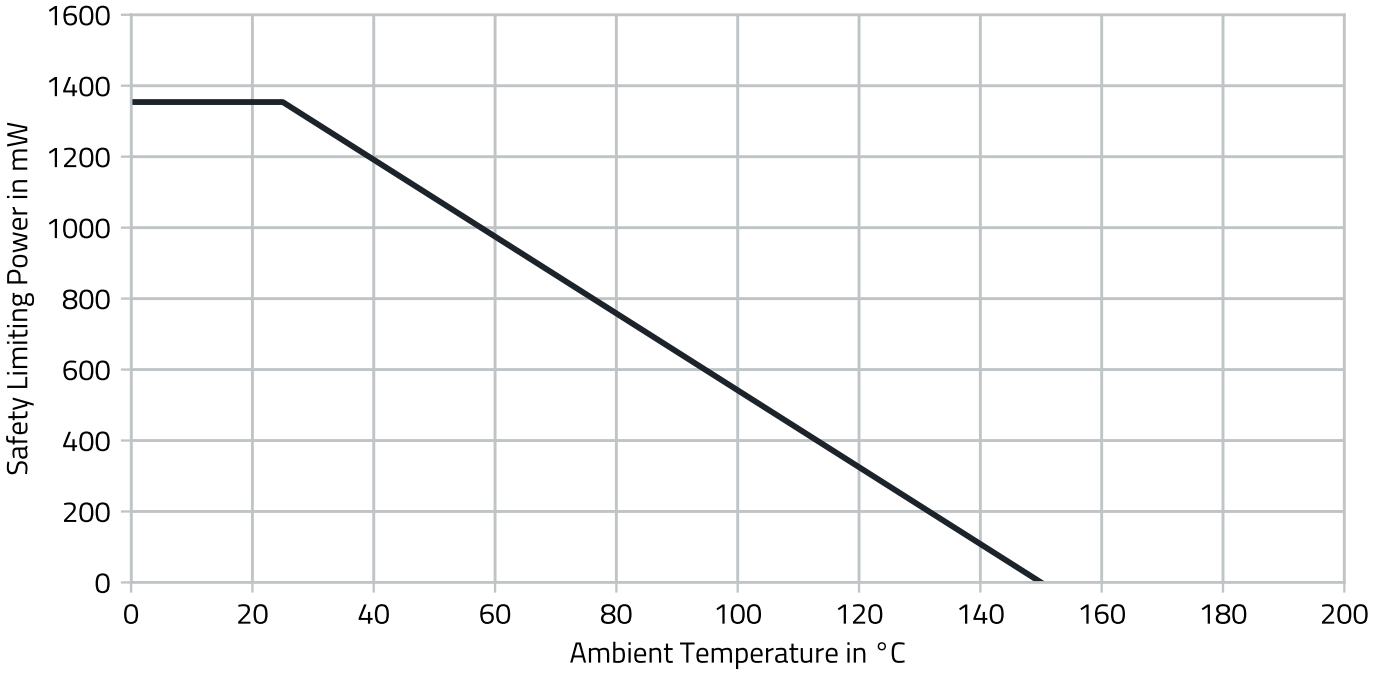


Figure 18: 18012x15421x safety limiting power.

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13 TRUTH TABLE

Table 14: I/O truth table.

V_{CC1}	V_{CC2}	Input V_{INX}	Output V_{OUTX}	Operation
≥2.375V	≥2.375V	H	H	Normal operation: The channel output follows the logic state of its input.
		L	L	
		Open	Default	Default output: When input V_{INX} is open, the corresponding channel output goes to its default logic state.
≤2V	≥2.375V	X	Default	Default output: When the primary supply is unpowered, a channel output assumes the logic state based on its default configuration. Parts with H have a default of high while parts with L have a default of low.
X	≤2V	X	Undetermined	If V_{CC2} is unpowered, the channel output is undetermined.

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14 I/O DESCRIPTION

Table 15: I/O schematics.

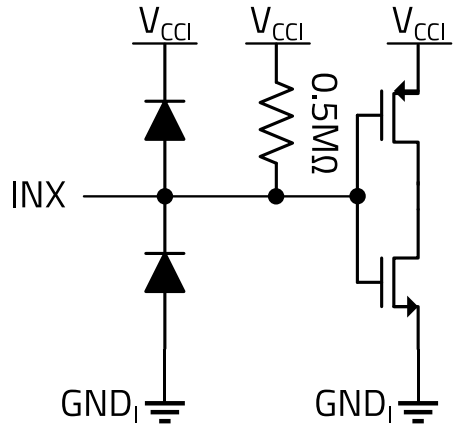


Figure 19: Default high channel input internal structure.

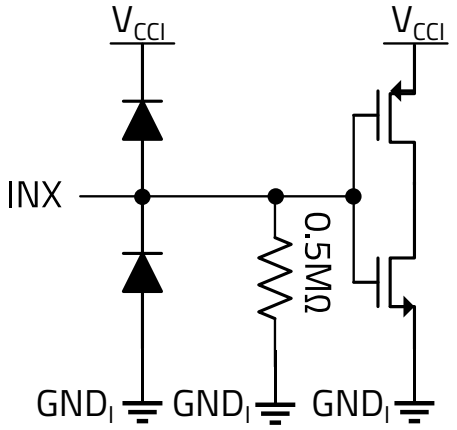


Figure 20: Default low channel input internal structure.

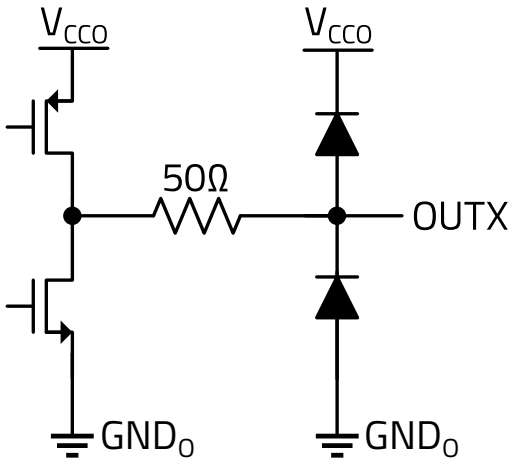


Figure 21: Channel output internal structure.

NOTE:
For forward channels $V_{CCI} = V_{CC1}$, $V_{CCO} = V_{CC2}$, GND_I = GND1 and GND_O = GND2.
For reverse channels $V_{CCI} = V_{CC2}$, $V_{CCO} = V_{CC1}$, GND_I = GND2 and GND_O = GND1.

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15 TEST SCHEMATICS

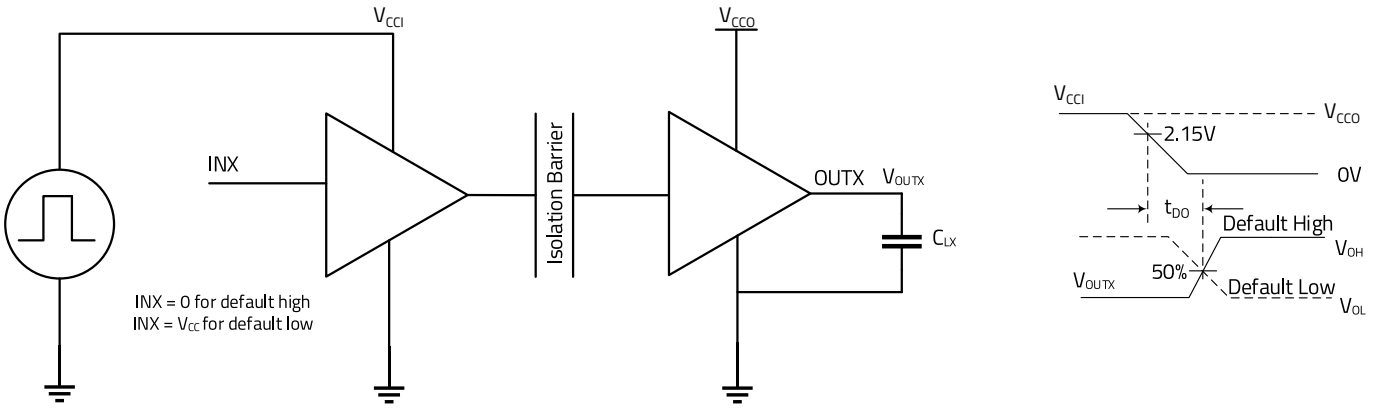


Figure 22: Default output delay test schematic.

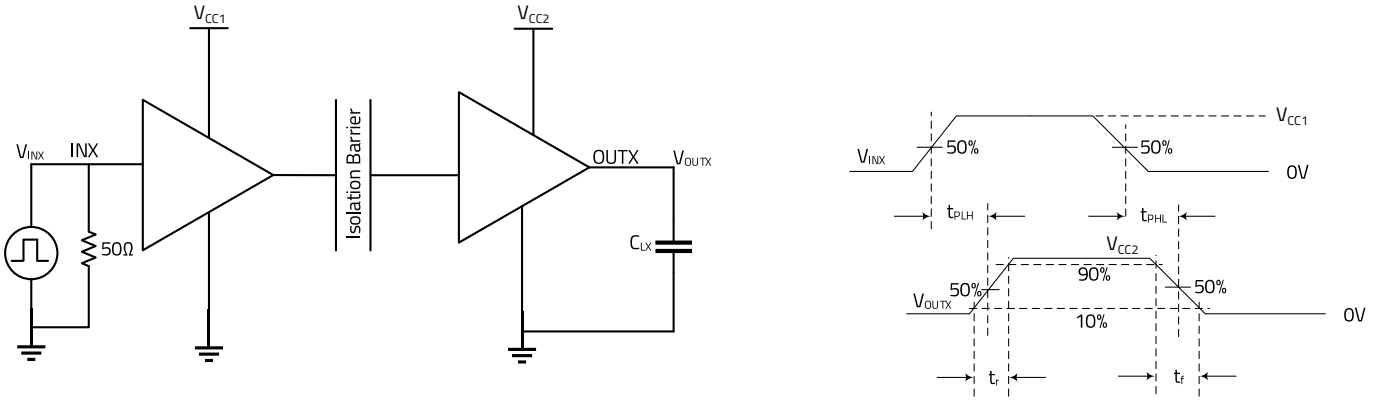


Figure 23: Propagation delay test schematic.

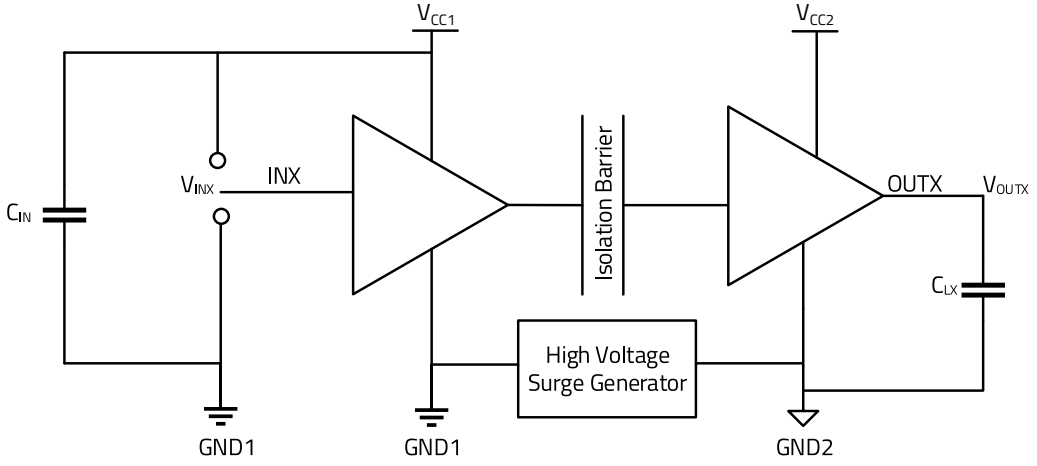


Figure 24: CMTI test schematic.
Note: C_{LX} = 15 pF and includes instrumentation and fixture capacitance within ±20%.

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16 BLOCK DIAGRAM

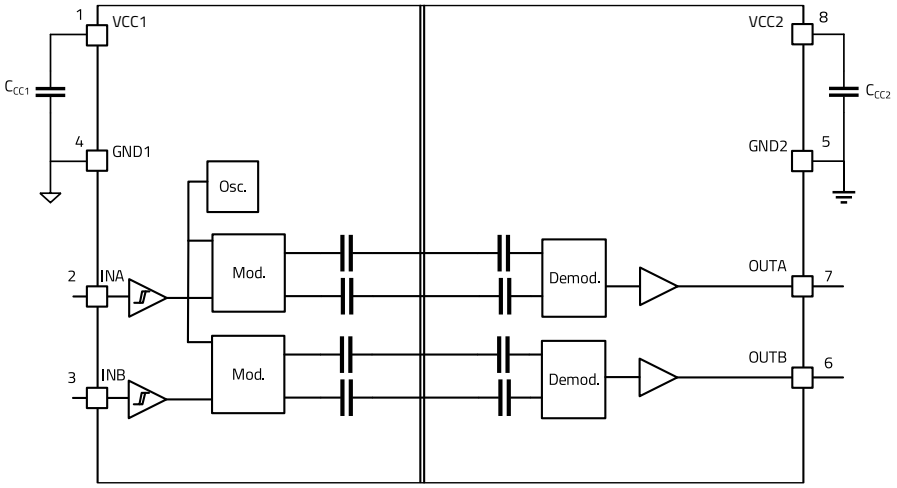


Figure 25: 18012015421x block diagram.

17 CIRCUIT DESCRIPTION

The WPME-CDIS digital isolator consists of two capacitive isolated digital channels that must be powered by two isolated supply voltages. The device is typically operated using 5V, 3.3V or 2.5V and the primary and secondary sides can be independently powered with any voltage within the operating conditions. The WPME-CDIS integrates the isolation capacitors in addition to the modulators and demodulators needed to construct the two isolated channels.

The isolation channels are realized using on/off key (OOK) modulation to transmit high or low speed signals through silicon dioxide isolation barriers. The on-chip oscillator is used to modulate the schmitt-triggered input signal. The modulator generates a differential signal that is transmitted through the capacitive isolation lines. The demodulator is located on the output side of the signal channel and used to amplify, filter and reconstruct the input signal with minimum propagation delay and distortion. Finally, the output of the demodulator is given to the output through buffer to improve the driving strength.

18 PROTECTION FEATURES

18.1 Input/Output Undervoltage Lockout (UVLO)

The device incorporates input and output undervoltage lockout (UVLO) to protect from unexpected behavior at input voltages below the recommended values. The thresholds of the UVLO are indicated in the ELECTRICAL SPECIFICATIONS.

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19 TYPICAL APPLICATION

The figure below depicts a typical application for a digital isolator used in a CAN bus configuration between a controller and transceiver.

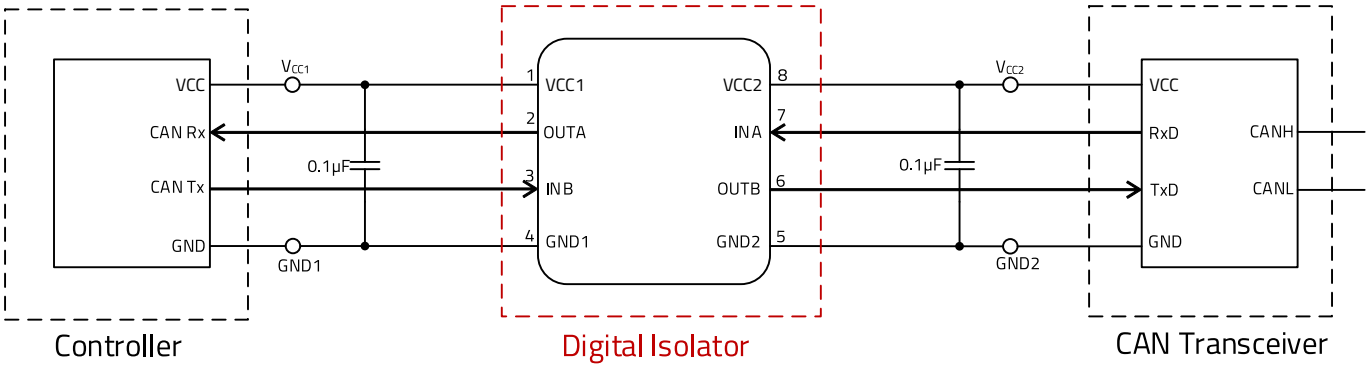


Figure 26: Typical application: CAN bus.

The 18012115421H and 18012115421L are shown in the above diagram in a conventional CAN implementation. The channel configuration allows for appropriate isolation and communication between the controller and transceiver.

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20 HANDLING RECOMMENDATIONS

1. The digital isolator is classified as MSL3 (JEDEC Moisture Sensitivity Level 3) and requires special handling due to moisture sensitivity (JEDEC J-STD033D).
2. The parts are delivered in a sealed bag (Moisture Barrier Bag = MBB) and should be processed within one year.
3. When opening the moisture barrier bag, check the Humidity Indicator Card (HIC) for the color status. Bake parts prior to soldering in case indicator color has changed according to the notes on the card.
4. Parts must be processed after 168 hour (7 days) of floor life. Once this time has been exceeded, bake parts prior to soldering per JEDEC J-STD033D recommendation.
5. Maximum number of soldering cycles is two.
6. For minimum risk, solder the device in the last solder cycle of the PCB production.
7. The component lead material is copper (Cu) and the lead finish is Matte Tin (Matte Sn).
8. For solder paste use a standard SAC Alloy such as SAC 305, type 3 or higher.
9. The profile below is valid for convection reflow only.
10. Other soldering methods (e.g. vapor phase) are not verified and have to be validated by the customer at their own risk.

20.1 Soldering Profile

Table 16: Reflow solder profile.

Profile Feature	Symbol	Value
Preheat temperature minimum	T_{s_min}	150 °C
Preheat temperature maximum	T_{s_max}	200 °C
Preheat time from T_{s_min} to T_{s_max}	t_s	60-120 seconds
Liquidous temperature	T_L	217 °C
Time maintained above T_L	t_L	60-90 seconds
Classification temperature	T_C	260 °C
Peak package body temperature	T_P	$T_P \leq T_C$
Time within T_C - 5 °C and T_C	t_P	$t_P \leq 30$ seconds
Ramp-up Rate (T_L to T_p)		3 °C/second maximum
Ramp-down rate (T_p to T_L)		6 °C/second maximum
Time 25 °C to peak temperature		8 minutes maximum

Please refer to JEDEC J-STD020 for further information pertaining to reflow soldering of electronic components.

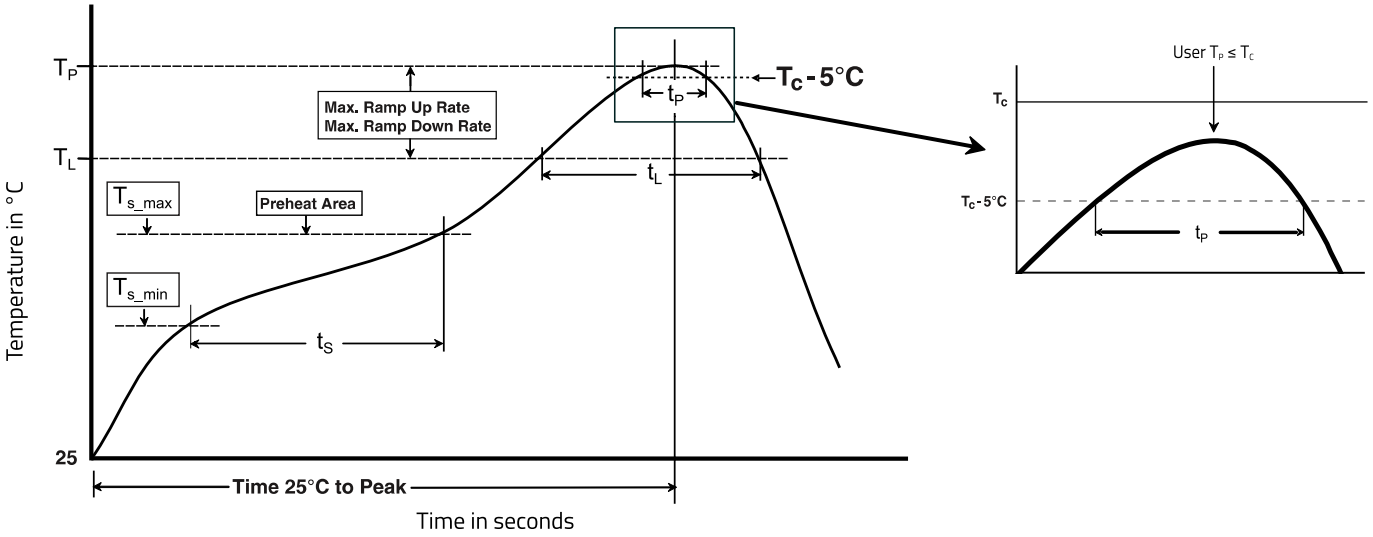


Figure 27: Soldering profile.

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21 PHYSICAL DIMENSIONS

Dimensions do not include mold flash, gate burrs, or protrusions.

21.1 Component

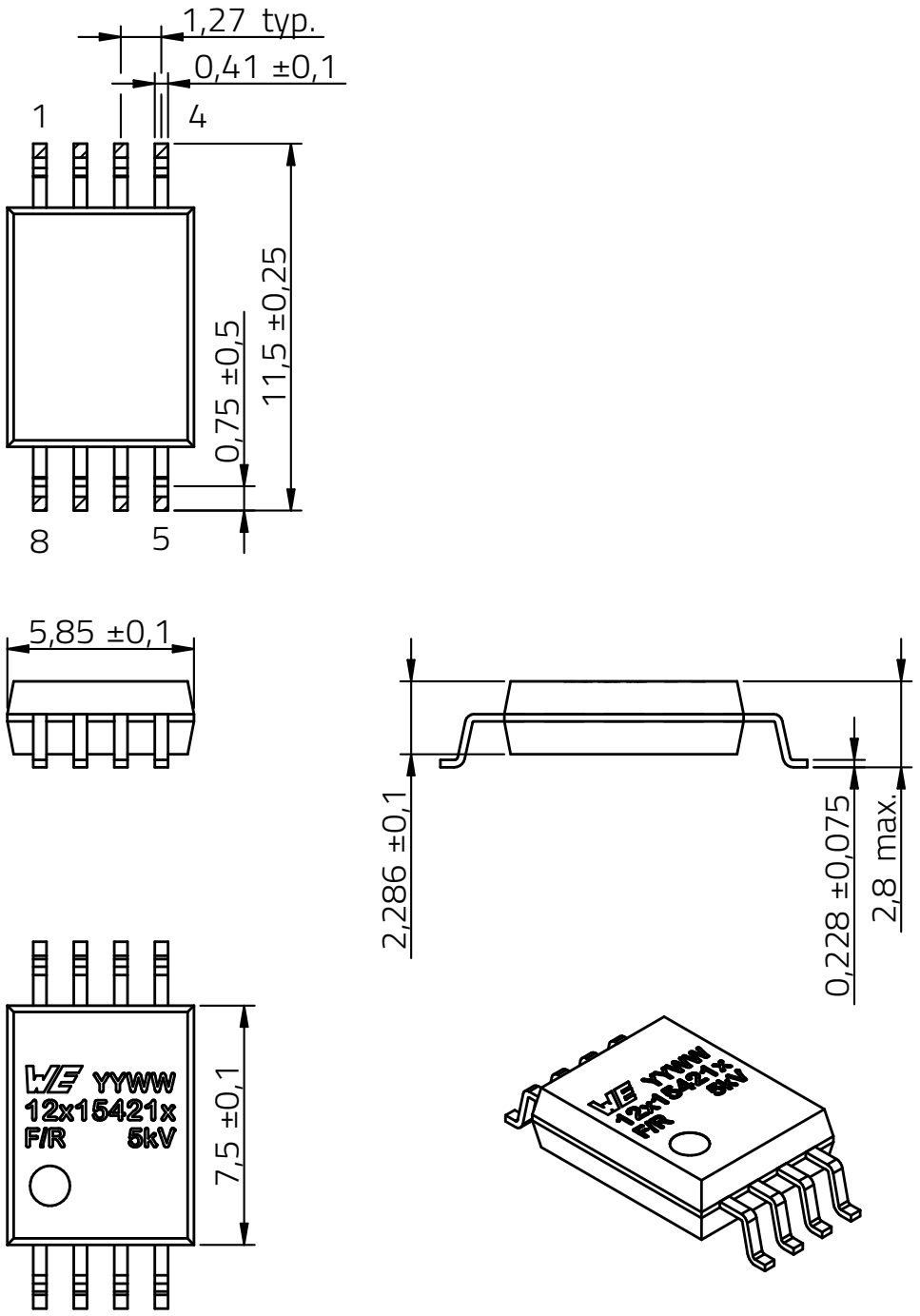


Figure 28: Component dimensions.

All dimensions in mm
Tolerance: xx.x =±0.5mm ; xx.xx = ±0.25mm unless otherwise noted
Dimensions do not include mold flash, gate burrs, or protrusions.

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21.2 Recommended Landpattern

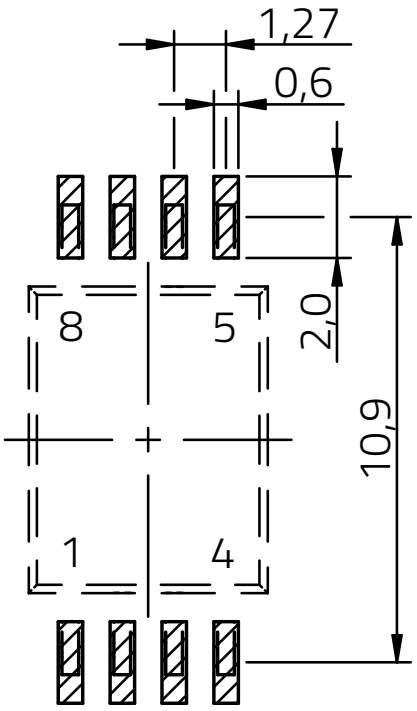


Figure 29: Recommended landpattern dimensions.
All dimensions in mm.

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21.3 Packaging

Reel in mm

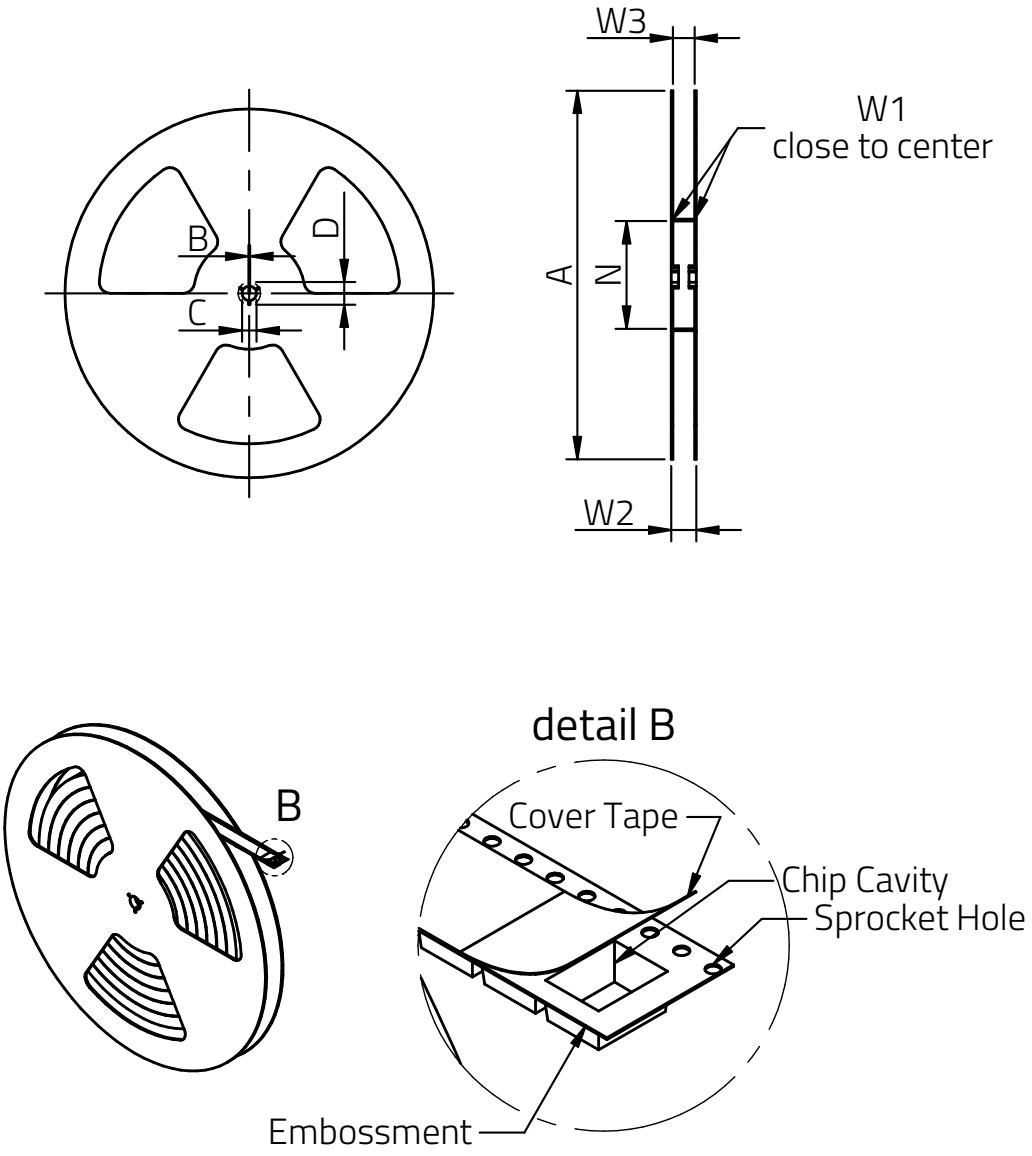


Figure 30: Reel dimensions.

Table 17: Reel dimensions.

A	B	C	D	N	W1	W1	W3	W3
typ.	±0.20	±0.20	±0.40	±0.50	min.	max.	min.	max.
330.00	2.30	13.00	21.00	100	16.10	16.70	15.40	19.40

Reel material is polystyrene.
All dimensions in mm.

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Tape in mm

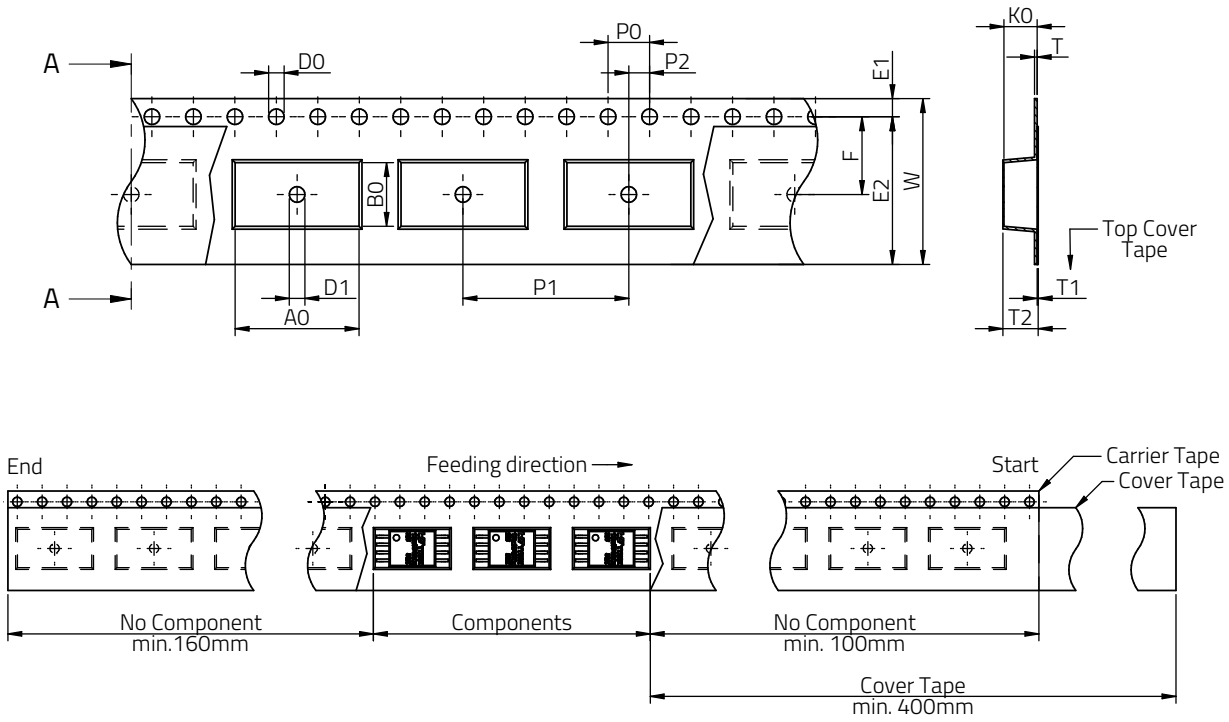


Figure 31: Tape dimensions.

Table 18: Tape dimensions part 1.

A0	B0	D0	D1	E1	F	P0	P1	P2	W
±0.10	±0.10	min.	min.	±0.10	±0.10	±0.10	±0.10	±0.10	max.
11.95	6.15	1.50	1.50	1.75	7.50	4.00	16.00	2.00	16.30

Table 19: Tape dimensions part 2.

K0	T	T1	T2	W
±0.10	±0.05	±0.005	±0.15	max.
3.20	0.35	0.05	3.60	16.30

Tape material is polystyrene.
All dimensions in mm.

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22 DOCUMENT HISTORY

Table 20: Document history.

Revision	Date	Description	Comment
1.0	April 2024	Initial release of data sheet	
1.1	June 2024		Updated VDE status from pending to certified and added VDE certification number
2.0	October 2026	PCN	As a datasheet information amendment, Würth Elektronik eiSos has specified the V_{OH} and V_{OL} in terms of channel output load current for each supply voltage and the V_{OH} typical value has referenced to V_{CCX} instead of V_{INX} in electrical specifications table. For process improvement purposes, Würth Elektronik eiSos has changed the bond wire material. There will be no change in form, fit, function, quality or reliability of the product.

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25 CAUTIONS AND WARNINGS

The following conditions apply to all goods within the product series of digital isolators of Würth Elektronik eiSos GmbH & Co. KG:

General:

- All recommendations according to the general technical specifications of the data-sheet have to be complied with.
- The usage and operation of the product within ambient conditions which probably alloy or harm the component surface has to be avoided.
- The responsibility for the applicability of customer specific products and use in a particular customer design is always within the authority of the customer. All technical specifications for standard products do also apply for customer specific products
- Residual washing varnish agent that is used during the production to clean the application might change the characteristics of the body, pins or termination. The washing varnish agent could have a negative effect on the long term function of the product. Direct mechanical impact to the product shall be prevented as the material of the body, pins or termination could flake or in the worst case it could break. As these devices are sensitive to electrostatic discharge customer shall follow proper IC Handling Procedures.
- Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Würth Elektronik eiSos GmbH & Co. KG components in its applications, notwithstanding any applications-related information or support that may be provided by Würth Elektronik eiSos GmbH & Co. KG.
- Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences lessen the likelihood of failures that might cause harm and take appropriate remedial actions
- Customer will fully indemnify Würth Elektronik eiSos and its representatives against any damages arising out of the use of any Würth Elektronik eiSos GmbH & Co. KG components in safety-critical applications

Product specific:

Follow all instructions mentioned in the datasheet, especially:

- The solder profile has to comply with the technical reflow or wave soldering specification, otherwise this will void the warranty.
- All products are supposed to be used before the end of the period of 12 months based on the product date-code.
- Violation of the technical product specifications such as exceeding the absolute maximum ratings will void the warranty.
- It is also recommended to return the body to the original moisture proof bag and reseal the moisture proof bag again.
- ESD prevention methods need to be followed for manual handling and processing by machinery.

Disclaimer:

This electronic component has been designed and developed for usage in general electronic equipment only. This product is not authorized for use in equipment where a higher safety standard and reliability standard is especially required or where a failure of the product is reasonably expected to cause severe personal injury or death, unless the parties have executed an agreement specifically governing such use. Moreover Würth Elektronik eiSos GmbH & Co. KG products are neither designed nor intended for use in areas such as military, aerospace, aviation, nuclear control, submarine, transportation (automotive control, train control, ship control), transportation signal, disaster prevention, medical, public information network etc. Würth Elektronik eiSos GmbH & Co. KG must be informed about the intent of such usage before the design-in stage. In addition, sufficient reliability evaluation checks for safety must be performed on every electronic component which is used in electrical circuits that require high safety and reliability functions or performance. These cautions and warnings comply with the state of the scientific and technical knowledge and are believed to be accurate and reliable. However, no responsibility is assumed for inaccuracies or incompleteness.

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26 IMPORTANT NOTES

General Customer Responsibility

Some goods within the product range of Würth Elektronik eiSos GmbH & Co. KG contain statements regarding general suitability for certain application areas. These statements about suitability are based on our knowledge and experience of typical requirements concerning the areas, serve as general guidance and cannot be estimated as binding statements about the suitability for a customer application. The responsibility for the applicability and use in a particular customer design is always solely within the authority of the customer. Due to this fact it is up to the customer to evaluate, where appropriate to investigate and decide whether the device with the specific product characteristics described in the product specification is valid and suitable for the respective customer application or not. Accordingly, the customer is cautioned to verify that the datasheet is current before placing orders.

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It has to be clearly pointed out that the possibility of a malfunction of electronic components or failure before the end of the usual lifetime cannot be completely eliminated in the current state of the art, even if the products are operated within the range of the specifications. In certain customer applications requiring a very high level of safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health it must be ensured by most advanced technological aid of suitable design of the customer application that no injury or damage is caused to third parties in the event of malfunction or failure of an electronic component.

Best Care and Attention

Any product-specific notes, warnings and cautions must be strictly observed. Any disregard will result in the loss of warranty.

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Due to constant product improvement product specifications may change from time to time. As a standard reporting procedure of the Product Change Notification (PCN) according to the JEDEC-Standard we inform about minor and major changes. In case of further queries regarding the PCN, the field sales engineer or the internal sales person in charge should be contacted. The basic responsibility of the customer as per Section 1 and 2 remains unaffected.

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Due to technical progress and economical evaluation we also reserve the right to discontinue production and delivery of products. As a standard reporting procedure of the Product Termination Notification (PTN) according to the JEDEC Standard we will inform at an early stage about inevitable product discontinuance. According to this we cannot guarantee that all products within our product range will always be available. Therefore it needs to be verified with the field sales engineer or the internal sales person in charge about the current product availability expectancy before or when the product for application design-in disposal is considered. The approach named above does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.

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