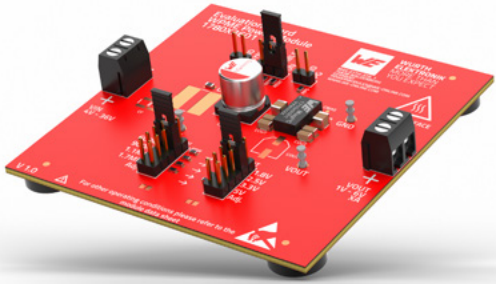
WÜRTH ELEKTRONIK
MORE THAN YOU EXPECT



QUICK START GUIDE

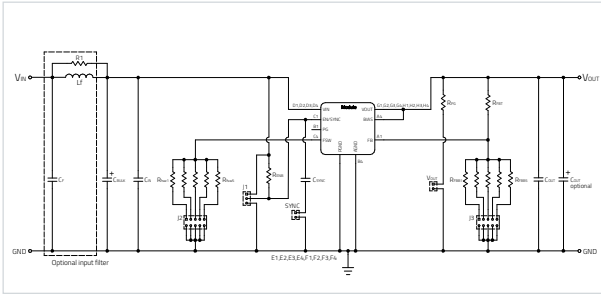
MagI³C Power Module Evaluation Board for 1710X3601 LGA-26

Evaluation Board 1780X3601

Version 1.0

SCHEMATIC

Features 1710X3601



The additional aluminum electrolytic capacitor C_{BULK} is only for evaluation board protection purposes. It is mounted at the termination of the supply line and provides slight damping of possible oscillations of the series resonance circuit represented by the inductance of the supply line and the input capacitance. It is not essential for operation.

For accurate V_{IN} and V_{OUT} voltage measurements it is recommended to measure directly at the test pins placed beside the input and output capacitors C_{IN} and C_{OUT}. It is **not** recommended to use this evaluation board with input and output wire lengths longer than 1 m.

For the datasheet of the power module visit us at: **https://www.we-online.com/catalog/en/MAGIC-VDLM**

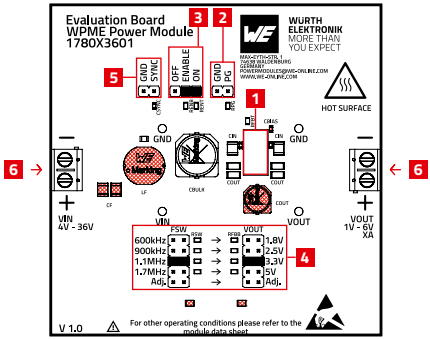
This product is highly sensitive to electrostatic discharge (ESD). As such, always use proper ESD precautions when handling. Failing to follow the aforementioned recommendations can result in severe damage to the part.

WARNING! – Before operating read the attached important notice document!

Ref. Des.	Description Order Code	
U1	MagI³C Power Module (1710X3601)	
C_{BULK}	Aluminum electrolytic capacitor 330µF, 50V (865230657014)	
C_{IN}	2 x Ceramic chip capacitor 10 µF, 50 V, X7R, 1210 (885012209073) + 2 x Ceramic chip capacitor 22 nF, 50 V, X7R, 0603 (885012206091)	
C_{BIAS}	Ceramic chip capacitor 1 µF/10 V/ X7R, 0603 (885012206026)	
CSYNC	Ceramic chip capacitor 1 nF/16 V/ X7R, 0603 (885012206034)	
C_{OUT}	4 x Ceramic chip capacitor 47 µF, 10 V, X5R, 1206 (885012108012)	
Cf	2 x Ceramic chip capacitor 10 µF, 50 V, X7R, 1210 (optional) (885012209073)	
Lf	Filter inductor, 3.3 µH, PD2 family, ISAT = 7 A, IR = 6 A (optional) (744776033)	
R_{FBT}	100 kΩ	
R_{FBB}	Set by jumper	24.9 kΩ for V_{OUT}= 5 V
		43.2 kΩ for V_{OUT}= 3.3 V
		66.5 kΩ for V_{OUT}= 2.5 V
		124 kΩ for V_{OUT}= 1.8 V
		To be soldered for adjustable output voltage $V_{OUT} = V_{REF}\left(\frac{R_{FBT}}{R_{FBB}} + 1\right)$
J1	Jumper for EN connection to either VIN (device enabled) or GND (device disabled) (61300311121)	
J2	Jumper for switching frequency selection. Only one resistor should be selected at a time (61301021121)	
J3	Jumper for output voltage selection. Only one resistor should be selected at a time (61301021121)	

For Layout, Gerber and Step files visit us on www.we-online.com/catalog/en/MAGIC-VDLM

OVERVIEW



Description

V_{IN} 4 V – 36 V
V_{OUT} 1 V – 6 V
I_{OUT} 4 A / 5 A

1. VDLM Variable Step Down LGA Module LGA26
2. Connection pin for power good signal
3. Jumpers (J1) for ENABLE & shut off the Module
4. Jumpers to set predefined output voltage V_{OUT} and fsw
5. Connect an external square wave signal to this pin to synchronize to an external clock.
6. Terminal block screw connectors for V_{IN} and V_{OUT}

Absolute maximum ratings Caution:
Exceeding the abs. max. values given in the datasheet may affect the device negatively and may cause permanent damage.

This evaluation board is intended to be operated in a research and development environment under the supervision of qualified technicians and engineers who are trained and experienced in the safe use of electronics. This evaluation board was designed and tested according to CISPR32 Class B standards under Würth Elektronik laboratory test conditions, as indicated in the data sheet of the corresponding power module. Operation in other test setups may cause unintended electrical behavior and exceed the stated performance and limits imposed by the CISPR32 Class B standards. This evaluation board is not intended for usage in final applications. This evaluation board is not intended for resale.

Würth Elektronik eiSos GmbH & Co. KG
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