APPLICATION NOTE

ANP137 | 3-Phase EMI Filter Design Measurement – Calculation – Simulation

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1. INTRODUCTION

The aim of this application note is to provide the reader with a concise and comprehensive overview of the essential steps involved in designing a suitable line filter for 3-phase applications. A discrete line filter is designed using calculations and LTspice simulations, and the results are then validated in the EMI lab. This application note also covers the calculation of varistors and leakage currents. A basic understanding of the use of passive components, filter technology, and EMI measurement techniques is assumed. For the design of 1-phase line filters and for further basic knowledge, please refer to ANP015.

2. MEASUREMENT SETUP

To verify the filter performance under realistic operating conditions, a 4 kW industrial fan with an integrated inverter is selected as the device under test (DUT).

For the measurements, both the housing of the fan and the inverter, as well as the PE terminal of the EMI filter, are bonded to a metal plate using a low-inductance connection. This ensures a common reference for the common-mode current, as is typically the case for permanently installed components in a closed conductive housing. This test setup is shown in Figure 1 and Figure 2.

Figure 1: Block diagram of the test setup.

According to current standards, no measurement of conducted emissions below 150 kHz is required for this product category. However, it is expected that limit values in the frequency range from 9 kHz to 150 kHz will also be introduced in the near future (CISPR PAS 39:2024). As this application note does not address the change to the standard, this analysis is limited to the frequency range above 150 kHz.

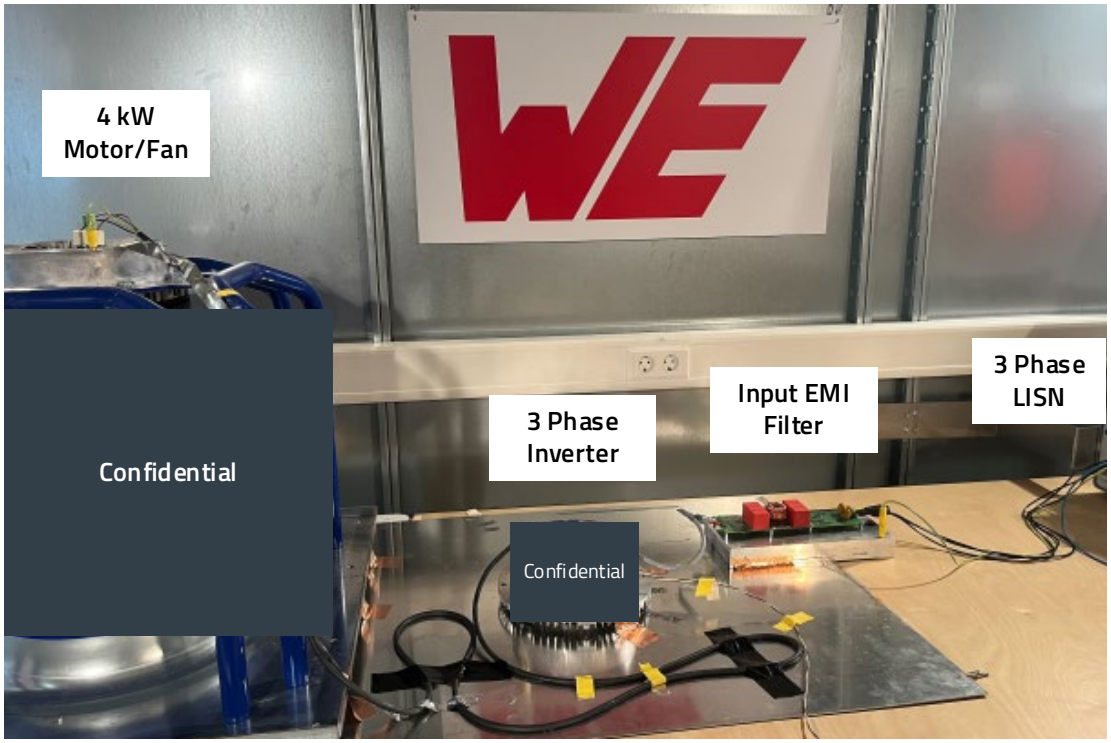

Figure 2: Test setup, conducted emissions 9 kHz – 30 MHz.

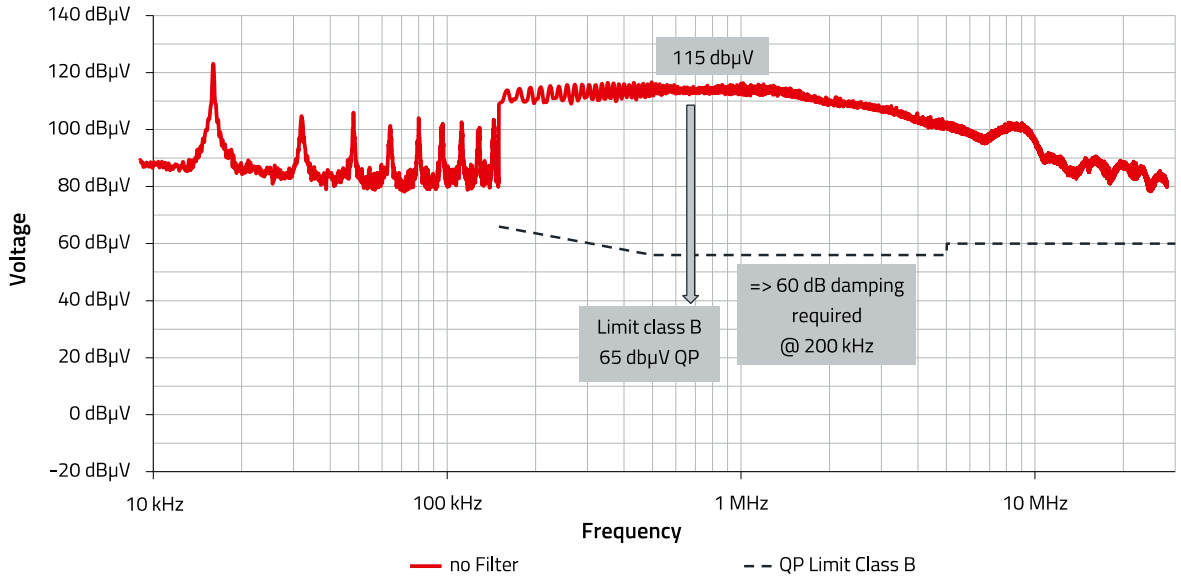

Figure 3: Quasi-peak (QP) measurement without EMI filter.

Prior measurement of the DUT is essential for optimum design of the EMI filter. The measured levels in Figure 3 serve as the starting point for determining the required filter attenuation. The lowest interference frequency is of particular importance here, as it determines the filter cutoff frequency and thus the physical dimensions of the components.

In this example, an interference voltage level of 115 dBµV (QP) was measured at 200 kHz. The QP limit according to CISPR 16 at this frequency is 65 dBµV.

An additional 10 dB margin is taken into account as a sufficient safety margin. This results in a required filter attenuation of 60 dB at 200 kHz.

The two different noise current paths have to be distinguished: common mode (CM) and differential mode (DM). For radio interference voltage measurements in accordance with CISPR 16-2-1, both interference current paths are always measured simultaneously. In the design of a line filter, it is advantageous at the outset to be able to measure both noise current paths, CM and DM, separately.

For the sake of simplicity, it is assumed that the DM and CM components are of equal magnitude. As shown in Figure 4 and Figure 5, the respective interference current components can be determined using a current clamp with sufficient bandwidth. If the magnitude of the two components differs significantly, it may be advantageous to define different cut-off frequencies for CM and DM in the subsequent calculation.

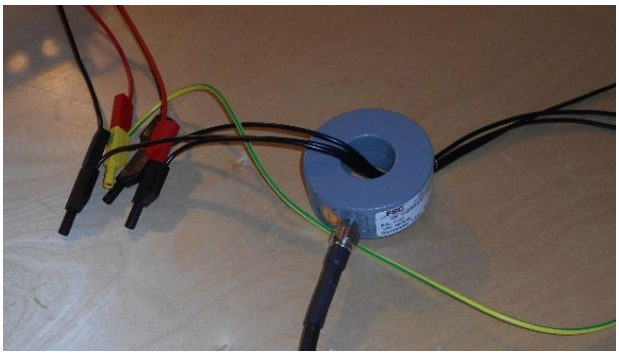

Figure 4: Common-mode (CM) measurement – all three phases pass through the current clamp.

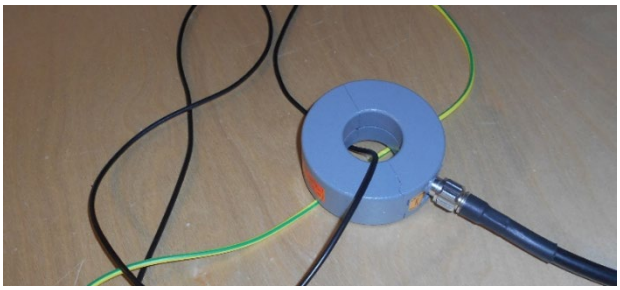

Figure 5: Differential-mode (DM) measurement with a residual common-mode (CM) component on one phase.

In the line impedance stabilization network (LISN) in Figure 6, three 50 Ω measurement resistors are used. In DM measurement, two 50 Ω resistors are always connected in series (R_{DM} = 100 Ω, phase-to-phase), whereas in CM measurement, three 50 Ω resistors have to be considered in parallel (R_{CM} = 16.6 Ω, phases to PE). The measuring receiver also has an input impedance of 50 Ω. This results in an overall attenuation of 6 dB.

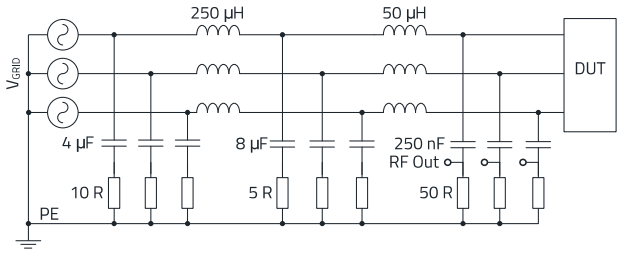

Figure 6: CISPR16 3-phase LISN.

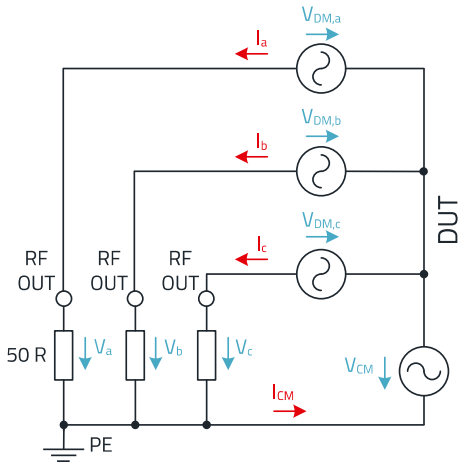

Figure 7: Simplified representation of the DM and CM currents/voltages between the LISN and the DUT.

$$R_{CM} = \frac{R_{LISN}}{3} = \frac{50\ \Omega}{3} = 16.67\ \Omega \quad (1)$$

$$R_{DM} = R_{LISN} \cdot 2 = 50\ \Omega \cdot 2 = 100\ \Omega \quad (2)$$

$$I_{CM} = I_a + I_b + I_c \quad (3)$$

$$V_{CM} = I_{CM} \cdot \frac{R_{LISN}}{3} = \frac{V_a + V_b + V_c}{3} \quad (4)$$

$$V_{DM\_a} = \frac{(2V_a - V_b - V_c)}{3} \quad (5)$$

For the subsequent simulation, it is helpful to determine the impedance relationships of the CM interference current loop.

These relationships are derived from the standardized measurement setup and the parasitic capacitive coupling within the DUT.

As described above, the CM impedance of the LISN with respect to the EMI chamber reference plane is 16.6 Ω. Within the DUT, a parasitic capacitance of 872 pF between the motor housing and the motor windings was measured using an LCR meter at a measurement frequency of 2 MHz.

$$X_{cMotor} = \frac{1}{2\pi f C_{Motor}} = \frac{1}{2\pi \cdot 2\ \text{MHz} \cdot 872\ \text{pF}} = 195\ \Omega \quad (6)$$

The motor housing, in turn, has a parasitic capacitance with respect to the EMI chamber reference plane. This depends on the surface area of the chassis (assumed to be 1 m²) and the distance to the reference plane (40 cm).

$$C_{Chassis\text{-}Referenceplane} = \frac{\varepsilon_0 \cdot A}{d} = \frac{8.85 \cdot 10^{-12}\ \frac{\text{AS}}{\text{Vm}} \cdot 1\ \text{m}^2}{0.4\ \text{m}} = 22\ \text{pF} \quad (7)$$

$$X_{cChassis\text{-}Referenceplane} = \frac{1}{2\pi f C} = \frac{1}{2\pi \cdot 2\ \text{MHz} \cdot 22\ \text{pF}} = 3.6\ \text{k}\Omega \quad (8)$$

The calculated impedance relationships of the CM current loop are shown in Figure 8.

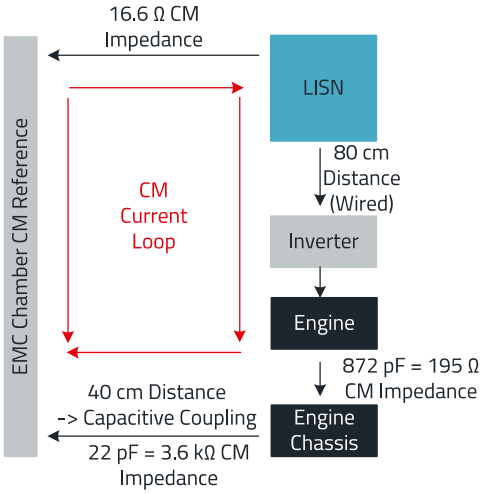

Figure 8: CM current loop and impedance relationships.

The impedance relationships in DM are determined on one hand by the defined 100 Ω of the LISN and by the input impedance of the inverter power electronics on the other.

The latter depends on various factors, such as the rectifier, the PFC stage, and the input capacitors. In practice, the input impedance can typically range between 0.1 Ω and 10 Ω. For simplification, a value of 1 Ω is assumed for the LTspice simulation in this application note.
The lower this value is, the less effective the X capacitors on the DUT side become or their capacitance must be increased significantly (i.e. the capacitive reactance decreases).

By taking the determined CM and DM impedances into account, the LTspice simulation then provides more realistic results. The CM impedance analysis at 2 MHz is only an approximation and is frequency-dependent. This applies only if the housing is not connected to PE.

3. EMI FILTER CALCULATION

To achieve the desired insertion loss of an EMI filter, it is crucial to arrange the filter components between the DUT and the LISN in the correct order. As indicated by the previous analysis, the interference current source in CM exhibits a high impedance, whereas the interference current source in DM is comparatively low-impedance. For this reason, the Y capacitors of the CM filter must be placed in parallel with the DUT, while the X capacitors of the DM filter are arranged in parallel with the LISN. In the example shown below, a CLC filter structure (π filter) is used for the DM filter, in which the

X capacitors are placed on both sides of the common-mode choke (CMC). If, by contrast, an LC filter with only a single X capacitor stage is used, it must always be arranged in parallel with the LISN.

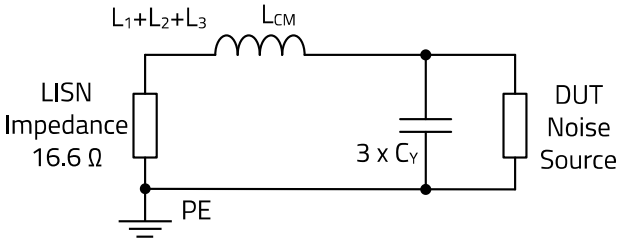

Figure 9: CM filter component placement.

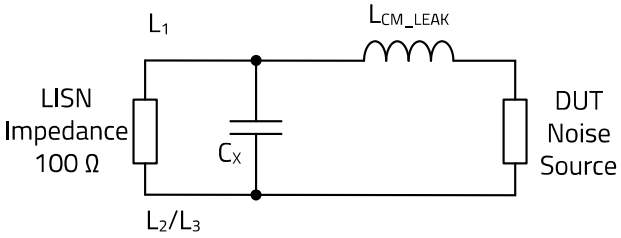

Figure 10: DM filter component placement; in a CLC structure, an additional C_X is located on the DUT side.

In 3-phase systems, an additional option for connecting the X capacitors arises compared to 1-phase applications. If the X capacitors are connected directly between the phases (phase-to-phase), an X1 type has to be used. This type of capacitor typically has a rated voltage of 440 V_{AC} and is designed for surge voltages of up to 4 kV. However, compared to an X2 type (310 V_{AC}, 2.5 kV surge) of the same capacitance, it has the disadvantage of higher cost and a larger package size. Since X2 capacitors, due to their insufficient rated voltage of 310 V_{AC}, must not be connected directly between the phases, a star configuration, as shown in Figure 11, is commonly used in practice, which halves the voltage across each X2 capacitor. Due to ageing effects, which cause the capacitance of the individual X-capacitors to degrade at different rates, larger asymmetries in the voltage distribution may occur over time.

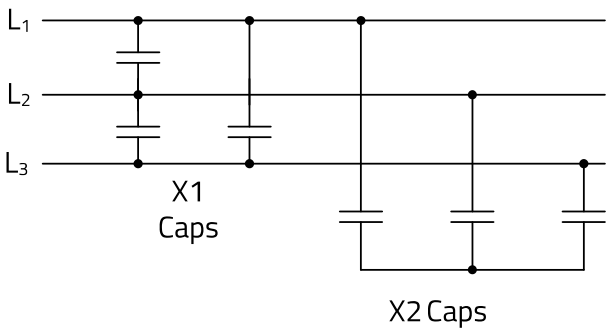

Figure 11: Connection options for X1 and X2 capacitors.

The star configuration also offers the advantage that a Y2 capacitor can be installed at the star point with respect to PE, as shown in Figure 12. This capacitor can have a significantly higher capacitance than what is typically used in conventional configurations. By connecting it at the star point, the leakage currents are significantly reduced, which is particularly advantageous for meeting regulatory limit values. A detailed discussion of this aspect is provided in a later section.

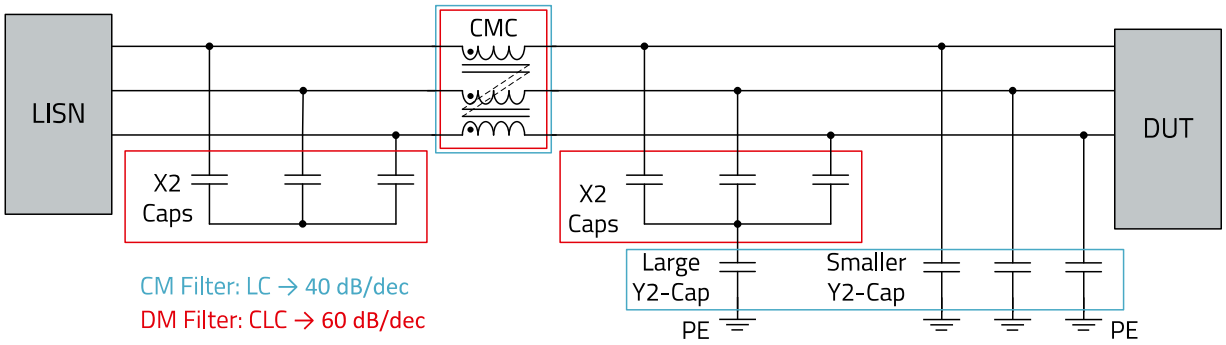

Figure 12: Filter structure used – including a combination of larger THT and smaller SMT ceramic Y2 capacitors. The larger THT capacitors increase the insertion loss in the range below 5 MHz, while the smaller SMT capacitors are effective above 5 MHz (see LTspice simulation).

From the preceding measurement without an EMI filter, it is clear that a filter is required which achieves an attenuation of 60 dB at 200 kHz (f_{sw}) in order to comply with the Class B limits.

For the calculation example, the filter structure shown in Figure 12 is used. In this configuration, the main inductance (L_{CM}) of the CMC, together with the Y2 capacitors, forms an LC-CM filter (blue) with an insertion loss of 40 dB/decade. The leakage inductance (L_{stray}) of the CMC, in combination with the X2 capacitors, forms a CLC-DM filter (red) that achieves an insertion loss of 60 dB/decade. These values apply above the respective filter cutoff frequency (f_{co}) and must be calculated based on the required attenuation (A_{fsw}).

First, the cutoff frequency (f_{co_CM}) for the LC-CM filter is determined:

$$A_{fsw} = \log\left(\frac{f_{sw}}{f_{co\_CM}}\right) \cdot 40\ \text{dB} \qquad (9)$$

$$f_{co\_CM} = \frac{f_{sw}}{10^{\frac{A_{fsw(dB)}}{40\ \text{dB}}}} = \frac{200\ \text{kHz}}{10^{\frac{60\ \text{dB}}{40\ \text{dB}}}} = 6.3\ \text{kHz}$$

Next, the cutoff frequency (f_{co_DM}) for the CLC-DM filter is determined:

$$A_{fsw} = \log\left(\frac{f_{sw}}{f_{co\_DM}}\right) \cdot 60\ \text{dB} \qquad (10)$$

$$f_{co\_DM} = \frac{f_{sw}}{10^{\frac{A_{fsw(dB)}}{60\ \text{dB}}}} = \frac{200\ \text{kHz}}{10^{\frac{60\ \text{dB}}{60\ \text{dB}}}} = 20\ \text{kHz}$$

Once both cutoff frequencies have been calculated, the component dimensioning can begin.

The process begins with defining capacitance values that can be freely chosen, while ensuring that electrical safety remains the highest priority. A safety-critical aspect is the maximum permissible leakage current, which is largely determined by the total capacitance of the Y capacitors used. For this reason, it is recommended to begin the dimensioning process with the maximum permissible total capacitance of the Y capacitors. For the filter in this calculation example, the following capacitors are used:

- 2 x 47 nF WCAP-FTY2 THT film capacitors;
- 3 x 2.2 nF WCAP-CSSA SMD ceramic capacitors.

The two larger THT film types are connected in series with the X2 capacitors at the star point. The effective total capacitance of all Y2 capacitors is calculated as follows.

$$C_{Y_{effektiv}} = \left(\frac{1}{C_{X1} + C_{X2} + C_{X3}} + \frac{1}{2 \cdot C_{Y_{groß}}}\right)^{-1} + (3 \cdot C_{Y_{klein}}) \qquad (11)$$

As the values of the X2 capacitors have not yet been calculated and are often 10 to 100 times larger in capacitance than the Y2 capacitors (which have little effect in a series connection), the equation can be simplified accordingly:

$$C_{Y_{effektiv}} = \left(2 \cdot C_{Y_{groß}}\right) + \left(3 \cdot C_{Y_{klein}}\right) \qquad (12)$$

$$C_{Y_{effektiv}} = (2 \cdot 47\ \text{nF}) + (3 \cdot 2.2\ \text{nF}) \approx 100\ \text{nF}$$

If MLCCs are used, sufficient clearance and creepage distances must be ensured with respect to the maximum operating voltage.

The missing element for the LC-CM filter is the main inductance (L_{CM}) of the CMC. For this purpose, the previously calculated filter cutoff frequency (f_{co_CM}) is also used.

$$L_{CM} = \frac{1}{(2\pi f_{co\_CM})^2 C_y} = \frac{1}{(2\pi \cdot 6.3\,\text{kHz})^2 \cdot 100\,\text{nF}} = 6.4\,\text{mH} \quad (13)$$

Due to the frequency and temperature dependence of many CMC core materials, as well as component tolerances, it is recommended to select an inductor with a nominal inductance 30% higher than the calculated value.

- Selected CMC: **8.4 mH** WE-TPB (I_r: 7.5 A)

This completes the calculation of the components for the LC-CM filter.

In the next step, the components for the CLC-DM filter must be calculated. The leakage inductance (L_{leak}) of the selected 8.4 mH CMC forms the inductive element "L". This must be determined first. The value of the leakage inductance (L_{leak}) is often not specified in the datasheets.

However, it can be determined very easily using the REDEXPERT simulation tool. For this purpose, the cursor in Figure 13 is positioned in a linearly rising (i.e. inductive) region.

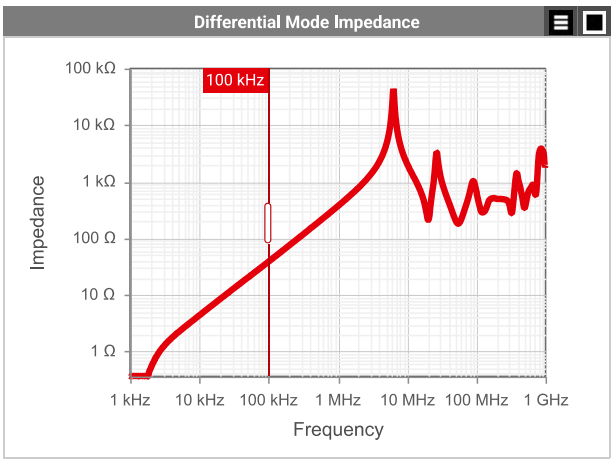

Figure 13: DM impedance curve of the 8.4 mH CMC (744833084075) from REDEXPERT.

In this example, the cursor was set to 100 kHz (f_{leak}), and the resulting impedance (X_L) was read from the table above in REDEXPERT: 39 Ω.

Using the impedance (X_L) and the frequency (f_{leak}), the leakage inductance (L_{leak}) can be calculated as follows:

$$L_{leak} = \frac{X_L}{2\pi f_{leak}} = \frac{39\,\Omega}{2\pi \cdot 100\,\text{kHz}} = 62\,\mu\text{H} \quad (14)$$

Finally, the values of the X2 capacitors must be determined in order to achieve the required cutoff frequency of 20 kHz.

$$C_x = \frac{1}{(2\pi f_{co\_DM})^2 L_{leak}} = \frac{1}{(2\pi \cdot 20\,\text{kHz})^2 \cdot 62\,\mu\text{H}} = 1.02\,\mu\text{F} \quad (15)$$

In this example, the X2 capacitors are arranged in a star configuration, causing them to form a series connection in pairs between the respective phases. The resulting capacitance of two identical capacitors connected in series is halved. As the CLC-DM filter represents a pi (π) structure, from a small-signal analysis perspective, the two X2 capacitor groups before and after the CMC are also connected in series. The effective X2 capacitance between two phases, C_{XG}, is therefore halved once again and is calculated as follows:

$$C_{XG} = \left(\frac{C_{X1} \cdot C_{X2}}{C_{X1} + C_{X2}}\right) : 2 = \left(\frac{4.7\,\mu\text{F} \cdot 4.7\,\mu\text{F}}{4.7\,\mu\text{F} + 4.7\,\mu\text{F}}\right) : 2 = 1.18\,\mu\text{F} \quad (16)$$

To obtain the required 1.02 µF, a total of six 4.7 µF WCAP-FTXX capacitors (890334027030CS) must be used, taking into account the twofold halving resulting from the series connections.

4. LTSPICE FILTER SIMULATION

It is recommended to first verify the frequency response of the calculated filter using a simulation tool before it is finally transferred to a circuit diagram and layout. The free simulation tool LTspice is used in this application note. The latest version of LTspice comes with all required Würth Elektronik passive components in the standard library (searchable by part number). Additional components can be found in the "Contrib" folder, including the WE-TPB CMC calculated here. The simulation is shown in Figure 14 and Figure 15.

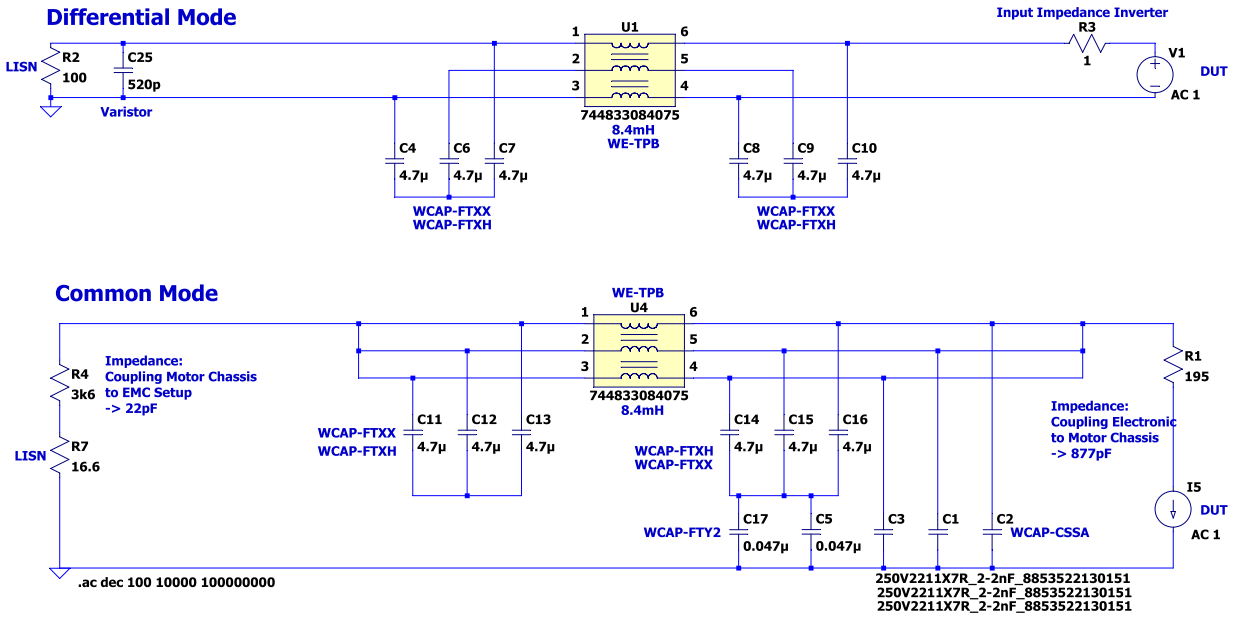

Figure 14: Filter structure used – including a combination of larger THT and smaller SMT ceramic Y2 capacitors. The larger THT capacitors increase the insertion loss in the range below 5 MHz, while the smaller SMT capacitors are effective above 5 MHz (see LTspice simulation).

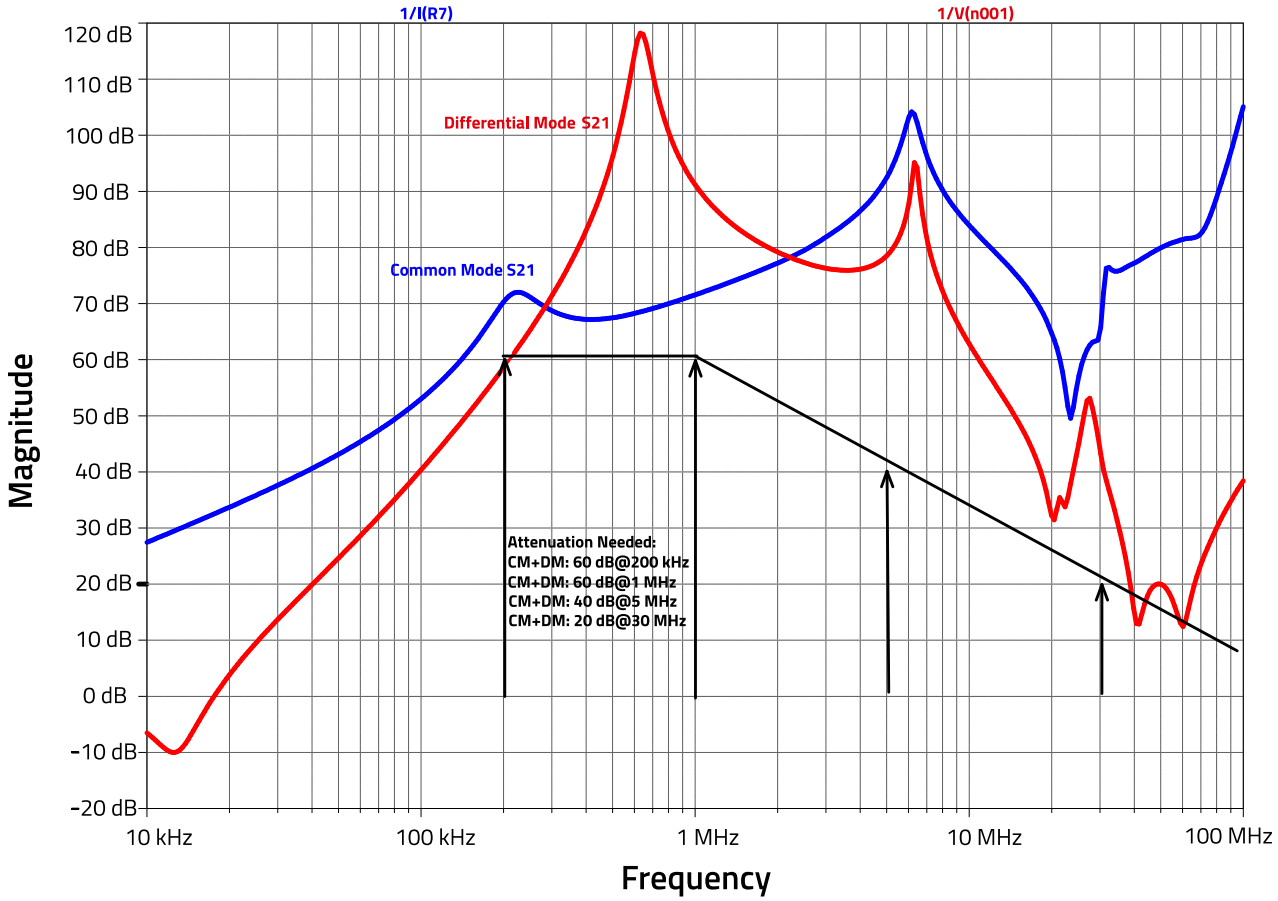

*Figure 15: Simulation of the filter insertion loss, shown separately for CM (blue) and DM (red). The **black** line shows the required attenuation based on the preliminary measurement without the filter.*

The LTspice simulation confirms that the selected passive components not only achieve the required attenuation of at least 60 dB at 200 kHz, but also provide the necessary insertion loss up to and beyond 30 MHz.

The increase in the blue CM insertion loss above 10 MHz is attributable to the three smaller MLCC Y2 capacitors. To obtain results as close to reality as possible, the following points should be considered in the simulation:

- Use components with realistic parasitic values;
- Enter the real loads (LISN) and source impedances (DUT);
- DM source impedance: low-impedance voltage source;
- CM source impedance: high-impedance current source.

5. CIRCUIT DIAGRAM & PCB EMI FILTER

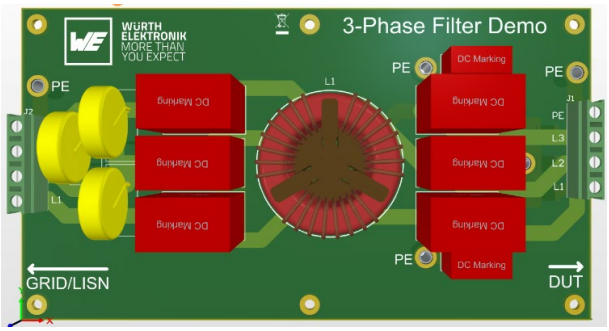

Figure 16: 3D top view of the 3-phase filter PCB.

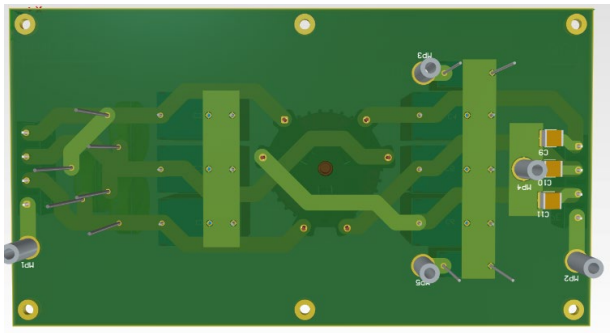

Figure 17: 3D bottom view of the 3-phase filter PCB.

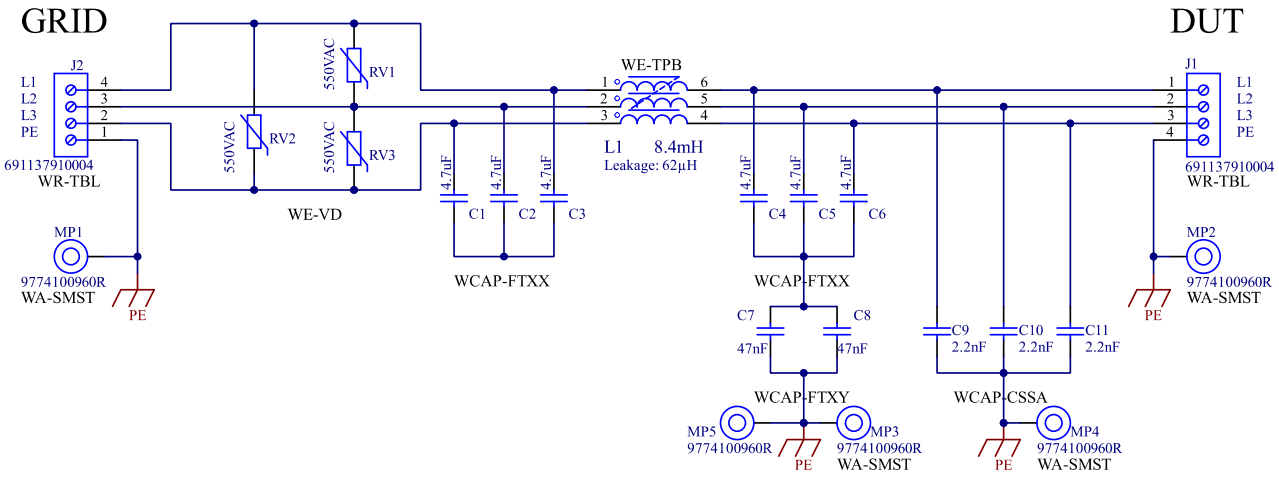

Figure 18: Altium circuit diagram 3-phase filter board.

6. LAYOUT GUIDELINES FOR THE EMI FILTER

A critical aspect of the layout is the correct connection of the Y capacitors to PE. This connection should be made along the shortest possible path and with minimal parasitic inductance. In practice, this is most easily achieved by using SMT spacers such as the WA-SMST. For multi-stage filters, the PE connection of the Y capacitor stages should not be implemented directly on the PCB. The reference potential for CM interference is the housing connected to PE. It is therefore crucial that all Y capacitors are connected to this PE reference potential via the shortest possible path, as shown in Figure 19.

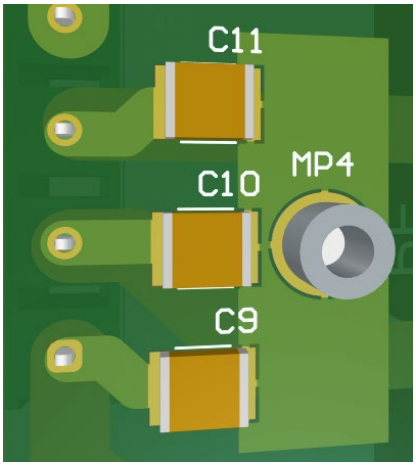

Figure 19: The low-inductance connection of the WCAP-CSSA Y2 ceramic capacitors to PE can be implemented using WA-SMST SMT-mountable spacers.

If the required clearance and creepage distances cannot be maintained. the THT Y2 capacitors, such as WCAP-FTY2, should be used, as shown in Figure 20.

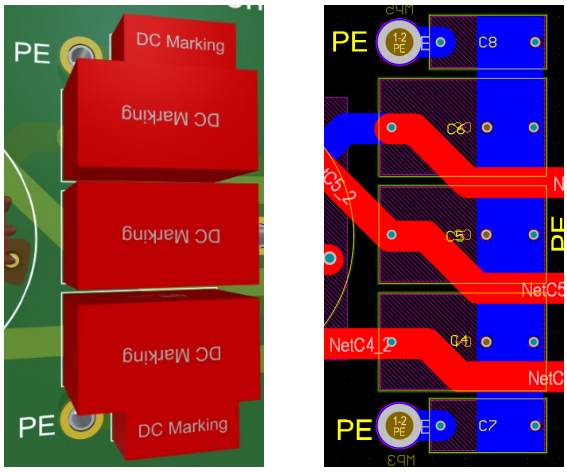

Figure 20: 3D and 2D views of the connection of the X2 and Y2 film capacitors (WCAP-FTXX / WCAP-FTY2).

Larger Y2 film capacitors must also be connected to the PE reference potential via WA-SMST SMT spacers along the shortest possible path and with minimal parasitic inductance. In compliance with all required clearance and creepage distances, the pins or terminals of all components should be directly connected to the traces. Stub traces should be avoided whenever possible. In addition, large-area polygon planes should not be used anywhere in the filter to minimize unwanted parasitic coupling effects. A possible filter PCB is shown in Figure 21.

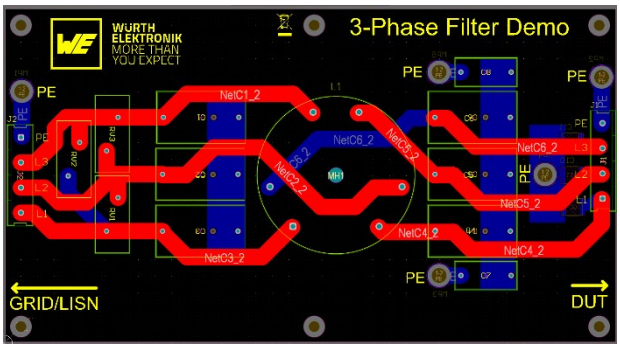

Figure 21: 2D overall view of the 3-phase filter PCB.

7. MEASUREMENT WITH EMI FILTER

As shown in Figure 22, the calculated and simulated filter provides the desired attenuation (green) over the relevant frequency range. However, if the Y capacitors are not placed on the DUT side of the CMC, but instead towards the LISN, they cannot form a low-impedance capacitive feedback path, which reduces the filter's effect over a wide frequency range (orange). If the small Y capacitors are removed, the emissions above 5 MHz rise significantly. The final result indicates that it makes sense to first design the filter mathematically based on the lowest interference frequency. In the second step, the selected components should be verified through simple simulation to check their insertion loss across the relevant frequency band.

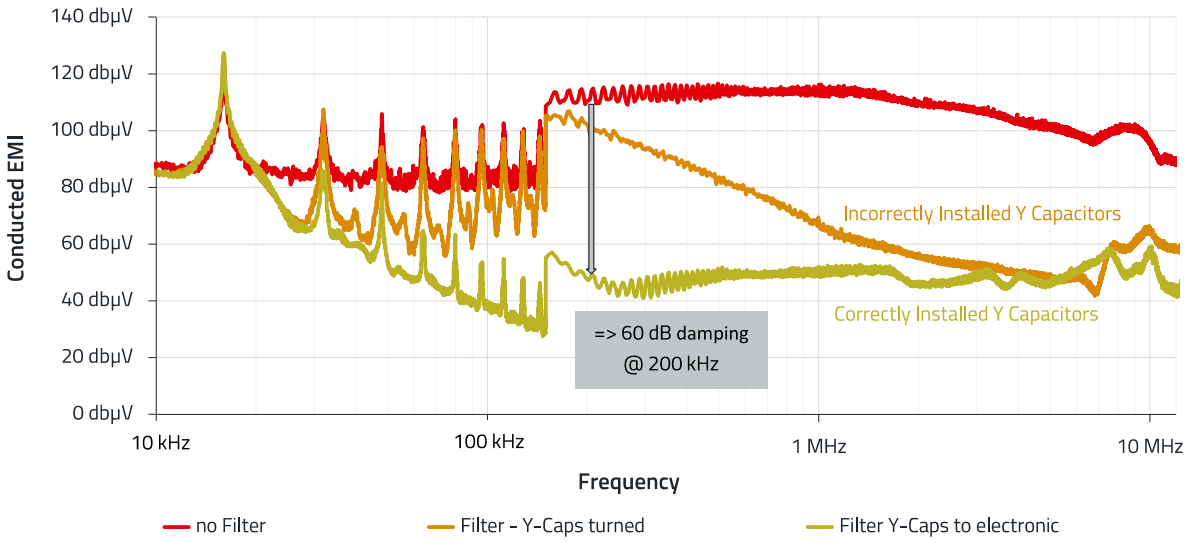

Figure 22: Measurement of the DUT without EMI filter (red), with EMI filter rotated 180° (orange) and with correctly placed EMI filter (green).

8. DIMENSIONING OF THE VARISTOR FOR 4 KV SURGE TEST BETWEEN THE PHASES

In the design shown in Figure 23, the "worst-case" scenario for the varistor is assumed. This is the case at 2 Ω surge generator output impedance, as the highest current can flow through the varistor in this case. The 8/20 µs current curve in Figure 24 shows that the generator can drive into a short circuit, serving as the basis for the calculation.

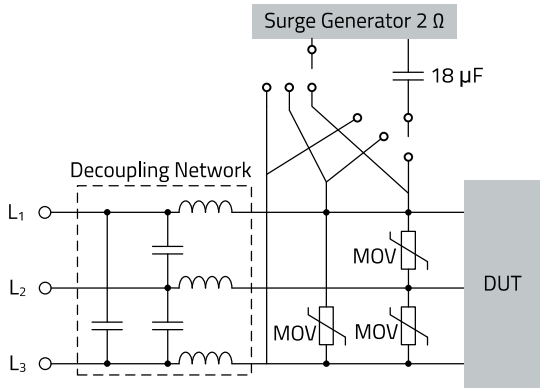

Figure 23: Schematic test setup for the surge test according to IEC 61000-4-5.

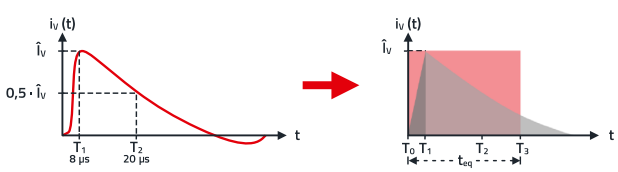

Figure 24: Surge generator short-circuit current curve (8/20 µs pulse).

The energy contained in the pulse is determined as follows:

$$W_V = \int_0^T I_V(t) \cdot V_V(t)\,dt \sim \hat{I}_V \cdot \hat{V}_V \cdot t_{eq} \qquad (17)$$

Whereby:

- T: time period under analysis;
- $I_{v(t)}$ and $V_{v(t)}$: Current and voltage as a function of time.

A conservative approximation of the integral is carried out according to Figure 24 with the current and voltage peak values over the time period t_{eq} in an energy-equivalent rectangular pulse.

A simpler and more practical alternative is to convert the area of the curve into an equivalent rectangular pulse. Here, the pulse duration t_{eq} is calculated from two time intervals $t_{eq,1}$ and $t_{eq,2}$ as follows:

Linear rise:

$$t_{eq,1} = 0.5 \cdot T_1 \qquad (18)$$

Exponential fall:

$$t_{eq,2} = 1.4 \cdot (T_2 - T_1) \qquad (19)$$

Combined:

$$t_{eq} = t_{eq,1} + t_{eq,2} \qquad (20)$$

This results in an equivalent pulse duration of **20.8 µs** for an 8/20 µs surge pulse.

Example calculation:

- Industrial application capable of withstanding up to 1.6 kV without damage (e.g. max. reverse voltage of the bridge rectifier);
- Surge test with 4 kV (V_G) and 2 Ω (Z_G) generator output impedance between the outer conductors L and N;
- Mains voltage 400 V_{RMS} (V_{Grid}).

The working voltage (V_{RMS}) of the varistor is selected as follows so it doesn't switch to the conductive state under normal conditions:

$$V_{RMS} > V_{GRID} + Tolerance_{GRID} \quad (21)$$

$$V_{RMS} > 400\ V_{RMS} + 10\ \% = 400\ V \cdot 1.1 = 440\ V_{RMS}$$

The next suitable varistor is a type with 460 V_{RMS} operating voltage. The electrical properties are shown in Figure 25.

Electrical Properties:

Properties		Test conditions	Value	Unit	Tol.
AC Operating Voltage	V_{RMS}		460	V	max.
DC Operating Voltage	V_{DC}		615	V	max.
Clamping Voltage	V_{Clamp}	100 A @ 8/20 µs	1240	V	max.
(Reverse) Peak Pulse Current	I_{Peak}	@ 8/20 µs	10000	A	max.
Power Dissipation	P_{Diss}		1	W	max.
Energy Absorption	W_{max}	10/1000 µs	440	J	max.
Nominal Discharge Current	I_n		5	kA	max.
Measured Limiting Voltage	V_{ML}		1690	V	max.
(Reverse) Breakdown Voltage	V_{BR}	1 mA	750	V	±10%
(Channel) Input Capacitance	C_{Ch}	1 kHz	520	pF	typ.

Figure 25: Datasheet excerpt: electrical properties of the WE-VD 820424611 high-surge 20 mm disc varistor; the 460 V_{RMS} working voltage is already specified including the max. tolerance.

Experience shows that as far as the power loss P_{Diss} and energy absorption capacity W_{max} is concerned, this varistor must have a diameter of at least 20 mm. The WE-VD 820424611 disc varistor is therefore selected for this example. The datasheet specifies a maximum clamping voltage (V_{CLAMP}) of 1240 V. This relates to a 100 A surge pulse. However, in the actual surge test the current through the varistor is many times higher.

The most unfavorable case is assumed in the following analysis, in which the varistor is connected directly to the surge generator output. The maximum clamping voltage is determined in this process. This must not exceed the reverse voltage of the semiconductors to be protected.

The first step is to determine the maximum current through the varistor. The calculation is carried out with the maximum clamping voltage (V_{CLAMP_max}) at the short-circuit current I_G) of the surge generator. To determine V_{CLAMP_max}, the V/I characteristic (incl. +10% tol.) for the component is required. (Figure 26) This can be displayed in REDEXPERT; the values for the short-circuit current (I_G) can be found using the cursor. For the worst case, the peak value (400 V_{RMS} x 1.41 = 564 V_{RMS}) of the mains voltage must also be added to the generator voltage (V_G).

$$I_G = \frac{V_G + V_{GRID}}{Z_G} = \frac{4\ kV + 564\ V}{2\ \Omega} = 2282\ A \quad (22)$$

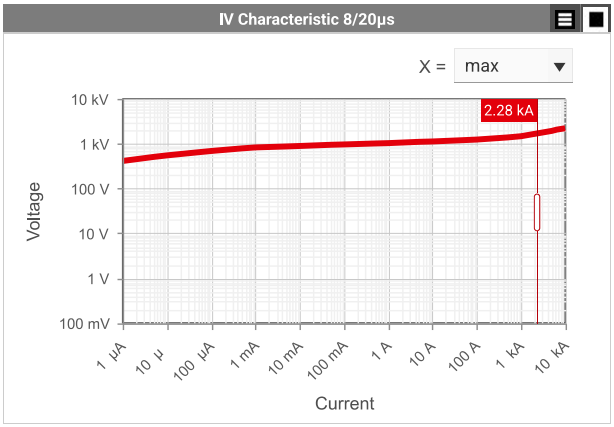

Figure 26: V/I characteristic from REDEXPERT of the WE-VD disk varistor 820424611, +10% tolerance at 2282 A → 1.69 kV. The desired tolerance can be selected using the drop-down tile at the top right.

$$V_{CALMP\_max} \rightarrow 1.69\ kV$$

The varistor current (I_{C1}) to be expected can now be further approximated to:

$$I_{C1} = \frac{V_G + V_{GRID} - V_{CLAMP\_max}}{Z_G} = \frac{4\ kV + 564\ V - 1.69\ kV}{2\ \Omega} \quad (23)$$

$$I_{C1} = 1437\ A$$

The next step is to determine the actual max. clamping voltage using the V/I curve in Figure 27 for current I_{C1}:

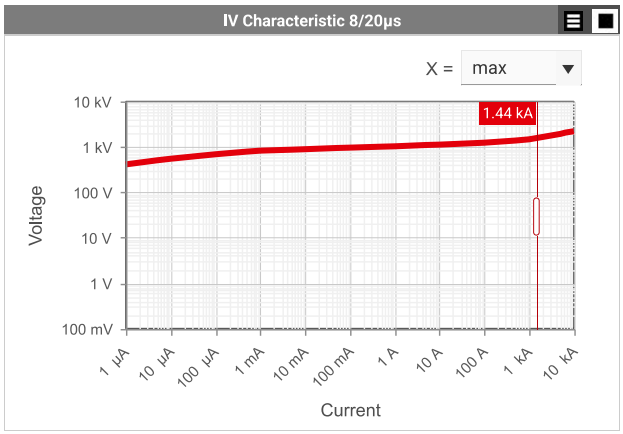

Figure 27: REDEXPERT V/I characteristic for the WE-VD disc varistor 820424611, +10% tolerance at 1437 A. The desired tolerance can be selected using the drop-down tile at the top right.

$$V_{CALMP\_max} \rightarrow 1560\ V$$

The requirement of max. 1.6 kV from the system specification is therefore complied with.

The graph is then set in REDEXPERT to 'min' tolerance, as shown in Figure 28, and the minimum possible clamping voltage V_{CLAMP_min} is read off for I_{C1} = 1437 A. This is required in order to determine the maximum possible current (I_{C_max}) through the varistor.

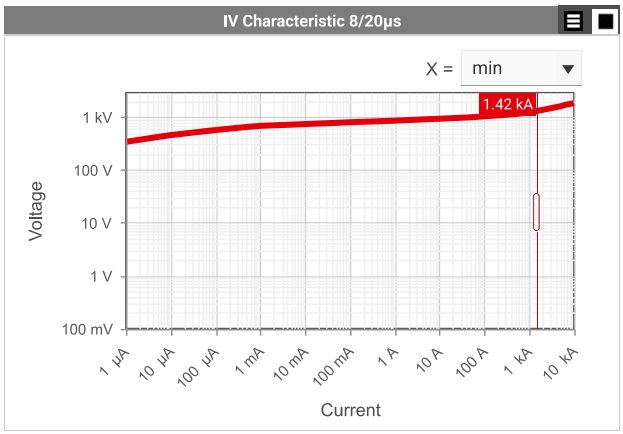

Figure 28: REDEXPERT V/I characteristic for the WE-VD disc varistor 820424611, -10% tolerance at 1423 A. The desired tolerance can be selected using the drop-down tile at the top right.

$$V_{CALMP\_max} \rightarrow 1290\ V$$

$$I_{C\_max} = \frac{V_G + V_{GRID} - V_{CLAMP\_min}}{Z_G} = \frac{4\ kV + 564\ V - 1290\ V}{2\ \Omega} \quad (24)$$

$$I_{C\_max} = 1637\ A \quad (25)$$

Now check how many 1637 A current pulses the selected varistor can withstand in relation to its lifetime. It is important that the varistor does not fail during the surge test with a total of 40 pulses (5x positive, 5x negative, at 0°, 90°, 180°, 270° phase angle). The graph in Figure 29 from the datasheet presents a set of curves illustrating the lifetime of the varistor as a function of the number of pulses and the pulse duration at various maximum currents flowing through the varistor.

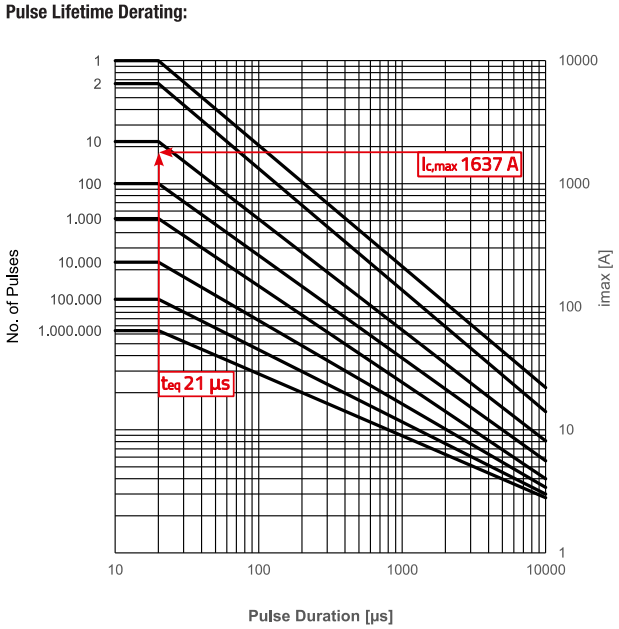

Figure 29: Lifetime derating as a function of current, pulse length and number of pulses.

Using a rectangular equivalent of 21.16 µs and a current of 1637 A, the varistor safely withstands approx. 45 pulses. A total of 40 pulse loads occurs during the surge test in accordance with IEC/EN 61000-4-5.

Next, the maximum energy emitted in the varistor is checked:

$$W_{max} = I_{C\_max} \cdot V_{CLAMP\_min} \cdot t_{Pulse} \quad (26)$$

$$W_{max} = 1637\ A \cdot 1290\ V \cdot 20.8\ \mu s = 43.9\ J \quad (27)$$

The datasheet specifies a maximum possible energy absorption of 440 J. It is then investigated whether the varistor has enough time to cool down between surge pulses (T_{cool}). IEC 61000-4-5 specifies that a pulse should be sent to the DUT every 60 seconds.

A maximum power loss P_{diss} of 1 W can be taken from the datasheet.

$$T_{cool} > \frac{W_{max}}{P_{diss}} = \frac{44.7\ J}{1\ W} = 44.7\ s \quad (28)$$

The selected varistor needs less than 45 seconds to cool down and is therefore ideally suited for use in the application. The entire worst-case analysis applies when the positive surge pulse occurs at a 90° phase angle and the negative pulse at 270°. For all other phase angles, the load for the varistor is significantly lower.

9. CALCULATION OF THE LEAKAGE CURRENT THROUGH THE Y CAPACITORS

Y capacitors are an effective instrument for reducing common-mode emissions. The greater the capacitance selected, usually the greater the reduction in EMI levels. However, the leakage currents to PE also increase with rising capacitance. Depending on the industrial standard and protection class, leakage currents from a few µA (e.g. medical technology) to many mA (e.g. permanently installed industrial systems) are permitted. In practice, a cap on the limit values for common applications with protective conductors is 3.5 mA.

In addition, the level of the leakage current depends on the mains voltage U_{GRID}, the mains frequency f_{GRID}, and the X capacitors.

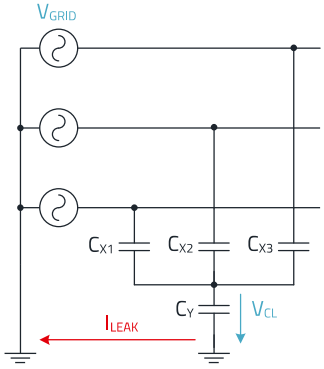

Figure 30: Y2 capacitor in series with X2 capacitors in a star configuration.

In a fully balanced X capacitor network in a star configuration (Figure 30), theoretically no leakage current (I_{leak}) would flow through the series-connected Y capacitor (C_Y).

In addition, tolerances in the mains voltage (V_{GRID}) between the three phases lead to additional asymmetries. If a mains voltage tolerance of 3% between the phases and a capacitor tolerance of 10% are taken into account, the worst-case leakage current results as follows:

$$\left|I_{leak\_max}\right| = 2\pi f \cdot C_{Y\_max} \cdot \frac{V_{GRID\_max} \cdot C_{X\_max} - V_{GRID\_min} \cdot C_{X\_min}}{C_{X\_max} + 2 \cdot C_{X\_min} + C_{Y\_max}} \quad (29)$$

Example calculation:

- C_X = 4.7 µF / C_Y=100 nF / ±10 % tol.;
- V_{GRID} = 400 V_{AC} 50 Hz / ±3 % tol. (EN50160).

$$\left|I_{leak\_max}\right| = 2\pi 50\ Hz \cdot 110\ nF \cdot \frac{412\ V \cdot 5.17\ \mu F - 388\ V \cdot 4.23\ \mu F}{5.17\ \mu F + 2 \cdot 4.23\ \mu F + 110\ nF} = 1.23\ mA \quad (30)$$

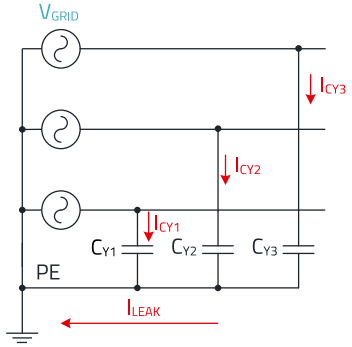

Figure 31: Alternative Y2 capacitor configuration directly from the phases to PE.

If the Y2 capacitors are connected as shown in Figure 31, the following calculation applies:

$$\left|I_{leak\_max}\right| = 2\pi f \cdot (C_{Y,max} - C_{Y,min}) \cdot V_{GRID\_max} \quad (31)$$

Example calculation:

- C_Y: 100 nF / +-10 % tol.;
- V_{GRID}: 400 VAC 50 Hz / +-3 %.

$$\left|I_{leak\_max}\right| = 2\pi \cdot 50\ Hz \cdot (110\ nF - 90\ nF) \cdot 412\ V = 2.59\ mA \quad (32)$$

The two calculation examples illustrate that leakage currents caused by Y capacitors can be significantly reduced in combination with a star configuration of the X capacitors. This advantage was deliberately taken into account in dimensioning the EMI filter.

The two large 47 nF Y2 capacitors used to suppress low-frequency CM interference components were placed at the star point of the X2 capacitors. The three smaller 2.2 nF Y2 capacitors, which are designed for high-frequency CM interference components, were connected directly between the phases and PE. This achieves broadband suppression of CM interference while keeping the leakage currents as low as possible.

10. CORE MATERIALS OF COMMON-MODE CHOKES

In common-mode chokes (CMCs) for three-phase systems, manganese-zinc (MnZn) and nanocrystalline (NC) materials are most commonly used as core materials. Impedance curves of various CMCs are shown in Figure 32 to Figure 34.

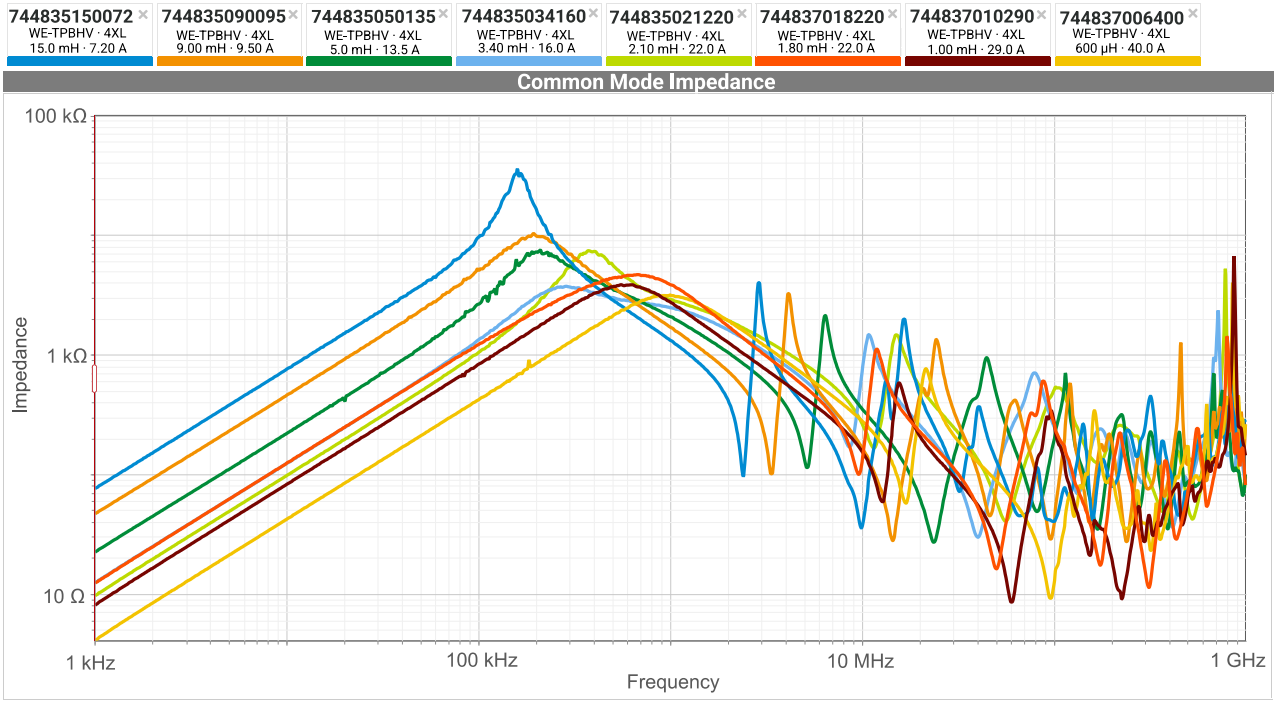

Figure 32: Impedance curves from REDEXPERT for CMCs of the WE-TPBHV series with manganese-zinc (MnZn) core material. A characteristic feature is the linear rise of the curve up to the first resonance frequency.

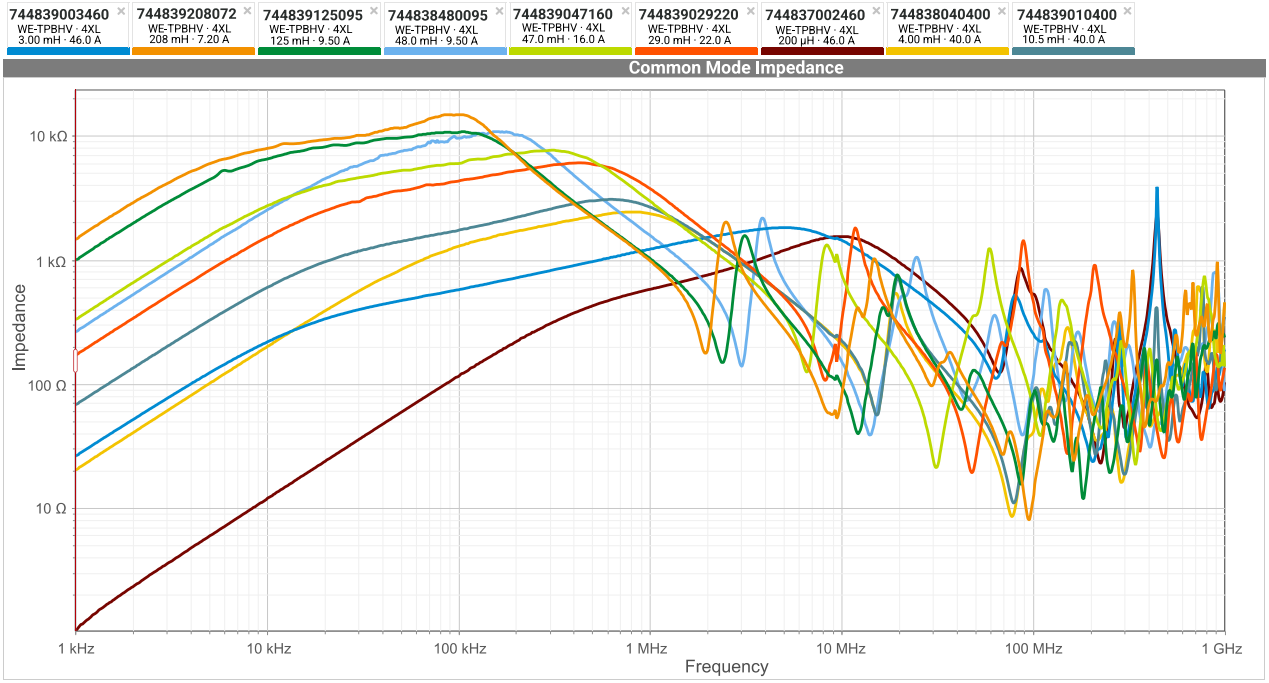

Figure 33: Impedance curves from REDEXPERT for CMCs of the WE-TPBHV series with nanocrystalline (NC) core material. Here, a characteristic bend can be observed in the rising section of the curve up to the first resonance.

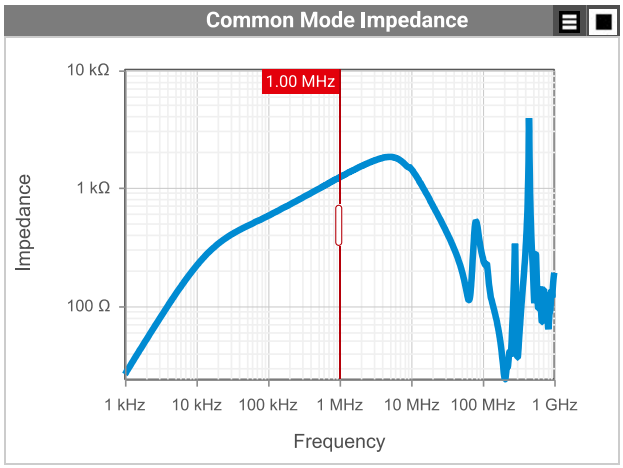

Figure 34: Impedance curve of the 744839003460 WE-TPBHV with nanocrystalline core. From approx. 10 kHz onward, the curve flattens significantly up to the first resonance.

As shown in Figure 34, the impedance curve of the common-mode inductance (L_{CM}) flattens significantly shortly after 10 kHz. The cause of this behavior is the frequency-dependent permeability of nanocrystalline cores in this frequency range. The datasheet for article number 744839003460 specifies a nominal inductance of 3 mH (±50% tol.), measured at 10 kHz. Using the cursor function in REDEXPERT, an impedance (X_L) of 217 Ω can be read at 10 kHz.

$$L_{CM} = \frac{XL}{2\pi f} = \frac{217\ \Omega}{2\pi \cdot 10\ \text{kHz}} = 3.46\ \text{mH} \qquad (33)$$

At first glance, the measured inductance (L_{CM}), taking the tolerance into account, matches the nominal inductance specified in the datasheet. If the cursor is set to 1 MHz, an impedance of 1.22 kΩ can be read.

$$L_{CM} = \frac{XL}{2\pi f} = \frac{1.22\ \text{k}\Omega}{2\pi \cdot 1\ \text{MHz}} = 194\ \mu\text{H} \qquad (34)$$

This results in a residual inductance (L_{CM}) of only 194 µH. This value must be taken into account in the mathematical design for the CM filter, and not the nominal inductance.

11. SUMMARY

It was shown how the developer can successfully design a 3-phase filter using simple mathematics, free design tools and common measurement technology. The primary aim is to correctly dimension the filter with regard to insertion loss in order to avoid unnecessary costs and to keep the filter as compact as possible. Würth Elektronik offers an extensive portfolio of passive and electromechanical components to establish a complete line filter.

12. PARTS LIST

Index	Description	Value	Package size	Art. no.
$C_{9, 10, 11}$	Y-Caps	2.2 nF / 250 V	2211	8853522130151
$C_{7, 8}$	Y-Caps	47 nF / 330 V	P 15 mm	890404125010CS
$C_{1, 2, 3, 4, 5, 6}$	X-Caps	4.7 µF / 310 V	P 275 mm	890334027030CS
$J_{1, 2}$	TBL	750 V / 24 A	P 7.5 mm	691137910004
L_1	CMC	8.4 mH / 7.5 A	47 mm	744833084075
$MP_{1, 2, 3, 4, 5}$	SMT Spacer	10 mm length	3.3/6 mm	9774100960R
$RV_{1, 2, 3}$	MOV	460 V / 6.5 kA	20 mm	820424611

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REVISION HISTORY

Document Version	Release Date	Changes
ANP137a	2026/02/17	Initial release of the application note

Note: *The current version of the document and the release date are indicated in the footer of each page of this document.*