

ANM004

SINGLE AND DOUBLE TAP EVENT
DETECTION

2533020201601,
25330202016011,
2533203301691

VERSION 1.2

AUGUST 29, 2025

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1 Abbreviations

Abbreviation	Description
FS	Full scale
I ² C	Inter integrated circuit
MEMS	Micro-electro-mechanical system
LSB	Least significant bit
ODR	Output data rate

2 Revision history

App note version	Notes	Date
1.0	<ul style="list-style-type: none">• Initial release of the app note	August 2021
1.1	<ul style="list-style-type: none">• Updated chapter Important notes• Updated chapter Legal notice	October 2024
1.2	<ul style="list-style-type: none">• Improved the description	August 2025

3 Introduction

The WSEN-ITDS 3-axis acceleration sensor (Part No: 2533020201601, 25330202016011) is equipped with built-in tap detection features, enabling intuitive human-machine interaction with minimal coding effort. The sensor can be configured to generate an interrupt signal on a dedicated pin when a tap is detected in any direction. The sensor can detect single and double tap events. Single and double tap recognition feature works similar to single click and double click of a mouse. These features can easily replace mechanical buttons in a display or monitors for user interfacing. It also provides more robust, user-friendly, simple and cost-effective design in with high system integration.

The single tap detection feature recognizes a user's finger tap on a device. The impact from the tap is measured by analyzing the amplitude of the acceleration detected by the sensor. When the acceleration amplitude exceeds a certain threshold and returns back within a short time the single tap interrupt is generated.

Double tap detection feature will recognize two consecutive taps on the device from the user. When two quick single taps are captured within a defined time frame the double tap interrupt is generated.

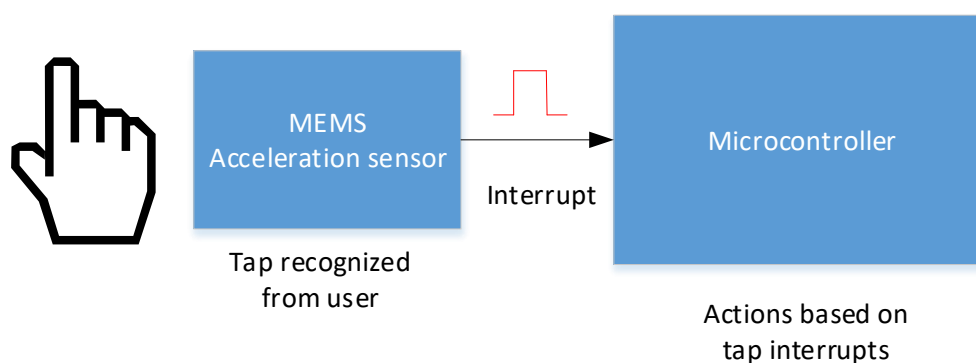


Figure 1: Tap event recognition from user

4 Single Tap Detection

When the high-pass filtered output data first rises above the defined threshold and then falls back below it within the specified shock time window, a single tap detection interrupt is generated. The direction of a single tap is recognised by enabling the TAP_X_EN, TAP_Y_EN and TAP_Z_EN bits of the TAP_Z_TH register.

Three parameters are necessary to enable the single tap detection feature which is shown in figure 2.

- Tap threshold
- Shock time
- Quiet time

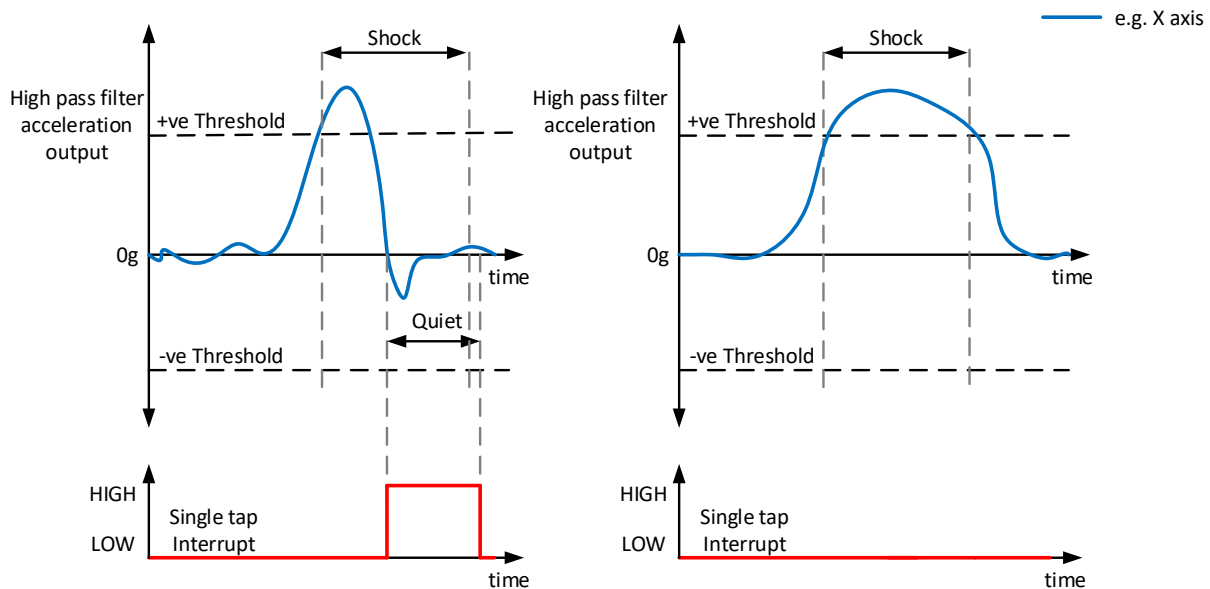


Figure 2: Single tap detection interrupt

4.1 Tap Threshold

The threshold defines the intensity of tap needed to generate the interrupt. The amplitude of tap is directly proportional to the force applied in either positive or negative axis of the sensor. The unsigned tap threshold is set using TAP_THSX[4_0], TAP_THSY[4_0], TAP_THSZ[4_0] bits of the TAP_X_TH, TAP_Y_TH and TAP_Z_TH registers. The tap threshold is valid for both positive and negative acceleration data. The value of 1 LSB change in threshold bits depends on the selected full scale range. i.e. 1 LSB = FS/32. Table 3 shows the possible tap threshold values for a full scale range of $\pm 2g$. Tap interrupts won't be generated if the threshold value is set to zero.

TAP_THX[4:0]	Threshold value (mg)
00001	$1 \cdot (2/32) = 62.5$
00010	$2 \cdot (2/32) = 125$
00011	$3 \cdot (2/32) = 187.5$
00100	$4 \cdot (2/32) = 250$
00101	$5 \cdot (2/32) = 312.5$
-	-
11111	$31 \cdot (2/32) = 1937.5$

Table 3: Tap threshold for $\pm 2g$

4.2 Shock Time Window

The shock time window sets the maximum allowed duration of a tap amplitude. After exceeding the set threshold when the acceleration falls below a set threshold within shock time window, an interrupt is generated. Otherwise the tap event is not recognised. The shock time window is set using SHOCK[1:0] bits of the INT_DUR register. By default SHOCK[1:0] bits are 00b which corresponds to 4/ODR. If the SHOCK[1:0] bits are set to different values, 1 LSB change in SHOCK[1:0] bits corresponds to 8/ODR time. Table 4 shows the possible shock time window values for a selected ODR of 400 Hz.

SHOCK[1:0]	Duration (ms)
00	$(4/400) = 10$
01	$1 \cdot (8/400) = 20$
10	$2 \cdot (8/400) = 40$
11	$3 \cdot (8/400) = 60$

Table 4: Shock time window

4.3 Quiet Time Window

The quiet time is a configurable interval in the WSEN-ITDS tap detection logic that defines the minimum amount of time during which no valid tap events should occur after a tap event is detected. It acts as a debounce period to prevent false or repeated detections caused by residual vibrations or unintended movements. It also determines the length of the interrupt pulse when latched mode is disabled. The quiet time window is set using QUIET[1:0] bits of the INT_DUR register. By default QUIET[1:0] bits are 00b which corresponds to 2/ODR. If the QUIET[1:0] bits are set to a different value, 1 LSB change in QUIET[1:0] bits corresponds to 4/ODR time. Table 5 shows the possible quiet time window values for a selected ODR of 400 Hz.

QUIET[1:0]	Duration (ms)
00	$(2/400) = 5$
01	$1 \cdot (4/400) = 10$
10	$2 \cdot (4/400) = 20$
11	$3 \cdot (4/400) = 30$

Table 5: Quiet time window

4.4 Tap Priority

The user can set the priority of tap direction using TAP_PRIOR[2:0] in the TAP_Y_TH register. TAP_PRIOR[2:0] bits are useful when a tap event is recognised on more than one axis at the same time. In this case, tap axis having higher priority set in TAP_Y_TH register is recognized.

4.5 Single Tap Interrupt Latching

The Latch feature on the single tap interrupt is enabled by LIR bit in CTRL_3 register. When the LIR bit is set to '1' the interrupt is kept high until the values of TAP_SRC or ALL_INT_SRC register is read. When LIR bit is set to '0' then latch feature is disabled. In this case, the single tap interrupt is kept high for the duration of quiet time which is set using QUIET[1:0] bits in INT_DUR register.



An output data rate of 400 Hz or above is required for the proper functioning of single and double tap detection

	Steps	Registers Involved
1	Enable high performance mode and select ODR	CTRL_1 (0x20)
2	Enable block data update and automatic address increment	CTRL_2 (0x21)
3	Select bandwidth and full scale range	CTRL_6 (0x25)
4	Set tap threshold for each axis, assign tap priority and enable tap detection on each axis	TAP_X_TH (0x30), TAP_Y_TH (0x31), TAP_Z_TH (0x32)
5	Set quiet time and shock time	INT_DUR (0x33)
6	Enable single tap detection & interrupts	WAKE_UP_TH (0x34), CTRL_7 (0x3F)
7	Route single tap detection to INT_0 pin	CTRL_4 (0x23)
8	Latch interrupt if needed	CTRL_3 (0x22)

Table 6: Configuration of single tap detection

5 Double Tap Detection

When configured for double tap detection, the WSEN-ITDS sensor generates an interrupt when two valid tap events are recognized in succession. Similar to single tap detection, double tap detection is governed by several parameters to minimize false positives and ensure accurate recognition.

The following parameters determine double tap detection:

- Tap threshold
- Shock time
- Quiet time
- Latency time

The first three parameters function the same as in single tap detection:

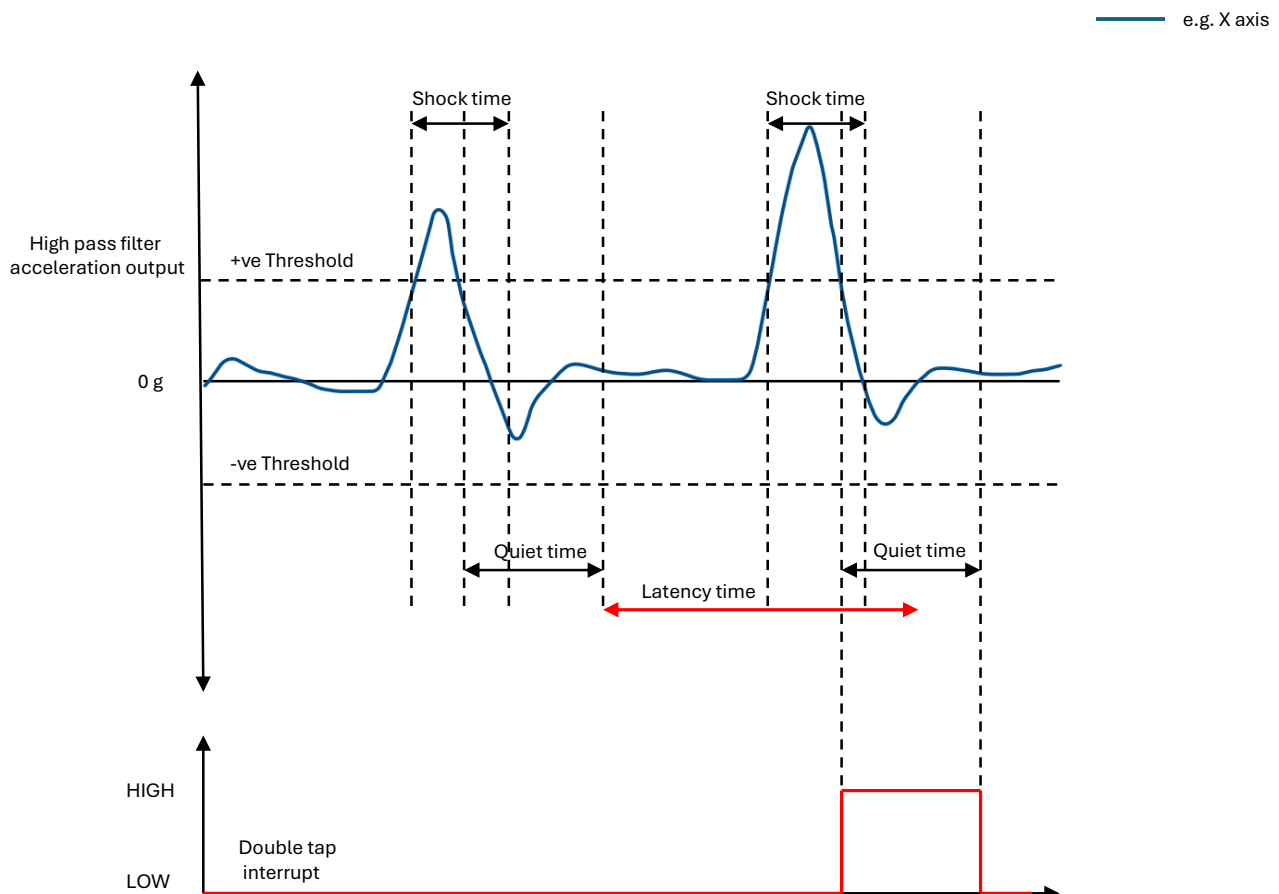


Figure 3: Double tap detection

The first tap is detected when the high pass filtered output exceeds the tap threshold and returns below it within the defined shock time. After detecting the first tap, the sensor waits for a

short interval, defined as the quiet time, during which any activity is ignored to prevent noise from triggering false taps. Following the quiet time, the sensor enters a window called latency time, during which it looks for a second tap. If a second tap is detected, meaning the high-pass filtered data again exceeds the threshold and falls back below it within the shock time, and this occurs within the latency time window, then a double tap interrupt is generated. Figure 3 shows how the double tap detection works when latched interrupt is not enabled.

The SINGLE_DOUBLE_TAP bit in WAKE_UP_TH register needs to be set to 1 to enable both single tap and double tap detection. Setting this bit to 0 enables only single-tap detection.



A single tap event is always detected before a double tap event

5.1 Latency Time

Latency time is the time window during which the sensor expects a second tap after a valid first tap has been detected in double tap detection mode. This parameter ensures that only taps occurring within a specific time frame are considered part of the same double tap gesture.

Latency time is a crucial parameter for the proper functioning of double tap detection. If the latency time is set too low, there is a risk that the second tap may occur outside the allowed window, and the double tap event will not be detected, as illustrated in Figure 4. Conversely, if the latency time is set too high, the sensor may mistakenly group unrelated taps into a double tap event, potentially causing false positives. However, a single tap will be detected in the case of Figure 4.

The latency time window can be configured using the bits LATENCY[3:0] from the INT_DUR register (0x33). By default the bits are set to 0000b, which is equivalent to 16/ODR time. If different values are assigned to LATENCY[3:0], then 1 LSB equals to 32/ODR time. Table 7 shows the possible latency time window values for a selected ODR of 400 Hz.

LATENCY[3:0]	Duration (ms)
0000	$(16/400) = 40$
0001	$1 \cdot (32/400) = 80$
0010	$2 \cdot (32/400) = 160$
0011	$3 \cdot (32/400) = 240$
0100	$4 \cdot (32/400) = 320$
-	-
1111	$15 \cdot (32/400) = 1200$

Table 7: Latency time window

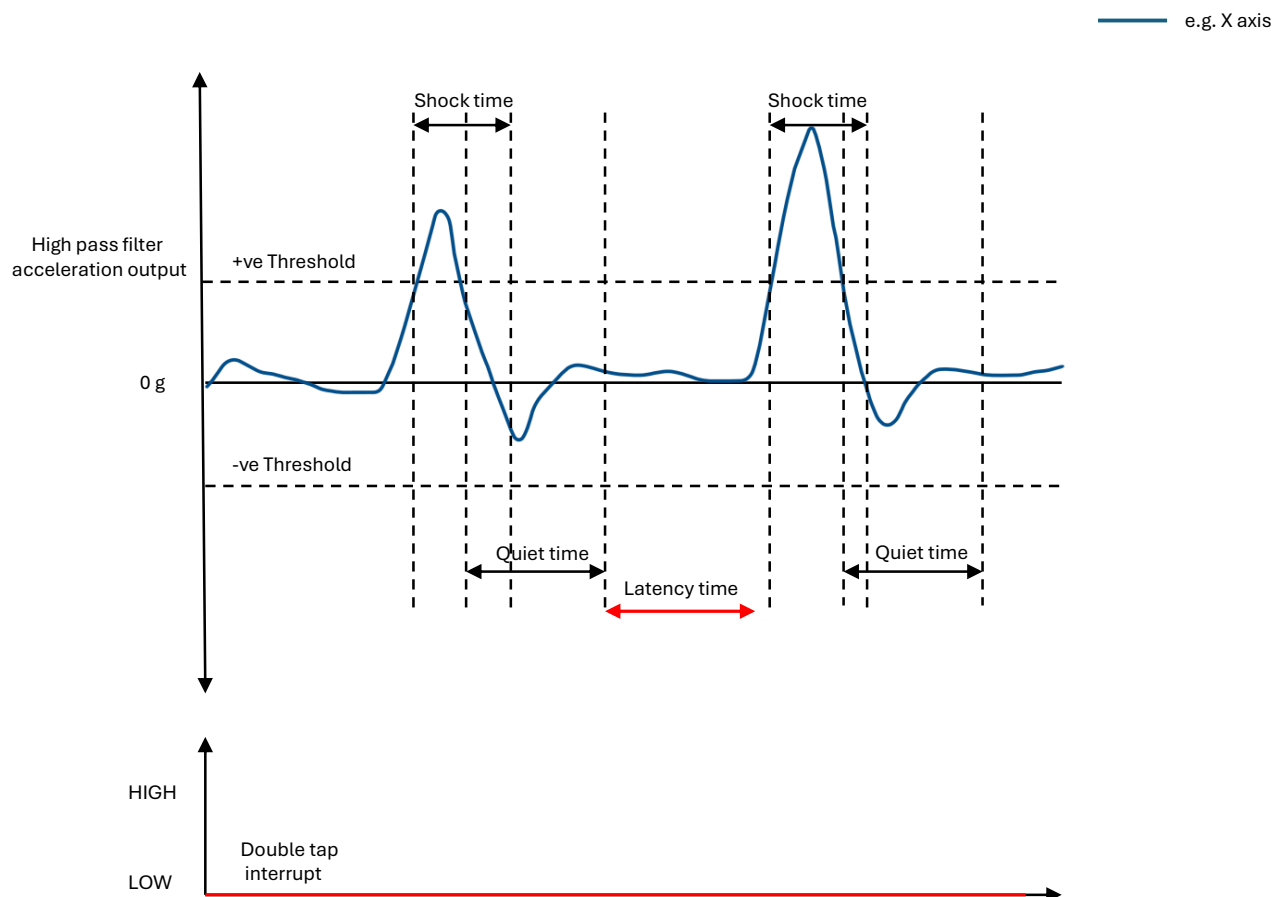


Figure 4: Double tap not detected

	Steps	Registers Involved
1	Enable high performance mode and select ODR	CTRL_1 (0x20)
2	Enable block data update and automatic address increment	CTRL_2 (0x21)
3	Select bandwidth and full scale range	CTRL_6 (0x25)
4	Set tap threshold for each axis, assign tap priority and enable tap detection on each axis	TAP_X_TH (0x30), TAP_Y_TH (0x31), TAP_Z_TH (0x32)
5	Set latency time, quiet time and shock time	INT_DUR (0x33)
6	Enable double tap detection & interrupts	WAKE_UP_TH (0x34), CTRL_7 (0x3F)
7	Route double tap detection to INT_0 pin	CTRL_4 (0x23)
8	Latch interrupt if needed	CTRL_3 (0x22)

Table 8: Configuration of double tap detection

6 Conclusion

The WSEN-ITDS 3-axis acceleration sensor offers an effective and compact solution for implementing physical tap-based user input through its built-in single and double tap detection features. By detecting intentional taps on a device's surface, it enables intuitive and responsive human-machine interaction. These features can replace traditional mechanical buttons, leading to simplified, cost-effective, and more reliable product designs. With easy configuration and minimal software requirements, the WSEN-ITDS is ideal for a variety of applications, including display controls, portable electronics, and embedded systems.



Visit our [GitHub](#) page for examples on tap detection

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