

APPLICATION NOTE

ANP143 | TVS diodes: basics, function and their applications



Dr.-Ing. (Doctor of Engineering) Heinz Zenkner

1. BASICS

TVS diodes (transient voltage suppressors) are used to protect circuits from high voltage spikes. They are designed to operate in reverse bias and work by discharging interference current when the reverse voltage exceeds the 'avalanche breakdown potential'. They are essentially high-power Zener diodes and represent a special form of avalanche diodes. TVS diodes can withstand large power spikes (hundreds or thousands of watts), but Zener diodes have a narrower voltage tolerance. TVS diodes generally have a higher parasitic capacitance than Zener diodes. They are available in either unidirectional or bidirectional versions. Unidirectional TVS diodes block up to the rated voltage in one direction and behave like a normal diode in forward bias in the other direction. Bidirectional TVS diodes block current flow in both directions up to the rated voltage (good for protecting AC signals). Unidirectional TVS diodes have a much faster response time than their bidirectional counterparts (e.g., 5 ps compared to 5 ns). The

electrical symbols for the unidirectional and bidirectional TVS diodes are shown in Figure 1.

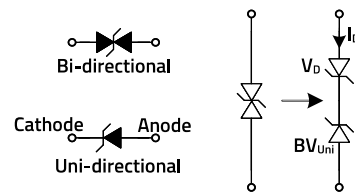


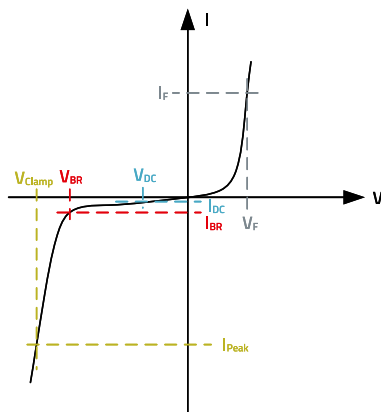
Figure 1: Electrical symbols for the uni- and bidirectional TVS diodes. Right figure: Functional equivalent of the bidirectional TVS diode.

The display on the right in Figure 1 shows how you can imagine a bidirectional TVS diode – as a circuit consisting of two TVS diodes connected in an “anti-serial” configuration. The typical voltage-current graphs of the diodes are displayed in Figure 2.

The parameters from the graphs above and the WE datasheets have the following meanings:

WE-TVSP Power TVS Diode, 824500101

Properties	Test conditions	Value	Unit	Tol.
DC Operating Voltage	V_{DC}	10	V	max.
(Reverse) Breakdown Voltage	V_{BR} 1 mA	11.7	V	±5%
Clamping Voltage	V_{clamp} I_{PEAK}	17	V	max.
(Reverse) Peak Pulse Current	I_{peak} 10/1000 μ s	23.5	A	max.
(Forward) Peak Pulse Current		40	A	max.
Leakage Current	I_{leak} V_{DC}	5	μ A	max.
Steady State Power Dissipation	P_{Diss} $T_A = 50^\circ C$	3.3	W	max.
Power Dissipation	P_{Diss} 10/1000 μ s	400	W	max.
Polarity	Unidirectional			



WE-TVSP Power TVS Diode, 824501101

Properties	Test conditions	Value	Unit	Tol.
DC Operating Voltage	V_{DC}	10	V	max.
(Reverse) Breakdown Voltage	V_{BR} 1 mA	11.7	V	±5%
Clamping Voltage	V_{clamp} I_{PEAK}	17	V	max.
(Reverse) Peak Pulse Current	I_{peak} 10/1000 μ s	23.5	A	max.
Leakage Current	I_{leak} V_{DC}	10	μ A	max.
Steady State Power Dissipation	P_{Diss} $T_A = 50^\circ C$	3.3	W	max.
Power Dissipation	P_{Diss} 10/1000 μ s	400	W	max.
Polarity	Bidirectional			

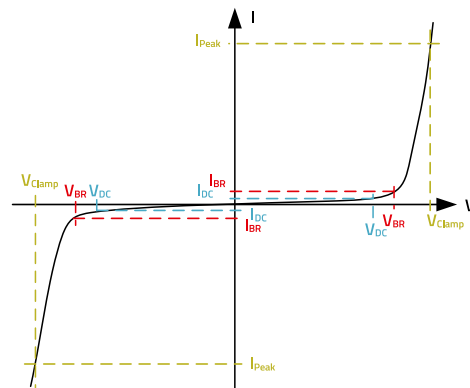


Figure 2: Graphs of unidirectional and bidirectional TVS diodes.

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DC operating voltage (V_{DC}), channel operating voltage (V_{CH})

The maximum operating peak voltage must not exceed V_{DC} . The TVS diode presents a high impedance to the protected circuit when the voltage across the diode is below this threshold value. Above this threshold, a high leakage current flows, which can lead to permanent failure of the TVS diode.

Reverse breakdown voltage (V_{BR})

This is the voltage threshold at which the TVS diode begins to conduct a defined current of 1 mA and is also referred to as the breakdown voltage. The value of V_{BR} , according to the datasheet, should be above the maximum operating voltage of the circuit to be protected, so that the TVS diode remains in a reverse-biased state under normal operating conditions of the device.

Limiting voltage, clamping voltage (V_{CLAMP})

The overvoltage transient is limited to the value defined by V_{CLAMP} , i.e., the maximum voltage that occurs in the protected circuit. The V_{CLAMP} voltage is defined for a specific peak pulse current (I_{PEAK}).

Peak pulse current (I_{PEAK})

This is the maximum surge current the TVS diode can withstand without damage. The peak pulse current is defined based on the transient waveform of the surge current, which is typically specified as 8/20 μ s in most industrial applications, where 8 μ s is the rise time (t_1) to the peak value and 20 μ s is the pulse duration until the current drops to 50% of the peak value (t_2).

Leakage current (I_{LEAK})

The leakage current is measured at V_{DC} and is the residual current that flows in the reverse direction.

Power dissipation (P_{DISS})

The power dissipation P_{DISS} indicates how much power the diode can absorb. A distinction is made between peak pulse power dissipation and the steady-state power dissipation.

Peak pulse power dissipation

The maximum peak power the TVS diode can dissipate during a transient event for a defined pulse waveform, in this case for the 10/1000 μ s pulse (10 μ s rise time, 1000 μ s decay to half amplitude).

Steady-state power dissipation:

The power the TVS diode can continuously absorb under normal operating conditions.

Ultra-low capacitance TVS diodes

There is a family of TVS diodes referred to as an ultra-low capacitance TVS diodes (or Super Speed Series, femtoF). They have a much lower capacitance than conventional TVS diodes, typically in the range of 0.1 to 0.5 pF, and are designed to protect high-speed data lines such as USB, HDMI, and Ethernet, as well as RF applications. The low capacitance is achieved by adding a forward-biased general-purpose diode in series with the TVS diode, which is usually reverse biased. The functional structure is illustrated in Figure 3.

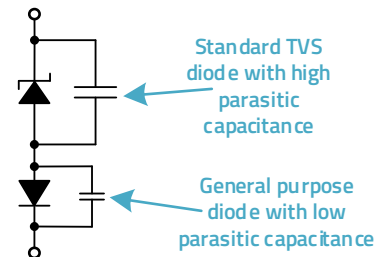


Figure 3: Functional structure of an ultra-low capacitance TVS diode.

Properties	Test Conditions		Value	Unit	Tol.
DC Operating Voltage		V_{DC}	6	V	max.
Capacitance	1 MHz	C_{typ}	0.05	pF	typ.
Capacitance	1 MHz	C_{max}	0.15	pF	max.
Leakage Current	6 V_{DC}	$I_{L,max}$	0.05	μ A	max.
Trigger Voltage	TLP measurement	V_{Tr}	250	V	typ.
Clamping Voltage	8 kV Contact, 30 ns	V_{Cl}	40	V	typ.
ESD Withstand	8 kV Contact		1000		min.

Table 1: Electrical characteristics of the "femtoF" TVS diode, 8231706A.

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2. TVS DIODES WITH "SNAPBACK" EFFECT

An ideal TVS diode completely blocks current, i.e., the current is zero when the input voltage is below the breakdown voltage. If the input voltage exceeds the breakdown voltage, the TVS diode ideally has a resistance close to zero, allowing the transient voltage to be effectively suppressed. A standard TVS diode clamps by beginning to conduct at a certain voltage and limiting the voltage drop across the diode. This diode exhibits a "non-ideal" behavior due to leakage currents and a finite low internal resistance (Figure 2).

A TVS diode can be realized by using a PN junction with a defined breakdown voltage. If a transient input voltage exceeds the breakdown voltage, current flows through the TVS diode to provide protection against transient voltages. However, the TVS type with a PN junction has no minority carriers and therefore exhibits poor clamping characteristics due to its high internal resistance. In semiconductor technology, there are alternative TVS implementations with bipolar NPN/PNP junctions in which a bipolar transistor provides the clamping property triggered by an avalanche effect. The base of the transistor is flooded with minority carriers, allowing the bipolar TVS to achieve a clamping voltage at a lower and constant level, as the avalanche current is increased by the transistor's bipolar gain from its base.

This type of "TVS diode" is based on the internal structure of MOSFET components and is significantly more complex than the circuit diagram of the TVS diode (Figure 1) suggests.

Every NMOS-FET contains a parasitic bipolar junction transistor (BJT) resulting from the configuration of the doped material. In normal operation of an NMOS component, the parasitic BJT does not take effect. As displayed in Figure 4, the BJT has the source as the emitter and the drain as the collector, and the underlying p-substrate can serve as the base of the BJT given the right conditions.

At this point, the "impact ionization" must be explained to further understand the function: A mobile electron or hole (positive charge carrier) moves under the influence of an electric field. In a weak electric field, it moves without changing the system. In a strong electric field, however, such as in a component with high voltage across its terminals, the mobile charge carrier encounters energetically bound charge carriers, which can then be liberated. These new charge carriers can, in turn, repeat the process, resulting in an avalanche current.

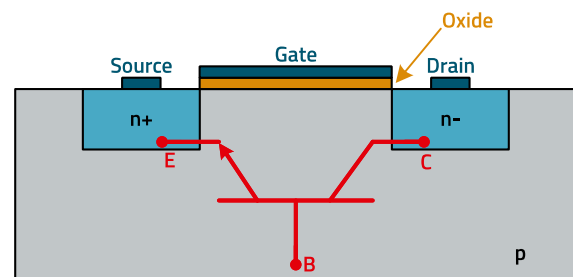


Figure 4: Parasitic bipolar junction transistor (BJT) in the NMOS FET.

When this avalanche current moves towards the base of the parasitic BJT, the base current can open the BJT and allow a large current to flow between the collector and emitter. The most interesting aspect of this is that after the component is opened, i.e., turned on, the high electric field that initiated the process is no longer necessary or even present to maintain the current. The conduction of current continues as the current increases, but at a much lower voltage between the emitter and collector. This phenomenon of triggering at a relatively high voltage and then falling back into conductivity at a lower voltage is known as snapback.

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High-bandwidth data and signal buses require multi-channel TVS diode arrays for ESD protection. Figure 5, for example, shows the circuit diagram of a two-channel transient protection on the left, and the functional circuit diagram of the TVS diode array on the right.

Figure 6 shows the cross-sectional view of the core of the four-channel array in the upper part, and its functional equivalent circuit diagram in the lower part. The TVS array includes a variety of high-side and low-side steering diodes connected in series, with the high-side steering diodes connected to V_{CC} and the low-side steering diodes connected to ground potential. In addition, these high-side and low-side

steering diodes are connected in parallel to a Zener main diode, the TVS diode (also see Figure 5). The steering diodes are much smaller and have a lower junction capacitance.

A p-WELL is a region within an n-type semiconductor substrate that is doped with p-type impurities. This creates a localized region of p-type material within the n-type substrate.

An n-WELL is a region within a p-type semiconductor substrate that is doped with n-type impurities. This creates a localized region of n-type material within the p-type substrate.

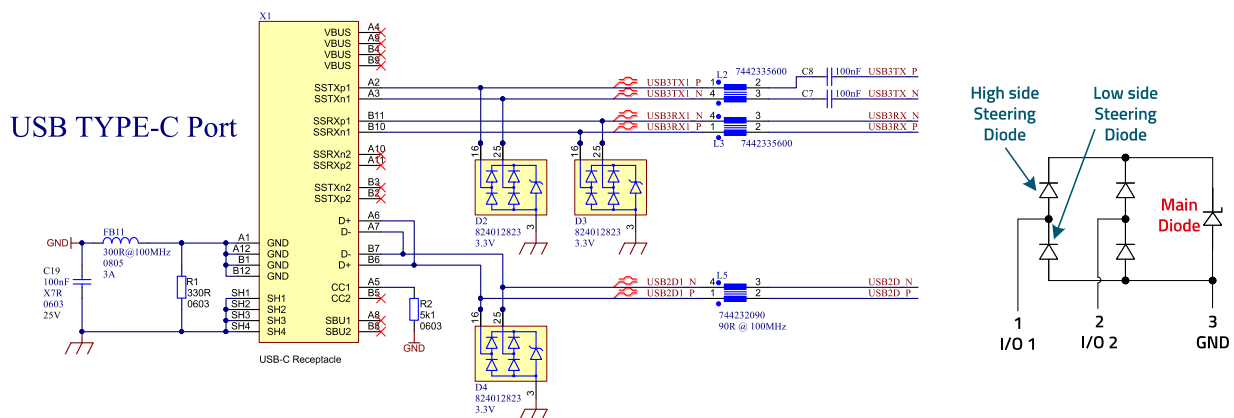


Figure 5: Transient protection at a USB interface with a TVS diode array.

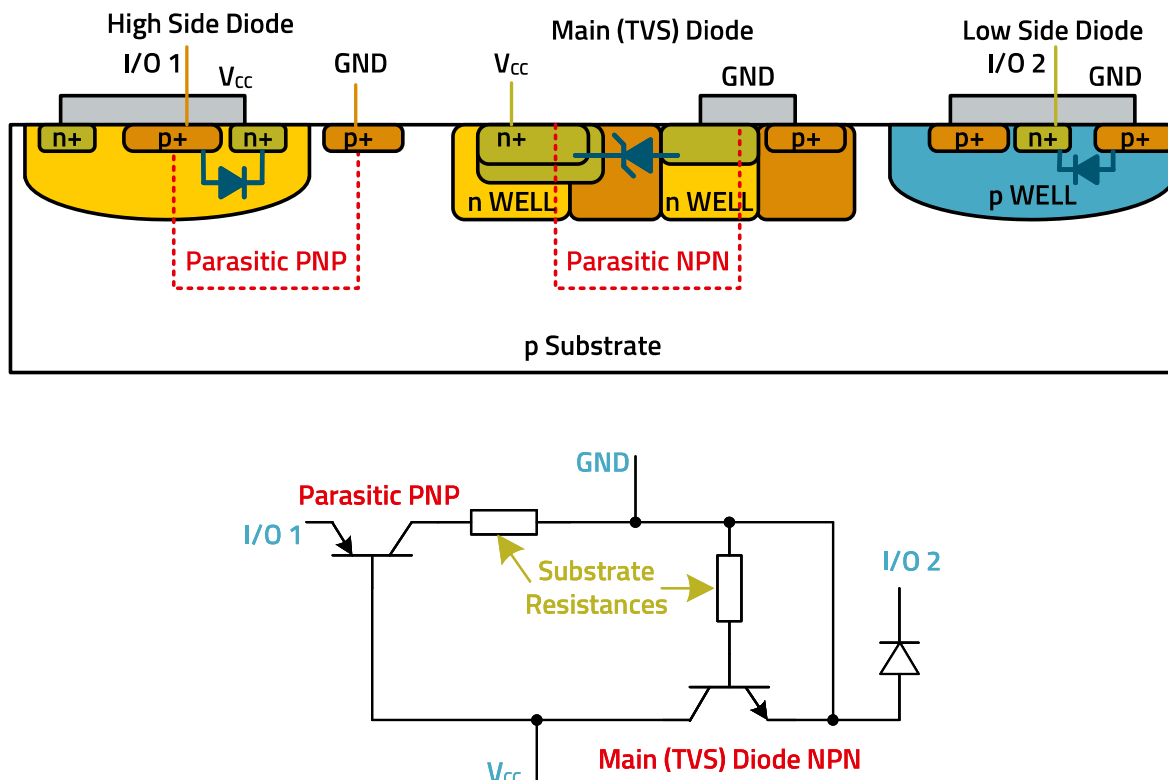


Figure 6: Cross-section of the core of a four-channel TVS diode array and its functional circuit diagram.

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In practice, implementing the function as shown Figure 6 proves to be challenging. Contemporary technologies for manufacturing a TVS array face the technical difficulty that in a TVS array – in which multiple PN junction diodes are created in a semiconductor substrate through the application of a standard CMOS processing step – there are inherent parasitic PNP and NPN transistors. When a transient voltage occurs, the parasitic NPN or PNP transistors of this TVS array are turned on and “locked”, causing a sudden and strong voltage rebound, known as the snapback effect, as already explained with the bipolar transistor (Figure 4). This effect arises between the source-body diode of a PMOSFET or NMOSFET, and an N+ in P-substrate junction, where a parasitic silicon-controlled rectifier (SCR) is formed as a parasitic component (Figure 7).

When the SCR is triggered, a strong current path is formed between the P+ region (anode, An) and the N+ region (cathode, Ca). This, in turn, leads to the clamping effect. Figure 8 shows the characteristic VI curves of different silicon components for

comparison: conventional semiconductor diode, NPN bipolar junction transistor (BJT), and SCR circuit.

The normal diode (Figure 8, left) undergoes Zener or avalanche breakdown at a specific voltage, known as the breakdown voltage V_{BR} . For diodes with a V_{BR} below 5.5 V, the ‘Zener breakdown’ predominates, whereas for diodes with a V_{BR} above 5.5 V, the avalanche breakdown (avalanche effect) predominates. Once the breakdown voltage is reached, the current increases sharply while the voltage remains relatively constant. There is no snapback effect. The diode can be damaged if the current is not limited. An NPN-BJT (Figure 8, middle) also undergoes avalanche breakdown in the collector-emitter region when the reverse voltage becomes too high. During breakdown, the collector current increases sharply, and the snapback effect occurs, in which the voltage at the collector suddenly drops as the current continues to rise. This can lead to the destruction of the transistor if the current is not controlled. An SCR (Figure 8, right) has a more complex breakdown mechanism due to its four semiconductor layers (p-n-p-n). The breakdown occurs

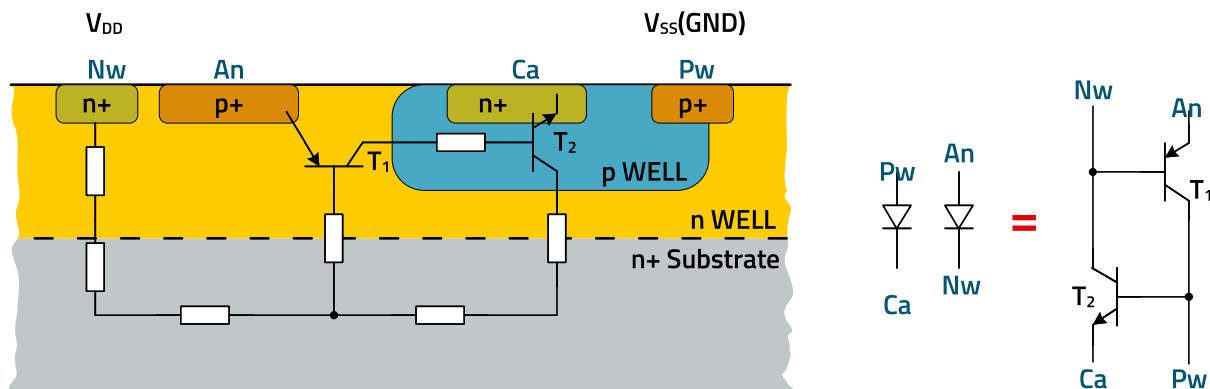


Figure 7: Schematic structure and equivalent symbols of an SCR in a CMOS process. The SCR is formed by the cross-coupled parasitic BJTs of the diodes.

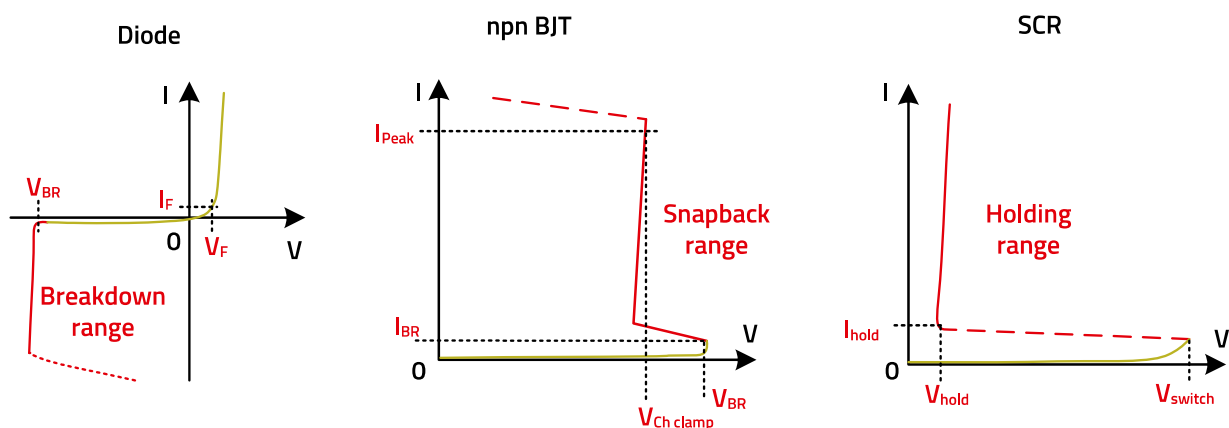


Figure 8: Comparison of the characteristic VI curves of different silicon components: conventional semiconductor diode, N-P-N bipolar junction transistor (BJT), and SCR circuit.

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when the voltage across the anode-cathode path reaches a critical threshold and the holding current is exceeded. After breakdown, the SCR can go into a conducting state and remains conductive even if the applied voltage decreases, until the current falls below the holding current, i.e., this also demonstrates the typical snapback effect, as with the BJT transistor. Figure 9 shows graphs of uni- and bidirectional TVS diodes with the snapback effect. For effective ESD protection, the trigger voltage should not be so high that it damages the circuit to be protected. Additionally, the lower holding voltage V_{hold} should be above the normal operating voltage of the circuit, which is ensured if the maximum operating voltage does not exceed V_{DC} or V_{Ch} . If the TVS diode is not correctly selected, there is a risk of 'latch-up'. The main reason for this is that when a transient overvoltage is coupled into a USB interface, for example, the voltage of the external overvoltage (ESD) is greater than the TVS breakdown voltage, which

causes the TVS diode to turn on. If the wrong type of TVS diode is used in the circuit to be protected, the lower holding voltage V_{hold} is lower than the normal operating voltage, and the TVS diode remains conductive even after the external interference has passed. In this case, the power supply is shorted, or the TVS diode may burn out, which, in the worst case leads to damage to the device. Similarly, at high temperatures, the SCR can be triggered by a high leakage current through the NP junction of the parasitic NPN BJT, which, in turn, leads to latch-up. The datasheet specifications should therefore be observed.

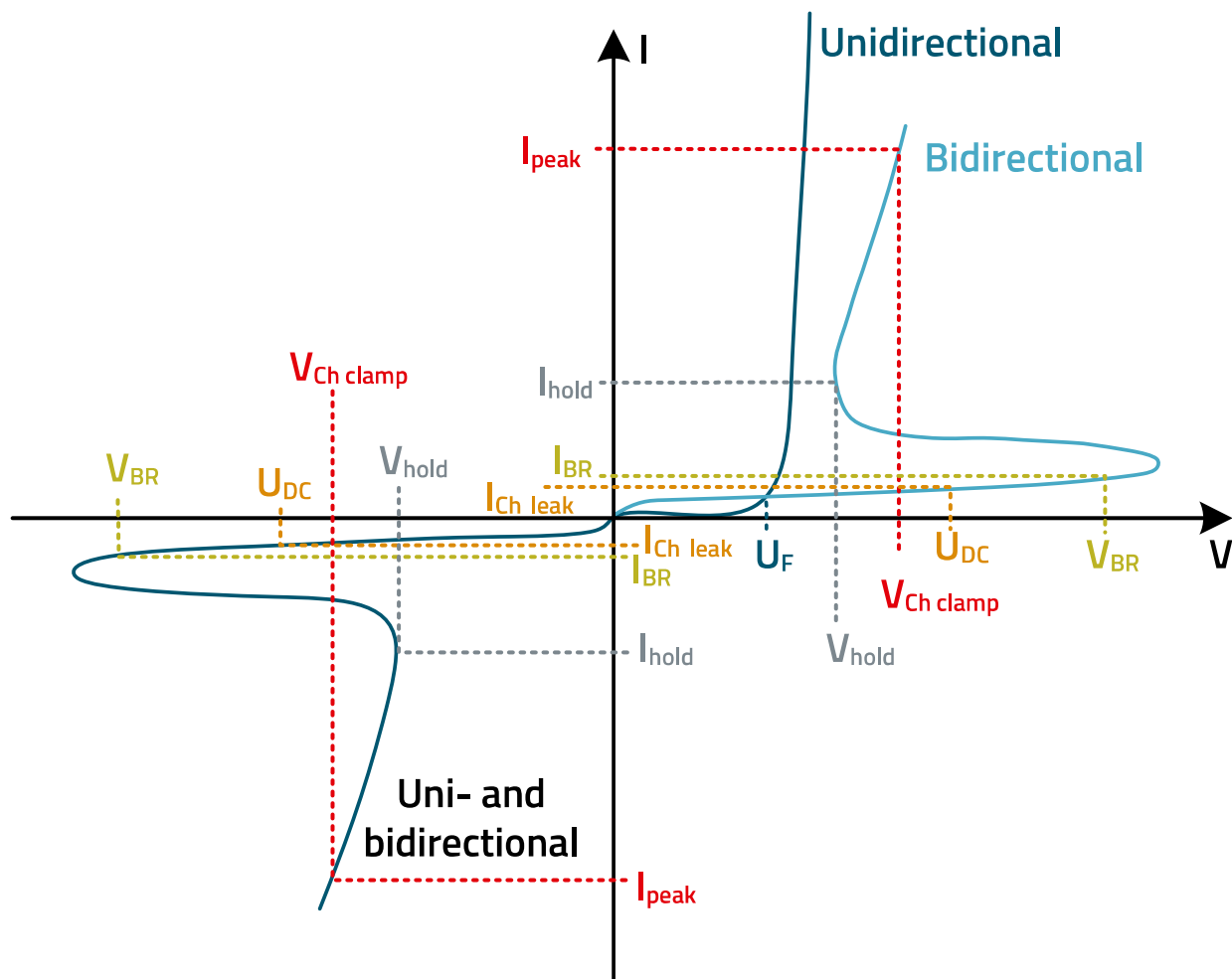


Figure 9: Characteristic VI curve of bidirectional TVS diodes with snapback effect.

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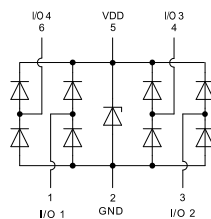
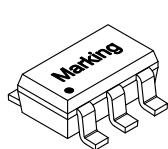
3. TVS DIODE HYBRID FOR SIGNAL AND DATA LINES

A voltage-limiting component must provide protection against transient events without impairing the normal operation of the circuit. This can be a challenge, as the parameters often work against each other. A TVS diode for high-frequency signal interfaces should have a low capacitance to avoid signal distortion due to capacitive load. However, the ability of a component to absorb energy depends on the size of the junction. The larger the junction, the more energy it can absorb. The downside is that as the size of the junction increases, and the capacitance of the component also increases. As shown in the first section, a common method to reduce the effective capacitance is the use of a low-capacitance diode circuit in conjunction with the TVS (Figure 3).

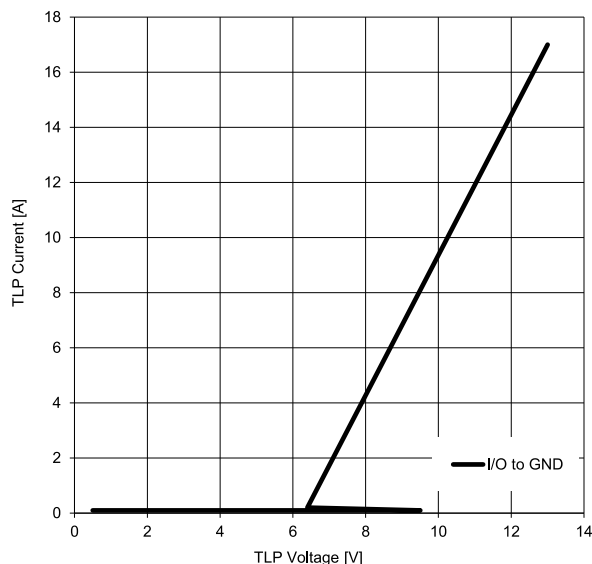
To protect multiple, symmetrical signal buses such as USB 3.1, multiple diode circuits are combined into an “array”.

Figure 10 shows an example. The VI curve was measured using the Transmission Line Pulsing (TLP) method to obtain the necessary signal rise time for determining the clamping voltage $V_{CH\text{ Clamp}}$. It is a common measurement method specified in IEC 62615:2010 and has become established to demonstrate the behavior of components under ESD conditions. The method guarantees precise and repeatable measurement.

The capacitance of the TVS diode is practically “hidden” from the circuit by the conventional diodes. The diodes must withstand the transient current and require a reverse breakdown voltage that is higher than the breakdown voltage of the TVS diode.



Transmission Line Pulsing (TLP) Measurement:



Electrical Properties:

Properties		Test conditions	Value			Unit	Tol.
			min.	typ.	max.		
Channel Operating Voltage	V_{CH}	I/O to GND			5	V	
DC Operating Voltage	V_{DC}	V_{DD} to GND	6			V	max.
(Reverse) Breakdown Voltage	V_{BR}	I/O to GND; $I_{BR}=1\text{ mA}$	6,1			V	
Leakage Current	I_{Leak}	V_{DD} to GND; $V_{DD}=V_{DC}$; $V_{GND}=0\text{ V}$	5			μA	max.
Channel (Reverse) Leakage Current	$I_{CH\text{ Leak}}$	I/O to GND $V_{DD}=V_{DC}$; $V_{I/O}=V_{DC}$; $V_{GND}=0\text{ V}$			1	μA	
Forward Voltage	V_F	GND to I/O; $I_F=15\text{ mA}$		0,7	1	V	
(Channel) Input Capacitance	C_{in}	I/O to GND $V_{DD}=5\text{ V}$; $V_{I/O}=2,5\text{ V}$; $V_{GND}=0\text{ V}$; $f=1\text{ MHz}$		1	1,5	pF	
Channel to Channel Input Capacitance	C_{Cross}	between I/O pins $V_{DD}=5\text{ V}$; $V_{I/O}=2,5\text{ V}$; $V_{GND}=0\text{ V}$; $f=1\text{ MHz}$		0,1	0,2	pF	
Channel ESD Clamping Voltage	$V_{CH\text{ Clamp ESD}}$	IEC 61000-4-2 +8 kV (TLP=16 A) Contact Mode, I/O to GND		13		V	
Channel Surge Clamping Voltage	$V_{CH\text{ Clamp}}$	I/O to GND 5 A, $t_b=8/20\text{ }\mu\text{s}$		7,8	8,5	V	
Polarity	Unidirectional						

Figure 10: Diode array with TVS diode for four channels, WE-TV5 High Speed Series, 824015.

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The resulting array is a component consisting of multiple functional regions. The integration and the resulting chassis ensure the required parameters for high-speed applications. For different applications, various IC groupings are available to achieve the required electrical parameters, making them easy to integrate into circuits. Typical schematic symbols are shown in Figure 11.

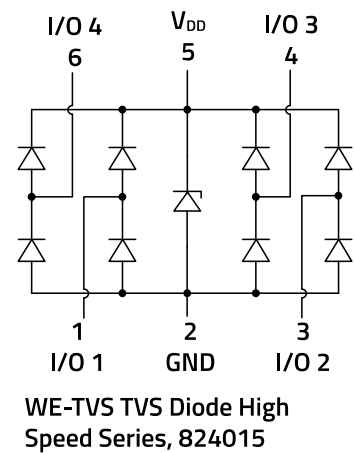
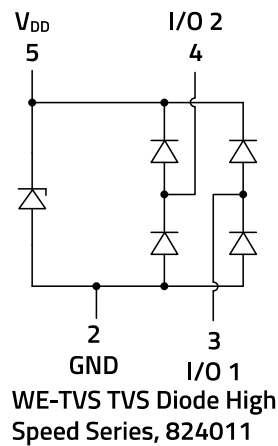
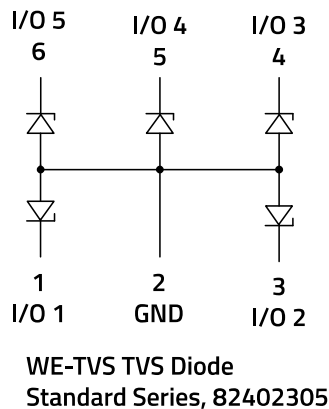
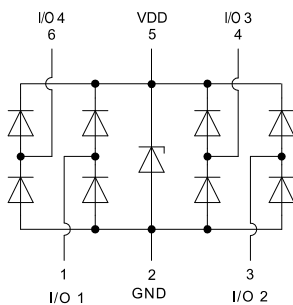
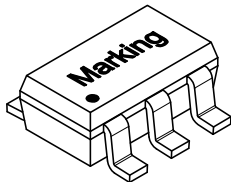


Figure 11: Different TVS diode arrays.



Electrical Properties:

Properties		Test conditions	Value			Unit	ToI.
			min.	typ.	max.		
Channel Operating Voltage	V_{ch}	I/O to GND			5	V	
DC Operating Voltage	V_{DC}	V_{DD} to GND	6			V	max.
(Reverse) Breakdown Voltage	V_{BR}	I/O to GND; $I_{BR}=1$ mA	6.1			V	
Leakage Current	I_{Leak}	V_{DD} to GND; $V_{DD}=V_{DC}$; $V_{GND}=0$ V	5			μ A	max.
Channel (Reverse) Leakage Current	$I_{Ch Leak}$	I/O to GND $V_{DD}=V_{DC}$; $V_{I/O}=V_{Ch}$; $V_{GND}=0$ V			1	μ A	
Forward Voltage	V_F	GND to I/O; $I_F=15$ mA		0.7	1	V	
(Channel) Input Capacitance	C_{Ch}	I/O to GND $V_{DD}=5$ V; $V_{I/O}=2.5$ V; $V_{GND}=0$ V; $f=1$ MHz		1	1.5	pF	
Channel to Channel Input Capacitance	C_{Cross}	between I/O pins $V_{DD}=5$ V; $V_{I/O}=2.5$ V; $V_{GND}=0$ V; $f=1$ MHz		0.1	0.2	pF	
Channel ESD Clamping Voltage	$V_{Ch Clamp ESD}$	IEC 61000-4-2 +8 kV (TLP=16 A) Contact Mode, I/O to GND		13		V	
Channel Surge Clamping Voltage	$V_{Ch Clamp}$	I/O to GND 5 A, $t_p = 8/20$ μ s		7.8	8.5	V	
Polarity	Unidirectional						

Figure 12: Schematic diagram and electrical parameters of the TVS diode array WE-TVS 824015.

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4.1 Clamping behavior of the TVS diode

This section explains the necessary conditions for safe and controlled clamping behavior. It shows the snapback effect and describes the behavior of the component when used in a deficient PCB design. The experimental setup for data acquisition is a lab setup that can be reconstructed in a well-equipped lab. The data provided in the component datasheet

was measured using a 'transmission line pulse generator', which offers high reproducibility and low error tolerance. To measure the clamping effect, the experimental lab setup displayed in Figure 13 was chosen. The measurement was taken using a 1.5 GHz active probe and a storage oscilloscope with a measurement bandwidth of 1 GHz to be in a position to display the fast processes.

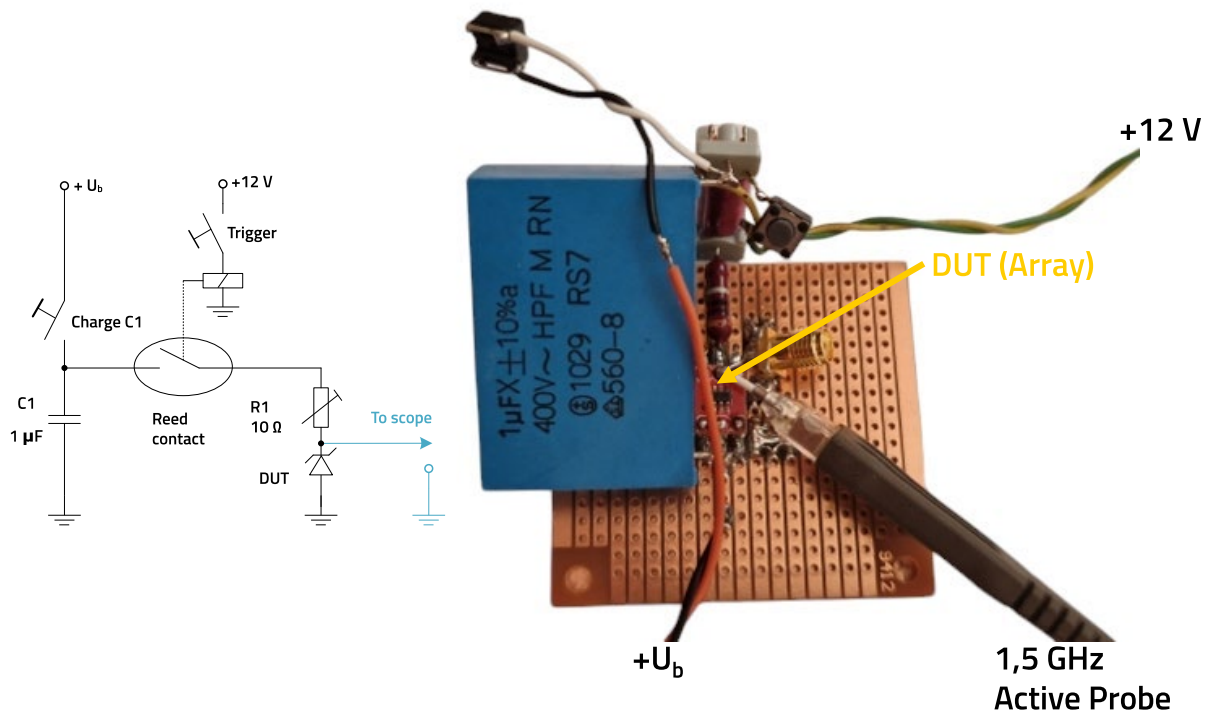


Figure 13: Setup for measuring the TVS diode clamping behavior.

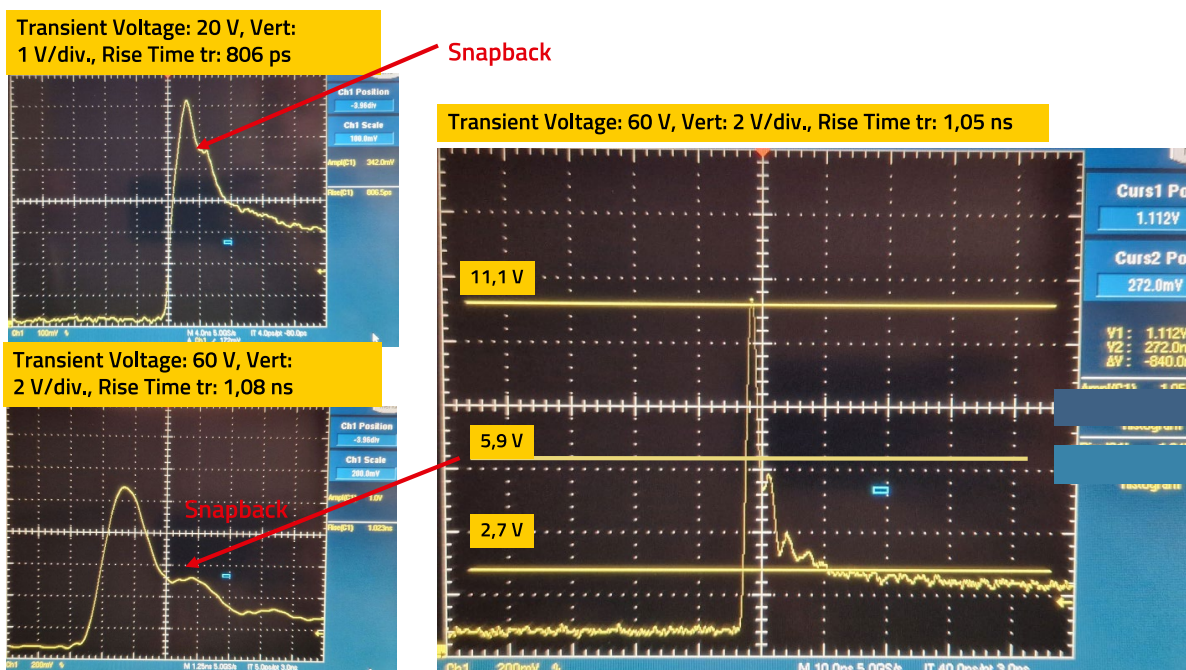


Figure 14: Clamping behavior of the TVS diode array.

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Besides the component-specific parameters, the clamping behavior depends very much on the setup. The main parameters here:

- Impedance and energy of the source, here the discharge capacitor C1
- Impedance of the lead from the energy source to the TVS diode, here defined by R1
- Impedance of the ground (GND), impedance between the energy source and the TVS diode

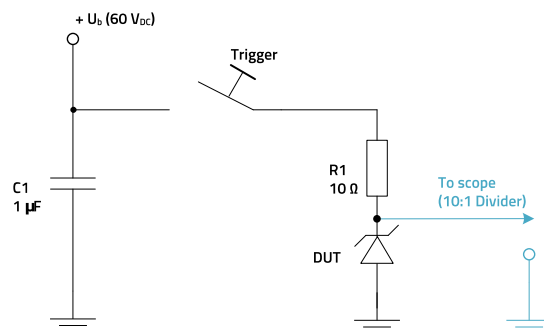
To carry out a defined discharge without switch bounce, a gas-filled reed relay was used in the setup, which was controlled by an auxiliary voltage. The measurement results are shown in the following images in Figure 14.

Upon applying a 60 V transient, the TVS diode used begins to conduct at approximately 11.2 V. The clamping voltage is observed as a ramp at around 5.9 V. The voltage in the circuit then gradually decreases as the capacitor voltage is disconnected by the relay.

(Figure 13).

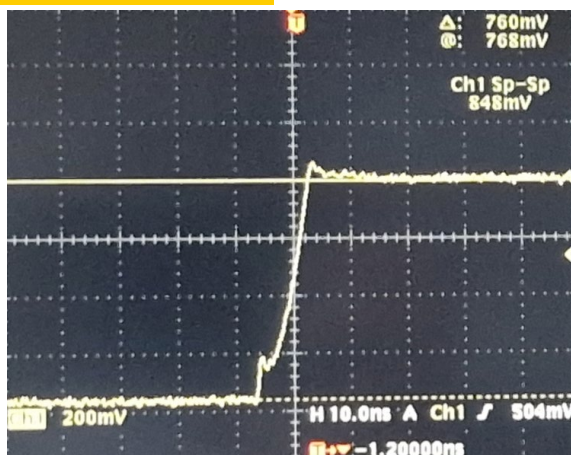
In Figure 15, the behavior of a conventional TVS diode is compared to the TVS diode of the array. The difference is clear: the conventional diode clamps without the snapback effect at around 8 V, while the TVS diode only begins to conduct at 7.7 V and then limits to approx. 5.8 V. Here there is no observable voltage decay because the capacitor remains connected.

In the theory section, it was described that the TVS diode itself is a complex structure of transistors, which causes the clamping effect through a mutual locking mechanism. This dynamic process includes a transition region of the VI curve, in which the slope of the characteristic curve and thus the resistance is negative. The snapback effect occurs when the voltage across the TVS diode drops to a lower value after breakdown, while the current continues to rise (Figure 9).



TVS Diode WE-TVSP 824500600

Divider 10:1, 2 V/div.



TVS-Diode Arrays WE-TVS 824015.

Divider 1:1, 1 V/div.

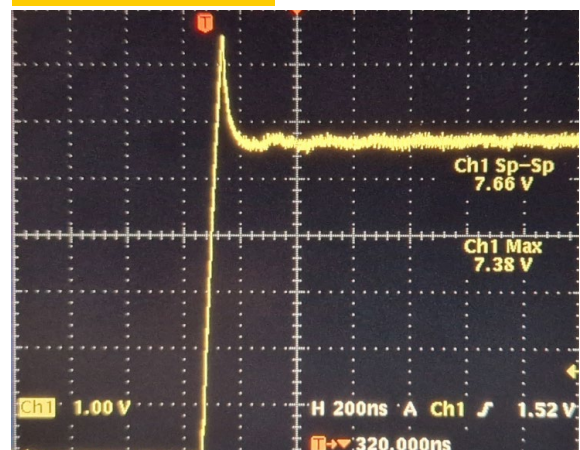


Figure 15: Clamping behavior of a conventional TVS diode, WE-TVSP 824500600, compared with the TVS element of the 824015 array.

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This means that in a certain range of the VI curve, an increase in current leads to a decrease in voltage, which is referred to as negative differential resistance. This suggests that oscillatory behavior may occur in the transition region, which can be rendered visible and possibly usable in circuit design. To

achieve this, it is necessary to pay more attention to the slope in the rise of voltage to be clamped, and here, in particular, the range around the breakdown voltage. A setup is chosen for this purpose that allows the current through the diode to be adjusted with a series resistor. The test setup and measurement results are displayed in Figure 16.

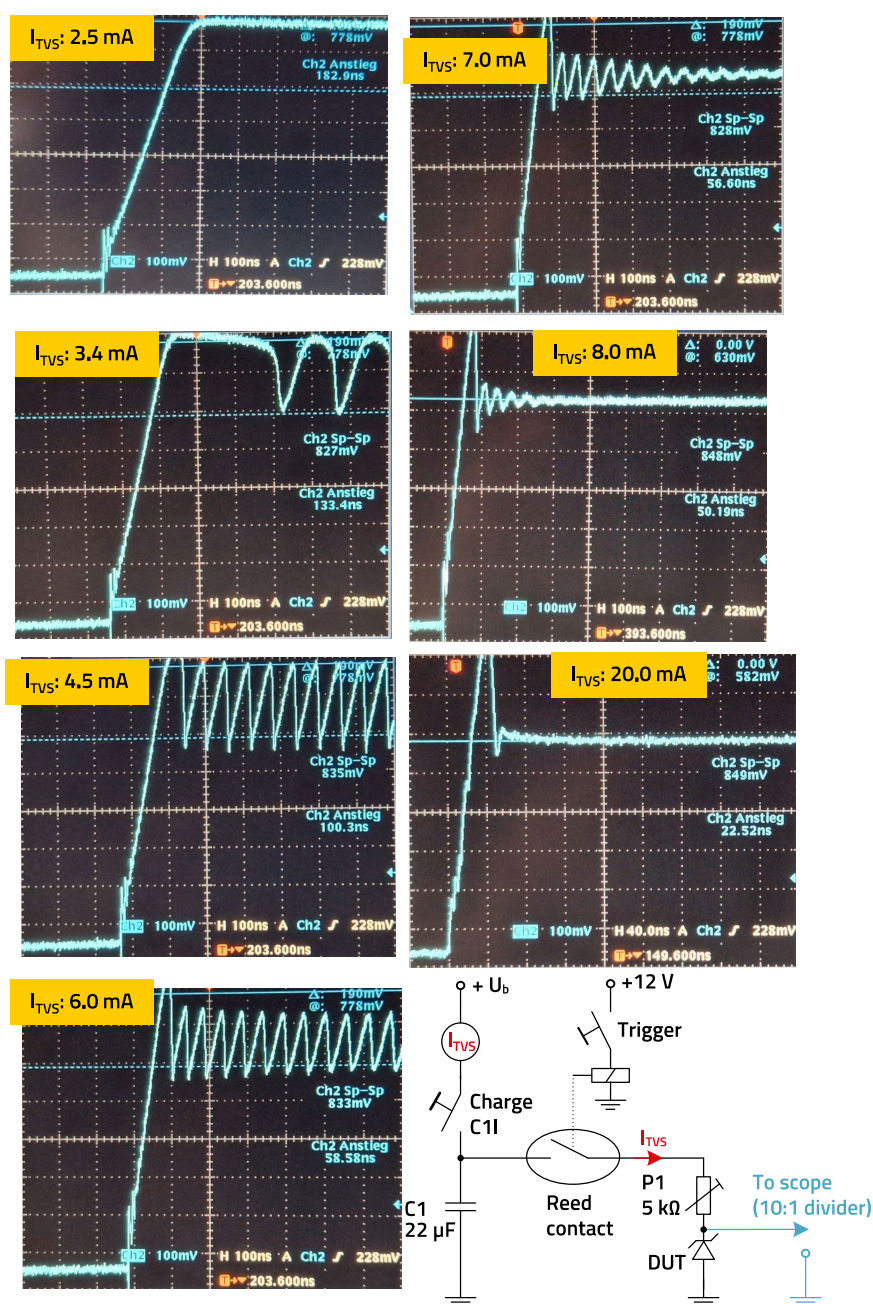


Figure 16: Test setup and behavior of the TVS element, displayed in the time domain.

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At a low clamping current of 2.5 mA, the element shows clamping behavior without the snapback effect. The voltage is limited to 7.8 V. Starting from 3.4 mA, the component begins to oscillate, reaching its maximum amplitude at around 4.5 mA and decaying with increasing current to around 8.0 mA. The snapback effect is observed from 4.5 mA; at higher currents above 10 mA, the component shows the expected voltage limiting effect without oscillation and with the snapback effect, as displayed in the graph with a current of 20 mA. It should also be mentioned that the onset of oscillation depends not only on the clamping current but also on the load, i.e., the impedance of the oscillating element. Figure 17 shows the oscillation in both the frequency and time domains. A series resistor of 3.3 k Ω was used in the circuit for these measurements. The frequency range of the fundamental oscillation lies between 1.5 and 12 MHz.

The oscillatory behavior starts at a current of approx. 2 mA; at 15 mA, the signal amplitude is significantly smaller, and above 20 mA the oscillation stops. Certainly, you could repurpose the array and use it as an oscillator. But what does this behavior of the component mean for its intended function as a voltage-limiting component? Under normal conditions, this low current range up to 20 mA is exceeded within a few nanoseconds when a transient interference signal occurs. However, if the rise time of the interference signal is short, the component may be stimulated into temporary oscillation. It can also become critical if there are longer-lasting interference spikes on a useful signal whose level is just above the breakdown voltage of the TVS element. This case is displayed in Figure 18. The breakdown voltage of the TVS diode would be set too low for this application.

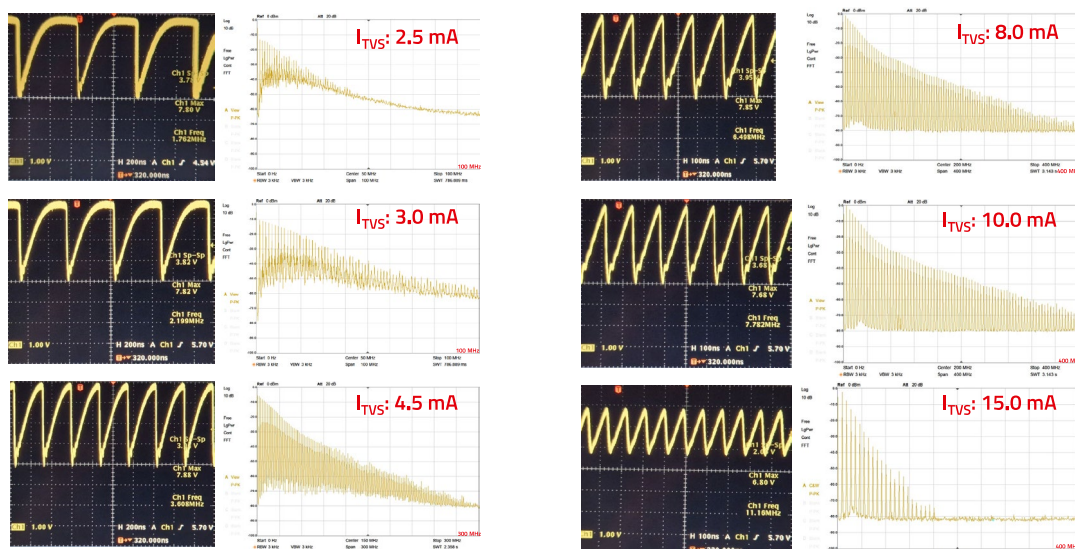


Figure 17: Oscillation of the TVS element as a function of the current I_{TVS} .

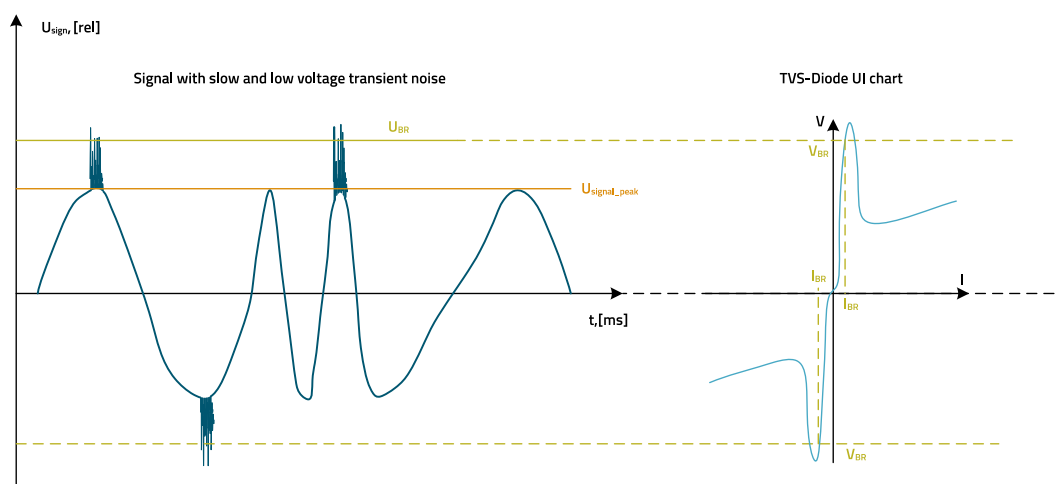


Figure 18: Interference signal on the useful signal with only a small amplitude.

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4.2 Signal behavior of the TVS diode array

The main use of TVS diode arrays is for protecting signal interfaces. When using these arrays, the signal properties should not be impaired if at all possible. Both the amplitude and frequency properties are important here. The frequency properties are mainly related to the system impedance and the parasitic capacitance of the array. The amplitude properties are therefore considered in more detail below, as they do not directly result from the functional circuit diagram, which is shown in various displays in Figure 19.

From the display of the steering diodes as a bridge rectifier shown in Figure 19 on the lower right, it can be seen that the maximum signal level between I/O 1 and I/O 2 depends on the

bias voltage between V_{DD} and GND. To determine the threshold value, the setup shown in Figure 20 was chosen. The signal voltage between I/O 1 and I/O 2 is not grounded, i.e., it is configured as a symmetrical signal and therefore has no ground reference to the power supply. Practical examples included USB, HDMI and Ethernet signals. The capacitor C1 decouples any DC voltage that may occur to protect the signal generator. R1 decouples the signal between the signal generator and the array for detecting distortion. The electrolytic capacitor C2 is the equivalent of the filter and back-up capacitor in real applications and short-circuits AC signals. R2 serves the load, i.e., for discharging the voltage when the voltage at the lab power supply is reduced.

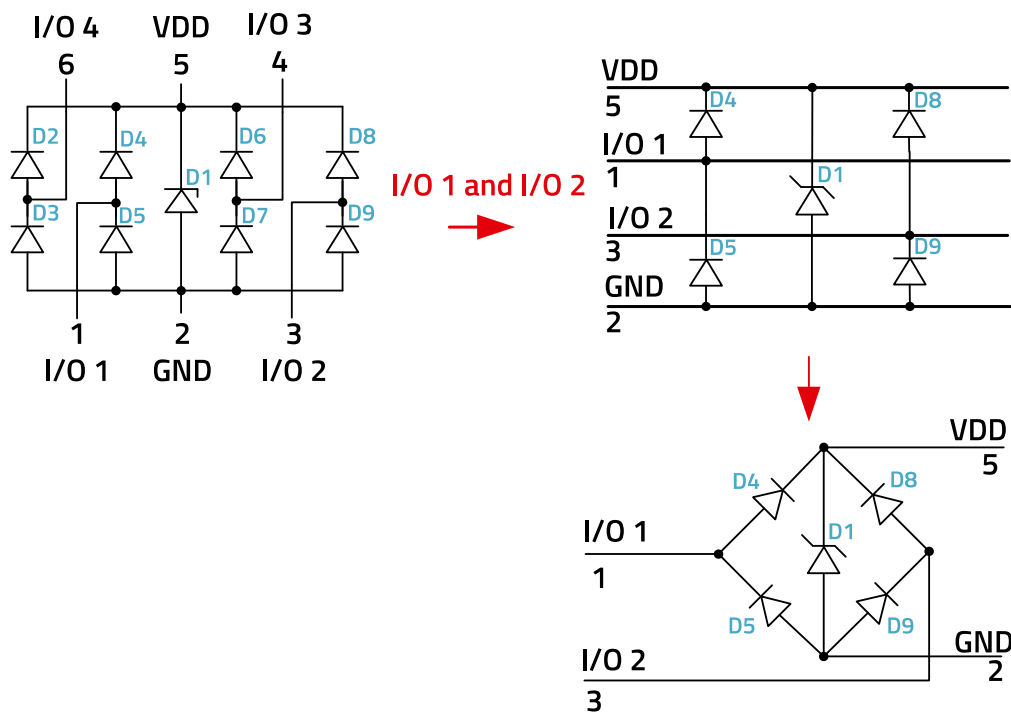


Figure 19: Different displays of two channels of the TVS diode array.

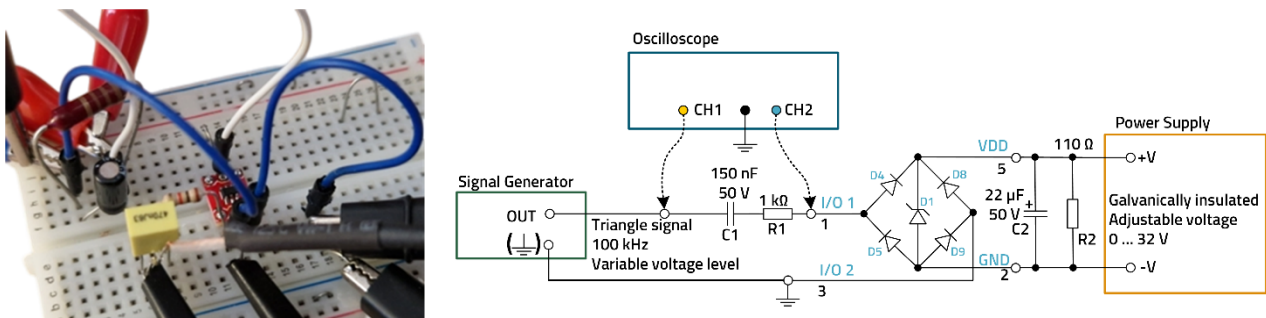
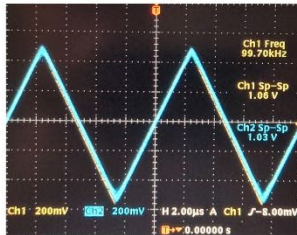


Figure 20: Setup for measuring the maximum input amplitude V_{PP} as a function of the bias voltage V_{DD} .

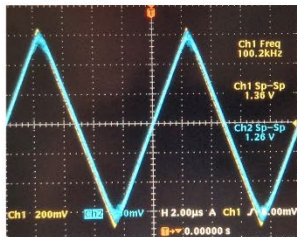
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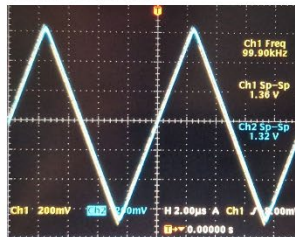
Input signal 1,0 V_{pp}, no Bias voltage
→ Input signal = Output signal



Input signal 1,35 V_{pp}, no Bias voltage
→ Beginning output signal distortion



Compensation of the distortion by
620 mV Bias voltage



Example of a strong distortion
Input: 2,5 V_{pp}, no Bias voltage

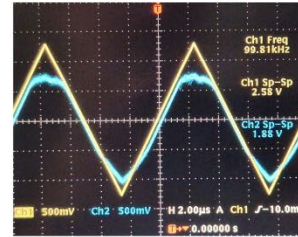


Figure 21: Examples of signal distortion as a function of the bias voltage.

By comparing the signals of the two channels CH1 and CH2, it is easy to determine the necessary bias voltage V_{DD} to avoid distortion by the array. It is shown that the dependence is not linear. Figure 21 displays examples of signal distortion as a function of the bias voltage.

It can be seen that the distortion range begins at approx. 1.3 V_{pp} signal amplitude. Amplitudes above this level require a bias voltage for the diodes between V_{DD} and GND (DC bias). The asymmetry in the last trace in Figure 21 results from the onset of forward current I_F of the TVS diode. The graph of the signal voltage as a function of the bias voltage is displayed in Figure 22.

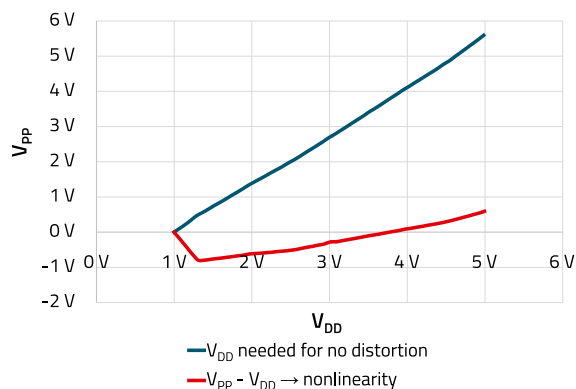


Figure 22: Graph of the signal voltage as a function of the bias voltage.

The blue curve shows the bias voltage V_{DD} required to achieve a distortion-free signal voltage V_{pp} . The progression is not linear, as can be seen from the red difference curve ($V_{pp} - V_{DD}$). In the signal level range just above 1.35 V_{pp}, only a low bias voltage is required to compensate for the distortion. As the signal voltage increases, the bias voltage must also increase, whereby the differential difference does not remain constant.

The non-linearity arises from the diode characteristic curve of the "steering diodes", and the diode characteristic curve is shown in Figure 23. It is apparent that the forward voltage range begins at approx. 0.8 V, i.e., according to Figure 20, for two steering diodes, a signal voltage of 1.6 V_{pp} will certainly affect the signal if the V_{DD} , according to the blue curve in Figure 22, is smaller than V_{pp} .

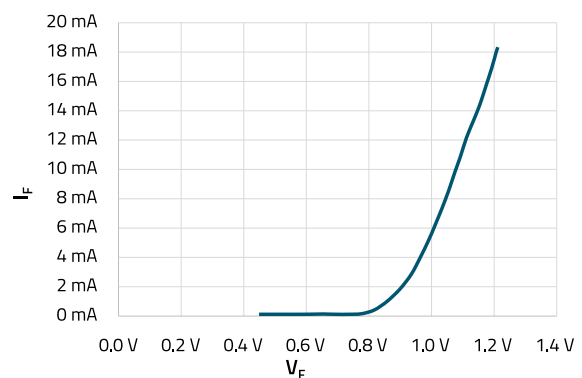


Figure 23: Diode characteristic curve of the "steering diodes".

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4.1 TVS diode array variations

The following section compares different arrays to demonstrate their function and potential applications. The lab setup with the associated circuit diagram is shown in Figure 24.

A 100 kHz triangular signal was input for the measurement, whose level is gradually increased. If the level was limited on one of the three channels, the DC voltage V_{CCa} was increased accordingly to apply an offset to the steering diodes. The following is an overview of the results with a brief explanation of the graphs in the "Remarks" column and a more detailed clarification at the end of the figure.

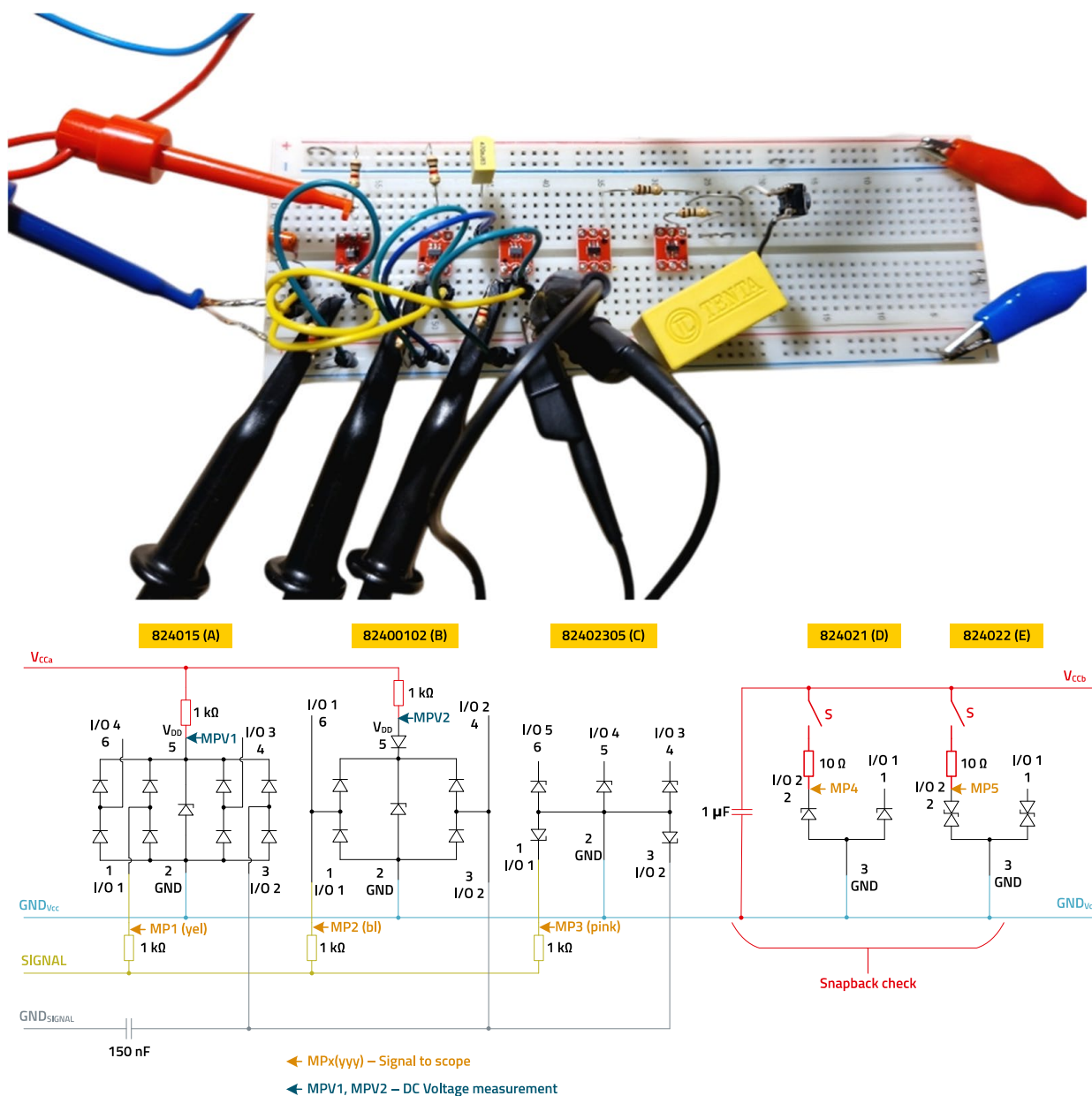


Figure 24: Lab setup with the associated circuit diagram for comparing different TVS diode arrays.

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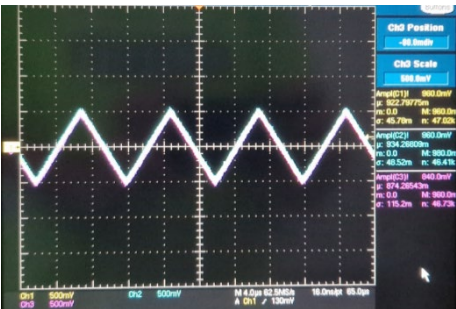
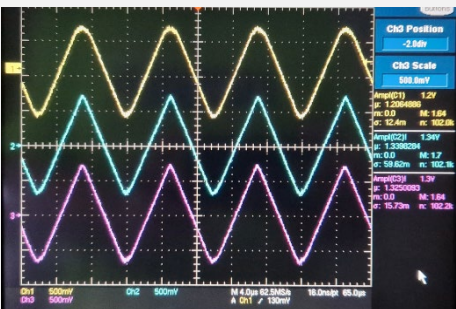
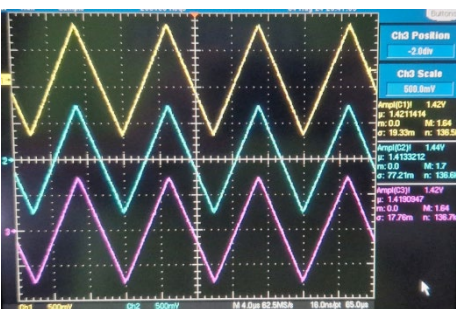
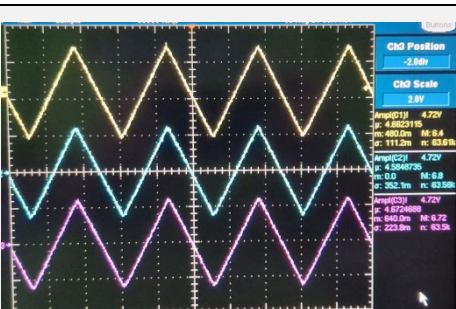
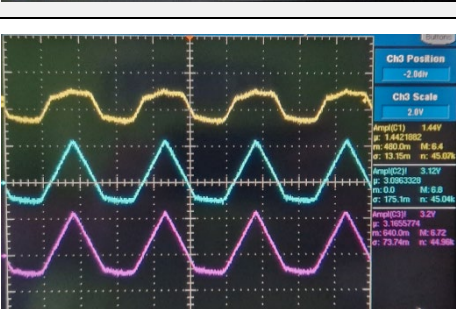
Signal amplitude [V _{ss}]	V _{CCa} [V _{DC}]	Trace	Remark
1.0	0		All three signals are undistorted; the signals here are displayed overlapping.
1.5	0		<ul style="list-style-type: none"> - 824015, limitation of both half-waves starting from 1.3 V_{ss} - all 3 arrays, starting from 1.5 V_{ss} neg. half-wave limitation
1.5	3.3		All three signals undistorted If V _{CCa} is increased to +5 V, the signal level can be increased to approx. 6.3 V _{ss} .
5.0	5.0		With a 5 V bias voltage, all three signals are undistorted at a level of 5.0 V _{ss} .
5.0	0		For positive signals, the two arrays 82400102 and 82402305 can be operated without bias voltage.

Figure 25: Comparison of the signal behavior of different TVS diode arrays, according to Figure 24, left part.

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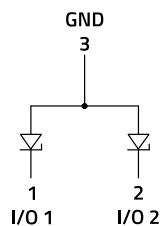
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The 824015 array limits the signal beyond the forward voltage of the steering diode, i.e., from about 0.7 V, corresponding to $2 \times 0.7 V_{SS}$ (2nd trace in Figure 25). A bias voltage gives the diode a voltage offset in the reverse direction, so the signal can be increased up to the offset voltage plus the forward voltage (3rd trace in Figure 25). In the bottom trace in Figure 25, the signal level for the 824015 array (yellow curve) exceeds the forward voltage of the steering diodes, so without bias, the level is limited to about $1.4 V_{PP}$. In contrast, for the 82400102 array (blue curve), the blocking diode to V_{DD} acts such that the signal is not limited in its positive half-cycle. The negative half-cycle, however, is limited by GND. For the 82402305 array (purple curve), the Zener breakdown voltage is not exceeded for the positive half-cycle and the negative half-cycle is limited to V_F via the connection to GND.

4.2 Practical guidance

The following measurements show the behavior of the two TVS diode arrays 824021 and 824022 (Figure 24, right part). The "transient voltage" in the setup was 100 V, the discharge was through a pre-charged $1.5 \mu\text{F}$ capacitor. The power supply leads to the arrays were intentionally kept long. The measurement result in Figure 26 shows the typical snapback effect, and the measurement also confirms the approx. 1 V lower clamping voltage of the bidirectional TVS diode in the 824022 array. A resonant decay of the voltage is observed due to the parasitic inductances of the power supply. Furthermore, the breakdown voltages V_{BR} of the two diodes are relatively high, ranging between 26 and 31 V.

WE-TVS TVS Diode 824021
Channel ESD clamping
voltage: 10 V typ.



WE-TVS TVS Diode 824022
Channel ESD clamping
voltage: 9 V typ.

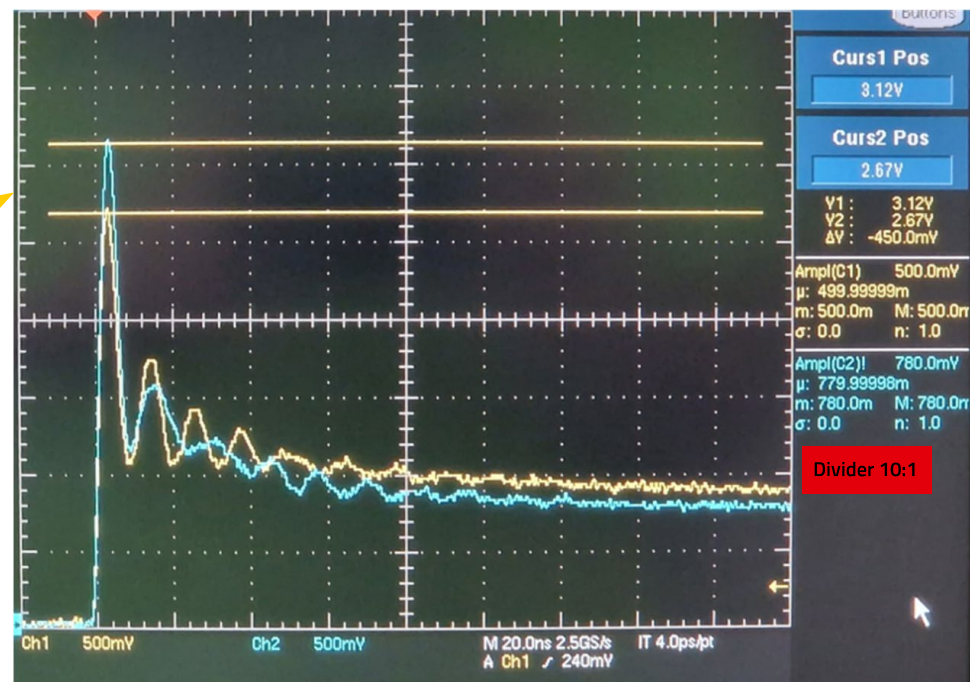
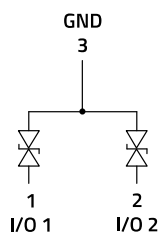


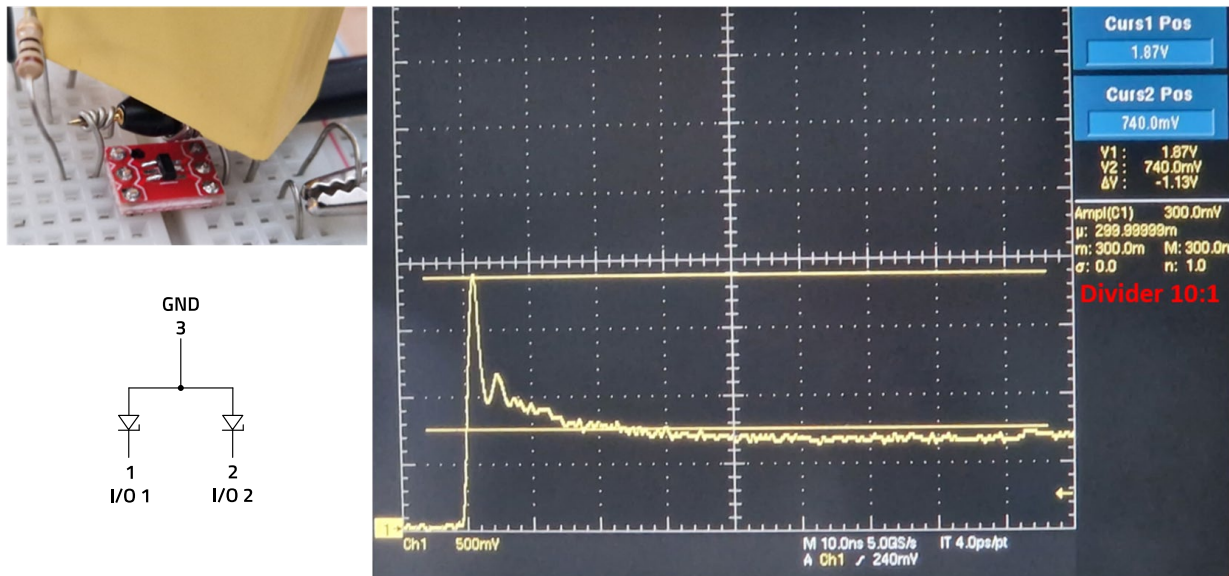
Figure 26: Clamping behavior of the two arrays according to Figure 24, right part.

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Here it is clear how important an RF-compatible design is, i.e., an RF-compatible layout in practice. The TVS diode must be integrated with low impedance in the current path in order to be effective. The following measurement was carried out under significantly better conditions. Figure 27 shows the test setup for the 824021 array with the corresponding measurement result. The breakdown voltage is now only 18.7 V and the clamping voltage is 7.4 V.

Finally, a practical application is shown. Figure 28 displays the circuit diagram of a USB 3.1 interface. The signal lines are protected against transient overvoltage by TVS diode arrays. The reference ground is the chassis, because the overvoltage, such as an electrostatic discharge, has the chassis or the earth as its ground reference.



WE-TVS TVS Diode 824021

Figure 27: Setup and results for measuring the breakdown and clamping voltage.

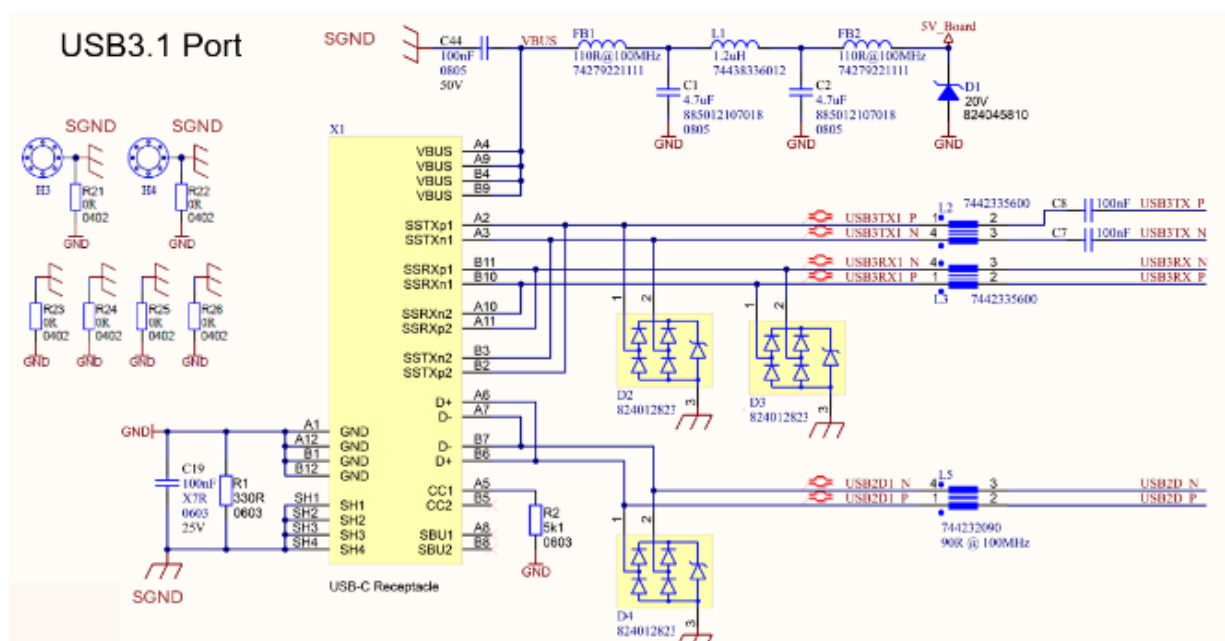


Figure 28: Circuit diagram of a USB 3.1 interface.

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Figure 29 shows the layout around the TVS diode arrays. The arrays are routed in the signal path, with the ground connection made directly to the SGND area to ensure the shortest possible ground connection.

SGND is the ground of the package, as displayed in Figure 29, left. The ground of the USB controller, which follows the inductors L2, L3, and L5, is "GND". The connection between SGND and GND is made through the components R21 – R26 in Figure 28, top left and R1, C19, C44 in Figure 29. For a detailed description, please refer to the reference designs RD016 and RD022, which can be downloaded from the website.

4.3 Other applications and circuit examples

The following section provides an overview of the various applications of TVS diodes and TVS diode arrays. For each application category, different circuits are presented to facilitate transfer to other applications.

4.5.1 Transient protection for DC inputs

In the following circuits, TVS diodes are used to limit overvoltage, whether caused by transient interference in terms of EMC or by "signal overvoltage".

4.5.1.1 Protection of rectifier diodes

The circuit in Figure 30 shows part of a power supply with a transformer and rectifier.

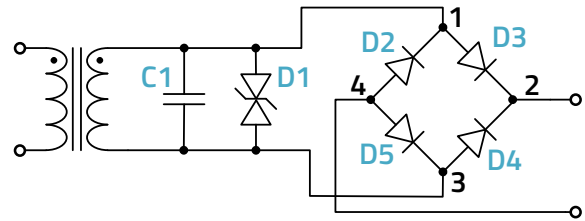


Figure 30: TVS diode for protecting rectifier diodes.

The bidirectional TVS diode D1 protects the rectifier diodes D2-D4 from transient differential overvoltage, i.e., common-mode transients are not limited here. The capacitor C1 attenuates low-energy high-frequency transient overvoltage, while the TVS diode limits the typical burst and surge transients. The circuit is useful where Schottky rectifier diodes with low forward voltage are used, as they generally also have a low maximum reverse voltage. C1 should typically be in the range 5 – 10 nF, and the clamping voltage of the TVS diode must, of course, be lower than the maximum reverse voltage of the Schottky diodes.

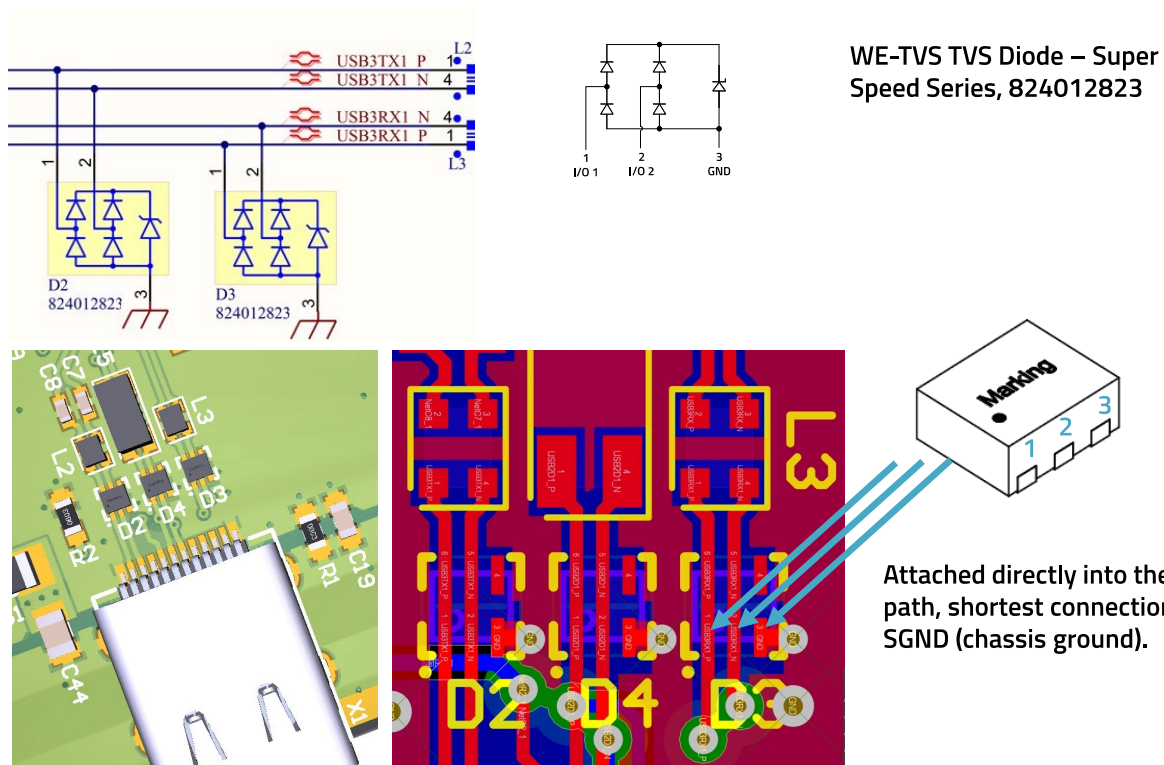


Figure 29: Layout of the USB 3.1 interface around the TVS diodes.

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4.5.1.2 Protection at the DC input of a device

The following circuit in Figure 31 shows a filter with transient protection for a DC input to power a device.

On the primary side of the common-mode inductor, the TVS diodes D22, D29, and the filter capacitors C106, C107 are connected to the chassis ground (SGND). The 824520241 TVS diodes have a breakdown voltage of 28.1 V and limit transient overvoltage that occurs in common mode. The capacitors, together with the current-compensated choke L13 and capacitors C108 and C109, form a π -filter for each current path (X4/1 and X4/2). The bidirectional TVS diode D1 limits differential overvoltage, which can be caused by the switching processes of inductive loads located in the nearby same circuit.

The clamping voltage of the diode must be below the maximum permissible input voltage of the downstream DC-DC controller. On the secondary side of inductor L13, at the transition between C109 / C2, the electronics ground and the chassis ground are connected. Figure 31 also shows the layout of the filter. It is clearly apparent that the TVS diodes are placed right at the interface input and are "looped" into the current path, i.e., directly into the trace lead, to prevent a current bypass. For more information, please refer to reference design RD041, which can be downloaded from the WE website.

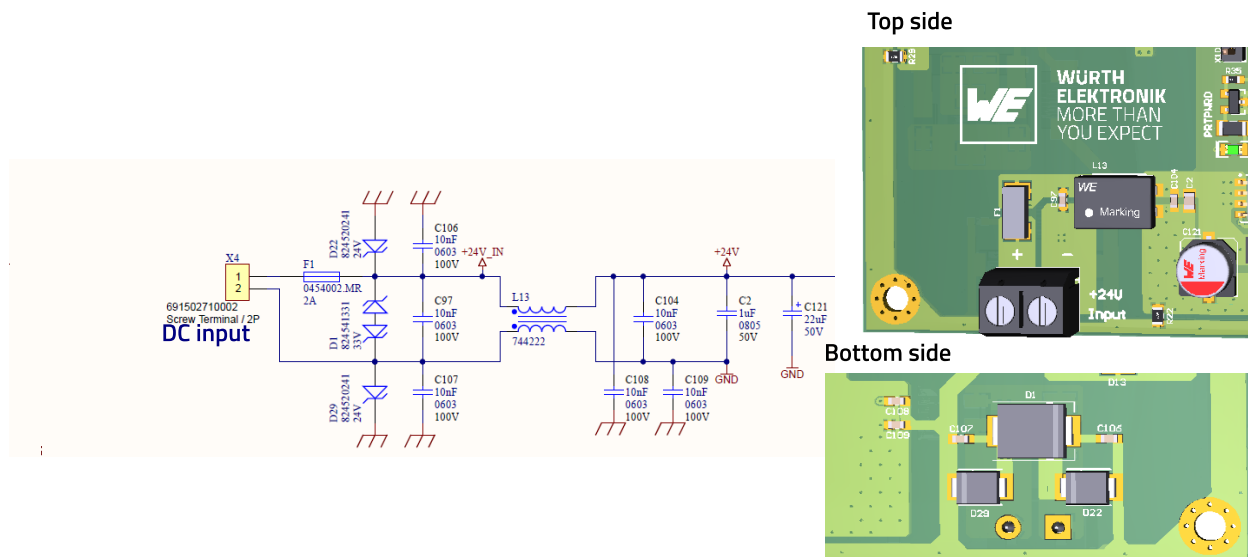


Figure 31: Protection at the DC input of a device.

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4.5.1.3 Protection at the measuring probe input of a device

The circuit in Figure 32 is an instrumentation amplifier as part of a measuring device. IN- and IN+ are the differential inputs for measuring the voltage in a system.

The voltage to be measured passes through the Wheatstone bridge to the non-inverting inputs of the OP amps. The bidirectional TVS diodes limit transient voltages against the primary ground (S_GND, chassis), which here also serves as the reference ground for common-mode interference.

The diodes clamp at 10.3 V and have a parasitic capacitance of typically > 1 nF, which, along with the bridge resistors, forms a low-pass filter at the input of the OP amps. If high differential overvoltages are expected, an additional bidirectional TVS diode can be installed in place of C1; J4 is then replaced with a wire bridge.

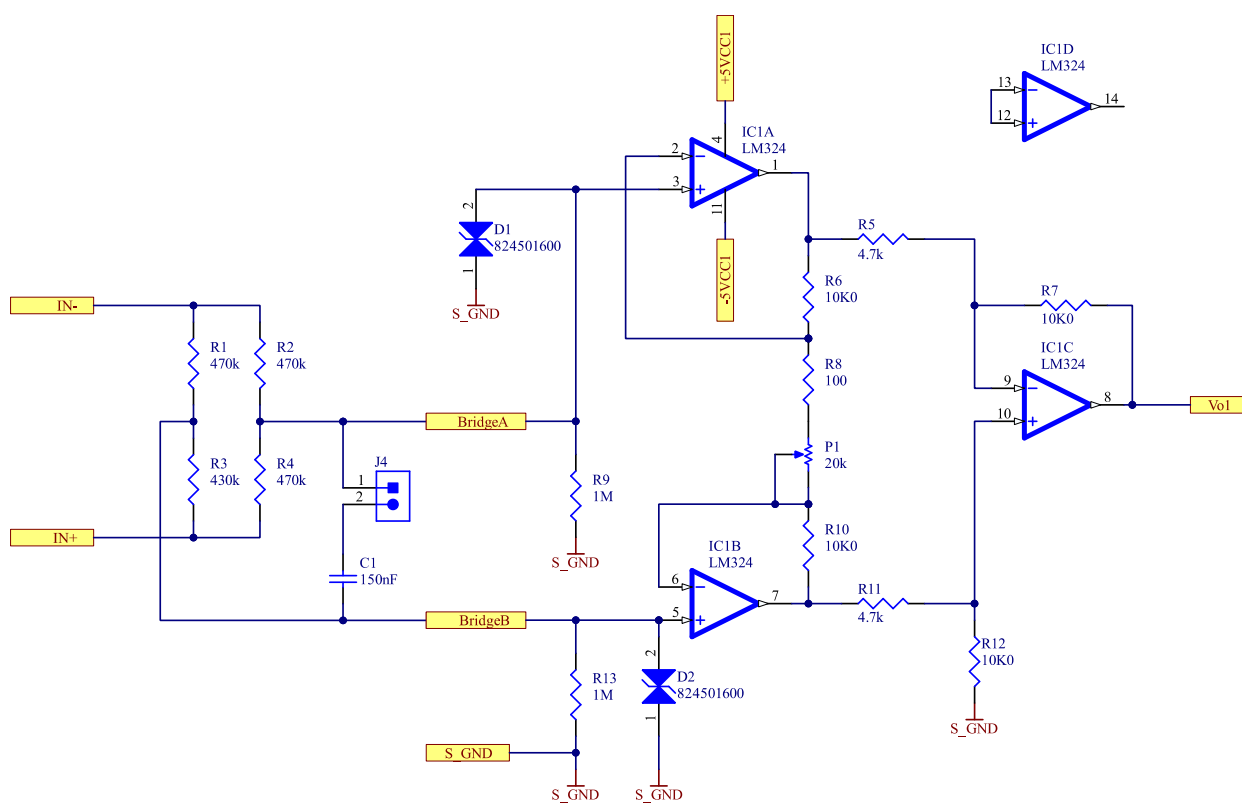


Figure 32: Protection at the measuring probe input of a device.

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4.5.2 Protection of an HDMI interface

The HDMI interface is now an important standard for many electronic devices. To reduce the risk of ESD damage to the HDMI connectors, manufacturers not only conduct tests on the plug or chassis, but also perform direct pin discharge to improve ESD robustness. To minimize signal distortion, the transmission channels D0, D1, D2, and CLK must be impedance-matched, and the TVS diodes for ESD protection must have a low parasitic capacitance.

The traces between the TVS diode and the line to be protected, as well as between the diode and the ground plane, must also be as short as possible to minimize the influence of inductance on the clamping voltage, because the parasitic inductance of the trace adds an additional voltage drop to the clamping voltage of the ESD protection device. Figure 33 shows the part of an HDMI interface with ESD protection.

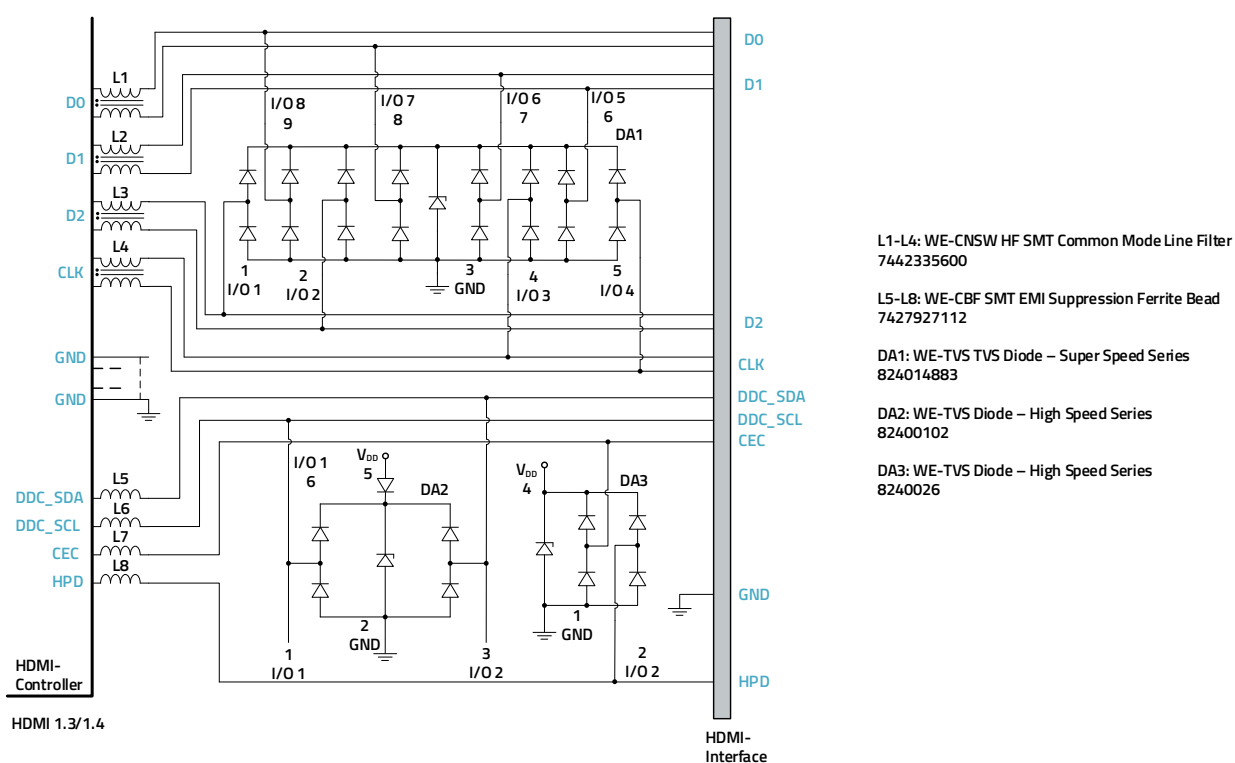


Figure 33: Section of the circuit diagram of an HDMI interface with ESD protection.

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Why is a TVS array (DA2) with an additional diode used in the DDC_SDA and DDC_SCL lines? If the HDMI sink is connected to the HDMI source (see Figure 34), a leakage current path can form through the protection diode of the TVS diode array at the source when the source is turned off (Figure 34, right), while the sink is in the boot state. This issue has been addressed in the TVS diode array 82400102 and effectively prevented by incorporating a backflow protection diode, as displayed in Figure 34.

5. FINAL REMARKS

This extensive Application Note explains in detail how TVS diodes are constructed, how they function, and the pros and cons of these components. The electrical parameters of these complex components must be taken into account in the application to ensure the desired protection against transient overvoltage is achieved. Furthermore, proper circuit design and layout are necessary to prevent parasitic effects from significantly impacting the function of the TVS diodes. Numerous examples show how the components can be used properly.

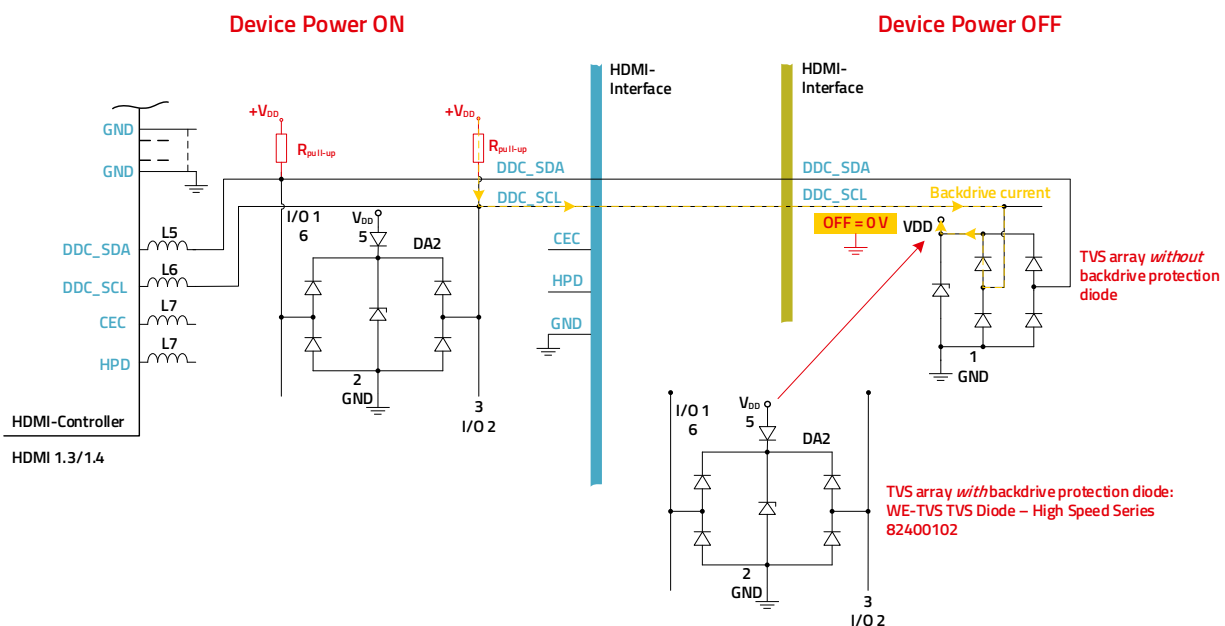


Figure 34: Excerpt from an HDMI interface system, display of the backflow current issue.

A APPENDIX

A.1 Literature

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Würth Elektronik eiSos GmbH & Co. KG

Max-Eyth-Str. 1 74638 Waldenburg Germany

www.we-online.com

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